# DS26LV31QML 3V Enhanced CMOS Quad Differential Line Driver

**Check for Samples: DS26LV31QML**

## FEATURES

- **Comparable to Both TIA/EIA-422 and ITU-T V.11 Standards.**
- **Interoperable with Existing 5V RS-422 Networks**
- **Low Quiescent Current**
- **Pin Compatible with DS26C31**

## DESCRIPTION

The DS26lV31 is a high-speed quad differential CMOS driver that is comparable to the TIA/EIA-422-B and ITU-T V.11 standards. The CMOS DS26LV31 features low static $I_{CC}$ of 125 µA Max which makes it ideal for battery powered and power conscious applications. Differential outputs have the same $V_{OD}$ specification (≥2V) as the 5V version. The EN and $\overline{EN}$ inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. Protection diodes protect all the driver inputs against electrostatic discharge. The driver and enable inputs (DI, EN, $\overline{EN}$) are compatible with low voltage LVTTL and LVCMOS devices.

## Connection Diagram

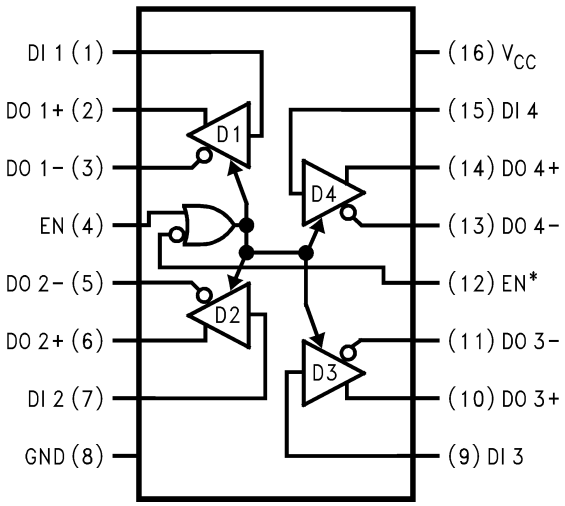


**Figure 1. CLGA Package- Top View**
**See Package Number NAD0016A**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings (1)(2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | -0.5V to 7.0V |
| DC Input Voltage ($V_I$) | -0.5V to $V_{CC}$+0.5V |
| DC Output Voltage ($V_O$) Power off | -0.5V to 7V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20mA |
| DC Output Current, per Pin ($I_O$) | ±150mA |
| Storage Temperature Range ($T_{Stg}$) | -65°C ≤ $T_A$ ≤ +150°C |
| Lead Temperature ($T_L$) Soldering, 4 seconds | 260°C |
| Maximum Power Dissipation +25°C (3) | 1119mW |
| Thermal Resistance | |
| $\theta_{JA}$ | 134°C/W |
| $\theta_{JC}$ | 12.5°C/W |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not verify specific performance limits. For verified specifications and test conditions, see the Electrical Characteristics. The verified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.
(3) Derate W package 7.5mW/°C above +25°C.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($v_{CC}$) | 3.0V to 3.6V |
| DC input or Output Voltage ($V_I$, $V_O$) | 0V to $V_{CC}$ |
| Operating Temperature Range ($T_A$) | −55°C ≤ $T_A$ ≤ +125°C |

**Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A**

| Subgroup | Description | Temp °C |
|---|---|---|
| 1 | Static tests at | 25 |
| 2 | Static tests at | 125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | 25 |
| 5 | Dynamic tests at | 125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | 25 |
| 8A | Functional tests at | 125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | 25 |
| 10 | Switching tests at | 125 |
| 11 | Switching tests at | -55 |
| 12 | Settling time at | 25 |
| 13 | Settling time at | 125 |
| 14 | Settling time at | -55 |

## DS26LV31M Electrical Characteristics DC Parameters

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Logical "1" Input Voltage | | (1) | 2.0 | | V | 1, 2, 3 |
| $V_{IL}$ | Logical "0" Input Voltage | | (1) | | 0.8 | V | 1, 2, 3 |
| $V_{OD1}$ | Differential Output Voltage | $R_L$ = No Load, $V_{CC}$ = 3.0/3.6V | (2) | | 4.0 | V | 1, 2, 3 |
| $V_{OD2}$ | Differential Output Voltage | $R_L$ = 100Ω, $V_{CC}$ = 3.0/3.6V | (2) | 2.0 | | V | 1, 2, 3 |
| $V_{OD2}$-$\overline{V_{OD2}}$ | Difference in Differential Output | $R_L$ = 100Ω, $V_{CC}$ = 3.0/3.6V | (2) | -0.4 | 0.4 | V | 1, 2, 3 |
| $V_{OD3}$ | Differential Output Voltage | $R_L$ = 3900Ω, $V_{CC}$ = 3.0/3.6V | (2) | | 3.6 | V | 1, 2, 3 |
| $V_{OC}$ | Common Mode Output Voltage | $R_L$ = 100Ω, $V_{CC}$ = 3.0/3.6V | (2) | | 2.0 | V | 1, 2, 3 |
| $V_{OC}$-$\overline{V_{OC}}$ | Difference in Common Mode Output | $R_L$ = 100Ω, $V_{CC}$ = 3.0/3.6V | (2) | -0.4 | 0.4 | V | 1, 2, 3 |
| $I_{IL}$ | Low Level Input Current | $V_I$ = Gnd, $V_{CC}$ = 3.6V | | -10 | | µA | 1, 2, 3 |
| $I_{IH}$ | High Level Input Current | $V_I$ = $V_{CC}$, $V_{CC}$ = 3.6V | | | 10 | µA | 1, 2, 3 |
| $V_{CL}$ | Input Clamp Voltage | $I_I$ = -18mA, $V_{CC}$ = 3.0V | | | -1.5 | V | 1, 2, 3 |
| $I_{CC}$ | Quiescent Power Supply Current | $I_O$ = 0uA, $V_I$ = $V_{CC}$ or Gnd, $V_{CC}$ = 3.6V | | | 125 | µA | 1, 2, 3 |
| $I_{OZ}$ | TRI-STATE Output Leakage Current | $V_O$ = $V_{CC}$ or Gnd, Enable = Vil, $V_{CC}$ = 3.6V, $\overline{Enable}$ = $V_{IH}$ | | | ±20 | µA | 1, 2, 3 |
| $I_{SC}$ | Output Short Circuit Current | $V_I$ = $V_{CC}$ or Gnd, $V_{CC}$ = 3.0/3.6V, $V_O$ = 0.0V | (2), (3) | -30 | -160 | mA | 1, 2, 3 |
| $I_{Off}$ | Output Leakage Current "Power Off" | $V_{CC}$ = 0V, $V_O$ = 6.0V or 3.0V | | | 100 | µA | 1, 2, 3 |
| | | $V_{CC}$ = 0V, $V_O$ = -0.25V | | | -200 | µA | 1, 2, 3 |

(1) Parameter tested Go-No-Go only.
(2) See EIA specification RS-422 for exact test condition.
(3) This is a current sourced when a high output is shorted to Gnd. Only one output at a time should be shorted.

## DS26LV31M Electrical Characteristics AC Parameters - Propagation Delay Time

The following conditions apply to all the following parameters, unless otherwise specified. AC: $V_{CC}$ = 3.0/3.6V

| Parameter | | Test Conditions | Notes | Min | Max | Units | Sub-groups |
|---|---|---|---|---|---|---|---|
| $t_{PLHD}$ | Differential Propagation Delay (Low to High) | $R_L$ = 100Ω, $C_L$ = 50pF | (1) | 5.0 | 25 | ns | 9, 10, 11 |
| $t_{PHLD}$ | Differential Propagation Delay (High to Low) | $R_L$ = 100Ω, $C_L$ = 50pF | (1) | 5.0 | 25 | ns | 9, 10, 11 |
| $t_{SKD}$ | Differential Skew $t_{PHLD}$-$t_{PLHD}$ (same channel) | $R_L$ = 100Ω, $C_L$ = 50pF | (1) | | 5.0 | ns | 9, 10, 11 |
| $t_{SK1}$ | Pin to Pin Skew (same device) | $R_L$ = 100Ω, $C_L$ = 50pF | (1) | | 5.0 | ns | 9, 10, 11 |
| $t_{PZH}$ | Output Enable Time | $R_L$ = 110Ω to Gnd, $C_L$ = 50pF | (2) | | 40 | ns | 9, 10, 11 |
| $t_{PZL}$ | Output Enable Time | $R_L$ = 110Ω to $V_{CC}$, $C_L$ = 50pF | (2) | | 40 | ns | 9, 10, 11 |
| $t_{PHZ}$ | Output Disable Time | $R_L$ = 110Ω to Gnd, $C_L$ = 50pF | (2) | | 35 | ns | 9, 10, 11 |
| $t_{PLZ}$ | Output Disable Time | $R_L$ = 110Ω to $V_{CC}$, $C_L$ = 50pF | (2) | | 35 | ns | 9, 10, 11 |

(1) Generator waveform is specified as follows: $f$ = 1MHz, Duty Cycle = 50%, $Z_O$ = 50Ω, $t_R$ = $t_F$ ≤ 6nS. Driver input = 0V to 3V with measure points equal to 1.5V. Differential output $V_{Diff}$ = $D_O$ - $\overline{D^O}$ with measure point equal to 0V.
(2) Generator waveform is specified as follows: $f$ = 1MHz, Duty Cycle = 50%, $Z_O$ = 50Ω, $t_R$ = $t_F$ ≤ 6nS. En/$\overline{En}$ inputs = 0V to 3V with measure points equal to 1.5V on the inputs, to 1.3V on the outputs for $Z_L$ and $Z_H$, and ($V_{OL}$ + 0.3V) for $L_Z$, and ($V_{OH}$.- 0.3V) for $H_Z$.

## REVISION HISTORY

| Released | Revision | Section | Originator | Changes |
|---|---|---|---|---|
| 3/01/06 | * | New Release, Corporate format | L. Lytle | 1 MDS data sheets converted into one Corp. data sheet format. MNDS26LV31-X Rev 1A0 will be archived. |
| 4/15/2013 | A | | TIS | Changed layout of National Data Sheet to TI format |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9858401QFA | ACTIVE | CFP | NAD | 16 | 19 | TBD | Call TI | Call TI | -55 to 125 | DS26LV31W-<br>QML Q<br>5962-98584<br>01QFA ACO<br>01QFA >T | Samples |
| DS26LV31W-QML | ACTIVE | CFP | NAD | 16 | 19 | TBD | Call TI | Call TI | -55 to 125 | DS26LV31W-<br>QML Q<br>5962-98584<br>01QFA ACO<br>01QFA >T | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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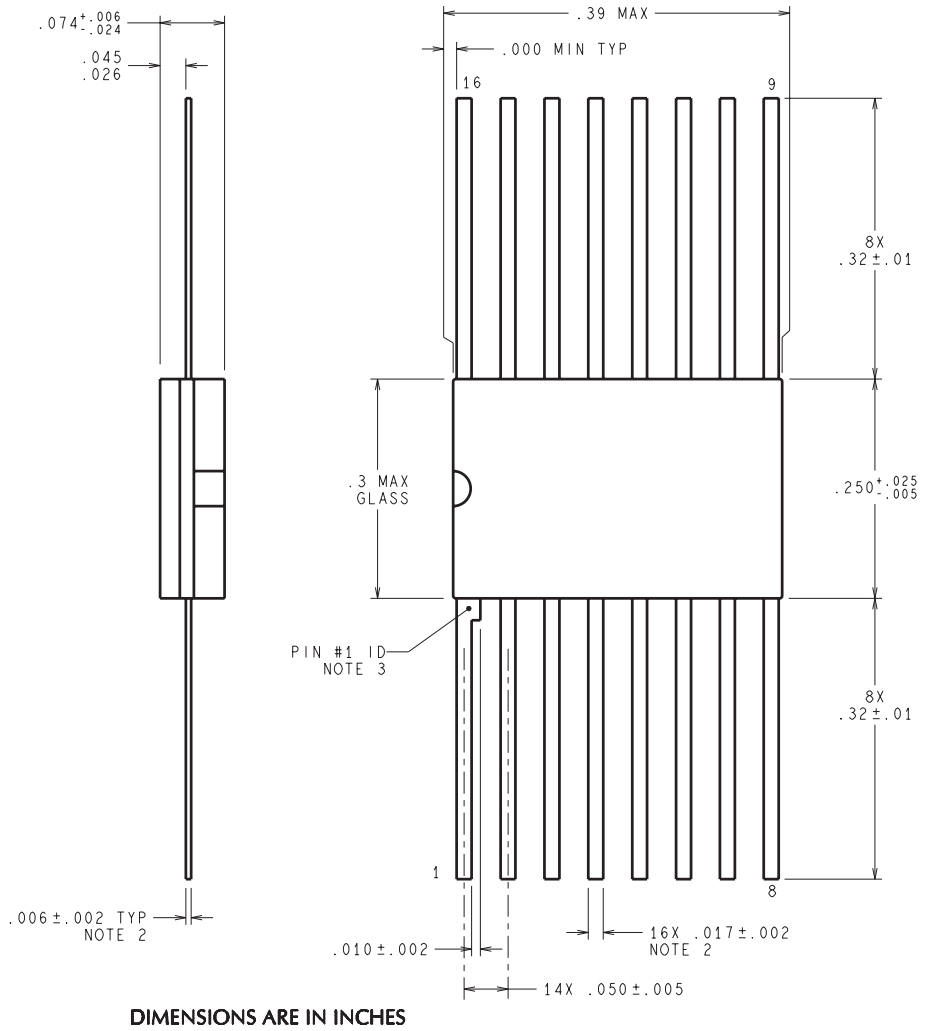


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