1.5 GHz Fully Differential Amplifier

Check for Samples: LMH6552

FEATURES

- **1.5 GHz −3 dB Small Signal Bandwidth @ A_V = 1**
- **1.25 GHz −3 dB Large Signal Bandwidth @ A_V = 1**
- **800 MHz Bandwidth @ A_V = 4**
- **450 MHz 0.1 dB Flatness**
- **3800 V/µs Slew Rate**
- **10 ns Settling Time to 0.1%**
  - **−90 dB THD @ 20 MHz**
  - **−74 dB THD @ 70 MHz**
- **20 ns Enable/Shutdown Pin**
- **5 to 12V Operation**

APPLICATIONS

- **Differential ADC Driver**
- **Video Over Twisted Pair**
- **Differential Line Driver**
- **Single End to Differential Converter**
- **High Speed Differential Signaling**
- **IF/RF Amplifier**
- **Level Shift Amplifier**
- **SAW Filter Buffer/Driver**

DESCRIPTION

The LMH6552 is a high performance fully differential amplifier designed to provide the exceptional signal fidelity and wide large-signal bandwidth necessary for driving 8 to 14 bit high speed data acquisition systems. Using TI's proprietary differential current mode input stage architecture, the LMH6552 allows operation at gains greater than unity without sacrificing response flatness, bandwidth, harmonic distortion, or output noise performance.

With external gain set resistors and integrated common mode feedback, the LMH6552 can be configured as either a differential input to differential output or single ended input to differential output gain block. The LMH6552 can be AC or DC coupled at the input which makes it suitable for a wide range of applications including communication systems and high speed oscilloscope front ends. The performance of the LMH6552 driving an ADC14DS105 is 86 dBc SFDR and 74 dBc SNR up to 40 MHz.

The LMH6552 is available in an 8-pin SOIC package as well as a space saving, thermally enhanced 8-Pin WSON package for higher performance.

Typical Application

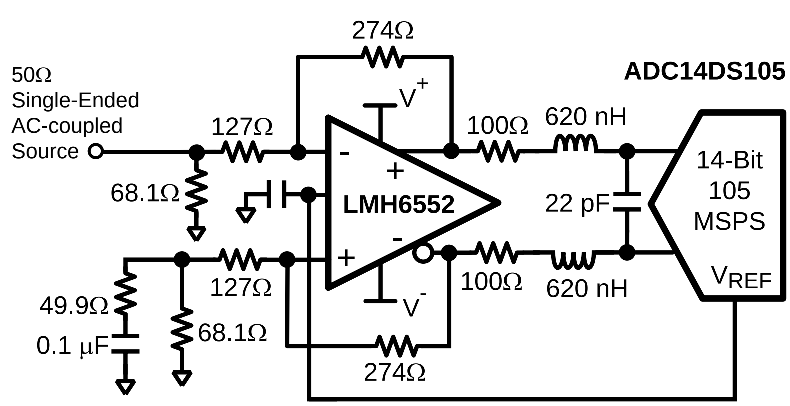


Figure 1. Single-Ended Input Differential Output ADC Driver

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage	13.2V
Common Mode Input Voltage	$\pm V_S$
Maximum Input Current (pins 1, 2, 7, 8)	30 mA
Maximum Output Current (pins 4, 5)	(3)
Maximum Junction Temperature	150°C
Soldering Information For soldering specifications see SNOA549C	

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) Human Body Model, applicable std. MIL-STD-883, Method 30157. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See POWER DISSIPATION of Application Information for more details.

Operating Ratings (1)

Operating Temperature Range (2)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Total Supply Voltage	4.5V to 12V
Package Thermal Resistance (θ_{JA})	
8-Pin SOIC	150°C/W
8-Pin WSON	58°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

±5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5V, V^- = −5V, A_V= 1, V_{CM} = 0V, R_F = R_G = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
AC Performance (Differential)						
SSBW	Small Signal −3 dB Bandwidth (2)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		1500		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		1000		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		930		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		810		
		V_{OUT} = 0.2 V_{PP}, A_V = 8		590		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		1250		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		950		
		V_{OUT} = 2 V_{PP}, A_V = 2		820		
		V_{OUT} = 2 V_{PP}, A_V = 4		740		
		V_{OUT} = 2 V_{PP}, A_V = 8		590		
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		450		MHz
	Slew Rate	4V Step, A_V = 1		3800		V/µs
	Rise/Fall Time, 10%-90%	2V Step		600		ps
	0.1% Settling Time	2V Step		10		ns
	Overdrive Recovery Time	V_{IN} = 1.8V to 0V Step, A_V = 5 V/V		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−92		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−74		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		−93		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		−84		
IMD3	Two-Tone Intermodulation	f ≥ 70 MHz, Third Order Products, V_{OUT} = 2 V_{PP} Composite		−87		dBc
	Input Noise Voltage	f ≥ 1 MHz		1.1		nV/√Hz
	Input Noise Current	f ≥ 1 MHz		19.5		pA/√Hz
	Noise Figure (See Figure 48)	50Ω System, A_V = 9, 10 MHz		10.3		dB
Input Characteristics						
I_{BI}	Input Bias Current (4)			60	110	µA
$I_{Boffset}$	Input Bias Current Differential (3)	V_{CM} = 0V, V_{ID} = 0V, $I_{Boffset}$ = $(I_B^- - I_B^+)/2$		2.5	18	µA
CMRR	Common Mode Rejection Ratio (3)	DC, V_{CM} = 0V, V_{ID} = 0V		80		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Voltage Range	CMRR > 38 dB	±3.5	±3.8		V
Output Performance						
	Output Voltage Swing (3)	Differential Output	14.8	15.4		V_{PP}
I_{OUT}	Linear Output Current (3)	V_{OUT} = 0V	±70	±80		mA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Application Information for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) I_{BI} is referred to a differential output offset voltage by the following relationship: $V_{OD(offset)} = I_{BI}*2R_F$

±5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +5V, V^- = −5V, A_V= 1, V_{CM} = 0V, R_F = R_G = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2V Single Ended (5)		±141		mA
	Output Balance Error	ΔV_{OUT} Common Mode /ΔV_{OUT} Differential, ΔV_{OD} = 1V, f < 1 MHz		−60		dB
Miscellaneous Performance						
Z_T	Open Loop Transimpedance	Differential		108		dBΩ
PSRR	Power Supply Rejection Ratio	DC, (V^+ - $\|V^-\|$) = ±1V		80		dB
I_S	Supply Current (3)	R_L = ∞	19	22.5	25 **28**	mA
	Enable Voltage Threshold		3.0			V
	Disable Voltage Threshold				2.0	V
	Enable/Disable time			15		ns
I_{SD}	Disable Shutdown Current			500	600	µA
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN}^+ = V_{IN}^- = 0		400		MHz
	Slew Rate	V_{IN}^+ = V_{IN}^- = 0		607		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0		1.5	±16.5	mV
	Input Bias Current	(6)		−3.2	±8	µA
	Voltage Range		±3.7	±3.8		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	1.0	1.012	V/V

(5) Short circuit current should be limited in duration to no more than 10 seconds. See POWER DISSIPATION of Application Information for more details.
(6) Negative input current implies current flowing out of the device.

±2.5V Electrical Characteristics (1)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +2.5V, V^- = −2.5V, A_V = 1, V_{CM} = 0V, R_F = R_G = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
SSBW	Small Signal −3 dB Bandwidth (2)	V_{OUT} = 0.2 V_{PP}, A_V = 1, R_L = 1 kΩ		1100		MHz
		V_{OUT} = 0.2 V_{PP}, A_V = 1		800		
		V_{OUT} = 0.2 V_{PP}, A_V = 2		740		
		V_{OUT} = 0.2 V_{PP}, A_V = 4		660		
		V_{OUT} = 0.2 V_{PP}, A_V = 8		498		
LSBW	Large Signal −3 dB Bandwidth	V_{OUT} = 2 V_{PP}, A_V = 1, R_L = 1 kΩ		820		MHz
		V_{OUT} = 2 V_{PP}, A_V = 1		690		
		V_{OUT} = 2 V_{PP}, A_V = 2		620		
		V_{OUT} = 2 V_{PP}, A_V = 4		589		
		V_{OUT} = 2 V_{PP}, A_V = 8		480		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Application Information for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

±2.5V Electrical Characteristics (1) (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +2.5V, V^- = −2.5V, A_V = 1, V_{CM} = 0V, R_F = R_G = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
	0.1 dB Bandwidth	V_{OUT} = 0.2 V_{PP}, A_V = 1		300		MHz
	Slew Rate	2V Step, A_V = 1		2100		V/μs
	Rise/Fall Time, 10% to 90%	2V Step		700		ps
	0.1% Settling Time	2V Step		10		ns
	Overdrive Recovery Time	V_{IN} = 0.7 V to 0 V Step, A_V = 5 V/V		6		ns
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		-82		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		-65		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz, R_L = 800Ω		-79		dBc
		V_{OUT} = 2 V_{PP}, f = 70 MHz, R_L = 800Ω		-67		
IMD3	Two-Tone Intermodulation	f ≥ 70 MHz, Third Order Products, V_{OUT} = 2 V_{PP} Composite		−77		dBc
	Input Noise Voltage	f ≥ 1 MHz		1.1		nV/√Hz
	Input Noise Current	f ≥ 1 MHz		19.5		pA/√Hz
	Noise Figure (See Figure 48)	50Ω System, A_V = 9, 10 MHz		10.2		dB
Input Characteristics						
I_{BI}	Input Bias Current (4)			54	90	μA
$I_{Boffset}$	Input Bias Current Differential (3)	V_{CM} = 0V, V_{ID} = 0V, $I_{Boffset}$ = (I_B^- - I_B^+)/2		2.3	18	μA
CMRR	Common-Mode Rejection Ratio (3)	DC, V_{CM} = 0V, V_{ID} = 0V		75		dBc
R_{IN}	Input Resistance	Differential		15		Ω
C_{IN}	Input Capacitance	Differential		0.5		pF
CMVR	Input Common Mode Range	CMRR > 38 dB	±1.0	±1.3		V
Output Performance						
	Output Voltage Swing (5)	Differential Output	5.6	6.0		V_{PP}
I_{OUT}	Linear Output Current (5)	V_{OUT} = 0V	±55	±65		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground, V_{IN} = 2V Single Ended (6)		±131		mA
	Output Balance Error	ΔV_{OUT} Common Mode /ΔV_{OUT} Differential, ΔV_{OD} = 1V, f < 1 MHz		60		dB
Miscellaneous Performance						
ZT	Open Loop Transimpedance	Differential		107		dBΩ
PSRR	Power Supply Rejection Ratio	DC, ΔV_S = ±1V		80		dB
I_S	Supply Current (5)	R_L = ∞	17	20.4	24 **27**	mA
	Enable Voltage Threshold		3.0			V
	Disable Voltage Threshold				2.0	V
	Enable/Disable Time			15		ns
I_{SD}	Disable Shutdown Current			500	600	μA
Output Common Mode Control Circuit						
	Common Mode Small Signal Bandwidth	V_{IN}^+ = V_{IN}^- = 0		310		MHz
	Slew Rate	V_{IN}^+ = V_{IN}^- = 0		430		V/μs

(4) I_{BI} is referred to a differential output offset voltage by the following relationship: $V_{OD(offset)} = I_{BI}*2R_F$
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(6) Short circuit current should be limited in duration to no more than 10 seconds. See POWER DISSIPATION of Application Information for more details.

±2.5V Electrical Characteristics [1] (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = +2.5V, V^- = −2.5V, A_V = 1, V_{CM} = 0V, R_F = R_G = 357Ω, R_L = 500Ω, for single ended in, differential out. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0		1.65	±15	mV
	Input Bias Current	[7]		−2.9		µA
	Voltage Range		±1.19	±1.25		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		80		dB
	Input Resistance			200		kΩ
	Gain	$\Delta V_{O,CM}/\Delta V_{CM}$	0.995	1.0	1.012	V/V

(7) Negative input current implies current flowing out of the device.

CONNECTION DIAGRAM

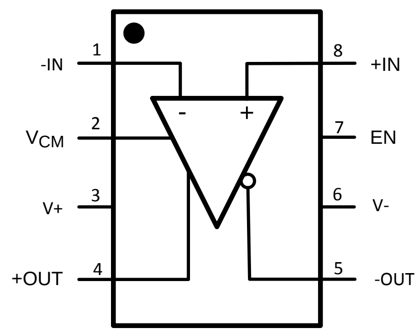


Figure 2. 8-Pin SOIC-Top View
See Package Number D0008A

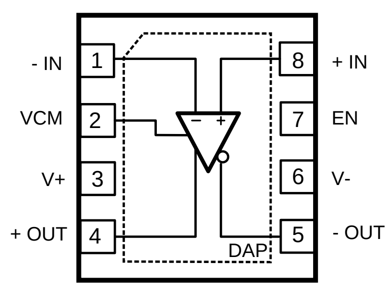


Figure 3. 8-Pin WSON-Top View
See Package Number NGS0008C

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	-IN	Negative Input
2	VCM	Output Common Mode Control
3	V+	Positive Supply
4	+OUT	Positive Output
5	-OUT	Negative Output
6	V-	Negative Supply
7	EN	Enable
8	+IN	Positive Input
DAP	DAP	Die Attach Pad (See THERMAL PERFORMANCE for more information)

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$

(T_A = 25°C, $R_F = R_G$ = 357Ω, R_L = 500Ω, A_V = 1, for single ended in, differential out, unless specified).

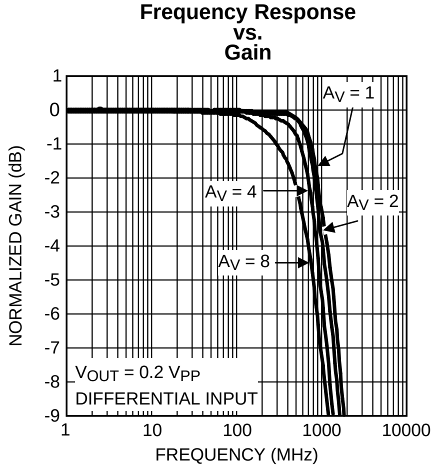


Figure 4.

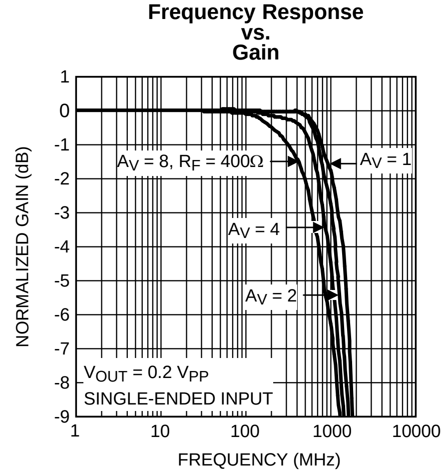


Figure 5.

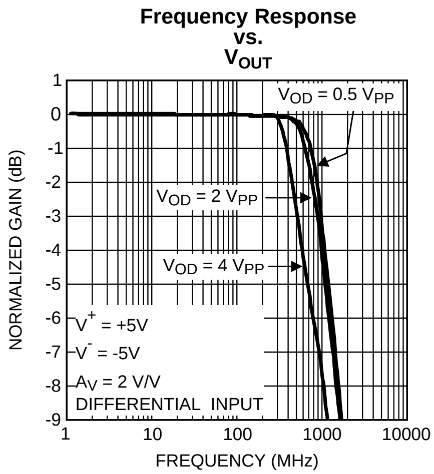


Figure 6.

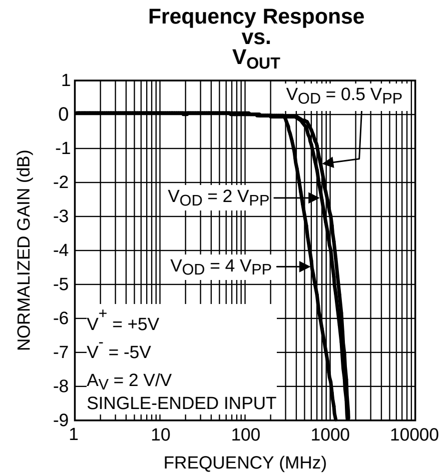


Figure 7.

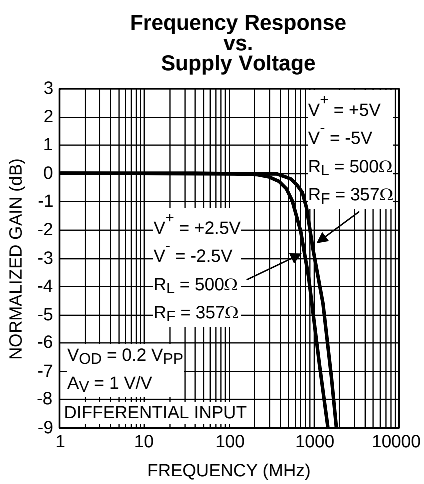


Figure 8.

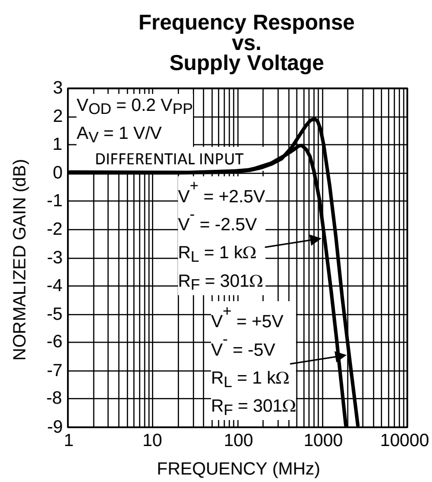


Figure 9.

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

($T_A = 25°C$, $R_F = R_G = 357\Omega$, $R_L = 500\Omega$, $A_V = 1$, for single ended in, differential out, unless specified).

Frequency Response vs. Capacitive Load

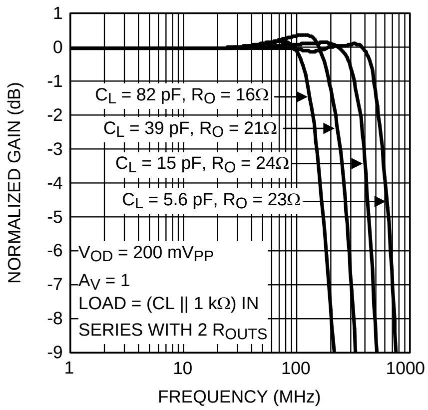


Figure 10.

Suggested R_{OUT} vs. Capacitive Load

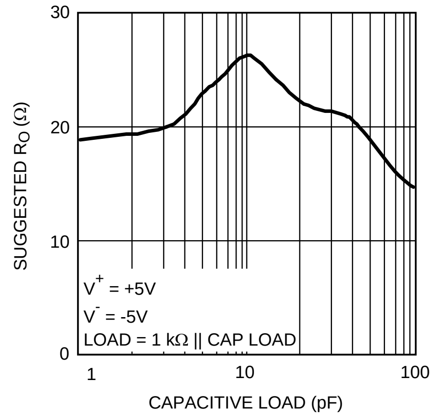


Figure 11.

Frequency Response vs. Resistive Load

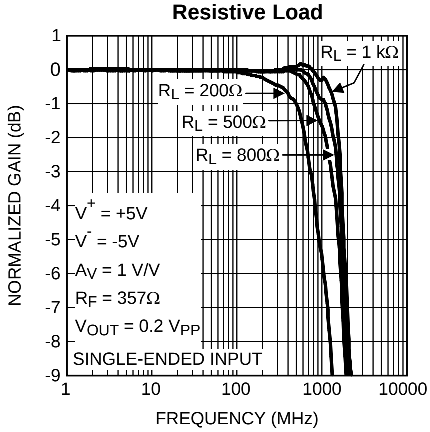


Figure 12.

Frequency Response vs. Resistive Load

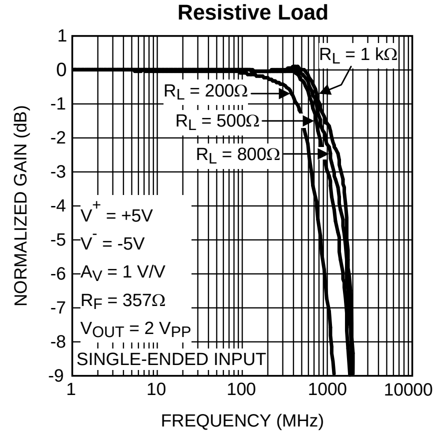


Figure 13.

Frequency Response vs. R_F

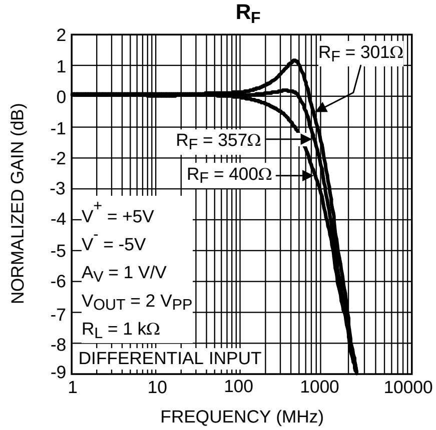


Figure 14.

1 V_{PP} Pulse Response Single Ended Input

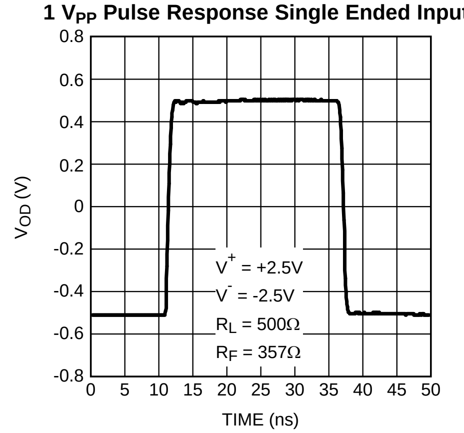


Figure 15.

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

(T_A = 25°C, $R_F = R_G$ = 357Ω, R_L = 500Ω, A_V = 1, for single ended in, differential out, unless specified).

2 V_{PP} Pulse Response Single Ended Input

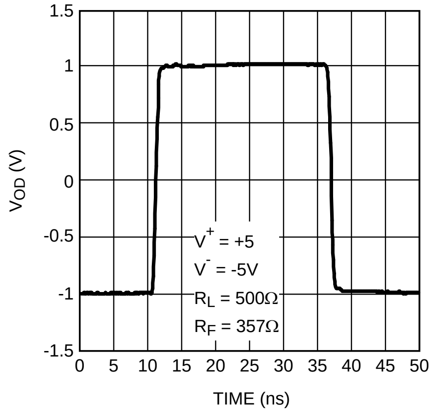


Figure 16.

Large Signal Pulse Response

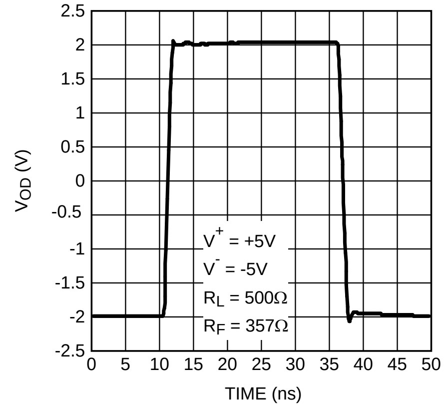


Figure 17.

Output Common Mode Pulse Response

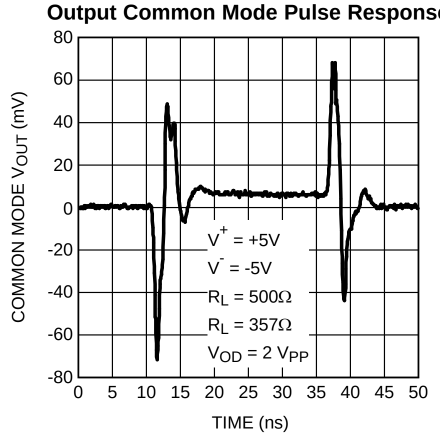


Figure 18.

Distortion vs. Frequency Single Ended Input

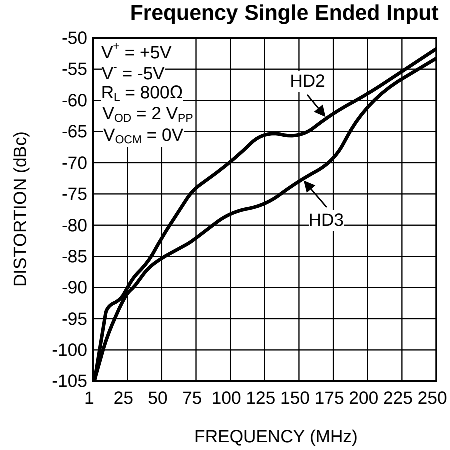


Figure 19.

Distortion vs. Supply Voltage

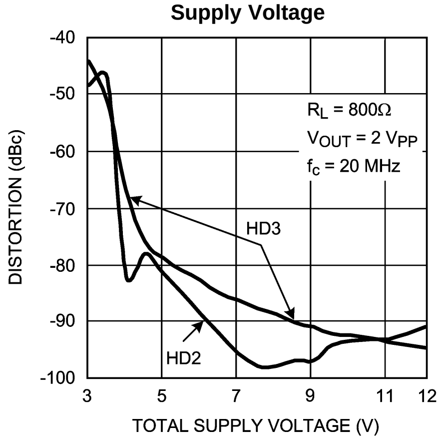


Figure 20.

Distortion vs. Supply Voltage

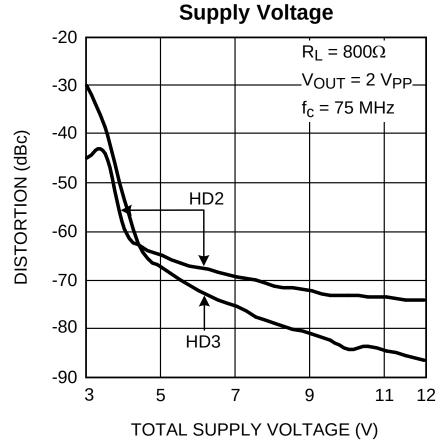


Figure 21.

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

(T_A = 25°C, $R_F = R_G$ = 357Ω, R_L = 500Ω, A_V = 1, for single ended in, differential out, unless specified).

Distortion vs. Output Common Mode Voltage

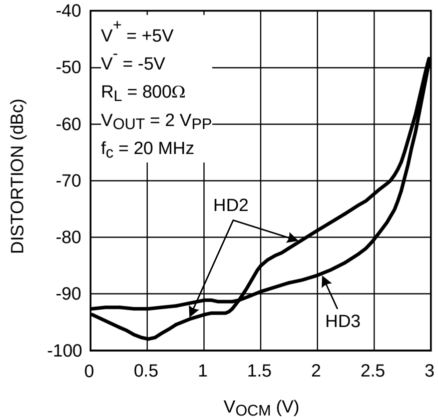


Figure 22.

Distortion vs. Output Common Mode Voltage

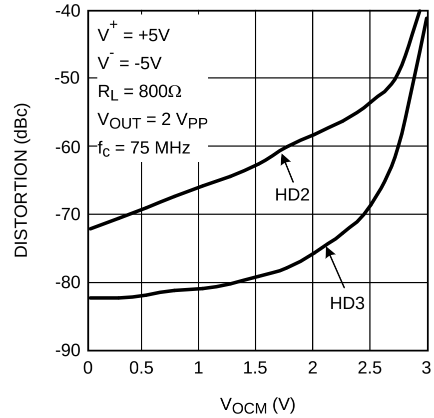


Figure 23.

Maximum V_{OUT} vs. I_{OUT}

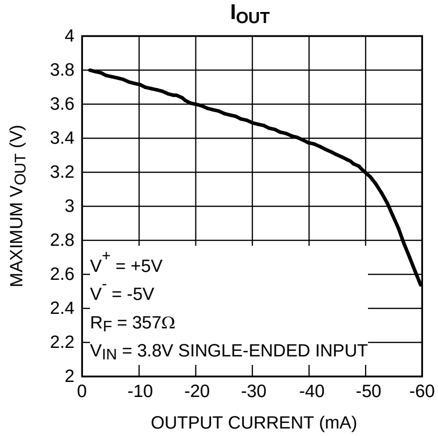


Figure 24.

Minimum V_{OUT} vs. I_{OUT}

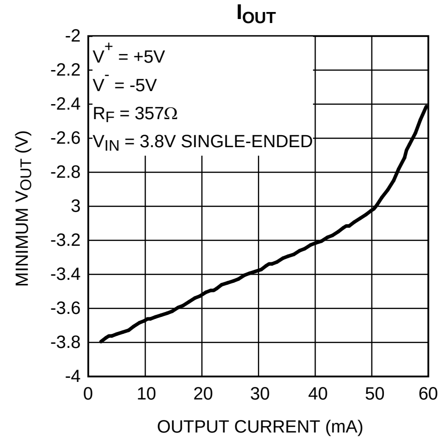


Figure 25.

Open Loop Transimpedance

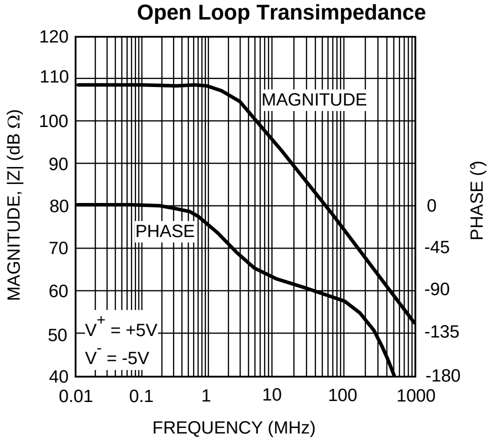


Figure 26.

Open Loop Transimpedance

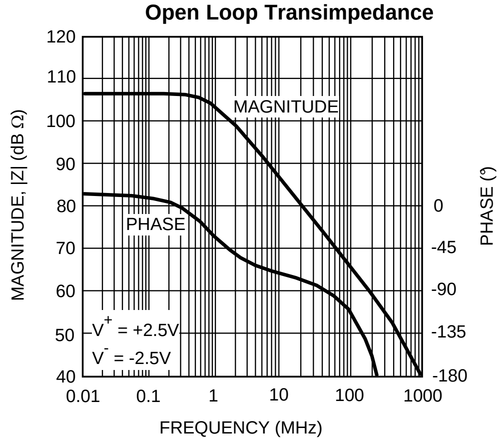


Figure 27.

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

(T_A = 25°C, R_F = R_G = 357Ω, R_L = 500Ω, A_V = 1, for single ended in, differential out, unless specified).

Closed Loop Output Impedance

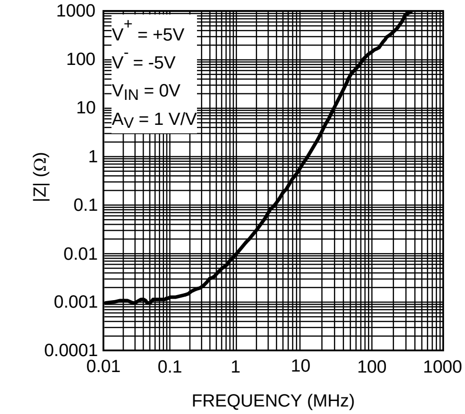


Figure 28.

Closed Loop Output Impedance

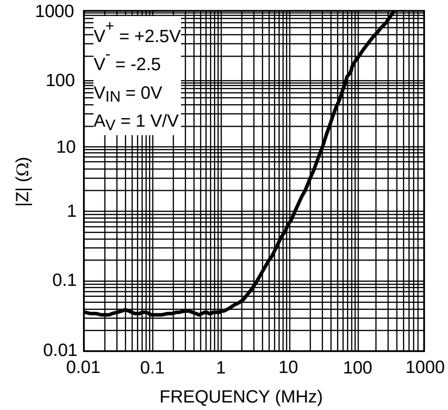


Figure 29.

Overdrive Recovery

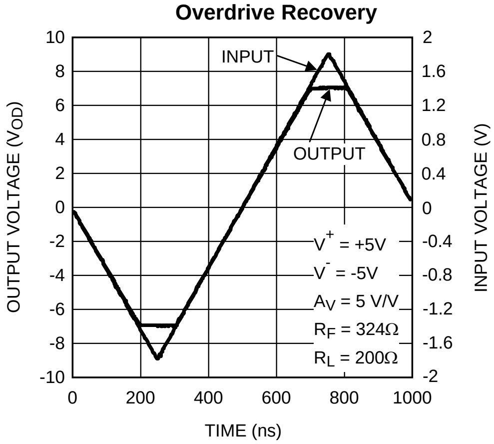


Figure 30.

Overdrive Recovery

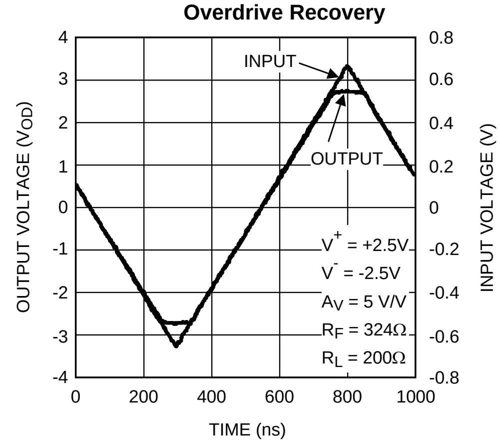


Figure 31.

PSRR

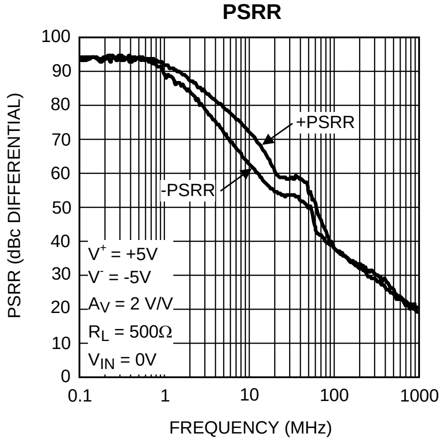


Figure 32.

PSRR

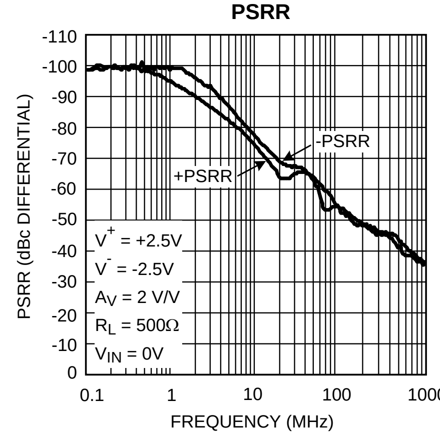


Figure 33.

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

(T_A = 25°C, R_F = R_G = 357Ω, R_L = 500Ω, A_V = 1, for single ended in, differential out, unless specified).

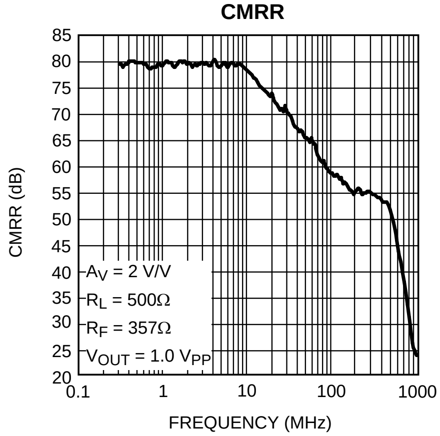


Figure 34.

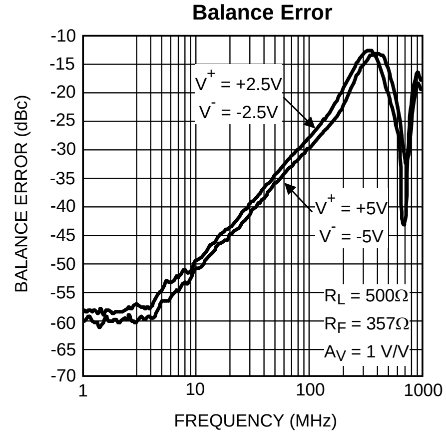


Figure 35.

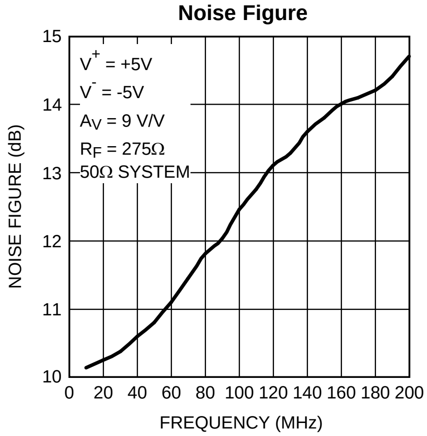


Figure 36.

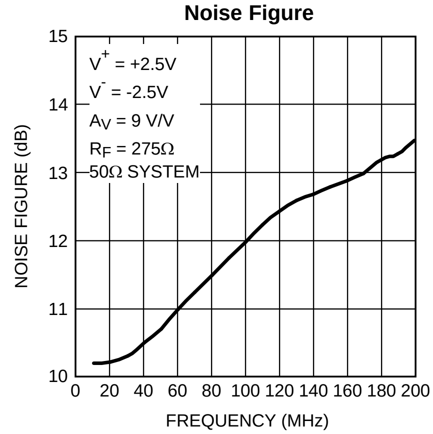


Figure 37.

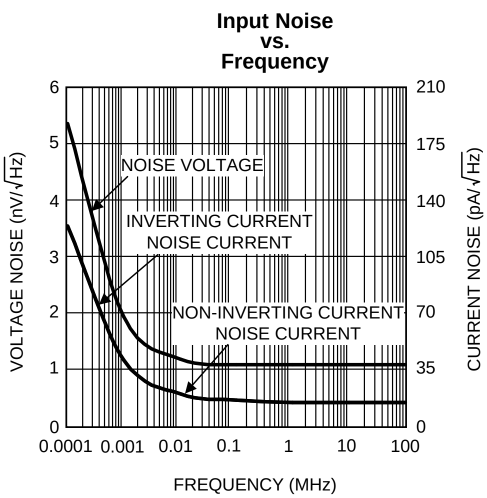


Figure 38.

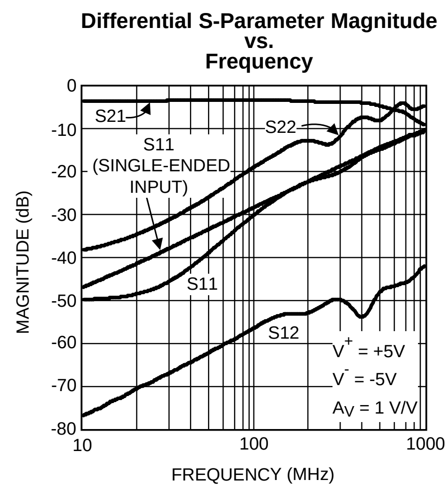


Figure 39.

Typical Performance Characteristics $V^+ = +5V$, $V^- = -5V$ (continued)

(T_A = 25°C, $R_F = R_G$ = 357Ω, R_L = 500Ω, A_V = 1, for single ended in, differential out, unless specified).

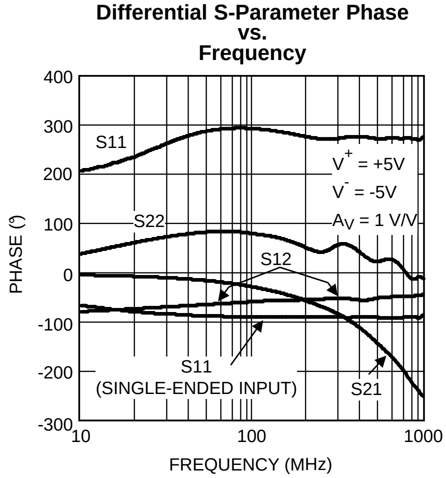


Figure 40.

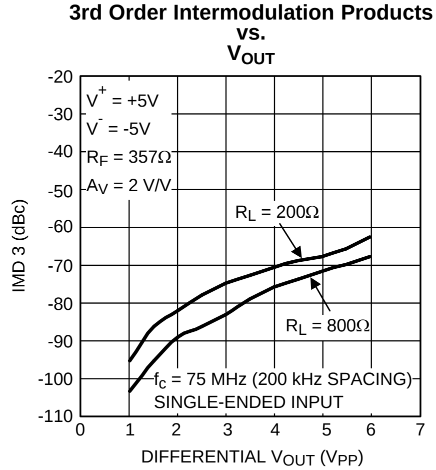


Figure 41.

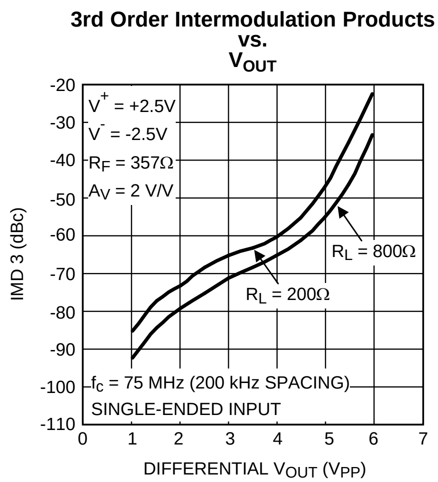


Figure 42.

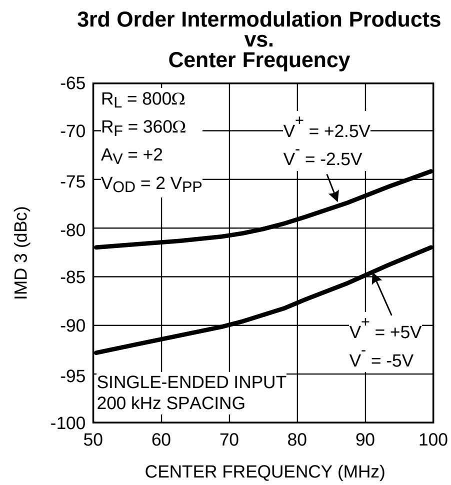


Figure 43.

APPLICATION INFORMATION

The LMH6552 is a fully differential current feedback amplifier with integrated output common mode control, designed to provide low distortion amplification to wide bandwidth differential signals. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the V^+ and V^- outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

The proprietary current feedback architecture of the LMH6552 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of R_{F1} and R_{F2}. Generally R_{F1} is set equal to R_{F2}, and R_{G1} equal to R_{G2}, so that the gain is set by the ratio R_F/R_G. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A minimum of 0.1% tolerance resistors are recommended for optimal performance, and the amplifier is internally compensated to operate with optimum gain flatness with values of R_F between 270Ω and 390Ω depending on package selection, PCB layout, and load resistance.

The output common mode voltage is set by the V_{CM} pin with a fixed gain of 1 V/V. This pin should be driven by a low impedance reference and should be bypassed to ground with a 0.1 µF ceramic capacitor. Any unwanted signal coupling into the V_{CM} pin will be passed along to the outputs, reducing the performance of the amplifier. This pin must not be left floating.

The LMH6552 can be operated on a supply range as either a single 5V supply or as a split +5V and −5V. Operation on a single 5V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling may be required. For example, in a DC coupled input application on a single 5V supply, with a V_{CM} of 1.5V, the input common voltage at a gain of 1 will be 0.75V which is outside the minimum 1.2V to 3.8V input common mode range of the amplifier. The minimum V_{CM} for this application should be greater than 2.5V depending on output signal swing. Alternatively, AC coupling of the inputs in this example results in equal input and output common mode voltages, so a 1.5V V_{CM} would be achievable. Split supplies will allow much less restricted AC and DC coupled operation with optimum distortion performance.

The LMH6552 is equipped with an ENABLE pin to reduce power consumption when not in use. The ENABLE pin, when not driven, floats high (on). When the ENABLE pin is pulled low the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. For this reason input to output isolation will be poor in the disabled state and the part is not recommended in multiplexed applications where outputs are all tied together.

WSON PACKAGE

Due to it's size and lower parasitics, the WSON requires the lower optimum value of 275Ω for R_F. This will give a flat frequency response with minimal peaking. With a lower R_F value the WSON package will have a reduction in noise compared to the SOIC with its optimum R_F = 360Ω.

FULLY DIFFERENTIAL OPERATION

The LMH6552 will perform best in a fully differential configuration. The circuit shown in Figure 44 is a typical fully differential application circuit as might be used to drive an analog to digital converter (ADC). In this circuit the closed loop gain $A_V = V_{OUT}/ V_{IN} = R_F/R_G$, where the feedback is symmetric. The series output resistors, R_O, are optional and help keep the amplifier stable when presented with a capacitive load. Refer to DRIVING CAPACITIVE LOADS for details.

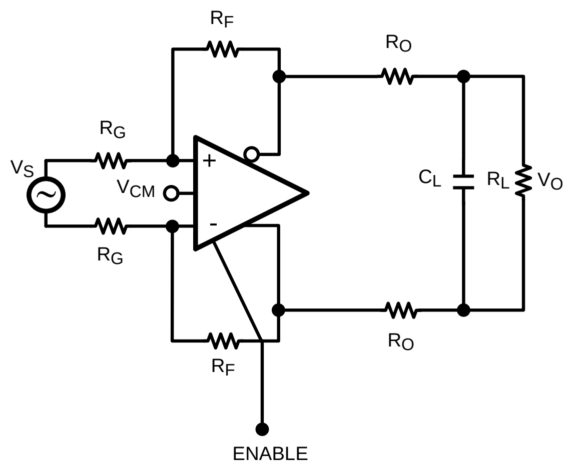


Figure 44. Typical Application

When driven from a differential source, the LMH6552 provides low distortion, excellent balance, and common mode rejection. This is true provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With an intrinsic device CMRR of 80 dB, using 0.1% resistors will give a worst case CMRR of around 60 dB for most circuits.

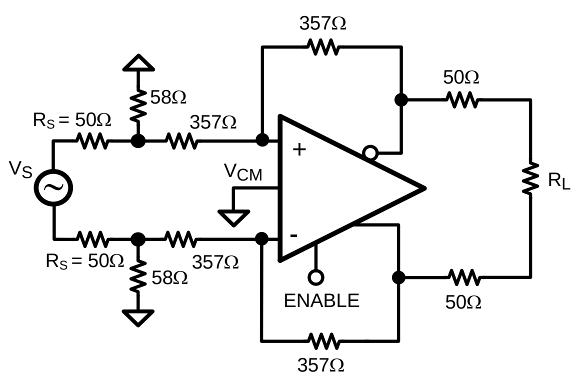
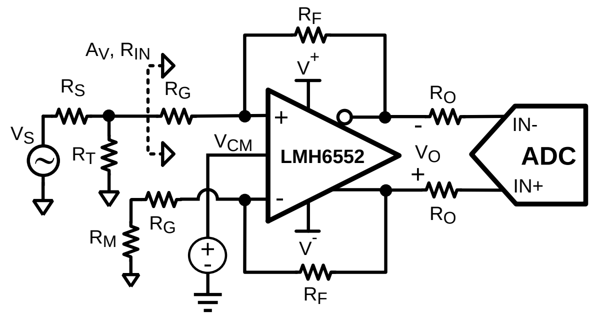


Figure 45. Differential S-Parameter Test Circuit

The circuit configuration shown in Figure 45 was used to measure differential S parameters in a 50Ω environment at a gain of 1 V/V. Refer to Figure 39 and Figure 40 in Typical Performance Characteristics V^+ = +5V, V^- = −5V for measurement results.

SINGLE ENDED INPUT TO DIFFERENTIAL OUTPUT OPERATION

In many applications, it is required to drive a differential input ADC from a single ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6552 provides excellent performance as a single-to-differential converter down to DC. Figure 46 shows a typical application circuit where an LMH6552 is used to produce a differential signal from a single ended source.



$$A_V = \left(\frac{2(1-\beta_1)}{\beta_1 + \beta_2}\right) \qquad \beta_1 = \left(\frac{R_G}{R_G + R_F}\right)$$

$$R_{IN} = \left(\frac{2R_G + R_M(1-\beta_2)}{1+\beta_2}\right) \qquad \beta_2 = \left(\frac{R_G + R_M}{R_G + R_F + R_M}\right)$$

$$R_S = R_T \,||\, R_{IN} \qquad R_M = R_T \,||\, R_S$$

Figure 46. Single Ended Input with Differential Output

When using the LMH6552 in single-to-differential mode, the complimentary output is forced to a phase inverted replica of the driven output by the common mode feedback circuit as opposed to being driven by its own complimentary input. Consequently, as the driven input changes, the common mode feedback action results in a varying common mode voltage at the amplifier's inputs, proportional to the driving signal. Due to the non-ideal common mode rejection of the amplifier's input stage, a small common mode signal appears at the outputs which is superimposed on the differential output signal. The ratio of the change in output common mode voltage to output differential voltage is commonly referred to as output balance error. The output balance error response of the LMH6552 over frequency is shown in Typical Performance Characteristics.

To match the input impedance of the circuit in Figure 46 to a specified source resistance, R_S, requires that $R_T \,||\, R_{IN} = R_S$. The equations governing R_{IN} and A_V for single-to-differential operation are also provided in Figure 46. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configurations in a 50Ω environment are given in Table 2. Gain Component Values for 50Ω System WSON Package. Typically R_S=50Ω while $R_M = R_S || R_T$.

Table 2. Gain Component Values for 50Ω System WSON Package

Gain	R_F	R_G	R_T	R_M
0 dB	275Ω	255Ω	59Ω	26.7Ω
6 dB	275Ω	127Ω	68.1Ω	28.7Ω
12 dB	275Ω	54.9Ω	107Ω	34Ω

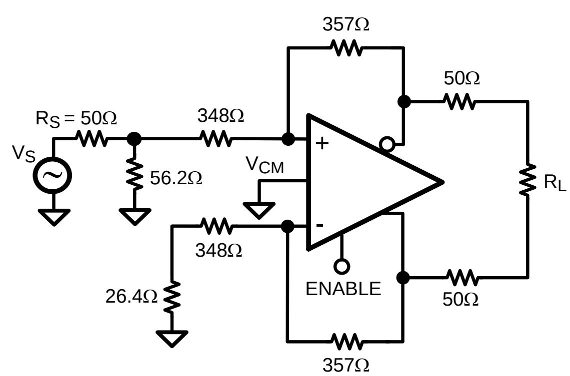
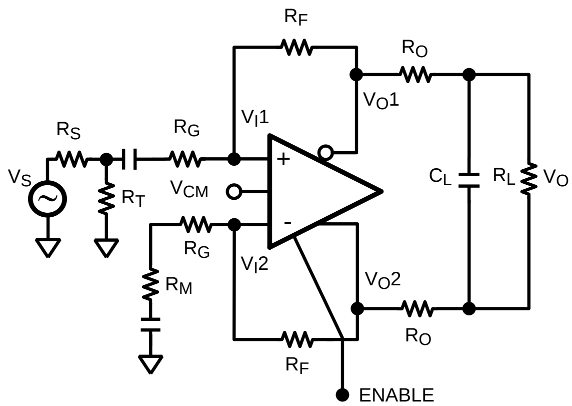


Figure 47. Single Ended Input S-Parameter Test Circuit (50Ω System)

The circuit shown in Figure 47 was used to measure S-parameters for a single-to-differential configuration. Figure 39 and Figure 40 in Typical Performance Characteristics are taken using the recommended component values for 0 dB gain.

SINGLE SUPPLY OPERATION

Single supply operation is possible on supplies from 5V to 10V; however, as discussed earlier, AC input coupling is recommended for low supplies such as 5V due to input common mode limitations. An example of an AC coupled, single supply, single-to-differential circuit is shown in Figure 48. Note that when AC coupling, both inputs need to be AC coupled irrespective of single-to-differential or differential-to-differential configuration. For higher supply voltages DC coupling of the inputs may be possible provided that the output common mode DC level is set high enough so that the amplifier's inputs and outputs are within their specified operating ranges.



$$^*V_{CM} = \frac{V_O1 + V_O2}{2}$$

*BY DESIGN

$$V_{ICM} = V_{OCM}$$

$$V_{ICM} = \frac{V_I1 + V_I2}{2}$$

Figure 48. AC Coupled for Single Supply Operation

SPLIT SUPPLY OPERATION

For optimum performance, split supply operation is recommended using +5V and −5V supplies; however, operation is possible on split supplies as low as +2.25V and −2.25V and as high as +6V and −6V. Provided the total supply voltage does not exceed the 4.5V to 12V operating specification, non-symmetric supply operation is also possible and in some cases advantageous. For example, if a 5V DC coupled operation is required for low power dissipation but the amplifier input common mode range prevents this operation, it is still possible with split supplies of (V^+) and (V^-). Where (V^+) - (V^-) = 5V and V^+ and V^- are selected to center the amplifier input common mode range to suit the application.

OUTPUT NOISE PERFORMANCE AND MEASUREMENT

Unlike differential amplifiers based on voltage feedback architectures, noise sources internal to the LMH6552 refer to the inputs largely as current sources, hence the low input referred voltage noise and relatively higher input referred current noise. The output noise is therefore more strongly coupled to the value of the feedback resistor and not to the closed loop gain, as would be the case with a voltage feedback differential amplifier. This allows operation of the LMH6552 at much higher gain without incurring a substantial noise performance penalty, simply by choosing a suitable feedback resistor.

Figure 49 shows a circuit configuration used to measure noise figure for the LMH6552 in a 50Ω system. An R_F value of 275Ω is chosen for the SOIC package to minimize output noise while simultaneously allowing both high gain (9 V/V) and proper 50Ω input termination. Refer to SINGLE ENDED INPUT TO DIFFERENTIAL OUTPUT OPERATION for calculation of resistor and gain values. Noise figure values at various frequencies are shown Figure 36 in Typical Performance Characteristics.

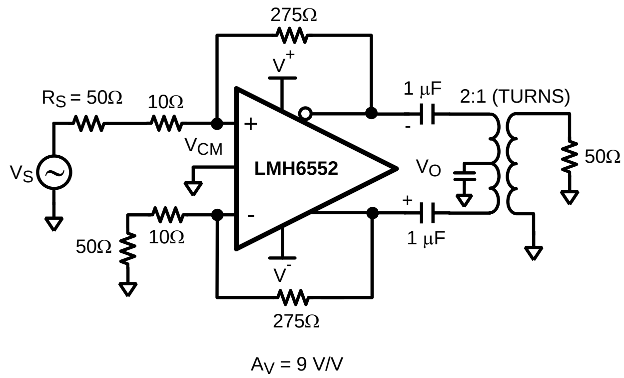


Figure 49. Noise Figure Circuit Configuration

DRIVING ANALOG TO DIGITAL CONVERTERS

Analog-to-digital converters present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there are usually current spikes associated with switched capacitor or sample and hold circuits. Figure 50 shows a combination circuit of the LMH6552 driving the ADC12DL080. The two 125Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier and ensure stability. In addition, the resistors, along with a 2.2 pF capacitor across the outputs (in parallel with the ADC input capacitance), form a low pass anti-aliasing filter with a pole frequency of about 60 MHz. For switched capacitor input ADCs, the input capacitance will vary based on the clock cycle, as the ADC switches between the sample and hold mode. See your particular ADC's datasheet for details.

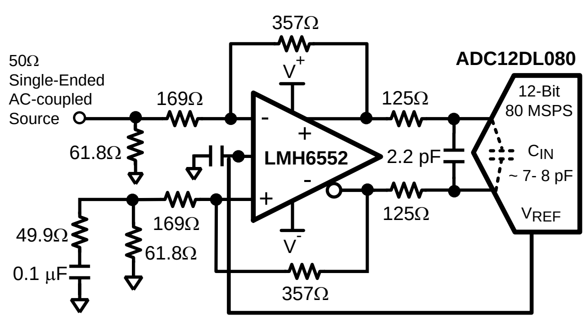


Figure 50. Driving a 12-bit ADC

Figure 51 shows the SFDR and SNR performance vs. frequency for the LMH6552 and ADC12DL080 combination circuit with the ADC input signal level at −1 dBFS. The ADC12DL080 is a dual 12-bit ADC with maximum sampling rate of 80 MSPS. The amplifier is configured to provide a gain of 2 V/V in single to differential mode. An external band-pass filter is inserted in series between the input signal source and the amplifier to reduce harmonics and noise from the signal generator. In order to properly match the input impedance seen at the LMH6552 amplifier inputs, R_M is chosen to match Z_S || R_T for proper input balance.

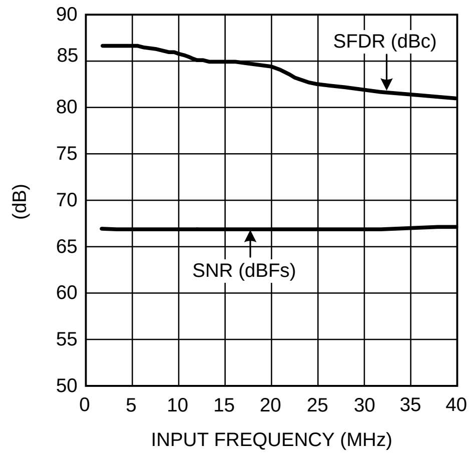


Figure 51. LMH6552/ADC12DL080 SFDR and SNR Performance vs. Frequency

Figure 52 shows a combination circuit of the LMH6552 driving the ADC14DS105. The ADC14DS105 is a dual channel 14-bit ADC with a sampling rate of 105 MSPS. The circuit in Figure 52 has a 2nd order low-pass LC filter formed by the 620 nH inductor along with the 22 pF capacitor across the differential outputs of the LMH6552. The filter has a pole frequency of about 50 MHz. Figure 53 shows the combined SFDR and SNR performance over frequency with a −1 dBFs input signal and a sampling rate of 1000 MSPS.

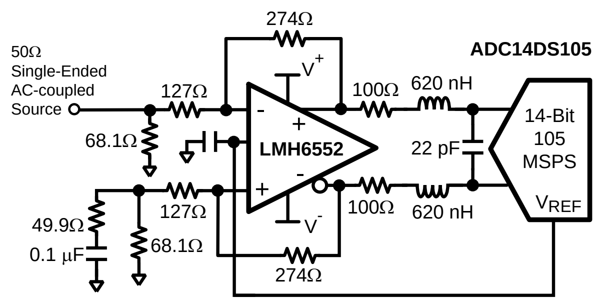


Figure 52. Driving a 14-bit ADC

The amplifier is configured to provide a gain of 2 V/V in a single-to-differential mode. The LMH6552 common mode voltage is set by the ADC14DS105. Circuit testing is the same as described for the LMH6552 and ADC12DL080 combination circuit. The 0.1 µF capacitor, in series with the 49.9Ω resistor, is inserted to ground across the 68.1Ω resistor to balance the amplifier inputs.

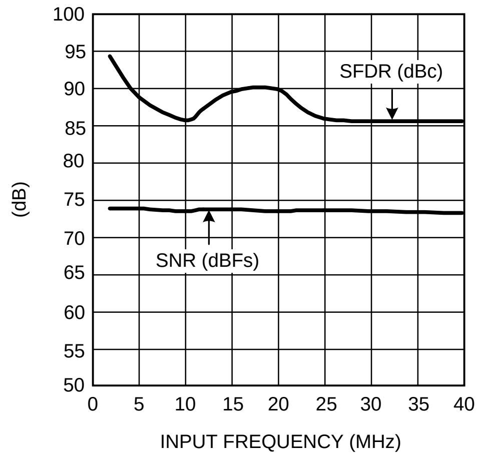


Figure 53. LMH6552/ADC14DS105 SFDR and SNR Performance vs. Frequency

The amplifier and ADC should be located as close as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. Some high performance ADCs have an input stage that has a bandwidth of several times its sample rate. The sampling process results in all input signals presented to the input stage mixing down into the first Nyquist zone (DC to Fs/2).

The LMH6552 is capable of driving a variety of Texas Instruments Analog-to-Digital Converters. This is shown in TABLE 3. DIFFERENTIAL INPUT ADC's COMPATIBLE WITH LMH6552 DRIVER, which offers a list of possible signal path ADC and amplifier combinations. The use of the LMH6552 to drive an ADC is determined by the application and the desired sampling process (Nyquist operation, sub-sampling or over-sampling). See application note AN-236 for more details on the sampling processes and application note AN-1393 'Using High Speed Differential Amplifiers to Drive ADCs. For more information regarding a particular ADC, refer to the particular ADC datasheet for details.

TABLE 3. DIFFERENTIAL INPUT ADC's COMPATIBLE WITH LMH6552 DRIVER

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC1173	15	8	SINGLE
ADC1175	20	8	SINGLE
ADC08351	42	8	SINGLE
ADC1175-50	50	8	SINGLE
ADC08060	60	8	SINGLE
ADC08L060	60	8	SINGLE
ADC08100	100	8	SINGLE
ADC08200	200	8	SINGLE
ADC08500	500	8	SINGLE
ADC081000	1000	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC10321	20	10	SINGLE
ADC10D020	20	10	DUAL
ADC10030	27	10	SINGLE
ADC10040	40	10	DUAL
ADC10065	65	10	SINGLE
ADC10DL065	65	10	DUAL
ADC10080	80	10	SINGLE
ADC11DL066	66	11	DUAL

Product Number	Max Sampling Rate (MSPS)	Resolution	Channels
ADC11L066	66	11	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE
ADC12010	10	12	SINGLE
ADC12020	20	12	SINGLE
ADC12040	40	12	SINGLE
ADC12D040	40	12	DUAL
ADC12DL040	40	12	DUAL
ADC12DL065	65	12	DUAL
ADC12DL066	66	12	DUAL
ADC12L063	63	12	SINGLE
ADC12C080	80	12	SINGLE
ADC12DS080	80	12	DUAL
ADC12L080	80	12	SINGLE
ADC12C105	105	12	SINGLE
ADC12DS105	105	12	DUAL
ADC12C170	170	12	SINGLE
ADC14L020	20	14	SINGLE
ADC14L040	40	14	SINGLE
ADC14C080	80	14	SINGLE
ADC14DS080	80	14	DUAL
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE

DRIVING CAPACITIVE LOADS

As noted previously, capacitive loads should be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 10 pF and the resistive component could be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors will be sufficient to isolate any subsequent capacitance.

BALANCED CABLE DRIVER

With up to 15 V_{PP} differential output voltage swing and 80 mA of linear drive current the LMH6552 makes an excellent cable driver as shown in Figure 54. The LMH6552 is also suitable for driving differential cables from a single ended source.

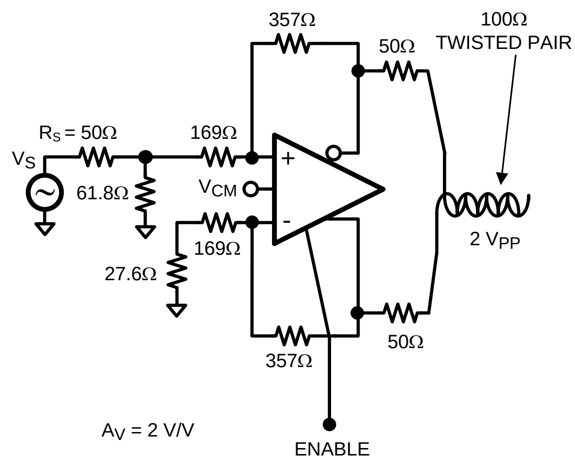


Figure 54. Fully Differential Cable Driver

POWER SUPPLY BYPASSING

The LMH6552 requires supply bypassing capacitors as shown in Figure 55 and Figure 56. The 0.01 µF and 0.1 µF capacitors should be leadless SMT ceramic capacitors and should be no more than 3 mm from the supply pins. These capacitors should be star routed with a dedicated ground return plane or trace for best harmonic distortion performance. A small capacitor, ~0.01 µF, placed across the supply rails, and as close to the chip's supply pins as possible, can further improve HD2 performance. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the V_{CM} and ENABLE pins to ground. These inputs are high impedance and can provide a coupling path into the amplifier for external noise sources, possibly resulting in loss of dynamic range, degraded CMRR, degraded balance and higher distortion.

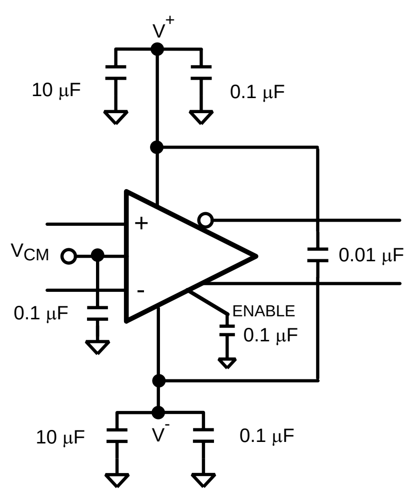


Figure 55. Split Supply Bypassing Capacitors

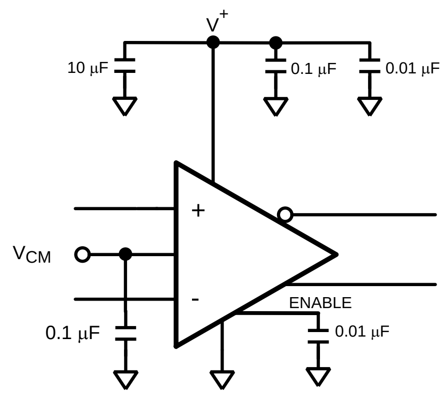


Figure 56. Single Supply Bypassing Capacitors

POWER DISSIPATION

The LMH6552 is optimized for maximum speed and performance in the small form factor of the standard SOIC package, and is essentially a dual channel amplifier. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the $T_{JMAX}$of 150°C is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6552:

1. Calculate the quiescent (no-load) power:

$P_{AMP} = I_{CC}* (V_S)$

where

- $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{OCM} is not mid-rail.) (1)

2. Calculate the RMS power dissipated in each of the output stages:

P_D (rms) = rms $((V_S - V^+_{OUT}) * I^+_{OUT})$ + rms $((V_S - V^-_{OUT}) * I^-_{OUT})$

where

- V_{OUT} and I_{OUT} are the voltage and the current measured at the output pins of the differential amplifier as if they were single ended amplifiers and V_S is the total supply voltage (2)

3. Calculate the total RMS power:

$P_T = P_{AMP} + P_D$ (3)

The maximum power that the LMH6552 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° – T_{AMB})/ \theta_{JA}$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the SOIC package θ_{JA} is 150°C/W
- For WSON package θ_{JA} is 58°C/W (4)

NOTE

If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

THERMAL PERFORMANCE

The WSON package is designed for enhanced thermal performance and features an exposed die attach pad (DAP) at the bottom center of the package that creates a direct path to the PCB for maximum power dissipation. The DAP is floating and is not electrically connected to internal circuitry. Compared to the traditional leaded packages where the die attach pad is embedded inside the molding compound, the WSON reduces one layer in the thermal path.

The thermal advantage of the WSON package is fully realized only when the exposed die attach pad is soldered down to a thermal land on the PCB board with thermal vias planted underneath the thermal land. The thermal land can be connected to any power or ground plane within the allowable supply voltage range of the device. Based on thermal analysis of the WSON package, the junction-to-ambient thermal resistance (θ_{JA}) can be improved by a factor of two when the die attach pad of the WSON package is soldered directly onto the PCB with thermal land and thermal vias are 1.27 mm and 0.33 mm respectively. Typical copper via barrel plating is 1 oz, although thicker copper may be used to further improve thermal performance.

For more information on board layout techniques, refer to Application Note 1187 “Leadless Lead Frame Package (LLP).” This application note also discusses package handling, solder stencil and the assembly process.

ESD PROTECTION

The LMH6552 is protected against electrostatic discharge (ESD) on all pins. The LMH6552 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6552 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

BOARD LAYOUT

The LMH6552 is a very high performance amplifier. In order to get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board should have a low inductance ground plane and well bypassed broad supply lines. External components should be leadless surface mount types. The feedback network and output matching resistors should be composed of short traces and precision resistors (0.1%). The output matching resistors should be placed within 3 or 4 mm of the amplifier as should the supply bypass capacitors. Refer to POWER SUPPLY BYPASSING for recommendations on bypass circuit layout. Evaluation boards are available free of charge through the product folder on ti.com.

By design, the LMH6552 is relatively insensitive to parasitic capacitance at its inputs. Nonetheless, ground and power plane metal should be removed from beneath the amplifier and from beneath R_F and R_G for best performance at high frequency.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry can contribute to distortion and balance errors.

EVALUATION BOARD

See the LMH6552 Product Folder for evaluation board availability and ordering information.

REVISION HISTORY

Changes from Revision G (March 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6552MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 52MA	Samples
LMH6552MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH65 52MA	Samples
LMH6552SD/NOPB	ACTIVE	WSON	NGS	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	6552	Samples
LMH6552SDX/NOPB	ACTIVE	WSON	NGS	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	6552	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

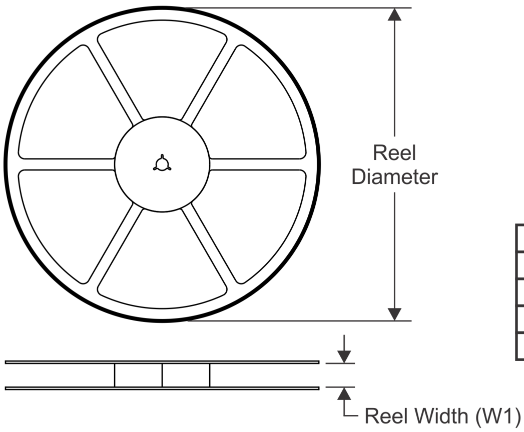
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

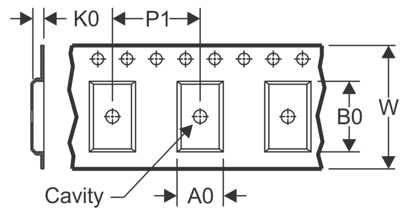
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

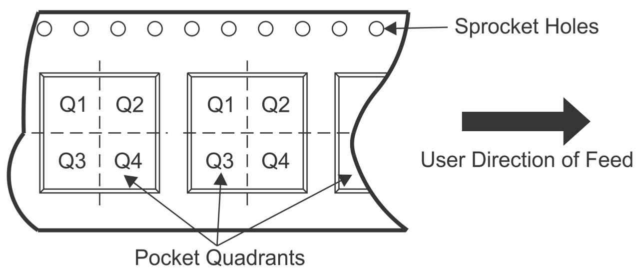
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

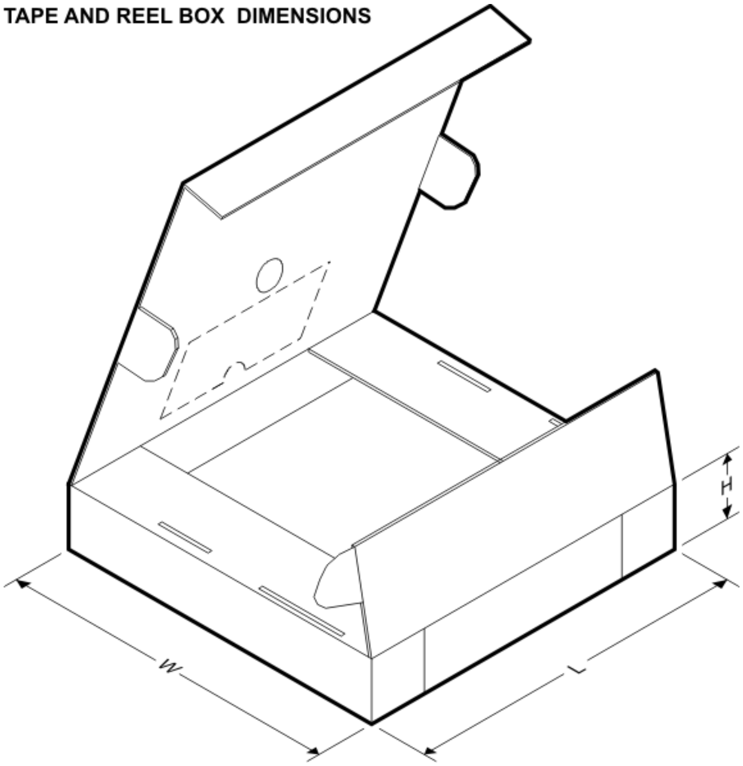
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

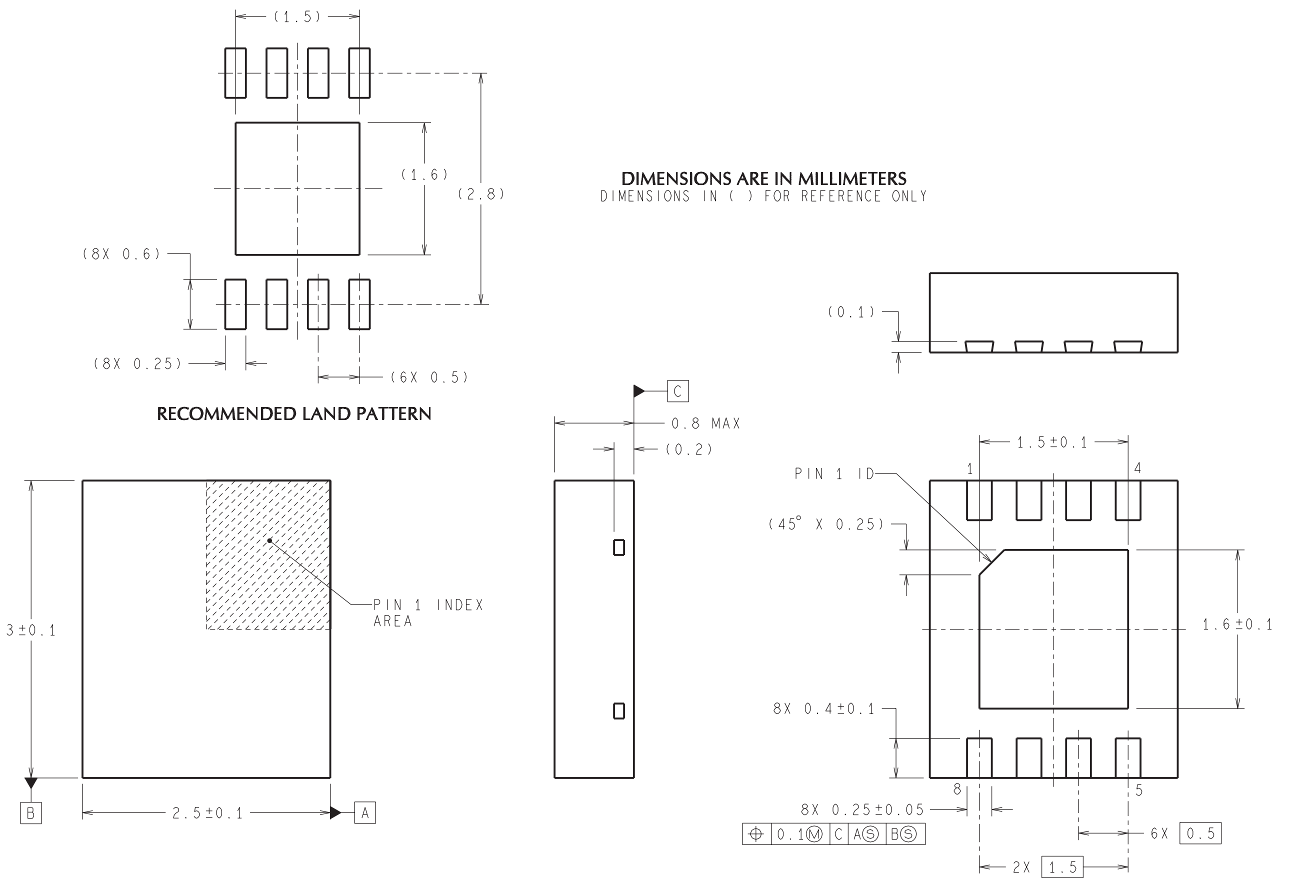
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6552MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6552SD/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LMH6552SDX/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



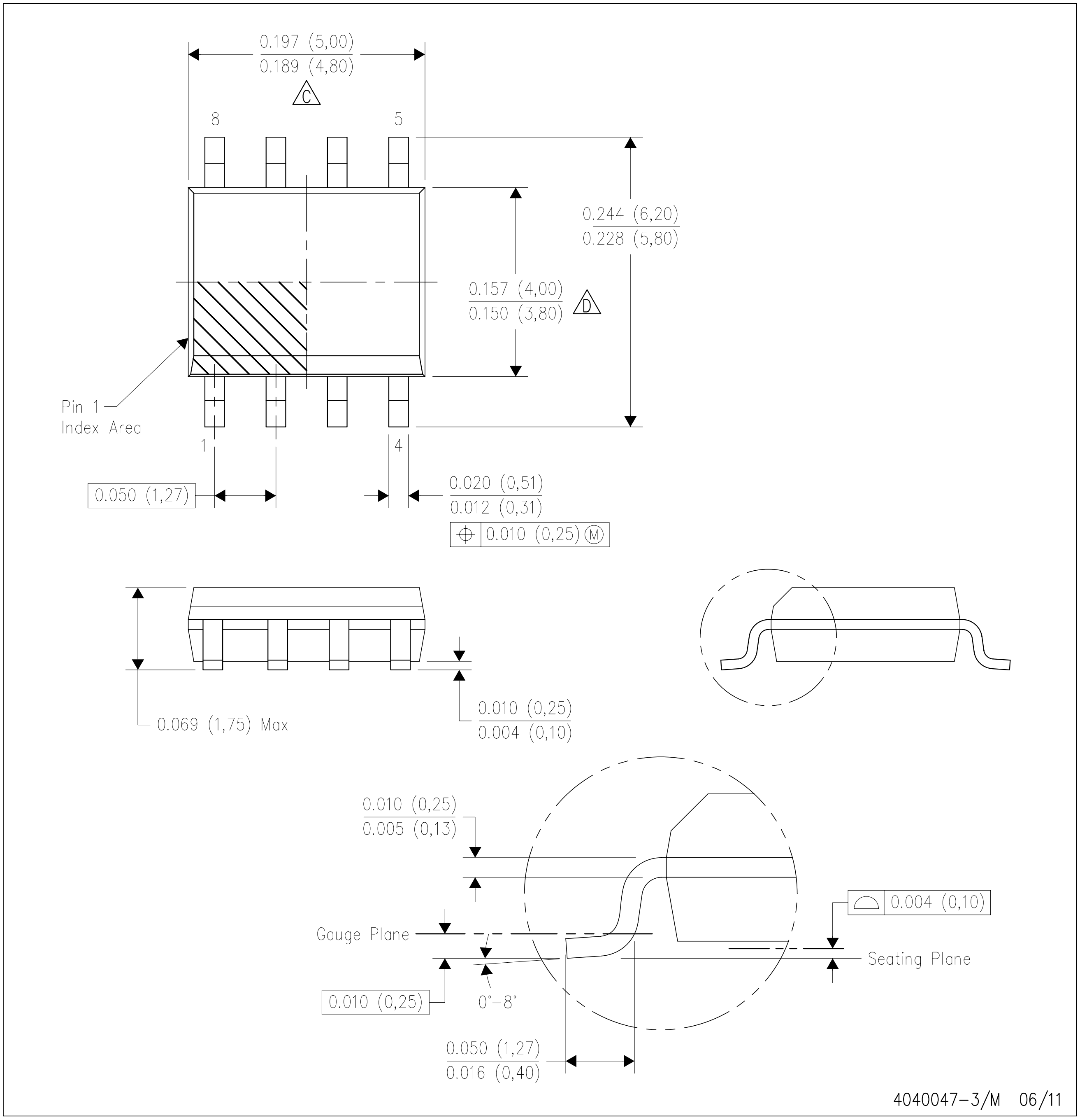
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6552MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6552SD/NOPB	WSON	NGS	8	1000	210.0	185.0	35.0
LMH6552SDX/NOPB	WSON	NGS	8	4500	367.0	367.0	35.0


(1.5)
(1.6)
(2.8)
(8X 0.6)
(8X 0.25)
(6X 0.5)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
C
0.8 MAX
(0.2)
3±0.1
PIN 1 INDEX AREA
B
2.5±0.1
A
1.5±0.1
1
4
PIN 1 ID
(45° X 0.25)
1.6±0.1
8X 0.4±0.1
8
5
8X 0.25±0.05
0.1 M C A S B S
6X 0.5
2X 1.5

SDA08C (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265