

LMP8671, LMP8672, LMP8674

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#### SNOSB39B-JULY 2011-REVISED MARCH 2013

# Single, Dual, and Quad 40V Low Noise Precision Amplifiers

Check for Samples: LMP8671, LMP8672, LMP8674

## **FEATURES**

- **Output Short Circuit Protection**
- PSRR and CMRR Exceed 110dB
- Best in Class Linearity (135dB)

## APPLICATIONS

- Low Noise Industrial Applications Including Test, Measurement, and Ultrasound
- **Precision Active Filters**
- **PLL Filters**
- 4-20mA Current Loops
- Motor Control

## **KEY SPECIFICATIONS**

- Input Offset Voltage 0.4mV
- TC Vos 2µV/°C (max)
- Power Supply Voltage Range ±2.5V to ±20V
- Voltage Noise Density 2.5nV/VHz
- Slew Rate ±20V/µs
- Gain Bandwidth Product 55MHz
- **Open Loop Gain 135dB**
- **Input Bias Current 10nA**

### **Connection Diagrams**

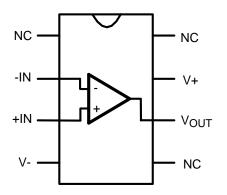


Figure 1. See Package Number — D0008A

### DESCRIPTION

The LMP8671/2/4 combines great precision, low noise and a large operating voltage range to provide a high SNR and a wide dynamic range. Its AC performance allows it to be used over a wide frequency without degradation. It is the ideal choice for applications requiring DC precision and low noise such as precision PLL filters, multi feedback and multi pole active filters, GPS receivers and precision control loop systems. The LMP8671/2/4 offers an extremely high open loop gain of 135dB, low voltage noise density (2.5nV/ $\sqrt{Hz}$ ), and a superb linearity of 0.000009%. These characteristics drastically reduce gain error which is a challenge in accurate systems requiring higher gains such as data acquisition systems.

To ensure that the most challenging loads are driven without compromise, the LMP8671/2/4 has a high slew rate of ±20V/µs and an output current capability of ±26mA.

The LMP8671/2 family of high-voltage amplifiers are available in SOIC-8, the LMP8674 in SOIC-14.

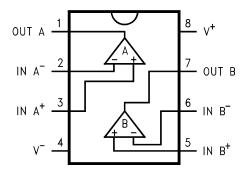


Figure 2. See Package Number — D0008A

AA

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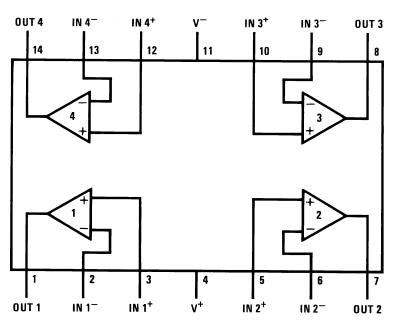


Figure 3. See Package Number — D0014A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

Power Supply Voltage ( $V_S = V^+ - V^-$ )		46V
Storage Temperature	−65°C to 150°C	
Input Voltage		(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit <sup>(4)</sup>		Continuous
Power Dissipation	Internally Limited	
ESD Rating <sup>(5)</sup>		2000V
ESD Rating <sup>(6)</sup>	Pins 1, 4, 7 and 8	200V
	Pins 2, 3, 5 and 6	100V
Junction Temperature		150°C
Thermal Resistance	θ <sub>JA</sub> (SO)	145°C/W
For soldering specifications, http://www.t	i.com/lit/SNOA549	

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub> or the number given in *Absolute Maximum Ratings*, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.

### **Operating Ratings**

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	-40°C ≤ T <sub>A</sub> ≤ 125°C
Supply Voltage Range LMP8671/2/4	$\pm 2.5 \forall \le \forall_{\text{S}} \le \pm 22 \forall$



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## Electrical Characteristics for the LMP8671/2/4<sup>(1)</sup>

The following specifications apply for  $V_S = \pm 20V$ ,  $R_L = 2k\Omega$ ,  $R_{SOURCE} = 10\Omega$ ,  $f_{IN} = 1$ kHz,  $T_A = 25$ °C, unless otherwise specified. **Boldface** limits apply at the temperature extremes.

0	Bananatan	O an l'itland	LMP86	Units	
Symbol	Parameter	Conditions	Typical <sup>(2)</sup>	Limit <sup>(3)</sup>	(Limits)
V <sub>OS</sub>	Offset Voltage		±100	±400 <b>±750</b>	μV (max)
$\Delta V_{OS} / \Delta Temp$	Average Input Offset Voltage Drift vs Temperature	–40°C ≤ T <sub>A</sub> ≤ 125°C	0.1	2	μV/°C (max)
		$V_{CM} = 0V$			
	lagut Diag Ourregt	LMP8671/4	10	±75 <b>±95</b>	nA (max)
I <sub>B</sub>	Input Bias Current	$V_{CM} = 0V$			
		LMP8672	50	±200 <b>±250</b>	nA (max)
		$V_{CM} = 0V$			
	Input Offect Ourrent	LMP8671/4	11	±50 <b>±95</b>	nA (max)
l <sub>os</sub>	Input Offset Current	$V_{CM} = 0V$			
		LMP8672	25	±100 <b>±125</b>	nA (max)
ΔI <sub>OS</sub> /ΔTemp	Input Bias Current Drift vs Temperature	–40°C ≤ T <sub>A</sub> ≤ 125°C	0.2		nA/°C
V <sub>IN-CM</sub>	Common-Mode Input Voltage Range		+17.1 -16.9		V (min) V (min)
7	Differential Input Impedance		30		kΩ
Z <sub>IN</sub>	Common Mode Input Impedance	-10V <vcm<10v< td=""><td>1000</td><td></td><td>MΩ</td></vcm<10v<>	1000		MΩ
	Equivalent Input Noise Voltage	20Hz to 20kHz	0.34	0.65	μV <sub>RMS</sub> (max)
e <sub>n</sub>	Equivalent Input Noise Density	f = 1kHz	2.5	4.7	nV/√Hz (max)
i <sub>n</sub>	Current Noise Density	f = 1kHz f = 10Hz	1.6 3.1		pAl√Hz
THD+N	Total Harmonic Distortion + Noise	$A_V = 1$ , $V_{OUT} = 3V_{rms}$ , $R_L = 600\Omega$	0.00003	0.00009	% (max)
t <sub>S</sub>	Settling time	$A_V = -1$ , 10V step, $C_L = 100 pF$ 0.1% error range	1.2		μs
GBWP	Gain Bandwidth Product		55	45	MHz (min)
SR	Slew Rate		±20	±15	V/µs (min)
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage	See <sup>(4)</sup>	125	110 <b>100</b>	dB (min)
CMRR	Common-Mode Rejection	–15V≤Vcm≤15V	115	105 <b>100</b>	dB (min)
A <sub>VOL</sub>	Open Loop Voltage Gain	$-15V \le Vout \le 15V$ R <sub>L</sub> = 2k $\Omega$	135	125	dB (min)
V <sub>OUTMAX</sub>	Maximum Output Voltage Swing	$R_L = 2k\Omega$	±19.0	±18.8 ±18.6	V (min)
I <sub>OUT-CC</sub>	Instantaneous Short Circuit Current		+53 -42		mA

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) Typical values represent most likely parametric norms at T<sub>A</sub> = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(3) Datasheet min/max specification limits are ensured by test or statistical analysis.

(4) PSRR is measured as follows: For V<sub>S</sub>, V<sub>OS</sub> is measured at two supply voltages, ±5V and ±20V, PSRR =  $|20log(\Delta V_{OS}/\Delta V_S)|$ .

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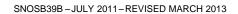
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## Electrical Characteristics for the LMP8671/2/4<sup>(1)</sup> (continued)

The following specifications apply for  $V_S = \pm 20V$ ,  $R_L = 2k\Omega$ ,  $R_{SOURCE} = 10\Omega$ ,  $f_{IN} = 1kHz$ ,  $T_A = 25^{\circ}C$ , unless otherwise specified. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	LMP86	LMP8671/2/4			
	Parameter	Conditions	Typical <sup>(2)</sup>	Limit <sup>(3)</sup>	(Limits)		
R <sub>OUT</sub>	Output Impedance	f <sub>IN</sub> = 10kHz Closed-Loop Open-Loop	0.01 13		Ω		
I <sub>OUT</sub>	Output Current	$R_L = 2k\Omega$	9.5	9.3	mA (min)		
		I <sub>OUT</sub> = 0mA					
I <sub>S</sub>	Total Quiescent Current	LMP8671	5	6 <b>8</b>	mA (max)		
		LMP8672	12.5	16	mA (max)		
		LMP8674	20	22	mA (max)		

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**Typical Performance Characteristics** 

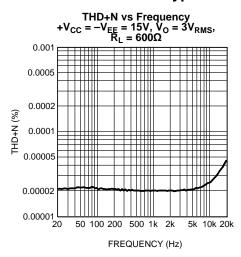
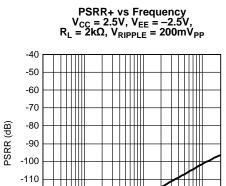
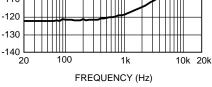
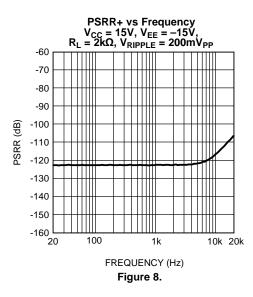


Figure 4.









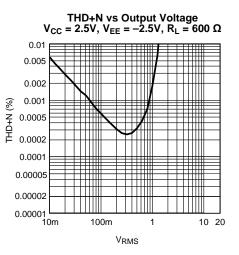


Figure 5.

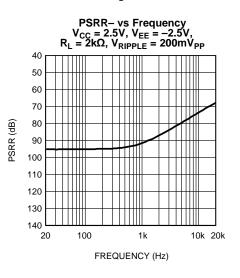
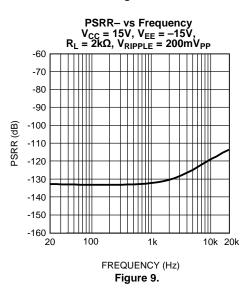
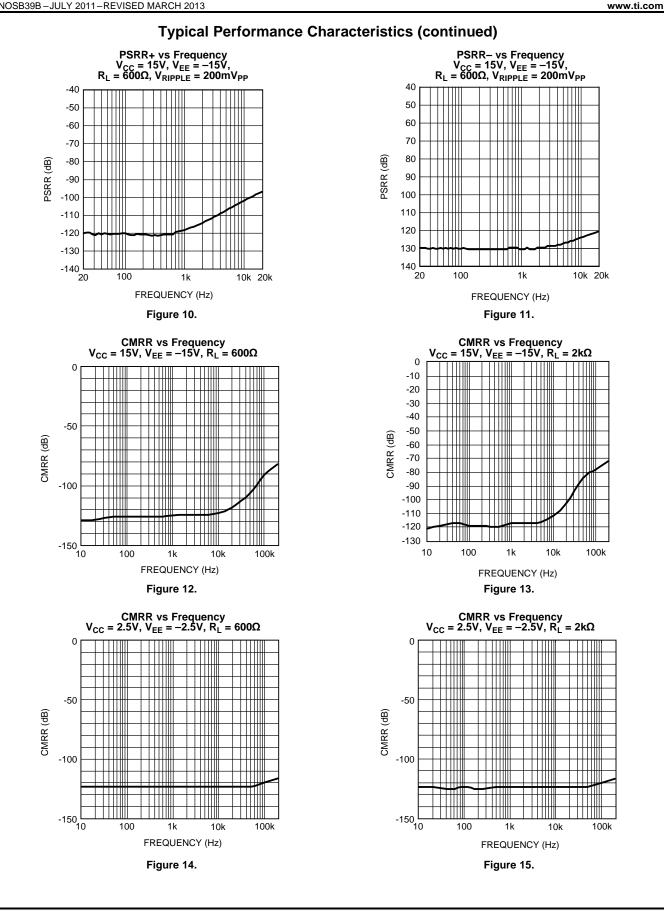


Figure 7.



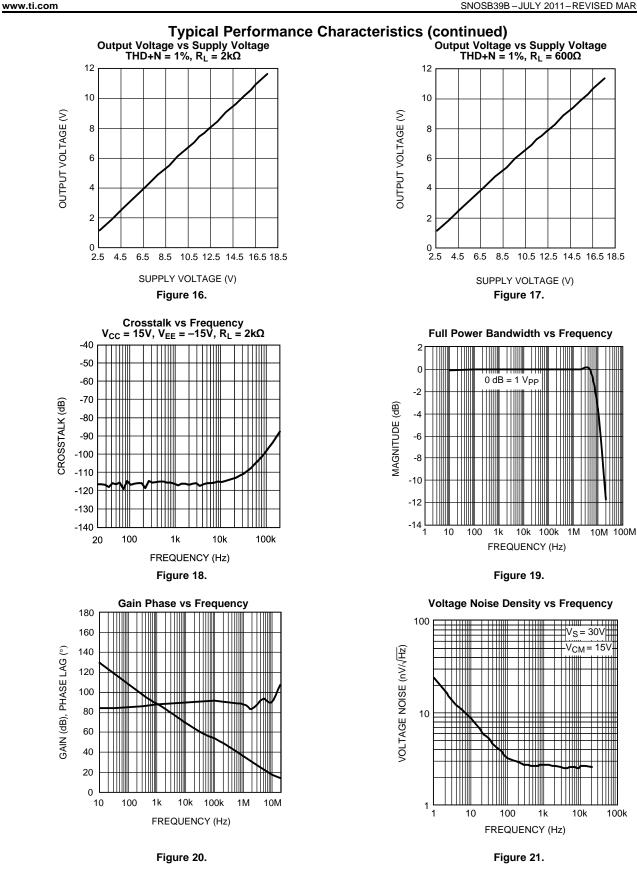
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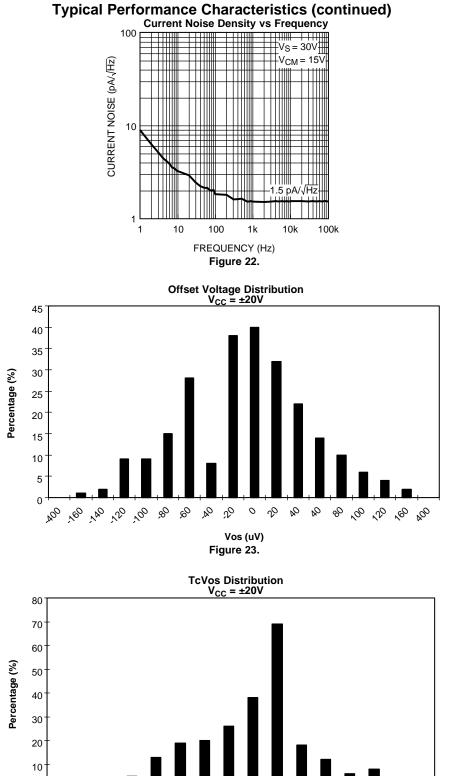
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-0.9 -0.8 -0.7 -0.6 -0.5 -0.4 -0.3 -0.2 -0.1 0

8

0

-2 -1.2 -1.1 -1

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## **REVISION HISTORY**

# Changes from Revision A (March 2013) to Revision B

•	Changed layout of National Data Sheet to TI format
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17-May-2013

## PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
LMP8671MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 71MA	Samples
LMP8671MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 71MA	Samples
LMP8672MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA	Samples
LMP8672MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 72MA	Samples
LMP8674MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8674 MA	Samples
LMP8674MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8674 MA	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



17-May-2013

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# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal												
Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8671MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8672MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8674MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

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# PACKAGE MATERIALS INFORMATION

8-Apr-2013



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8671MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8672MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8674MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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