Phase Dimmable Offline LED Driver with Integrated FET

Check for Samples: LM3448

FEATURES

- **Input phase angle dim decoder circuit for LED dimming**
- **Integrated, vertical 600V MOSFET with superior avalanche energy capability**
- **Application voltage range $85V_{AC}$ – $265V_{AC}$**
- **Adjustable switching frequency**
- **Adaptive programmable off-time allows for constant ripple current**
- **No 120Hz flicker possible**
- **Low quiescent current**
- **Thermal shutdown**
- **Low profile 16-pin Narrow SOIC package**
- **Wave solder capable**

APPLICATIONS

- **Retrofit TRIAC Dimming**
- **Solid State Lighting**
- **Industrial and Commercial Lighting**
- **Residential Lighting**

DESCRIPTION

The LM3448 is an adaptive constant off-time AC/DC buck (step-down) constant current LED regulator designed to be compatible with TRIAC dimmers. The LM3448 provides a constant current for illuminating high power LEDs and includes a phase angle dim decoder. The dim decoder allows wide range LED dimming using standard forward and reverse phase TRIAC dimmers. The integrated high-voltage and low Rdson MOSFET reduces design complexity while improving LED driver efficiency. The integrated and patented architecture facilitates implementation of small form factor LED drivers suitable for integrated LED lamps with very low external component count. The LM3448 also provides the flexibility required to implement both isolated and non-isolated solutions based on the Flyback, Buck or Buck-Boost topology using either active or passive power factor correction (Valley-Fill) circuits. Additional features include thermal shutdown, current limit and V_{CC} under-voltage lockout.

Typical LM3448 LED Driver Application Circuit

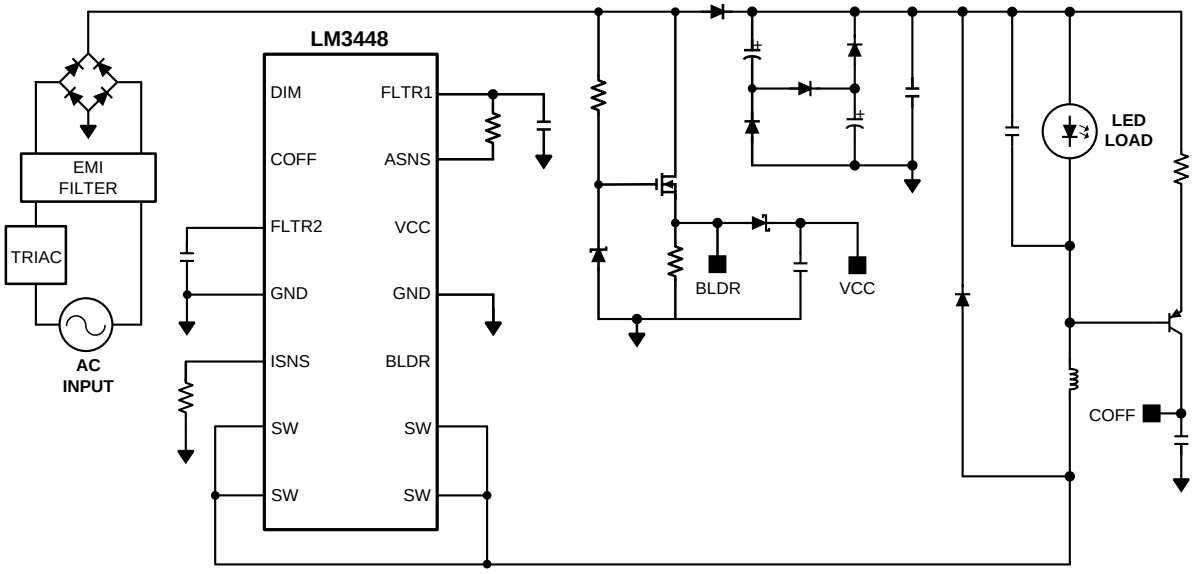


Figure 1. Typical Application Circuit

Connection Diagram

Top View

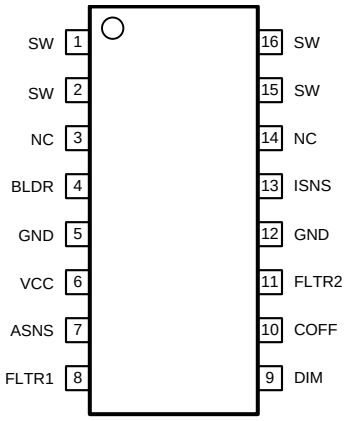


Figure 2. 16-Lead Narrow SOIC Package

PIN DESCRIPTIONS

Pin(s)	Name	Description
1, 2, 15, 16	SW	Drain connection of internal 600V MOSFET.
3, 14	NC	No connect. Provides clearance between high voltage and low voltage pins. Do not tie to GND.
4	BLDR	Bleeder pin. Provides the input signal to the angle detect circuitry. A 230Ω internal resistor ensures BLDR is pulled down for proper angle sense detection.
5, 12	GND	Circuit ground connection.
6	VCC	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver. Connect a 22uF (minimum) bypass capacitor to ground.
7	ASNS	PWM output of the TRIAC dim decoder circuit. Outputs a 0 to 4V PWM signal with a duty cycle proportional to the TRIAC dimmer on-time.
8	FLTR1	First filter input. The 120Hz PWM signal from ASNS is filtered to a DC signal and compared to a 1 to 3V, 5.85 kHz ramp to generate a higher frequency PWM signal with a duty cycle proportional to the TRIAC dimmer firing angle. Pull above 4.9V (typical) to TRI-STAT DIM.
9	DIM	Input/output dual function dim pin. This pin can be driven with an external PWM signal to dim the LEDs. It may also be used as an output signal and connected to the DIM pin of other LM3448/LM3445 devices or LED drivers to dim multiple LED circuits simultaneously.
10	COFF	OFF time setting pin. A user set current and capacitor connected from the output to this pin sets the constant OFF time of the switching controller.
11	FLTR2	Second filter input. A capacitor tied to this pin filters the PWM dimming signal to supply a DC voltage to control the LED current. Could also be used as an analog dimming input.
13	ISNS	LED current sense pin (internally connected to MOSFET source). Connect a resistor from ISNS to GND to set the maximum LED current.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

		VALUE / UNIT
SW to GND		-0.3V to +600V
BLDR to GND		-0.3V to +17V
VCC, FLTR1 to GND		-0.3V to +14V
ISNS to GND		-0.3V to +2.5V
ASNS, DIM, FLTR2, COFF to GND		-0.3V to +7.0V
SW FET Drain Current:	Peak	1.2A
	Continuous	Limited by T_{J-MAX}
Continuous Power Dissipation (2)		Internally Limited
ESD Susceptibility:	HBM (3)	2 kV
Junction Temperature (T_{J-MAX})		125°C
Storage Temperature Range		-65°C to +150°C
Maximum Lead Temperature (Solder and Reflow)		260°C

(1) Absolute Maximum Ratings are limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin unless otherwise specified.

(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at approximately T_J = 165°C (typ.) and disengages at approximately T_J = 145°C (typ).

(3) Human Body Model, applicable std. JESD22-A114-C.

OPERATING CONDITIONS (1)

	VALUE/ UNIT
V_{CC}	8V to 12V
Junction Temperature Range	−40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin unless otherwise specified.

ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 12V unless otherwise noted. Limits in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25ºC and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
BLEEDER						
R_{BLDR}	Bleeder resistance to GND	I_{BLDR} = 10mA		230	**325**	Ω
V_{CC} SUPPLY						
I_{VCC}	Operating supply current	Non-switching		2.00	**2.85**	mA
$V_{CC-UVLO}$	Rising threshold			7.4	**7.7**	V
	Falling threshold		**6.0**	6.4		
	Hysterisis			1		
COFF						
V_{COFF}	Time out threshold		**1.225**	1.276	**1.327**	V
R_{COFF}	Off timer sinking impedance			33	**60**	Ω
t_{COFF}	Restart timer			180		µs
CURRENT LIMIT						
V_{ISNS}	ISNS limit threshold		**1.174**	1.269	**1.364**	V
t_{ISNS}	Leading edge blanking time			125		ns
	Current limit reset delay			180		µs
INTERNAL PWM RAMP						
f_{RAMP}	Frequency			5.85		kHz
V_{RAMP}	Valley voltage		**0.96**	1.00	**1.04**	V
	Peak voltage		**2.85**	3.00	**3.08**	
D_{RAMP}	Maximum duty cycle		**96.5**	98.0		%
DIM DECODER						
V_{ANG_DET}	Angle detect rising threshold	Observed on BLDR pin	**6.79**	7.21	**7.81**	V
V_{ASNS}	ASNS filter delay			4		µs
	ASNS VMAX		**3.81**	3.96	**4.11**	V
I_{ASNS}	ASNS drive capability sink	V_{ASNS} = 2V		-7.6		mA
	ASNS drive capability source	V_{ASNS} = 2V		4.3		
I_{DIM}	DIM low sink current	V_{DIM} = 1V		-2.80	**-1.65**	
	DIM high source current	V_{DIM} = 4V	**3.00**	4.00		
V_{DIM}	DIM low voltage	PWM input voltage threshold	**0.9**	1.33		V
	DIM high voltage			2.33	**3.15**	
V_{TSTH}	TRI-STATE threshold voltage	Apply to FLTR1 pin		4.87	**5.25**	V
R_{DIM}	DIM comparator TRI-STATE impedance		**10**			MΩ
CURRENT SENSE COMPARATOR						
V_{FLTR2}	FLTR2 open circuit voltage		**720**	750	**780**	mV
R_{FLTR2}	FLTR2 impedance			420		kΩ
OUTPUT MOSFET (SW FET)						
V_{BVDS}	SW to ISNS breakdown voltage		600	660		V

(1) Absolute Maximum Ratings are limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin unless otherwise specified.

(2) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(3) Typical numbers are at 25°C and represent the most likely norm.

ELECTRICAL CHARACTERISTICS[1] (continued)

V_{CC} = 12V unless otherwise noted. Limits in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25ºC and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
I_{DS}	SW to ISNS leakage current [4]	SW - ISNS = 600V			1	µA
R_{ON}	SW to ISNS switch on resistance			3.6		Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	See [5]		165		°C
	Thermal shutdown hysteresis			20		
THERMAL RESISTANCE						
$R\theta_{JA}$	Junction to Ambient	See [5] [6]		95		°C/W

(4) High voltage devices such as the LM3448 are susceptible to increased leakage currents when exposed to high humidity and high pressure operating environments. Users of this device are cautioned to satisfy themselves as to the suitability of this product in the intended end application and take any necessary precautions (e.g. system level HAST/HALT testing, conformal coating, potting, etc.) to ensure proper device operation.

(5) These electrical parameters are specified by design and are not verified by test.

(6) This $R\theta_{JA}$ typical value determined using JEDEC specifications JESD51-1 to JESD51-11. However junction-to-ambient thermal resistance is highly board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C and V_{CC} = 12V unless otherwise specified.

Efficiency vs. Input Line Voltage(1)

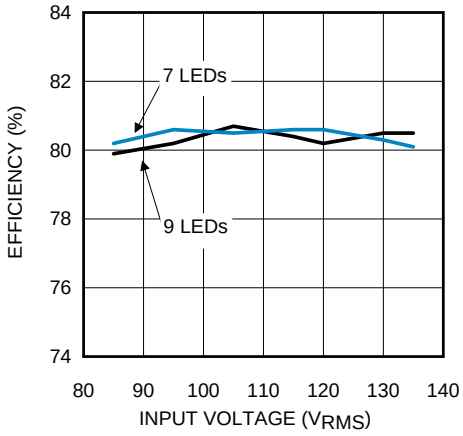


Figure 3.

Power Factor vs. Input Line Voltage(1)

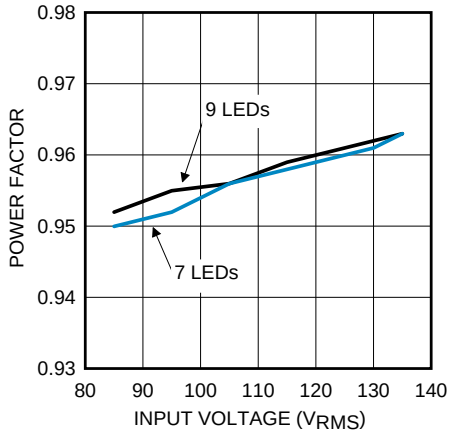


Figure 4.

LED Current vs. Input Line Voltage(2)

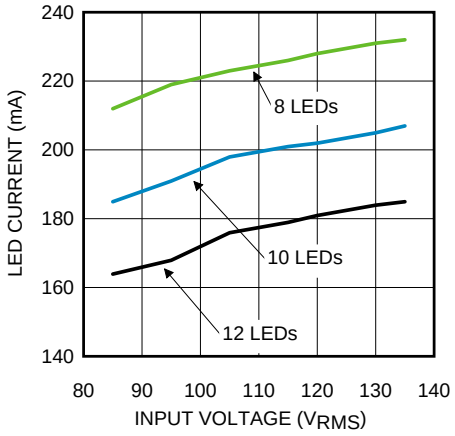


Figure 5.

f_{SW} vs. Input Line Voltage(2)

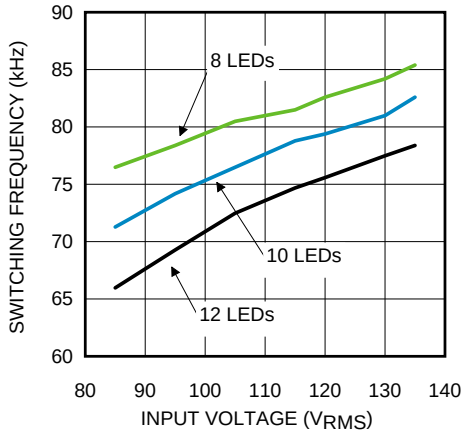


Figure 6.

Min On-Time (t_{ON}) vs. Temperature

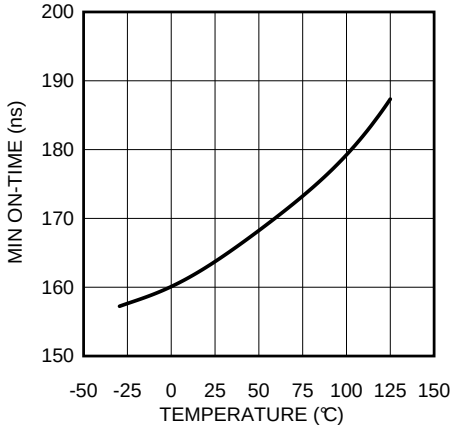


Figure 7.

BLDR Resistor vs. Temperature

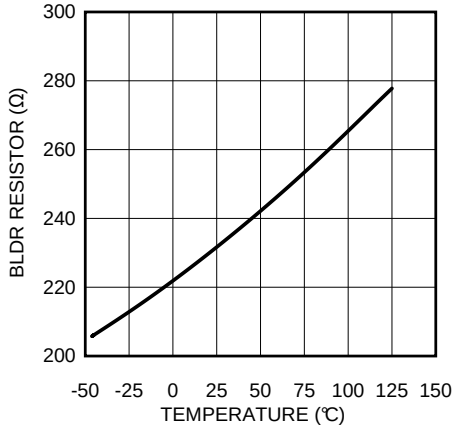


Figure 8.

(1) Data used for this plot taken from Design #3.
(2) Data used for this plot taken from Design #2.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C and V_{CC} = 12V unless otherwise specified.

V_{CC} UVLO vs. Temperature

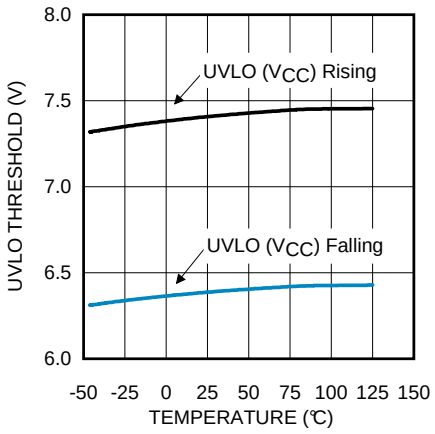


Figure 9.

V_{COFF} Threshold vs. Temperature

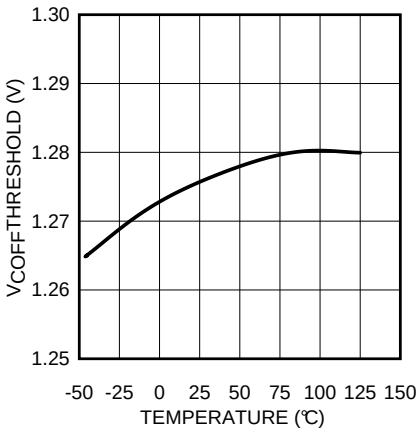


Figure 10.

Angle Detect Threshold vs. Temperature

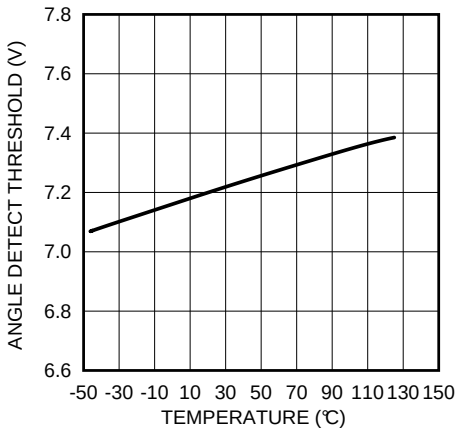


Figure 11.

Leading Edge Blanking Variation Over Temperature

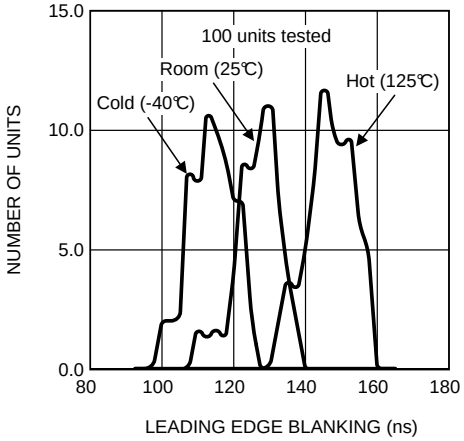


Figure 12.

DIM Pin Duty Cycle vs. FLTR1 Voltage(3)

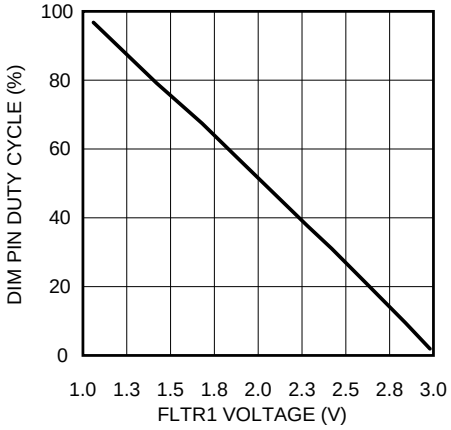


Figure 13.

(3) Data used for this plot taken from Design #3.

SIMPLIFIED INTERNAL BLOCK DIAGRAM

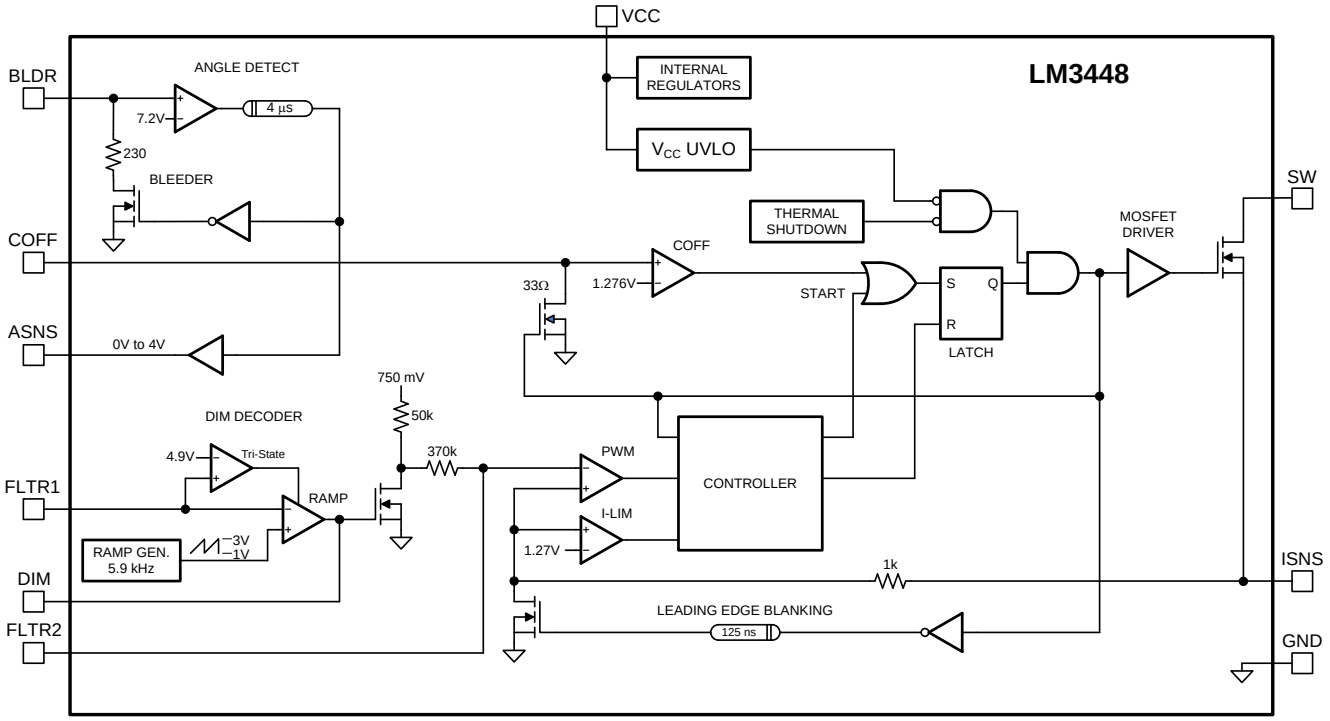


Figure 14. Simplified Block Diagram

THEORY OF OPERATION

The LM3448 contains all the necessary circuitry to build a line-powered (mains powered) constant current LED driver whose output current can be controlled with a conventional TRIAC dimmer.

OVERVIEW OF PHASE CONTROL DIMMING

A basic "phase controlled" TRIAC dimmer circuit is shown in Figure 15.

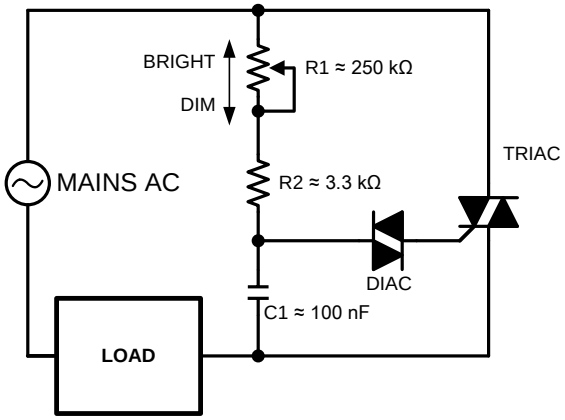


Figure 15. Basic TRIAC Dimmer

An RC network consisting of R1, R2, and C1 delay the turn on of the TRIAC until the voltage on C1 reaches the trigger voltage of the diac. Increasing the resistance of the potentiometer (wiper moving downward) increases the turn-on delay which decreases the on-time or "conduction angle" of the TRIAC (θ). This reduces the average power delivered to the load.

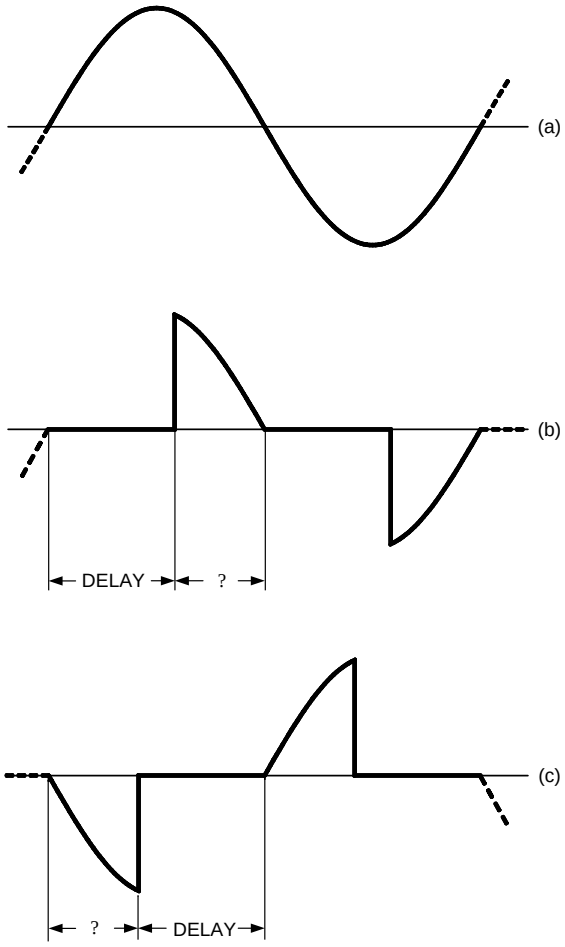


Figure 16. Line Voltage and Dimming Waveforms

Voltage waveforms for a simple TRIAC dimmer are shown in Figure 16. Figure 16(a) shows the full sinusoid of the input voltage. Even when set to full brightness, few dimmers will provide 100% on-time (i.e. the full sinusoid). Figure 16(b) shows a theoretical waveform from a dimmer. The on-time is often referred to as the "conduction angle" and may be stated in degrees or radians. The off-time represents the delay caused by the RC circuit feeding the TRIAC. The off-time can be referred to as the "firing angle" and is simply (180° - θ).

Figure 16(c) shows a waveform from a reverse phase dimmer, sometimes referred to as an electronic dimmer. These typically are more expensive, microcontroller based dimmers that use switching elements other than TRIACs. Note that the conduction starts from the zero-crossing and terminates some time later. This method of control reduces the noise spike at the transition. Since the LM3448 has been designed to assess the relative on-time and control the LED current accordingly, most phase control dimmers both forward and reverse phase may be used with success.

A bridge rectifier converts the line (mains) voltage of Figure 17(b) into a series of half-sines as shown in Figure 17(a).

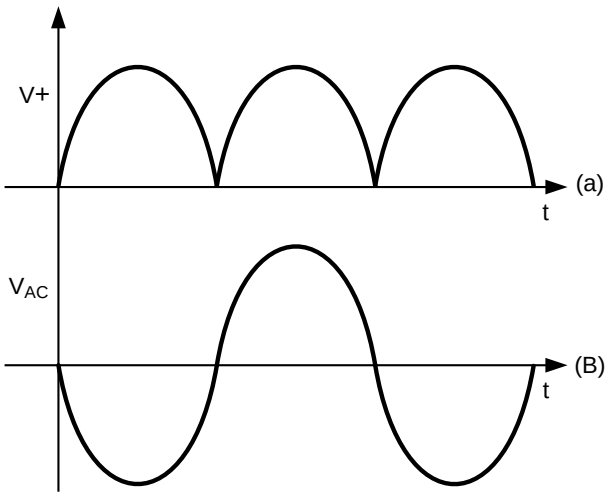


Figure 17. Voltage Waveforms After Bridge Rectifier Without TRIAC Dimming

Figure 18(b) and Figure 18(a) show typical TRIAC dimmed voltage waveforms before and after the bridge rectifier.

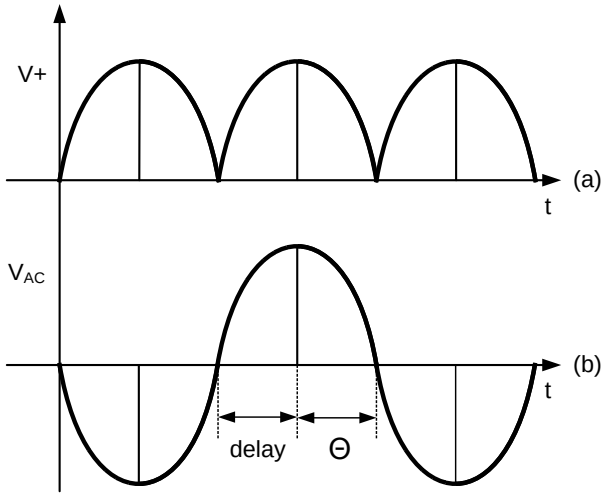


Figure 18. Voltage Waveforms After Bridge Rectifier With TRIAC Dimming

SENSING THE RECTIFIED TRIAC WAVEFORM

An external series pass regulator (R2, D1, and Q1) translates the rectified line voltage to a level where it can be sensed by the BLDR pin on the LM3448 as shown in Figure 19.

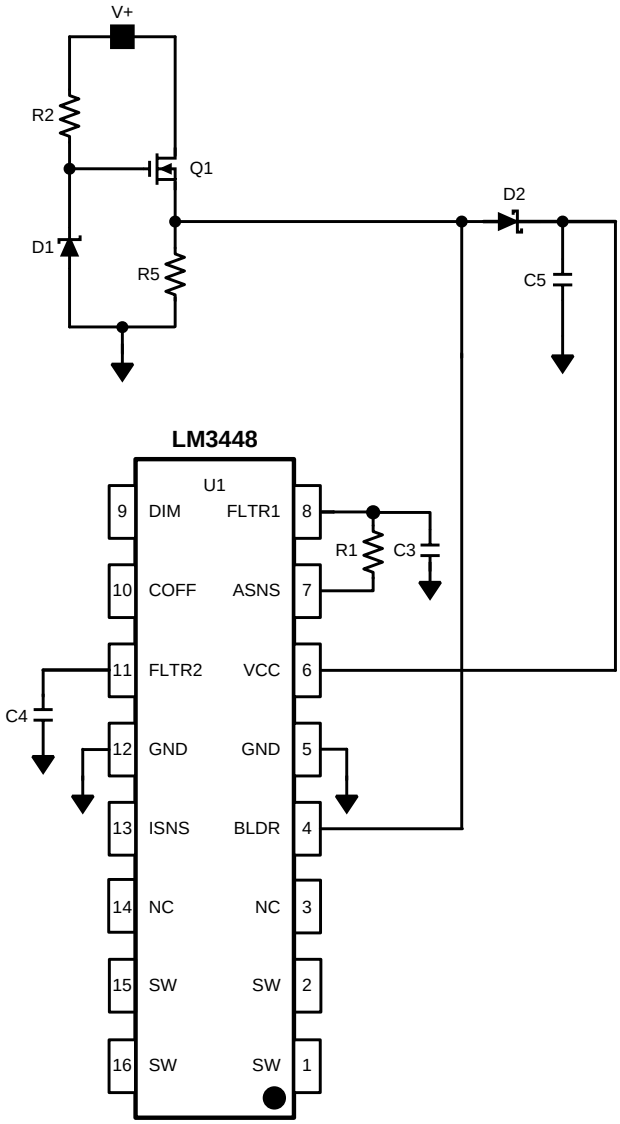


Figure 19. AC Line Sense Circuitry

D1 is typically a 15V zener diode which forces transistor Q1 to “stand-off” most of the rectified line voltage. Having no capacitance on the source of Q1 allows the voltage on the BLDR pin to rise and fall with the rectified line voltage as the line voltage drops below zener voltage D1 (see the section on Angle Detect).

A diode-capacitor network (D2, C5) is used to maintain the voltage on the VCC pin while the voltage on the BLDR pin goes low. This provides the supply voltage to operate the LM3448.

Resistor R5 is used to bleed charge out of any stray capacitance on the BLDR node and may be used to provide the necessary holding current for the dimmer when operating at light output currents.

ANGLE DETECT

The Angle Detect circuit uses a comparator with a fixed threshold voltage of 7.21V to monitor the BLDR pin to determine whether the TRIAC is on or off. The output of the comparator drives the ASNS buffer and also controls the bleeder circuit. A 4s delay line on the output is used to filter out noise that could be present on this signal.

The output of the Angle Detect circuit is limited to a 0V to 4.0V swing by the buffer and presented to the ASNS pin. R1 and C3 comprise a low-pass filter with a bandwidth on the order of 1.0Hz.

The Angle Detect circuit and its filter produce a DC level which corresponds to the duty cycle (relative on-time) of the TRIAC dimmer. As a result, the LM3448 will work equally well with 50Hz or 60Hz line voltages.

BLEEDER

While the BLDR pin is below the 7.21V threshold, the internal bleeder MOSFET is on to place a small load (230Ω) on the series pass regulator. This additional load is necessary to complete the circuit through the TRIAC dimmer so that the dimmer delay circuit can operate correctly. Above 7.21V, the bleeder resistor is removed to increase efficiency.

FLTR1 PIN

The FLTR1 pin has two functions. Normally it is fed by ASNS through filter components R1 and C3 and drives the dim decoder. However if the FLTR1 pin is tied above 4.9V (e.g., to VCC) the ramp comparator is at TRI-STATE disabling the dim decoder.

DIM DECODER

The ramp generator produces a 5.85 kHz saw tooth wave with a minimum of 1.0V and a maximum of 3.0V. The filtered ASNS signal enters pin FLTR1 where it is compared against the output of the Ramp Generator. The output of the ramp comparator will have an on-time which is inversely proportional to the average voltage level at pin FLTR1. However since the FLTR1 signal can vary between 0V and 4.0V (the limits of the ASNS pin), and the ramp generator signal only varies between 1.0V and 3.0V, the output of the ramp comparator will be on continuously for V_{FLTR1} < 1.0V and off continuously for V_{FLTR1} > 3.0V. This allows a decoding range from 45° to 135° to provide a 0 – 100% dimming range.

The output of the ramp comparator drives both a common source N-channel MOSFET through a Schmitt trigger and the DIM pin. The MOSFET drain is pulled up to 750 mV by a 50kΩ resistor.

Since the MOSFET inverts the output of the ramp comparator, the drain voltage of the MOSFET is proportional to the duty cycle of the line voltage that comes through the TRIAC dimmer. The amplitude of the ramp generator causes this proportionality to "hard limit" for duty cycles above 75% and below 25%.

FLTR2

The MOSFET drain signal next passes through an RC filter comprised of an internal 370kΩ resistor and an external capacitor on pin FLTR2. This forms a second low pass filter to further reduce the ripple in this signal which is used as a reference by the PWM comparator. This RC filter is generally set to 10Hz.

The net effect is that the output of the dim decoder is a DC voltage whose amplitude varies from near 0V to 750 mV as the duty cycle of the dimmer varies from 25% to 75%. This corresponds to conduction angles of 45° to 135°.

The output voltage of the dim decoder directly controls the peak current that will be delivered by the internal SW FET.

As the TRIAC fires beyond 135°, the DIM decoder no longer controls the dimming. At this point the LEDs will dim gradually for one of two reasons:

- The voltage at V_{BUCK} decreases and the buck converter runs out of headroom and causes LED current to decrease as V_{BUCK} decreases.
- Minimum on-time is reached which fixes the duty-cycle and therefore reduces the voltage at V_{BUCK}.

The transition from dimming with the DIM decoder to headroom or minimum on-time dimming is seamless. LED currents from full load to as low as 0.5mA can be easily achieved.

COFF AND CONSTANT OFF-TIME CONTROL OVERVIEW

The LM3448 is a buck regulator that uses a proprietary constant off-time method to maintain constant current through a string of LEDs as shown in Figure 20.

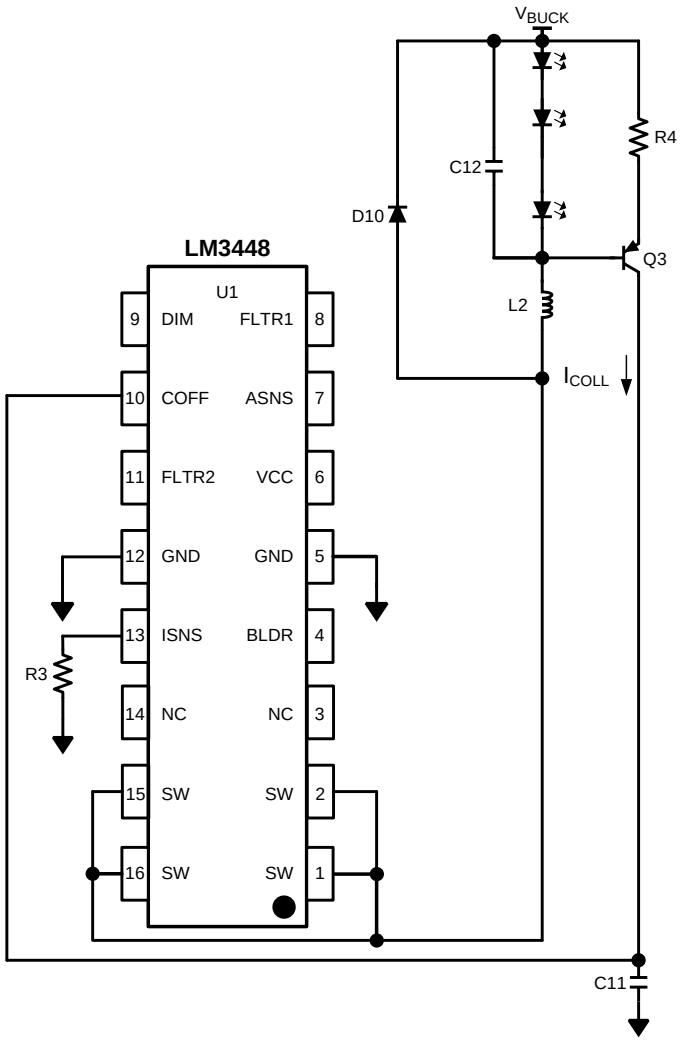


Figure 20. Simplified Buck Regulation Circuit

Constant off-time control architecture operates by simply defining the off-time and allowing the on-time, and therefore the switching frequency, to vary as either V_{IN} or V_O changes. The output voltage is equal to the LED string voltage (V_{LED}), and should not change significantly for a given application. The input voltage or V_{BUCK} in this analysis will vary as the input line varies. The length of the on-time is determined by the sensed inductor current through a resistor to a voltage reference at a comparator. During the on-time denoted by t_{ON}, the SW FET is on causing the inductor current to increase (see Figure 21). During the on-time, current flows from V_{BUCK} through the LEDs, L2, the LM3448's internal SW FET and finally through R3 to ground. At some point in time the inductor current reaches a maximum ($I_{L2\text{-}PK}$) determined by the voltage at the ISNS pin. This sensed voltage across R3 is compared against the dim decoder voltage on FLTR2 at which point the SW FET is turned off by the regulator. During the off-period denoted by t_{OFF}, the current through L2 continues to flow through the LEDs via D10. Capacitor C12 eliminates most of the ripple current seen in the inductor. Resistor R4, capacitor C11 and transistor Q3 provide a linear current ramp that in conjunction with the COFF comparator threshold sets the constant off-time for a given output voltage.

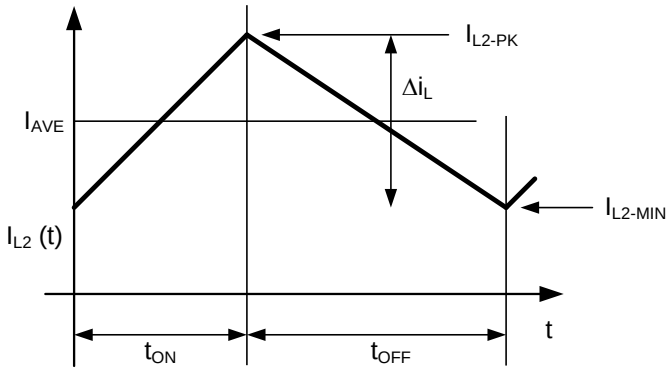


Figure 21. Inductor Current Waveform in CCM

VCC BIAS SUPPLY

The LM3448 requires a supply voltage at the VCC pin in the range of 8V to 12V. The device has V_{CC} under-voltage lockout (UVLO) with rising and falling thresholds of 7.4V and 6.4V respectively. Methods for supplying the V_{CC} voltage are discussed in the "Design Considerations" section of this datasheet.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the internal SW FET when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the SW FET will not turn on until the junction temperature drops to approximately 145°C.

Design Considerations

VALLEY-FILL POWER FACTOR CORRECTION

For the non-isolated buck converter, a valley-fill power factor correction (PFC) circuit shown in Figure 22 provides a simple means of improving the converter's power factor performance.

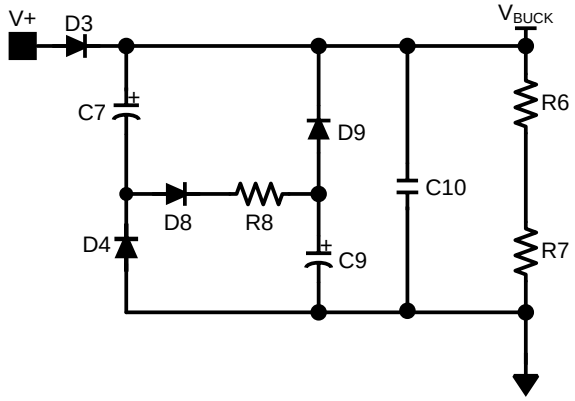


Figure 22. Two Stage Valley Fill Circuit

The valley-fill circuit allows the buck regulator to draw power throughout a larger portion of the AC line. This allows the capacitance needed at V_{BUCK} to be lower than if there were no valley-fill circuit and adds passive power factor correction (PFC) to the application. Besides better power factor correction, a valley-fill circuit allows the buck converter to operate while separate circuitry translates the dimming information. This allows for dimming that isn't subject to 120Hz flicker that can possibly be perceived by the human eye.

V_{BUCK} supplies the power which drives the LED string. Diode D3 allows V_{BUCK} to remain high while V+ cycles on and off. V_{BUCK} has a relatively small hold capacitor C10 which reduces the voltage ripple when the valley-fill capacitors are being charged. However, the network of diodes and capacitors shown between D3 and C10 make up a "valley-fill" circuit. The valley-fill circuit can be configured with two or three stages. The most common configuration is two stages which is illustrated in Figure 22.

When the “input line is high”, power is derived directly through D3. The term “input line is high” can be explained as follows. The valley-fill circuit charges capacitors C7 and C9 in series when the input line is high (see Figure 23).

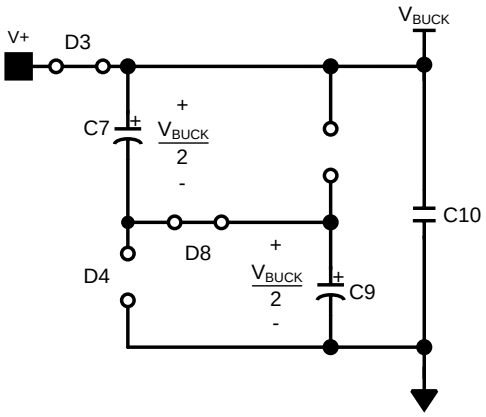


Figure 23. Two stage Valley-Fill Circuit when AC Line is High

The peak voltage of a two stage valley-fill capacitor is:

$$V_{VF\text{-}CAP} = \frac{V_{AC\text{-}RMS}\sqrt{2}}{2} \quad (1)$$

As the AC line decreases from its peak value every cycle, there will be a point where the voltage magnitude of the AC line is equal to the voltage that each capacitor is charged. At this point diode D3 becomes reversed biased, and the capacitors are placed in parallel to each other (see Figure 24) and V_{BUCK} equals the capacitor voltage.

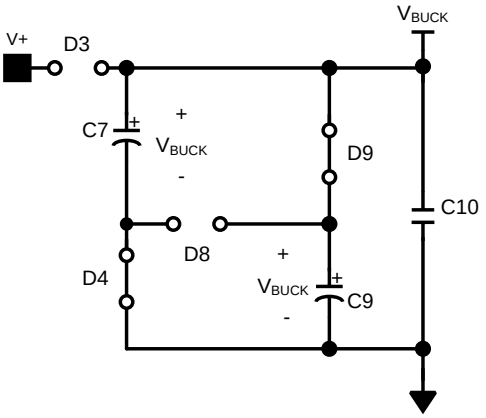


Figure 24. Two stage Valley-Fill Circuit when AC Line is Low

The valley-fill circuit can be optimized for power factor, voltage hold-up and overall application size and cost. The LM3448 will operate with a single stage or a three stage valley-fill circuit as well. Resistor R8 functions as a current limiting resistor during start-up and during the transition from series to parallel connection. Resistors R6 and R7 are 1MΩ bleeder resistors and may or may not be necessary for each application.

FLTR2 LINE-INJECTION

The technique of line-injection is another very effective means of improving power factor performance. When using this method, the valley-fill circuit can be eliminated which results in a much simpler driver design. The trade off will be an increase of 120Hz ripple on the LED current.

Different FLTR2 circuits are shown in Figure 25. Figure 25(a) shows how to set up FLTR2 when a passive PFC circuit (e.g. valley-fill) is already being used and no line-injection is utilized. If passive PFC is not being implemented, then the “direct line-injection” of Figure 25(b) or “AC line-injection” of Figure 25(c) can be used.

Direct line-injection involves injecting a small portion (750mV to 1.00V) of rectified AC line voltage (i.e. V+) into the FLTR2 pin. The result is that current shaping of the input current will yield power factor values greater than 0.94.

AC coupled line-injection goes one step further by adding a capacitor C14 between R15 and C11. This improves LED line regulation but does so by trading out a small portion of the power factor improvement from the direct-injection circuit. For example with AC coupled line-injection, LED current regulation of up to +/- 3% is possible for an input voltage range of 105VAC to 135VAC when operating at a nominal 120VAC.

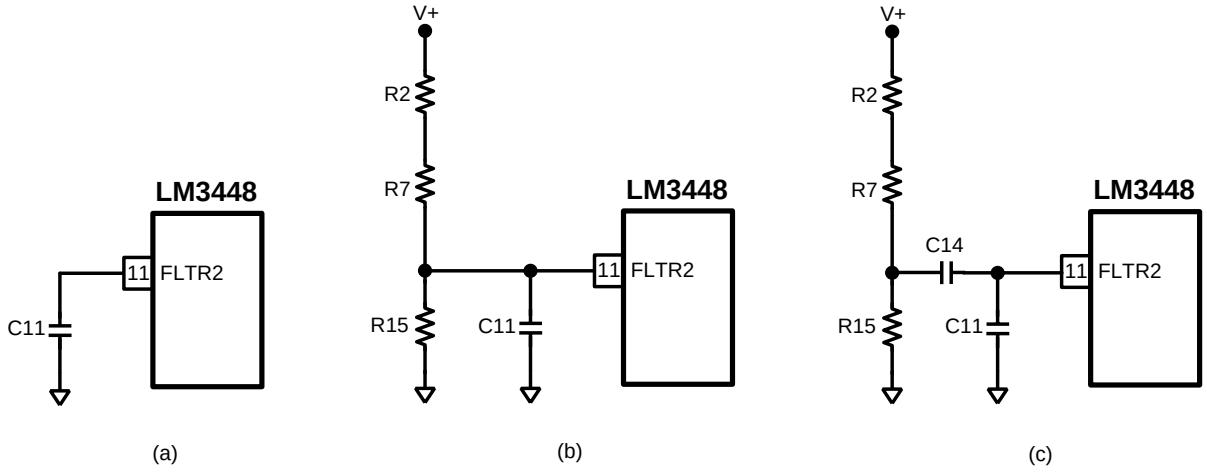


Figure 25. (a) No line-injection, (b) Direct line-injection, (c) AC-coupled line injection

DIRECT LINE-INJECTION FOR FLYBACK TOPOLOGY

For flyback converters using the LM3448, direct-line injection can result in power factors greater than 0.95. Using this technique, the LM3448 circuit is essentially turned into a constant power flyback converter operating in discontinuous conduction mode (DCM). The LM3448 normally works as a constant off-time regulator, but by injecting a $1.0V_{PK}$ rectified AC voltage into the FLTR2 pin, the on-time can be made to be constant. With a DCM flyback converter the primary side current, i, needs to increase as the rectified input voltage, V+, increases as shown in the following equations,

$$v = L\frac{di}{dt} \tag{2}$$

or,

$$\frac{L}{t_{ON}} = \frac{V+}{\Delta i} \tag{3}$$

Therefore a constant on-time (since inductor L is constant) can be obtained.

By using the line voltage injection technique, the FLTR2 pin has the voltage wave shape shown in Figure 26 on it with no TRIAC dimmer in-line. Peak voltage at the FLTR2 pin should be kept below 1.25V otherwise current limit will be tripped. Capacitor C11 is chosen small enough so as not to distort the AC signal but just add a little filtering.

Although the on-time is probably never truly constant, it can be observed in Figure 27 how (by injecting the rectified voltage) the on-time is adjusted.

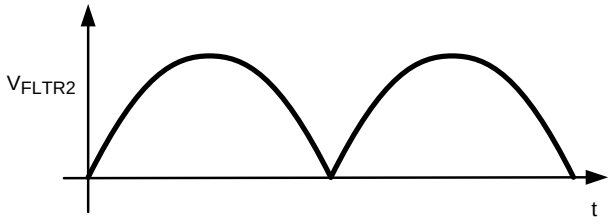


Figure 26. FLTR2 Waveform with No Dimmer

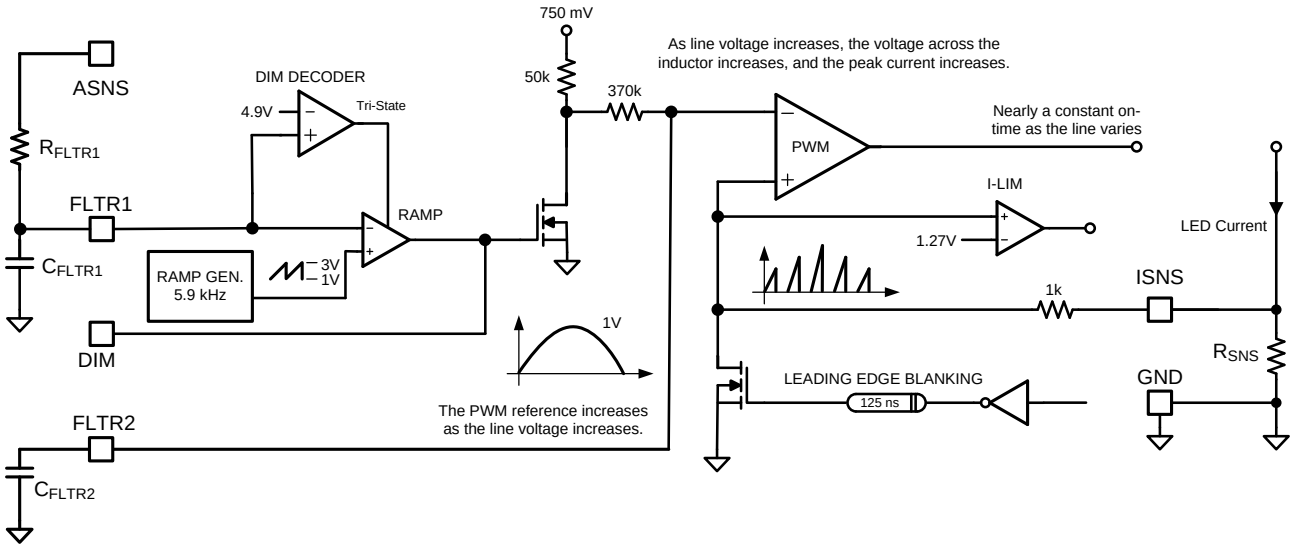


Figure 27. Typical Operation of Direct Line-Injection into FLTR2 Pin

TRIAC DIMMER HOLDING CURRENT

In order to emulate an incandescent light bulb (essentially a resistor) with any LED driver, the existing TRIAC will require a small amount of holding current throughout the AC line cycle. As shown in Figure 28, a simple circuit consisting of R3, D1, Q1 and R4 can accomplish this. With R4 placed on the source of Q1, additional holding current can be pulled from the TRIAC. Most TRIAC dimmers only require a few milliamps of current to hold them on. A few “less expensive” TRIACs sold on the market will require a bit more current. The value of resistor R4 will depend on the type of TRIAC being used and how many light fixtures are running off the TRIAC.

With a single LM3448 circuit on a common TRIAC dimmer, a holding current resistor between 3kΩ and 5kΩ will be required. As the number of LM3448 circuits added to a single dimmer increases, R4’s resistance can also be increased. A few TRIAC dimmers will require a resistor as low as 1kΩ or smaller for a single LM3448 circuit. Therefore the trade-off will be dimming performance versus efficiency. As the holding resistor R4 is increased, the overall system efficiency will also increase.

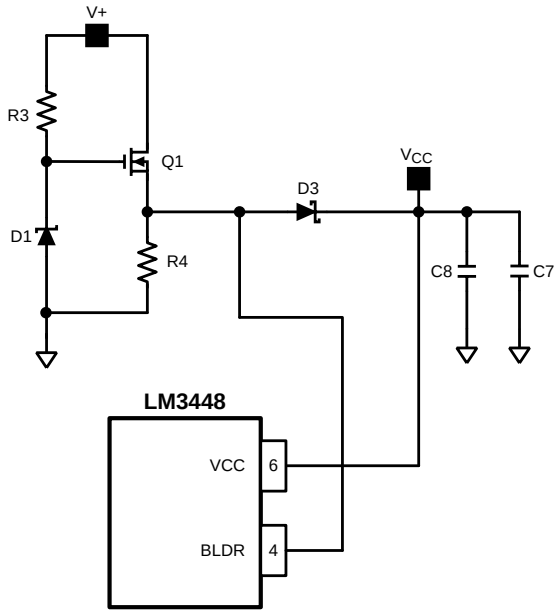


Figure 28. Basic holding current circuit

OPTIMIZING THE HOLDING CURRENT

For optimal system performance and efficiency, only enough holding current should be applied at the right time in the cycle to keep the TRIAC operating properly. This will ensure no variation or 'flicker' is seen in the LED light output while improving the circuit efficiency. Circuits that do this are outlined individually as blocks in Figure 15. These circuits are designed to identify the type of phase dimmer in-line with the LM3448, add holding current for different dimming conditions, or to discharge parasitic capacitances. The objective is to only add enough holding current as needed regardless if the dimmer is of a forward or reverse phase type. This allows the lighting manufacturer to optimize efficiency and gain Energy Star approval if desired.

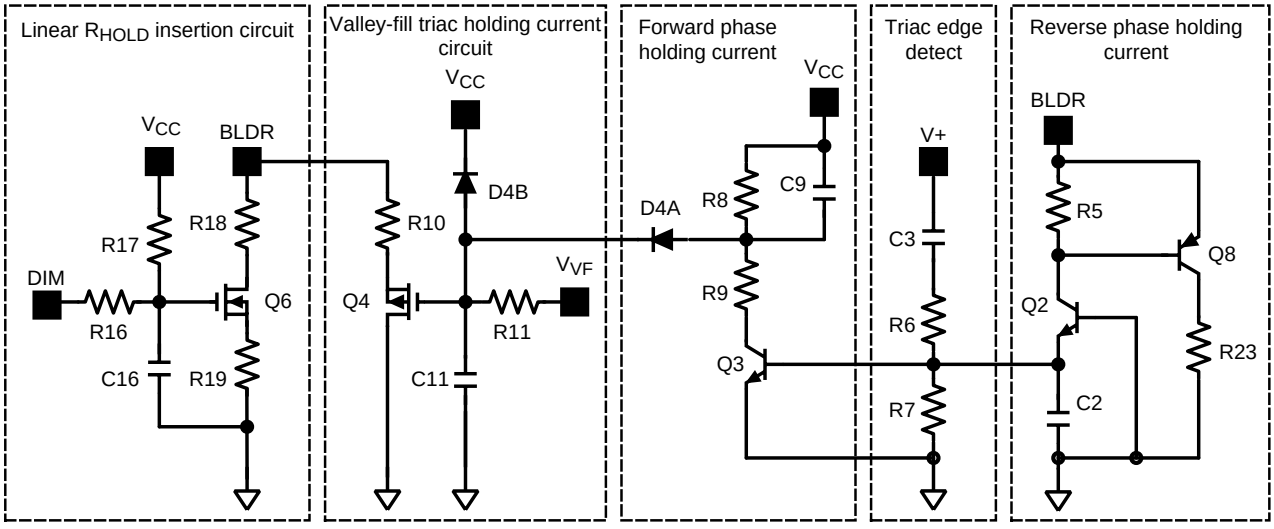


Figure 29. TRIAC Holding Current Circuits

Linear Hold Insertion Circuit

This circuit adds holding current during low TRIAC conduction angles. A variable voltage between 0 and 5 volts is generated at the Q6 gate by averaging the square wave output signal on the DIM pin. The duty cycle of this square wave varies with the TRIAC firing angle. As the LEDs are dimmed, the voltage at the Q6 gate will rise pulling a “holding current” equal to the Q6 source voltage divided by resistor R19.

Valley-Fill Holding Current Circuit

As described in the section on valley-fill PFC operation, when the valley-fill capacitors are in parallel there is a brief period of time where the output load is being supplied by these two capacitors. Therefore there is minimal or no line current being drawn from the AC line and the minimum holding current requirement is not met. The TRIAC may turn off at this time which causes phase dimming decode issues. A circuit can be added that detects when the valley-fill capacitors are in parallel. The result is that the gate of Q4 is pulled low, allowing additional hold current to be sourced through resistor R10.

TRIAC Edge Detect Circuit

During initial turn on (forward phase) or turn off (reverse phase) of a phase dimmer, a little extra holding current is sometimes required to latch the phase dimmer on or discharge any parasitic capacitances on the AC line. In order to determine which dimmer is being used, a TRIAC edge detect circuit is needed.

When the TRIAC fires, a sharp edge is created that can be captured by a properly sized R-C circuit. The combination of C3 and R6 creates a positive pulse on R7 for a forward phase dimmer or a negative pulse on R7 for a reverse phase dimmer. The pulse polarity determines whether the forward or reverse phase holding current circuit will be used. The value of R7 can be adjusted to vary the sensitivity of the edge detect circuit.

Forward Phase Holding Current Circuit

This circuit adds holding current when a forward phase TRIAC edge is detected. The TRIAC edge detect R-C circuit creates a positive pulse on the base of Q3 each cycle when a forward phase dimmer is present and dimming. The positive pulse turns on Q3 which results in additional holding current being pulled through R9.

Reverse Phase Holding Current Circuit

This circuit adds holding current when a reverse phase TRIAC edge is detected. The TRIAC edge detect R-C circuit creates a negative pulse on the emitter of Q2 each cycle when a reverse phase dimmer is present and dimming. This turns on Q8 and connects R23 to the Q1 pass MOSFET, adding holding current and sharpening the turn-off of the reverse phase dimmer.

START-UP AND BIAS SUPPLY

Figure 30 shows how to generate the necessary V_{CC} bias supply at start-up. Since the AC line peak voltage is always higher than the rating of the regulator, all designs require an N-channel MOSFET (passFET). The passFET (Q1) is connected with its drain attached to the rectified AC. The gate of Q1 is connected to a zener diode (D1) which is then biased from the rectified AC line through series resistance (R3). The source of Q1 is held at a V_{GS} below the zener voltage and current flows through Q1 to charge up whatever capacitance is present. If the capacitance is large enough, the source voltage will remain relatively constant over the line cycle and this becomes the input bias supply at VCC. This bias circuit also enables instant turn-on.

However once the circuit is operational, it can be desirable to bootstrap VCC to an auxiliary winding of the inductor or transformer as shown in Figure 31. The two bias paths are each connected to VCC through a diode to ensure the higher of the two is providing VCC current. This bootstrapping greatly improves efficiency while still maintaining quick start-up response.

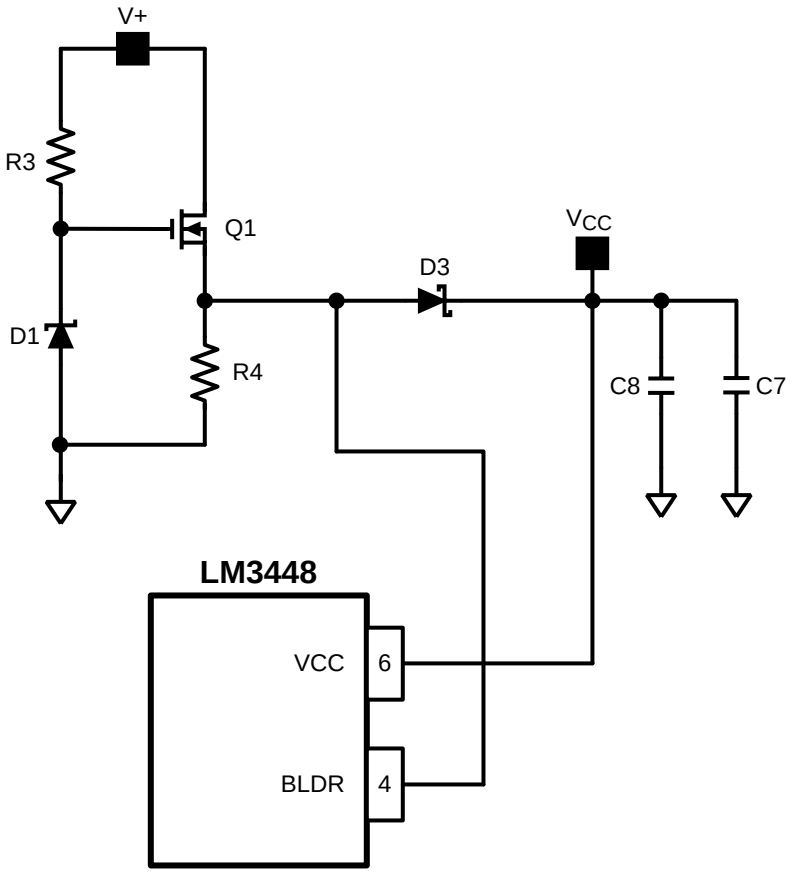


Figure 30. V_{CC} Start-up Circuit

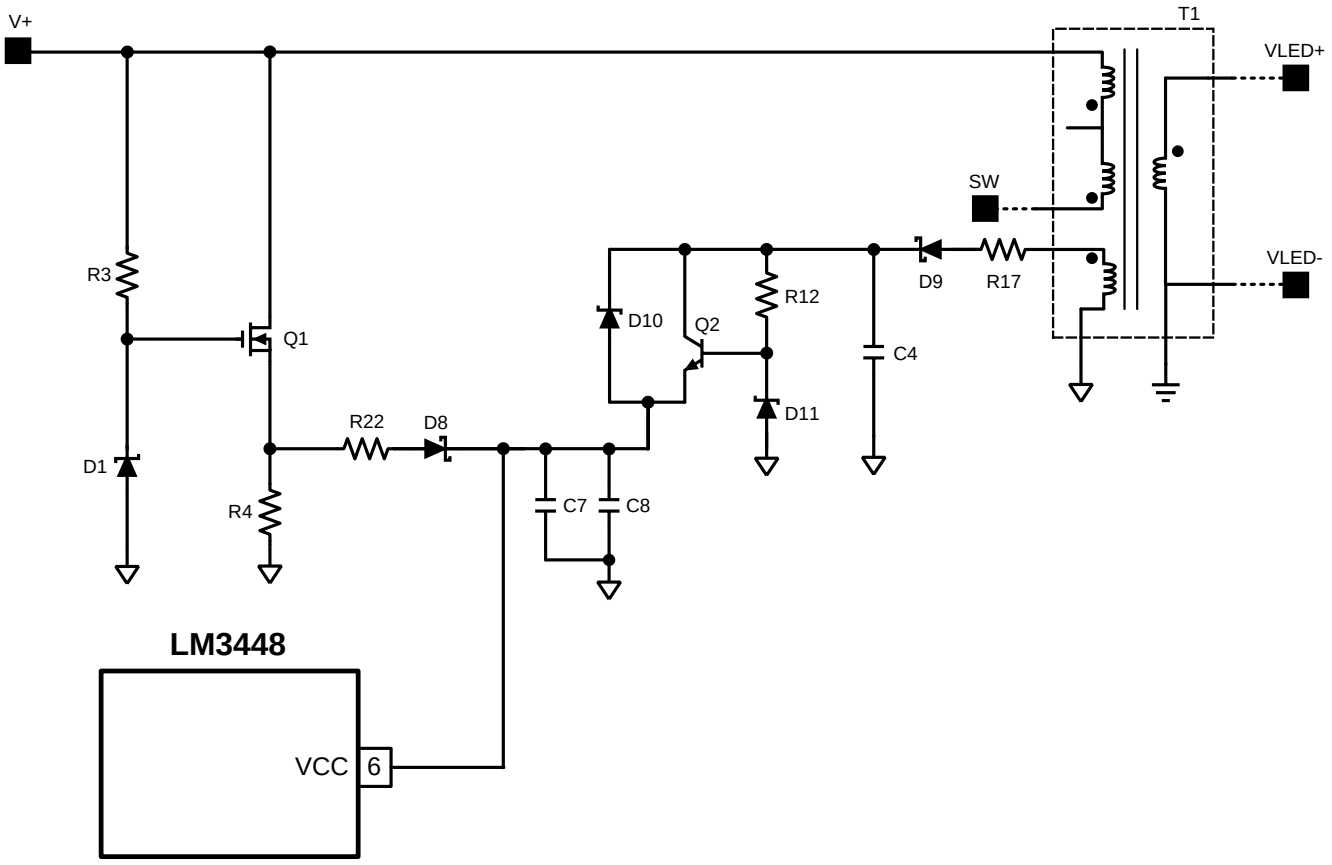


Figure 31. V_{CC} Auxiliary Winding Bias Circuit

COFF CURRENT SOURCE CIRCUITS

There are a few different current source circuits that can be used for establishing the LM3448 constant-off time control as shown in Figure 32.

Figure 32(a) shows the simplest current source circuit. Capacitor C_{OFF} will be charged with a constant current from V_{CC} through resistor R_{OFF}.

If there is large noise or ripple on the VCC pin, then the previously described circuit will fluctuate and the off-time will not be constant. The circuit of Figure 32(b) addresses this by using a zener diode D1 across R_{OFF} which establishes a stable voltage reference for the current source with inherent V_{CC} ripple rejection.

LED loads can exhibit voltage drift due to self-heating or external thermal conditions. A change in the LED stack voltage will result in the LED current to drift as well. Figure 32(c) addresses this issue by having the COFF current source referenced to the LED stack voltage using Q1 and R_{OFF} and thereby compensating for LED voltage drift. Another benefit is that the number of series LEDs in the LED string can be changed while still maintaining the same output drive current.

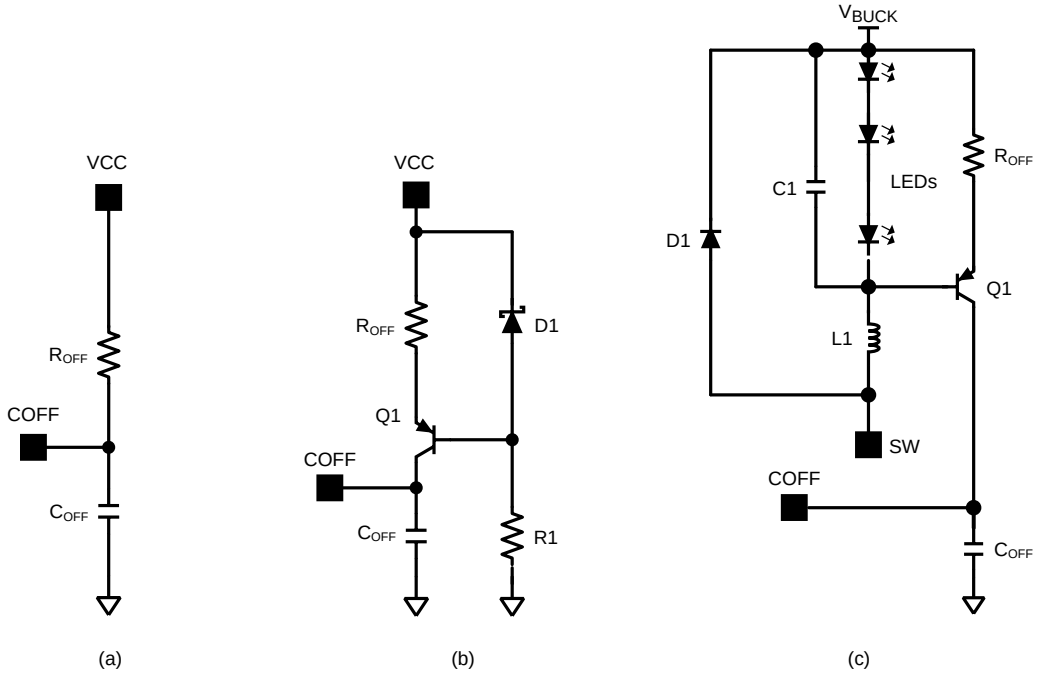


Figure 32. COFF Current Source Circuits

Design Guide

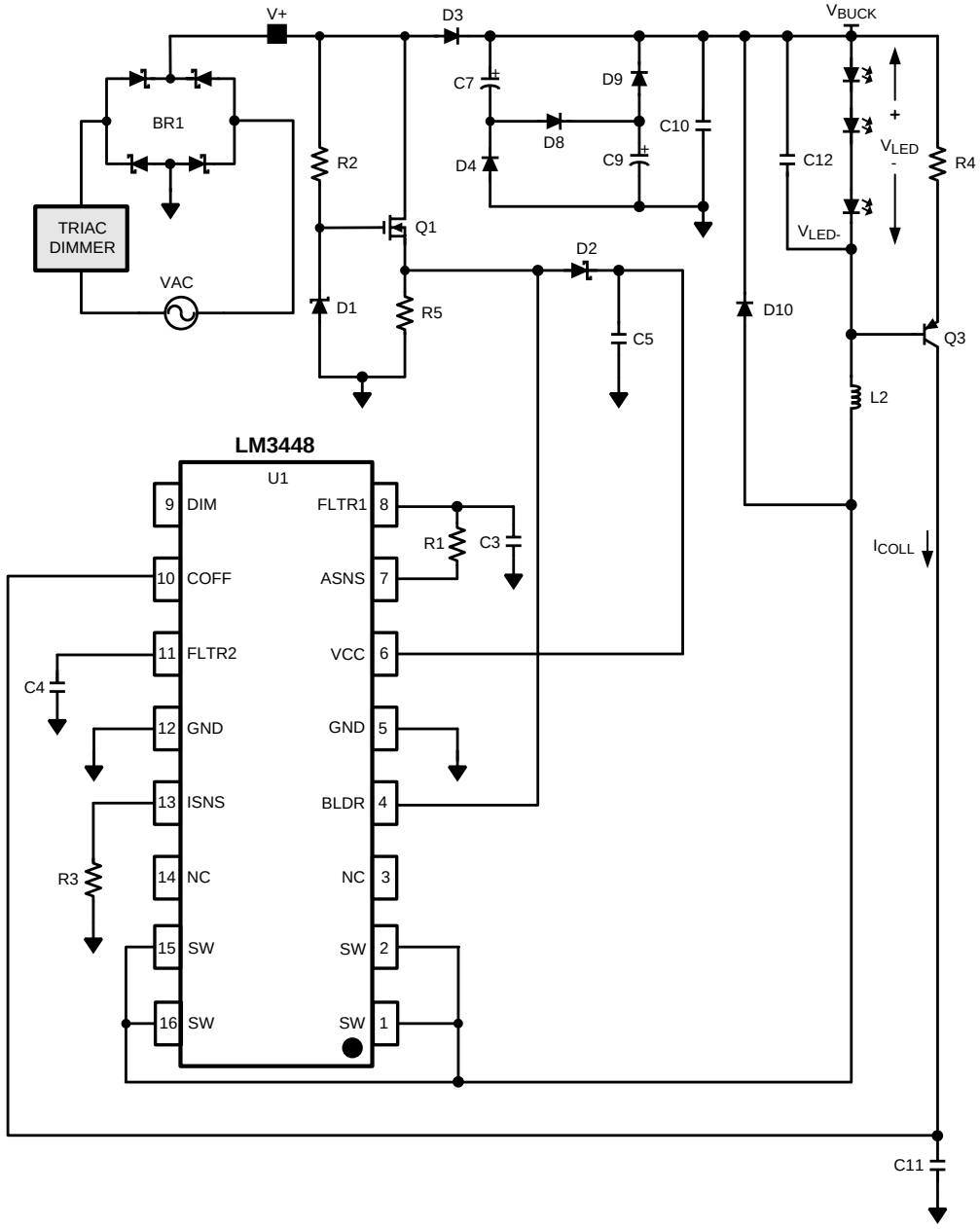


Figure 33. Typical Non-Isolated Buck Converter with Valley-Fill PFC

The following design guide is an example of how to design the LM3448 as a non-isolated buck converter with valley-fill PFC as shown in Figure 19.

DETERMINING DUTY-CYCLE (D)

Duty cycle (D) approximately equals:

$$\frac{V_{LED}}{V_{BUCK}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \quad (4)$$

With efficiency considered:

$$\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}} = D \tag{5}$$

For simplicity, choose efficiency between 75% and 85%.

CALCULATING OFF-TIME

The “Off-Time” of the LM3448 is set by the user and remains fairly constant as long as the voltage of the LED stack remains constant. Calculating the off-time is the first step in determining the switching frequency (f_{SW}) of the converter, which is integral in determining some external component values.

PNP transistor Q3, resistor R4, and the LED string voltage define a charging current into capacitor C11. A constant current into a capacitor creates a linear charging characteristic.

$$i = C\frac{dv}{dt} \tag{6}$$

Resistor R4, capacitor C11 and the current through resistor R4 (i_{COLL}), which is approximately equal to V_{LED}/R4, are all fixed. Therefore, dv is fixed and linear, and dt (i.e. t_{OFF}) can now be calculated.

$$t_{OFF} = C11 \times 1.276V \times \left(\frac{R4}{V_{LED}}\right) \tag{7}$$

Common equations for determining duty cycle and switching frequency in any buck converter:

$$f_{SW} = \left(\frac{1}{t_{ON} + t_{OFF}}\right) \tag{8}$$

$$D = \left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right) = \left(\frac{V_{LED}}{V_{BUCK}}\right) \tag{9}$$

$$D' = \left(\frac{t_{OFF}}{t_{ON} + t_{OFF}}\right) \tag{10}$$

Therefore:

$$f_{SW} = \left(\frac{D}{t_{ON}}\right), \text{and } f_{SW} = \left(\frac{1-D}{t_{OFF}}\right) \tag{11}$$

With efficiency of the buck converter in mind:

$$\frac{V_{LED}}{V_{BUCK}} = \eta \times D \tag{12}$$

Substitute equations and rearrange:

$$f_{SW} = \frac{\left(1 - \left(\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)\right)}{t_{OFF}} \tag{13}$$

Off-time and switching frequency can now be calculated using the equations above.

SETTING THE SWITCHING FREQUENCY

Selecting the switching frequency for nominal operating conditions is based on tradeoffs between efficiency (better at low frequency) and solution size/cost (smaller at high frequency). The input voltage to the buck converter (V_{BUCK}) changes with both line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string will, however, remain constant and therefore the off-time remains constant.

The on-time (t_{ON}) and therefore the switching frequency, will vary as the V_{BUCK} voltage changes with line voltage. A good design practice is to choose a desired nominal switching frequency knowing that the switching frequency will decrease as the line voltage drops and increase as the line voltage increases.

The off-time of the LM3448 can be programmed for switching frequencies ranging from 30 kHz to over 1MHz. A trade-off between efficiency and solution size must be considered when designing the LM3448 application.

The maximum switching frequency attainable is limited only by the minimum on-time requirement (200 ns).

Worst case scenario for minimum on time is when V_{BUCK} is at its maximum voltage (AC high line) and the LED string voltage (V_{LED}) is at its minimum value.

$$t_{ON(MIN)} = \left(\frac{1}{\eta} \times \frac{V_{LED(MIN)}}{V_{LED(MAX)}} \right) \frac{1}{f_{SW}} \tag{14}$$

The maximum voltage seen by the Buck Converter is:

$$V_{BUCK(MAX)} = V_{AC-RMS(MAX)} \times \sqrt{2} \tag{15}$$

INDUCTOR SELECTION

The controlled off-time architecture of the LM3448 regulates the average current through the inductor (L2), and therefore the LED string current (see Figure 34). The input voltage to the buck converter (V_{BUCK}) changes with line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string is relatively constant, and therefore the current through R4 is constant. This current sets the off-time of the converter and therefore the output volt-second product (V_{LED} x off-time) remains constant. A constant volt-second product makes it possible to keep the ripple through the inductor constant as the voltage at V_{BUCK} varies.

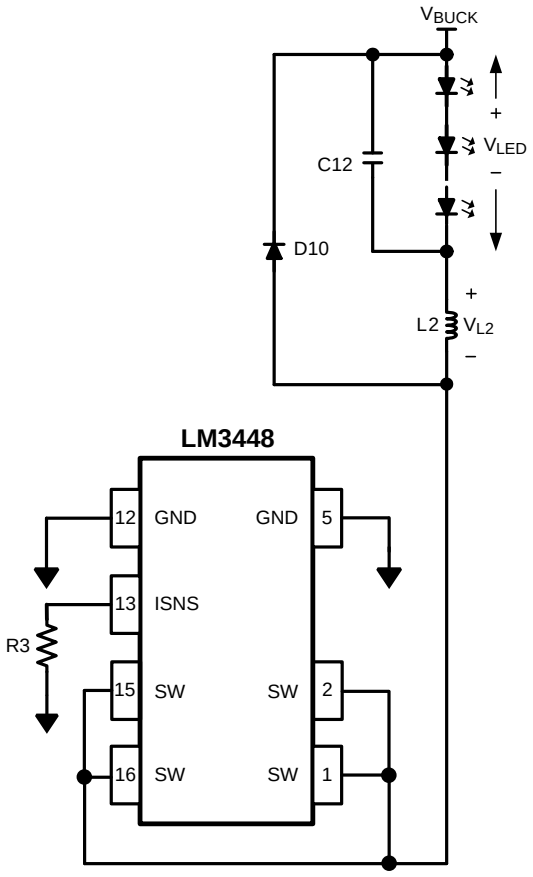


Figure 34. Simplified LM3448 Buck Converter

The equation for an ideal inductor is:

$$v = L\frac{di}{dt} \tag{16}$$

Given a fixed inductor value, L, this equation states that the change in the inductor current over time is proportional to the voltage applied across the inductor.

During the on-time, the voltage applied across the inductor is,

$$V_{L(ON-TIME)} = V_{BUCK} - (V_{LED} + V_{DS} + I_{L2} \times R3) \tag{17}$$

Since the voltage across the SW FET (V_{DS}) is relatively small as is the voltage across sense resistor R3, we can simplify this as approximately,

$$V_{L(ON-TIME)} = V_{BUCK} - V_{LED} \tag{18}$$

During the off-time, the voltage seen by the inductor is approximately,

$$V_{L(OFF-TIME)} = V_{LED} \tag{19}$$

The value of $V_{L(OFF-TIME)}$ will be relatively constant, because the LED stack voltage will remain constant. If we rewrite the equation for an inductor inserting what we know about the circuit during the off-time, we get,

$$V_{L(OFF-TIME)} = V_{LED} = L \times \left(\frac{\Delta i}{\Delta t}\right) \tag{20}$$

$$V_{L(OFF-TIME)} = V_{LED} = L \times \left(\frac{I_{MAX} - I_{MIN}}{\Delta t}\right) \tag{21}$$

Re-arranging this gives,

$$\Delta i \cong t_{OFF} \times \frac{V_{LED}}{L2} \tag{22}$$

From this we can see that the ripple current (Δi) is proportional to off-time (t_{OFF}) multiplied by a voltage which is dominated by V_{LED} divided by a constant inductance (L2).

These equations can be rearranged to calculate the desired value for inductor L2.

$$L2 \cong t_{OFF} \times \frac{V_{LED}}{\Delta i} \tag{23}$$

where,

$$t_{OFF} = \frac{1 - \left(\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{f_{SW}} \tag{24}$$

and finally,

$$L_2 = \frac{V_{LED}\left(1 - \left(\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)\right)}{f_{SW} \times \Delta i} \tag{25}$$

Refer to “Design Example” section of the datasheet to better understand the design process.

SETTING THE LED CURRENT

Figure 35 shows the inductor current waveform (I_{L2}) when operating in continuous conduction mode (CCM). The LM3448 constant off-time control loop regulates the peak inductor current (I_{L2-PK}). Since the average inductor current equals the average LED current (I_{AVE}), LED current is controlled by regulating the peak inductor current.

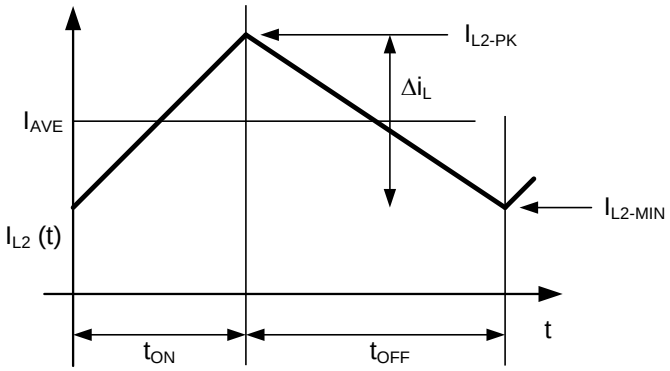


Figure 35. Inductor Current Waveform in CCM

Knowing the desired average LED current (I_{AVE}) and the nominal inductor current ripple (Δi_L), the peak current for an application running in CCM is defined as follows:

$$i_{L2\text{-}PK} = I_{AVE} + \frac{\Delta i_L}{2} \tag{26}$$

Or, the maximum (i.e. un-dimmed) LED current would then be,

$$I_{AVE(UNDIM)} = I_{L2\text{-}PK(UNDIM)} - \frac{\Delta i_L}{2} \tag{27}$$

This is important to calculate because this peak current multiplied by the sense resistor R3 will determine when the internal comparator is tripped. The internal comparator turns the SW FET off once the peak sensed voltage reaches 750 mV.

$$I_{L\text{-}PK(UNDIM)} = \frac{750mV}{R3} \tag{28}$$

CURRENT LIMIT

Under normal circumstances, the trip voltage on the PWM comparator would be less than or equal to 750 mV depending on the amount of dimming. However if there is a short circuit or an excessive load on the output, higher than normal switch currents will cause a voltage above 1.27V on the ISNS pin which will trip the I-LIM comparator. The I-LIM comparator will reset the RS latch, turning off the internal SW FET. It will also inhibit the Start Pulse Generator and the COFF comparator by holding the COFF pin low. A delay circuit will prevent the start of another cycle for 180µs.

VALLEY FILL CAPACITORS

The maximum voltage seen by the valley-fill capacitors is,

$$V_{BUCK(MIN)} = \frac{V_{AC\text{-}RMS(MIN)}\sqrt{2} \times \sin(\theta)}{\#\,stages} \tag{29}$$

This assumes that the capacitors chosen have identical capacitance values and split the line voltage equally. Often a 20% difference in capacitance could be observed between like capacitors. Therefore a voltage rating margin of 25% to 50% should be considered.

The valley-fill capacitors should be sized to supply energy to the buck converter (V_{BUCK}) when the input line is less than its peak divided by the number of stages used in the valley-fill. The capacitance value should be calculated when the TRIAC is not firing (i.e. when full LED current is being drawn by the LED string). The maximum power is delivered to the LED string at this time and therefore the most capacitance will be needed.

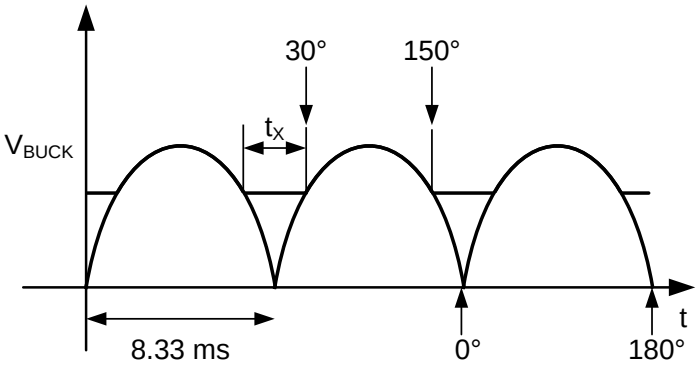


Figure 36. Two Stage Valley-Fill V_{BUCK} Voltage with no TRIAC Dimming

From Figure 36 and the equation for current in a capacitor,

$$i = C\frac{dv}{dt} \tag{30}$$

the amount of capacitance needed at V_{BUCK} can be calculated using the following method.

At 60Hz and a valley-fill circuit of two stages, the hold-up time (t_X) required at V_{BUCK} is calculated as follows. The total angle of an AC half cycle is 180° and the total time of a half AC line cycle is 8.33ms. When the angle of the AC waveform is at 30° and 150°, the voltage of the AC line is exactly ½ of its peak. With a two stage valley-fill circuit, this is the point where the LED string switches from power being derived from AC line to power being derived from the hold-up capacitors (C7 and C9). At 60° out of 180° of the cycle or 1/3 of the cycle, the power is derived from the hold-up capacitors (1/3 x 8.33 ms = 2.78 ms). This is equal to the hold-up time (dt) from the above equation, and dv is the amount of voltage the circuit is allowed to droop. From the next section ("Determining Maximum Number of Series Connected LEDs Allowed") we know the minimum V_{BUCK} voltage will be about 45V for a 90VAC to 135VAC line. At a 90VAC low line operating condition input, ½ of the peak voltage is 64V. Therefore with some margin the voltage at V_{BUCK} cannot droop more than about 15V (dv). (i) is equal to (P_{OUT}/ V_{BUCK}), where P_{OUT} is equal to (V_{LED} x I_{LED}). Total capacitance (C7 in parallel with C9) can now be calculated. See " Design Example" section for further calculations of the valley-fill capacitors.

MAXIMUM NUMBER OF SERIES CONNECTED LEDS

A buck converter topology requires that the input voltage (V_{BUCK}) of the output circuit must be greater than the voltage of the LED stack (V_{LED}) for proper regulation. One must determine what the minimum voltage observed by the buck converter will be before the maximum number of series LEDs allowed can be determined. Two variables will have to be determined in order to accomplish this.

1. AC line operating voltage. This is usually 90VAC to 135VAC for North America. Although the LM3448 can operate at much lower and higher input voltages a range is needed to illustrate the design process.
2. Number of stages being implemented in the valley-fill circuit.

In this example a two-stage valley-fill circuit will be used.

Figure 37 shows three TRIAC dimmed waveforms. One can easily see that the peak voltage (V_{PEAK}) from 0° to 90° will always be,

$$V_{AC\text{-}RMS\text{-}PK}\sqrt{2} \tag{31}$$

Once the TRIAC is firing at an angle greater than 90° the peak voltage will lower and be equal to,

$$V_{AC\text{-}RMS\text{-}PK}\sqrt{2} \times \sin(\theta) \tag{32}$$

The voltage at V_{BUCK} with a valley-fill stage of two will look similar to the waveforms of Figure 38. The purpose of the valley-fill circuit is to allow the buck converter to pull power directly off of the AC line when the line voltage is greater than its peak voltage divided by two (for a two stage valley-fill circuit). During this time, the capacitors within the valley-fill circuit (C7 and C9) are charged up to the peak of the AC line voltage. Once the line drops below its peak divided by two, the two capacitors are placed in parallel and deliver power to the buck converter. One can now see that if the peak of the AC line voltage is lowered due to variations in the line voltage, or if the TRIAC is firing at an angle above 90°, the DC offset (V_{DC}) will lower. V_{DC} is the lowest value that voltage V_{BUCK} will encounter.

$$V_{BUCK(MIN)} = \frac{V_{AC\text{-}RMS(MIN)}\sqrt{2} \times \sin(\theta)}{\#\,stages} \quad (33)$$

Example:

Line voltage = 90VAC to 135VAC

Valley-fill stages = 2

$$V_{BUCK(MIN)} = \frac{90\sqrt{2} \times \sin(135°)}{2} = 45V \quad (34)$$

Depending on what type and value of capacitors are used, some derating should be used for voltage droop when the capacitors are delivering power to the buck converter. When the TRIAC is firing at 135° the current through the LED string will be small. Therefore the droop should be small at this point and a 5% voltage droop should be a sufficient derating. With this derating, the lowest voltage the buck converter will see is about 42.5V in this example.

To determine how many LEDs can be driven, take the minimum voltage the buck converter will see (42.5V) and divide it by the worst case forward voltage drop of a single LED.

Example:

42.5V/3.7V = 11.5 LEDs (11 LEDs with margin)

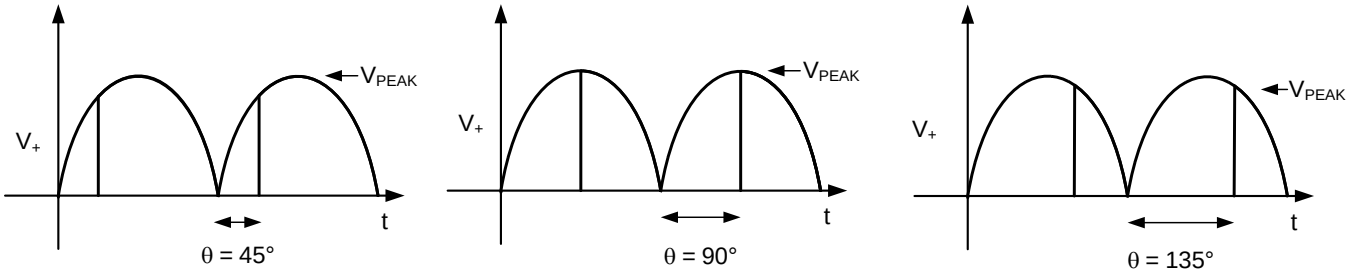


Figure 37. V_{BUCK} Waveforms with Various TRIAC Firing Angles

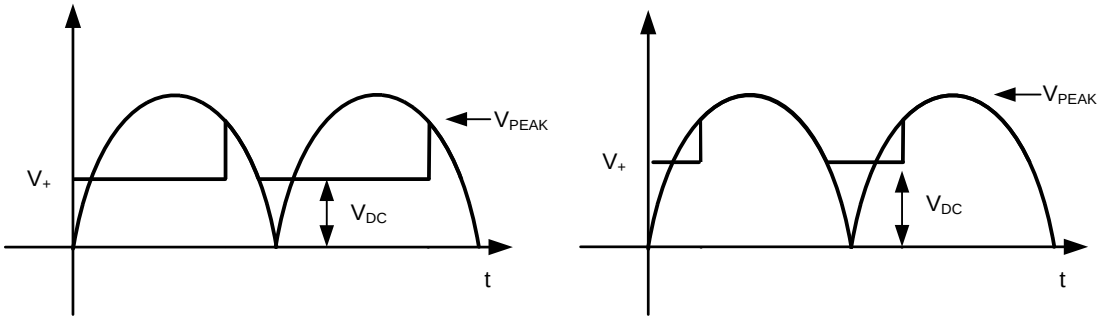


Figure 38. Two Stage Valley-Fill V_{BUCK} Waveforms with Various TRIAC Firing Angles

OUTPUT CAPACITOR

A capacitor placed in parallel with the LED or array of LEDs can be used to reduce the LED current ripple while keeping the same average current through both the inductor and the LED array. With a buck topology the output inductance (L2) can now be lowered, making the magnetics smaller and less expensive. With a well designed converter, you can assume that all of the ripple will be seen by the capacitor and not the LEDs. One must ensure that the capacitor you choose can handle the RMS current of the inductor. Refer to manufacture's datasheets to ensure compliance. Usually an X5R or X7R capacitor between 1µF and 10µF of the proper voltage rating will be sufficient.

RE-CIRCULATING DIODE

The LM3448 Buck converter requires a re-circulating diode D10 to carry the inductor current during the off-time of the internal SW FET. The most efficient choice for D10 is a diode with a low forward drop and near-zero reverse recovery time that can withstand a reverse voltage of the maximum voltage seen at V_{BUCK}. For a common 110VAC ± 20% line, the reverse voltage could be as high as 190V.

$$V_D \geq V_{AC\text{-}RMS(MAX)}\sqrt{2} \tag{35}$$

The current rating must be at least,

$$I_D = \left(1 - D_{MIN}\right) \times I_{LED(AVE)} \tag{36}$$

or,

$$I_D = \left(1 - \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}}\right) \times I_{LED(AVE)} \tag{37}$$

Another consideration when choosing a diode is to make sure that the diode's reverse recovery time is much greater than the leading edge blanking time for proper operation.

Design Calculation Example

The following design example illustrates the process of actually calculating external component values for a LM3448 non-isolated buck converter with valley-fill PFC according to the following specifications.

SPECIFICATIONS:

1. Input voltage range (90VAC – 135VAC)
2. Nominal input voltage = 115VAC
3. Number of LEDs in series = 7
4. Forward voltage drop of a single LED = 3.6V
5. LED stack voltage = (7 x 3.6V) = 25.2V

CHOSEN VALUES:

1. Target nominal switching frequency, f_{SW} = 250kHz
2. $I_{LED(AVE)}$ = 400mA
3. P_{OUT} = (25.2V) x (400mA) = 10.1W
4. Ripple current Δi (usually 15% - 30% of $I_{LED(AVE)}$) = (0.30 x 400mA) = 120mA
5. Valley fill stages = 2
6. Assumed minimum efficiency = 80%

CALCULATIONS:

1. Calculate minimum voltage V_{BUCK} equals:

$$V_{BUCK(MIN)} = \frac{90\sqrt{2} \times \sin\left(135°\right)}{2} = 45V \tag{38}$$

2. Calculate maximum voltage V_{BUCK} voltage,

$$V_{BUCK(MAX)} = 135\sqrt{2} = 190V \quad (39)$$

3. Calculate t_{OFF} at V_{BUCK} nominal line voltage,

$$t_{OFF} = \frac{\left(1-\left(\frac{1}{0.8}\times\frac{25.2V}{115\sqrt{2}V}\right)\right)}{250kHz} = 3.23\mu s \quad (40)$$

4. Calculate $t_{ON(MIN)}$ at high line to ensure that
   – $t_{ON(MIN)}$ > 200ns,

$$t_{ON(MIN)} = \frac{\left(\frac{1}{0.8}\times\frac{25.2V}{135\sqrt{2}V}\right)}{\left(1-\left(\frac{1}{0.8}\times\frac{25.2V}{135\sqrt{2}V}\right)\right)}\times 3.23\mu s = 638ns \quad (41)$$

5. Calculate C11 and R4:
6. Choose current through R4 (between 50µA and 100µA): 70µA
   – Calculate R4,

$$R4 = \frac{V_{LED}}{I_{COLL}} = 360k\Omega \quad (42)$$

7. Choose a standard value of 365kΩ
8. Calculate C11,

$$C11 = \left(\frac{V_{LED}}{R4}\right)\left(\frac{t_{OFF}}{1.276V}\right) = 175pF \quad (43)$$

9. Choose standard value of 120pF.
10. Calculate inductor value at t_{OFF} = 3µs,

$$L2 = \frac{2.52V\left(1-\left(\frac{1}{0.8}\times\frac{25.2V}{115\sqrt{2}V}\right)\right)}{(250kHz\times 0.12A)} = 677\mu H \quad (44)$$

11. Choose C10 = 1.0µF, 200V.
12. Calculate valley-fill capacitor values,
   – VAC low line = 90VAC, V_{BUCK} minimum equals 45V (no TRIAC dimming at maximum LED current). Set droop for 20V maximum at full load and low line.

$$i = C\frac{dv}{dt} \quad (45)$$

   – Since "i" equals P_{OUT}/V_{BUCK} = 224mA, "dV" equals 20V, "dt" equals 2.78ms, and then C_{TOTAL} equals 31µF.
   – Therefore choose C7 = C9 = 15µF.

APPLICATIONS INFORMATION

DESIGN #1: 7W, 120VAC Non-isolated Buck LED Driver with Valley-Fill PFC

SPECIFICATIONS:

- AC Input Voltage: 120VAC nominal (85VAC – 135VAC)
- Output Voltage: 21.1V_{DC}
- LED Output Current: 342mA

This TRIAC dimmer compatible design incorporates the following features:

- Passive valley-fill PFC for improved power factor performance,
- Comprehensive TRIAC holding current coverage,
- Standard V_{CC} start-up and bias circuit,
- Constant-off time control with LED voltage drift compensation.

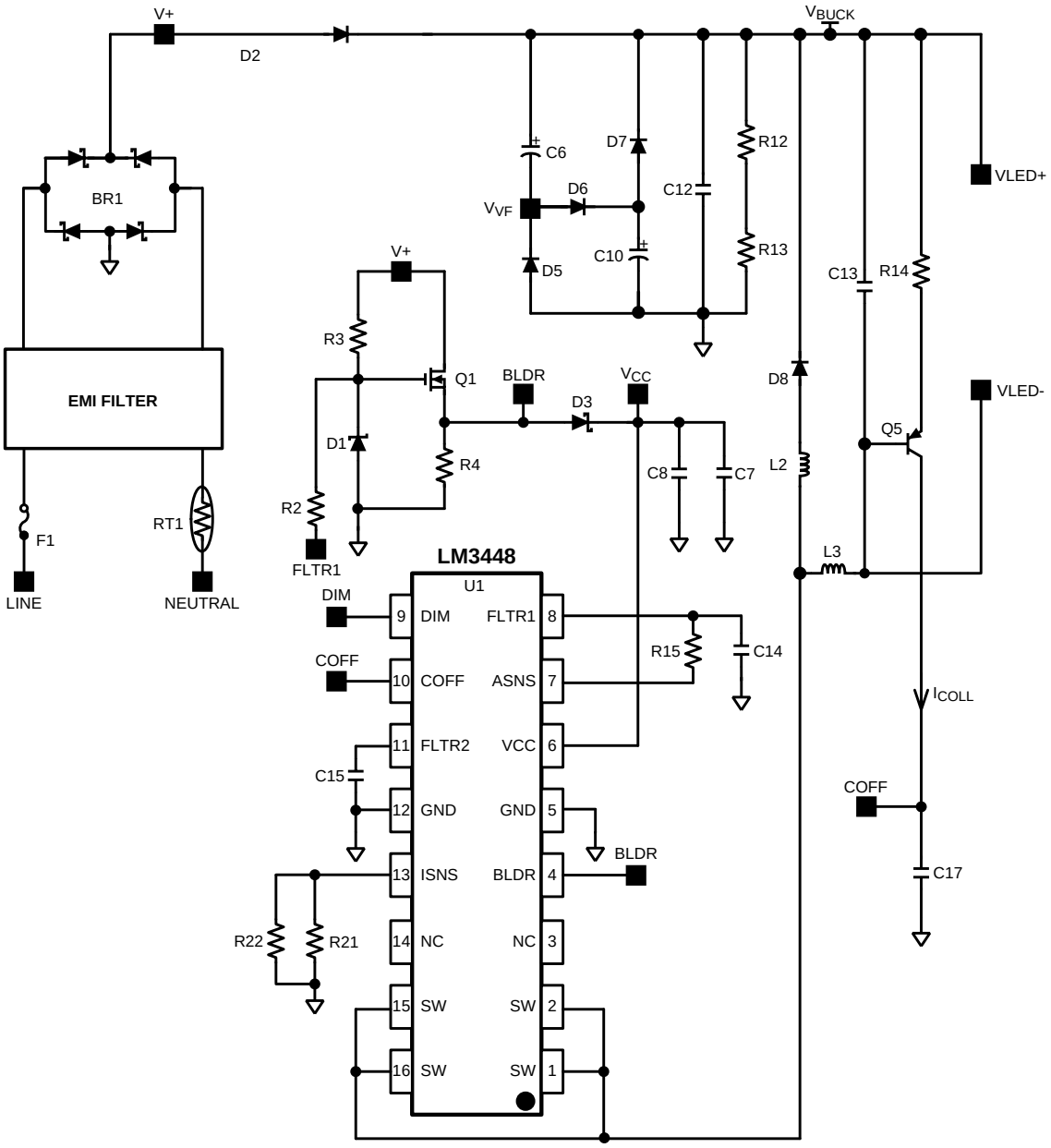


Figure 39. DESIGN #1 Circuit

Table 1. DESIGN #1 BILL OF MATERIALS

Part ID	Description	Manufacturer	Part Number
U1	IC LED Driver	Texas Instruments	LM3448MA
BR1	Bridge Rectifier Vr = 400V, Io = 0.8A, Vf = 1V	Diodes Inc.	HD04-T
C2	Ceramic, 0.01uF, X7R, 25V, 10%	Murata	GRM188R71E103KA01D
C3	Ceramic, 1000pF 500V X7R 1206	Kemet	C1206C102KCRACTU
C12	.01uF	KEMIT	C1808C103KDRACTU
C6, C10	CAP 33uF 100V ELECT NHG RADIAL	Panasonic-ECG	ECA-2AHG330
C7	22uF, Ceramic, X5R, 25V, 10%	Murata	GRM32ER61E226KE15L
C8	DNP	-	-
C9	4.7uF		C3216X7R1E475K
C11	DNP	-	-
C13	Ceramic, 1.0uF 100V X7R 1206	Murata	GRM31CR72A105KA01
C14	Ceramic, X7R, 16V, 10%	Murata	GRM188R71C474KA88D
C15	Ceramic, 0.1uF, X7R, 16V, 10%	Murata	GRM188R71C104KA01D
C16	Ceramic, 0.22uF, X7R, 16V, 10%	Murata	GRM188R71E224KA88D
C17	Ceramic, 330pF 100V C0G 0603	Murata	GCM1885C2A331JA16D
D1	DIODE ZENER 225MW 15V SOT23	ON Semiconductor	BZX84C15LT1G
D2, D3, D5, D6, D7	DIODE FAST REC 200V 1A	Rohm Semiconductor	RF071M2STR
D4	DIODE SWITCH SS DUAL 70V SOT323	Fairchild	BAV99WT1G
D8	DIODE SUPER FAST 200V 1A SMB	Diodes Inc	MURS120-13-F
F1	FUSE 1A 125V FAST	Cooper/Bussman	6125FA1A
L2	10mH, FERRITE CHIP POWER 160 OHM	Steward	HI1206T161R-10
L3	1mH, Shielded Drum Core,	Coilcraft Inc.	MSS1260-105
Q1	MOSFET N-CHAN 250V 4.4A DPAK	Fairchild	FDD6N25
Q2, Q3	TRANS NPN 350MW 40V SMD SOT23	Diodes Inc	MMBT4401-7-F
Q4	MOSFET P-CH 50V 130MA SOT-323	Diodes Inc	BSS84W-7-F
Q5	TRANS HIVOLT PNP AMP SOT-23	Fairchild	MMBTA92
Q6	MOSFET N-CHANNEL 100V SOT323	Diodes Inc	BSS123W-7-F
Q8	TRANS PNP LP 100MA 30V SOT23	ON Semiconductor	BC858CLT1G
R2	4.75M, 0805, 1%, 0.125W	Vishay-Dale	CRCW08054M75FKEA
R3	1%, 0.25W	Vishay-Dale	CRCW1206332kFKEA
R4	DNP	-	-
R5, R16	RES 49.9K OHM, 0.1W, 1% 0603	Vishay-Dale	CRCW060349k9FKEA
R6	RES 100K OHM, 0.25W1%, 1206	Vishay-Dale	CRCW1206100kFKEA
R7	RES 7.50K OHM, 0.1W, 1% 0603	Vishay-Dale	CRCW06037k50FKEA
R8	RES 10.0K OHM, 0.1W, 1% 0603	Vishay-Dale	CRCW060310k0FKEA
R9	RES 100 OHM, 0.25W1%, 1206	Vishay-Dale	CRCW1206100RFKEA
R10	RES 124 OHM, 0.25W1%, 1206	Vishay-Dale	CRCW1206124RFKEA
R11	RES 200K OHM, 0.125W, 1%, 0805	Vishay-Dale	CRCW0805200kFKEA
R12, R13	RES 1.0M OHM, 0.125W, 1%, 0805	Vishay-Dale	CRCW08051M00FKEA
R14	RES 576K OHM, 1/10W 1% 0603	Vishay-Dale	CRCW0603576kFKEA
R15	RES 280K OHM, 1/10W 1% 0603	Vishay-Dale	CRCW0603280kFKEA
R17	DNP	-	-
R18	RES 301 OHM, 0.25W1%, 1206	Vishay-Dale	CRCW1206301RFKEA
R19	RES 49.9 OHM, 0.125W, 1%, 0805	Vishay-Dale	CRCW080549R9FKEA
R21	RES 12.1 OHM, 0.25W1%, 1206	Vishay-Dale	CRCW120612R1FKEA
R22	RES 1.8 OHM 1/3W 5% 1210	Vishay-Dale	CRCW12101R80JNEA
R23	RES 499 OHM, 0.25W1%, 1206	Vishay-Dale	CRCW1206499RFKEA
RT1	CURRENT LIM INRUSH 60OHM 20%	Canterm	MF72-060D5

DESIGN #2: 6.5W, 120VAC Non-isolated "A19 Edison" Retrofit with AC-Coupled Line Injection

SPECIFICATIONS:

- AC Input Voltage: 120VAC nominal (85VAC – 135VAC)
- Output Voltage: 35.7V_{DC}
- LED Output Current: 181mA

This TRIAC dimmer compatible design incorporates the following features:

- AC coupled line-injection for improved power factor performance and LED current regulation,
- Standard V_{CC} start-up and bias circuit,
- V_{CC} derived COFF current source.

NOTE: Refer to LM3448 Application Note, AN-2127 (TI Lit Number SNOA559), for additional information and BOM regarding this design.

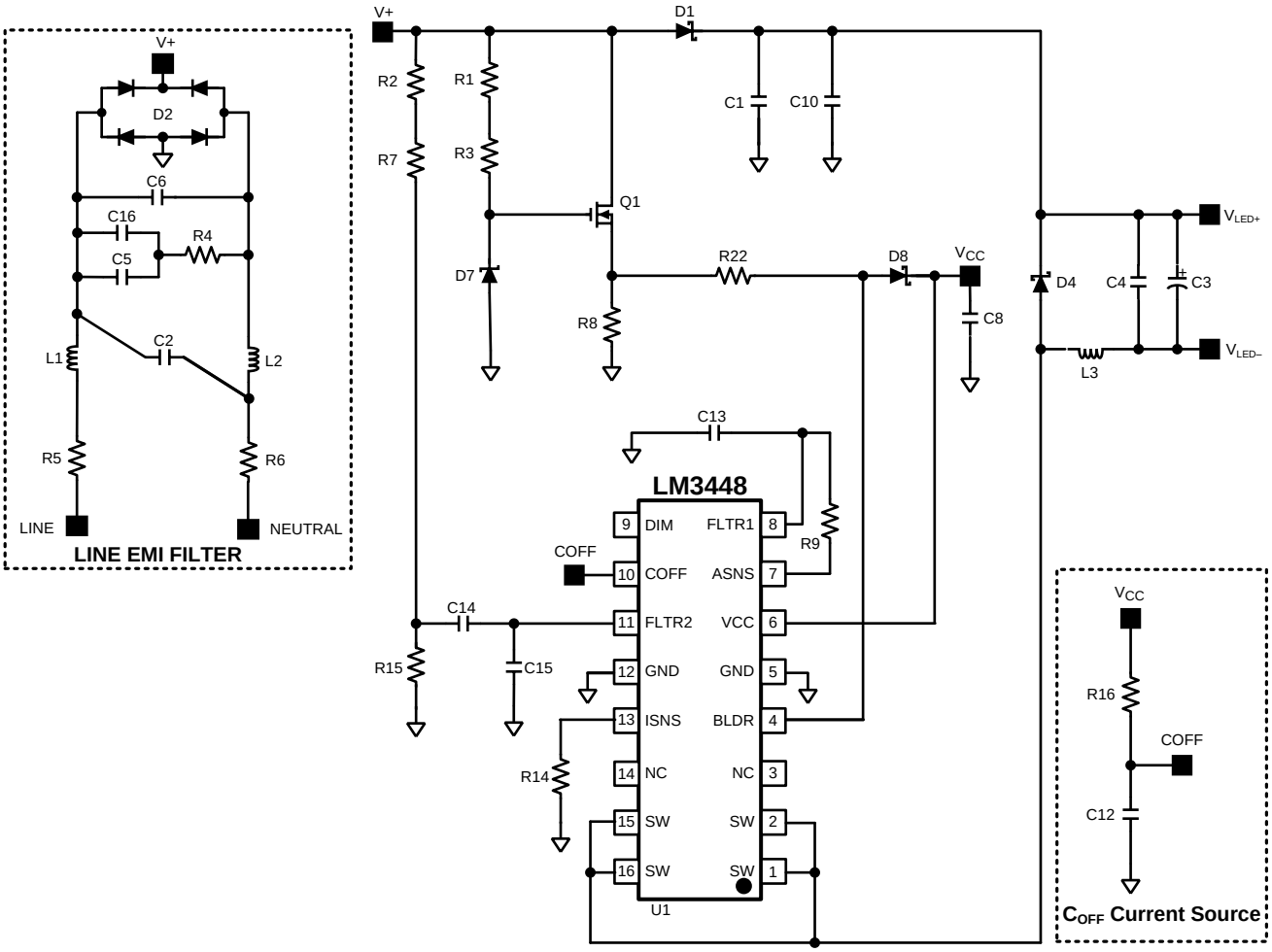


Figure 40. DESIGN #2 Circuit

DESIGN #3: 6W, 120VAC Isolated Flyback LED Driver with Direct Line Injection

SPECIFICATIONS:

- AC Input Voltage: 120VAC nominal (85VAC – 135VAC)
- Flyback Output Voltage: 27.1V_{DC}
- LED Output Current: 228mA

This TRIAC dimmer compatible design incorporates the following features:

- Direct line-injection for improved power factor performance,
- Standard V_{CC} start-up with auxiliary winding bias circuit for improved system efficiency,
- Zener diode derived COFF current source for improved V_{CC} ripple rejection,
- Additional TRIAC holding current circuit for improved dimmer performance at low conduction angles,
- Output overvoltage protection (OVP).

NOTE: Refer to LM3448 Application Note, AN-2090 (TI Lit Number SNOA554), for additional information and BOM regarding this design.

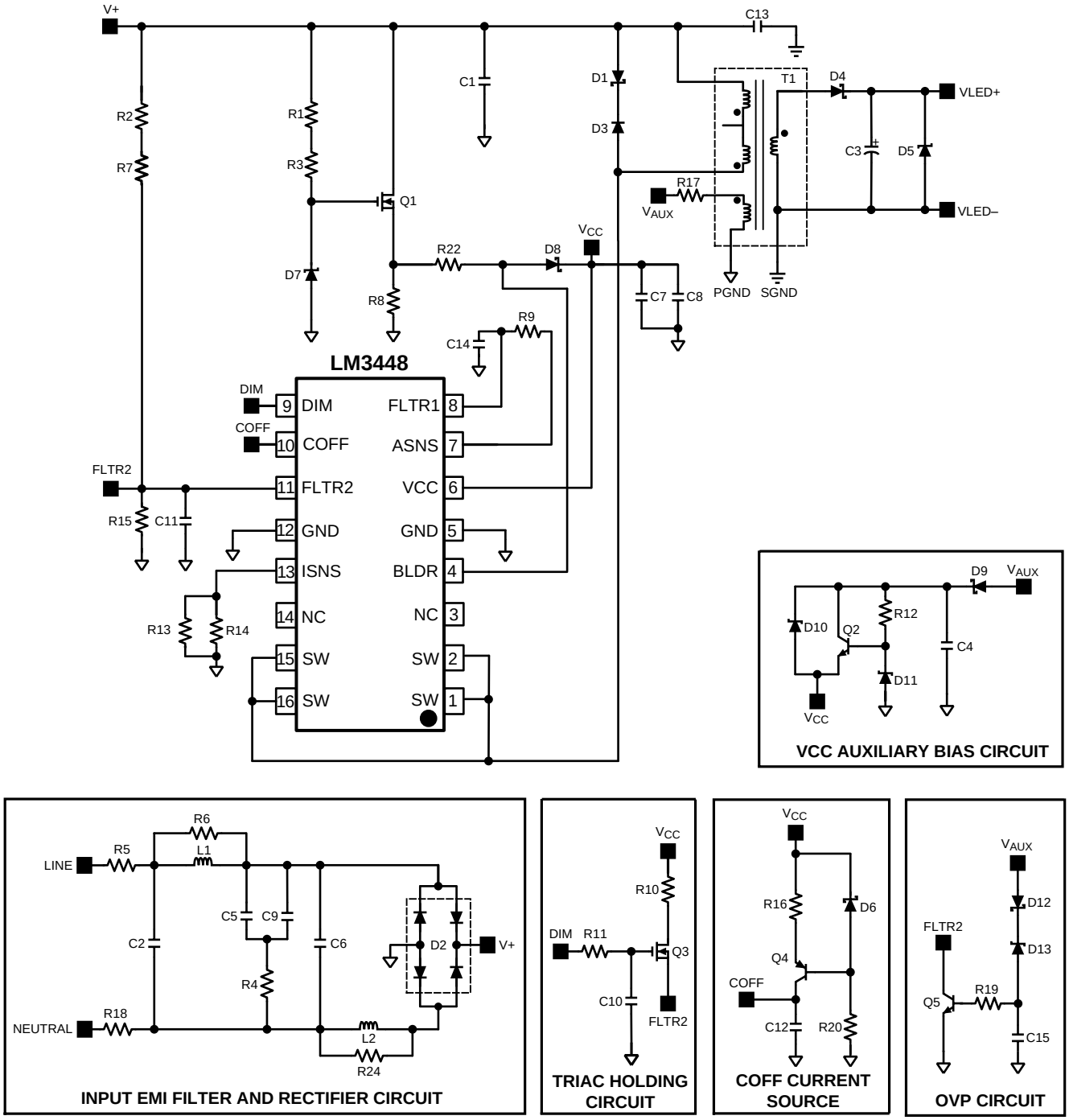


Figure 41. DESIGN #3 Circuit

DESIGN #4: 6W, 230VAC Isolated Flyback LED Driver with Direct Line Injection

SPECIFICATIONS:

- AC Input Voltage: 230VAC nominal (180VAC – 265VAC)
- Flyback Output Voltage: 27.0V_{DC}
- LED Output Current: 226mA

This TRIAC dimmer compatible design incorporates the following features:

- Direct line-injection for improved power factor performance
- Standard V_{CC} start-up with auxiliary winding bias circuit for improved system efficiency,
- V_{CC} derived COFF current source,
- Additional TRIAC holding current circuit for improved dimmer performance at low conduction angles,
- Output overvoltage protection (OVP).

NOTE: Refer to LM3448 Application Note, AN-2091 (TI Lit Number SNOA555), for additional information and BOM regarding this design.

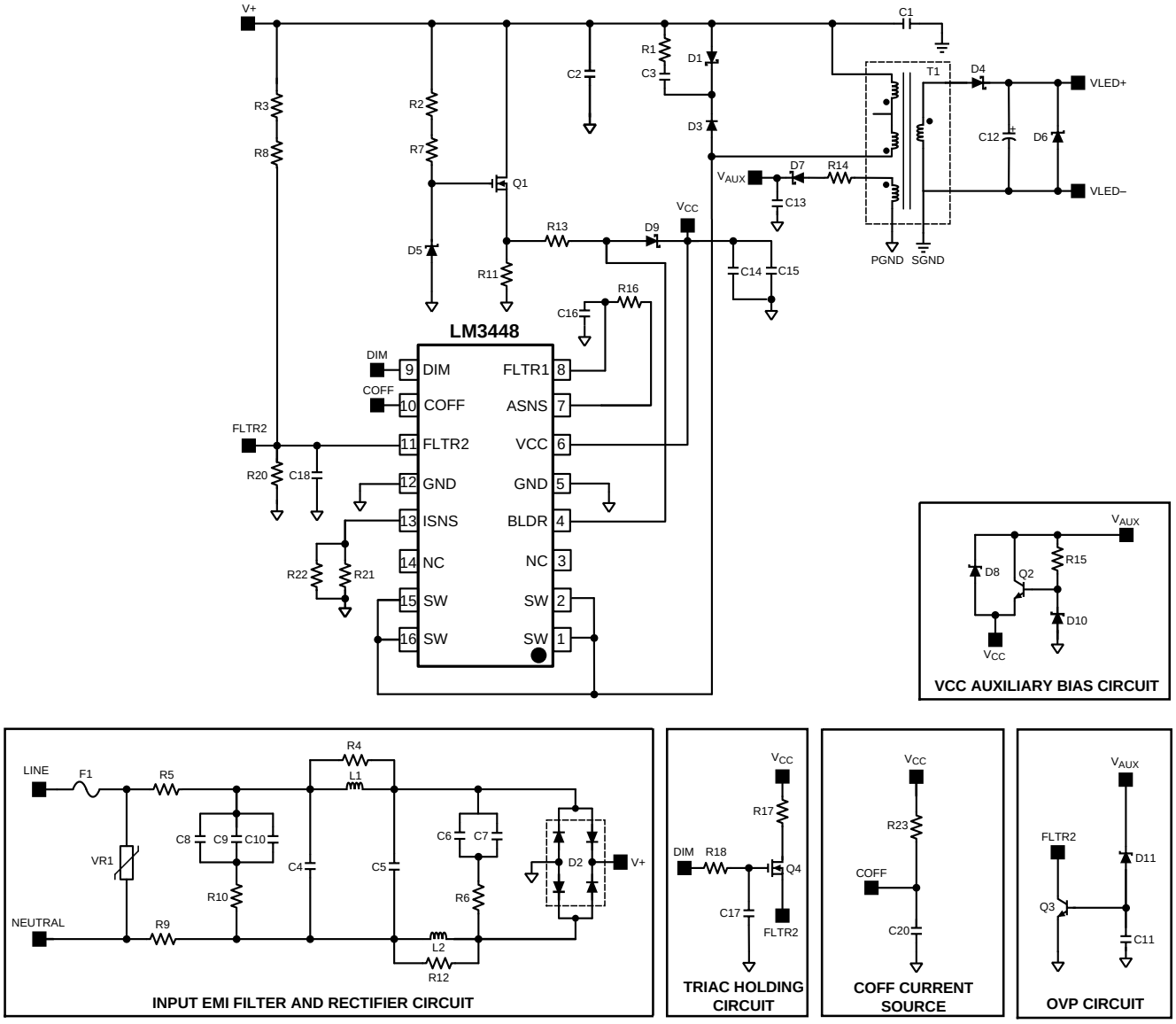


Figure 42. DESIGN #4 Circuit

REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	38

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3448MA/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM3448 MA	Samples
LM3448MAX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM3448 MA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

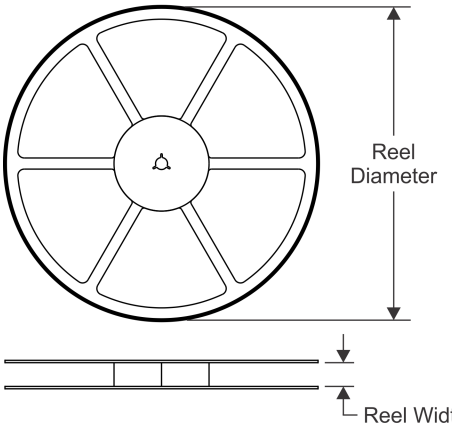
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

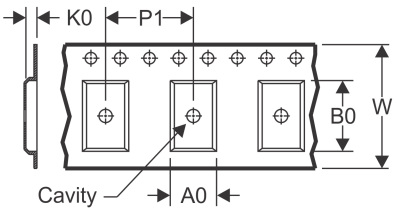
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

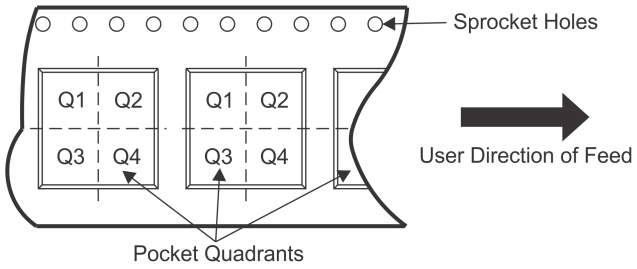


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

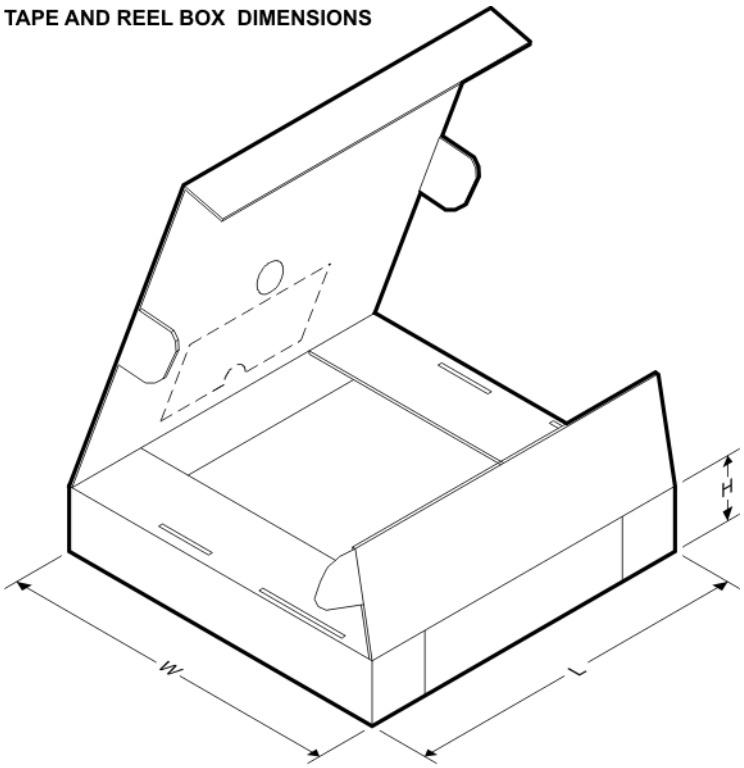
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3448MAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

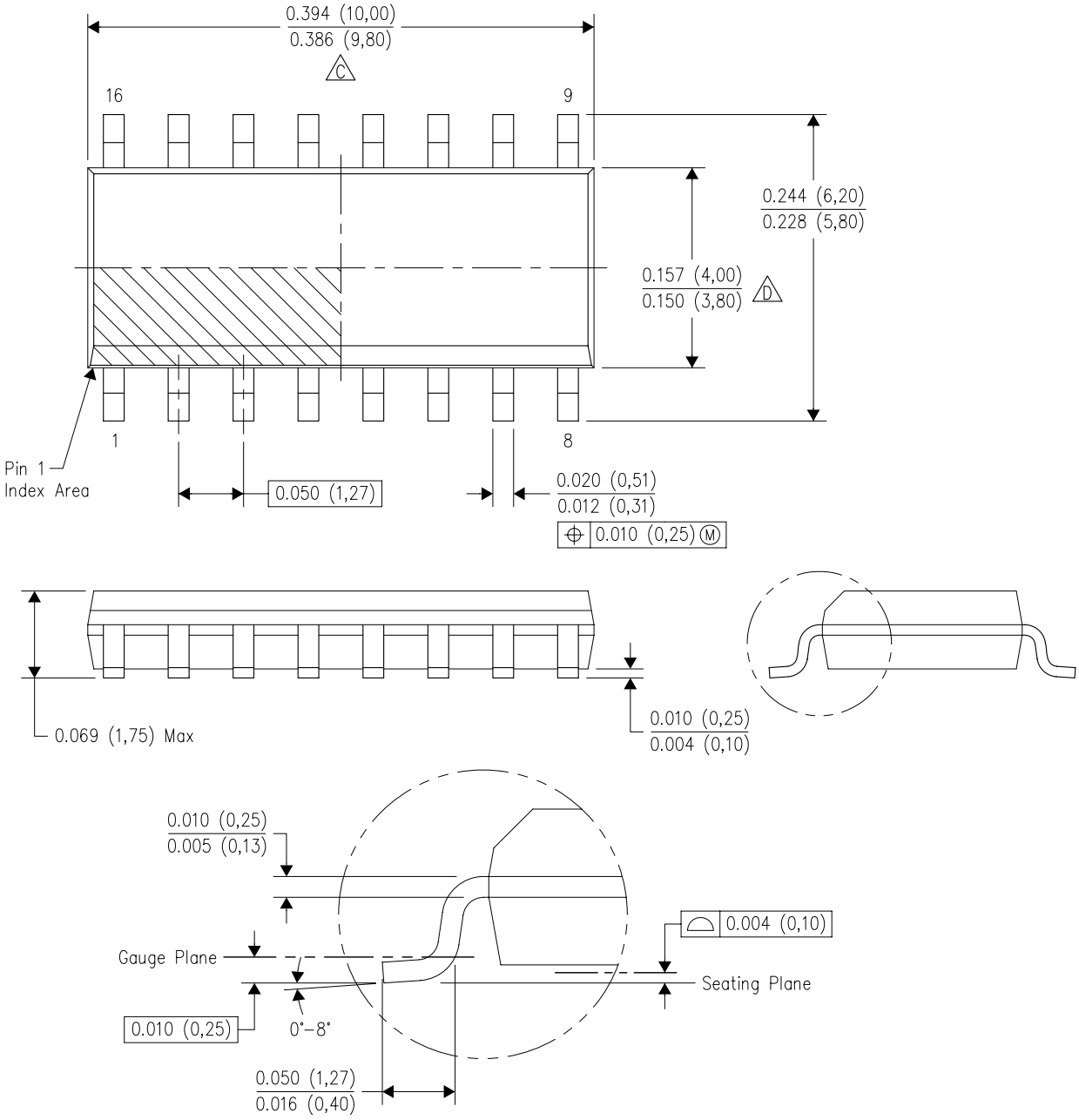
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3448MAX/NOPB	SOIC	D	16	2500	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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