

LMH6522 High Performance Quad DVGA

Check for Samples: [LMH6522](#)

FEATURES

- **OIP3: 49dBm @ 200MHz**
- **Noise Figure: 8.5dB**
- **Voltage Gain: 26dB**
- **1dB Gain Steps**
- **-3dB Bandwidth of 1400 MHz**
- **Gain Step Accuracy: 0.2 dB**
- **Disable Function for Each Channel**
- **Parallel and Serial Gain Control**
- **Low Power Mode for Power Management Flexibility**
- **Small Footprint WQFN Package**

APPLICATIONS

- **Cellular Base Stations**
- **Wideband and Narrowband IF Sampling Receivers**
- **Wideband Direct Conversion**
- **ADC Driver**

DESCRIPTION

The LMH6522 contains four, high performance, digitally controlled variable gain amplifiers (DVGA). It has been designed for use in narrowband and broadband IF sampling applications. Typically, the LMH6522 drives a high performance ADC in a broad range of mixed signal and digital communication applications such as mobile radio and cellular base stations where automatic gain control (AGC) is required to increase system dynamic range.

Each channel of LMH6522 has an independent, digitally controlled attenuator and a high linearity, differential output, amplifier. All circuitry has been optimized for low distortion and maximum system design flexibility. Power consumption is managed by a three-state enable pin. Individual channels can be disabled or placed into a Low Power Mode or a higher performance, High Power Mode.

The LMH6522 digitally controlled attenuator provides precise 1dB gain steps over a 31dB range. The digital attenuator can be controlled by either a SPI™ Serial bus or a high speed parallel bus.

The output amplifier has a differential output, allowing large signal swings on a single 5V supply. The low impedance output provides maximum flexibility when driving a wide range filter designs or analog to digital converters. For applications which have very large changes in signal level LMH6522 can support up to 62dB of gain range by cascading channels.

The LMH6522 operates over the industrial temperature range of -40°C to +85°C. The LMH6522 is available in a 54-Pin, thermally enhanced, WQFN package.

Performance Curve

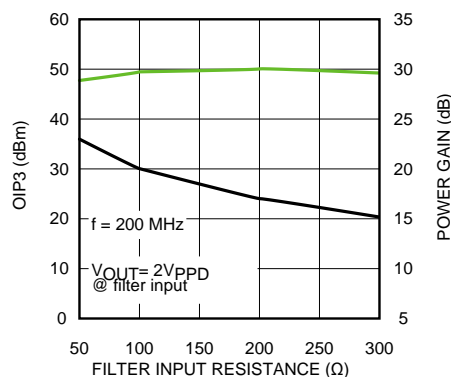


Figure 1. OIP3 vs Filter Input Resistance



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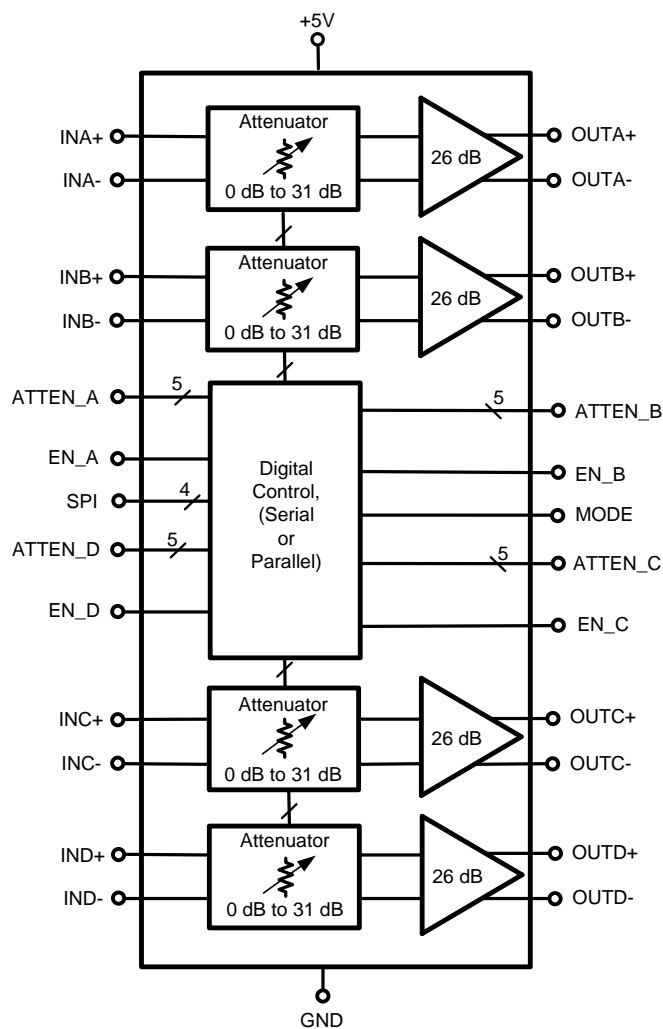
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Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | |
|--|-----------------|
| ESD Tolerance ⁽³⁾ | |
| Human Body Model | 2 kV |
| Machine Model | 200V |
| Charged Device Model | 750V |
| Positive Supply Voltage (Pin 3) | –0.6V to 5.5V |
| Differential Voltage between Any Two Grounds | <200 mV |
| Analog Input Voltage Range | –0.6V to 5.5V |
| Digital Input Voltage Range | –0.6V to 5.5V |
| Output Short Circuit Duration (one pin to ground) | Infinite |
| Junction Temperature | +150°C |
| Storage Temperature Range | –65°C to +150°C |
| Soldering Information | |
| Infrared or Convection (30 sec) | 260°C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Operating Ratings⁽¹⁾

| | |
|--|----------------|
| Supply Voltage (Pin 3) | 4.75V to 5.25V |
| Differential Voltage Between Any Two Grounds | <10 mV |
| Analog Input Voltage Range, AC Coupled | 0V to V+ |
| Temperature Range ⁽²⁾ | –40°C to +85°C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the Electrical Characteristics tables.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

| | | |
|---|-------------------|-------------------|
| Package Thermal Resistance ⁽¹⁾ | (θ_{JA}) | (θ_{JC}) |
| 54pin WQFN | 23°C/W | 4.7°C/W |

- (1) Junction to ambient (θ_{JA}) thermal resistance measured on JEDEC 4 layer board. Junction to case (θ_{JC}) thermal resistance measured at exposed thermal pad; package is not mounted to any PCB.

5V Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

The following specifications apply for single supply with $V_+ = 5V$, Maximum Gain (0 Attenuation), $R_L = 200\Omega$, $V_{OUT} = 4V_{PPD}$, $f_{in} = 200\text{ MHz}$, High Power Mode, Boldface limits apply at temperature extremes.

| Symbol | Parameter | Conditions | Min (4) | Typ (5) | Max (4) | Units |
|----------------------------|---|--|------------|------------|------------|-----------|
| Dynamic Performance | | | | | | |
| 3dBBW | –3dB Bandwidth | $V_{OUT} = 2 V_{PPD}$ | | 1.4 | | GHz |
| | Output Noise Voltage | Source = 100Ω | | 30 | | nV/√Hz |
| NF | Noise Figure | Source = 100Ω | | 8.5 | | dB |
| OIP3 | Output Third Order Intercept Point | $f = 100\text{ MHz}$, $V_{OUT} = 4\text{ dBm}$ per tone | | 53 | | dBm |
| | Output Third Order Intercept Point | $f = 200\text{ MHz}$, $V_{OUT} = 4\text{ dBm}$ per tone | | 49 | | |
| OIP2 | Output Second Order Intercept Point | $P_{OUT} = 4\text{ dBm}$ per Tone, $f_1 = 101\text{ MHz}$, $f_2 = 203\text{ MHz}$ | | 78 | | dBm |
| IMD3 | Third Order Intermodulation Products | $f = 100\text{ MHz}$, $V_{OUT} = 4\text{ dBm}$ per tone | | –98 | | dBc |
| | Third Order Intermodulation Products | $f = 200\text{ MHz}$, $V_{OUT} = 4\text{ dBm}$ per tone | | –90 | | |
| P1dB | 1dB Compression Point | | | 17 | | dBm |
| HD2 | Second Order Harmonic Distortion | $f = 100\text{ MHz}$, $V_{OUT} = 2 V_{PPD}$ | | –88 | | dBc |
| HD2 | Second Order Harmonic Distortion | $f = 200\text{ MHz}$, $V_{OUT} = 2 V_{PPD}$ | | –78 | | dBc |
| HD3 | Third Order Harmonic Distortion | $f = 100\text{ MHz}$, $V_{OUT} = 2 V_{PPD}$ | | –99 | | dBc |
| HD3 | Third Order Harmonic Distortion | $f = 200\text{ MHz}$, $V_{OUT} = 2 V_{PPD}$ | | –75 | | dBc |
| CMRR | Common Mode Rejection | $P_{in} = -15\text{ dBm}$ | | –35 | | dBc |
| Analog I/O | | | | | | |
| R_{IN} | Input Resistance | Differential, Measured at DC | | 97 | | Ω |
| V_{ICM} | Input Common Mode Voltage | Self Biased | | 2.5 | | V |
| | Maximum Input Voltage Swing | Volts peak to peak, differential | | 5.5 | | V_{PPD} |
| | Maximum Differential Output Voltage Swing | Differential, $f < 10\text{ MHz}$ | | 10 | | V_{PPD} |
| R_{OUT} | Output Resistance | Differential, Measured at DC | | 20 | | Ω |
| XTLK | Channel to Channel Crosstalk | Maximum Gain, $f = 200\text{ MHz}$ | | –65 | | dBc |
| Gain Parameters | | | | | | |
| | Maximum Voltage Gain | Attenuation code 00000 | | 25.74 | | dB |
| | Minimum Gain | Attenuation code 11111 | | –4.3 | | dB |
| | Gain Steps | | | 32 | | |
| | Gain Step Size | | | 1.0 | | dB |
| | Channel Matching | Gain error between channels | | ± 0.15 | | dB |
| | Gain Step Error | Any two adjacent steps over entire range | | ± 0.5 | | dB |
| | Gain Step Error | Any two adjacent steps, 0 dB attenuation to 23 dB attenuation | | ± 0.1 | | dB |
| | Gain Step Phase Shift | Any two adjacent steps over entire range | | ± 3 | | Degrees |
| | Gain Step Phase Shift | Any two adjacent steps, 0dB attenuation to 23 dB attenuation | | ± 2 | | Degrees |
| | Gain Step Switching Time | | | 20 | | ns |
| | Enable/ Disable Time | Settled to 90% level | | 200 | | ns |

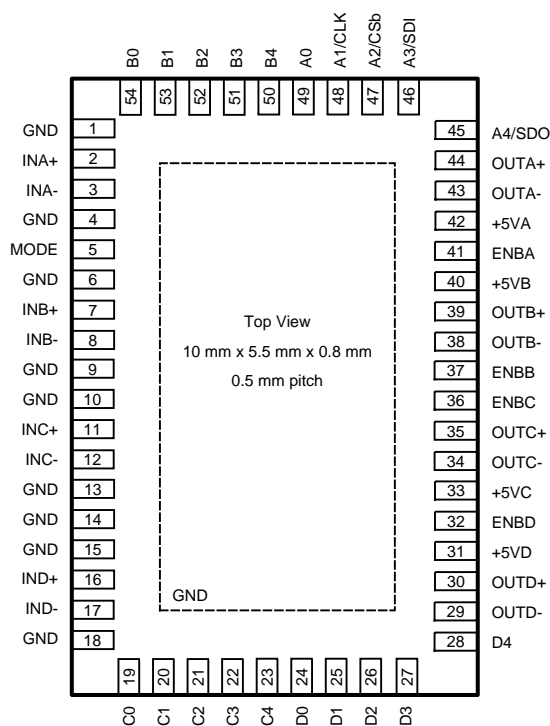
- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No specification of parametric performance is indicated in the electrical tables under conditions different than those tested
- (2) Negative input current implies current flowing out of the device.
- (3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
- (4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.
- (5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

5V Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾ (continued)

The following specifications apply for single supply with $V_+ = 5V$, Maximum Gain (0 Attenuation), $R_L = 200\Omega$, $V_{OUT} = 4V_{PPD}$, $f_{in} = 200\text{ MHz}$, High Power Mode, Boldface limits apply at temperature extremes.

| Symbol | Parameter | Conditions | Min (4) | Typ (5) | Max (4) | Units |
|--|--|---|------------|------------|------------|-------|
| Power Requirements | | | | | | |
| ICC | Supply Current | | | 465 | 485 | mA |
| P | Power | | | 2.3 | 2.43 | W |
| I _{BIAS} | Output Pin Bias Current | External inductor, no load, $V_{OUT} < 200\text{ mV}$ | | 36 | | mA |
| ICC | Disabled Supply Current | | | 74 | | mA |
| All Digital Inputs Except Enables | | | | | | |
| | Logic Compatibility | TTL, 2.5V CMOS, 3.3V CMOS, 5V CMOS | | | | |
| VIL | Logic Input Low Voltage | | 0 | | 0.4 | V |
| VIH | Logic Input High Voltage | | 2.0 | | 5.0 | V |
| IIH | Logic Input High Input Current | Digital Input Voltage = 2.0V | | –9 | | μA |
| IIL | Logic Input Low Input Current | Digital Input Voltage = 0.4V | | –47 | | μA |
| Enable Pins | | | | | | |
| VIL | Logic Input Low Voltage | Amplifier disabled | 0 | | 0.4 | V |
| VIM | Logic Input Mid Level | Amplifier Low Power Mode | 0.6 | | 1.9 | V |
| VIH | Logic Input High Level | Amplifier High Power Mode | 2.2 | | 5 | V |
| VSB | Enable Pin Self Bias Voltage | No external load | | 1.37 | | V |
| IIL | Input Bias Current, Logic Low | Digital input voltage = 0.2V | | –200 | | μA |
| IIM | Input Bias Current, Logic Mid | Digital input voltage = 1.5V | | 28 | | μA |
| IIH | Input Bias Current, Logic High | Digital input voltage = 3.0V | | 500 | | μA |
| Parallel Mode Timing | | | | | | |
| t _{GS} | Setup Time | | 3 | | | ns |
| t _{GH} | Hold Time | | 3 | | | ns |
| Serial Mode | | | | | | |
| f _{CLK} | SPI Clock Frequency | 50% duty cycle, ATE tested @ 20MHz | 20 | 50 | | MHz |
| Low Power Mode | | | | | | |
| (Enable pins are self biased) | | | | | | |
| I _{CC} | Total Supply Current | all four channels in low power mode | | 370 | 398 | mA |
| I _{BIAS} | Output Pin Bias Current | External Inductor, No Load, $V_{OUT} < 200\text{mV}$ | | 26 | | mA |
| I _{CC} | Disabled Supply Current | Enable Pin < 0.4V | | 74 | | mA |
| OIP3 | Output Intermodulation Intercept Point | f = 200 MHz, $V_{OUT} = 4\text{ dBm}$ per tone | | 44 | | dBm |
| P1dB | 1dB Compression Point | | | 16 | | dBm |
| HD2 | Second Order Harmonic Distortion | f = 100 MHz, $V_{OUT} = 2 V_{PPD}$ | | –90 | | dBc |
| HD2 | Second Order Harmonic Distortion | f = 200 MHz, $V_{OUT} = 2 V_{PPD}$ | | –79 | | dBc |
| HD3 | Third Order Harmonic Distortion | f = 100 MHz, $V_{OUT} = 2 V_{PPD}$ | | –91 | | dBc |
| HD3 | Third Order Harmonic Distortion | f = 200 MHz, $V_{OUT} = 2 V_{PPD}$ | | –79 | | dBc |

CONNECTION DIAGRAM



**Figure 2. 54-Pin WQFN
Top View**

PIN DESCRIPTIONS

| Pin Number | Symbol | Pin Category | Description |
|---|------------------------|-----------------|--|
| Analog I/O | | | |
| 2, 3 | INA+, INA - | Analog Input | Differential inputs channel A |
| 44, 43 | OUTA+, OUTA- | Analog Output | Differential outputs Channel A |
| 7, 8 | INB+, INB - | Analog Input | Differential inputs channel B |
| 39, 38 | OUTB+, OUTB- | Analog Output | Differential outputs Channel B |
| 11, 12 | INC+, INC - | Analog Input | Differential inputs channel C |
| 35, 34 | OUTC+, OUTC- | Analog Output | Differential outputs Channel C |
| 16, 17 | IND+, IND - | Analog Input | Differential inputs channel D |
| 30, 29 | OUTD+, OUTD- | Analog Output | Differential outputs Channel D |
| Power | | | |
| 1, 4, 6, 9, 10, 13, 14, 15, 18 | GND | Ground | Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins. |
| 31, 33, 40, 42 | +5VD, +5VC, +5VB, +5VA | Power | Power supply pins. Valid power supply range is 4.75V to 5.25V. |
| Exposed Center Pad | | Thermal/ Ground | Thermal management/ Ground |
| Digital Inputs | | | |
| 5 | MODE | Digital Input | 0= Parallel Mode, 1 = Serial Mode |
| Parallel Mode Digital Pins, MODE = Logic Low | | | |
| 49, 48, 47, 46, 45 | A0, A1, A2, A3, A4 | Digital Input | Channel A attenuator control |
| 41 | ENBA | Digital Input | Channel A enable pin |
| 54, 53, 52, 51, 50 | B0, B1, B2, B3, B4 | Digital Input | Channel B attenuator control |

PIN DESCRIPTIONS (continued)

| Pin Number | Symbol | Pin Category | Description |
|--|--------------------|--------------------------------|--|
| 37 | ENBB | Digital Input | Channel B enable pin: pin has three states: Low, Mid, High |
| 19, 20, 21, 22, 23 | C0, C1, C2, C3, C4 | Digital Input | Channel C attenuator control |
| 36 | ENBC | Digital Input | Channel C enable pin |
| 24, 25, 26, 27, 28 | D0, D1, D2, D3, D4 | Digital Input | Channel D attenuator control |
| 32 | ENBD | Digital Input | Channel D enable pin |
| Serial Mode Digital Pins, MODE = Logic High SPI™ Compatible | | | |
| 45 | SDO | Digital Output- Open Collector | Serial Data Output (Requires external bias.) |
| 46 | SDI | Digital Input | Serial Data In |
| 47 | CSb | Digital Input | Chip Select |
| 48 | CLK | Digital Input | Clock |

PIN LIST

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1 | GND | 28 | D4 |
| 2 | INA+ | 29 | OUTD– |
| 3 | INA– | 30 | OUTD+ |
| 4 | GND | 31 | +5VD |
| 5 | MODE | 32 | ENBD |
| 6 | GND | 33 | +5VC |
| 7 | INB+ | 34 | OUTC– |
| 8 | INB– | 35 | OUTC+ |
| 9 | GND | 36 | ENBC |
| 10 | GND | 37 | ENBB |
| 11 | INC+ | 38 | OUTB– |
| 12 | INC– | 39 | OUTB+ |
| 13 | GND | 40 | +5VB |
| 14 | GND | 41 | ENBA |
| 15 | GND | 42 | +5VA |
| 16 | IND+ | 43 | OUTA– |
| 17 | IND– | 44 | OUTA+ |
| 18 | GND | 45 | A4 / SDO |
| 19 | C0 | 46 | A3 / SDI |
| 20 | C1 | 47 | A2 / CSb |
| 21 | C2 | 48 | A1 / CLK |
| 22 | C3 | 49 | A0 |
| 23 | C4 | 50 | B4 |
| 24 | D0 | 51 | B3 |
| 25 | D1 | 52 | B2 |
| 26 | D2 | 53 | B1 |
| 27 | D3 | 54 | BO |

Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).

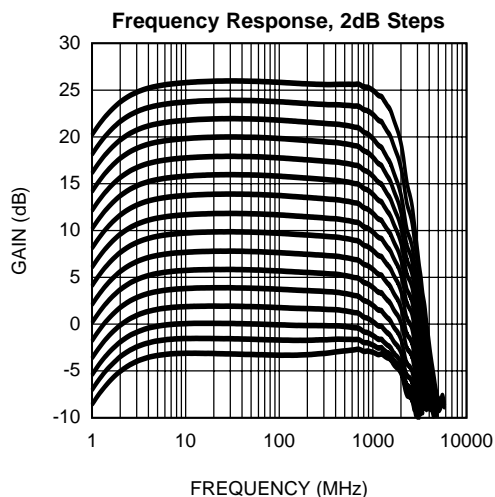


Figure 3.

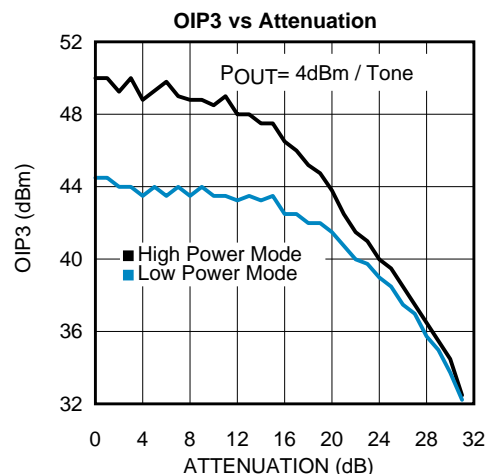


Figure 4.

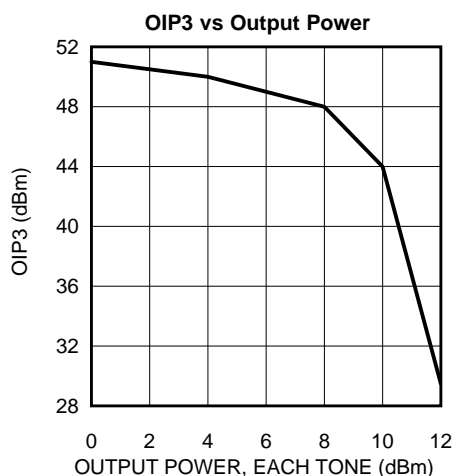


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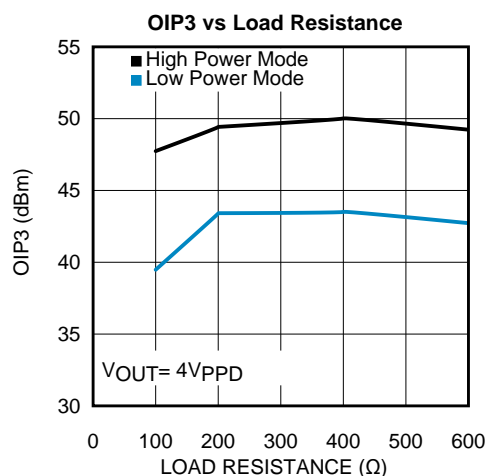


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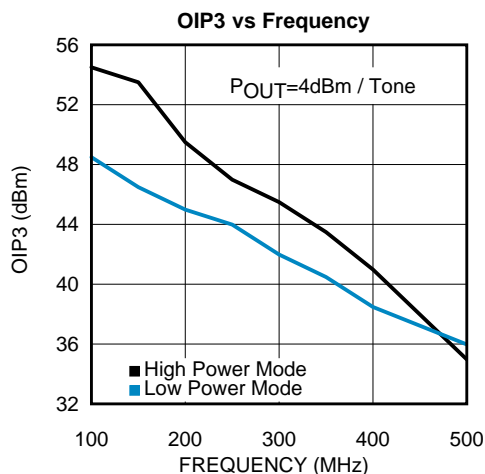


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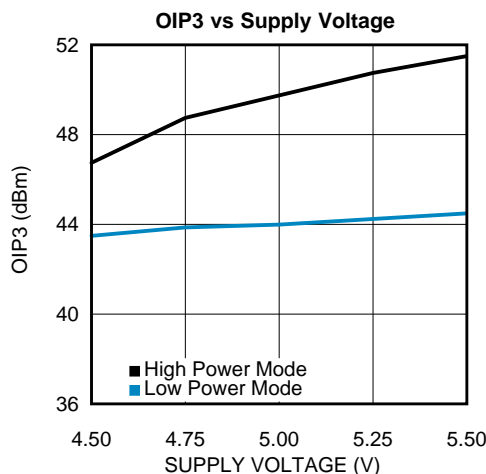


Figure 8.

Typical Performance Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).

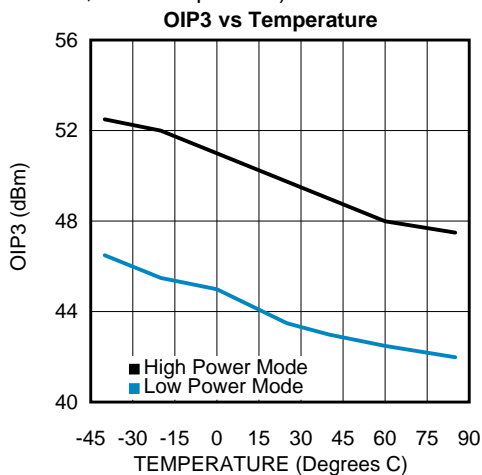


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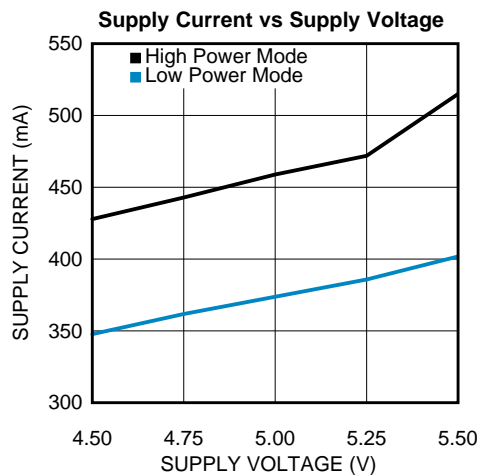


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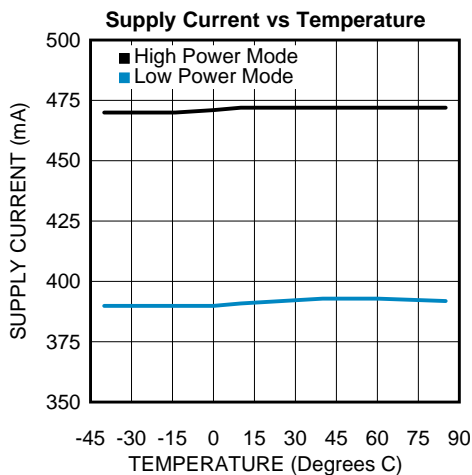


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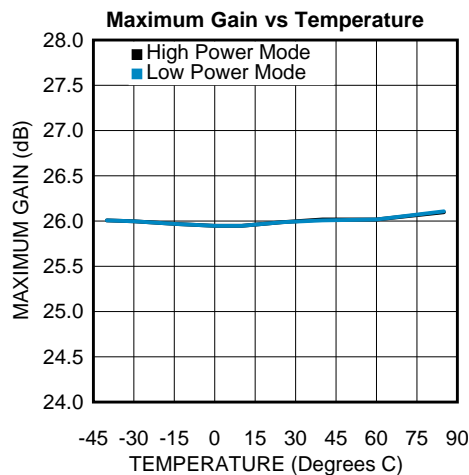


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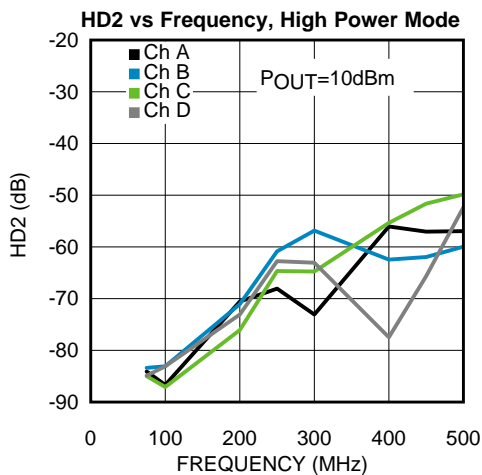


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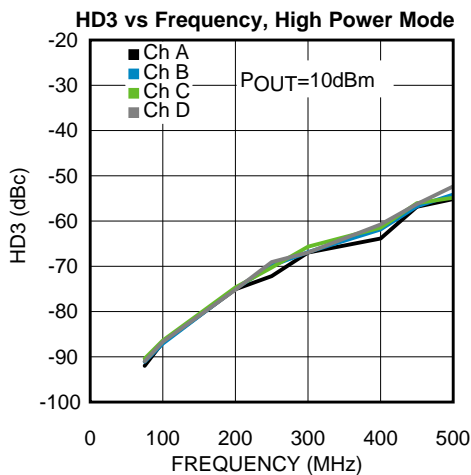
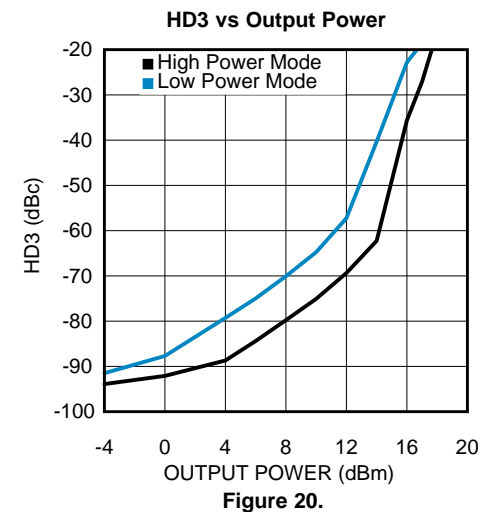
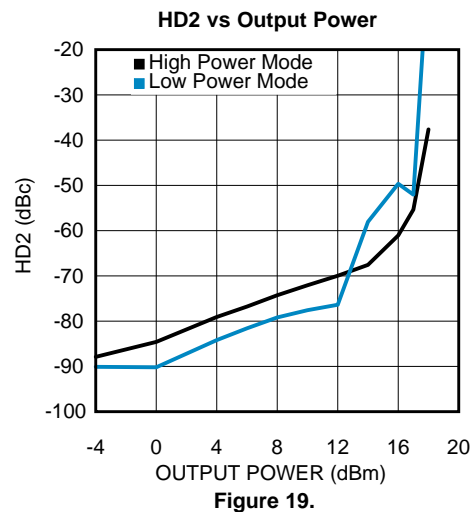
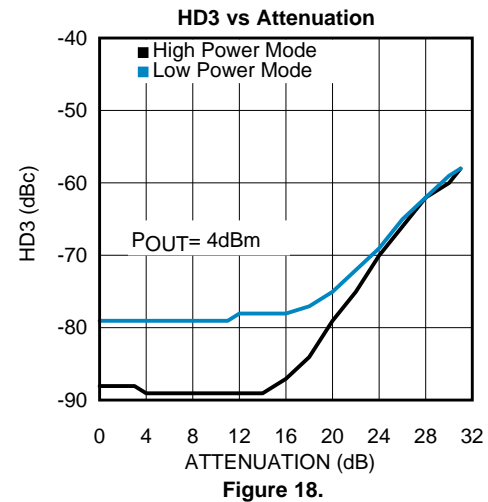
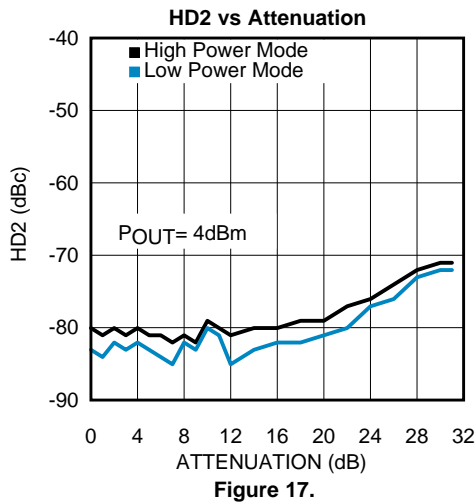
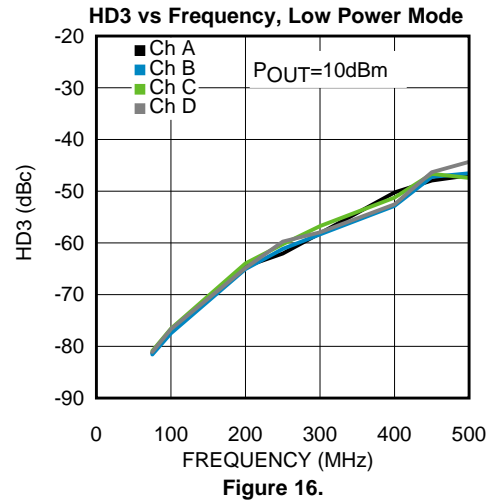
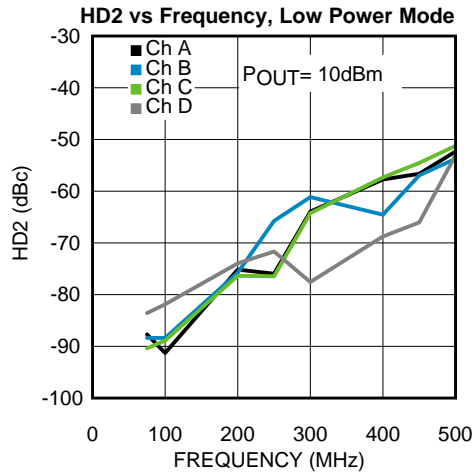


Figure 14.

Typical Performance Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).



Typical Performance Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).

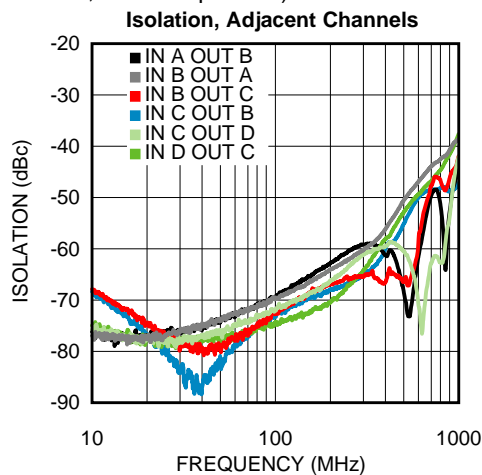


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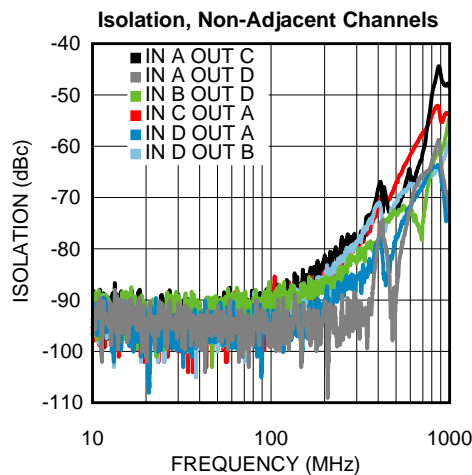


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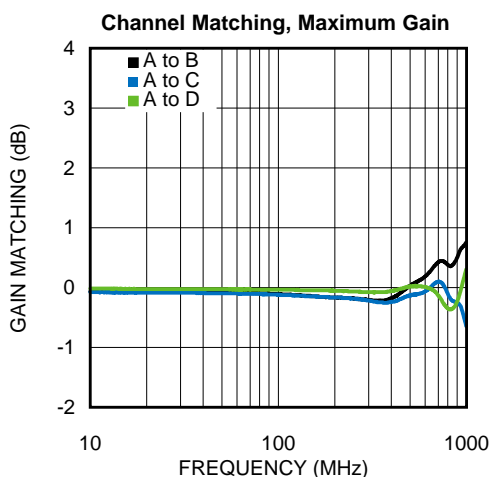


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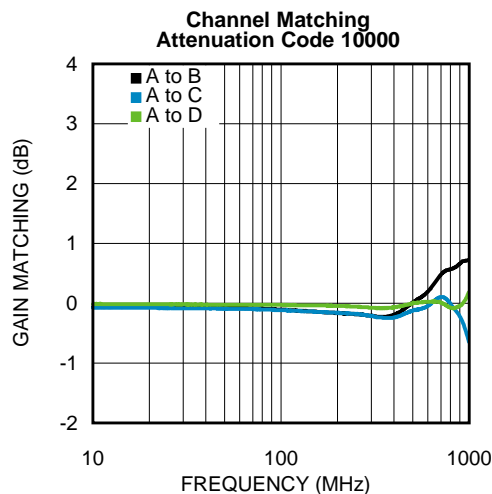


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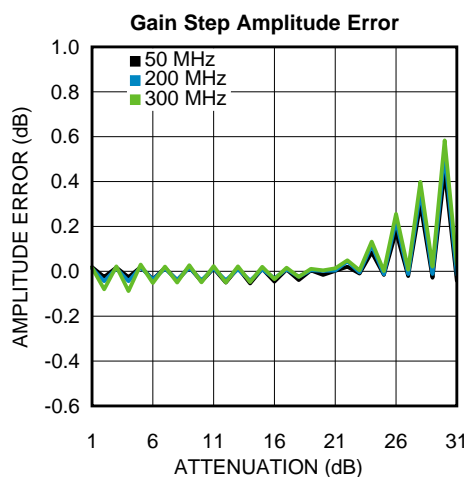


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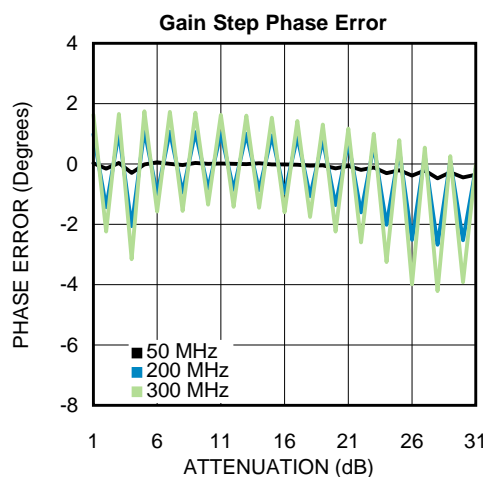
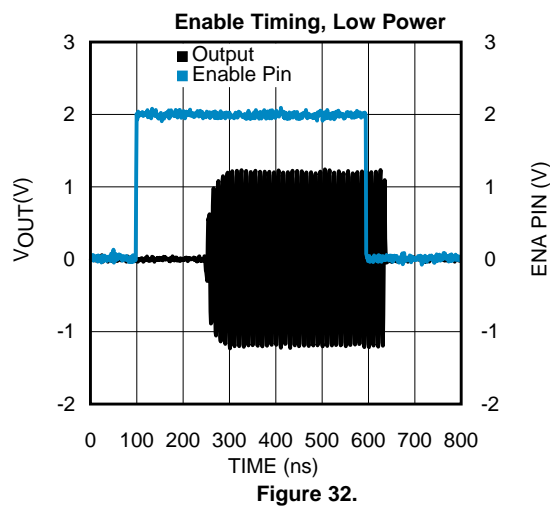
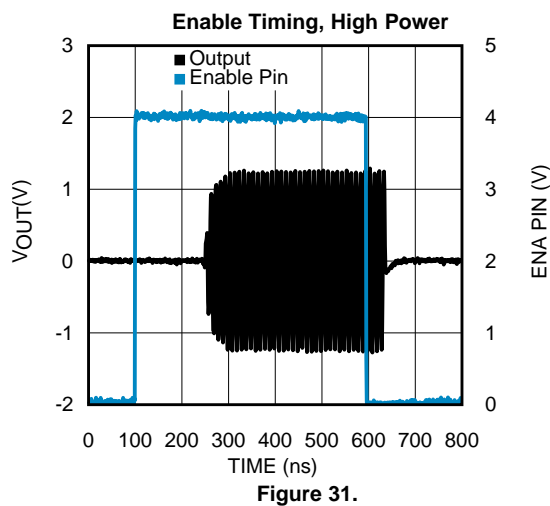
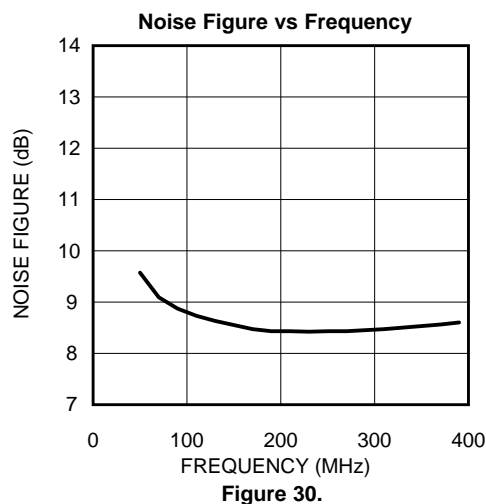
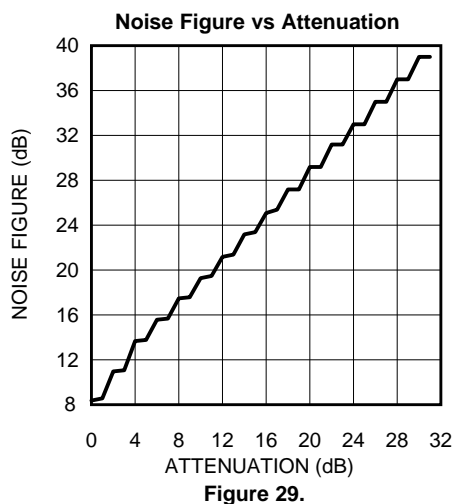
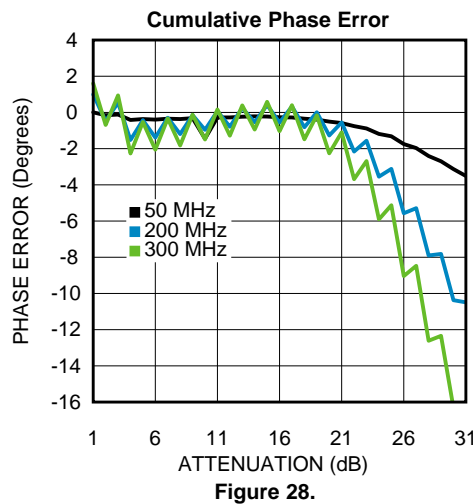
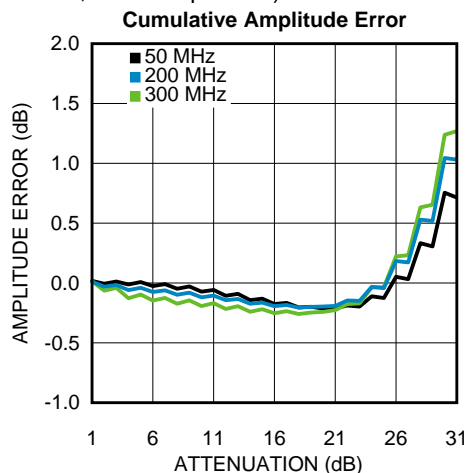


Figure 26.

Typical Performance Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).



Typical Performance Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).

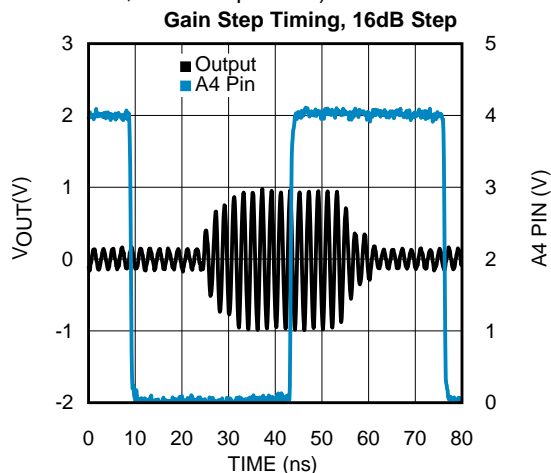


Figure 33.

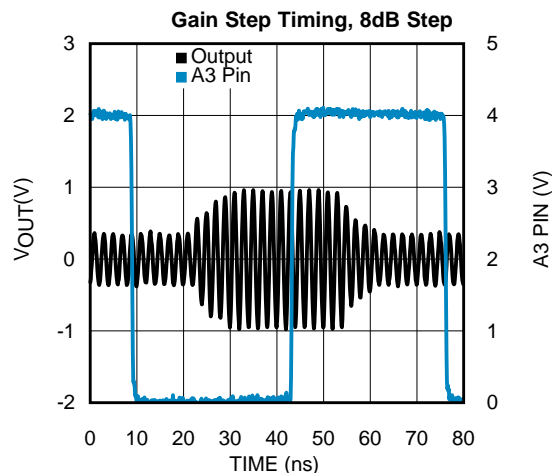


Figure 34.

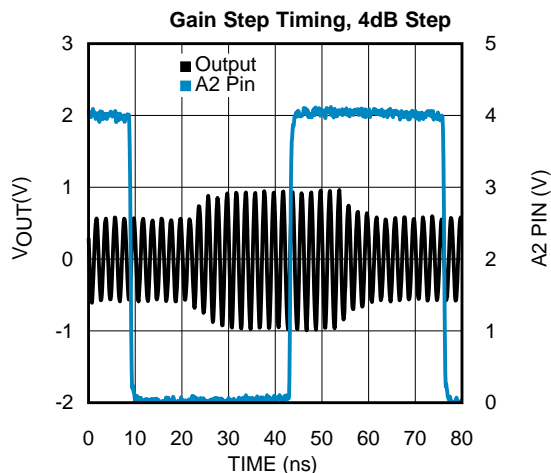


Figure 35.

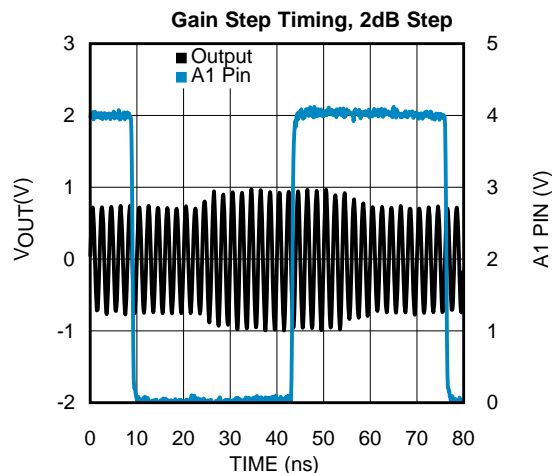


Figure 36.

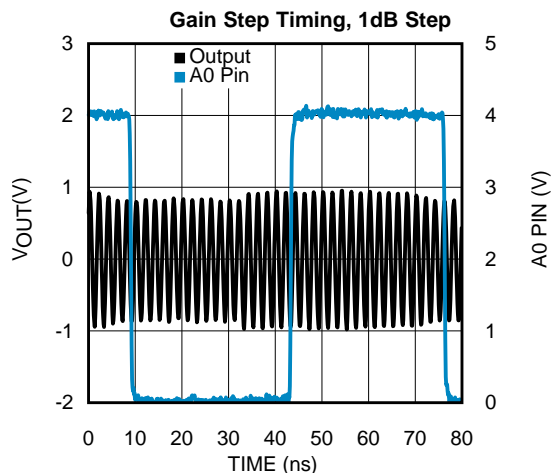


Figure 37.

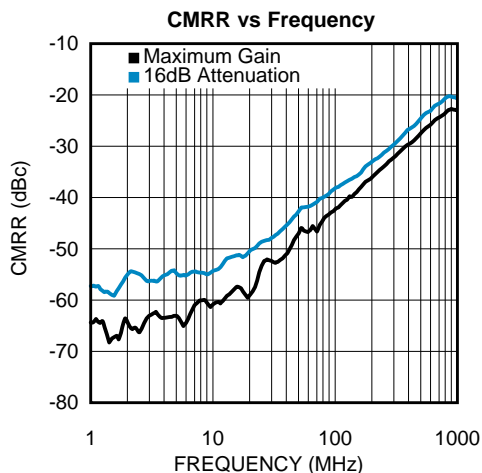


Figure 38.

Typical Performance Characteristics (continued)

($T_A = 25^\circ\text{C}$, $V_+ = 5\text{V}$, $R_L = 200\Omega$, Maximum Gain, High Power, $f = 200\text{MHz}$; LMH6522 soldered onto LMH6522EVAL evaluation board, Unless Specified).

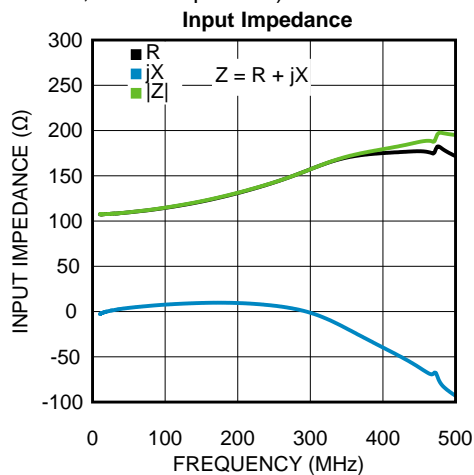


Figure 39.

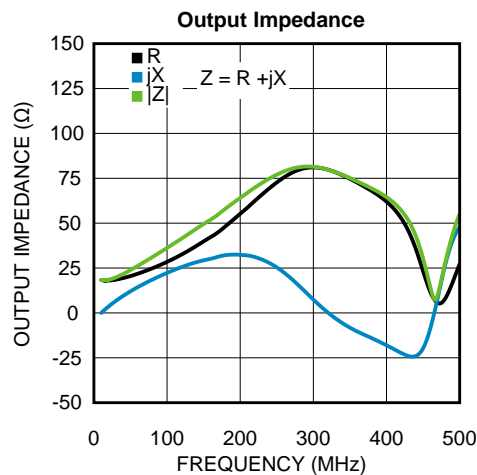


Figure 40.

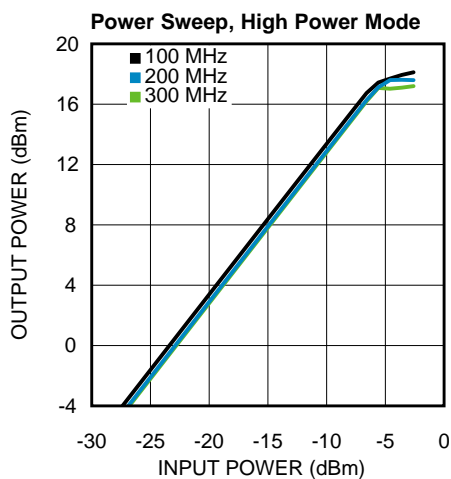


Figure 41.

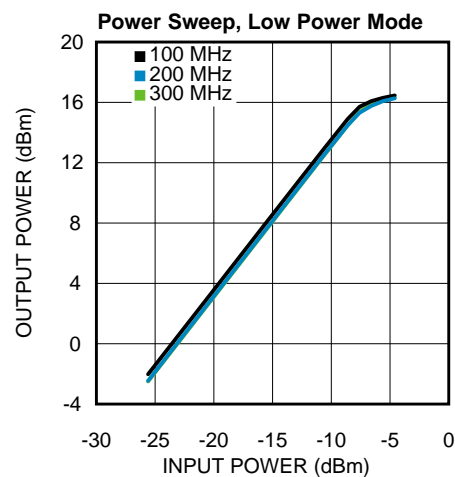


Figure 42.

APPLICATION INFORMATION

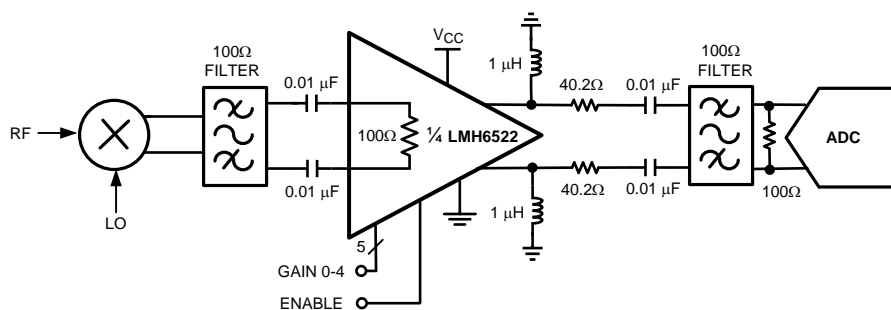


Figure 43. LMH6522 Typical Application

INTRODUCTION

The LMH6522 is a fully differential amplifier optimized for signal path applications up to 400 MHz. The LMH6522 has a 100Ω input and a low impedance output. The gain is digitally controlled over a 31 dB range from +26dB to -5dB. The LMH6522 is optimized for accurate gain steps and minimal phase shift combined with low distortion products. This makes the LMH6522 ideal for voltage amplification and an ideal analog to digital converter (ADC) driver where high linearity is necessary.

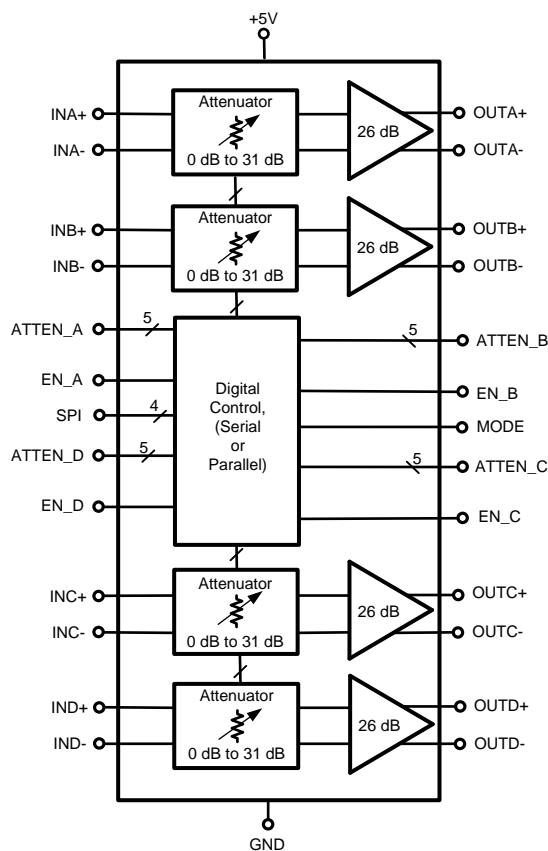


Figure 44. LMH6522 Block Diagram

BASIC CONNECTIONS

A voltage between 4.75 V and 5.25 V should be applied to the supply pin labeled +5V. Each supply pin should be decoupled with a low inductance, surface-mount ceramic capacitor of 0.01 μ F as close to the device as possible. Additional bypass capacitors of 0.1 μ F and 1 nF are optional, but would provide bypassing over a wider frequency range.

The outputs of the LMH6522 need to be biased to ground using inductors and output coupling capacitors of 0.01 μ F are recommended. The input pins are self biased to 2.5V and should be ac-coupled with 0.01 μ F capacitors as well. The output bias inductors and ac-coupling capacitors are the main limitations for operating at low frequencies. Larger values of inductance on the bias inductors and larger values of capacitance on the coupling capacitors will give more low frequency range. Using bias inductors over 1 μ H, however, may compromise high frequency response due to unwanted parasitic loading on the amplifier output pins.

Each channel of the LMH6522 consists of a digital step attenuator followed by a low distortion 26 dB fixed gain amplifier and a low impedance output stage. The attenuation is digitally controlled over a 31 dB range from 0 dB to 31 dB. The LMH6522 has a 100 Ω differential input impedance and a low, 20 Ω , output impedance.

Each channel of the LMH6522 has an enable pin. Grounding the enable pin will put the channel in a power saving shutdown mode. Additionally, there are two “on” states which gives the option of two power modes. High Power Mode is selected by biasing the enable pins at 2.0 V or higher. The LMH6522 enable pins will self bias to the Low Power State, alternatively supplying a voltage between 0.6V and 1.8V will place the channel in Low Power Mode. If connected to a TRI-STATE buffer the LMH6522 enable pins will be in shutdown for a logic 0 output, in High Power Mode for a logic 1 state and they will self bias to Low Power Mode for the high impedance state.

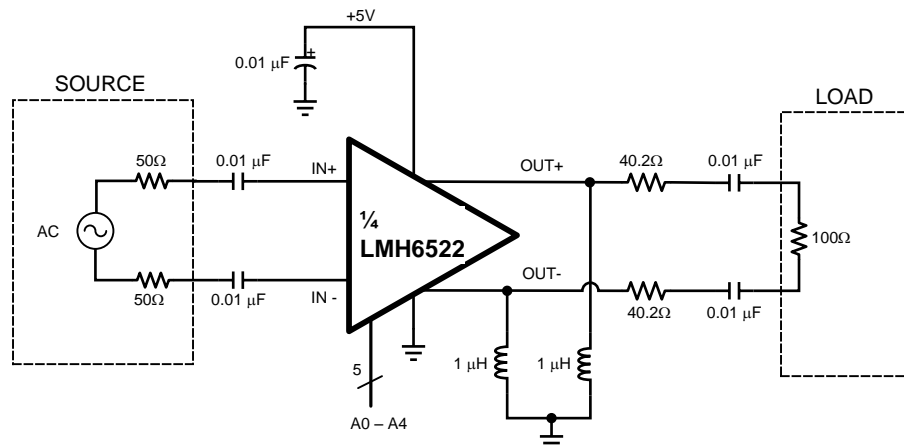


Figure 45. LMH6522 Basic Connections Schematic

INPUT CHARACTERISTICS

The LMH6522 input impedance is set by internal resistors to a nominal 100 Ω . Process variations will result in a range of values. At higher frequencies parasitic reactances will start to impact the impedance. This characteristic will also depend on board layout and should be verified on the customer's system board.

At maximum gain the digital attenuator is set to 0 dB and the input signal will be much smaller than the output. At minimum gain the output is 5 dB or more smaller than the input. In this configuration the input signal will begin to clip against the ESD protection diodes before the output reaches maximum swing limits. The input signal cannot swing more than 0.5V below the negative supply voltage (normally 0V) nor should it exceed the positive supply voltage. The input signal will clip and cause severe distortion if it is too large. Because the input stage self biases to approximately mid rail the supply voltage will impose the limit for input voltage swing.

At higher frequencies the LMH6522 input impedance is not purely resistive. In Figure 46 a circuit is shown that matches the amplifier input impedance with a source that is 100 Ω . This would be the case when connecting the LMH6522 directly to a mixer. For an easy way to calculate the L and C circuit values there are several options for online tools or down-loadable programs. The following tool might be helpful.

Excel can also be used for simple circuits; however, the “Analysis ToolPak” add-in must be installed to calculate complex numbers.

<http://www.circuitsage.com/matching/matcher2.html>

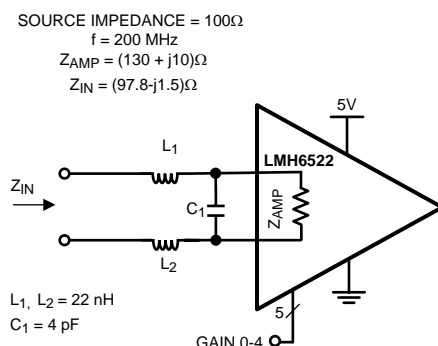


Figure 46. Differential LC Conversion Circuit

OUTPUT CHARACTERISTICS

The LMH6522 has a low impedance output very similar to a traditional Op-amp output. This means that a wide range of loads can be driven with good performance. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier. This flexibility makes system design and gain calculations very easy.

By using a differential output stage the LMH6522 can achieve very large voltage swings on a single 5V supply. This is illustrated in Figure 47. This figure shows how a voltage swing of $5V_{PPD}$ is realized while only swinging $2.5V_{PP}$ on each output. The LMH6522 can swing up to $10V_{PPD}$ which is sufficient to drive most ADCs to full scale while using a matched impedance anti alias filter between the amplifier and the ADC. The LMH6522 has been designed for AC coupled applications and has been optimized for operation above 5 MHz.

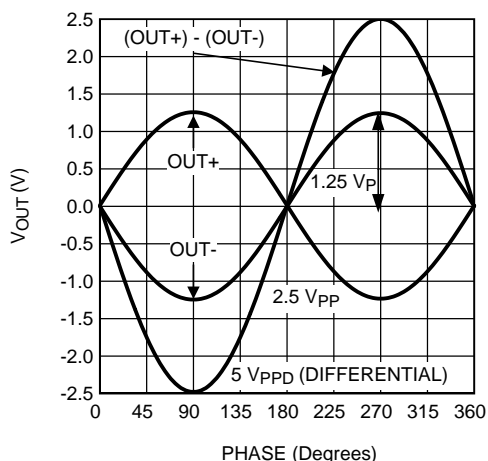


Figure 47. Differential Output Voltage

Like most closed loop amplifiers the LMH6522 output stage can be sensitive to capacitive loading. To help with board layout and to help minimize sensitivity to bias inductor capacitance the LMH5522 output lines have internal 10Ω resistors. These resistors should be taken into account when choosing matching resistor values. This is shown in Figure 45 as using 40.2Ω resistors instead of 50Ω resistors to match the 100Ω differential load. Best practise is to place the external termination resistors as close to the DVGA output pins as possible. Due to reactive components between the DVGA output and the filter input it may be desirable to use even smaller value resistors than a simple calculation would indicate. For instance, at 200 MHz resistors of 30 Ohms provide slightly better OIP3 performance on the LMH6522EVAL evaluation board and may also provide a better match to the filter input.

The LMH6522 output pins require a DC path to ground. On the evaluation board, inductors are installed to provide proper output biasing. The bias current is approximately 36mA per output pin. The resistance of the output bias inductors will raise the output common mode slightly. An inductor with low resistance will keep the output bias voltage close to zero, so the DC resistance of the inductor chosen will be important. It is also important to make sure that the inductor can handle the 36mA of bias current.

In addition to the DC current in the inductor there will be some AC current as well. With large inductors and high operating frequencies the inductor will present a very high impedance and will have minimal AC current. If the inductor is chosen to have a smaller value, or if the operating frequency is very low there could be enough AC current flowing in the inductor to become significant. The total current should not exceed the inductor current rating.

Another reason to choose low resistance bias inductors is that due to the nature of the LMH6522 output stage, the output offset voltage is determined by the output bias components. The output stage has an offset current that is typically 3mA and this offset current, multiplied by the resistance of the output bias inductors will determine the output offset voltage.

The ability of the LMH6522 to drive low impedance loads while maintaining excellent OIP3 performance creates an opportunity to greatly increase power gain and drive low impedance filters. Figure 48 shows the OIP3 performance of the LMH6522 over a range of filter impedances. Also on the same graph is the power gain realized by changing load impedance. The power gain reflects the 6dB of loss caused by the termination resistors necessary to match the amplifier output impedance to the filter characteristic impedance. The graphs shows the ability of the LMH6522 to drive a constant voltage to an ADC input through various filter impedances with very little change in OIP3 performance. This gives the system designer much needed flexibility in filter design.

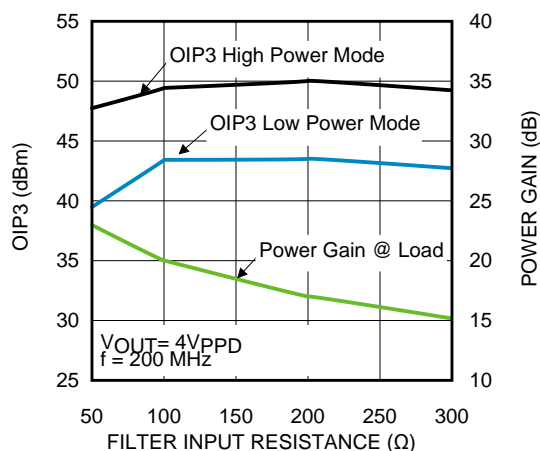


Figure 48. OIP3 and Power Gain vs Filter Impedance
OIP3 and Gain Measured at Amplifier Output, Filter Back Terminated

Printed circuit board (PCB) design is critical to high frequency performance. In order to ensure output stability the load matching resistors should be placed as close to the amplifier output pins as possible. This allows the matching resistors to mask the board parasitics from the amplifier output circuit. An example of this is shown in Figure 49. If the Filter is a bandpass filter with no DC path the 0.01μF coupling capacitors can be eliminated. The LMH6522EVAL evaluation board is available to serve a guide for system board layout.

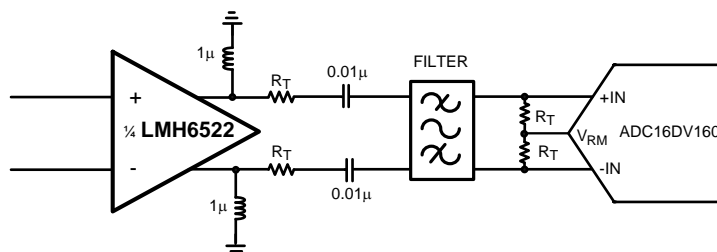


Figure 49. Output Configuration

CASCADE OPERATION

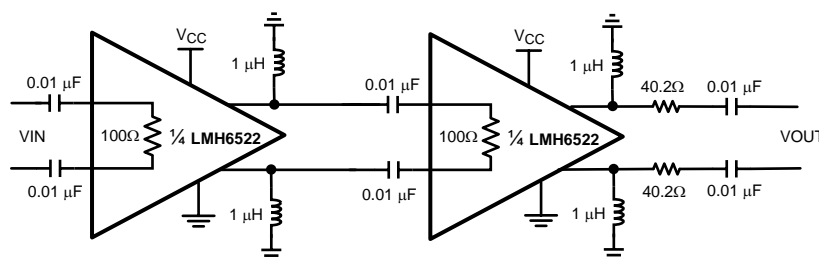


Figure 50. Schematic for Cascaded Amplifiers

With four amplifiers in one package the LMH6522 is ideally configured for cascaded operation. By using two amplifiers in series additional gain range can be achieved. The schematic in Figure 50 shows one way to connect two stages of the LMH6522. The resultant frequency response is shown below in Figure 51. When using the LMH6522 amplifiers in a cascade configuration it is important to keep the signal level within reasonable limits at all nodes of the signal path. With over 40dB of total gain it is possible to amplify signals to clipping levels if the gain is not set correctly.

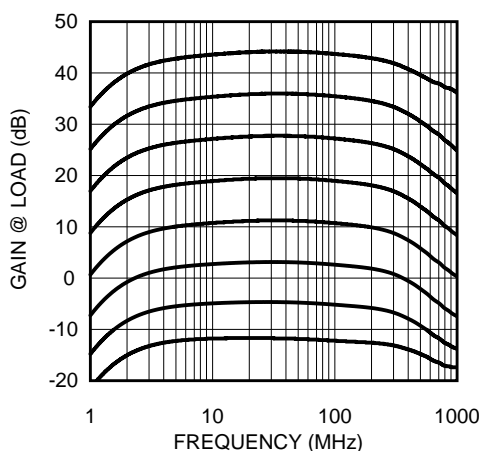


Figure 51. Frequency Response of Cascaded Amplifiers

DIGITAL CONTROL

The LMH6522 will support two modes of control, parallel mode and serial mode (SPI compatible). Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI compatible systems.

The LMH6522 has gain settings covering a range of 31 dB. To avoid undesirable signal transients the LMH6522 should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs.

The LMH6522 was designed to interface with 2.5V to 5V CMOS logic circuits. If operation with 5V logic is required care should be taken to avoid signal transients exceeding the DVGA supply voltage. Long, unterminated digital signal traces are particularly susceptible to these transients. Signal voltages on the logic pins that exceed the device power supply voltage may trigger ESD protection circuits and cause unreliable operation.

Some pins on the LMH6522 have different functions depending on the digital control mode. These functions will be described in the sections to follow.

Table 1. Pins with Dual Functions⁽¹⁾

| Pin | MODE = 0 | MODE = 1 |
|-----|----------|----------|
| 45 | A4 | SDO* |
| 46 | A3 | SDI |
| 47 | A2 | CSb |
| 48 | A1 | CLK |

(1) Pin 45 requires external bias. See Serial Mode Section for Details.

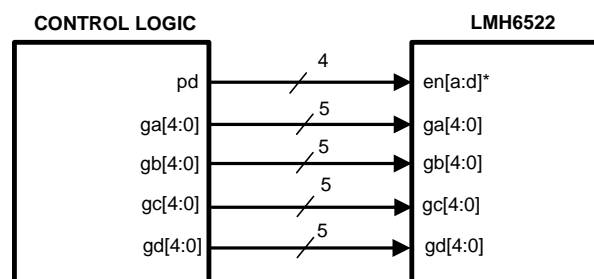
PARALLEL INTERFACE

Parallel mode offers the fastest gain update capability with the drawback of requiring the most board space dedicated to control lines. When designing a system that requires very fast gain changes parallel mode is the best selection. To place the LMH6522 into parallel mode the MODE pin (pin 5) is set to the logical zero state. Alternately the MODE pin can be connected directly to ground.

The attenuator control pins are internally biased to logic high state with weak pull up resistors. The MODE pin has a weak internal resistor to ground. The enable pins bias to a mid logic state which is the Low Power Mode.

The LMH6522 has a 5-bit gain control bus. Data from the gain control pins is immediately sent to the gain circuit (i.e. gain is changed immediately). To minimize gain change glitches all gain pins should change at the same time. In order to achieve the very fast gain step switching time the internal gain change circuit is very fast. Gain glitches could result from timing skew between the gain set bits. This is especially the case when a small gain change requires a change in state of three or more gain control pins. If necessary the DVGA could be put into a disabled state while the gain pins are reconfigured and then brought active when they have settled.

ENA, ENB, ENC and END pins are provided to reduce power consumption by disabling the highest power portions of the LMH6522. The gain register will preserve the last active gain setting during the disabled state. These pins have three logic states and will float to the middle or low power, enabled state if left floating. When grounded the EN pins will disable the associated channel and when biased to the highest logic level the associated channel will be in the high power, enabled state. See the [Typical Performance Characteristics](#) section for disable and enable timing information.



*Enable pins are tri state buffer compatible.

Figure 52. Parallel Mode Connection

SPI™ COMPATIBLE SERIAL INTERFACE

Serial interface allows a great deal of flexibility in gain programming and reduced board complexity. Using only 4 wires for both channels allows for significant board space savings. The trade off for this reduced board complexity is slower response time in gain state changes. For systems where gain is changed only infrequently or where only slow gain changes are required serial mode is the best choice. To place the LMH6522 into serial mode the MODE pin (Pin 5) should be put into the logic high state. Alternatively the MODE pin can be connected directly to the 5V supply bus.

The LMH6522 serial interface is a generic 4-wire synchronous interface that is compatible with SPI type interfaces that are used on many microcontrollers and DSP controllers. In this configuration the pins function as shown in the pin description table. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out (SDO), and serial chip select (CSb). The chip select pin is active low.

The enable pins are inactive in the serial mode. These pins can be left disconnected for serial mode.

The CLK pin is the serial clock pin. It is used to register the input data that is presented on the SDI pin on the rising edge; and to source the output data on the SDO pin on the falling edge. User may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled.

The CSb pin is the chip select pin. The b indicates that this pin is actually a “NOT chip select” since the chip is selected in the logic low state. Each assertion starts a new register access - i.e., the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the CSb pin is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted-in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the deasserted pulse - which is specified in the [Electrical Specifications](#) section.

The SDI pin is the input pin for the serial data. It must observe setup / hold requirements with respect to the SCLK. Each cycle is 16-bits long

The SDO pin is the data output pin. This output is normally at a high impedance state, and is driven only when CSb is asserted. Upon CSb assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. Upon power-up, the default register address is 00h. The SDO pin requires external bias for clock speeds over 1MHz. See [Figure 54](#) for details on sizing the external bias resistor. Because the SDO pin is a high impedance pin, the board capacitance present at the pin will restrict data out speed that can be achieved. For a RC limited circuit the frequency is $\sim 1 / (2 \cdot \pi \cdot RC)$. As shown in the figure resistor values of 300 to 2000 Ohms are recommended.

Each serial interface access cycle is exactly 16 bits long as shown in [Figure 53](#). Each signal's function is described below. the read timing is shown in [Figure 55](#), while the write timing is shown in [Figure 56](#).

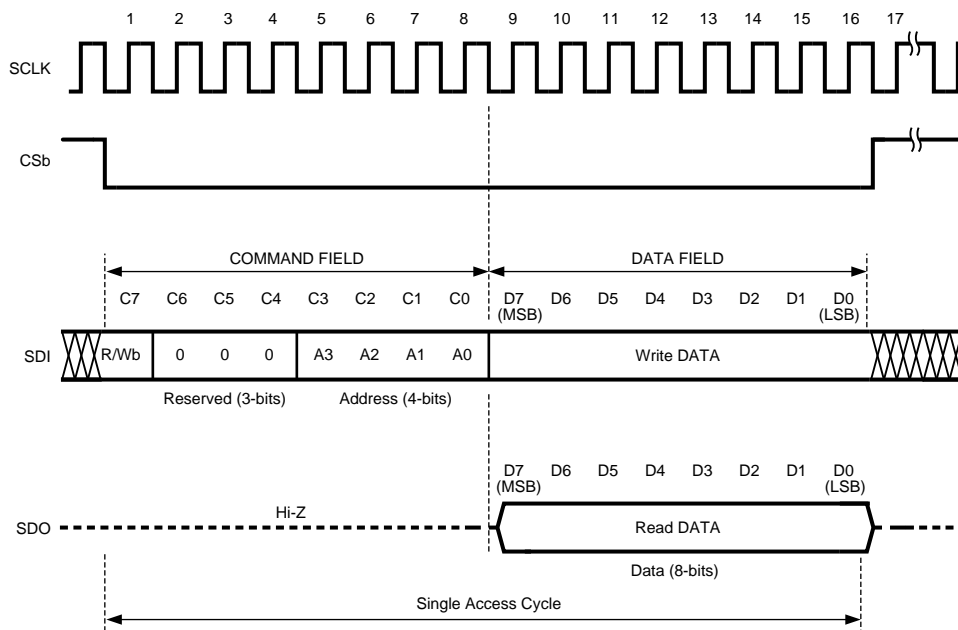


Figure 53. Serial Interface Protocol (SPI compatible)

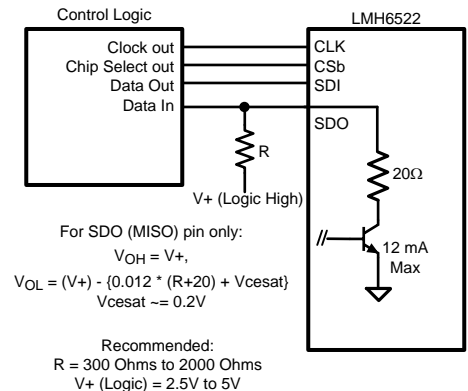


Figure 54. Internal Operation of the SDO pin

| | |
|----------|---|
| R/Wb | Read / Write bit. A value of 1 indicates a read operation, while a value of 0 indicates a write operation. |
| Reserved | Not used. Must be set to 0. |
| ADDR: | Address of register to be read or written. |
| DATA | In a write operation the value of this field will be written to the addressed register when the chip select pin is deasserted. In a read operation this field is ignored. |

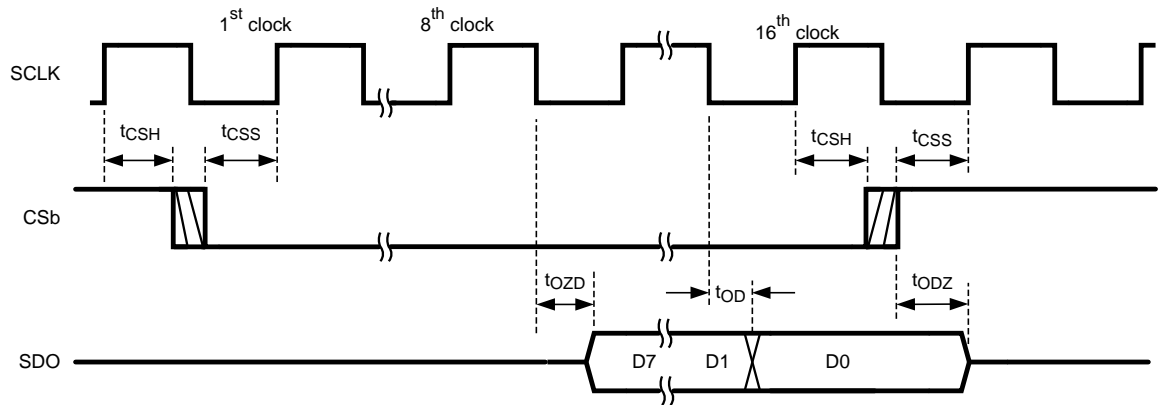
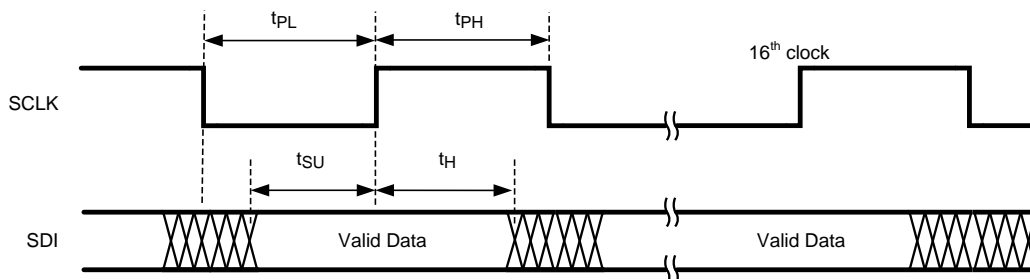


Figure 55. Read Timing

Table 2. Read Timing
Data Output on SDO Pin

| Parameter | Description |
|------------------|---------------------------|
| t _{CSH} | Chip select hold time |
| t _{CSS} | Chip select setup time |
| t _{ODZ} | Initial output data delay |
| t _{ODZ} | High impedance delay |
| t _{OD} | Output data delay |



**Figure 56. Write Timing
Data Written to SDI Pin**

**Table 3. Write Timing
Data Input on SDI Pin**

| Parameter | Description |
|-----------|--|
| t_{PL} | Minimum clock low time (clock duty cycle) |
| t_{PH} | Minimum clock high time (clock duty cycle) |
| t_{SU} | Input data setup time |
| t_H | Input data hold time |

Table 4. Serial Word Format for LMH6522

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|--------------------|----|----|----|----|--|----|----|
| 1= read 0=write | 0 | 0 | 0 | 0 | 000= CHA 001=CHB 010=CHC 011=CHD 100=Fast Adjust | | |

Table 5. CH A through D Register Definition

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----------------------------------|-----------------------------|---|---|---|---|---|
| Reserved, =0 | Power Level: 0= Low 1=High | Enable: 0 = OFF 1= ON | Attenuation Setting: 00000 = Maximum Gain 11111 = Minimum Gain | | | | |

Table 6. Fast Adjust Register Definition

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|------|---|------|---|------|---|
| CH D | | CH C | | CH B | | CH A | |

Table 7. Fast Adjust Codes

| Code | Action |
|------|--------------------------------------|
| 00 | No Change |
| 01 | Decrease Attenuation by 1 Step (1dB) |
| 10 | Increase Attenuation by 1 Step (1dB) |
| 11 | Reserved, action undefined |

SPISU2 SPI CONTROL BOARD AND TINYI2CSPI SOFTWARE

Also available separately from the LMH6522EVAL evaluation board is a USB to SPI control board and supporting software. The SPISU2 board will connect directly to the LMH6522 evaluation board and provides a simple way to test and evaluate the SPI interface. For more details refer to the LMH6522EVAL user's guide. The evaluation board user's guide provides instructions on connecting the SPISU2 board and for configuring the TinyI2CSPI software.

THERMAL MANAGEMENT

The LMH6522 is packaged in a thermally enhanced package. The exposed pad is connected to the GND pins. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of this pad to the system printed circuit board (PCB). The exposed pad should be attached to as much copper on the PCB as possible, preferably external copper. However, it is also very important to maintain good high speed layout practices when designing a system board. Please refer to the LMH6522 evaluation board for suggested layout techniques.

The LMH6522EVAL evaluation board was designed for both signal integrity and thermal dissipation. The LMH6522EVAL has eight layers of copper. The inner copper layers are two ounce copper and are as solid as design constraints allow. The exterior copper layers are one ounce copper in order to allow fine geometry etching. The benefit of this board design is significant. The JEDEC standard 4 layer test board gives a θ_{JA} of 23°C/W. The LMH6522EVAL eight layer board gives a measured θ_{JA} of 15°C/W (ambient temperature 25°C, no forced air). With the typical power dissipation of 2.3W this is a temperature difference of 18 degrees in junction temperature between the standard 4 layer board and the enhanced 8 layer evaluation board. In a system design the location and power dissipation of other heat sources may change the results observed compared with the LMH6522EVAL board.

Applying a heat sink to the package will also help to remove heat from the device. The ATS-54150K-C2-R0 heat sink, manufactured by Advanced Thermal Solutions, provided good results in lab testing. Using both a heat sink and a good board thermal design will provide the best cooling results. If a heat sink will not fit in the system design, the external case can be used as a heat sink.

Package information is available on the TI web site.

<http://www.ti.com/packaging>

INTERFACING TO AN ADC

The LMH6522 was designed to be used with high speed ADCs such as the ADC16DV160. As shown in the Typical Application on page 1, AC coupling provides the best flexibility especially for IF sub-sampling applications.

The inputs of the LMH6522 will self bias to the optimum voltage for normal operation. The internal bias voltage for the inputs is approximately mid rail which is 2.5V with the typical 5V power supply condition. In most applications the LMH6522 input will need to be AC coupled.

The output pins require a DC path to ground that will carry the ~36 mA of bias current required to power the output transistors. The output common mode voltage should be established very near to ground. This means that using RF chokes or RF inductors is the easiest way to bias the LMH6522 output pins. Inductor values of 1μH to 400nH are recommended. High Q inductors will provide the best performance. If low frequency operation is desired, particular care must be given to the inductor selection because inductors that offer good performance at very low frequencies often have very low self resonant frequencies. If very broadband operation is desired the use of conical inductors such as the BCL-802JL from Coilcraft may be considered. These inductors offer very broadband response, at the expense of large physical size and a high DC resistance of 3.4 Ohms.

ADC Noise Filter

Below are schematics and a table of values for second order Butterworth response filters for some common IF frequencies. These filters, shown in [Figure 57](#), offer a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as is used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology works best with the 12, 14 and 16 bit analog to digital converters shown in [Table 8](#).

Table 8. Filter Component Values

| Center Frequency | 75 MHz | 150 MHz | 180 MHz | 250 MHz |
|------------------|--------|---------|---------|---------|
| Bandwidth | 40 MHz | 60 MHz | 75 MHz | 100 MHz |
| R1, R2 | 90Ω | 90Ω | 90Ω | 90Ω |
| L1, L2 | 390 nH | 370 nH | 300 nH | 225 nH |
| C1, C2 | 10 pF | 3 pF | 2.7 pF | 1.9 pF |
| C3 | 22 pF | 19 pF | 15 pF | 11 pF |
| L5 | 220 nH | 62 nH | 54 nH | 36 nH |

Table 8. Filter Component Values (continued)

| | | | | |
|--------|------|------|------|------|
| R3, R4 | 100Ω | 100Ω | 100Ω | 100Ω |
|--------|------|------|------|------|

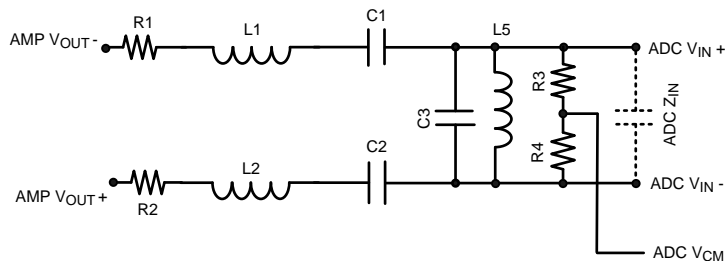


Figure 57. Sample Filter

POWER SUPPLIES

The LMH6522 was designed primarily to be operated on 5V power supplies. The voltage range for V+ is 4.75V to 5.25V. Power supply accuracy of 2.5% or better is advised. When operated on a board with high speed digital signals it is important to provide isolation between digital signal noise and the LMH6522 inputs. The SP16160CH1RB reference board provides an example of good board layout.

DYNAMIC POWER MANAGEMENT, USING LOW POWER MODE

The LMH6522 offers the option of a reduced power mode of operation referred to as Low Power Mode. In this mode of operation power consumption is reduced by approximately 20%. In many applications the linearity of the LMH6522 is fully adequate for most signal conditions. This would apply for a radio in a noise limited environment with no close-in blocker signals. During these conditions the LMH6522 can be operated in the low power mode. When a blocking signal is detected, or when system dynamic range needs to be increased, the LMH6522 can be rapidly switched from the Low Power Mode to the standard, High Power Mode.

The output response shown in Figure 58 is for a 2 MHz switching frequency pulse applied to the enable pin with a 50 MHz input signal. Analysis with a spectrum analyzer showed that the power mode switching spurs created by the switching signal were -80dBc with respect to the 50 MHz tone signal. This shows that rapid switching of power modes has virtually no impact on the signal quality.

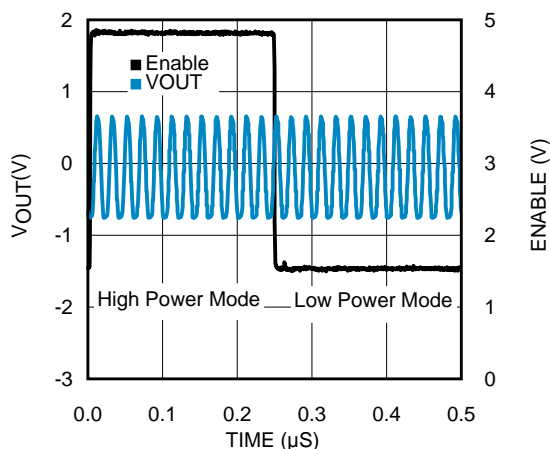


Figure 58. Signal Output During Mode Change from High Power Mode to Low Power Mode

COMPATIBLE HIGH SPEED ANALOG TO DIGITAL CONVERTERS

| Product Number | Max Sampling Rate (MSPS) | Resolution | Channels |
|----------------|--------------------------|------------|----------|
| ADC12L063 | 62 | 12 | SINGLE |
| ADC12DL065 | 65 | 12 | DUAL |
| ADC12L066 | 66 | 12 | SINGLE |
| ADC12DL066 | 66 | 12 | DUAL |
| CLC5957 | 70 | 12 | SINGLE |
| ADC12L080 | 80 | 12 | SINGLE |
| ADC12DL080 | 80 | 12 | DUAL |
| ADC12C080 | 80 | 12 | SINGLE |
| ADC12C105 | 105 | 12 | SINGLE |
| ADC12C170 | 170 | 12 | SINGLE |
| ADC12V170 | 170 | 12 | SINGLE |
| ADC14C080 | 80 | 14 | SINGLE |
| ADC14C105 | 105 | 14 | SINGLE |
| ADC14DS105 | 105 | 14 | DUAL |
| ADC14I55 | 155 | 14 | SINGLE |
| ADC14V155 | 155 | 14 | SINGLE |
| ADC16V130 | 130 | 16 | SINGLE |
| ADC16DV160 | 160 | 16 | DUAL |
| ADC08D500 | 500 | 8 | DUAL |
| ADC08500 | 500 | 8 | SINGLE |
| ADC08D1000 | 1000 | 8 | DUAL |
| ADC081000 | 1000 | 8 | SINGLE |
| ADC08D1500 | 1500 | 8 | DUAL |
| ADC081500 | 1500 | 8 | SINGLE |
| ADC08(B)3000 | 3000 | 8 | SINGLE |
| ADC08L060 | 60 | 8 | SINGLE |
| ADC08060 | 60 | 8 | SINGLE |
| ADC10DL065 | 65 | 10 | DUAL |
| ADC10065 | 65 | 10 | SINGLE |
| ADC10080 | 80 | 10 | SINGLE |
| ADC08100 | 100 | 8 | SINGLE |
| ADCS9888 | 170 | 8 | SINGLE |
| ADC08(B)200 | 200 | 8 | SINGLE |
| ADC11C125 | 125 | 11 | SINGLE |
| ADC11C170 | 170 | 11 | SINGLE |

REVISION HISTORY

| Changes from Revision C (March 2013) to Revision D | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 25 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LMH6522SQ/NOPB | ACTIVE | WQFN | NJY | 54 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | L6522 | Samples |
| LMH6522SQE/NOPB | ACTIVE | WQFN | NJY | 54 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 85 | L6522 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH6522SQ/NOPB | WQFN | NJY | 54 | 2000 | 330.0 | 16.4 | 5.8 | 10.3 | 1.0 | 12.0 | 16.0 | Q1 |
| LMH6522SQE/NOPB | WQFN | NJY | 54 | 250 | 178.0 | 16.4 | 5.8 | 10.3 | 1.0 | 12.0 | 16.0 | Q1 |

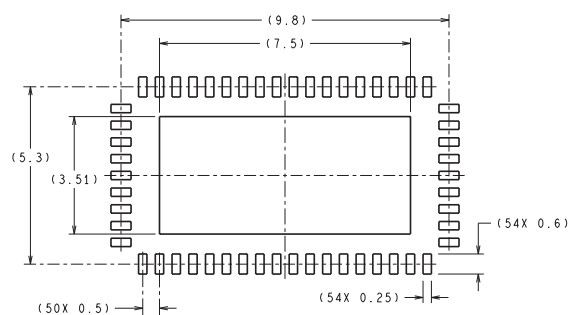
TAPE AND REEL BOX DIMENSIONS



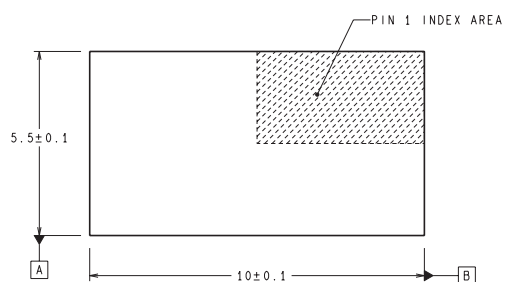
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH6522SQ/NOPB | WQFN | NJY | 54 | 2000 | 367.0 | 367.0 | 38.0 |
| LMH6522SQE/NOPB | WQFN | NJY | 54 | 250 | 213.0 | 191.0 | 55.0 |

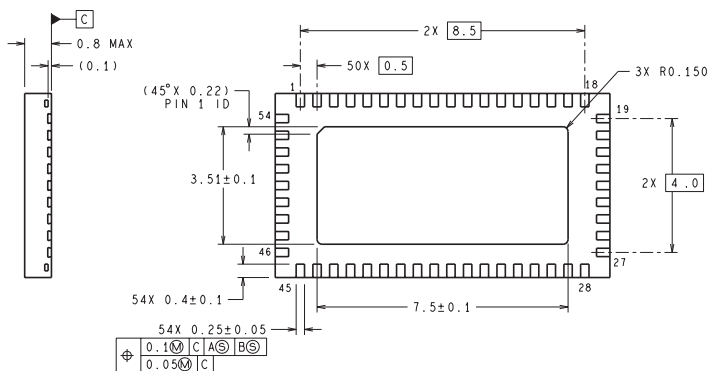
NJY0054A



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SQA54A (Rev B)

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