Tiny 7A MOSFET Gate Driver

Check for Samples: SM74101

FEATURES

- Renewable Energy Grade
- Compound CMOS and Bipolar Outputs Reduce Output Current Variation
- 7A sink/3A Source Current
- Fast Propagation Times (25 ns Typical)
- Fast Rise and Fall Times (14 ns/12 ns Rise/Fall with 2 nF Load)
- Inverting and Non-Inverting Inputs Provide Either Configuration with a Single Device
- Supply Rail Under-Voltage Lockout Protection
- Dedicated Input Ground (IN_REF) for Split Supply or Single Supply Operation
- Power Enhanced 6-Pin WSON Package (3.0mm x 3.0mm)
- Output Swings from V_{CC} to V_{EE} which can be Negative Relative to Input Ground

DESCRIPTION

The SM74101 MOSFET gate driver provides high peak gate drive current in the tiny WSON-6 package (SOT23 equivalent footprint), with improved power dissipation required for high frequency operation. The compound output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 7A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is provided to prevent damage to the MOSFET due to insufficient gate turn-on voltage. The SM74101 provides both inverting and non-inverting inputs to satisfy requirements for inverting and non-inverting gate drive with a single device type.

BLOCK DIAGRAM

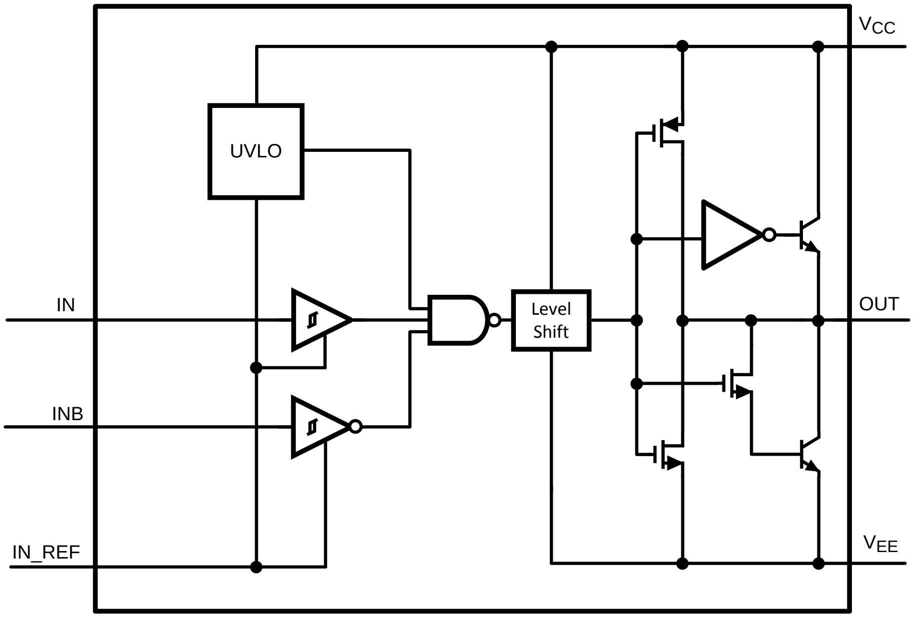


Figure 1. Block Diagram of SM74101

Pin Configurations

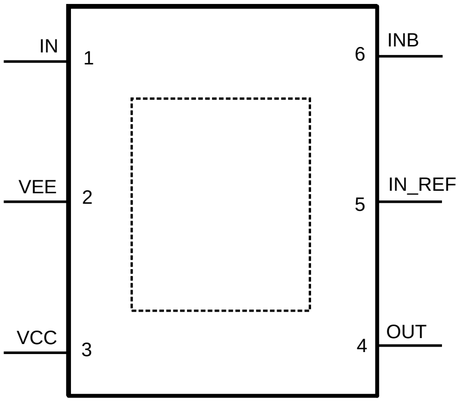


Figure 2. WSON-6
Package Number NGG0006A

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	IN	Non-inverting input pin	TTL compatible thresholds. Pull up to VCC when not used.
2	VEE	Power ground for driver outputs	Connect to either power ground or a negative gate drive supply for positive or negative voltage swing.
3	VCC	Positive Supply voltage input	Locally decouple to VEE. The decoupling capacitor should be located close to the chip.
4	OUT	Gate drive output	Capable of sourcing 3A and sinking 7A. Voltage swing of this output is from VEE to VCC.
5	IN_REF	Ground reference for control inputs	Connect to power ground (VEE) for standard positive only output voltage swing. Connect to system logic ground when VEE is connected to a negative gate drive supply.
6	INB	Inverting input pin	TTL compatible thresholds. Connect to IN_REF when not used.
- - -	Exposed Pad	Exposed Pad, underside of package	Internally bonded to the die substrate. Connect to VEE ground pin for low thermal impedance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{CC} to V_{EE}	−0.3V to 15V
V_{CC} to IN_REF	−0.3V to 15V
IN/INB to IN_REF	−0.3V to 15V
IN_REF to V_{EE}	−0.3V to 5V
Storage Temperature Range	−55°C to +150°C
Maximum Junction Temperature	+150°C
Operating Junction Temperature	−40°C+125°C
ESD Rating	2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Electrical Characteristics

T_J = −40°C to +125°C, V_{CC} = 12V, INB = IN_REF = V_{EE} = 0V, No Load on output, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY						
V_{CC}	V_{CC} Operating Range	V_{CC} – IN_REF and V_{CC} - V_{EE}	3.5		14	V
UVLO	V_{CC} Under-voltage Lockout (rising)	V_{CC} – IN_REF	2.4	3.0	3.5	V
V_{CCH}	V_{CC} Under-voltage Hysteresis			230		mV
I_{CC}	V_{CC} Supply Current			1.0	2.0	mA
CONTROL INPUTS						
V_{IH}	Logic High		2.3			V
V_{IL}	Logic Low				0.8	V
V_{thH}	High Threshold		1.3	1.75	2.3	V
V_{thL}	Low Threshold		0.8	1.35	2.0	V
HYS	Input Hysteresis			400		mV
I_{IL}	Input Current Low	IN = INB = 0V	-1	0.1	1	µA
I_{IH}	Input Current High	IN = INB = V_{CC}	-1	0.1	1	µA
OUTPUT DRIVER						
R_{OH}	Output Resistance High	I_{OUT} = -10mA (1)		30	50	Ω
R_{OL}	Output Resistance Low	I_{OUT} = 10mA (1)		1.4	2.5	Ω
I_{SOURCE}	Peak Source Current	OUT = V_{CC}/2, 200ns pulsed current		3		A
I_{SINK}	Peak Sink Current	OUT = V_{CC}/2, 200ns pulsed current		7		A
SWITCHING CHARACTERISTICS						
td1	Propagation Delay Time Low to High, IN/ INB rising (IN to OUT)	C_{LOAD} = 2 nF, see Figure 3 and Figure 4		25	40	ns
td2	Propagation Delay Time High to Low, IN / INB falling (IN to OUT)	C_{LOAD} = 2 nF, see Figure 3 and Figure 4		25	40	ns
tr	Rise time	C_{LOAD} = 2 nF , see Figure 3 and Figure 4		14		ns
tf	Fall time	C_{LOAD} = 2 nF , see Figure 3 and Figure 4		12		ns
LATCHUP PROTECTION						
	AEC –Q100, METHOD 004	T_J = 150°C		500		mA
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient, 0 LFPM Air Flow	WSON-6 Package		40		°C/W
θ_{JC}	Junction to Case	WSON-6 Package		7.5		°C/W

(1) The output resistance specification applies to the MOS device only. The total output current capability is the sum of the MOS and Bipolar devices.

Timing Waveforms

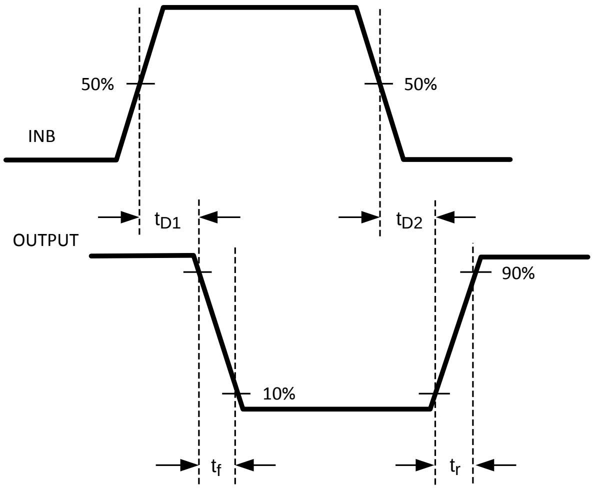


Figure 3. Inverting

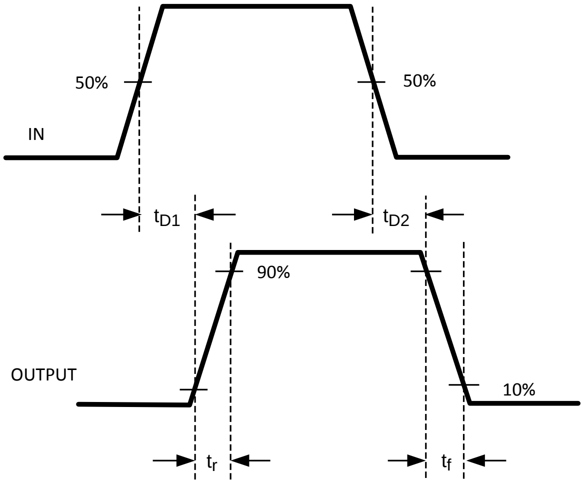
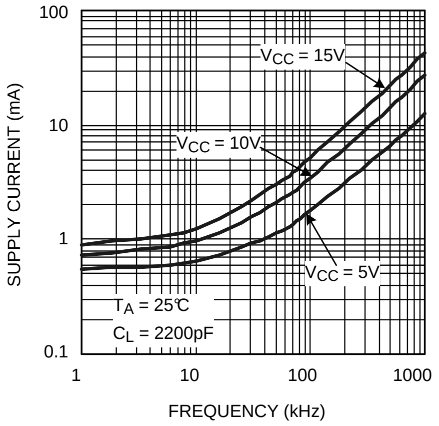


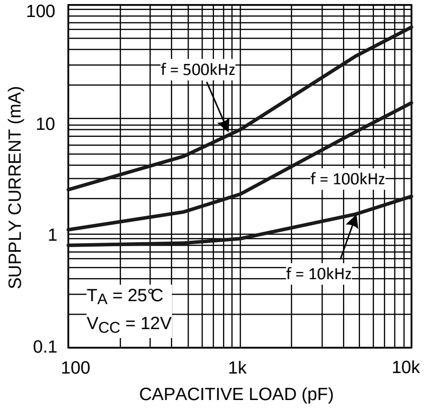
Figure 4. Non-Inverting

Typical Performance Characteristics



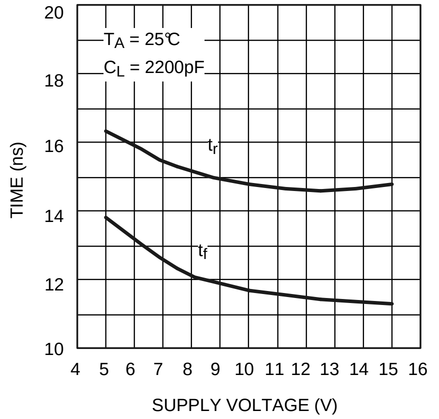
Supply Current vs Frequency

Figure 5.



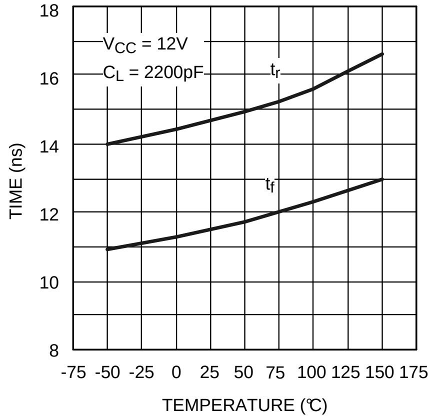
Supply Current vs Capacitive Load

Figure 6.



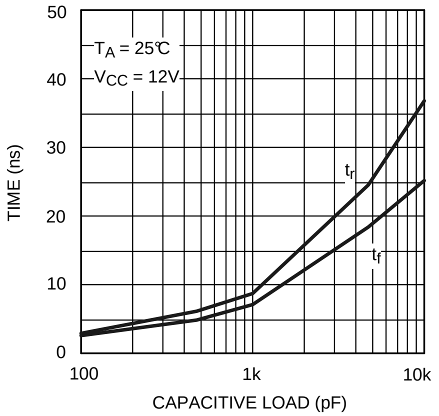
Rise and Fall Time vs Supply Voltage

Figure 7.



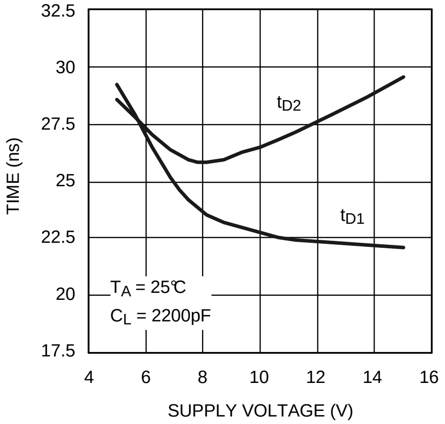
Rise and Fall Time vs Temperature

Figure 8.



Rise and Fall Time vs Capacitive Load

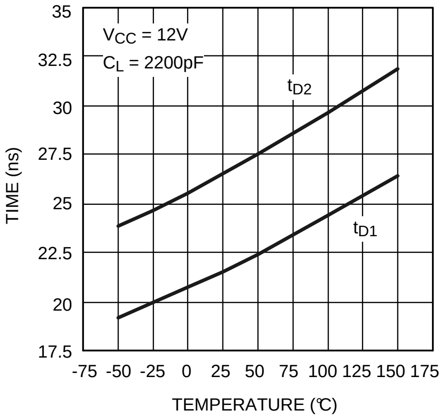
Figure 9.



Delay Time vs Supply Voltage

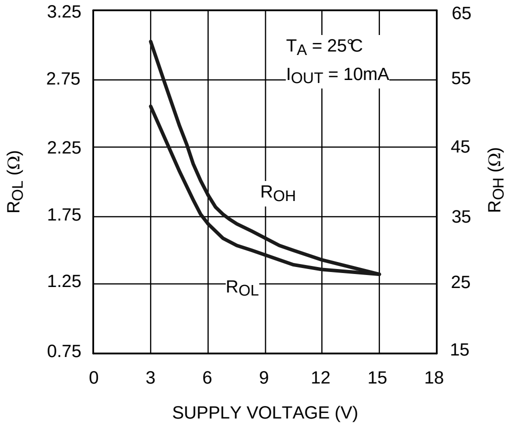
Figure 10.

Typical Performance Characteristics (continued)



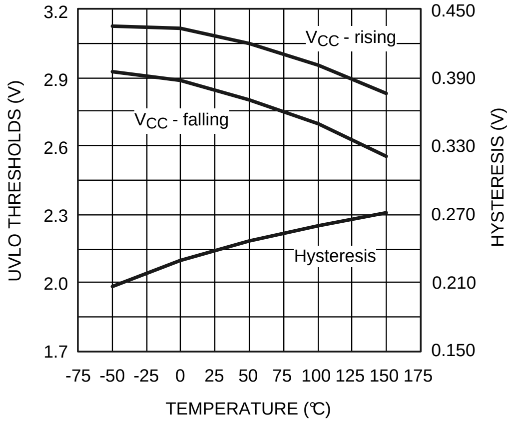
Delay Time vs Temperature

Figure 11.



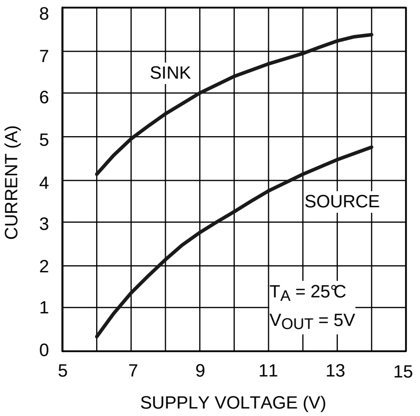
RDSON vs Supply Voltage

Figure 12.



UVLO Thresholds and Hysteresis vs Temperature

Figure 13.



Peak Current vs Supply Voltage

Figure 14.

Simplified Application Block Diagram

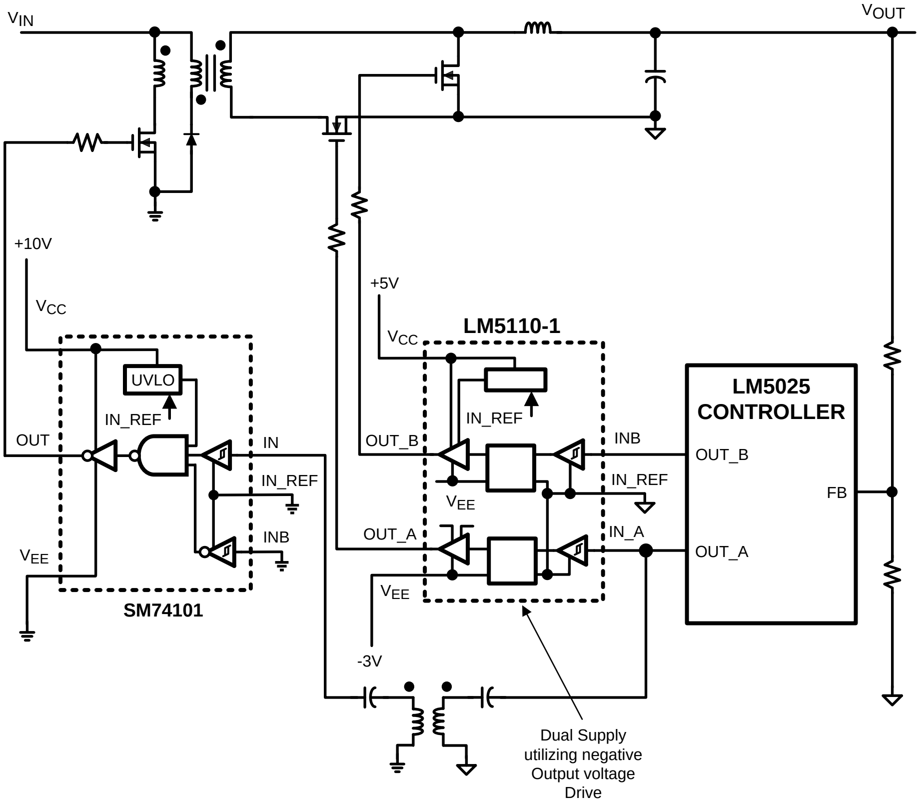


Figure 15. Simplified Application Block Diagram

DETAILED OPERATING DESCRIPTION

The SM74101 is a high speed , high peak current (7A) single channel MOSFET driver. The high peak output current of the SM74101 will switch power MOSFET's on and off with short rise and fall times, thereby reducing switching losses considerably. The SM74101 includes both inverting and non-inverting inputs that give the user flexibility to drive the MOSFET with either active low or active high logic signals. The driver output stage consists of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical Miller plateau region of the MOSFET V_{GS} , while the MOS device provides rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage V_{CC} and the power ground potential at the V_{EE} pin.

The control inputs of the driver are high impedance CMOS buffers with TTL compatible threshold voltages. The negative supply of the input buffer is connected to the input ground pin IN_REF. An internal level shifting circuit connects the logic input buffers to the totem pole output drivers. The level shift circuit and separate input/output ground pins provide the option of single supply or split supply configurations. When driving the MOSFET gates from a single positive supply, the IN_REF and V_{EE} pins are both connected to the power ground.

The isolated input and output stage grounds provide the capability to drive the MOSFET to a negative V_{GS} voltage for a more robust and reliable off state. In split supply configuration, the IN_REF pin is connected to the ground of the controller which drives the SM74101 inputs. The V_{EE} pin is connected to a negative bias supply that can range from the IN_REF potential to as low as 14 V below the Vcc gate drive supply. For reliable operation, the maximum voltage difference between V_{CC} and IN_REF or between V_{CC} and V_{EE} is 14V.

The minimum recommended operating voltage between Vcc and IN_REF is 3.5V. An Under Voltage Lock Out (UVLO) circuit is included in the SM74101 which senses the voltage difference between V_{CC} and the input ground pin, IN_REF. When the V_{CC} to IN_REF voltage difference falls below 2.8V the driver is disabled and the output pin is held in the low state. The UVLO hysteresis prevents chattering during brown-out conditions; the driver will resume normal operation when the V_{CC} to IN_REF differential voltage exceeds 3.0V.

Layout Considerations

Attention must be given to board layout when using SM74101. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the V_{CC} and V_{EE} pins to support high peak currents being drawn from V_{CC} during turn-on of the MOSFET.
2. Proper grounding is crucial. The driver needs a very low impedance path for current return to ground avoiding inductive loops. Two paths for returning current to ground are a) between SM74101 IN_REF pin and the ground of the circuit that controls the driver inputs and b) between SM74101 V_{EE} pin and the source of the power MOSFET being driven. Both paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. These ground paths should be distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the SM74101. With rise and fall times in the range of 10 to 30nsec, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated when driving large capacitive loads.
3. If either channel is not being used, the respective input pin (IN or INB) should be connected to either V_{EE} or V_{CC} to avoid spurious output signals.

Thermal Performance

INTRODUCTION

The primary goal of the thermal management is to maintain the integrated circuit (IC) junction temperature (Tj) below a specified limit to ensure reliable long term operation. The maximum T_J of IC components should be estimated in worst case operating conditions. The junction temperature can be calculated based on the power dissipated on the IC and the junction to ambient thermal resistance θ_{JA} for the IC package in the application board and environment. The θ_{JA} is not a given constant for the package and depends on the PCB design and the operating environment.

DRIVE POWER REQUIREMENT CALCULATIONS IN SM74101

SM74101 is a single low side MOSFET driver capable of sourcing / sinking 3A / 7A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.

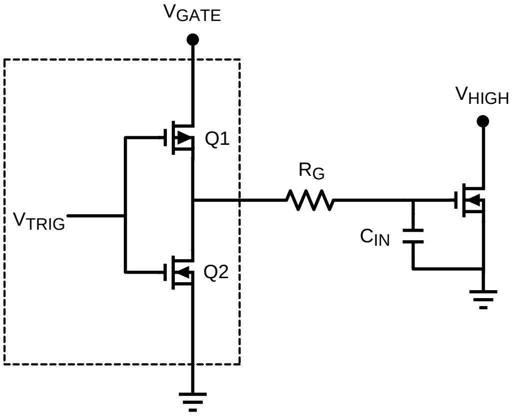


Figure 16.

The schematic above shows a conceptual diagram of the SM74101 output and MOSFET load. Q1 and Q2 are the switches within the gate driver. Rg is the gate resistance of the external MOSFET, and Cin is the equivalent gate capacitance of the MOSFET. The equivalent gate capacitance is a difficult parameter to measure as it is the combination of Cgs (gate to source capacitance) and Cgd (gate to drain capacitance). The Cgd is not a constant and varies with the drain voltage. The better way of quantifying gate capacitance is the gate charge Qg in coloumbs. Qg combines the charge required by Cgs and Cgd for a given gate drive voltage Vgate. The gate resistance Rg is usually very small and losses in it can be neglected. The total power dissipated in the MOSFET driver due to gate charge is approximated by:

$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$

Where

- F_{SW} = switching frequency of the MOSFET. (1)

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for V_{GATE} = 12V.

Therefore, the power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and V_{GATE} of 12V is equal to

P_{DRIVER} = 12V x 30 nC x 300 kHz = 0.108W. (2)

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the SM74101 changes state, current will flow from V_{CC} to V_{EE} for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the SM74101 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V V_{GATE} supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

P_D = 0.118 + 0.008 + 0.012 = 0.138W. (3)

We know that the junction temperature is given by

$T_J = P_D \times \theta_{JA} + T_A$ (4)

Or the rise in temperature is given by

$T_{RISE} = T_J - T_A = P_D \times \theta_{JA}$ (5)

For WSON-6 package, the integrated circuit die is attached to leadframe die pad which is soldered directly to the printed circuit board. This substantially decreases the junction to ambient thermal resistance (θ_{JA}). By providing suitable means of heat dispersion from the IC to the ambient through exposed copper pad, which can readily dissipate heat to the surroundings, θ_{JA} as low as 40°C / Watt is achievable with the package. The resulting Trise for the driver example above is thereby reduced to just 5.5 degrees.

Therefore T_{RISE} is equal to

T_{RISE} = 0.138 x 40 = 5.5°C (6)

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	9

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