DS0026 Dual High-Speed MOS Driver

Check for Samples: DS0026

FEATURES

- **Fast Rise and Fall Times—20 ns 1000 pF Load**
- **High Output Swing—20V**
- **High Output Current Drive—±1.5 Amps**
- **TTL Compatible Inputs**
- **High Rep Rate—5 to 10 MHz Depending on Power Dissipation**
- **Low Power Consumption in MOS "0" State—2 mW**
- **Drives to 0.4V of GND for RAM Address Drive**

DESCRIPTION

DS0026 is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. The device may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 is intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026 is designed to fulfill a wide variety of MOS interface requirements. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

Connection Diagram

Top View

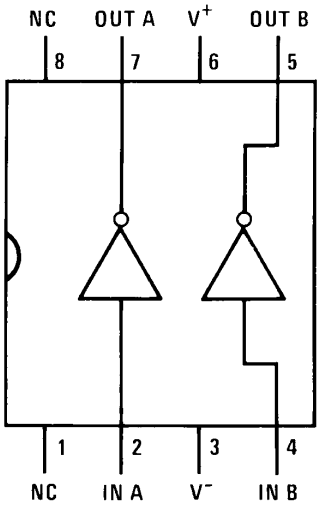


Figure 1. PDIP Package
See Package Number P0008E

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

$(V^+) - (V^-)$ Differential Voltage	22V
Input Current	100 mA
Input Voltage (V_{IN}) − (V^-)	5.5V
Peak Output Current	1.5A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be specified. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics provides conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Operating Ratings

$(V^+) - (V^-)$ Differential Voltage	10V to 20V
Maximum Power Dissipation at T_A = 25°C (1)	1168mW
P0008E θ_{JA}	107°C/W
P0008E θ_{JC}	37°C/W
D0008A θ_{JA}	180°C/W
DGK0008A θ_{JA}	220°C/W
Operating Temperature Range, T_A	0°C to +70°C

(1) Derate P0008E package 9.3 mW/°C for T_A above 25°C.

Electrical Characteristics (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage	V^- = 0V	2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^-$ = 2.4V		10	15	mA
V_{IL}	Logic "0" Input Voltage	V^- = 0V		0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^-$ = 0V		−3	−10	µA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^-$ = 2.4V, I_{OL} = 1 mA		V^-+0.7	V^-+1.0	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^-$ = 0.4V, $V_{SS} \geq V^+ + 1.0V$ I_{OH} = − 1 mA	$V^+ - 1.0$	V^+−0.8		V
$I_{CC(ON)}$	"ON" Supply Current (one side on)	$V^+ - V^-$ = 20V, $V_{IN} - V^-$ = 2.4V		30	40	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^-$ = 20V, $V_{IN} - V^-$ = 0V		10	100	µA

(1) These specifications apply for $V^+ - V^-$ = 10V to 20V, C_L = 1000 pF, over the temperature range of 0°C to +70°C for the DS0026CN.
(2) All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
(3) All typical values for T_A = 25°C.

Switching Characteristics

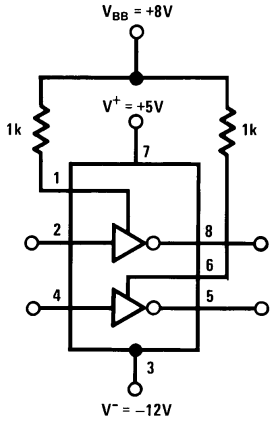
(T_A = 25°C) (1) (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{ON}	Turn-On Delay	(Figure 11)		5	7.5	12	ns
		(Figure 12)			11		ns
t_{OFF}	Turn-Off Delay	(Figure 11)			12	15	ns
		(Figure 12)			13		ns
t_r	Rise Time	(Figure 11) (1)	C_L = 500 pF		15	18	ns
			C_L = 1000 pF		20	35	ns
		(Figure 12) (1)	C_L = 500 pF		30	40	ns
			C_L = 1000 pF		36	50	ns
t_f	Fall Time	(Figure 11) (1)	C_L = 500 pF		12	16	ns
			C_L = 1000 pF		17	25	ns
		(Figure 12) (1)	C_L = 500 pF		28	35	ns
			C_L = 1000 pF		31	40	ns

(1) Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic “0” to logic “1” which is voltage fall.

(2) The high current transient (as high as 1.5A) through the resistance of the internal interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

Figure 2. Typical V_{BB} Connection



Typical Performance Characteristics

Input Current vs Input Voltage

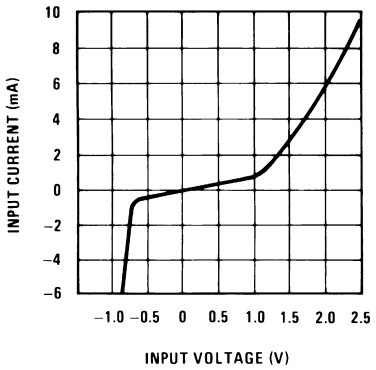


Figure 3.

Supply Current vs Temperature

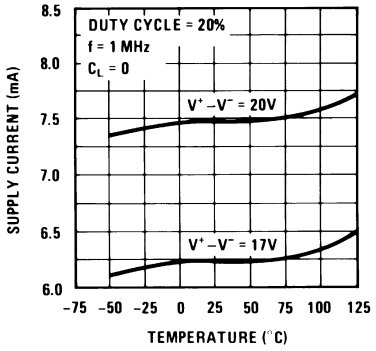


Figure 4.

Turn-On and Turn-Off Delay vs Temperature

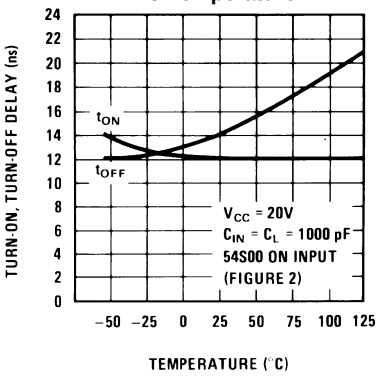


Figure 5.

Rise Time vs Load Capacitance

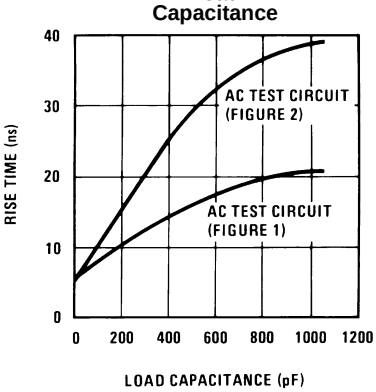


Figure 6.

Fall Time vs Load Capacitance

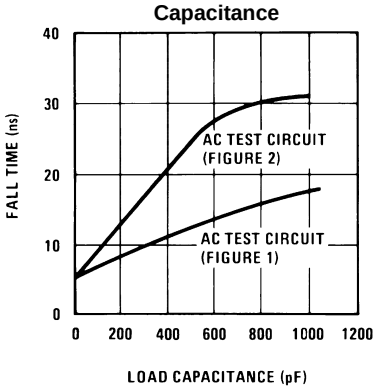


Figure 7.

Recommended Input Coding Capacitance

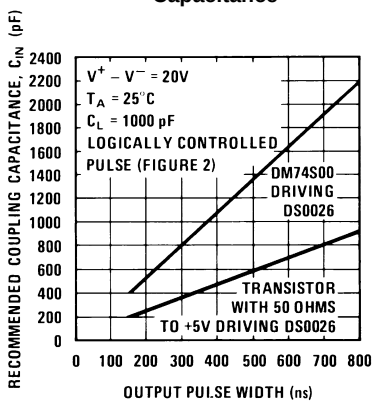


Figure 8.

Typical Performance Characteristics (continued)

DC Power (P_{DC}) vs Duty Cycle

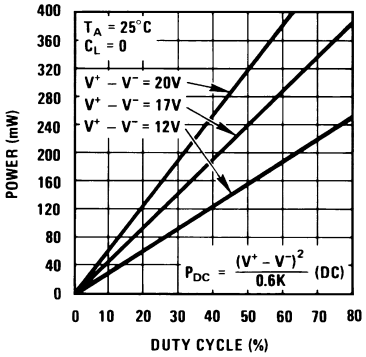


Figure 9.

Schematic Diagram

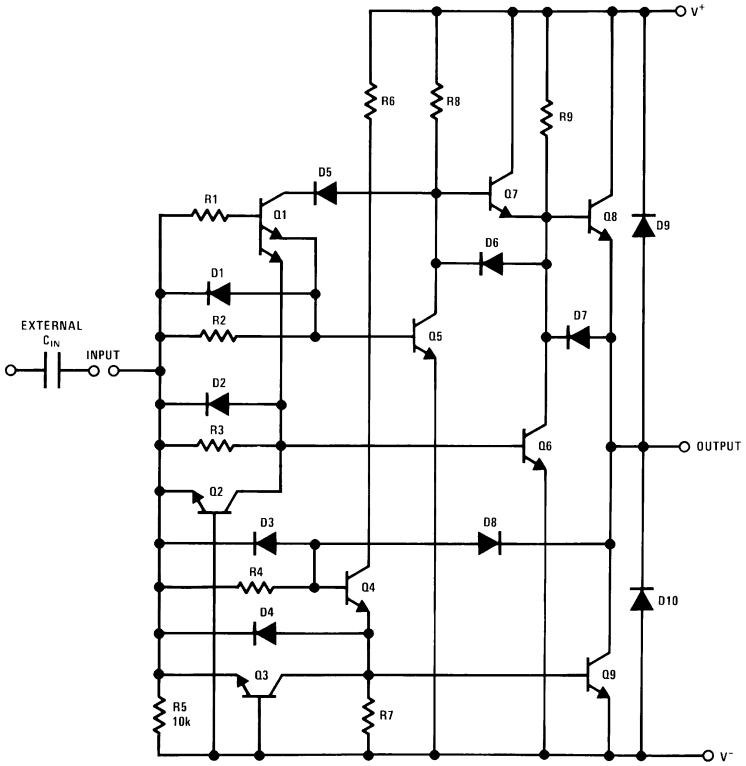


Figure 10. 1/2 DS0026

AC Test Circuits and Switching Time Waveforms

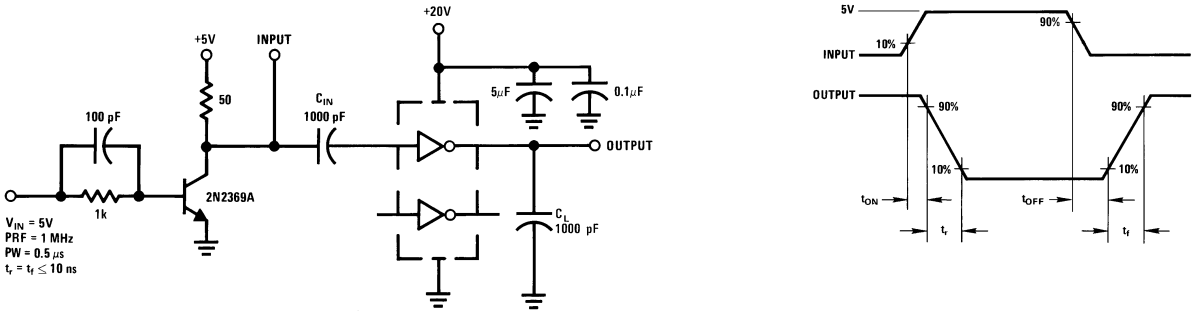


Figure 11.

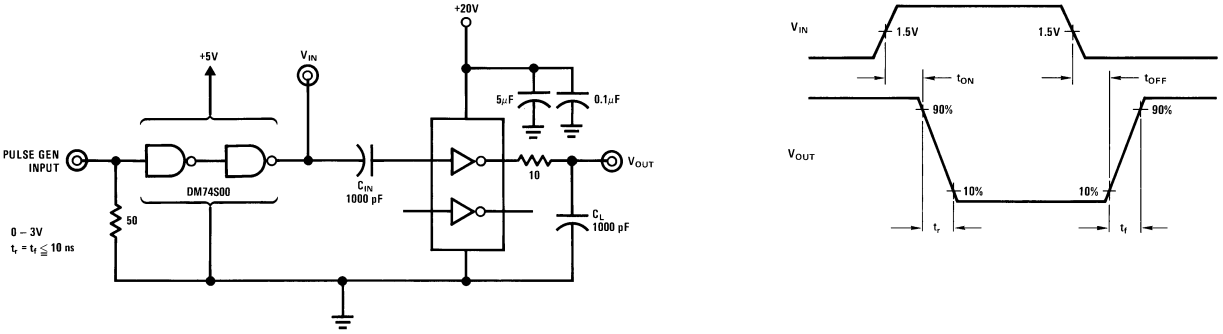


Figure 12.

Typical Applications

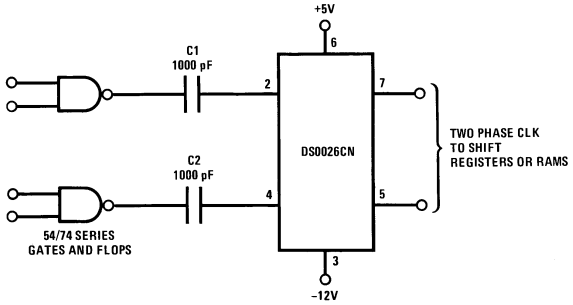


Figure 13. AC Coupled MOS Clock Driver

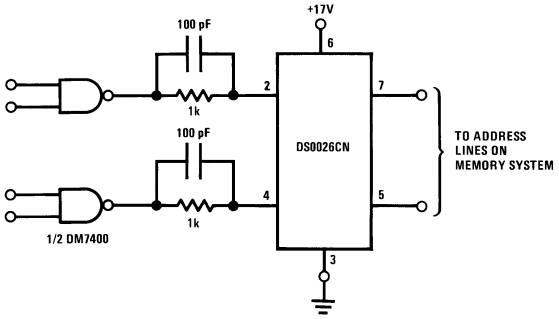


Figure 14. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

APPLICATION HINTS

DRIVING THE MM5262 WITH THE DS0026 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. Figure 15 shows the clock specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the V_{SS} − 1 V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to Figure 11, if the threshold voltage of a transistor were −1.3V, the clock going to V_{SS} − 1 would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

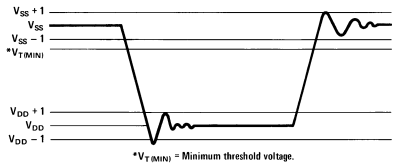


Figure 15. Clock Waveform

Controlling the clock ringing is particularly difficult because of the relative magnitude of the allowable ringing, compared to magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10Ω to 20Ω is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

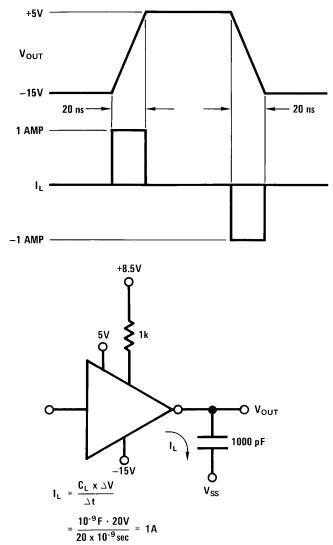


Figure 16. Clock Waveforms (Voltage and Current)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. Figure 16 gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies. A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0026 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since the noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. Figure 17 shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock transient from the 7404 because of the inductance, L.

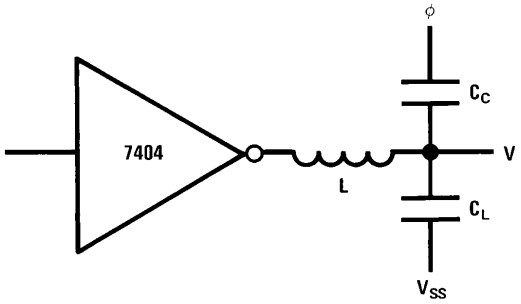


Figure 17. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56 + 1}\right) = 0.35V \quad (1)$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the “1” state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA \tag{2}$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the φ2 clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from φ1 clock.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

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