

DS3893A BTL TURBOTRANSCEIVER

Check for Samples: [DS3893A](#)

FEATURES

- **Fast Single Ended Transceiver (Typical Driver Enable and Receiver Propagation Delays are 3.5 ns and 5 ns)**
- **Backplane Transceiver Logic (BTL) Levels (1V logic swing)**
- **Less than 5 pF Bus-Port Capacitance**
- **Drives Densely Loaded Backplanes with Equivalent Load Impedances Down to 10Ω**
- **Specially Designed for Stripline Backplanes**
- **Separate Bus Ground Returns for Each Driver to Minimize Ground Noise**
- **High Impedance, MOS and TTL Compatible Inputs**
- **TRI-STATE Control for Receiver Outputs**
- **Built-in Bandgap Reference Provides Accurate Receiver Threshold**
- **Glitch Free Power Up/Down Protection on all Outputs**
- **Oxide Isolated Bipolar Technology**

DESCRIPTION

The TURBOTRANSCEIVER is designed for use in very high speed bus systems. The bus terminal characteristics of the TURBOTRANSCEIVER are referred to as "Backplane Transceiver Logic" (BTL). BTL is a new logic signaling standard that has been developed to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard eliminates the settling time delays, that severely limit the TTL bus performance, to provide significantly higher bus transfer rates.

The TURBOTRANSCEIVER is compatible with the requirements of the proposed IEEE 896 Futurebus draft standard. It is similar to the DS3896/97 BTL TRAPEZOIDAL Transceivers but the trapezoidal feature has been removed to improve the propagation delay. A stripline backplane is therefore required to reduce the crosstalk induced by the faster rise and fall times. This device can drive a 10Ω load with a typical propagation delay of 3.5 ns for the driver and 5 ns for the receiver.

When multiple devices are used to drive a parallel bus, the driver enables can be tied together and used as a common control line to get on and off the bus. The driver enable delay is designed to be the same as the driver propagation delay in order to provide maximum speed in this configuration. The low input current on the enable pin eases the drive required for the common control line.

The bus driver is an open collector NPN with a Schottky diode in series to isolate the transistor output capacitance from the bus when the driver is in the inactive state. The active output low voltage is typically 1V. The bus is intended to be operated with termination resistors (selected to match the bus impedance) to 2.1V at both ends. Each of the resistors can be as low as 20Ω.



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Connection and Logic Diagram

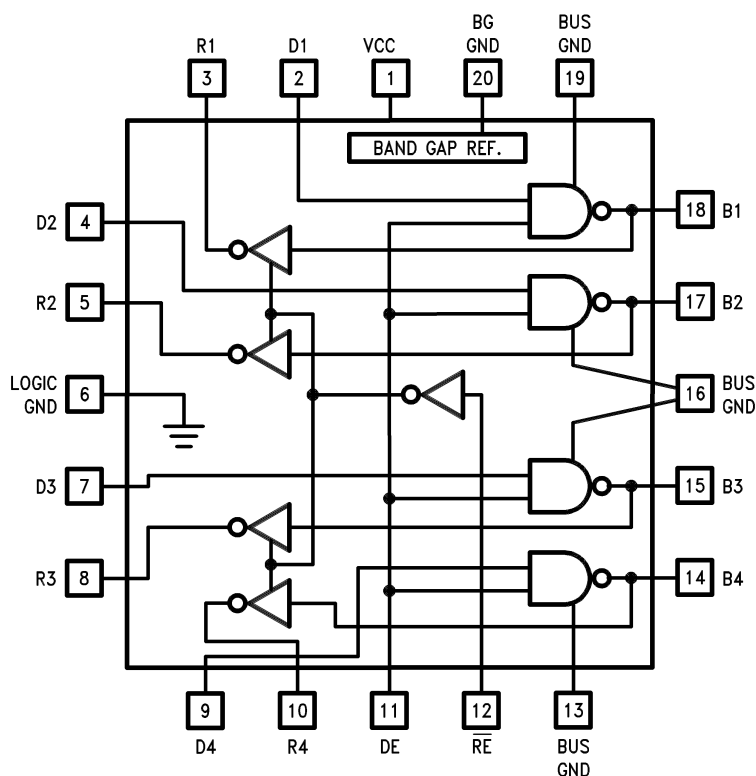


Figure 1. See Package Number FN0020A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage	6.5V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Driver Output Receiver Input Clamp Current	±15 mA
Power Dissipation at 70°C	900 mW
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 3 sec.)	260°C

- (1) "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.0	2.2	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

 $T_A = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (DE, $\overline{\text{RE}}$, Dn)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_I	Input Leakage Current	$\text{DE} = \overline{\text{RE}} = \text{Dn} = V_{CC}$			100	μA
I_{IH}	Input High Current	$\text{DE} = \overline{\text{RE}} = \text{Dn} = 2.5\text{V}$			20	μA
I_{IL}	Dn Input Low Current	$\text{Dn} = 0.5\text{V}$, $\text{DE} = V_{CC} = \text{Max}$			-200	μA
	DE Input Low Current	$\text{DE} = 0.5\text{V}$, $\text{Dn} = V_{CC} = \text{Max}$			-500	μA
	$\overline{\text{RE}}$ Input Low Current	$\overline{\text{RE}} = 0.5\text{V}$, $V_{CC} = \text{Max}$			-100	μA
V_{CL}	Input Diode Clamp Voltage	$I_{\text{clamp}} = -12 \text{ mA}$			-1.2	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage	$\text{Dn} = \text{DE} = V_{IH}$ (Figure 3) $R_T = 10\Omega$, $V_T = 2.2\text{V}$	0.75	1.0	1.2	V
		$\text{Dn} = \text{DE} = V_{IH}$ (Figure 3) $R_T = 18.5\Omega$, $V_T = 2.14$	0.75	1.0	1.1	V
I_{ILB}	Output Bus Current (Power On)	$\text{Dn} = \text{DE} = 0.8\text{V}$, $V_{CC} = \text{Max}$ $\text{Bn} = 0.75\text{V}$	-250		100	μA
I_{IHB}	Output Bus Current (Power Off)	$\text{Dn} = \text{DE} = 0.8\text{V}$, $V_{CC} = 0\text{V}$ $\text{Bn} = 1.2\text{V}$			100	μA
V_{OCB}	Driver Output Positive Clamp	$V_{CC} = \text{Max}$ or 0V , $\text{Bn} = 1 \text{ mA}$ $V_{CC} = \text{Max}$ or 0V , $\text{Bn} = 10 \text{ mA}$			2.9 3.2	V
V_{OHB}	Output High Bus Voltage	$V_{CC} = \text{Max}$, $\text{Dn} = 0.8\text{V}$ (Figure 3) $V_T = 2.0\text{V}$, $R_T = 10\Omega$	1.90			V
V_{TH}	Receiver Input Threshold		1.47	1.55	1.62	V
RECEIVER OUTPUT: (Rn)						
V_{OH}	Voltage Output High	$\text{Bn} = 1.2\text{V}$, $I_{oh} = -3 \text{ mA}$, $\overline{\text{RE}} = 0.8\text{V}$	2.5V			V
V_{OL}	Voltage Output Low	$\text{Bn} = 2\text{V}$, $I_{ol} = 6 \text{ mA}$, $\overline{\text{RE}} = 0.8\text{V}$		0.35	0.5	V
I_{OZ}	TRI-STATE Leakage	$V_o = 2.5\text{V}$, $\overline{\text{RE}} = 2\text{V}$ $V_o = 0.5\text{V}$, $\overline{\text{RE}} = 2\text{V}$			20 -20	μA
I_{OS}	Output Short Circuit Current	$\text{Bn} = 1.2\text{V}$, $V_o = 0\text{V}$ $\overline{\text{RE}} = 0.8\text{V}$, $V_{CC} = \text{Max}$	-80	-120	-200	mA
I_{CC}	Supply Current	$\text{Dn} = \text{DE} = \overline{\text{RE}} = V_{IH}$, $V_{CC} = \text{Max}$		70	95	mA

- (1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- (2) All typicals are given for $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
- (3) Unused inputs should not be left floating. Tie unused inputs to either V_{CC} or GND thru a resistor.
- (4) Only one output at a time should be shorted.

Switching Characteristics

 $T_A = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER: (Figure 4 and Figure 7)						
t_{PHL}	Driver Input to Output	$V_T = 2\text{V}$, $R_T = 10\Omega$, $C_L = 30 \text{ pF}$, $\text{DE} = 3\text{V}$	1	3.5	7	ns
t_{PLH}	Driver Input to Output	$V_T = 2\text{V}$, $R_T = 10\Omega$, $C_L = 30 \text{ pF}$, $\text{DE} = 3\text{V}$	1	3.5	7	ns
t_r	Output Rise time	$V_T = 2\text{V}$, $R_T = 10\Omega$, $C_L = 30 \text{ pF}$, $\text{DE} = 3\text{V}$	1	2	5	ns
t_f	Output Fall Time	$V_T = 2\text{V}$, $R_T = 10\Omega$, $C_L = 30 \text{ pF}$, $\text{DE} = 3\text{V}$	1	2	5	ns
t_{skew}	Skew Between Drivers	(1)		1		ns

- (1) t_D and t_R skew is an absolute value, defined as differences seen in propagation delays between each of the drivers or receivers in the same package of the same delay, V_{CC} , temperature and load conditions.

Switching Characteristics (continued)

 $T_A = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	in Same Package					
DRIVER ENABLE: (Figure 4 and Figure 7)						
t_{PHL}	Enable Delay	$V_T = 2\text{V}$, $R_T = 10\Omega$, $C_L = 30\text{ pF}$, $D_n = 3\text{V}$	1	3.5	7	ns
t_{PLH}	Disable Delay	$V_T = 2\text{V}$, $R_T = 10\Omega$, $C_L = 30\text{ pF}$, $D_n = 3\text{V}$	1	3.5	7	ns
RECEIVER: (Figure 6 and Figure 8)						
t_{PHL}	Receiver Input to Output	$C_L = 50\text{ pF}$, $\overline{RE} = DE = 0.3\text{V}$, S_3 Closed	2	5	8	ns
t_{PLH}	Receiver Input to Output	$C_L = 50\text{ pF}$, $\overline{RE} = DE = 0.3\text{V}$, S_3 Open	2	5	8	ns
t_{skew}	Skew Between Receivers	(1)		1		ns
	in Same Package					
RECEIVER ENABLE: (Figure 5 and Figure 9)						
t_{ZL}	Receiver Enable to	$C_L = 50\text{ pF}$, $R_L = 500$, $DE = 0.3\text{V}$	2	6	12	ns
	Output Low	S_2 Open $B_n = 2\text{V}$				
t_{ZH}	Receiver Enable to	$C_L = 50\text{ pF}$, $R_L = 500$, $DE = 0.3\text{V}$	2	5	12	ns
	Output High	S_1 Open $B_n = 1\text{V}$				
t_{LZ}	Receiver Disable	$C_L = 50\text{ pF}$, $R_L = 500$, $DE = 0.3\text{V}$	1	5	8	ns
	From Output Low	S_2 Open $B_n = 2\text{V}$				
t_{HZ}	Receiver Disable	$C_L = 50\text{ pF}$, $R_L = 500$, $DE = 0.3\text{V}$	1	4	8	ns
	From Output High	S_1 Open $B_n = 1\text{V}$				

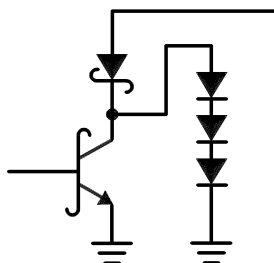
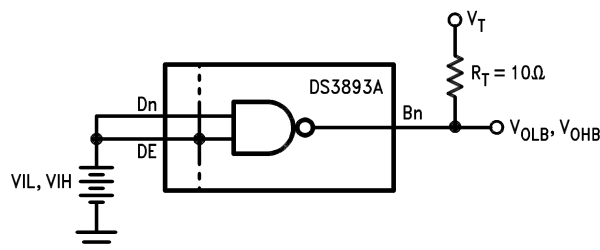


Figure 2. Equivalent Bus Output



Note: $n = 1, 2, 3, 4$

Figure 3. Driver Output Voltage

AC Test Circuits

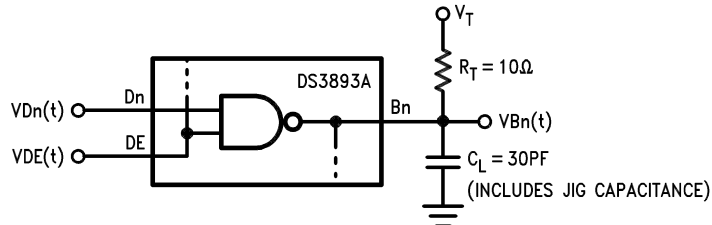


Figure 4.

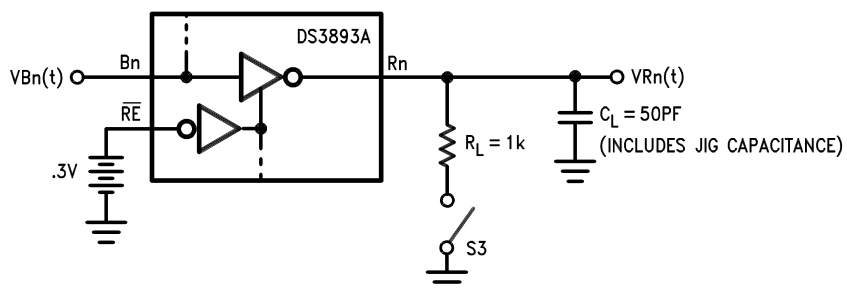
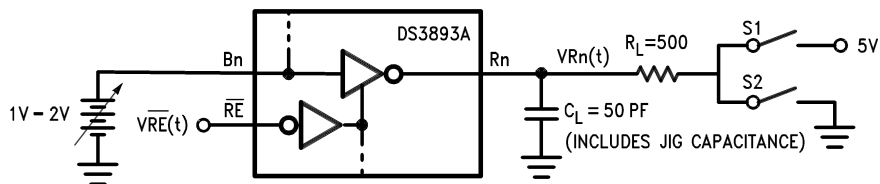


Figure 5.



Note:
Unless Otherwise Specified
The Switches are Closed

Figure 6.

Switching Time Waveforms

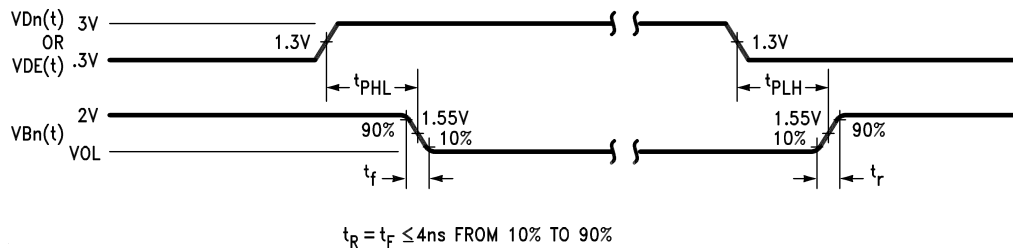
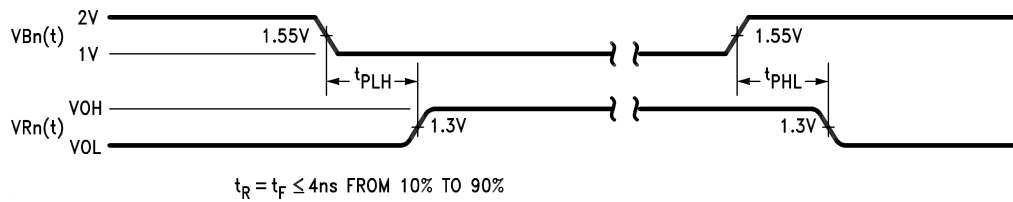
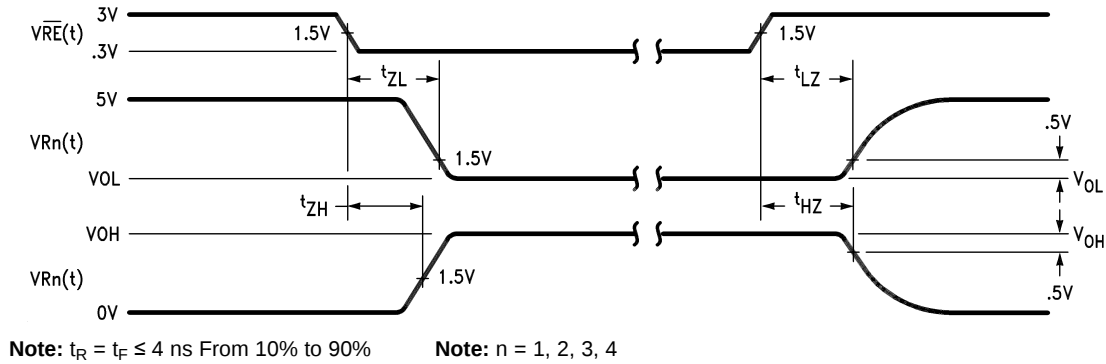
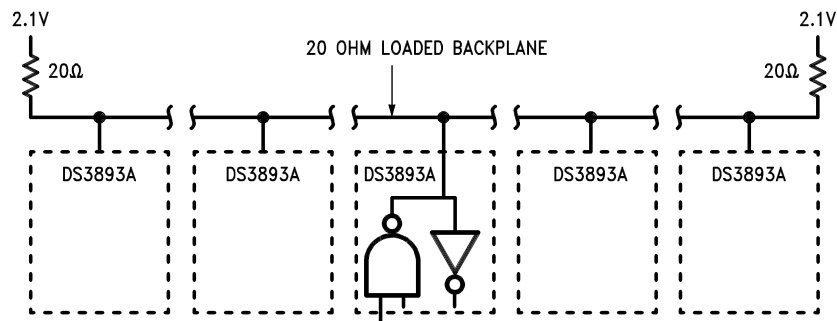


Figure 7. Driver Propagation Delay

**Figure 8. Receiver Propagation Delay****Figure 9. Receiver Enable and Disable Times****Typical Application**

APPLICATION INFORMATION

Due to the high current and very high speed capability of the TURBOTRANSCEIVER's driver output stage, circuit board layout and bus grounding are critical factors that affect the system performance.

Each of the TURBOTRANSCEIVER's bus ground pins should be connected to the nearest backplane ground pin with the shortest possible path. The ground pins on the connector should be distributed evenly through its length.

Although the bandgap reference receiver threshold provides sufficient DC noise margin (Figure 10), ground noise and ringing on the data paths could easily exceed this margin if the series inductance of the traces and connectors are not kept to a minimum. The bandgap ground pin should be returned to the connector through a separate trace that does not carry transient switching currents. The transceivers should be mounted as close as possible to the connector. It should be noted that even one inch of trace can add a significant amount of ringing to the bus signal.

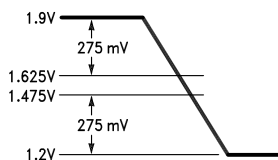
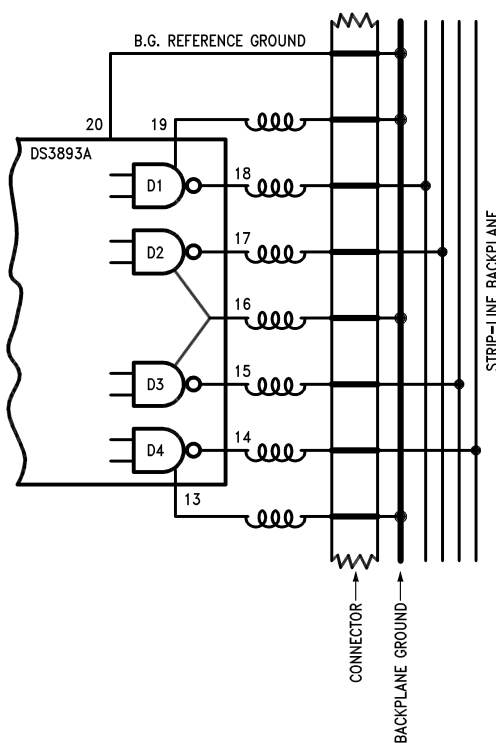


Figure 10. Noise Margin



REVISION HISTORY

Changes from Revision C (February 2013) to Revision D

Page

- Changed layout of National Data Sheet to TI format [7](#)

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