

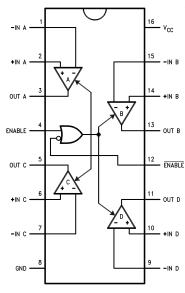
DS26F32M Quad Differential Line Receivers

Check for Samples: DS26F32M

FEATURES

- Military Temperature Range
- Input Voltage Range of ±7.0V (Differential or Common Mode) ±0.2V Sensitivity Over the Input Voltage Range
- Meets All the Requirements of EIA Standards RS-422 and RS-423
- High Input Impedance (18k Typical)
- 30 mV Input Hysteresis
- Operation from Single +5.0V Supply
- Input Pull-Down Resistor Prevents Output Oscillation on Unused Channels
- Tri-state Outputs, with Choice of Complementary Enables, for Receiving Directly onto a Data Bus
- Propagation Delay 15 ns Typical

Connection Diagram



For Complete Military Product Specifications, refer to the appropriate SMD or MDS.

Figure 1. 16-Lead DIP Top View See Package Number NAJ0020A, NFE0016A or NAD0016A

DESCRIPTION

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and tri-state outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

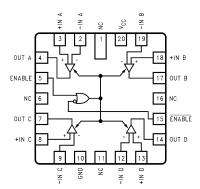


Figure 2. 20-Lead LCCC

Table 1. Function Table (1) (Each Receiver)

Differential Inputs	Enables		Outputs
$V_{ID} = (V_{IN} +) - (V_{IN} -)$	E	Ē	OUT
V _{ID} ≥ 0.2V	Н	Х	Н
	Х	L	Н
V _{ID} ≤ −0.2V	Н	Х	L
	Х	L	L
X	L	Н	Z

(1) H = High Level

L = Low Level

X = Immaterial

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

- <u></u>	1	
Storage Temperature Range CDIP		−65°C + to 175°C
Operating Temperature Range	DS26F32M	−55°C to +125°C
	DS26F32C	0°C to +70°C
Lead Temperature CDIP (soldering, 60 sec)		300°C
Maximum Power Dissipation (3) at 25°C	Cavity Package	1500 mW
	Supply Voltage	7.0V
	Common Mode Voltage Range	±25V
	Differential Input Voltage	±25V
	Enable Voltage	7.0V
	Output Sink Current	50 mA

⁽¹⁾ Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics provide conditions for actual device operation.

Operating Range

DS26F32M	Temperature	−55°C to +125°C
	Supply Voltage	4.5V to 5.5V

Product Folder Links: DS26F32M

²⁾ If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

⁽³⁾ Derate cavity package 10 mW/°C above 25°C.



Electrical Characteristics (1)(2)

Over operating range, unless otherwise specified

Symbol	Parameter	Conditions		Min	Тур	Max	Units
V _{TH}	Differential Input Voltage	$-7.0V \le V_{CM} \le +7.0V$, $V_O = V_{OL} \text{ or } V_{OH}$		-0.2	±0.06	+0.2	V
R _I	Input Resistance	-15V ≤ V _{CM} ≤ +15V, One Input AC Ground		14	18		kΩ
l _l	Input Current (under Test)	$V_{\parallel} = +15V,$ Other Input $-15V \le V_{\parallel} \le +15V$ $V_{\parallel} = -15V,$ Other Input $-15V \le V_{\parallel} \le +15V$				2.3	mA
						-2.8	
V _{OH}	Output Voltage HIGH	V _{CC} = Min,	0°C to +70°C	2.8	3.4		V
		$\Delta V_{I} = +1.0V,$ $V_{ENABLE} = 0.8V,$ $I_{OH} = -440 \mu A$	−55°C to +125°C	2.5	3.4		
V _{OL}	Output Voltage LOW	$V_{CC} = Min,$ $\Delta V_{I} = -1.0V,$ $V_{ENABLE} = 0.8V$	I _{OL} = 4.0 mA			0.4	V
			I _{OL} = 8.0 mA			0.45	
V _{IL}	Enable Voltage LOW					0.8	V
V _{IH}	Enable Voltage HIGH			2.0			V
V _{IC}	Enable Clamp Voltage	V _{CC} = Min, I _I = −18 mA				-1.5	V
I _{OZ}	Off State (High Impedance) Output Current	V _{CC} = Max	V _O = 2.4V			20	
			$V_0 = 0.4V$			-20	μA
I _{IL}	Enable Current LOW	V _I = 0.4V			-0.2	-0.36	mA
I _{IH}	Enable Current HIGH	V _I = 2.7V			0.5	10	μΑ
I _I	Enable Input High Current	V _I = 5.5V			1.0	50	μΑ
I _{os}	Output Short Circuit Current	$V_O = 0V$, $V_{CC} = Max$, See ⁽³⁾ $\Delta V_I = +1.0V$		-15	-50	-85	mA
I _{CC}	Supply Current	V _{CC} = Max, All V _I = GND, Outputs Disabled			30	50	mA
V_{HYST}	Input Hysteresis	$T_A = 25^{\circ}C, V_{CC} = 5.0V, V_{CM} = 0V$			30		mV

⁽¹⁾ Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F32M and across the 0°C

Switching Characteristics (1)(2)

 $V_{CC} = 5.0V, T_A = 25^{\circ}C$

Symbol	Parameter	Condit	Conditions		Тур	Max	Units
t _{PLH}	Input to Output	See (Figure 4, and	$C_{L} = 15 \text{ pF}$		15	22	ns
t _{PHL}	Input to Output	Figure 5)			15	22	ns
t_{LZ}	Enable to Output		0 5-5		14	18	ns
t_{HZ}	Enable to Output	See (Figure 4, and	$C_L = 5 pF$		15	20	ns
t_{ZL}	Enable to Output	Figure 6)	C 15 pF		13	18	ns
t_{ZH}	Enable to Output		$C_L = 15 pF$		12	16	ns

⁽¹⁾ All diodes are IN916 or IN3064.

Product Folder Links: DS26F32M

to +70°C range for the DS26F32C. All typicals are given for V $_{CC}$ = 5V and T_A = 25°C. All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

⁽³⁾ Only one output at a time should be shorted.

⁽²⁾ C L includes probe and jig capacitance.



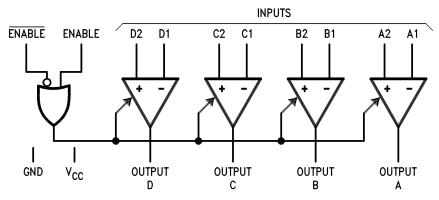


Figure 3. Logic Symbol

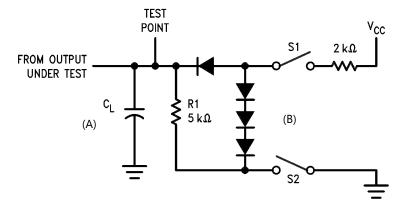


Figure 4. Load Test Circuit for Three-State Outputs

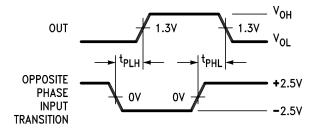


Figure 5. Propagation Delay⁽³⁾⁽⁴⁾⁽⁵⁾

(3) Diagram shown for ENABLE Low.

(4) S1 and S2 of Load Circuit are closed except where shown.

(5) Pulse Generator of all Pulses: Rate $\leq 1.0 \text{ MHz}$, $Z_0 = 50\Omega$, $t_r \leq 6.0 \text{ ns}$, $t_f \leq 6.0 \text{ ns}$.



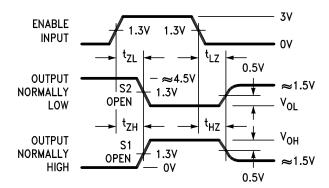
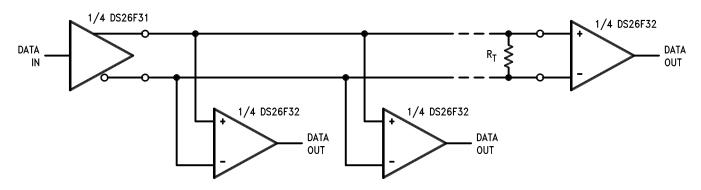


Figure 6. Enable and Disable Times (3)(4)(5)

TYPICAL APPLICATION



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REVISION HISTORY

Cł	hanges from Revision B (April 2013) to Revision C	Pag	j€
•	Changed layout of National Data Sheet to TI format		5

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