DS96177 RS-485/RS-422 Differential Bus Repeater

Check for Samples: DS96177

FEATURES

- **Meets EIA Standard RS-422A and RS-485**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **TRI-STATE Outputs**
- **Bus Voltage Range −7.0V to +12V**
- **Positive and Negative Current Limiting**
- **Driver Output Capability ±60 mA max**
- **Driver Thermal Shutdown Protection**
- **Receiver Input High Impedance**
- **Receiver Input Sensitivity of ±200 mV**
- **Receiver Unput Hysteresis of 50 mV Typical**
- **Operates from Single 5.0V Supply**
- **Low Power Requirements**

DESCRIPTION

The DS96177 Differential Bus Repeater is a monolithic integrated device designed for one-way data communication on multipoint bus transmission lines. This device is designed for balanced transmission bus line applications and meets EIA Standard RS-485 and RS-422A. The device is designed to improve the performance of the data communication over long bus lines. The DS96177 has an active high Enable.

The DS96177 features positive and negative current limiting and TRI-STATE outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

The DS96177 is designed for optimum performance when used on transmission buses employing the DS96172 and DS96174 differential line drivers, DS96173 and DS96175 differential line receivers, or DS96176 differential bus transceivers.

Connection Diagram

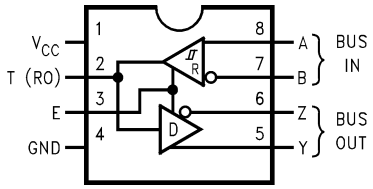


Figure 1. 8-Lead PDIP Package - Top View

Table 1. Function Table(1)

Differential Inputs	Enable	Outputs		
A–B	**E**	**T**	**Y**	**Z**
$V_{ID} \geq 0.2V$	H	H	H	L
$V_{ID} \leq -0.2V$	H	L	L	H
X	L	Z	Z	Z

(1) T is an output pin only, monitoring the BUS (RO).
H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Storage Temperature Range	CDIP	−65°C to +175°C
	PDIP	−65°C to +150°C
Lead Temperature	CDIP (Soldering, 60 sec.)	300°C
	PDIP (Soldering, 10 sec.)	265°C
Maximum Power Dissipation[3] at 25°C	PDIP Package	930 mW
Supply Voltage		7.0V
Input Voltage		5.5V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Derate PDIP package 7.5 mW/°C above 25°C.

Recommended OperatingConditions

		Min	Typ	Max	Units
Supply Voltage (V_{CC})		4.75	5.0	5.25	V
Voltage at any Bus Terminal					
(Separately or Common Mode) (V_I or V_{CM})		−7.0		12	V
Differential Input Voltage (V_{ID})				±12	V
Output Current HIGH (I_{OH})	Driver			−60	mA
	Receiver			−400	µA
Output Current LOW (I_{OL})	Driver			60	mA
	Receiver			16	
Operating Temperature (T_A)		0	25	70	°C

Electrical Characteristics[1][2]

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER SECTION							
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, Figure 2		2.0	2.25		V
		R_L = 54Ω, Figure 2 and Figure 3		1.5	2.0		
$\Delta\|V_{OD2}\|$	Change in Magnitude of Differential Output Voltage[3]	R_L = 100Ω, Figure 2				±0.2	V
		R_L = 54Ω Figure 2 and Figure 3	V_{CM} = 0V				
V_{OC}	Common Mode Output Voltage[4]	R_L = 54Ω or 100Ω (Figure 2)				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage[3]					±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V				±100	µA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±50	±200	µA
I_{IH}	Input Current HIGH	V_I = 2.7V				20	µA

(1) Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96177. All typicals are given for V_{CC} = 5V and T_A = 25°C.
(2) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD}, V_{OC} respectively, that occur when the input is changed from a high level to a low level.
(4) In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Electrical Characteristics[1][2] (continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Input Current LOW	V_I = 0.5V				−100	µA
I_{OS}	Short Circuit Output Current[5]	V_O = −7.0V				−250	
		V_O = 0V				−150	mA
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	
RECEIVER SECTION							
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage[6]	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
V_{T+}−V_{T-}	Hysteresis[7]	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{ID} = 200 mV, I_{OH} = −400 µA, Figure 4		2.7			V
V_{OL}	Low Level Output Voltage	V_{ID} = −200 mV, Figure 4	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4V				−360	µA
		V_O = 2.4V				20	
I_I	Line Input Current[8]	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	µA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	µA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	See[9]		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

(5) Only one output at a time should be shorted.
(6) The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
(7) Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.
(8) Refer to EIA Standards RS-485 for exact conditions.
(9) Only one output at a time should be shorted.

Drive Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, Figure 5		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60Ω, Figure 5		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, Figure 6		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27Ω, Figure 6		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, Figure 7		25	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, Figure 8		25	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, Figure 7		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, Figure 8		29	35	ns

Receiver Switching Characteristics

V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, Figure 9		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, (1)		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, (1)		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

(1) Testing at 20 pF assures conformance to 5 pF specification.

Parameter Measurement Information

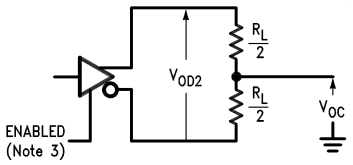


Figure 2. Driver V_{OD2} and V_{OC} (2)

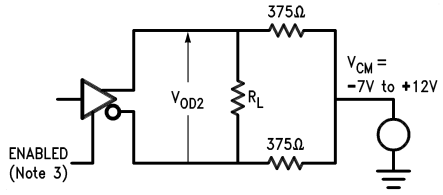


Figure 3. Driver V_{OD2} with Varying Common Mode Voltage (2)

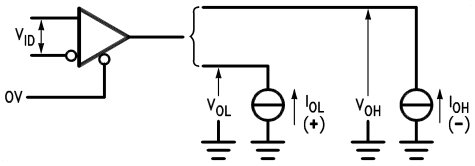


Figure 4. Receiver V_{OH} and V_{OL}

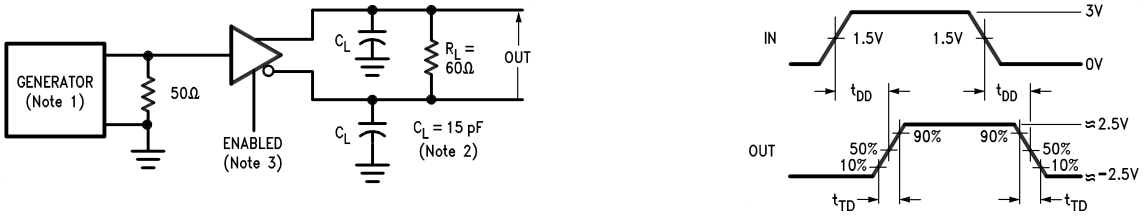


Figure 5. Driver Differential Output Delay and Transition Times (2) (3) (4)

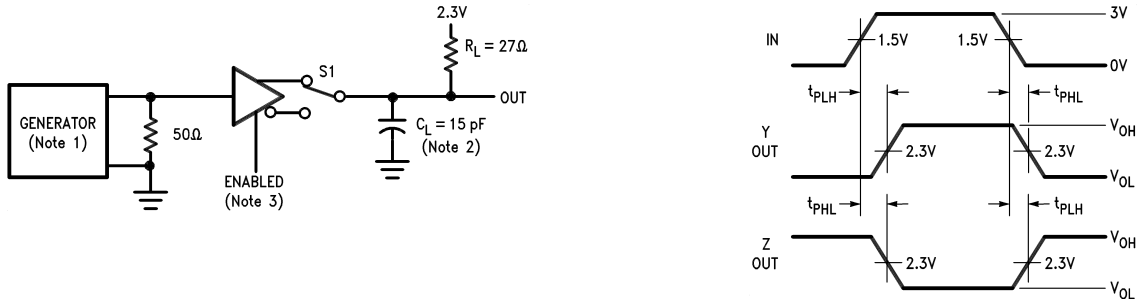


Figure 6. Drive Propagation Times (2) (3) (4)

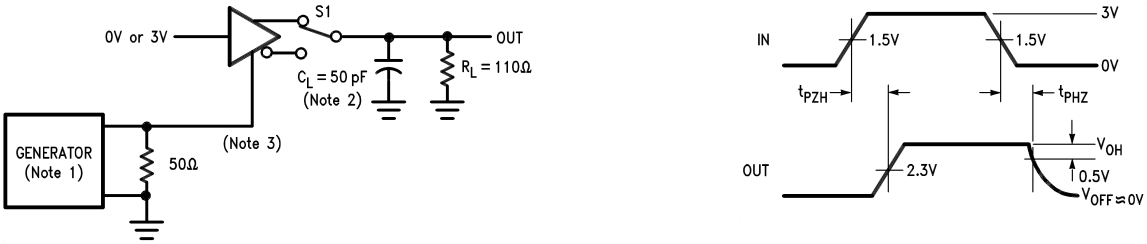


Figure 7. Driver Enable and Disable Times (t_{PZH}, t_{PHZ}) (2) (3) (4)

(2) DS96177 Enable is active high.
(3) The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle ≈ 50%, tr ≤ 6.0 ns, tf ≤ 6.0 ns, ZO = 50Ω.
(4) CL includes probe and stray capacitance.

Parameter Measurement Information (continued)

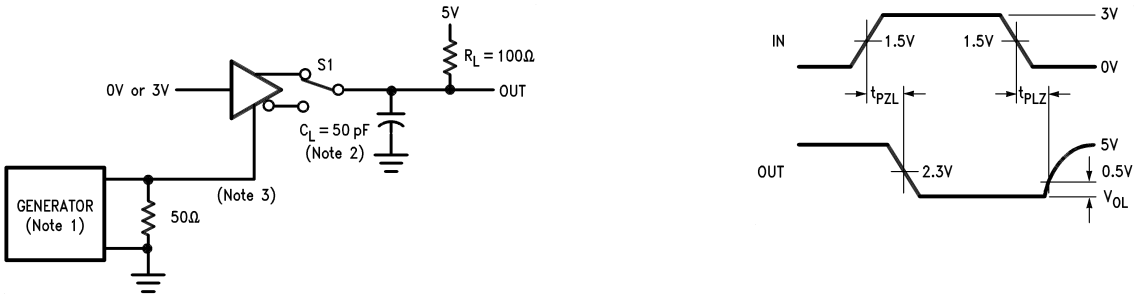


Figure 8. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})(2)(3)(4)

Parameter Measurement Information (continued)

Figure 9. Receiver Propagation Delay Times(5)(6)(7)

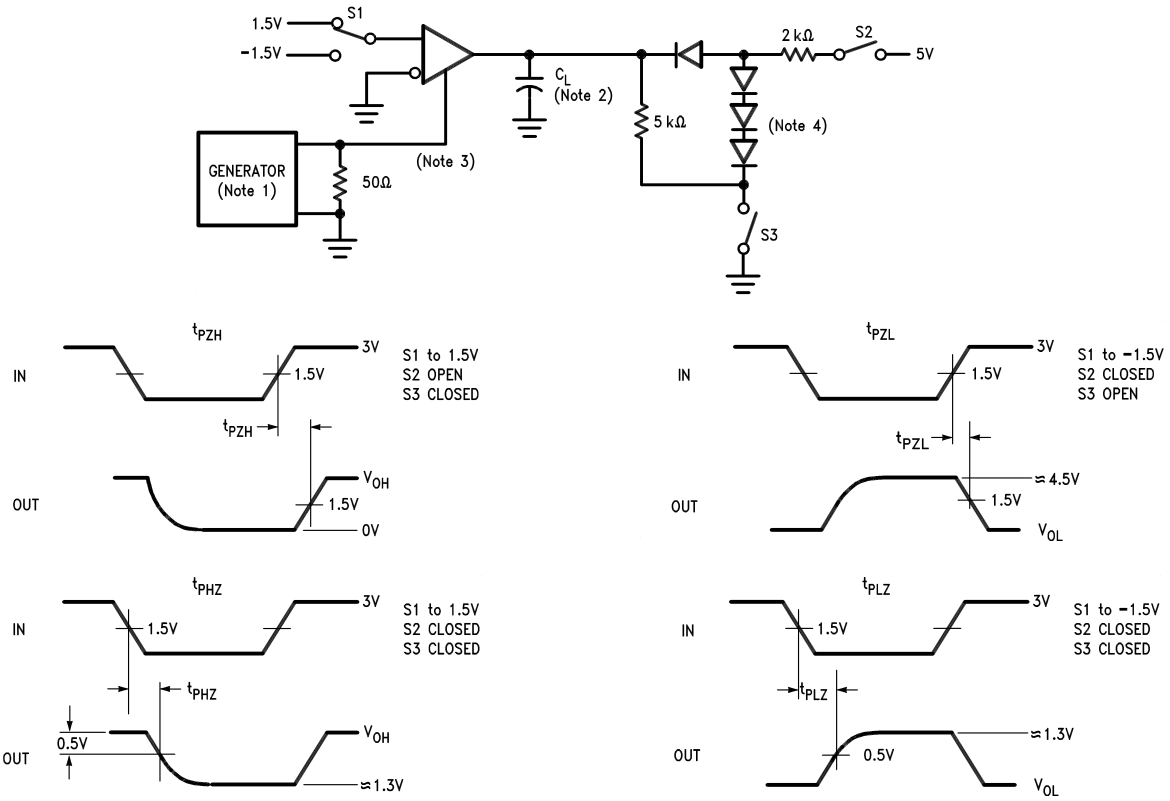
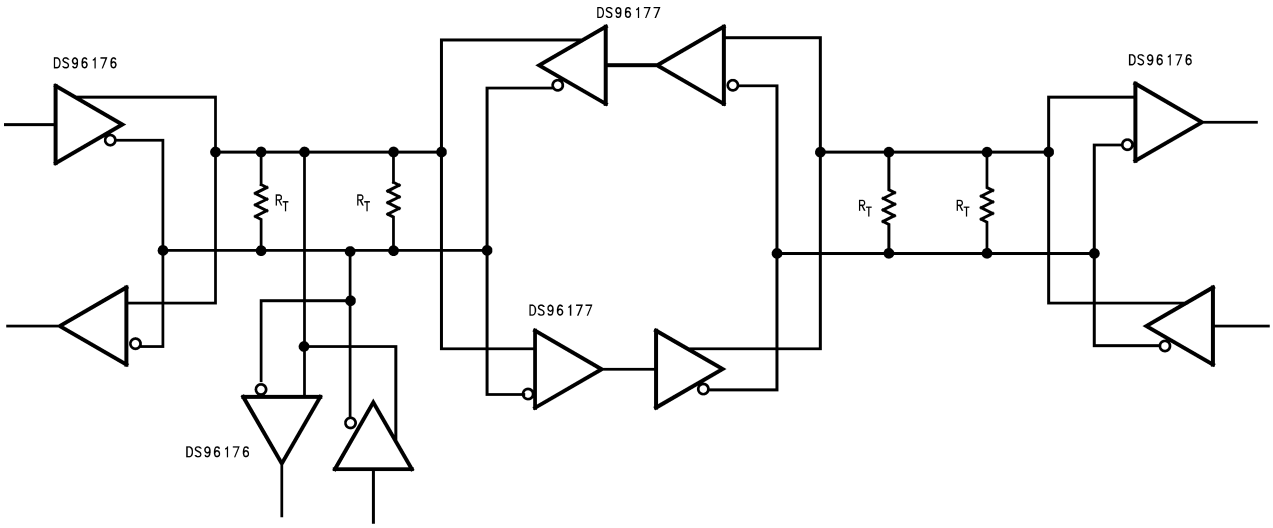


Figure 10. Receiver Enable and Disable Times(5)(6)(7)(8)

(5) DS96177 Enable is active high.
(6) The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle ≈ 50%, tr ≤ 6.0 ns, tf ≤ 6.0 ns, ZO = 50Ω.
(7) CL includes probe and stray capacitance.
(8) All diodes are 1N916 or equivalent.

TYPICAL APPLICATION



The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.
Repeater control logic not shown

Figure 11.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

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