LM3017 High Efficiency Low-Side Controller with True Shutdown

Check for Samples: LM3017

FEATURES

- **Fully compliant to Thunderbolt™ Technology specifications**
- **True shutdown for short circuit protection**
- **Single enable pin with three modes of operation: boost, pass through, or shutdown**
- **Built-in charge pump for high-side NFET disconnect switch**
- **1A push-pull driver for low-side NFET**
- **Peak current mode control**
- **Simple slope compensation**
- **Protection features: thermal shutdown, cycle-by-cycle current limit, short circuit protection, output overvoltage protection, and latch-off**
- **Internal soft-start**
- **2.4mm x 2.7mm x 0.8mm 10-pin QFN package**

APPLICATIONS

- **Thunderbolt Technology™ Host Ports**
- **Notebook and Desktop Computers, Tablets, and Other Portable Consumer Electronics**
- **Hard Disc Drives, Solid State Drives**
- **Offline Power Supplies**
- **Set-Top Boxes**

DESCRIPTION

The LM3017 is a versatile low-side NFET controller incorporating true shutdown and input side current limiting. It is designed for simple implementation of boost conversions in Thunderbolt™ Technology. The LM3017 can also be configured for flyback or SEPIC designs. The input voltage range of 5V to 18V accommodates a two or three cell lithium ion battery or a 12V rail. The enable pin accepts a single input to drive three different modes of operation: boost, pass through, or shutdown mode. The LM3017 draws very low current in shutdown mode, typically 40nA from the input supply.

The LM3017 provides an adjustable output from V_{IN} to 20V in order to drive the Power Load Switch or Mux for the host Thunderbolt™ port. The ability to drive an external high-side NMOS provides for true isolation of the load from the input. Current limiting on the input ensures that inrush and short-circuit currents are always under control. The LM3017 incorporates built in thermal shutdown, cycle-by-cycle current limit, short circuit protection, output overvoltage protection, and soft-start. It is available in a 10-pin QFN package.

Table 1. Key Specifications

		VALUE	UNIT
Input voltage range of 5V to 18V			
400 kHz fixed frequency operation			
±1% reference voltage accuracy over temperature			
Low shutdown current (< 1µA), 40nA typical			
±3% D.C. input current limit			

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Typical Application Circuit

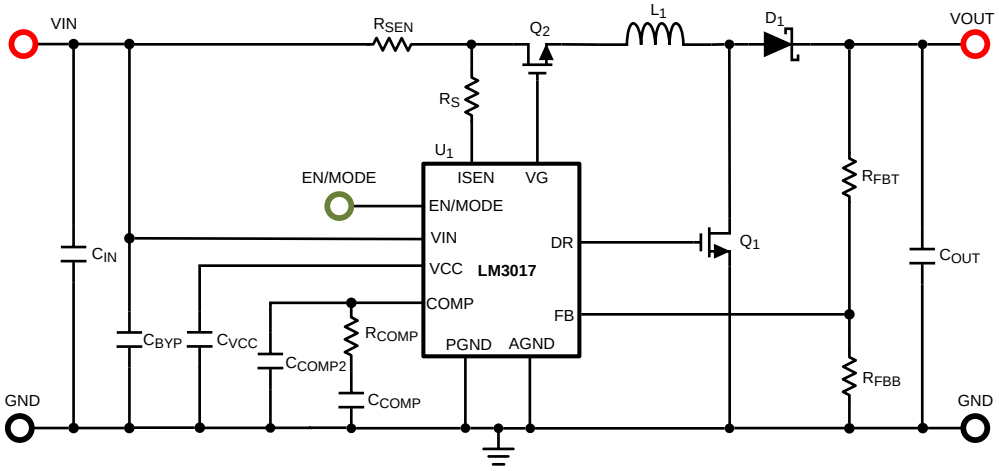
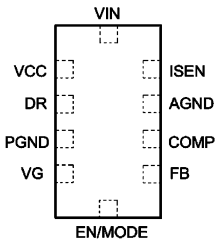


Figure 1. Typical Boost Converter Application

10-pin QFN
Top View



Pin Descriptions

Pin	Name	Description	Function
1	VCC	Driver supply voltage pin	Output of internal regulator powering low side NMOS driver. A minimum of 0.47µF must be connected from this pin to PGND for proper operation.
2	DR	Low-side NMOS gate driver output	Output gate drive to low side NMOS gate.
3	PGND	Power Ground	Ground for power section. External power circuit reference. Should be connected to AGND at a single point.
4	VG	High side NMOS gate driver output	Output gate drive to high side NMOS gate.
5	EN/MODE	Multi-function input pin	This input provides for chip enable, and mode selection. See functional description for details.
6	FB	Feed-back input pin	Negative input to error amplifier. Connect to feed-back resistor tap to regulate output.
7	COMP	Compensation pin	A resistor and capacitor combination connected to this pin provides frequency compensation for the regulator control loop.
8	AGND	Analog Ground	Ground for analog control circuitry. Reference point for all stated voltages.
9	ISEN	Current sense input	Current sense input, with respect to Vin, for all current limit functions.
10	VIN	Power Supply input pin	Input supply to regulator. See applications section for recommendations on bypass capacitors on this pin.

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Absolute Maximum Ratings (1)

VIN to PGND, AGND	-0.3V to 20V
FB, EN/MODE, COMP, VCC	-0.3V to 6V
ISEN, DR, VG to PGND, AGND	-0.3V to 20V
Peak low side driver output current	1.0A

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicates conditions for which the device is intended to be functional, but does not specify performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions.

Operating Ratings (1)

VIN	5V to 18V
Junction Temperature Range (T_J)	−40°C to +125°C
ESD Susceptibility (2)	±2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicates conditions for which the device is intended to be functional, but does not specify performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions.
(2) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method is per JESD-22-114.

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Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: Vin = 12V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{FB}	Feedback Voltage	Vcomp = 1.4V, 5V ≤ Vin ≤ 18V 0°C to +85°C	**1.26225**	1.275	**1.28775**	V
	Feedback Voltage	Vcomp = 1.4V, 5V ≤ Vin ≤ 18V -40°C to +125°C	**1.2495**	1.275	**1.3005**	V
ΔV_{LINE}	Feedback Voltage Line Regulation	5V ≤ Vin ≤ 18V		TBD		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	Vin = 12V		TBD		%/A
V_{UVLO}	Input Under Voltage Lock-Out reference Voltage	Ramping up	**TBD**	4.5	**TBD**	V
	Input Under Voltage Lock-Out reference Voltage Hysteresis		**TBD**	300	**TBD**	mV
F_{nom}	Nominal Switching Frequency	(3)	**360**	400	**440**	kHz
$R_{DS(ON)}$	Low side NMOS driver resistance; top switch	Vin = 5V, I_{DR} = 0.2A		4		Ω
	Low side NMOS driver resistance; bottom switch	Vin = 5V, I_{DR} = 0.2A		2		Ω
$V_{DR\ (max)}$	Maximum Driver Voltage Supply	Vin < 6V		Vin		V
		Vin ≥ 6V		6		
D_{max}	Maximum Duty Cycle			85		%
$T_{min(on)}$	Minimum On Time			250		ns
I_{run}	Supply Current in Boost Mode - No-load	EN/MODE pin = 1.6V FEEDBACK pin = 1.4V		4	**TBD**	mA
I_Q	Supply Current in Shutdown Mode	EN/MODE pin = 0.3V			**1**	µA
I_{stby}	Supply Current in Stand-by mode	EN/MODE pin = 2.6V		1.2	**TBD**	mA
$V_{en\text{-}stby}$	Stand-by Mode Threshold	EN/MODE pin thresholds	**TBD**	2.6	**TBD**	V
$V_{en\text{-}shutdown}$	Shut-down Mode Threshold	EN/MODE pin thresholds	**TBD**	0.4	**TBD**	V
$V_{en\text{-}run}$	Run Mode Window	EN/MODE pin thresholds	**1.6**	1.9	**2.2**	V
I_{en}	EN/MODE pin bias current	EN/MODE = 1.6V	**TBD**	±1.0	**TBD**	µA
V_{SENSE}	Cycle-by-Cycle Current Limit Threshold during boost mode	EN/MODE = 1.6V FB = 0.5V	**153**	170	**187**	mV
V_{SL}	Internal Ramp Compensation Voltage			90		mV
V_{LIM1}	Input Current Limit Threshold Voltage in Stand-by mode	EN/MODE = 2.6V (4)	**82**	85	**88**	mV
V_{LIM2}	Input Current Limit Threshold Voltage in Stand-by Mode (during Start-up)	EN/MODE = 2.6V (4)	**TBD**	102	**TBD**	mV
V_{OVP}	Output-Over Voltage Protection Threshold	Measured with respect to FB pin. VCOMP = 1.4V	**TBD**	85	**TBD**	mV
$V_{OVP(HYS)}$	Output-Over Voltage Protection Threshold Hysteresis	Measured with respect to FB pin. VCOMP = 1.4V	**TBD**	70	**TBD**	mV
V_{SC}	Short Circuit Current Limit Threshold during boost mode			200		mV
G_m	Error Amplifier Transconductance	VCOMP = 1.4V	**216**	450	**690**	µA/V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate the Average Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Typical values are programmed by metal mask options. The following options are available: 100 kHz, 200 kHz, 340 kHz, 400 kHz, 500 kHz, 750 kHz, 1 MHz. Consult the factory for details.
(4) See text for details of current limit operation.

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Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: Vin = 12V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{G-max}	Maximum Drive voltage at VG pin	Vin = 5V, Isense = 5V I_G = 0A		10		V
V_{G-min}	Minimum Drive voltage at VG pin	Vin = 5V, Isense = Vin - 200mV I_G = 0A		100		mV
I_G	Maximum Drive current at VG pin	Vin = 5V, Isense = 5V V_G = Vin		500		µA
A_{VOL}	Error Amplifier Open Loop Voltage Gain		**35**	60	**66**	V/V
I_{EAO}	Error Amplifier Output Current Limits	SOURCING: VCOMP = 1.4V V_{FB} = 1.1V	**475**	640	**837**	µA
		SINKING: VCOMP = 1.4V VFB = 1.4V	**31**	65	**100**	µA
V_{EAO}	Error Amplifier Output Voltage Limits	UPPER LIMIT: VFB = 0V	**2.45**	2.7	**2.93**	V
		LOWER LIMIT: V_{FB} = 1.4V	**0.32**	0.6	**0.9**	V
T_{ss}	Internal Soft-Start Delay	V_{FB} = 1.2V		10		ms
T_{LIM1}	Current Limit time at VLIM1	(4)		TBD		ms
T_{LIM2}	Current Limit time at VLIM2	(5)		TBD		
T_{sc}	Short-Circuit Time in Boost	(5)		TBD		ms
T_{DELAY}	Time delay to transition between stand-by and boost	(5)		TBD		
T_{BLANK}	Current Limit Latch-off Blank Time	(5)		TBD		
T_r	Drive Pin Rise Time	Cload = 3nF V_{DR} = 0V to 3V		25		ns
T_f	Drive Pin Fall Time	Cload = 3nF V_{DR} = 3V to 0V		25		ns
T_{SD}	Thermal Shutdown Threshold			165		°C
$T_{SD-hyst}$	Thermal Shutdown Threshold Hysteresis			10		°C

(5) See text for details of current limit operation.

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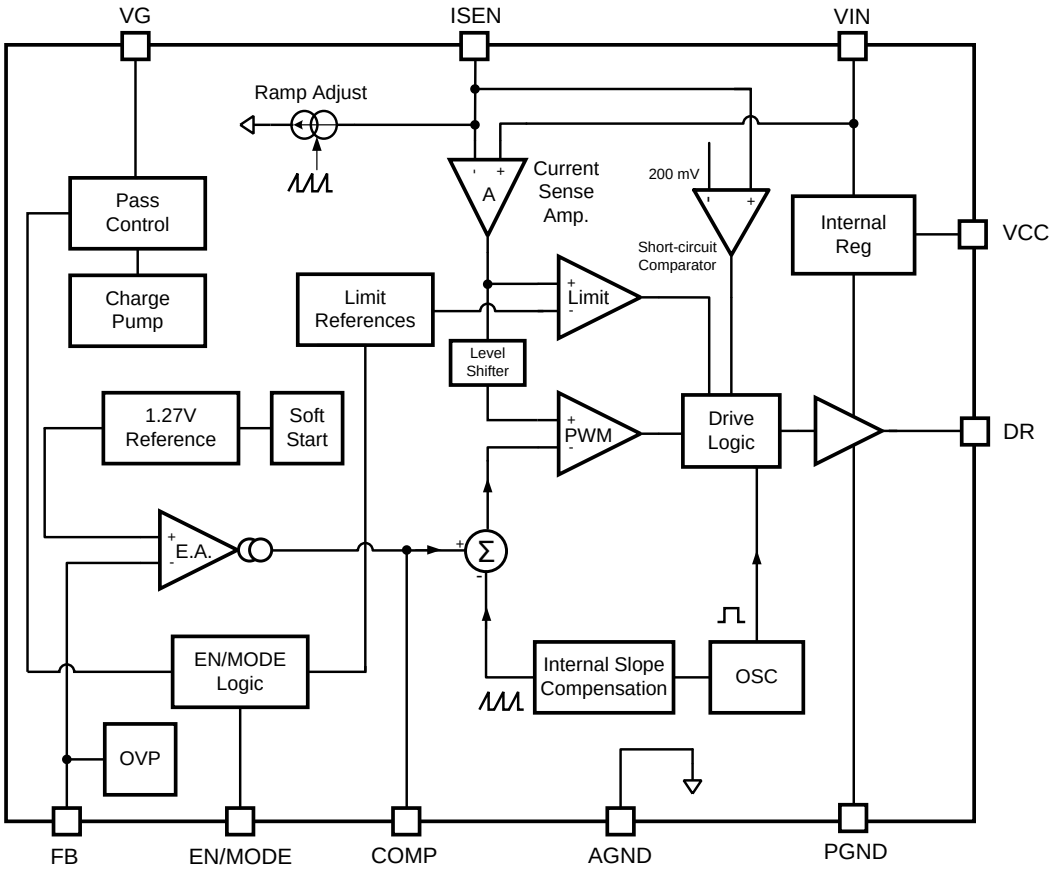
Functional Block Diagram



Functional Description

The LM3017 uses a fixed frequency, Pulse Width Modulated (PWM), current mode control architecture. In a typical application circuit, the peak current through the external high side MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is then level shifted and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier (EA) negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator.

At the start of any switching cycle, the oscillator sets a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the Drive Logic is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in Figure 2. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration, called the blank-out time, is typically 250 ns and is specified as T_{min} (on) in the electrical characteristics section.

Under extremely light load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the blank-out time is more than what is delivered to the load. An over-voltage comparator inside the LM3017 prevents the output voltage from rising under these conditions by sensing the feedback (FB pin) voltage and resetting the RS latch. The latch remains in a reset state until the output decays to the nominal value. Thus the operating frequency decreases at light loads, resulting in excellent efficiency.

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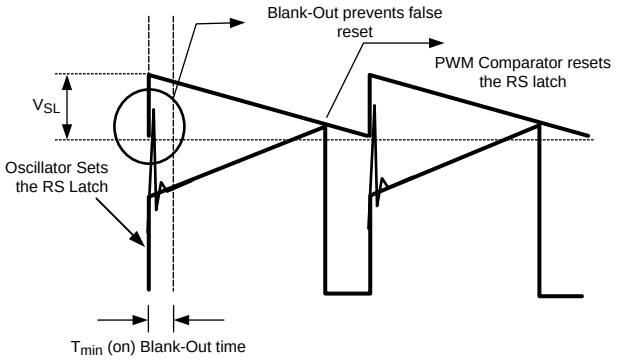

Figure 2. Basic Operation of the PWM comparator

OPERATION OF THE EN/MODE PIN

The EN/MODE pin drives the high side gate (VG pin) to enable or disable the output through the high side MOSFET (pass MOSFET), furthermore it defines the current limit for each operation mode (see next section).

1) $V_{EN/MODE}$ < 0.4V **Shutdown mode** (1)
2) 0.4V < $V_{EN/MODE}$ < 2.6V **Boost mode** (2)
3) $V_{EN/MODE}$ > 2.6V **Standby mode** (3)

SHUTDOWN MODE

Pulling the EN/MODE pin to less than 0.4V, for more than 50µS, during any mode of operation, will place the part in full shutdown mode. The boost regulator and high-side NMOS FET will be off and the load will be disconnected from the input supply. In this mode, the regulator will draw a maximum of 1µA from the input supply.

BOOST MODE

The boost regulator can be turned on by bringing the EN/MODE pin to greater than 1.6V, but less than 2.2V. This is the run mode for the boost regulator. Note that the LM3017 will always start in stand-by and transition to boost mode, after a delay of TDELAY=XXms (typ); see typical waveforms. If the EN/MODE pin is taken to a value >2.6V, the part will enter stand-by mode.

STANDBY MODE

Pulling the EN/MODE pin to greater than 2.6V, for more than 50µS, during any mode of operation, will place the part in stand-by mode. The boost regulator will be off and the high-side NMOS FET will be on. During this mode, the load is connected to the input supply through the inductor.

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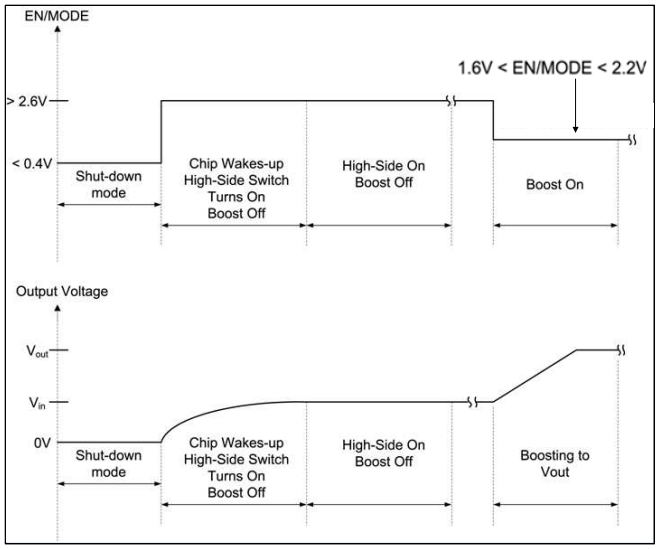

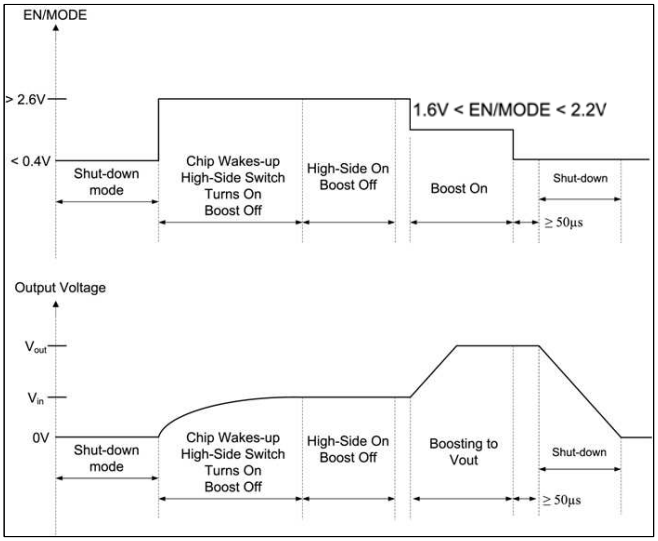

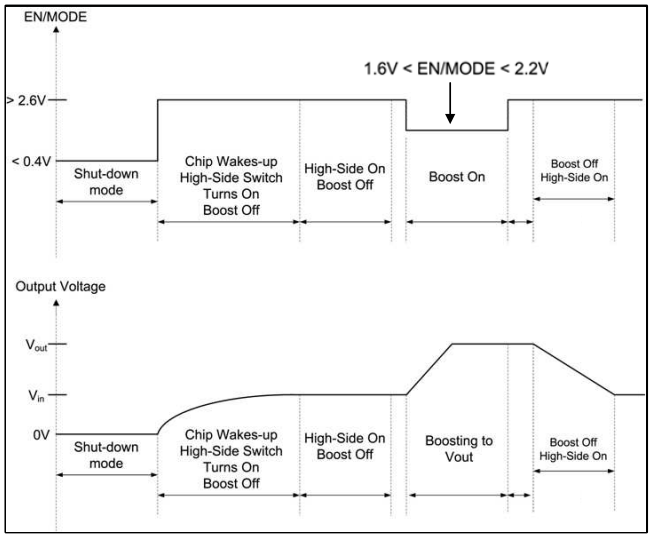

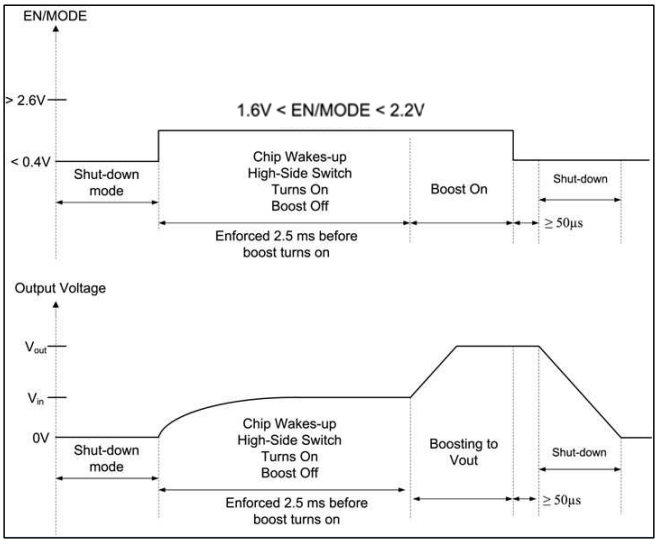

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CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

Boost Mode

In boost mode the LM3017 features both cycle-by-cycle current limit and short circuit protection. Unlike most boost regulators, the LM3017 can protect itself from short circuits on the output by shutting off the pass FET. The boost current limit, defined by V_{CL}=170mV in the electrical characteristics table, turns off the boost FET for normal overloads on a cycle-by-cycle basis. The current is limited to V_{CL}/R_{SEN} until the overload is removed. Should the output be shorted, or otherwise pulled below V_{IN}, the inductor current will have a tendency to "run-away". This is prevented by the short circuit protection feature, defined as V_{SC} = 200mV in the electrical characteristics table. When this current limit is tripped, the current is limited to V_{SC}/R_{SEN} by controlling the pass FET. If the short persists for T_{SC} > 450µs the pass FET will be latched off. In this way, the current is limited to VSC/Rsen until the short is removed or the time of T_{SC} = 450µs is completed. Pulling the EN/MODE pin low (<0.4V, typ) is required to reset this short circuit latch-off mode. The delay of T_{SC} = 450µs helps to prevent nuisance latch-off during a momentary short on the output.

Standby Mode

In stand-by mode the power path is protected from shorts and overloads by the current limit defined as V_{LIM1} = 85mV in the electrical characteristics table. When this current limit is tripped, the current is limited to V_{LIM1}/R_{SEN} by controlling the pass FET. If the short persists for T_{LIM1} > 900µs the pass FET will be latched off. In this way, the current is limited to V_{LIM1}/R_{SEN} until the short is removed or the time of T_{LIM1} = 900µs is completed. Pulling the EN/MODE pin low (<0.4V, typ) is required to reset this latch-off mode.

Start-up Stand-bye Mode

During start-up in stand-by mode, the current limit is defined by V_{LIM2} = 100mV in the electrical characteristics table, for the first T_{LIM2} = 3.6ms. The current is limited to V_{LIM2}/R_{SEN}, for this period . Once the T_{LIM2} = 3.6ms timer has finished, the current limit is reduced to V_{LIM1} = 85mV . For the first T_{LIM2} = 3.6ms of the start-up, the latch-off feature is not enabled, however the current will always be limited to V_{LIM2}/R_{SEN}. This allows the part to start-up normally. If the current limit is still tripped at the end of T_{LIM2} = 3.6ms, the T_{LIM1} = 900µs timer is started. Once the T_{LIM1}= 900µs time has expired, the pass FET is latched off. This gives a total current-limited time of T_{LIM1}+ T_{LIM2} = 4.5ms, in cases where the LM3017 is started into a short circuit at the output.

Start-up Boost Mode

During start-up in boost mode, the current limit is defined by V_{LIM2} = 100mV (typ) in the electrical characteristics table, for the first T_{LIM2} = 3.6ms. The current is limited to V_{LIM2}/R_{SEN}, for this period . Once the T_{LIM2} = 3.6ms timer has finished, the current limit is increased to V_{SC} = 200mV. For the first T_{LIM2} = 3.6ms of the start-up, the latch-off feature is not enabled, however the current will always be limited to V_{LIM2}/R_{SEN}. This allows the part to start-up normally. If the current limit is still tripped at the end of T_{LIM2} = 3.6ms, the T_{SC} = 450µs timer is started. Once the T_{SC} = 450µs time has expired, the pass FET is latched off. This gives a total current-limited time of T_{SC} + T_{LIM2} = 4.05ms, in cases where the LM3017 is started into a short circuit at the output.

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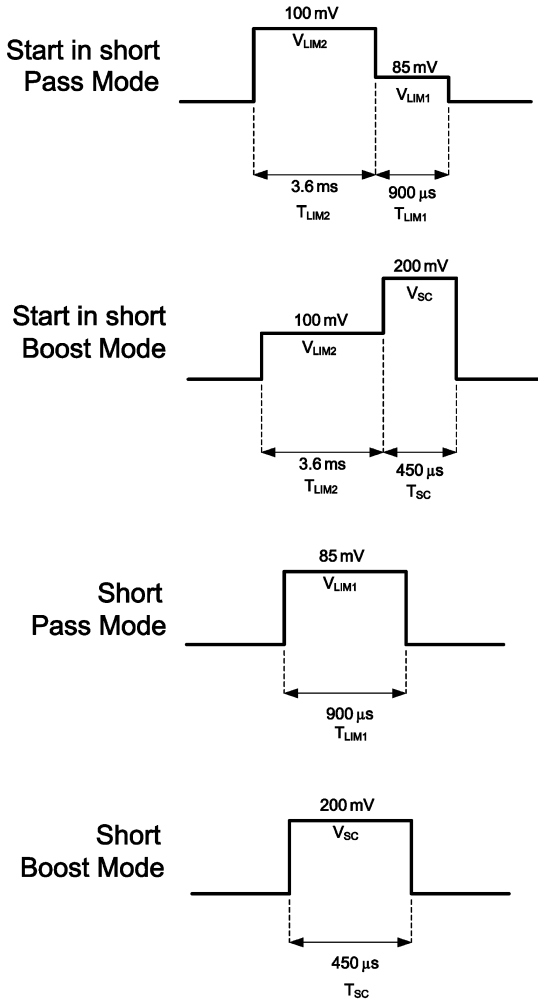

Figure 3. Current Limit / Short Circuit protection

OVER VOLTAGE PROTECTION

The LM3017 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at anytime the voltage at the feedback pin rises to V_{FB} + V_{OVP}, OVP is triggered. See the electrical characteristics section for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin (DR) to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3017 will begin switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See the electrical characteristics section for limits on $V_{OVP(HYS)}$.

SLOPE COMPENSATION RAMP

The LM3017 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch, simpler control loop characteristics and excellent line and load transient response. However there is a natural instability that will occur for duty cycles, D, greater than 50% if additional slope compensation is not addressed as described below.

$$M_C > M_2 / 2 \quad (4)$$

For the boost topology:

$$M_1 = [V_{IN} / L] \times R_{SEN} \times A \quad (5)$$

$$M_2 = [(V_{OUT} - V_{IN}) / L] \times R_{SEN} \times A \quad (6)$$

Where:

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- $\mathbf{M_C}$ is the slope of the compensation ramp.
- $\mathbf{M_1}$ is the slope of the inductor current during the ON time.
- $\mathbf{M_2}$ is the slope of the inductor current during the OFF time.
- $\mathbf{R_{SEN}}$ is the sensing resistor value.
- $\mathbf{V_{OUT}}$ represents the output voltage.
- $\mathbf{V_{IN}}$ represents the input voltage.
- **A** is equal to 0.86 and it is the internal sensing amplification of the LM3017.

The compensation ramp has been added internally in the LM3017. The slope of this compensation ramp has been selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using the formula:

$$M_C = V_{SL} \times f_S \quad (7)$$

In the above equation, V_{SL} is the amplitude of the internal compensation ramp and f_S is the controller's switching frequency. Limits for V_{SL} have been specified in the electrical characteristics section.

In order to provide the user additional flexibility, a patented scheme has been implemented inside the IC to increase the slope of the compensation ramp externally, if the need arises. Adding a single external resistor, R_S (as shown in Figure 5) increases the amplitude of the compensation ramp as shown in Figure 4.

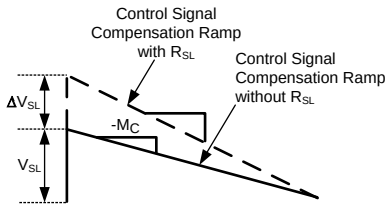

Figure 4. Additional Slope Compensation Added Using External Resistor R_S

Where,

$$\Delta V_{SL} = K \times R_S \quad (8)$$

K = 40 µA typically and changes slightly as the switching frequency changes.

A more general equation for the slope compensation ramp, M_C, is shown below to incluse ΔV_{SL} cause by the resistor R_S.

$$M_C = (V_{SL} + \Delta V_{SL}) \times f_S \quad (9)$$

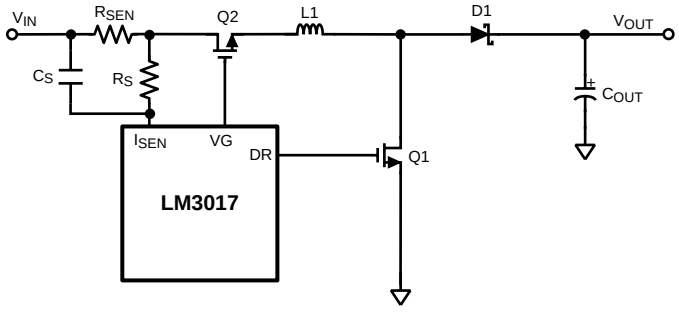

Figure 5. Increasing the Slope of the Compensation Ramp

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Application Circuits

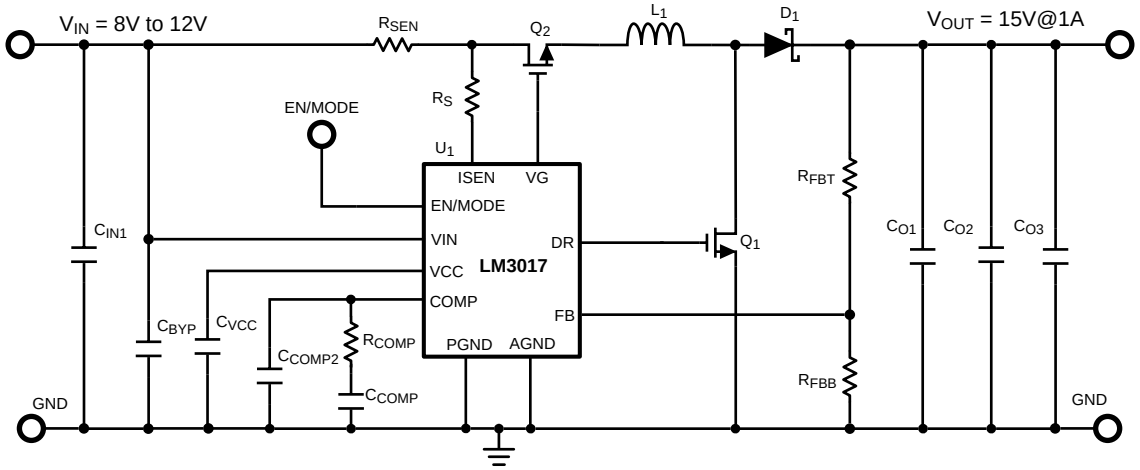

Figure 6. Typical High Efficiency Step-Up (Boost) Converter

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Table 2. Bill of Materials (BOM)

Designation	Description	Size	Manufacturer Part #	Vendor
C_{IN1}	Cap 22µF 25V X5R	1206	GRM31CR61E226KE15L	Murata
C_{O1},C_{O2}, C_{O3}	Cap 22µF 25V X5R	1206	GRM31CR61E226KE15L	Murata
C_{COMP}	Cap 0.022µF	0603		
C_{COMP2}	Cap 1000pF	0603		
C_{BYP}	Cap 0.1µF 25V X7R	0603	06033C104KAT2A	AVX
C_{VCC}	Cap 0.47µF 16V X7R	0805	C2012X7R1C474K	TDK
R_{COMP}	RES, 10k ohm, 1%, 0.1W	0603	CRCW060310K0FKEA	Vishay
R_{FBT}	RES, 21.5k ohm, 1%, 0.1W	0603	CRCW060321K5FKEA	Vishay
R_{FBB}	RES, 2k ohm, 1%, 0.1W	0603	CRCW06032K00FKEA	Vishay
R_S	RES, 100 ohm, 1%, 0.1W	0603	CRCW0603100RFKEA	Vishay
R_{SEN}	RES, 0.03 ohm, 1%, 1W	1206	WSLP1206R0300FEA	Vishay
Q_1	NexFET™ N-CH, 25V, 60A, $R_{DS(on)}$= 4.4mohm	8-SON	CSD16323Q3	TI
Q_2	NexFET™ N-CH, 25V, 60A, $R_{DS(on)}$= 4.3mohm	8-SON	CSD16340Q3	TI
D_1	Diode Schottky, 30V, 2A	SMB	20BQ030TRPBF	Vishay
L_1	Shielded Inductor, 2.2µH, 3.4A	4.45mm L x 4.06mm W x 1.85mm H	MPI4040R3	Cooper
U_1	LM3017			TI

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3017LE/NOPB	PREVIEW	WQFN	NKL	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-NOTCALC	-40 to 125	SK6B	
LM3017LEX/NOPB	PREVIEW	WQFN	NKL	10	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-NOTCALC	-40 to 125	SK6B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

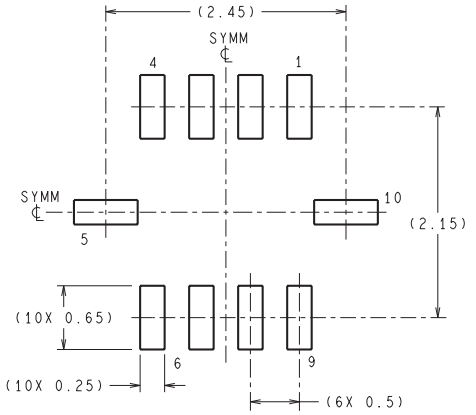
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

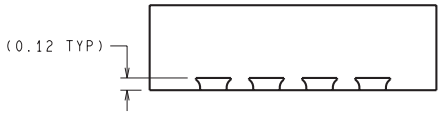
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

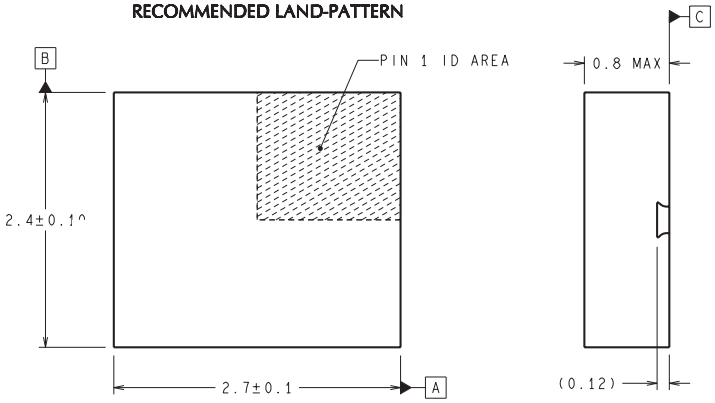
NKL0010A



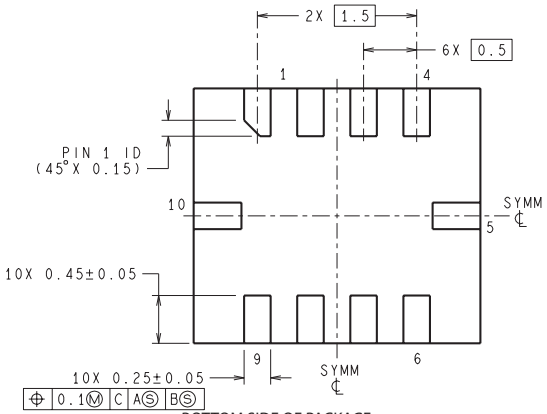
RECOMMENDED LAND-PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN ( ) FOR REFERENCE ONLY





TOP SIDE OF PACKAGE



BOTTOM SIDE OF PACKAGE

LEK10A (Rev A)

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