

# LMV611 Single/LMV612 Dual/LMV614 Quad 1.4 MHz, Low Power General Purpose, 1.8V Operational Amplifiers

Check for Samples: [LMV611](#), [LMV612](#), [LMV614](#)

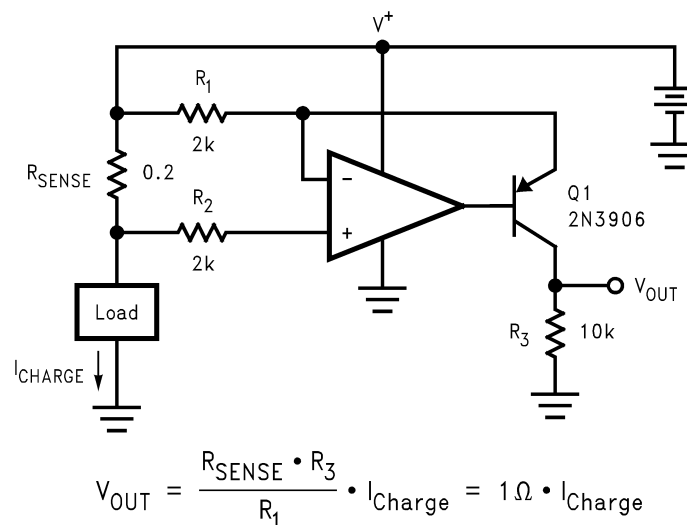
## FEATURES

- (Typical 1.8V Supply Values; Unless Otherwise Noted)
- Ensured 1.8V, 2.7V and 5V Specifications
- Output Swing
  - w/600Ω Load 80mV from Rail
  - w/2kΩ Load 30mV from Rail
- $V_{CM}$  200mV Beyond Rails
- Supply Current (Per Channel) 100μA
- Gain Bandwidth Product 1.4MHz
- Maximum  $V_{OS}$  4.0mV
- Temperature Range –40°C to 125°C

## APPLICATIONS

- Consumer Communication
- Consumer Computing
- PDAs
- Audio Pre-Amp
- Portable/Battery-Powered Electronic Equipment
- Supply Current Monitoring
- Battery Monitoring

## Typical Application



## DESCRIPTION

The LMV611/LMV612/LMV614 are single, dual, and quad low voltage, low power Operational Amplifiers. They are designed specifically for low voltage general purpose applications. Other important product characteristics are, rail-to-rail input/output, low supply voltage of 1.8V and wide temperature range. The LMV611/LMV612/LMV614 input common mode extends 200mV beyond the supplies and the output can swing rail-to-rail unloaded and within 30mV with 2kohm load at 1.8V supply. The LMV611/2/4 achieves a gain bandwidth of 1.4MHz while drawing 100 uA (typ) quiescent current.

The industrial-plus temperature range of –40°C to 125°C allows the LMV611/LMV612/LMV614 to accommodate a broad range of extended environment applications.

The LMV611 is offered in the tiny 5-Pin SC70 package, the LMV612 in space saving 8-Pin VSSOP and SOIC, and the LMV614 in 14-Pin TSSOP and SOIC. These small package amplifiers offer an ideal solution for applications requiring minimum PCB footprint. Applications with area constrained PC board requirements include portable and battery operated electronics.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

ESD Tolerance <sup>(3)</sup>	Machine Model	200V
	Human Body Model	2000V
Supply Voltage (V <sup>+</sup> -V <sup>-</sup> )		6V
Differential Input Voltage		± Supply Voltage
Voltage at Input/Output Pins		V <sup>+</sup> +0.3V, V <sup>-</sup> -0.3V
Storage Temperature Range		-65°C to 150°C
Junction Temperature <sup>(4)</sup>		150°C
For soldering specifications see product folder at <a href="http://www.ti.com">www.ti.com</a> and <a href="#">SNOA549</a>		

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (4) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub> and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a PC Board.

**Operating Ratings<sup>(1)</sup>**

Supply Voltage Range		1.8V to 5.5V
Temperature Range		-40°C to 125°C
Thermal Resistance (θ <sub>JA</sub> )	5-Pin SC70	414°C/W
	5-Pin SOT-23	265°C/W
	8-Pin VSSOP	235°C/W
	8-Pin SOIC	175°C/W
	14-Pin TSSOP	155°C/W
	14-Pin SOIC	127°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

## 1.8V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 1.8\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See <sup>(1)</sup>

Symbol	Parameter	Condition	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units	
$V_{\text{OS}}$	Input Offset Voltage	LMV611 (Single)		1	4	mV	
		LMV612 (Dual) LMV614 (Quad)		1	5.5	mV	
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift			5.5		$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input Bias Current			15		nA	
$I_{\text{OS}}$	Input Offset Current			13		nA	
$I_S$	Supply Current (per channel)			103	185	$\mu\text{A}$	
CMRR	Common Mode Rejection Ratio	LMV611, $0 \leq V_{\text{CM}} \leq 0.6\text{V}$ $1.4\text{V} \leq V_{\text{CM}} \leq 1.8\text{V}$ <sup>(4)</sup>	60	78		dB	
		LMV612 and LMV614 $0 \leq V_{\text{CM}} \leq 0.6\text{V}$ $1.4\text{V} \leq V_{\text{CM}} \leq 1.8\text{V}$ <sup>(4)</sup>	55	76			
		$-0.2\text{V} \leq V_{\text{CM}} \leq 0\text{V}$ $1.8\text{V} \leq V_{\text{CM}} \leq 2.0\text{V}$	50	72			
PSRR	Power Supply Rejection Ratio	$1.8\text{V} \leq V^+ \leq 5\text{V}$		100		dB	
CMVR	Input Common-Mode Voltage Range	For CMRR Range $\geq 50\text{dB}$	$T_A = 25^\circ\text{C}$	$V^- - 0.2$	-0.2 to 2.1	$V^+ + 0.2$	V
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	$V^-$		$V^+$	
			$T_A = 125^\circ\text{C}$	$V^- + 0.2$		$V^+ - 0.2$	
$A_V$	Large Signal Voltage Gain LMV611 (Single)	$R_L = 600\Omega$ to $0.9\text{V}$ , $V_O = 0.2\text{V}$ to $1.6\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	77	101		dB	
		$R_L = 2\text{k}\Omega$ to $0.9\text{V}$ , $V_O = 0.2\text{V}$ to $1.6\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	80	105			
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	$R_L = 600\Omega$ to $0.9\text{V}$ , $V_O = 0.2\text{V}$ to $1.6\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	75	90		dB	
		$R_L = 2\text{k}\Omega$ to $0.9\text{V}$ , $V_O = 0.2\text{V}$ to $1.6\text{V}$ , $V_{\text{CM}} = 0.5\text{V}$	78	100			
$V_O$	Output Swing	$R_L = 600\Omega$ to $0.9\text{V}$ $V_{\text{IN}} = \pm 100\text{mV}$	1.65	1.72		V	
					0.077		0.105
		$R_L = 2\text{k}\Omega$ to $0.9\text{V}$ $V_{\text{IN}} = \pm 100\text{mV}$	1.75	1.77			0.024
$I_O$	Output Short Circuit Current <sup>(5)</sup>	Sourcing, $V_O = 0\text{V}$ $V_{\text{IN}} = 100\text{mV}$		8		mA	
		Sinking, $V_O = 1.8\text{V}$ $V_{\text{IN}} = -100\text{mV}$		9			

- Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- All limits are specified by testing or statistical analysis.
- Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- For specified temperature ranges, see Input Common-Mode Voltage Range specifications.
- Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ . Output currents in excess of  $45\text{mA}$  over long term may adversely affect reliability.

## 1.8V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 1.8\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See <sup>(1)</sup>

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
SR	Slew Rate	See <sup>(4)</sup>		0.35		V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product			1.4		MHz
$\Phi_m$	Phase Margin			67		deg
$G_m$	Gain Margin			7		dB
$e_n$	Input-Referred Voltage Noise	$f = 10\text{ kHz}$ , $V_{\text{CM}} = 0.5\text{V}$		60		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 10\text{ kHz}$		0.08		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$ , $A_V = +1$ $R_L = 600\Omega$ , $V_{\text{IN}} = 1\text{ V}_{\text{PP}}$		0.023		%
	Amp-to-Amp Isolation	See <sup>(5)</sup>		123		dB

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) All limits are specified by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) Connected as voltage follower with input step from  $V^-$  to  $V^+$ . Number specified is the slower of the positive and negative slew rates.
- (5) Input referred,  $R_L = 100\text{k}\Omega$  connected to  $V^+/2$ . Each amp excited in turn with  $1\text{ kHz}$  to produce  $V_O = 3V_{\text{PP}}$  (For Supply Voltages  $< 3\text{V}$ ,  $V_O = V^+$ ).

## 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See <sup>(1)</sup>

Symbol	Parameter	Condition	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
$V_{\text{OS}}$	Input Offset Voltage	LMV611 (Single)		1	4	mV
		LMV612 (Dual)		1	5.5	mV
		LMV614 (Quad)				
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift			5.5		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current			15		nA
$I_{\text{OS}}$	Input Offset Current			8		nA
$I_S$	Supply Current (per channel)			105	190	$\mu\text{A}$
CMRR	Common Mode Rejection Ratio	LMV611, $0 \leq V_{\text{CM}} \leq 1.5\text{V}$ $2.3\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$ <sup>(4)</sup>	60	81		dB
		LMV612 and LMV614 $0 \leq V_{\text{CM}} \leq 1.5\text{V}$ $2.3\text{V} \leq V_{\text{CM}} \leq 2.7\text{V}$ <sup>(4)</sup>	55	80		
		$-0.2\text{V} \leq V_{\text{CM}} \leq 0\text{V}$ $2.7\text{V} \leq V_{\text{CM}} \leq 2.9\text{V}$	50	74		
PSRR	Power Supply Rejection Ratio	$1.8\text{V} \leq V^+ \leq 5\text{V}$ $V_{\text{CM}} = 0.5\text{V}$		100		dB

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) All limits are specified by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) For specified temperature ranges, see Input Common-Mode Voltage Range specifications.

## 2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See<sup>(1)</sup>

Symbol	Parameter	Condition	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units	
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR Range $\geq 50\text{dB}$	$T_A = 25^\circ\text{C}$	$V^- - 0.2$	-0.2 to 3.0	$V^+ + 0.2$	V
			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$	$V^-$		$V^+$	
			$T_A = 125^\circ\text{C}$	$V^- + 0.2$		$V^+ - 0.2$	
$A_V$	Large Signal Voltage Gain LMV611 (Single)	$R_L = 600\Omega$ to $1.35\text{V}$ , $V_O = 0.2\text{V}$ to $2.5\text{V}$	87	104		dB	
		$R_L = 2\text{k}\Omega$ to $1.35\text{V}$ , $V_O = 0.2\text{V}$ to $2.5\text{V}$	92	110			
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	$R_L = 600\Omega$ to $1.35\text{V}$ , $V_O = 0.2\text{V}$ to $2.5\text{V}$	78	90		dB	
		$R_L = 2\text{k}\Omega$ to $1.35\text{V}$ , $V_O = 0.2\text{V}$ to $2.5\text{V}$	81	100			
$V_O$	Output Swing	$R_L = 600\Omega$ to $1.35\text{V}$ $V_{\text{IN}} = \pm 100\text{mV}$	2.55	2.62		V	
		$R_L = 2\text{k}\Omega$ to $1.35\text{V}$ $V_{\text{IN}} = \pm 100\text{mV}$	2.65	2.675	0.110		
		$R_L = 2\text{k}\Omega$ to $1.35\text{V}$ $V_{\text{IN}} = \pm 100\text{mV}$		0.025	0.04		
$I_O$	Output Short Circuit Current <sup>(5)</sup>	Sourcing, $V_O = 0\text{V}$ $V_{\text{IN}} = 100\text{mV}$		30		mA	
		Sinking, $V_O = 0\text{V}$ $V_{\text{IN}} = -100\text{mV}$		25			

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of  $150^\circ\text{C}$ . Output currents in excess of  $45\text{mA}$  over long term may adversely affect reliability.

## 2.7V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.0\text{V}$ ,  $V_O = 1.35\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See<sup>(1)</sup>

Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
SR	Slew Rate	See <sup>(4)</sup>		0.4		$\text{V}/\mu\text{s}$
GBW	Gain-Bandwidth Product			1.4		MHz
$\Phi_m$	Phase Margin			70		deg
$G_m$	Gain Margin			7.5		dB
$e_n$	Input-Referred Voltage Noise	$f = 10\text{kHz}$ , $V_{\text{CM}} = 0.5\text{V}$		57		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 10\text{kHz}$		0.08		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = +1$ $R_L = 600\Omega$ , $V_{\text{IN}} = 1V_{\text{PP}}$		0.022		%
	Amp-to-Amp Isolation	See <sup>(5)</sup>		123		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) All limits are specified by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) Connected as voltage follower with input step from  $V^-$  to  $V^+$ . Number specified is the slower of the positive and negative slew rates.

(5) Input referred,  $R_L = 100\text{k}\Omega$  connected to  $V^+/2$ . Each amp excited in turn with  $1\text{kHz}$  to produce  $V_O = 3V_{\text{PP}}$  (For Supply Voltages  $< 3\text{V}$ ,  $V_O = V^+$ ).

### 5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See <sup>(1)</sup>

Symbol	Parameter	Condition	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units	
V <sub>OS</sub>	Input Offset Voltage	LMV611 (Single)		1	4	mV	
		LMV612 (Dual) LMV614 (Quad)		1	5.5	mV	
TCV <sub>OS</sub>	Input Offset Voltage Average Drift			5.5		$\mu\text{V}/^\circ\text{C}$	
I <sub>B</sub>	Input Bias Current			14	35	nA	
I <sub>OS</sub>	Input Offset Current			9		nA	
I <sub>S</sub>	Supply Current (per channel)			116	210	$\mu\text{A}$	
CMRR	Common Mode Rejection Ratio	$0 \leq V_{CM} \leq 3.8\text{V}$ $4.6\text{V} \leq V_{CM} \leq 5.0\text{V}$ <sup>(4)</sup>	60	86		dB	
		$-0.2\text{V} \leq V_{CM} \leq 0\text{V}$ $5.0\text{V} \leq V_{CM} \leq 5.2\text{V}$	50	78			
PSRR	Power Supply Rejection Ratio	$1.8\text{V} \leq V^+ \leq 5\text{V}$ $V_{CM} = 0.5\text{V}$		100		dB	
CMVR	Input Common-Mode Voltage Range	For CMRR Range $\geq 50\text{dB}$	T <sub>A</sub> = 25°C	V <sup>-</sup> -0.2	-0.2 to 5.3	V <sup>+</sup> +0.2	V
			T <sub>A</sub> = -40°C to 85°C	V <sup>-</sup>		V <sup>+</sup>	
			T <sub>A</sub> = 125°C	V <sup>-</sup> +0.3		V <sup>+</sup> -0.3	
A <sub>V</sub>	Large Signal Voltage Gain LMV611 (Single)	R <sub>L</sub> = 600 $\Omega$ to 2.5V, V <sub>O</sub> = 0.2V to 4.8V	88	102		dB	
		R <sub>L</sub> = 2k $\Omega$ to 2.5V, V <sub>O</sub> = 0.2V to 4.8V	94	113			
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	R <sub>L</sub> = 600 $\Omega$ to 2.5V, V <sub>O</sub> = 0.2V to 4.8V	81	90		dB	
		R <sub>L</sub> = 2k $\Omega$ to 2.5V, V <sub>O</sub> = 0.2V to 4.8V	85	100			
V <sub>O</sub>	Output Swing	R <sub>L</sub> = 600 $\Omega$ to 2.5V V <sub>IN</sub> = $\pm 100\text{mV}$	4.855	4.890		V	
					0.120		0.160
		R <sub>L</sub> = 2k $\Omega$ to 2.5V V <sub>IN</sub> = $\pm 100\text{mV}$	4.945	4.967			0.037
I <sub>O</sub>	Output Short Circuit Current <sup>(5)</sup>	LMV611, Sourcing, V <sub>O</sub> = 0V V <sub>IN</sub> = 100mV		100		mA	
		Sinking, V <sub>O</sub> = 5V V <sub>IN</sub> = -100mV		65			

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) All limits are specified by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) For specified temperature ranges, see Input Common-Mode Voltage Range specifications.
- (5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

## 5V AC Electrical Characteristics

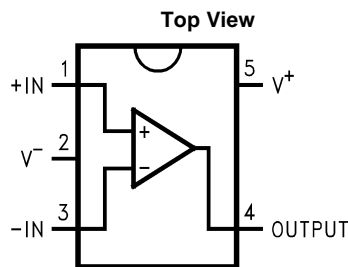
Unless otherwise specified, all limits ensured for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = 2.5\text{V}$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes. See<sup>(1)</sup>

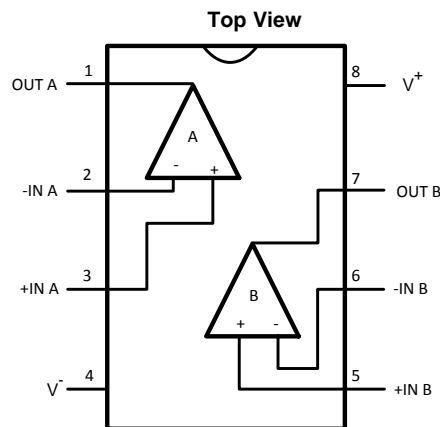
Symbol	Parameter	Conditions	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
SR	Slew Rate	See <sup>(4)</sup>		0.42		V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product			1.5		MHz
$\Phi_m$	Phase Margin			71		deg
$G_m$	Gain Margin			8		dB
$e_n$	Input-Referred Voltage Noise	$f = 10\text{ kHz}$ , $V_{CM} = 1\text{V}$		50		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 10\text{ kHz}$		0.08		pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{kHz}$ , $A_V = +1$ $R_L = 600\Omega$ , $V_O = 1\text{V}_{PP}$		0.022		%
	Amp-to-Amp Isolation	See <sup>(5)</sup>		123		dB

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) All limits are specified by testing or statistical analysis.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
- (4) Connected as voltage follower with input step from  $V^-$  to  $V^+$ . Number specified is the slower of the positive and negative slew rates.
- (5) Input referred,  $R_L = 100\text{k}\Omega$  connected to  $V^+/2$ . Each amp excited in turn with 1kHz to produce  $V_O = 3V_{PP}$  (For Supply Voltages  $< 3\text{V}$ ,  $V_O = V^+$ ).

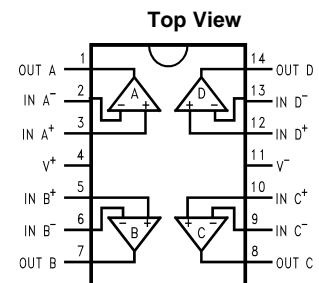
## Connection Diagrams



**Figure 1. 5-Pin SC70/SOT-23 (LMV611)**  
See Package Numbers DCK and DBV



**Figure 2. 8-Pin VSSOP/SOIC (LMV612)**  
See Package Numbers DGK and D



**Figure 3. 14-Pin TSSOP/SOIC (LMV614)**  
See Package Numbers PW and D

### Typical Performance Characteristics

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

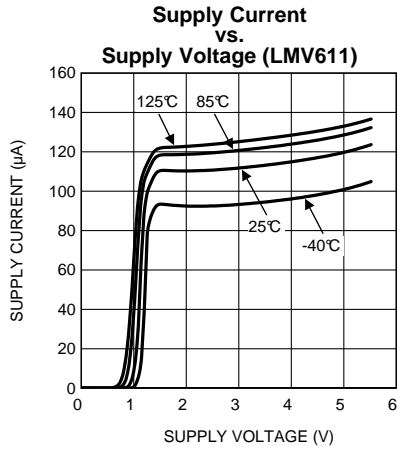


Figure 4.

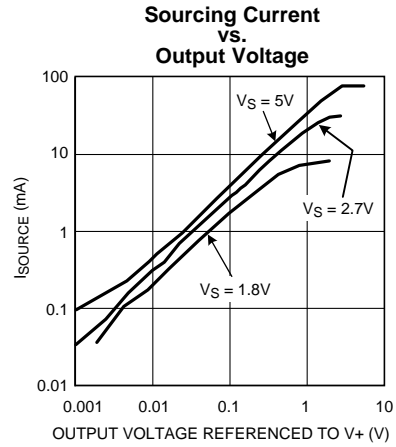


Figure 5.

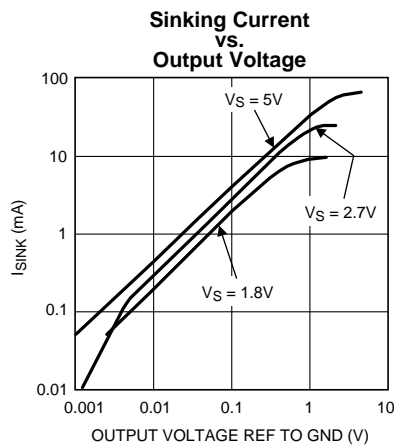


Figure 6.

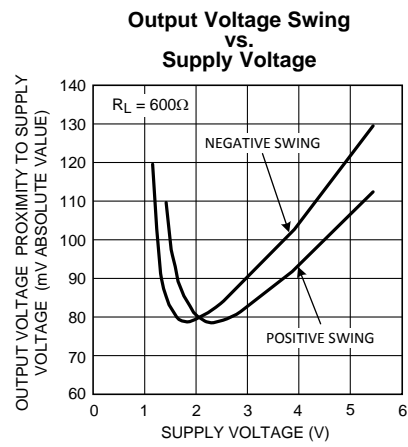


Figure 7.

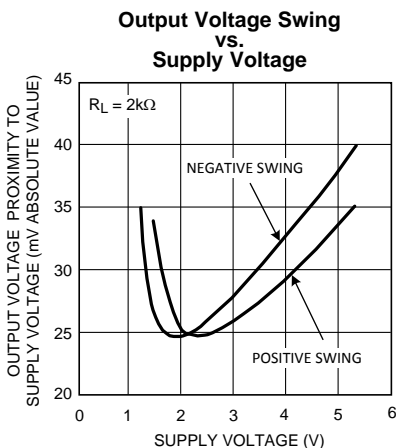


Figure 8.

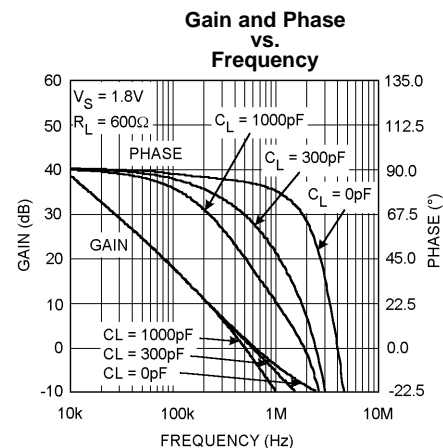


Figure 9.



Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

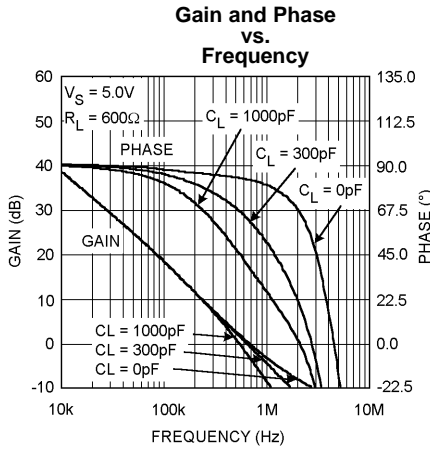


Figure 10.

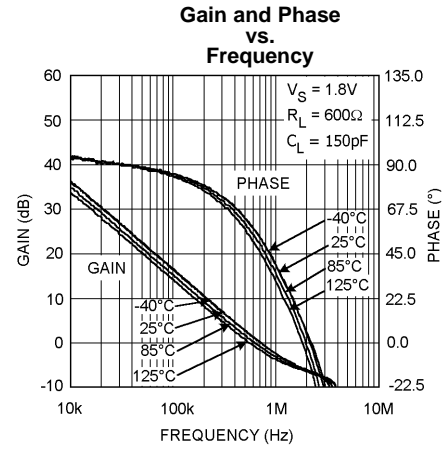


Figure 11.

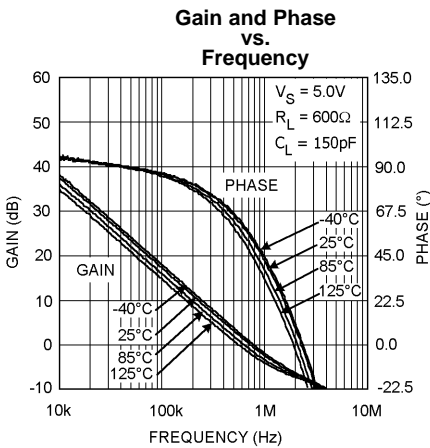


Figure 12.

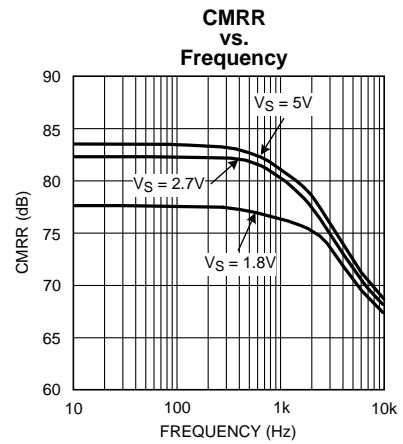


Figure 13.

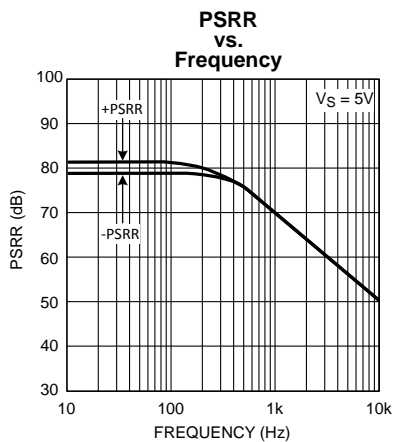


Figure 14.

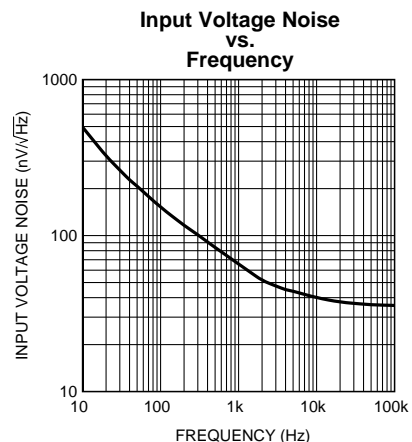


Figure 15.

**Typical Performance Characteristics (continued)**

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

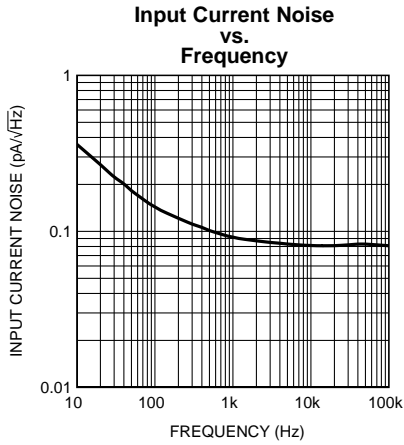


Figure 16.

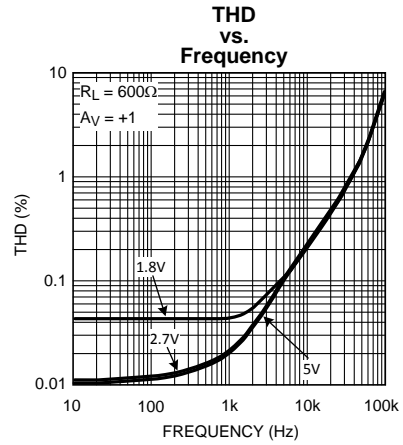


Figure 17.

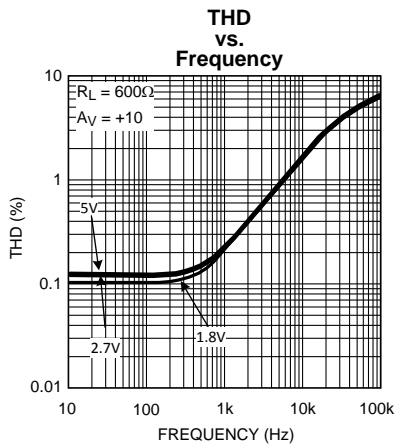


Figure 18.

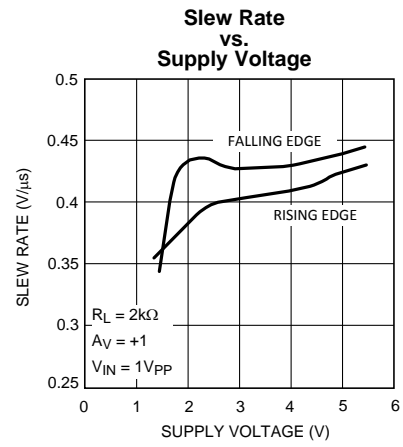


Figure 19.

**Small Signal Non-Inverting Response**

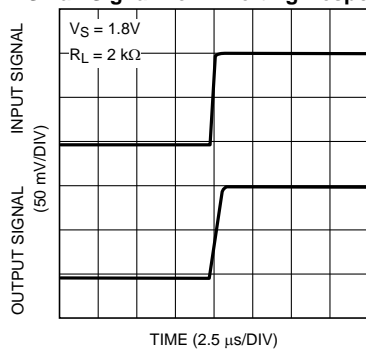


Figure 20.

**Small Signal Non-Inverting Response**

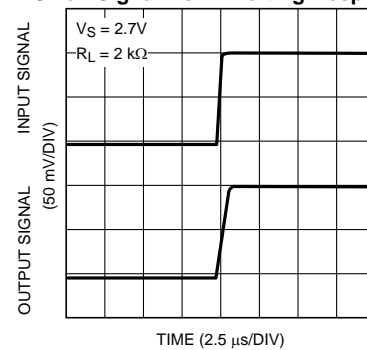


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .

Small Signal Non-Inverting Response

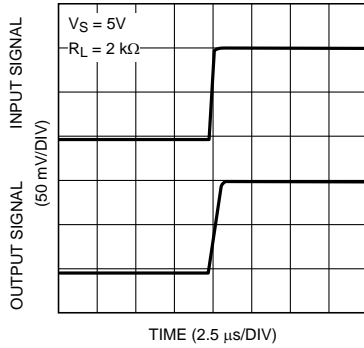


Figure 22.

Large Signal Non-Inverting Response

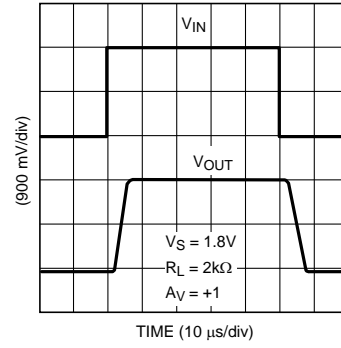


Figure 23.

Large Signal Non-Inverting Response

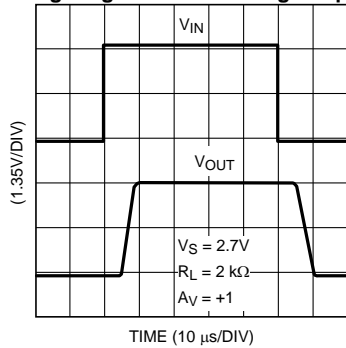


Figure 24.

Large Signal Non-Inverting Response

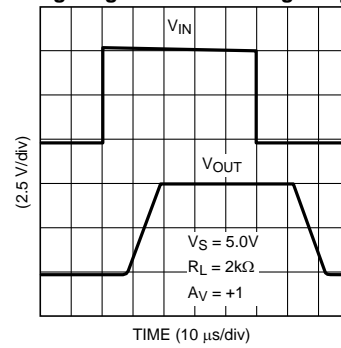


Figure 25.

Short Circuit Current vs. Temperature (Sinking)

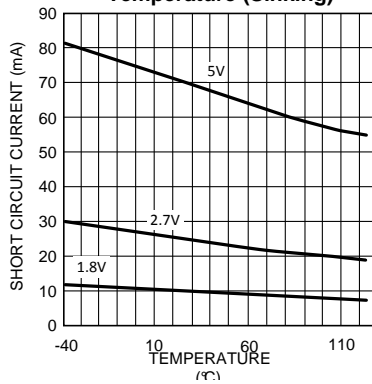


Figure 26.

Short Circuit Current vs. Temperature (Sourcing)

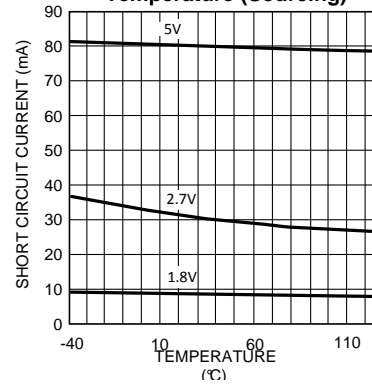
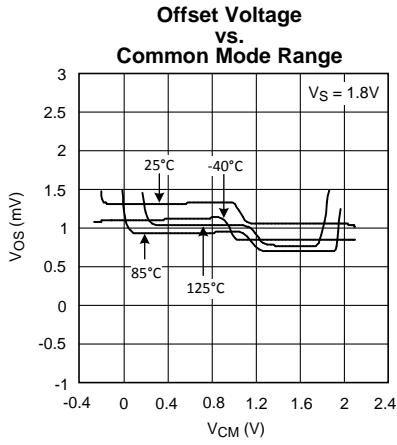


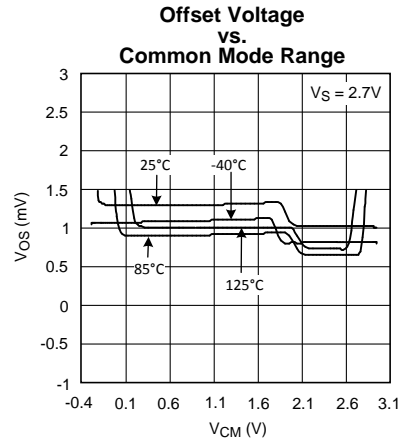
Figure 27.

**Typical Performance Characteristics (continued)**

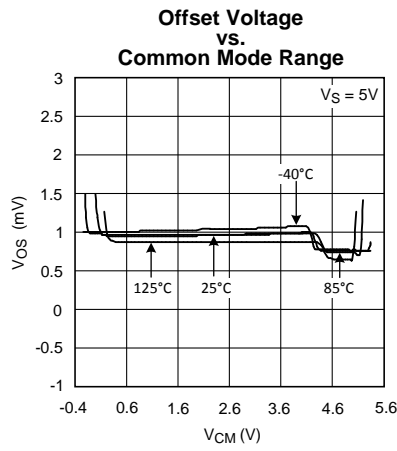
Unless otherwise specified,  $V_S = +5V$ , single supply,  $T_A = 25^\circ C$ .



**Figure 28.**



**Figure 29.**



**Figure 30.**

## APPLICATION NOTE

### INPUT AND OUTPUT STAGE

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV611/LMV612/LMV614 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near  $V^-$  and the NPN stage senses common mode voltage near  $V^+$ . The transition from the PNP stage to NPN stage occurs 1V below  $V^+$ . Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below  $V^+$ .

This  $V_{OS}$  crossover point can create problems for both DC and AC coupled signals if proper care is not taken. Large input signals that include the  $V_{OS}$  crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with  $V_S = 5V$ , a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of  $-1$  circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the  $V_{OS}$  cross-over point. For small signals, this transition in  $V_{OS}$  shows up as a  $V_{CM}$  dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the  $V_{OS}$  crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600 $\Omega$  loads. Because of the high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

### INPUT BIAS CURRENT CONSIDERATION

The LMV611/LMV612/LMV614 family has a complementary bipolar input stage. The typical input bias current ( $I_B$ ) is 15nA. The input bias current can develop a significant offset voltage. This offset is primarily due to  $I_B$  flowing through the negative feedback resistor,  $R_F$ . For example, if  $I_B$  is 50nA and  $R_F$  is 100k $\Omega$ , then an offset voltage of 5mV will develop ( $V_{OS} = I_B \times R_F$ ). Using a compensation resistor ( $R_C$ ), as shown in Figure 31, cancels this effect. But the input offset current ( $I_{OS}$ ) will still contribute to an offset voltage in the same manner.

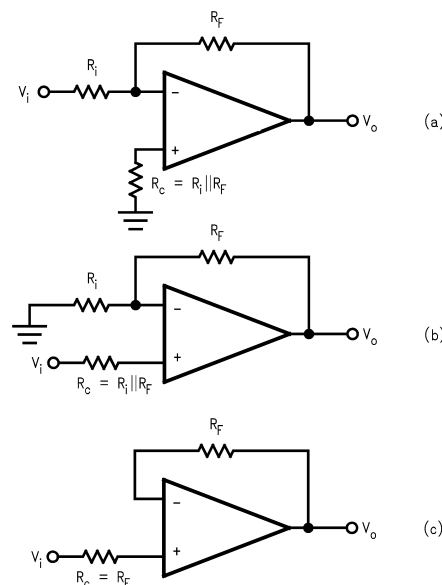


Figure 31. Canceling the Offset Voltage due to Input Bias Current

## Typical Applications

### HIGH SIDE CURRENT SENSING

The high side current sensing circuit (Figure 32) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor  $R_{SENSE}$  is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV611/LMV612/LMV614 are ideal for this application because its common mode input range goes up to the rail.

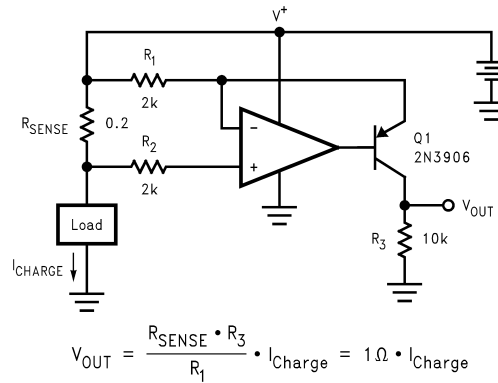


Figure 32. High Side Current Sensing

### HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the LMV611/LMV612/LMV614 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In Figure 33 the circuit is referenced to ground, while in Figure 34 the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV611/LMV612/LMV614 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage.  $R_1$  should be large enough not to load the LMV611/LMV612/LMV614.

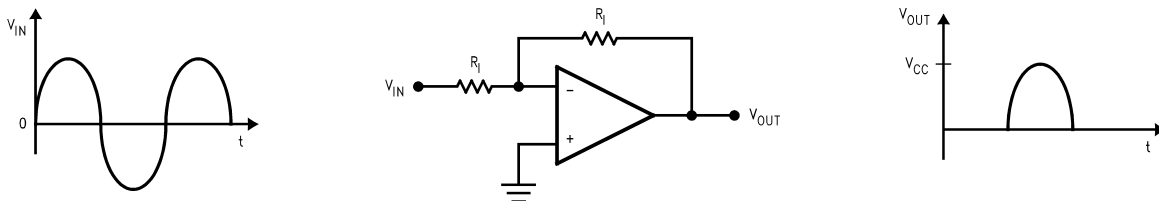


Figure 33. Half-Wave Rectifier with Rail-To-Ground Output Swing Referenced to Ground

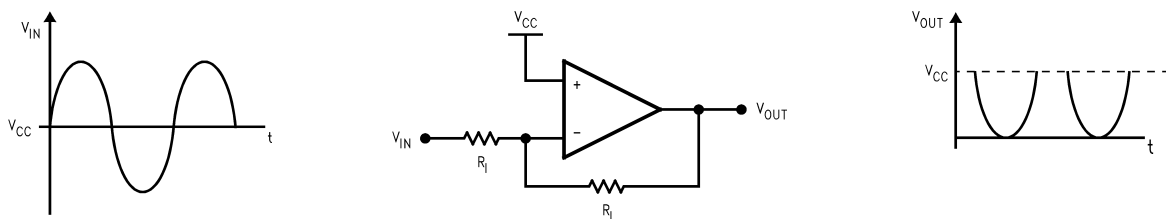


Figure 34. Half-Wave Rectifier with Negative-Going Output Referenced to  $V_{CC}$

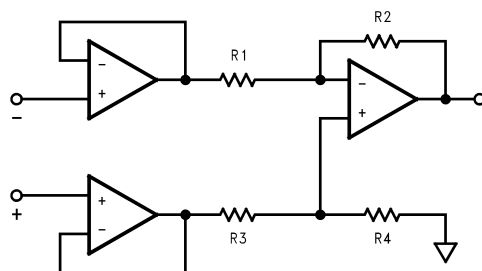
**INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL INPUT AND OUTPUT**

Some manufactures make a non-“rail-to-rail”-op amp rail-to-rail by using a resistive divider on the inputs. The resistors divide the input voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get the obtained gain, the amplifier must have a higher closed loop gain. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. The LMV611/LMV612/LMV614 is rail-to-rail and therefore doesn't have these disadvantages.

Using three of the LMV611/LMV612/LMV614 amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in [Figure 35](#).

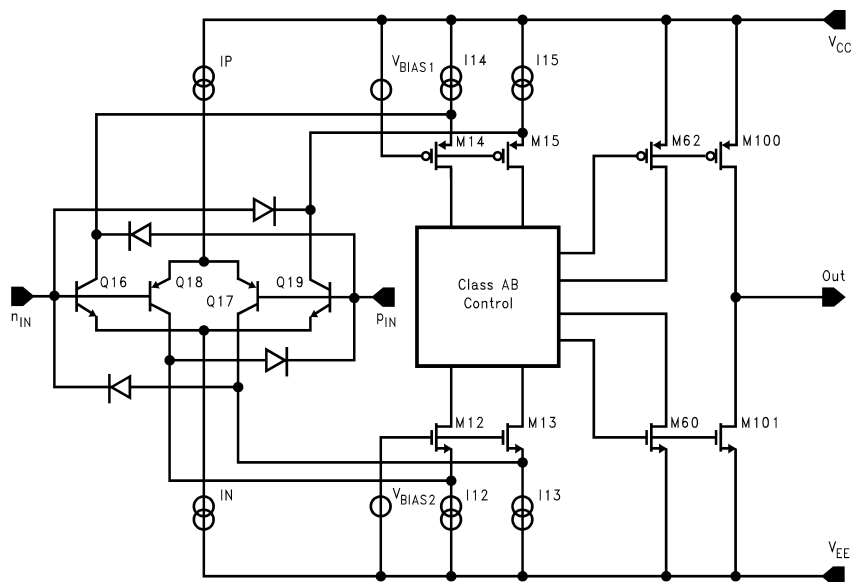
In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching  $R_1$ - $R_2$  with  $R_3$ - $R_4$ . The gain is set by the ratio of  $R_2/R_1$  and  $R_3$  should equal  $R_1$  and  $R_4$  equal  $R_2$ . With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater than the supplies or limiting will occur. For additional applications, see the following TI application reports:

- AN-29 Application Report ([SNOA624](#))
- AN-31 Application Report ([SNLA140](#))
- AN-71 Application Report ([SNOA652](#))
- AN-127 Application Report ([SNVA516](#))



**Figure 35. Rail-to-rail Instrumentation Amplifier**

**Simplified Schematic**



## REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">15</a>



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV611MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AE9A	<a href="#">Samples</a>
LMV611MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AE9A	<a href="#">Samples</a>
LMV611MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AVA	<a href="#">Samples</a>
LMV611MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AVA	<a href="#">Samples</a>
LMV612MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMV6 12MA	<a href="#">Samples</a>
LMV612MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMV6 12MA	<a href="#">Samples</a>
LMV612MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AD9A	<a href="#">Samples</a>
LMV612MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AD9A	<a href="#">Samples</a>
LMV614MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMV614MA	<a href="#">Samples</a>
LMV614MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMV614MA	<a href="#">Samples</a>
LMV614MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMV61 4MT	<a href="#">Samples</a>
LMV614MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LMV61 4MT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV611MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV611MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV612MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV612MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV612MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV614MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV614MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

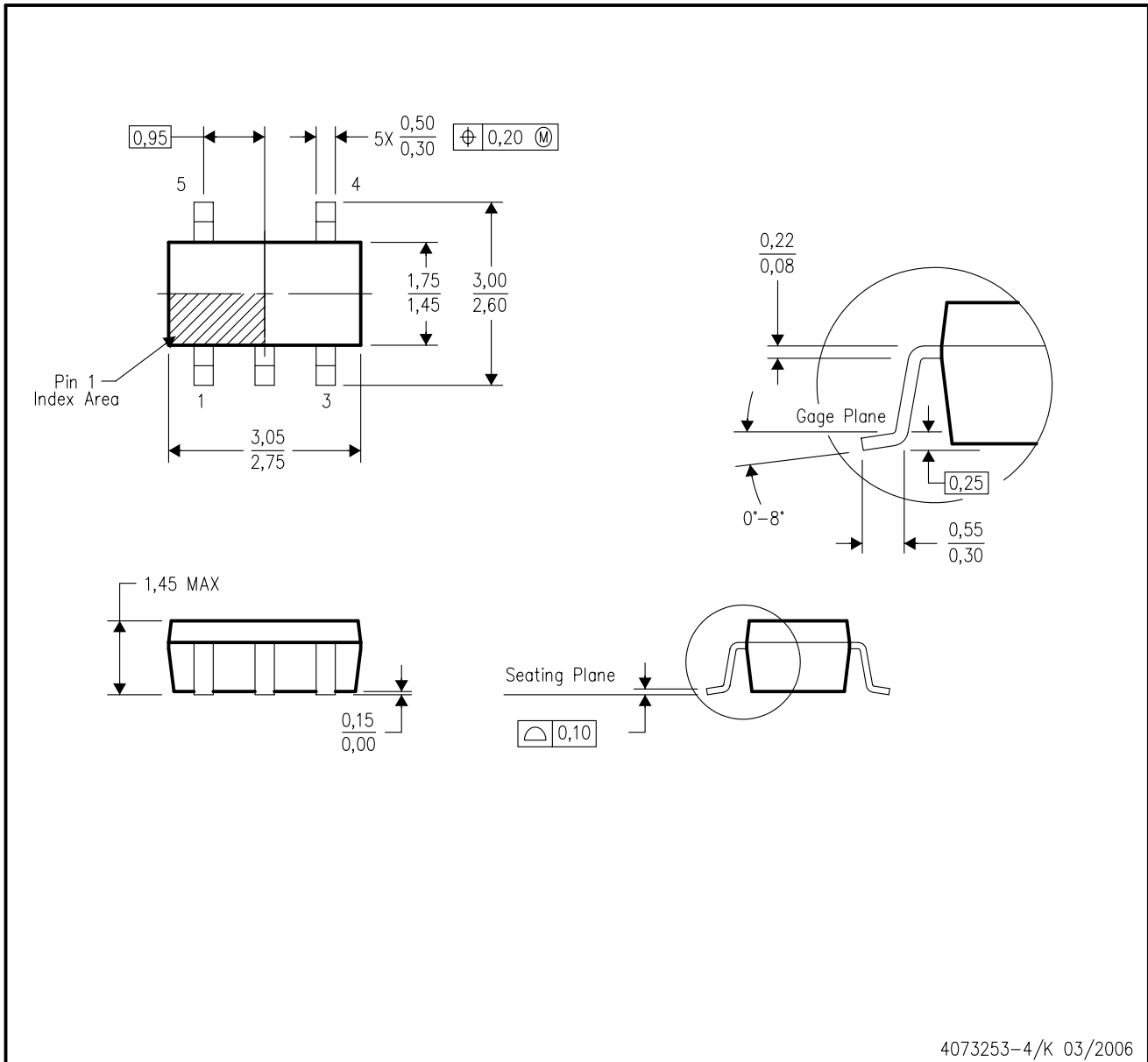
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV611MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV611MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV611MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV611MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV612MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV612MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV612MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV614MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV614MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

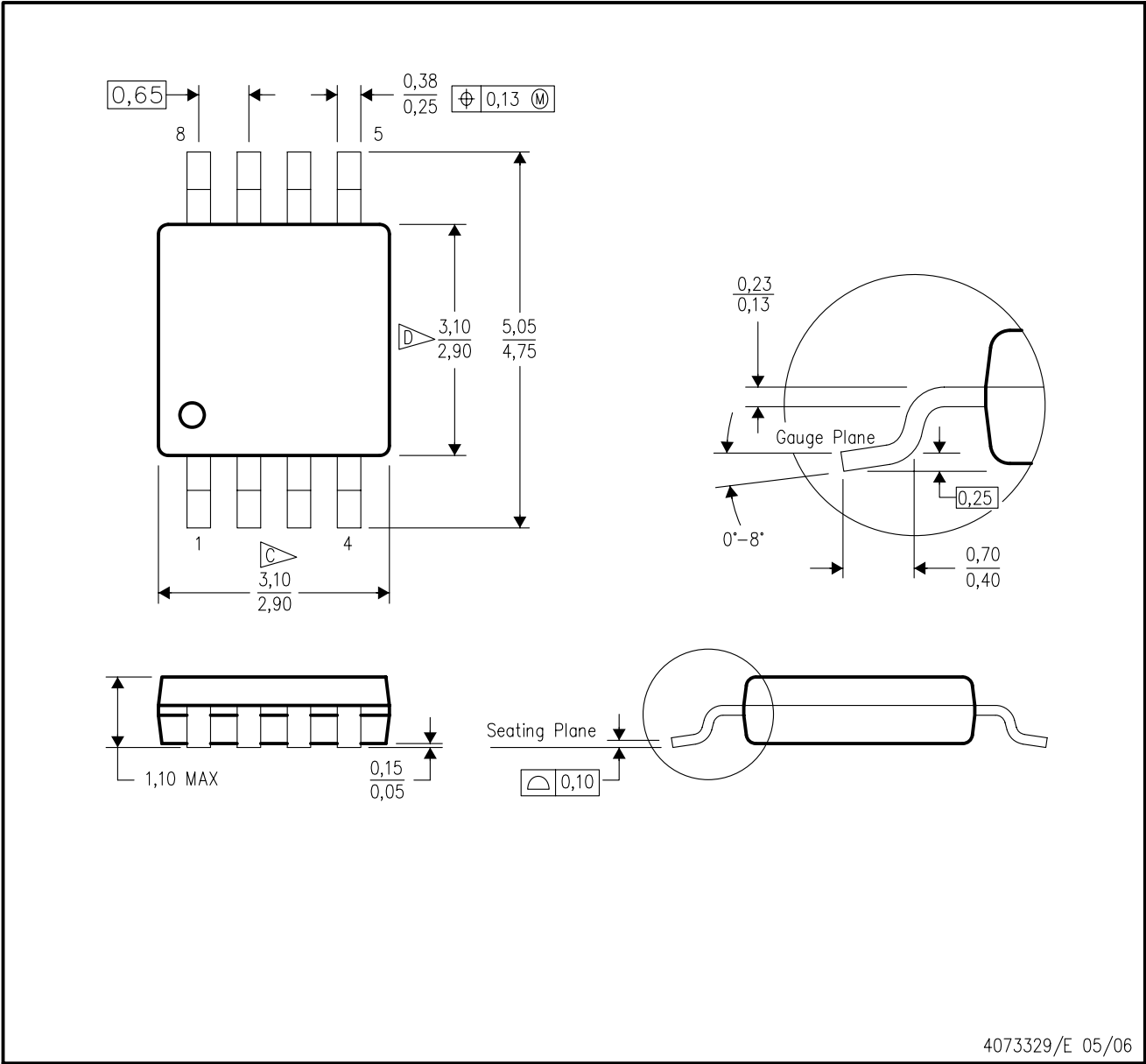
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



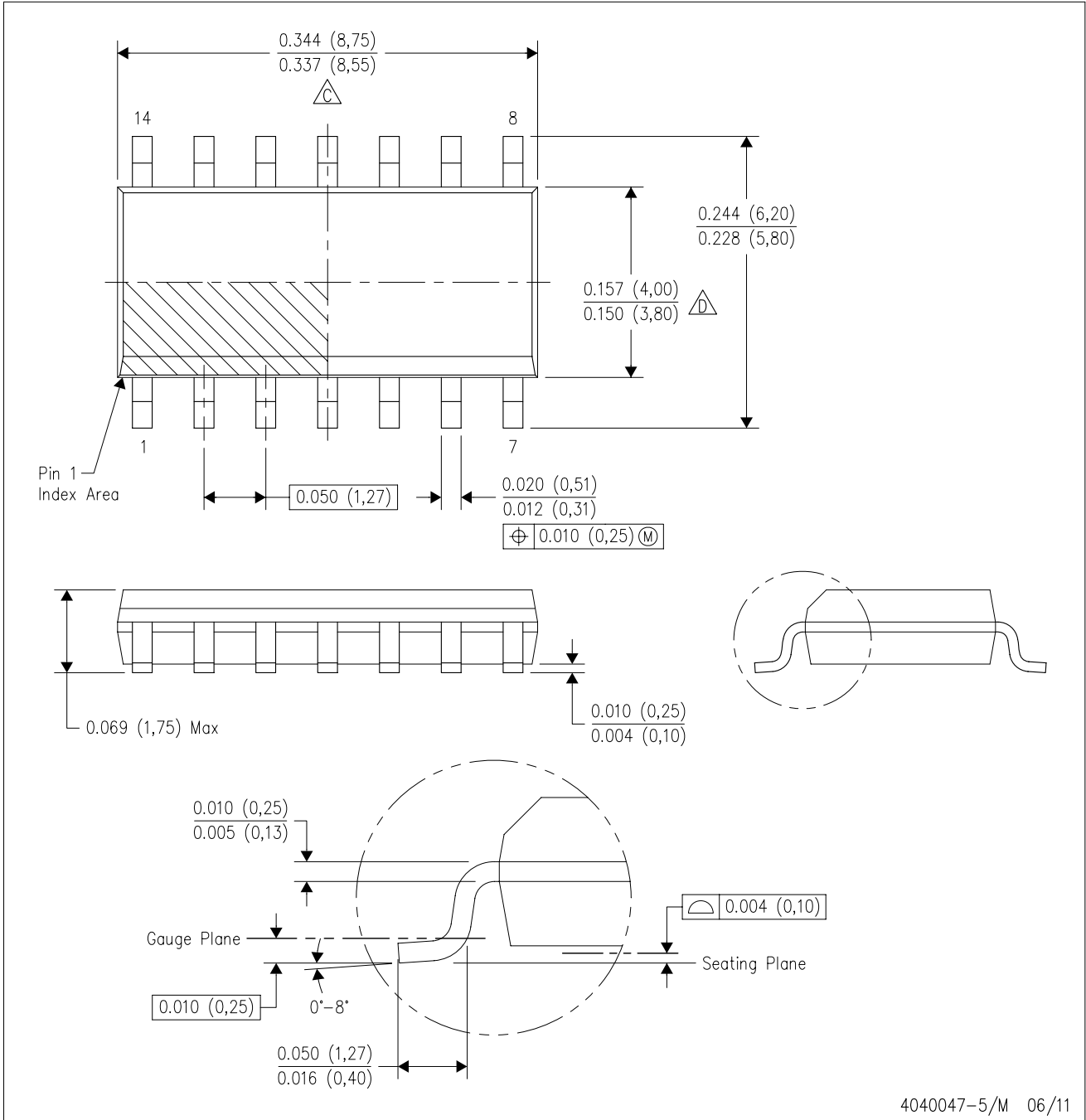
4073329/E 05/06



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



D (R-PDSO-G14)

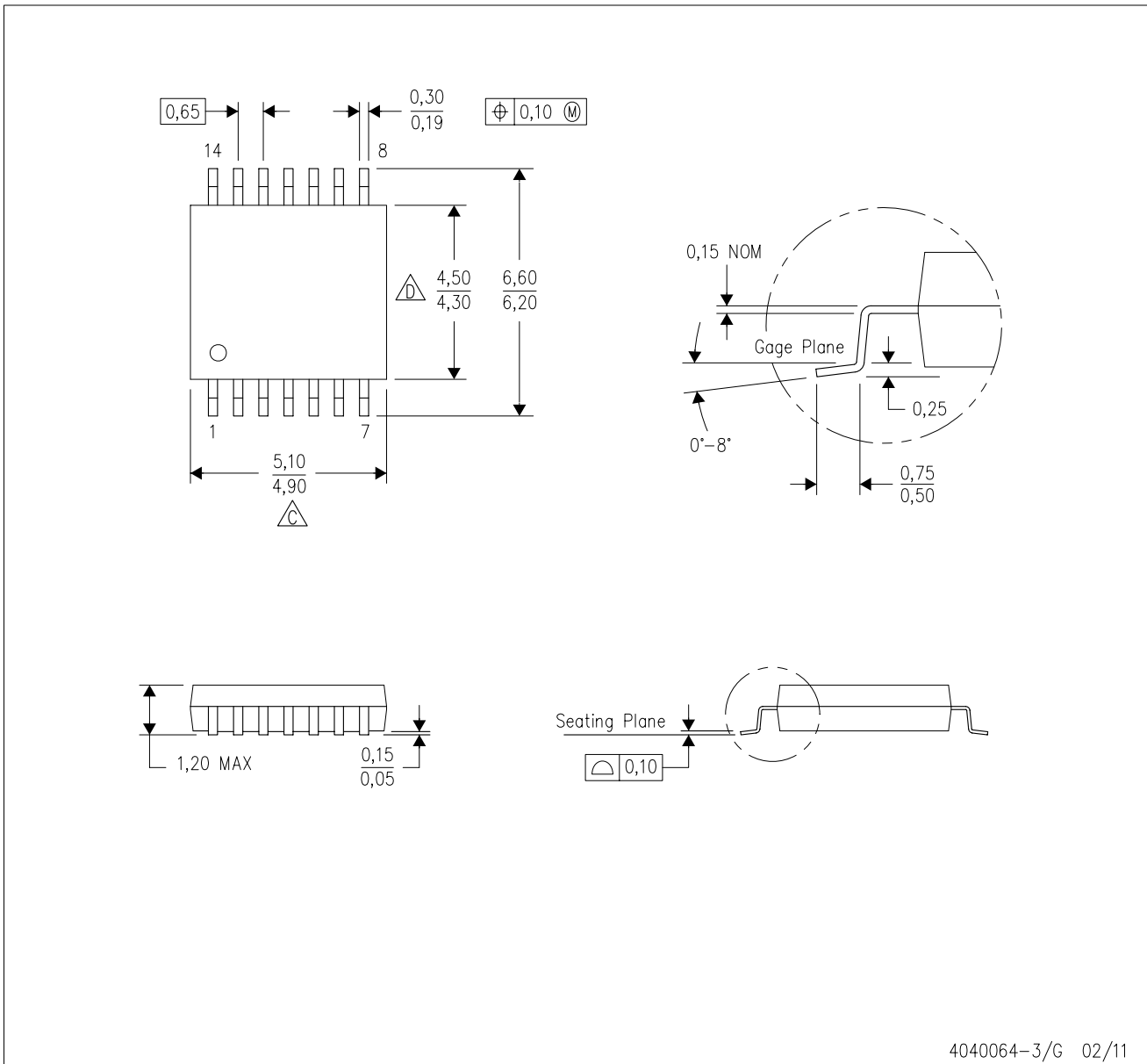
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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