

## LMH6619Q 130 MHz, 1.25 mA RRIO Operational Amplifier

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### FEATURES

- $V_S = 5V$ ,  $R_L = 1\text{ k}\Omega$ ,  $T_A = 25^\circ\text{C}$  and  $A_V = +1$ , unless otherwise specified.
- Operating voltage range 2.7V to 11V
- Supply current per channel 1.25 mA
- Small signal bandwidth 130 MHz
- Input offset voltage (limit at  $25^\circ\text{C}$ )  $\pm 0.75\text{ mV}$
- Slew rate 55 V/ $\mu\text{s}$
- Settling time to 0.1% 90 ns
- Settling time to 0.01% 120 ns
- SFDR ( $f = 100\text{ kHz}$ ,  $A_V = +1$ ,  $V_{OUT} = 2\text{ V}_{PP}$ ) 100 dBc
- 0.1 dB bandwidth ( $A_V = +2$ ) 15 MHz
- Low voltage noise 10 nV/ $\sqrt{\text{Hz}}$
- Rail-to-Rail input and output

- AEC-Q100 grade 2 qualified  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$
- Manufactured on an automotive grade flow

### APPLICATIONS

- ADC driver
- DAC buffer
- Active filters
- High speed sensor amplifier
- Current sense amplifier
- Portable video
- STB, TV video amplifier
- Automotive

### DESCRIPTION

The LMH6619Q (dual) is a 130 MHz rail-to-rail input and output amplifier designed for ease of use in a wide range of applications requiring high speed, low supply current, low noise, and the ability to drive complex ADC and video loads. The operating voltage range extends from 2.7V to 11V and the supply current is typically 1.25 mA per channel at 5V. The LMH6619Q is a member of the PowerWise<sup>®</sup> family and have an exceptional power-to-performance ratio.

The amplifier's voltage feedback design topology provides balanced inputs and high open loop gain for ease of use and accuracy in applications such as active filter design. Offset voltage is typically 0.1 mV and settling time to 0.01% is 120 ns which combined with an 100 dBc SFDR at 100 kHz makes the part suitable for use as an input buffer for popular 8-bit, 10-bit, 12-bit and 14-bit mega-sample ADCs.

The input common mode range extends 200 mV beyond the supply rails. On a single 5V supply with a ground terminated 150 $\Omega$  load the output swings to within 37 mV of the ground rail, while a mid-rail terminated 1 k $\Omega$  load will swing to 77 mV of either rail, providing true single supply operation and maximum signal dynamic range on low power rails. The amplifier output will source and sink 35 mA and drive up to 30 pF loads without the need for external compensation.

The LMH6619Q is offered in the 8-Pin SOIC package.

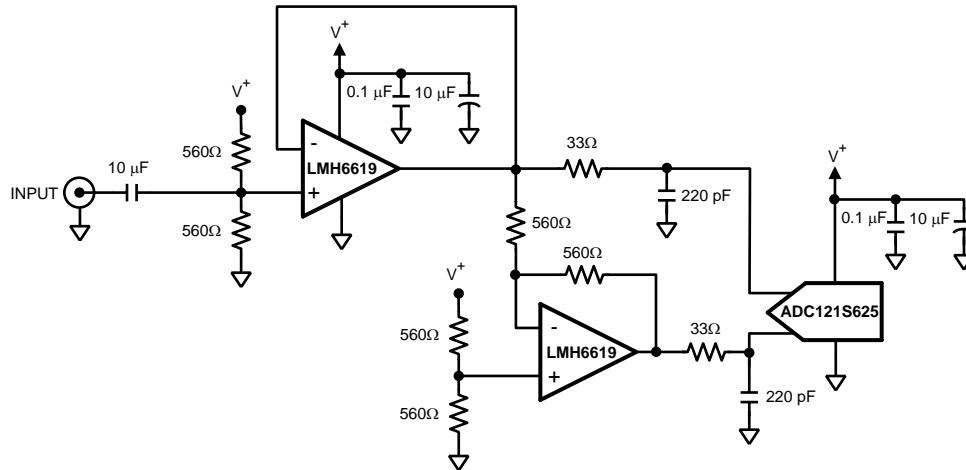
**PRODUCT PREVIEW**


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## Typical Application

**Figure 1. Single to Differential ADC Driver**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)</sup>

ESD Tolerance <sup>(2)</sup>	
Human Body Model	
For input pins only	2000V
For all other pins	2000V
Machine Model	
	200V
Supply Voltage ( $V_S = V^+ - V^-$ )	12V
Junction Temperature <sup>(3)</sup>	150°C max
Storage Temperature Range	-65°C to 150°C
Soldering Information:	
See product folder at <a href="http://www.ti.com">www.ti.com</a> and <a href="http://www.ti.com/lit/an/snoa549c/snoa549c.pdf">www.ti.com/lit/an/snoa549c/snoa549c.pdf</a> .	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
- (3) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

### Operating Ratings <sup>(1)</sup>

Supply Voltage ( $V_S = V^+ - V^-$ )	2.7V to 11V
Ambient Temperature Range <sup>(2)</sup>	-40°C to +105°C
Package Thermal Resistance ( $\theta_{JA}$ )	
8-Pin SOIC	160°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of  $T_{J(MAX)}$ ,  $\theta_{JA}$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly onto a PC Board.

### +3V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = +25^\circ\text{C}$ ,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ ,  $R_L = 1\text{ k}\Omega \parallel 5\text{ pF}$ . **Boldface** Limits apply at temperature extremes. <sup>(1)</sup>

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
<b>Frequency Domain Response</b>						
SSBW	–3 dB Bandwidth Small Signal	$A_V = 1$ , $R_L = 1\text{ k}\Omega$ , $V_{\text{OUT}} = 0.2\text{ V}_{\text{PP}}$		120		MHz
		$A_V = 2$ , $-1$ , $R_L = 1\text{ k}\Omega$ , $V_{\text{OUT}} = 0.2\text{ V}_{\text{PP}}$		56		
GBW	Gain Bandwidth	$A_V = 10$ , $R_F = 2\text{ k}\Omega$ , $R_G = 221\Omega$ , $R_L = 1\text{ k}\Omega$ , $V_{\text{OUT}} = 0.2\text{ V}_{\text{PP}}$	55	63		MHz
LSBW	–3 dB Bandwidth Large Signal	$A_V = 1$ , $R_L = 1\text{ k}\Omega$ , $V_{\text{OUT}} = 2\text{ V}_{\text{PP}}$		13		MHz
		$A_V = 2$ , $R_L = 150\Omega$ , $V_{\text{OUT}} = 2\text{ V}_{\text{PP}}$		13		
Peak	Peaking	$A_V = 1$ , $C_L = 5\text{ pF}$		1.5		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2$ , $V_{\text{OUT}} = 0.5\text{ V}_{\text{PP}}$ , $R_F = R_G = 825\Omega$		15		MHz
DG	Differential Gain	$A_V = +2$ , 4.43 MHz, $0.6\text{V} < V_{\text{OUT}} < 2\text{V}$ , $R_L = 150\Omega$ to $V^+/2$		0.1		%
DP	Differential Phase	$A_V = +2$ , 4.43 MHz, $0.6\text{V} < V_{\text{OUT}} < 2\text{V}$ , $R_L = 150\Omega$ to $V^+/2$		0.1		deg
<b>Time Domain Response</b>						
$t_r/t_f$	Rise & Fall Time	2V Step, $A_V = 1$		36		ns
SR	Slew Rate	2V Step, $A_V = 1$	36	46		V/ $\mu\text{s}$
$t_{s\_0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
<b>Noise and Distortion Performance</b>						
SFDR	Spurious Free Dynamic Range	$f_C = 100\text{ kHz}$ , $V_{\text{OUT}} = 2\text{ V}_{\text{PP}}$ , $R_L = 1\text{ k}\Omega$		100		dBc
		$f_C = 1\text{ MHz}$ , $V_{\text{OUT}} = 2\text{ V}_{\text{PP}}$ , $R_L = 1\text{ k}\Omega$		61		
		$f_C = 5\text{ MHz}$ , $V_{\text{OUT}} = 2\text{ V}_{\text{PP}}$ , $R_L = 1\text{ k}\Omega$		47		
$e_n$	Input Voltage Noise Density	$f = 100\text{ kHz}$		10		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Current Noise Density	$f = 100\text{ kHz}$		1		pA/ $\sqrt{\text{Hz}}$
CT	Crosstalk	$f = 5\text{ MHz}$ , $V_{\text{IN}} = 2\text{ V}_{\text{PP}}$		80		dB
<b>Input, DC Performance</b>						
$V_{\text{OS}}$	Input Offset Voltage	$V_{\text{CM}} = 0.5\text{V}$ (pnp active) $V_{\text{CM}} = 2.5\text{V}$ (nnp active)		0.1	$\pm 0.75$ <b><math>\pm 1.3</math></b>	mV
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Temperature Drift	<sup>(4)</sup>		0.8		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	$V_{\text{CM}} = 0.5\text{V}$ (pnp active)		-1.4	<b>-2.6</b>	$\mu\text{A}$
		$V_{\text{CM}} = 2.5\text{V}$ (nnp active)		+1.0	<b>+1.8</b>	
$I_{\text{OS}}$	Input Offset Current			0.01	<b><math>\pm 0.27</math></b>	$\mu\text{A}$
$C_{\text{IN}}$	Input Capacitance			1.5		pF
$R_{\text{IN}}$	Input Resistance			8		M $\Omega$
CMVR	Common Mode Voltage Range	DC, $\text{CMRR} \geq 65\text{ dB}$	-0.2		3.2	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}}$ Stepped from -0.1V to 1.4V	78	96		dB
		$V_{\text{CM}}$ Stepped from 2.0V to 3.1V	81	107		
$A_{\text{OL}}$	Open Loop Voltage Gain	$R_L = 1\text{ k}\Omega$ to +2.7V or +0.3V	85	98		dB
		$R_L = 150\Omega$ to +2.6V or +0.4V	76	82		
<b>Output DC Characteristics</b>						

(1) Boldface limits apply to temperature range of  $-40^\circ\text{C}$  to  $105^\circ\text{C}$

(2) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(4) Voltage average drift is determined by dividing the change in  $V_{\text{OS}}$  by temperature change.

### +3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for  $T_J = +25^\circ\text{C}$ ,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ ,  $R_L = 1\text{ k}\Omega \parallel 5\text{ pF}$ . **Boldface** Limits apply at temperature extremes. <sup>(1)</sup>

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
$V_{\text{OUT}}$	Output Voltage Swing High (Voltage from $V^+$ Supply Rail)	$R_L = 1\text{ k}\Omega$ to $V^+/2$		50	56 <b>62</b>	mV from either rail
		$R_L = 150\Omega$ to $V^+/2$		160	172 <b>198</b>	
	Output Voltage Swing Low (Voltage from $V^-$ Supply Rail)	$R_L = 1\text{ k}\Omega$ to $V^+/2$		62	68 <b>76</b>	
		$R_L = 150\Omega$ to $V^+/2$		175	189 <b>222</b>	
		$R_L = 150\Omega$ to $V^-$		34	44 <b>48</b>	
$I_{\text{OUT}}$	Linear Output Current	$V_{\text{OUT}} = V^+/2$ <sup>(5)</sup>	$\pm 25$	$\pm 35$		mA
$R_{\text{OUT}}$	Output Resistance	$f = 1\text{ MHz}$		0.17		$\Omega$
<b>Power Supply Performance</b>						
PSRR	Power Supply Rejection Ratio	DC, $V_{\text{CM}} = 0.5\text{V}$ , $V_S = 2.7\text{V}$ to $11\text{V}$	84	104		dB
$I_S$	Supply Current (per channel)	$R_L = \infty$		1.2	1.5 <b>1.75</b>	

(5) Do not short circuit the output. Continuous source or sink currents larger than the  $I_{\text{OUT}}$  typical are not recommended as it may damage the part.

## +5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = +25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{k}\Omega$  for  $A_V \neq +1$ ,  $R_L = 1\text{k}\Omega \parallel 5\text{pF}$ . **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
<b>Frequency Domain Response</b>						
SSBW	–3 dB Bandwidth Small Signal	$A_V = 1$ , $R_L = 1\text{k}\Omega$ , $V_{\text{OUT}} = 0.2 V_{\text{PP}}$		130		MHz
		$A_V = 2$ , $-1$ , $R_L = 1\text{k}\Omega$ , $V_{\text{OUT}} = 0.2 V_{\text{PP}}$		53		
GBW	Gain Bandwidth	$A_V = 10$ , $R_F = 2\text{k}\Omega$ , $R_G = 221\Omega$ , $R_L = 1\text{k}\Omega$ , $V_{\text{OUT}} = 0.2 V_{\text{PP}}$	54	57		MHz
LSBW	–3 dB Bandwidth Large Signal	$A_V = 1$ , $R_L = 1\text{k}\Omega$ , $V_{\text{OUT}} = 2 V_{\text{PP}}$		15		MHz
		$A_V = 2$ , $R_L = 150\Omega$ , $V_{\text{OUT}} = 2 V_{\text{PP}}$		15		
Peak	Peaking	$A_V = 1$ , $C_L = 5\text{pF}$		0.5		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2$ , $V_{\text{OUT}} = 0.5 V_{\text{PP}}$ , $R_F = R_G = 1\text{k}\Omega$		15		MHz
DG	Differential Gain	$A_V = +2$ , 4.43 MHz, $0.6\text{V} < V_{\text{OUT}} < 2\text{V}$ , $R_L = 150\Omega$ to $V^+/2$		0.1		%
DP	Differential Phase	$A_V = +2$ , 4.43 MHz, $0.6\text{V} < V_{\text{OUT}} < 2\text{V}$ , $R_L = 150\Omega$ to $V^+/2$		0.1		deg
<b>Time Domain Response</b>						
$t_r/t_f$	Rise & Fall Time	2V Step, $A_V = 1$		30		ns
SR	Slew Rate	2V Step, $A_V = 1$	44	55		V/ $\mu\text{s}$
$t_{s\_0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
<b>Distortion and Noise Performance</b>						
SFDR	Spurious Free Dynamic Range	$f_C = 100\text{kHz}$ , $V_{\text{OUT}} = 2 V_{\text{PP}}$ , $R_L = 1\text{k}\Omega$		100		dBc
		$f_C = 1\text{MHz}$ , $V_{\text{OUT}} = 2 V_{\text{PP}}$ , $R_L = 1\text{k}\Omega$		88		
		$f_C = 5\text{MHz}$ , $V_O = 2 V_{\text{PP}}$ , $R_L = 1\text{k}\Omega$		61		
$e_n$	Input Voltage Noise Density	$f = 100\text{kHz}$		10		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Current Noise Density	$f = 100\text{kHz}$		1		pA/ $\sqrt{\text{Hz}}$
CT	Crosstalk	$f = 5\text{MHz}$ , $V_{\text{IN}} = 2 V_{\text{PP}}$		80		dB
<b>Input, DC Performance</b>						
$V_{\text{OS}}$	Input Offset Voltage	$V_{\text{CM}} = 0.5\text{V}$ (pnp active) $V_{\text{CM}} = 4.5\text{V}$ (nnp active)		0.1	$\pm 0.75$ <b><math>\pm 1.3</math></b>	mV
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Temperature Drift	(3)		0.8		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	$V_{\text{CM}} = 0.5\text{V}$ (pnp active)		–1.5	<b>–2.4</b>	$\mu\text{A}$
		$V_{\text{CM}} = 4.5\text{V}$ (nnp active)		+1.0	<b>+1.9</b>	
$I_{\text{OS}}$	Input Offset Current			0.01	<b><math>\pm 0.26</math></b>	$\mu\text{A}$
$C_{\text{IN}}$	Input Capacitance			1.5		pF
$R_{\text{IN}}$	Input Resistance			8		M $\Omega$
CMVR	Common Mode Voltage Range	DC, $\text{CMRR} \geq 65\text{dB}$	–0.2		5.2	V
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}}$ Stepped from –0.1V to 3.4V	81	98		dB
		$V_{\text{CM}}$ Stepped from 4.0V to 5.1V	84	108		
$A_{\text{OL}}$	Open Loop Voltage Gain	$R_L = 1\text{k}\Omega$ to +4.6V or +0.4V	84	100		dB
		$R_L = 150\Omega$ to +4.5V or +0.5V	78	83		
<b>Output DC Characteristics</b>						

- (1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (3) Voltage average drift is determined by dividing the change in  $V_{\text{OS}}$  by temperature change.

### +5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are guaranteed for  $T_J = +25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{k}\Omega$  for  $A_V \neq +1$ ,  $R_L = 1\text{k}\Omega \parallel 5\text{pF}$ . **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
$V_{\text{OUT}}$	Output Voltage Swing High Voltage from $V^+$ Supply Rail)	$R_L = 1\text{k}\Omega$ to $V^+/2$		60	73 <b>82</b>	mV from either rail
		$R_L = 150\Omega$ to $V^+/2$		230	255 <b>295</b>	
	Output Voltage Swing Low Voltage from $V^-$ Supply Rail)	$R_L = 1\text{k}\Omega$ to $V^+/2$		77	85 <b>98</b>	
		$R_L = 150\Omega$ to $V^+/2$		255	275 <b>326</b>	
		$R_L = 150\Omega$ to $V^-$		37	48 <b>50</b>	
$I_{\text{OUT}}$	Linear Output Current	$V_{\text{OUT}} = V^+/2$ (4)	$\pm 25$	$\pm 35$		mA
$R_{\text{OUT}}$	Output Resistance	$f = 1\text{MHz}$		0.17		$\Omega$
<b>Power Supply Performance</b>						
PSRR	Power Supply Rejection Ratio	DC, $V_{\text{CM}} = 0.5\text{V}$ , $V_S = 2.7\text{V}$ to $11\text{V}$	84	104		dB
$I_S$	Supply Current (per channel)	$R_L = \infty$		1.3	1.5 <b>1.75</b>	

(4) Do not short circuit the output. Continuous source or sink currents larger than the  $I_{\text{OUT}}$  typical are not recommended as it may damage the part.

## ±5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for  $T_J = +25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = -5\text{V}$ ,  $V_{CM} = V_O = 0\text{V}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{k}\Omega$  for  $A_V \neq +1$ ,  $R_L = 1\text{k}\Omega \parallel 5\text{pF}$ . **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
<b>Frequency Domain Response</b>						
SSBW	–3 dB Bandwidth Small Signal	$A_V = 1$ , $R_L = 1\text{k}\Omega$ , $V_{OUT} = 0.2 V_{PP}$		140		MHz
		$A_V = 2$ , $-1$ , $R_L = 1\text{k}\Omega$ , $V_{OUT} = 0.2 V_{PP}$		53		
GBW	Gain Bandwidth	$A_V = 10$ , $R_F = 2\text{k}\Omega$ , $R_G = 221\Omega$ , $R_L = 1\text{k}\Omega$ , $V_{OUT} = 0.2 V_{PP}$	54	58		MHz
LSBW	–3 dB Bandwidth Large Signal	$A_V = 1$ , $R_L = 1\text{k}\Omega$ , $V_{OUT} = 2 V_{PP}$		16		MHz
		$A_V = 2$ , $R_L = 150\Omega$ , $V_{OUT} = 2 V_{PP}$		15		
Peak	Peaking	$A_V = 1$ , $C_L = 5\text{pF}$		0.05		dB
0.1 dBBW	0.1 dB Bandwidth	$A_V = 2$ , $V_{OUT} = 0.5 V_{PP}$ , $R_F = R_G = 1.21\text{k}\Omega$		15		MHz
DG	Differential Gain	$A_V = +2$ , 4.43 MHz, $0.6\text{V} < V_{OUT} < 2\text{V}$ , $R_L = 150\Omega$ to $V^+/2$		0.1		%
DP	Differential Phase	$A_V = +2$ , 4.43 MHz, $0.6\text{V} < V_{OUT} < 2\text{V}$ , $R_L = 150\Omega$ to $V^+/2$		0.1		deg
<b>Time Domain Response</b>						
$t_r/t_f$	Rise & Fall Time	2V Step, $A_V = 1$		30		ns
SR	Slew Rate	2V Step, $A_V = 1$	45	57		V/ $\mu\text{s}$
$t_{s\_0.1}$	0.1% Settling Time	2V Step, $A_V = -1$		90		ns
$t_{s\_0.01}$	0.01% Settling Time	2V Step, $A_V = -1$		120		
<b>Noise and Distortion Performance</b>						
SFDR	Spurious Free Dynamic Range	$f_C = 100\text{kHz}$ , $V_{OUT} = 2 V_{PP}$ , $R_L = 1\text{k}\Omega$		100		dBc
		$f_C = 1\text{MHz}$ , $V_{OUT} = 2 V_{PP}$ , $R_L = 1\text{k}\Omega$		88		
		$f_C = 5\text{MHz}$ , $V_{OUT} = 2 V_{PP}$ , $R_L = 1\text{k}\Omega$		70		
$e_n$	Input Voltage Noise Density	$f = 100\text{kHz}$		10		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Current Noise Density	$f = 100\text{kHz}$		1		pA/ $\sqrt{\text{Hz}}$
CT	Crosstalk	$f = 5\text{MHz}$ , $V_{IN} = 2 V_{PP}$		80		dB
<b>Input DC Performance</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = -4.5\text{V}$ (pnp active) $V_{CM} = 4.5\text{V}$ (nnp active)		0.1	$\pm 0.75$ <b><math>\pm 1.3</math></b>	mV
$TCV_{OS}$	Input Offset Voltage Temperature Drift	(3)		0.9		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current	$V_{CM} = -4.5\text{V}$ (pnp active)		-1.5	<b>-2.4</b>	$\mu\text{A}$
		$V_{CM} = 4.5\text{V}$ (nnp active)		+1.0	<b>+1.9</b>	
$I_{OS}$	Input Offset Current			0.01	<b><math>\pm 0.26</math></b>	$\mu\text{A}$
$C_{IN}$	Input Capacitance			1.5		pF
$R_{IN}$	Input Resistance			8		M $\Omega$
CMVR	Common Mode Voltage Range	DC, $CMRR \geq 65\text{dB}$	-5.2		5.2	V
CMRR	Common Mode Rejection Ratio	$V_{CM}$ Stepped from -5.1V to 3.4V	84	100		dB
		$V_{CM}$ Stepped from 4.0V to 5.1V	83	108		
$A_{OL}$	Open Loop Voltage Gain	$R_L = 1\text{k}\Omega$ to +4.6V or -4.6V	86	95		dB
		$R_L = 150\Omega$ to +4.3V or -4.3V	79	84		
<b>Output DC Characteristics</b>						

- (1) Limits are 100% production tested at  $25^\circ\text{C}$ . Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
- (3) Voltage average drift is determined by dividing the change in  $V_{OS}$  by temperature change.

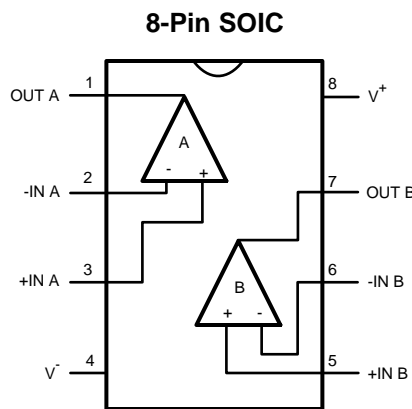
**±5V Electrical Characteristics (continued)**

Unless otherwise specified, all limits are guaranteed for  $T_J = +25^{\circ}\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = -5\text{V}$ ,  $V_{\text{CM}} = V_O = 0\text{V}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ ,  $R_L = 1\text{ k}\Omega \parallel 5\text{ pF}$ . **Boldface** Limits apply at temperature extremes.

Symbol	Parameter	Condition	Min (1)	Typ (2)	Max (1)	Units
$V_{\text{OUT}}$	Output Voltage Swing High (Voltage from $V^+$ Supply Rail)	$R_L = 1\text{ k}\Omega$ to GND		100	111 <b>126</b>	mV from either rail
		$R_L = 150\Omega$ to GND		430	457 <b>526</b>	
	Output Voltage Swing Low (Voltage from $V^-$ Supply Rail)	$R_L = 1\text{ k}\Omega$ to GND		115	126 <b>141</b>	
		$R_L = 150\Omega$ to GND		450	484 <b>569</b>	
		$R_L = 150\Omega$ to $V^-$		45	61 <b>62</b>	
$I_{\text{OUT}}$	Linear Output Current	$V_{\text{OUT}} = V^+/2$ (4)	$\pm 25$	$\pm 35$		mA
$R_{\text{OUT}}$	Output Resistance	$f = 1\text{ MHz}$		0.17		$\Omega$
<b>Power Supply Performance</b>						
PSRR	Power Supply Rejection Ratio	DC, $V_{\text{CM}} = -4.5\text{V}$ , $V_S = 2.7\text{V}$ to $11\text{V}$	84	104		dB
$I_S$	Supply Current (per channel)	$R_L = \infty$		1.45	1.65 <b>2.0</b>	

(4) Do not short circuit the output. Continuous source or sink currents larger than the  $I_{\text{OUT}}$  typical are not recommended as it may damage the part.

**Connection Diagram**



**Figure 2. Top View**

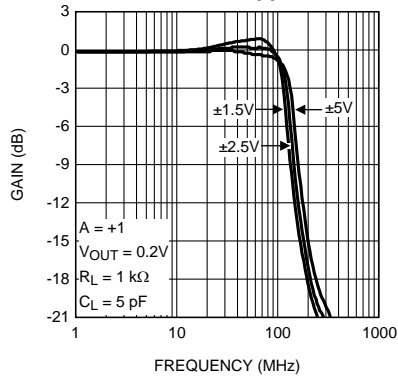
PRODUCT PREVIEW



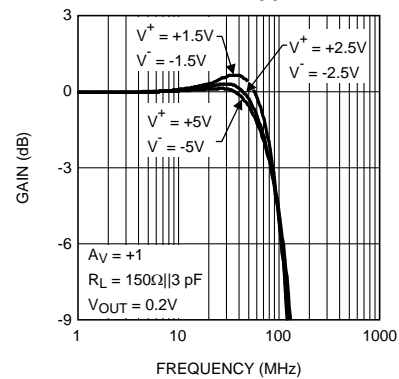
### Typical Performance Characteristics

At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.

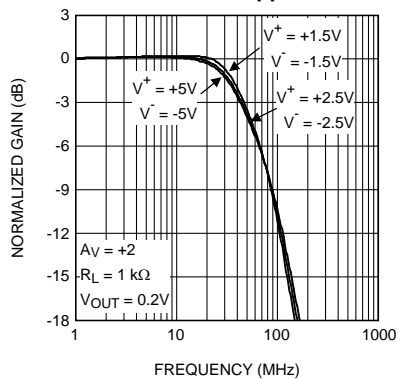
**Closed Loop Frequency Response for Various Supplies**



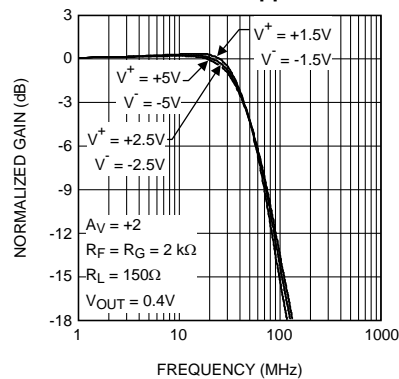
**Closed Loop Frequency Response for Various Supplies**



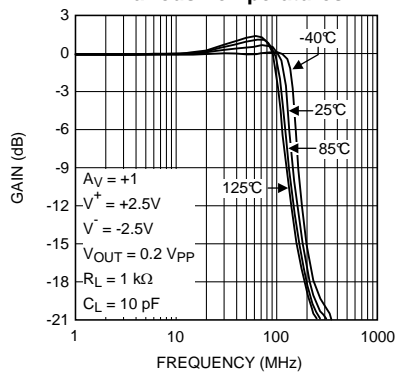
**Closed Loop Frequency Response for Various Supplies**



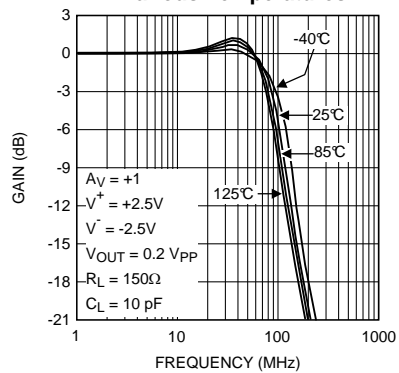
**Closed Loop Frequency Response for Various Supplies**



**Closed Loop Frequency Response for Various Temperatures**



**Closed Loop Frequency Response for Various Temperatures**

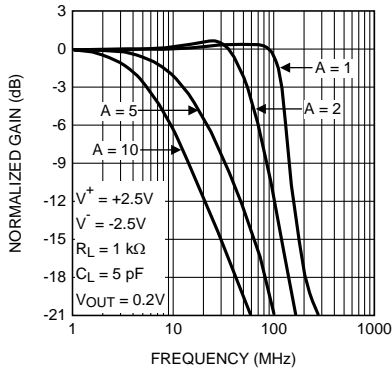


PRODUCT PREVIEW

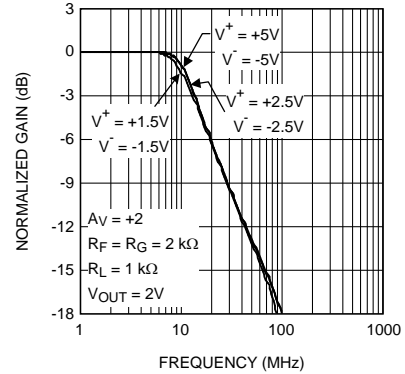
**Typical Performance Characteristics (continued)**

At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.

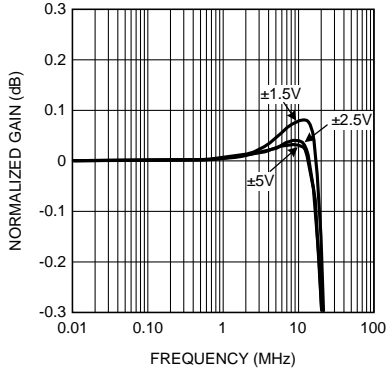
**Closed Loop Gain vs. Frequency for Various Gains**



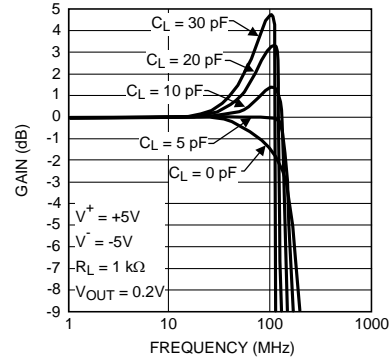
**Large Signal Frequency Response**



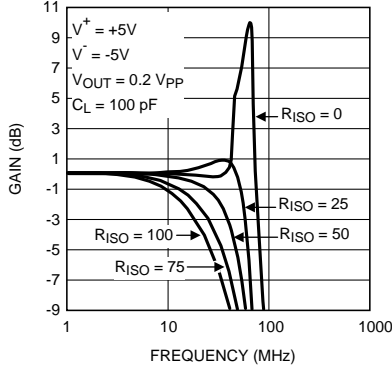
**$\pm 0.1\text{ dB}$  Gain Flatness for Various Supplies**



**Small Signal Frequency Response with Various Capacitive Load**



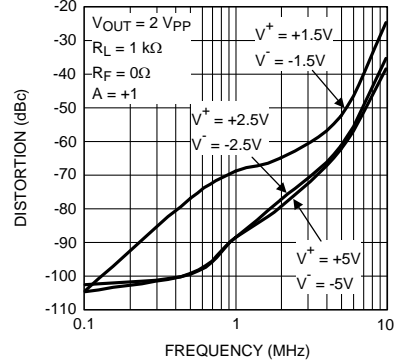
**Small Signal Frequency Response with Capacitive Load and Various  $R_{ISO}$**



**HD2**

vs.

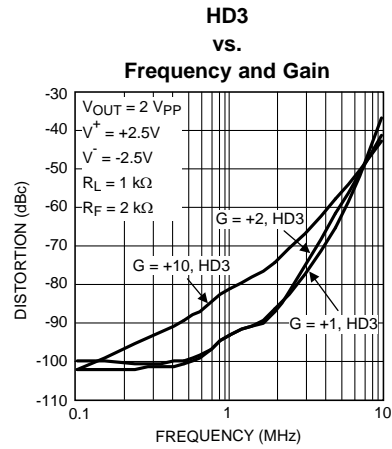
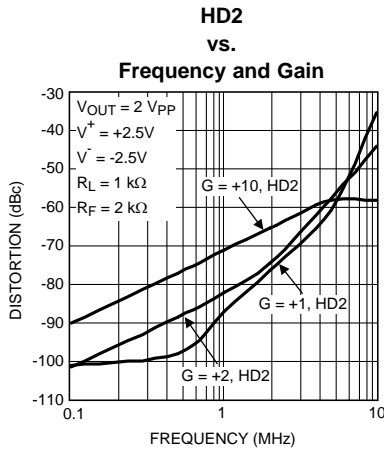
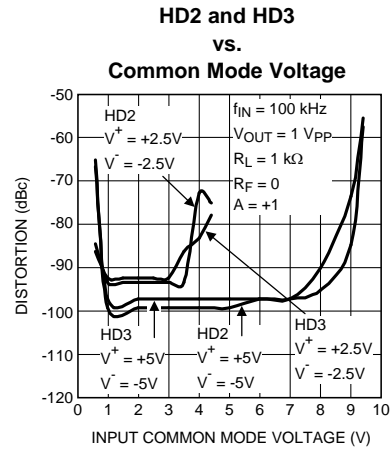
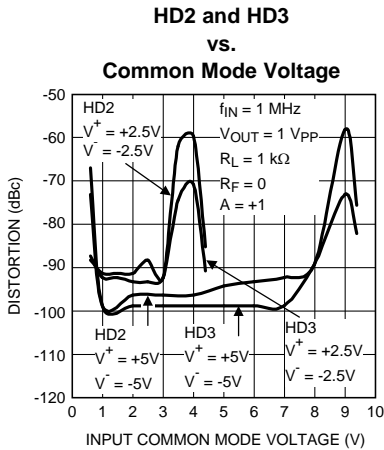
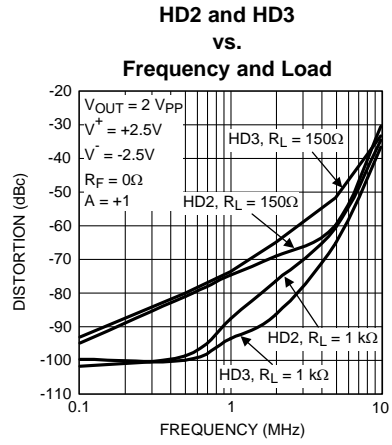
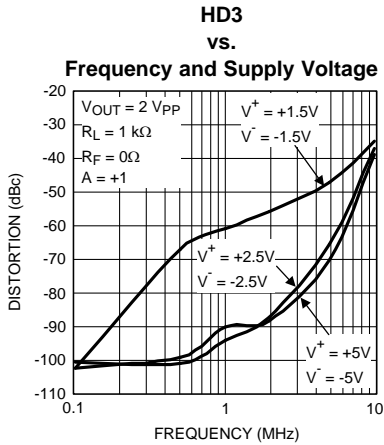
**Frequency and Supply Voltage**



PRODUCT PREVIEW

Typical Performance Characteristics (continued)

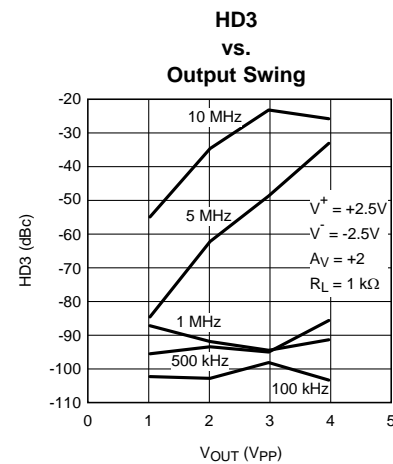
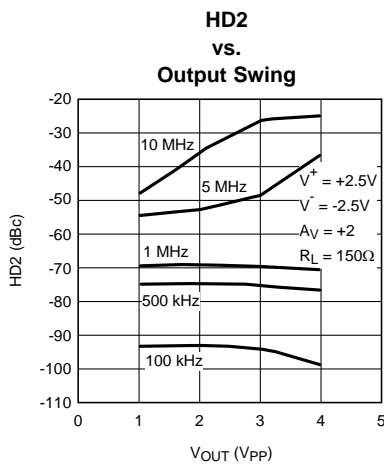
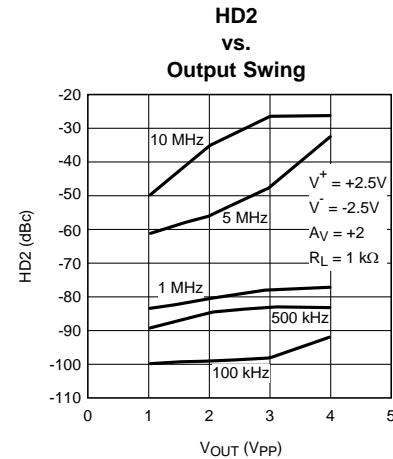
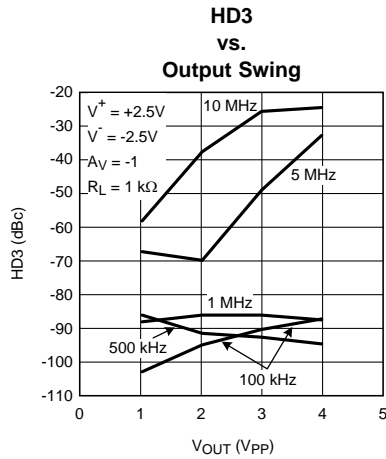
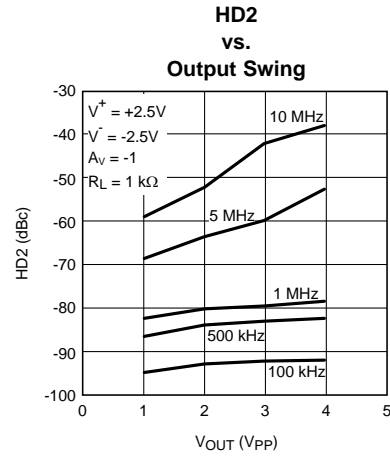
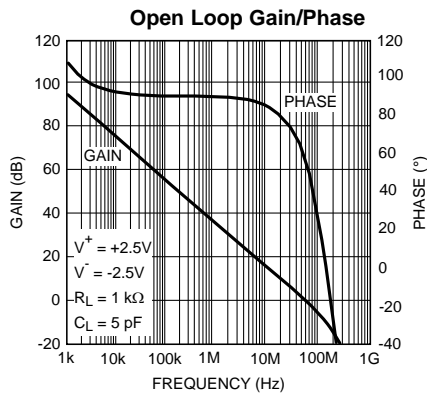
At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.



PRODUCT PREVIEW

**Typical Performance Characteristics (continued)**

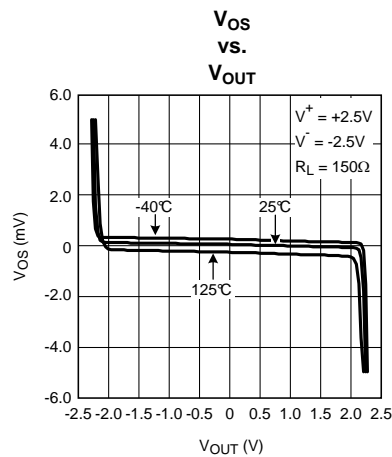
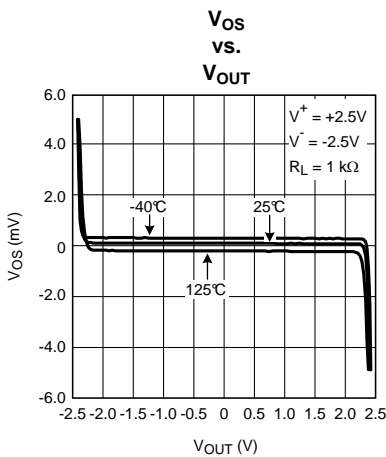
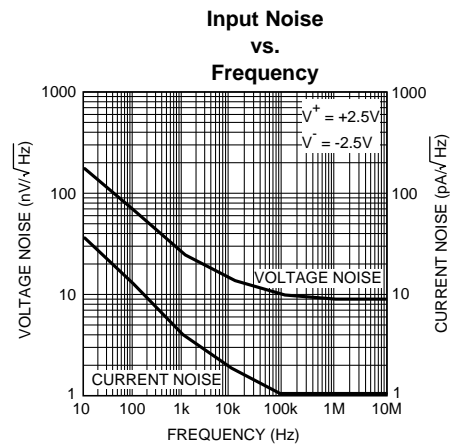
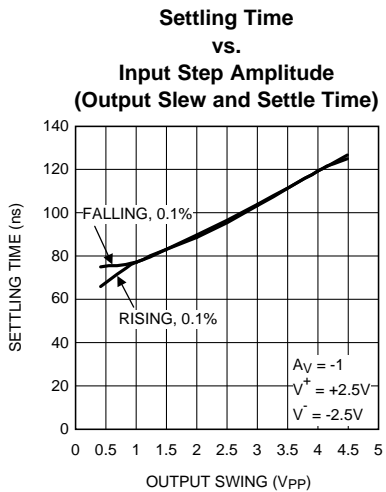
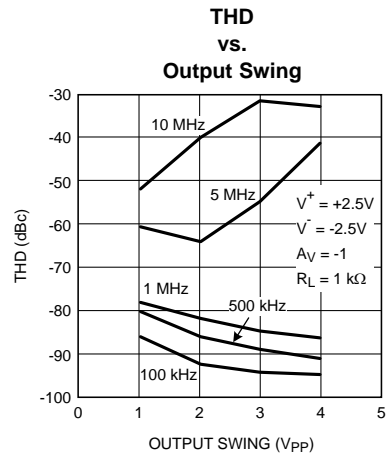
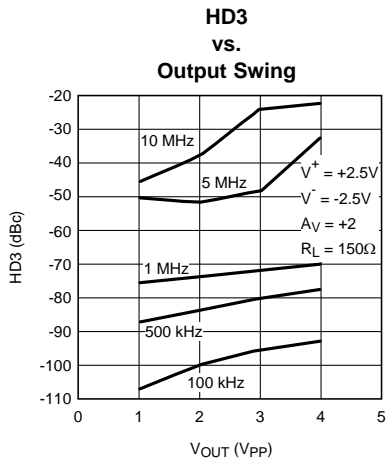
At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.



PRODUCT PREVIEW

**Typical Performance Characteristics (continued)**

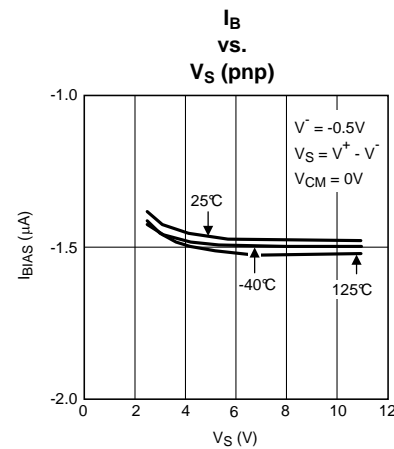
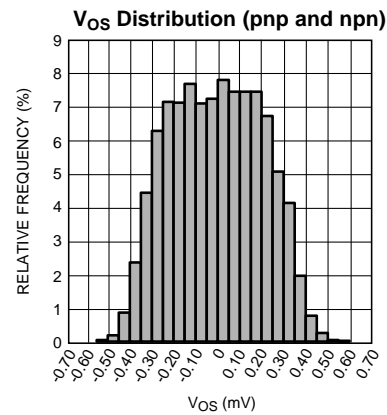
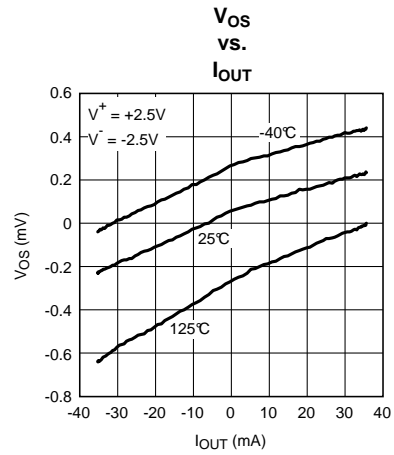
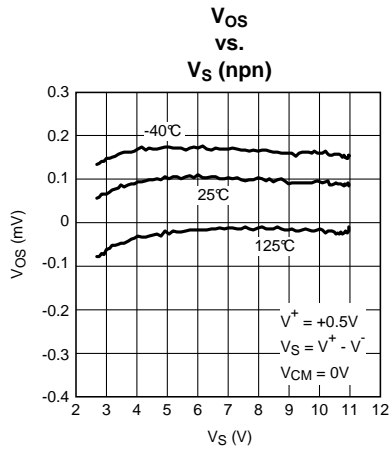
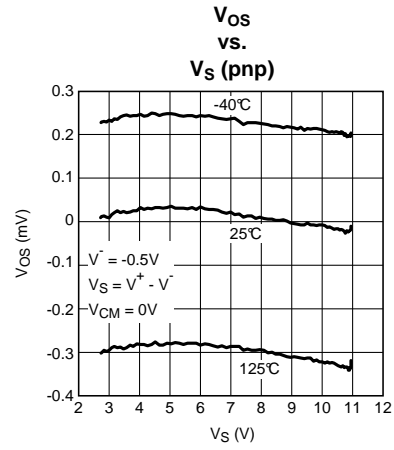
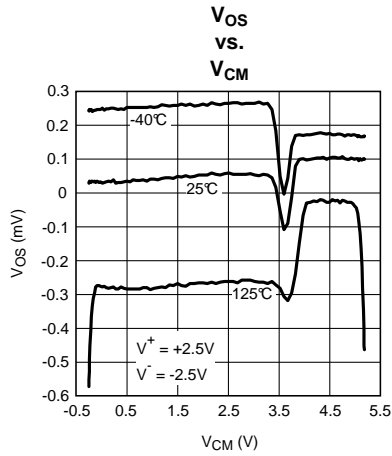
At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.



PRODUCT PREVIEW

**Typical Performance Characteristics (continued)**

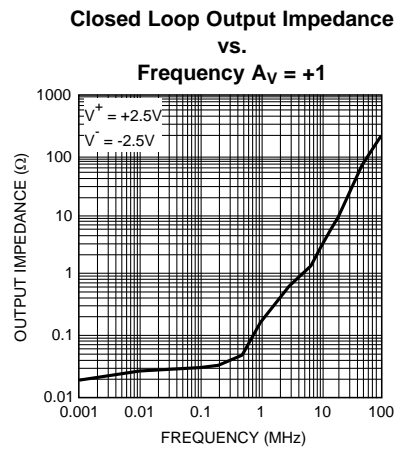
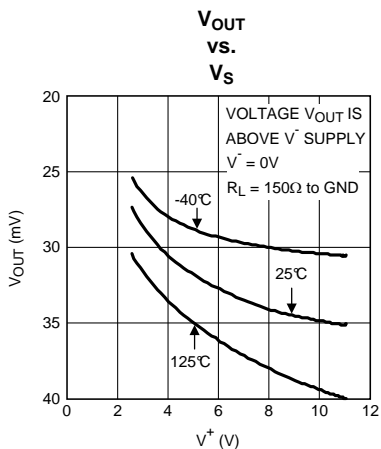
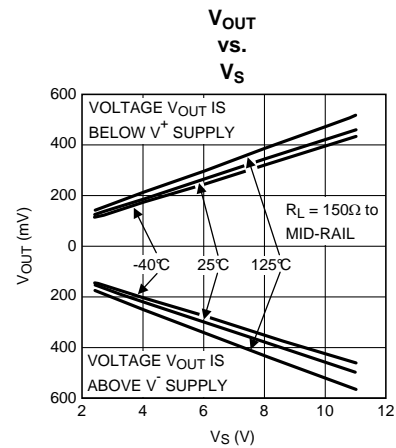
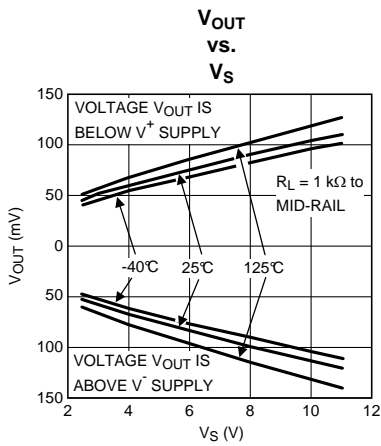
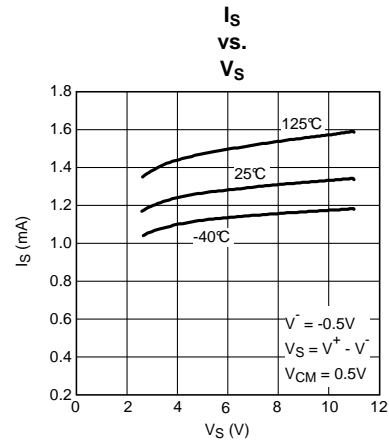
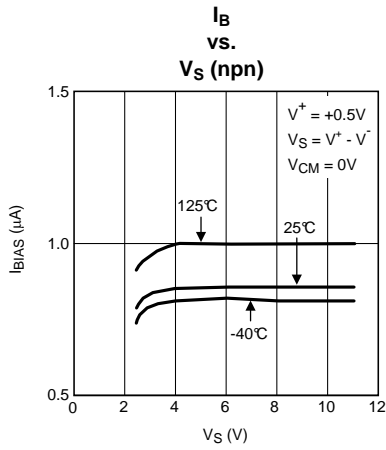
At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.



PRODUCT PREVIEW

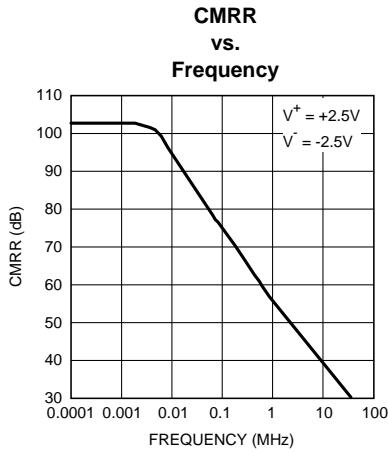
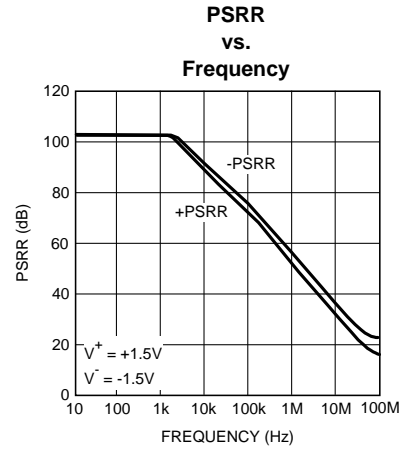
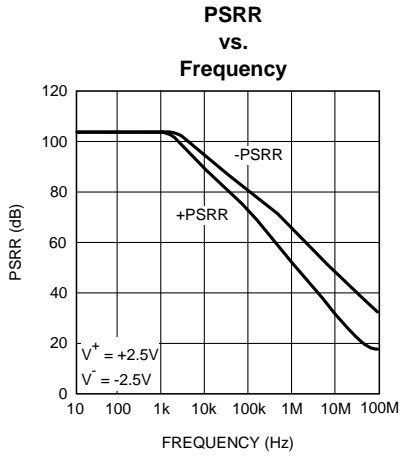
**Typical Performance Characteristics (continued)**

At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.

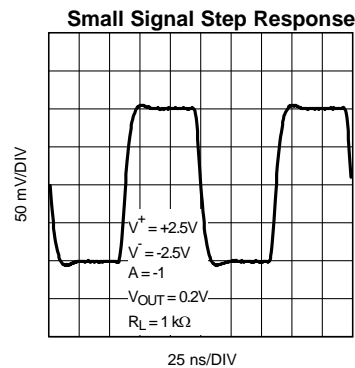
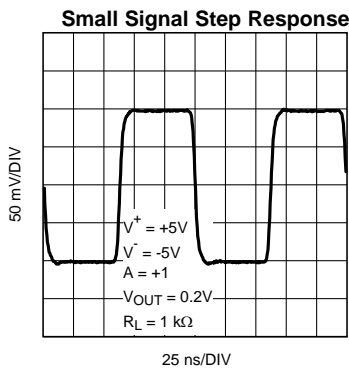
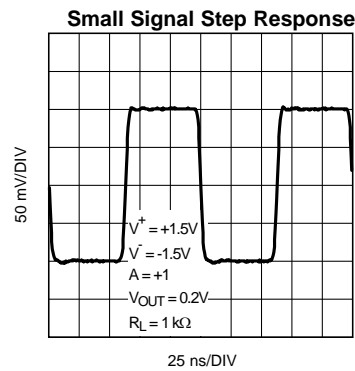
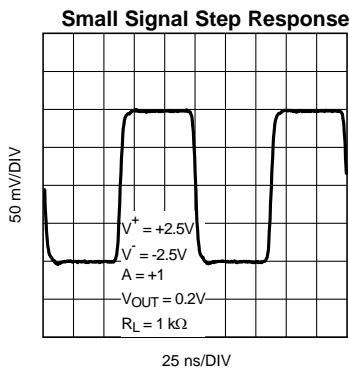
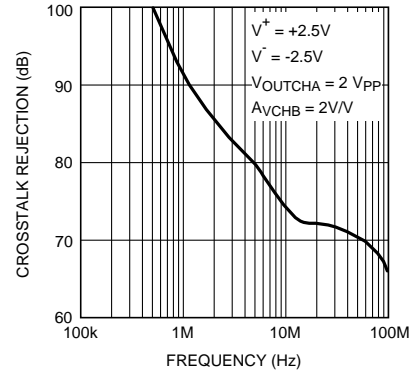


**Typical Performance Characteristics (continued)**

At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{ k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.



**Crosstalk Rejection vs. Frequency (Output to Output)**

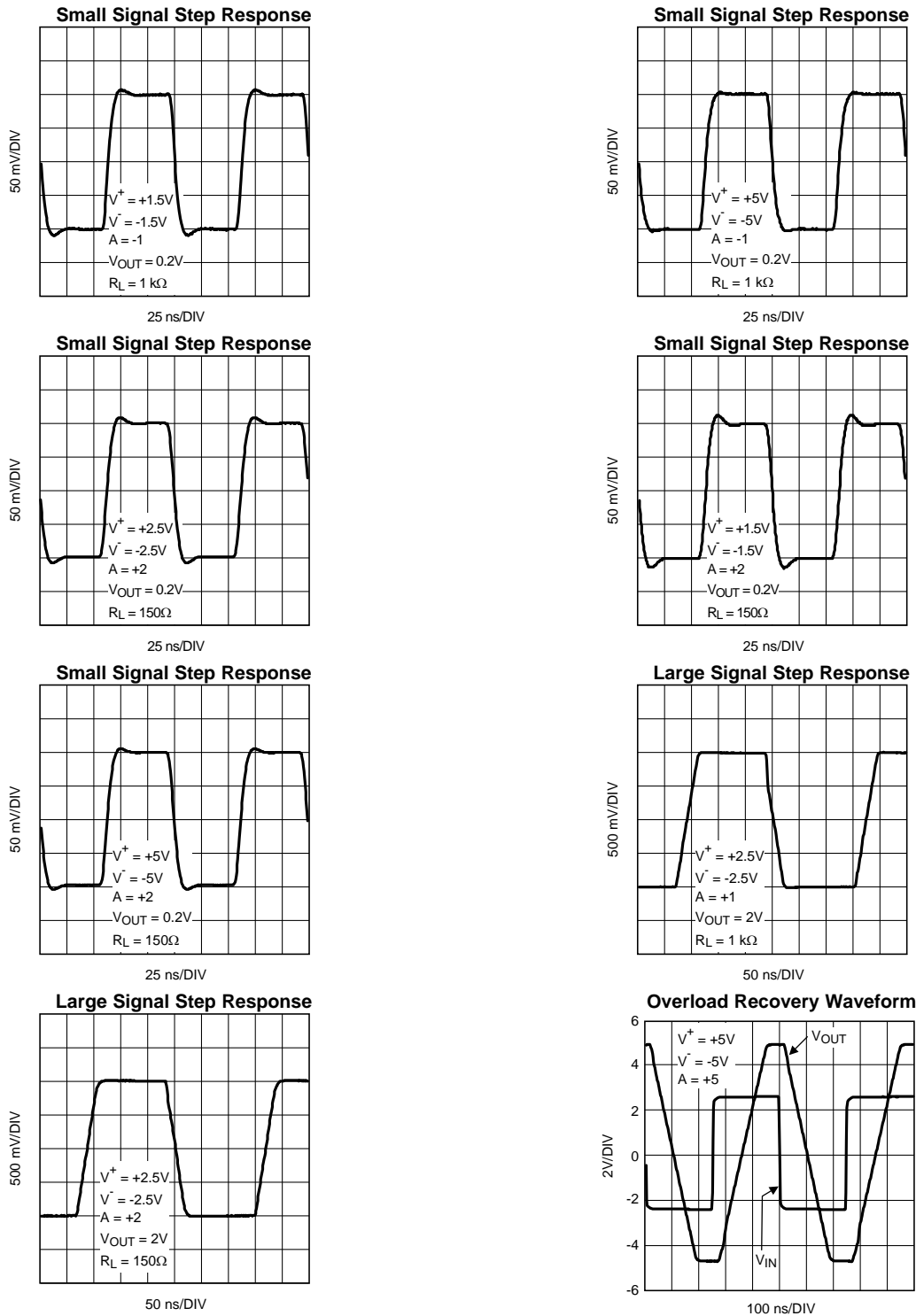


PRODUCT PREVIEW



### Typical Performance Characteristics (continued)

At  $T_J = 25^\circ\text{C}$ ,  $A_V = +1$  ( $R_F = 0\Omega$ ), otherwise  $R_F = 2\text{k}\Omega$  for  $A_V \neq +1$ , unless otherwise specified.



PRODUCT PREVIEW

### Application Information

The LMH6619Q is based on National Semiconductor's proprietary VIP10 dielectrically isolated bipolar process. This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high  $f_t$  (~8 GHz) even under low supply voltage (2.7V) and

low bias current.

- Common emitter push-push output stage. This architecture allows the output to reach within millivolts of either supply rail.
- Consistent performance from any supply voltage (2.7V - 11V) with little variation with supply voltage for the most important specifications (e.g. BW, SR, I<sub>OUT</sub>.)
- Significant power saving compared to competitive devices on the market with similar performance.

With 3V supplies and a common mode input voltage range that extends beyond either supply rail, the LMH6619Q is well suited to many low voltage/low power applications. Even with 3V supplies, the -3 dB BW (at A<sub>V</sub> = +1) is typically 120 MHz.

The LMH6619Q is designed to avoid output phase reversal. With input over-drive, the output is kept near the supply rail (or as close to it as mandated by the closed loop gain setting and the input voltage). Figure 3 shows the input and output voltage when the input voltage significantly exceeds the supply voltages.

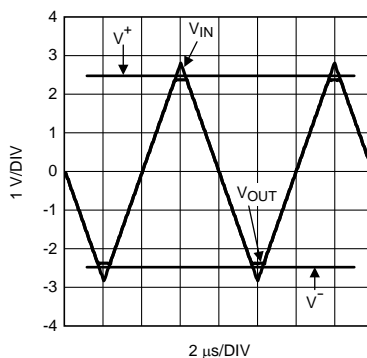


Figure 3. Input and Output Shown with CMVR Exceeded

**SINGLE TO DIFFERENTIAL ADC DRIVER**

Figure 4 shows the LMH6619Q used to drive a differential ADC with a single-ended input. The ADC121S625 is a fully differential 12-bit ADC. Table 1 shows the performance data of the LMH6619Q and the ADC121S625.

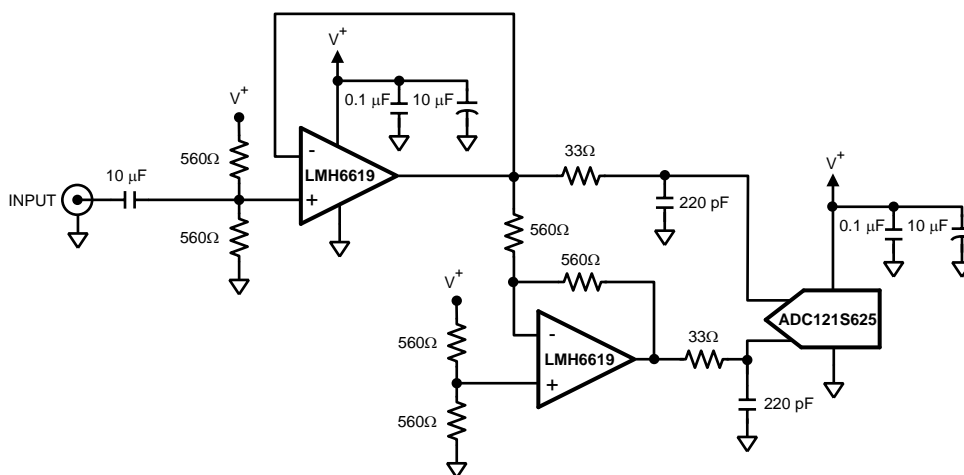


Figure 4. LMH6619Q Driving an ADC121S625

Table 1. Performance Data for the Single to Differential ADC Driver

Parameter	Measured Value
Signal Frequency	10 kHz
Signal Amplitude	2.5V

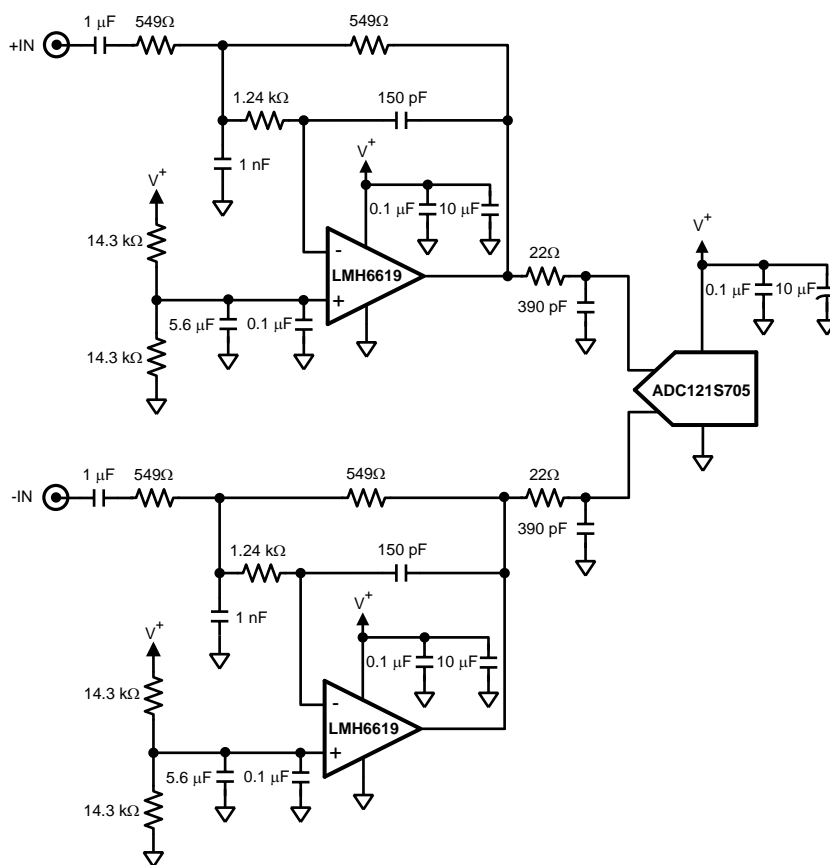
PRODUCT PREVIEW

**Table 1. Performance Data for the Single to Differential ADC Driver (continued)**

Parameter	Measured Value
SINAD	67.9 dB
SNR	68.29 dB
THD	-78.6 dB
SFDR	75.0 dB
ENOB	11.0 bits

**DIFFERENTIAL ADC DRIVER**

Its low noise and wide bandwidth make the LMH6619Q an excellent choice for driving a 12-bit ADC. Figure 5 shows the LMH6619Q driving an ADC121S705. The ADC121S705 is a fully differential 12-bit ADC. The LMH6619Q is set up in a 2nd order multiple-feedback configuration with a gain of -1. The -3 dB point is at 500 kHz and the -0.01 dB point is at 100 kHz. The 22Ω resistor and 390 pF capacitor form an antialiasing filter for the ADC121S705. The capacitor also stores and delivers charge to the switched capacitor input of the ADC. The capacitive load on the LMH6619Q created by the 390 pF capacitor is decreased by the 22Ω resistor. Table 2 shows the performance data.



**Figure 5. LMH6619Q Driving an ADC121S705**

**Table 2. Performance Data for the Differential ADC Driver**

Parameter	Measured Value
Signal Frequency	100 kHz
SINAD	71.5 dB
SNR	71.87 dB
THD	-82.4 dB

**Table 2. Performance Data for the Differential ADC Driver (continued)**

Parameter	Measured Value
SFDR	90.97 dB
ENOB	11.6 bits

**DC LEVEL SHIFTING**

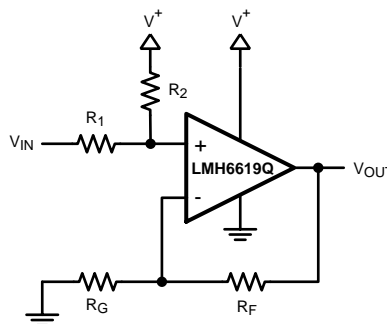
Often a signal must be both amplified and level shifted while using a single supply for the op amp. The circuit in [Figure 6](#) can do both of these tasks. The procedure for specifying the resistor values is as follows.

1. Determine the input voltage.
2. Calculate the input voltage midpoint,  $V_{INMID} = V_{INMIN} + (V_{INMAX} - V_{INMIN})/2$ .
3. Determine the output voltage needed.
4. Calculate the output voltage midpoint,  $V_{OUTMID} = V_{OUTMIN} + (V_{OUTMAX} - V_{OUTMIN})/2$ .
5. Calculate the gain needed,  $gain = (V_{OUTMAX} - V_{OUTMIN})/(V_{INMAX} - V_{INMIN})$
6. Calculate the amount the voltage needs to be shifted from input to output,  $\Delta V_{OUT} = V_{OUTMID} - gain \times V_{INMID}$ .
7. Set the supply voltage to be used.
8. Calculate the noise gain,  $noise\ gain = gain + \Delta V_{OUT}/V_S$ .
9. Set  $R_F$ .
10. Calculate  $R_1$ ,  $R_1 = R_F/gain$ .
11. Calculate  $R_2$ ,  $R_2 = R_F/(noise\ gain - gain)$ .
12. Calculate  $R_G$ ,  $R_G = R_F/(noise\ gain - 1)$ .

Check that both the  $V_{IN}$  and  $V_{OUT}$  are within the voltage ranges of the LMH6619Q.

The following example is for a  $V_{IN}$  of 0V to 1V with a  $V_{OUT}$  of 2V to 4V.

1.  $V_{IN} = 0V$  to  $1V$
2.  $V_{INMID} = 0V + (1V - 0V)/2 = 0.5V$
3.  $V_{OUT} = 2V$  to  $4V$
4.  $V_{OUTMID} = 2V + (4V - 2V)/2 = 3V$
5.  $Gain = (4V - 2V)/(1V - 0V) = 2$
6.  $\Delta V_{OUT} = 3V - 2 \times 0.5V = 2$
7. For the example the supply voltage will be +5V.
8.  $Noise\ gain = 2 + 2/5V = 2.4$
9.  $R_F = 2\ k\Omega$
10.  $R_1 = 2\ k\Omega/2 = 1\ k\Omega$
11.  $R_2 = 2\ k\Omega/(2.4 - 2) = 5\ k\Omega$
12.  $R_G = 2\ k\Omega/(2.4 - 1) = 1.43\ k\Omega$

**Figure 6. DC Level Shifting**

### 4<sup>th</sup> ORDER MULTIPLE FEEDBACK LOW-PASS FILTER

Figure 7 shows the LMH6619Q used as the amplifier in a multiple feedback low pass filter. This filter is set up to have a gain of +1 and a -3 dB point of 1 MHz. Values can be determined by using the WEBENCH® Active Filter Designer found at amplifiers.national.com.

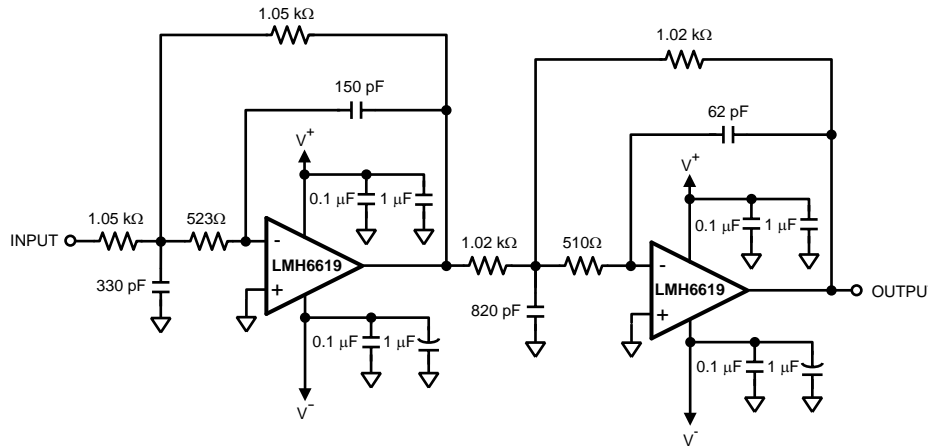


Figure 7. 4<sup>th</sup> Order Multiple Feedback Low-Pass Filter

### CURRENT SENSE AMPLIFIER

With its rail-to-rail input and output capability, low  $V_{OS}$ , and low  $I_B$  the LMH6619Q is an ideal choice for a current sense amplifier application. Figure 8 shows the schematic of the LMH6619Q set up in a low-side sense configuration which provides a conversion gain of 2V/A. Voltage error due to  $V_{OS}$  can be calculated to be  $V_{OS} \times (1 + R_F/R_G)$  or  $0.6 \text{ mV} \times 21 = 12.6 \text{ mV}$ . Voltage error due to  $I_O$  is  $I_O \times R_F$  or  $0.26 \text{ μA} \times 1 \text{ k}\Omega = 0.26 \text{ mV}$ . Hence total voltage error is  $12.6 \text{ mV} + 0.26 \text{ mV}$  or  $12.86 \text{ mV}$  which translates into a current error of  $12.86 \text{ mV}/(2 \text{ V/A}) = 6.43 \text{ mA}$ .

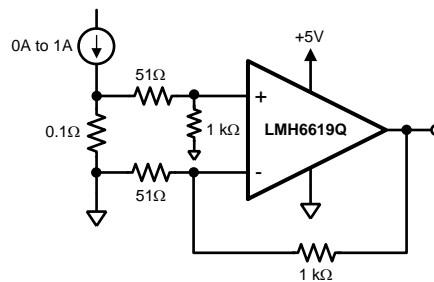


Figure 8. Current Sense Amplifier

### TRANSIMPEDANCE AMPLIFIER

By definition, a photodiode produces either a current or voltage output from exposure to a light source. A Transimpedance Amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal. The TIA often will need to be compensated to insure proper operation.

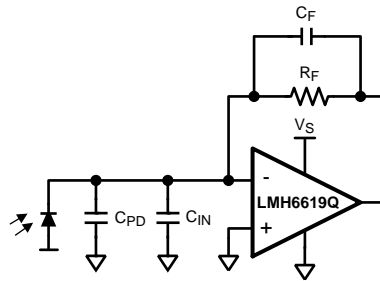


Figure 9. Photodiode Modeled with Capacitance Elements

Figure 9 shows the LMH6619Q modeled with photodiode and the internal op amp capacitances. The LMH6619Q allows circuit operation of a low intensity light due to its low input bias current by using larger values of gain ( $R_F$ ). The total capacitance ( $C_T$ ) on the inverting terminal of the op amp includes the photodiode capacitance ( $C_{PD}$ ) and the input capacitance of the op amp ( $C_{IN}$ ). This total capacitance ( $C_T$ ) plays an important role in the stability of the circuit. The noise gain of this circuit determines the stability and is defined by:

$$NG = \frac{1 + sR_F(C_T + C_F)}{1 + sC_F R_F} \tag{1}$$

Where,  $f_z \cong \frac{1}{2\pi R_F C_T}$  and  $f_p = \frac{1}{2\pi R_F C_F}$  (2)

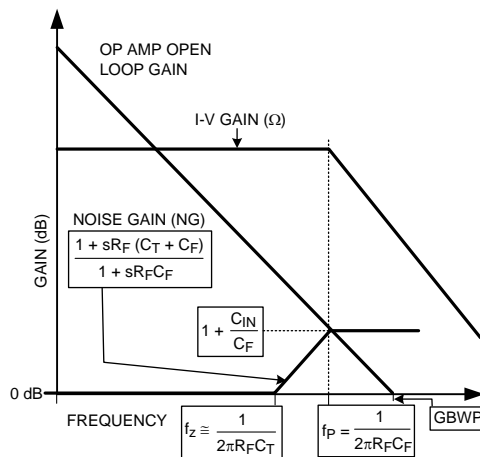


Figure 10. Bode Plot of Noise Gain Intersecting with Op Amp Open-Loop Gain

Figure 10 shows the bode plot of the noise gain intersecting the op amp open loop gain. With larger values of gain,  $C_T$  and  $R_F$  create a zero in the transfer function. At higher frequencies the circuit can become unstable due to excess phase shift around the loop.

A pole at  $f_p$  in the noise gain function is created by placing a feedback capacitor ( $C_F$ ) across  $R_F$ . The noise gain slope is flattened by choosing an appropriate value of  $C_F$  for optimum performance.

Theoretical expressions for calculating the optimum value of  $C_F$  and the expected  $-3$  dB bandwidth are:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F(GBWP)}} \tag{3}$$

$$f_{-3dB} = \sqrt{\frac{GBWP}{2\pi R_F C_T}} \tag{4}$$

Equation 4 indicates that the  $-3$  dB bandwidth of the TIA is inversely proportional to the feedback resistor. Therefore, if the bandwidth is important then the best approach would be to have a moderate transimpedance gain stage followed by a broadband voltage gain stage.

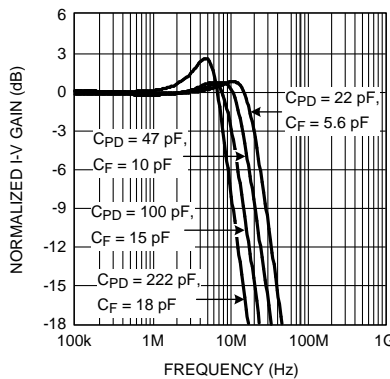
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Table 3 shows the measurement results of the LMH6619Q with different photodiodes having various capacitances ( $C_{PD}$ ) and a feedback resistance ( $R_F$ ) of 1 k $\Omega$ .

**Table 3. TIA (Figure 1) Compensation and Performance Results**

$C_{PD}$ (pF)	$C_T$ (pF)	$C_F$ CAL (pF)	$C_F$ USED (pF)	$f_{-3\text{ dB CAL}}$ (MHz)	$f_{-3\text{ dB MEAS}}$ (MHz)	Peaking (dB)
22	24	7.7	5.6	23.7	20	0.9
47	49	10.9	10	16.6	15.2	0.8
100	102	15.8	15	11.5	10.8	0.9
222	224	23.4	18	7.81	8	2.9

Figure 11 shows the frequency response for the various photodiodes in Table 3.



**Figure 11. Frequency Response for Various Photodiode and Feedback Capacitors**

When analyzing the noise at the output of the TIA, it is important to note that the various noise sources (i.e. op amp noise voltage, feedback resistor thermal noise, input noise current, photodiode noise current) do not all operate over the same frequency band. Therefore, when the noise at the output is calculated, this should be taken into account. The op amp noise voltage will be gained up in the region between the noise gain's zero and pole ( $f_z$  and  $f_p$  in Figure 10). The higher the values of  $R_F$  and  $C_T$ , the sooner the noise gain peaking starts and therefore its contribution to the total output noise will be larger. It is obvious to note that it is advantageous to minimize  $C_{IN}$  by proper choice of op amp or by applying a reverse bias across the diode at the expense of excess dark current and noise.

### DIFFERENTIAL CABLE DRIVER FOR NTSC VIDEO

The LMH6619Q can be used to drive an NTSC video signal on a twisted-pair cable. Figure 12 shows the schematic of a differential cable driver for NTSC video. This circuit can be used to transmit the signal from a camera over a twisted pair to a monitor or display located a distance.  $C_1$  and  $C_2$  are used to AC couple the video signal into the LMH6619Q. The two amplifiers of the LMH6619Q are set to a gain of 2 to compensate for the 75 $\Omega$  back termination resistors on the outputs. The LMH6619Q is set to a gain of 1. Because of the DC bias the output of the LMH6619Q is AC coupled. Most monitors and displays will accept AC coupled inputs.

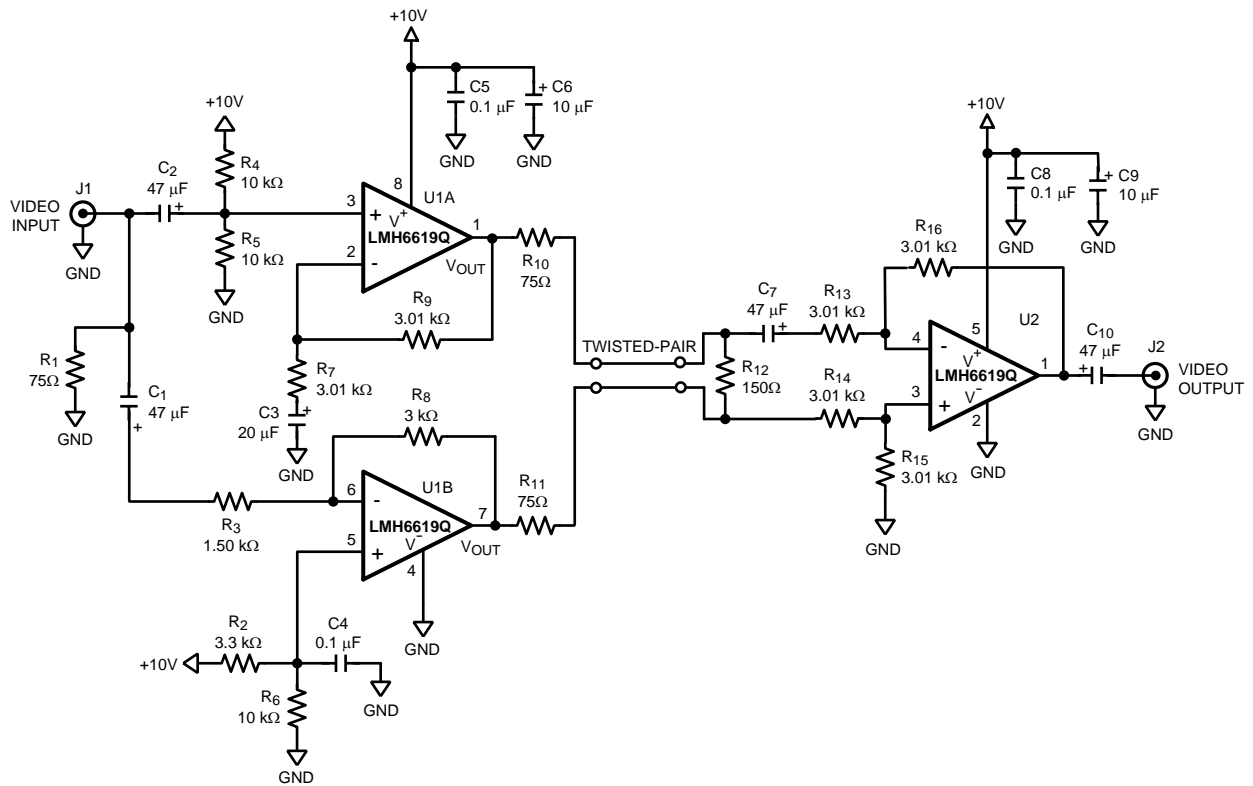


Figure 12. Differential Cable Driver

PRODUCT PREVIEW



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6619QMAK/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	LMH66 19QMA	<a href="#">Samples</a>
LMH6619QMAKE/NOPB	ACTIVE	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	LMH66 19QMA	<a href="#">Samples</a>
LMH6619QMAKX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	LMH66 19QMA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF LMH6619-Q1 :**

- Catalog: [LMH6619](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



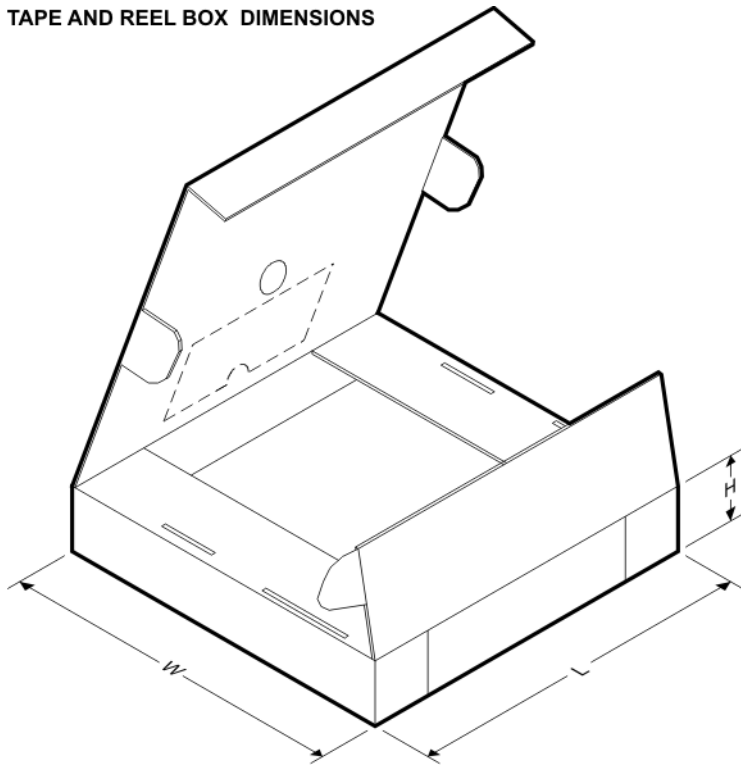
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6619QMAKE/NOPB	SOIC	D	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6619QMAKX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

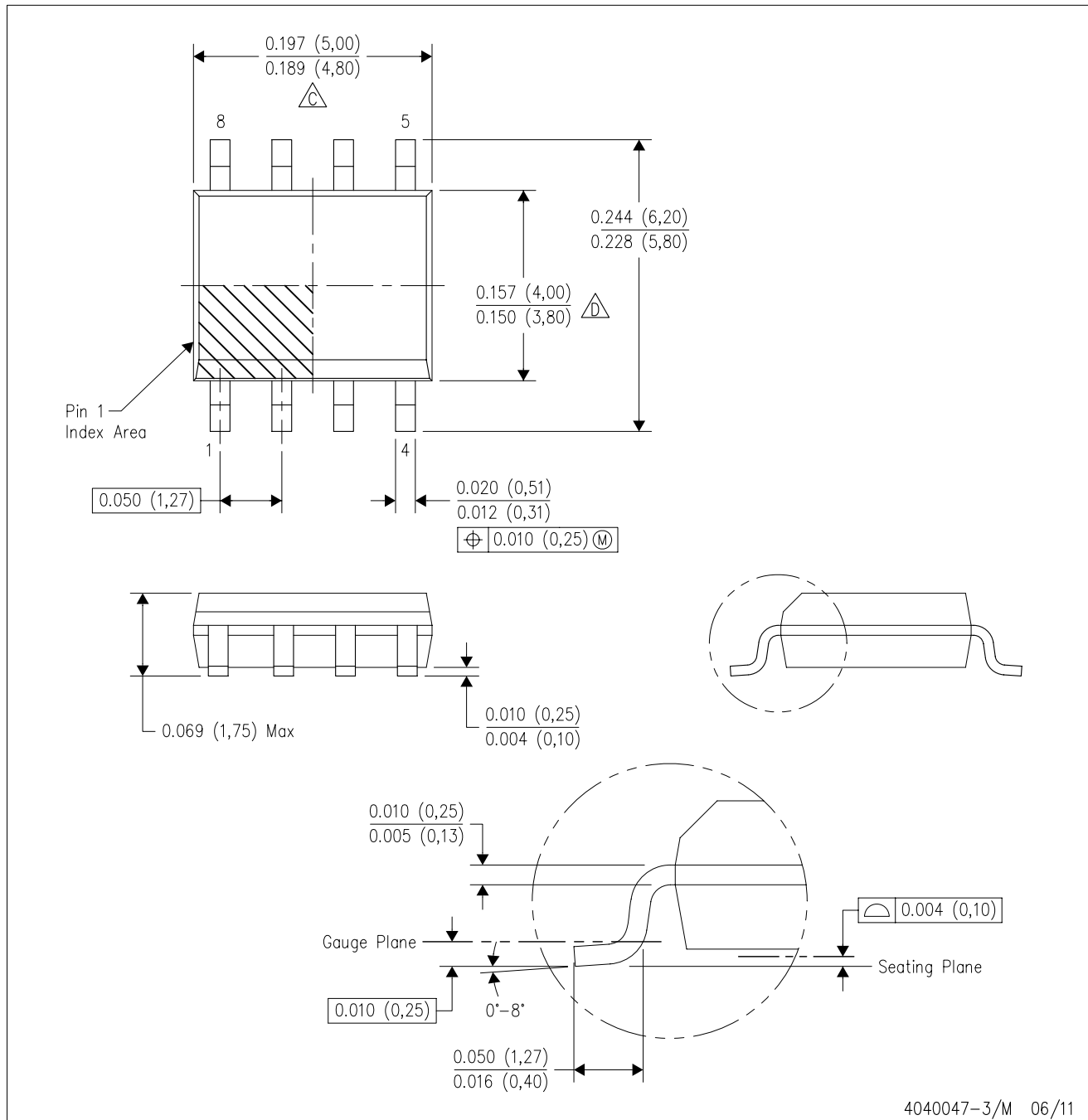


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6619QMAKE/NOPB	SOIC	D	8	250	210.0	185.0	35.0
LMH6619QMAKX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

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