

# LM1202

*LM1202 230 MHz Video Amplifier System*



Literature Number: SNVS105

## LM1202 230 MHz Video Amplifier System

### General Description

The LM1202 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications. In addition to the wideband video amplifier the LM1202 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0V to 4V range for easy interface to bus controlled alignment systems. The LM1202 operates from a nominal 12V supply but can be operated with supply voltages down to 8V for applications that require reduced IC package power dissipation characteristics.

### Features

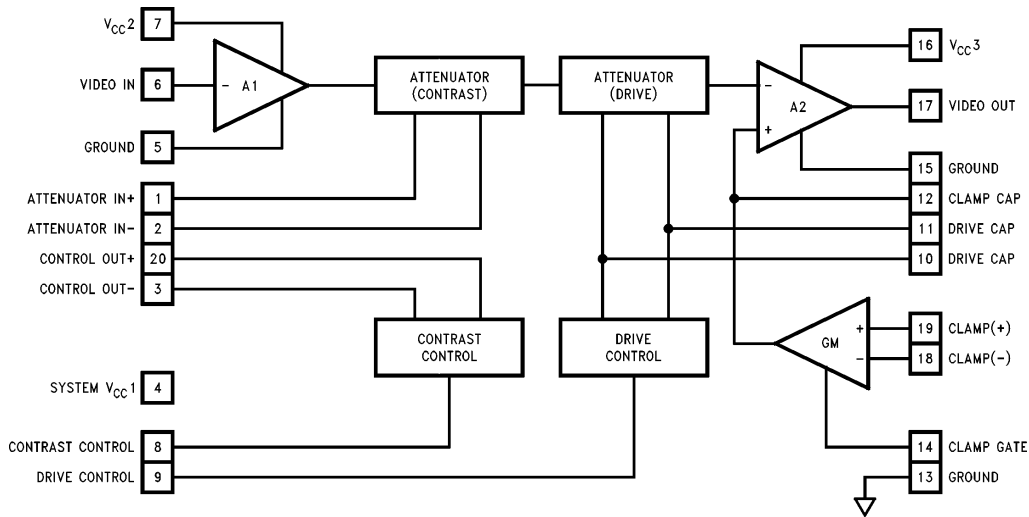
- Wideband video amplifier  
( $f_{-3dB} = 230 \text{ MHz}$  at  $V_O = 4 \text{ V}_{PP}$ )
- $t_r, t_f = 1.5 \text{ ns}$  at  $V_O = 4 \text{ V}_{PP}$

- Externally gated comparator for brightness control
- 0V to 4V high input impedance DC contrast control (>40 dB range)
- 0V to 4V high input impedance DC drive control ( $\pm 3 \text{ dB}$  range)
- Easy to parallel three LM1202s for optimum color tracking in RGB systems
- Output stage clamps to 0.65V and provides up to 9V output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

### Applications

- High resolution CRT monitors
- Video switches
- Video AGC amplifier
- Wideband amplifier with gain and DC offset control

### Block and Connection Diagram



Order Number LM1202N or LM1202M  
See NS Package Number N20A or M20B

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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $V_{CC}$ Pins 4, 7, 16 to Ground Pins 5, 13, 15	13.5V
Voltage at Any Input Pin ( $V_{IN}$ )	$V_{CC} \geq V_{IN} \geq GND$
Video Output Current ( $I_{17}$ )	28 mA
Package Power Dissipation at $T_A = 25^\circ\text{C}$ (Above $25^\circ\text{C}$ Derate Based $\theta_{JA}$ and $T_J$ )	1.56W
Package Thermal Resistance ( $\theta_{JA}$ )	
N20A	68°C/W
M20B	90°C/W

Junction Temperature ( $T_J$ )	150°C
Storage Temperature Range ( $T_{stg}$ )	-65°C to +150°C
Lead Temperature	
N Package (Soldering, 10 sec.)	265°C
ESD Susceptibility	
Human Body Model: 100 pF Discharged through a 1.5k Resistor	1.5 kV

## Operating Ratings (Note 2)

Temperature Range	-20°C to +80°C
Supply Voltage ( $V_{CC}$ )	$8V \leq V_{CC} \leq 13.2V$

**DC Electrical Characteristics** See Test Circuit (Figure 1),  $T_A = 25^\circ\text{C}$ ,  $V_4 = V_7 = V_{16} = 12V$ ,  $S_1$  Open,  $V_{19} = 4V$ ,  $V_8 = 4V$ ,  $V_9 = 4V$ ,  $V_{14} = 0V$  unless otherwise noted.

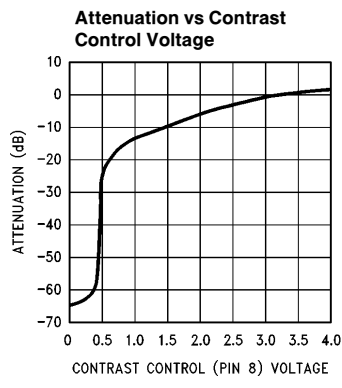
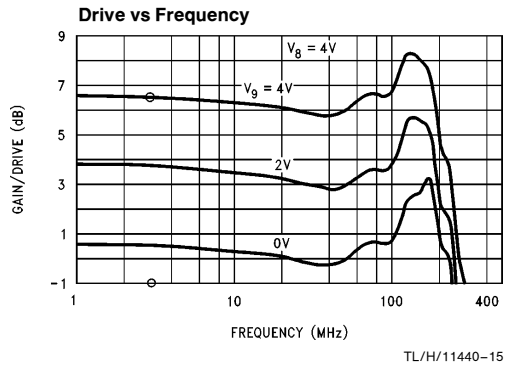
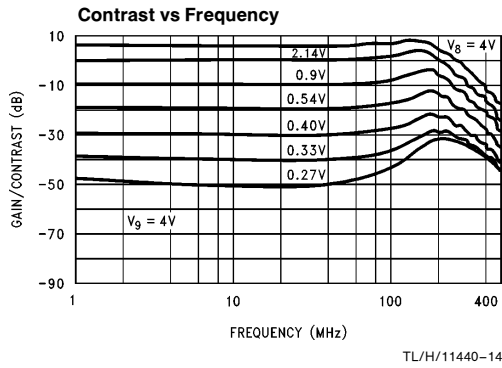
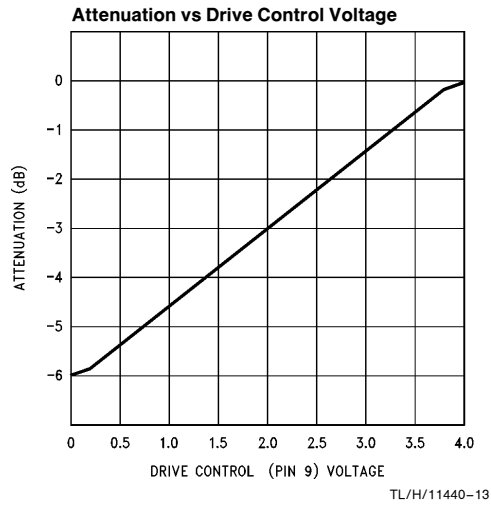
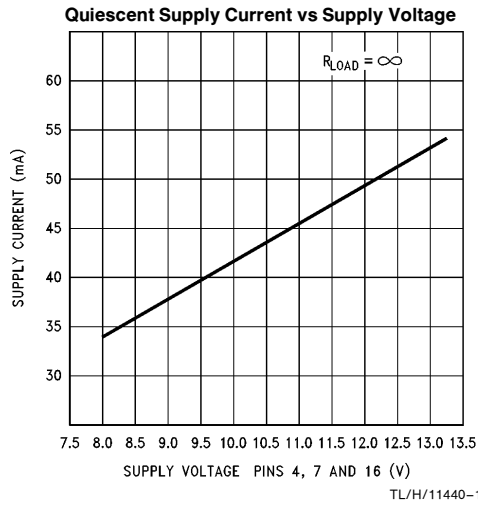
Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
$I_S$ 4, 7, 16	Total Supply Current	$R_{Load} = \infty$ (Note 5)	48	60	mA (max)
$V_6$	Video Input Bias Voltage		2.4	2	V (min)
$V_{14L}$	Clamp Gate Low Input Voltage	Clamp Comparator On		0.8	V (max)
$V_{14H}$	Clamp Gate High Input Voltage	Clamp Comparator Off		2	V (min)
$I_{14L}$	Clamp Gate Low Input Current	$V_{14} = 0V$	-0.5		$\mu\text{A}$
$I_{14H}$	Clamp Gate High Input Current	$V_{14} = 12V$	0.005		$\mu\text{A}$
$I_{12+}$	Clamp Cap Charge Current	$V_{12} = 0V$	800	500	$\mu\text{A}$ (min)
$I_{12-}$	Clamp Cap Discharge Current	$V_{12} = 5V$	-800	-500	$\mu\text{A}$ (min)
$V_{17L}$	Video Output Low Voltage	$V_{12} = 0V$	0.2	0.65	V (max)
$V_{17H}$	Video Output High Voltage	$V_{12} = 6V$	10	9	V (min)
$V_{OS}$	Comparator Input Offset Voltage	$V_{18} - V_{19}$	15	$\pm 50$	mV (max)

**AC Electrical Characteristics** See Test Circuit (Figure 1),  $T_A = 25^\circ\text{C}$ ,  $V_4 = V_7 = V_{16} = 12V$ ,  $S_1$  Closed,  $V_{19} = 4V$ ,  $V_8 = 4V$ ,  $V_9 = 4V$ ,  $V_{14} = 0V$  unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
$R_{IN}$	Video Amplifier Input Resistance	$f_{IN} = 12\text{ kHz}$	20		$k\Omega$
$A_V$ max	Video Amplifier Gain	$V_8 = 4V$ , $V_9 = 4V$	20	16	V/V (min)
$\Delta A_V$ 2V	Attenuation at 2V	Ref: $A_V$ max, $V_8 = 2V$	-6		dB
$\Delta A_V$ 0.5V	Attenuation at 0.5V	Ref: $A_V$ max, $V_8 = 0.5V$	-38	-23	dB (min)
$\Delta$ Drive	$\Delta$ Gain Range	$V_9 = 0V$ to $4V$	6	5	dB (min)
THD	Video Amplifier Distortion	$V_O = 4 V_{PP}$ , $f_{IN} = 12\text{ kHz}$	0.5	1	% (max)
$f_{-3\text{ dB}}$	Video Amplifier Bandwidth (Note 6)	$V_O = 4 V_{PP}$	230		MHz
$t_r$	Output Rise Time (Note 6)	$V_O = 4 V_{PP}$	1.5	2	ns (max)
$t_f$	Output Fall Time (Note 6)	$V_O = 4 V_{PP}$	1.5	2	ns (max)



**Typical Performance Characteristics** ( $V_{CC} = 12V$ ,  $T_A = 25^\circ C$  unless otherwise specified)



## Circuit Description

Figure 2 shows a block diagram of the LM1202 video amplifier along with contrast and brightness (black level) control. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. As shown in Figure 2, pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independent gain adjustment of each channel is required.

The brightness or black level clamping requires a "sample and hold" circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration, is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period (see Figure 2). When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the

voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width ( $t_W$  in Figure 2) must be greater than 100 ns for proper operation.

### VIDEO AMPLIFIER SECTION (Input Stage)

A simplified schematic of LM1202's video amplifier input stage is shown in Figure 3. The 5.4V zener diode, Q1, Q6 and R2 bias the base of Q7 at 2.6V. The AC coupled video signal applied to pin 6 is referenced to the 2.6V voltage. Transistor Q7 buffers the video signal,  $V_{IN}$ , and Q8 converts the voltage to current. The AC collector current through Q8 is  $I_{C8} = V_{IN}/R9$ . Under maximum gain condition, transistors Q9 and Q11 are off and all of  $I_{C8}$  flows through the load resistors R10 and R11. The maximum signal gain at the base of Q13 is,  $A_{V1} = -(R10 + R11)/R9 = -2$ . Signal attenuation is achieved by varying the base drive to the differential pairs Q9, Q10 and Q11, Q12 thereby unbalancing the collector currents through the transistor pairs. Base of Q10 is biased at 5.3V by externally connecting pin 1 to pin 20 through a 100Ω resistor. Pin 2 is connected to pin 3 through a 100Ω resistor. Adjusting the contrast voltage at

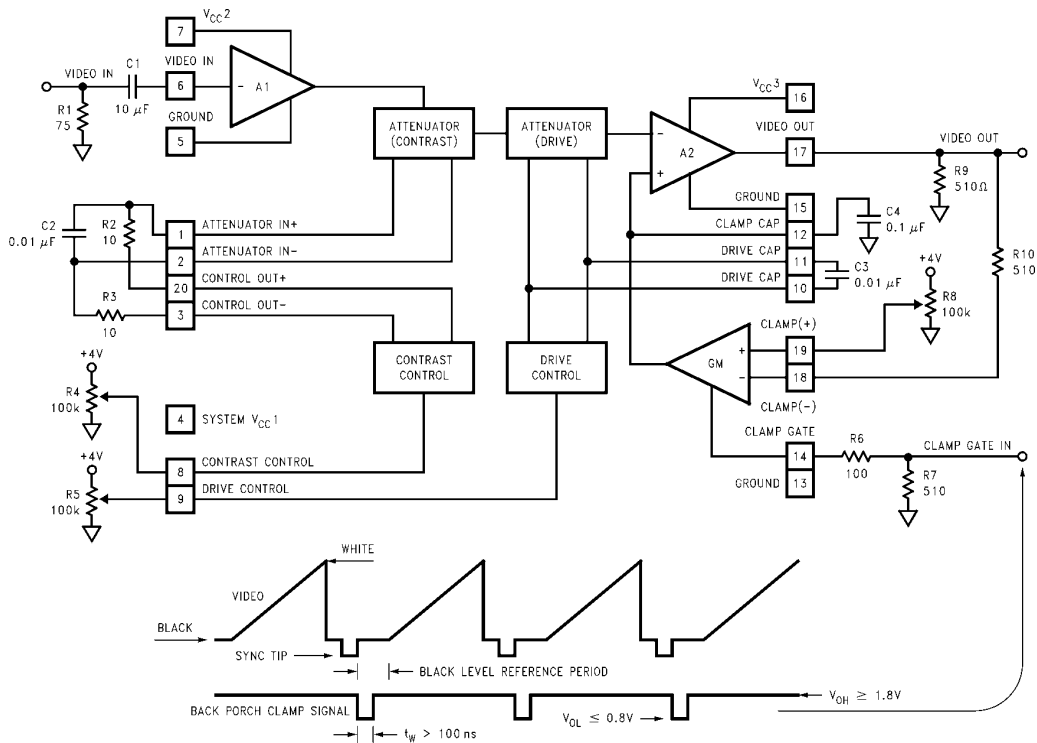


FIGURE 2. Block Diagram of the LM1202 Video Amplifier with Contrast and Brightness (Black Level) Control

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### Circuit Description (Continued)

pin 8 produces a control voltage at pin 3 which drives the base of Q9. By varying the voltage at the base of Q9, Q8's collector current ( $I_{C8}$ ) is diverted away from the load resistors R10 and R11, thereby providing signal attenuation. Maximum attenuation is achieved when all of  $I_{C8}$  flows through Q9 and no current flows through the load resistors.

The differential pair Q11 and Q12 provide drive control. Q12's base is internally biased at 7.3V. Adjusting the voltage at the drive control input (pin 9) produces a control voltage at the base of Q11. With Q9 off and Q12 off, all of  $I_{C8}$  flows through R10, thus providing a gain of  $A_{V1} = -(R10/R9) \times V_{IN} = -1$ . Drive control thus provides a 6 dB attenuation range.

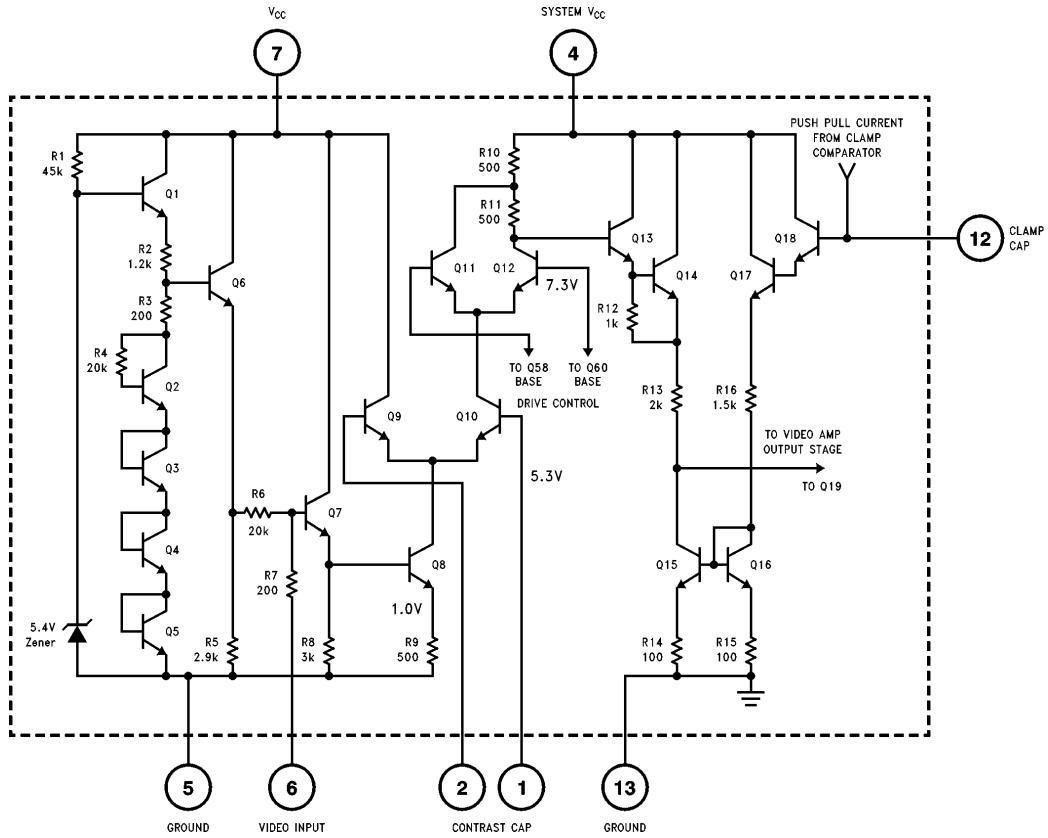


FIGURE 3. Simplified Schematic of the LM1202 Video Amplifier Input Stage

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## Circuit Description (Continued)

### VIDEO AMPLIFIER SECTION (Output Stage)

A simplified schematic of LM1202's video amplifier output stage is shown in *Figure 4*. The output stage is the second gain stage. Ideally the gain of the second gain stage would be  $A_{V2} = -R21/R18 = -16$ . Because of the output stage's low open loop gain, the gain is approximately  $A_{V2} = -10$ . Thus the maximum gain of the video amplifier is  $A_V = A_{V1} \times A_{V2} = 20$ . Transistors Q23 and Q24 provide a push-pull drive to the load. The output voltage can swing from 0.2V to 10V.

### CONTRAST CONTROL SECTION

A simplified schematic of LM1202's contrast control section is shown in *Figure 5*. A 0V to 4V DC voltage is applied at the contrast input (pin 8). Transistors Q29, Q30 and Q34 buffer and level shift the contrast voltage to the base of Q36. The voltage at the emitter of Q36 equals the contrast voltage ( $V_{cont}$ ) and the current through Q36's collector is given by  $I_{C36} = V_{cont}/R28$ .

Transistor Q36's collector current is used to unbalance the current through the differential pair comprised of Q38

and Q40. Q40's base is internally biased at 5.3V and made available at pin 20. Pin 20 is externally connected to pin 1 through a 100Ω resistor (see *Figures 2 and 3*). The base of Q38 (pin 3) is externally connected to pin 2 through a 100Ω resistor (see *Figures 2 and 3*). With  $V_{cont} = 2V$ , the differential pair (Q38, Q40) is balanced and the voltage at pins 1 and 2 is 5.3V. Under this condition, Q8's collector current is equally split between Q9 and Q10 (see *Figure 3*) and the amplifier's gain is half the maximum gain. If contrast voltage at pin 8 is greater than 2V then Q36's collector current increases, thus pulling Q38's collector node lower and consequently moving Q38's base below 5.3V. With pin 2 at a lower voltage than pin 1, current through Q10 (see *Figure 3*) increases and the amplifier's gain increases. With  $V_{cont} = 4V$ , the amplifier's gain is maximum.

If the contrast voltage at pin 8 is less than 2V then Q36's collector current decreases and Q38's base is pulled above 5.3V. With pin 2 voltage greater than pin 1 voltage, less current flows through Q10 (see *Figure 3*), consequently the amplifier's gain decreases. With  $V_{cont} = 0V$ , the amplifier's gain is minimum (i.e., maximum attenuation).

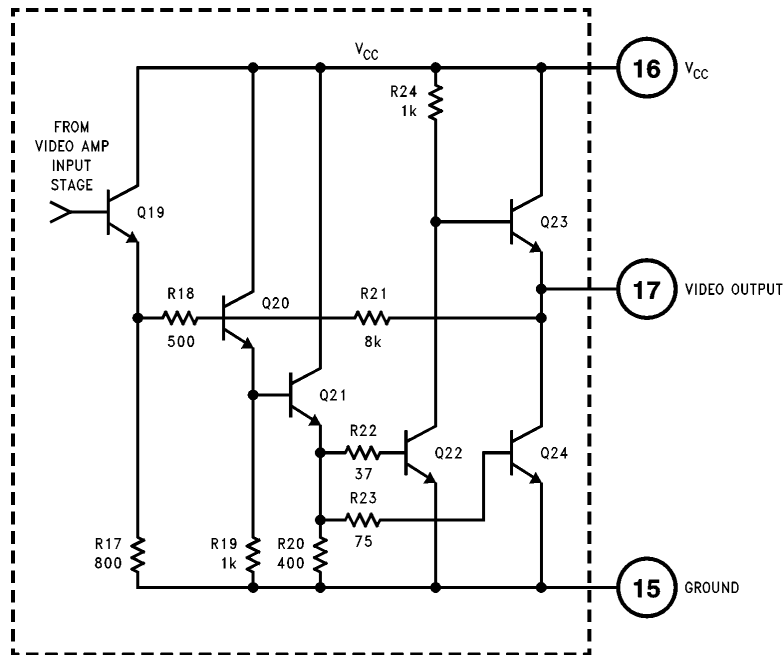
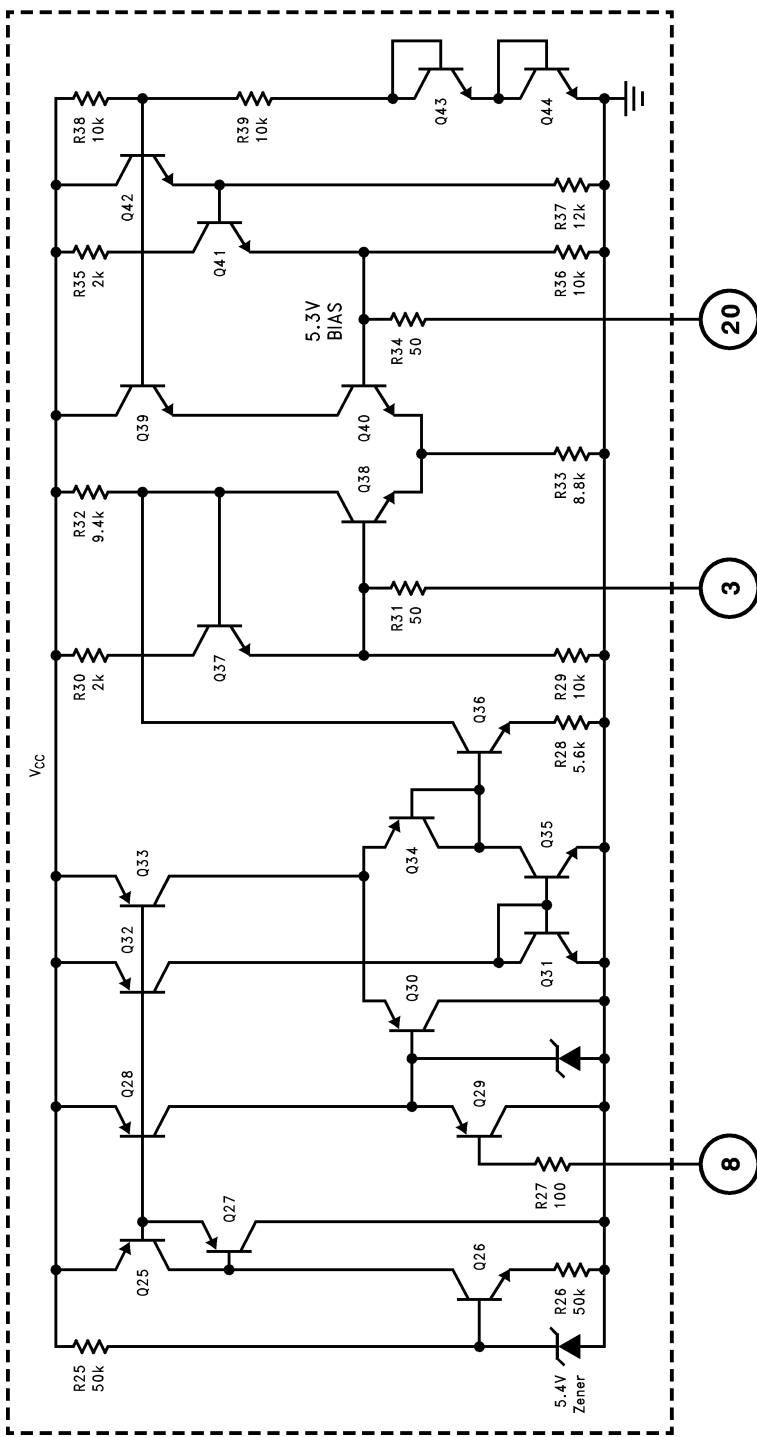


FIGURE 4. Simplified Schematic of LM1202 Video Amplifier Output Stage

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Circuit Description (Continued)



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FIGURE 5. Simplified Schematic of LM1202 Contrast Control

CONTRAST CONTROL INPUT

## Circuit Description (Continued)

### DRIVE CONTROL SECTION

A simplified schematic of the LM1202's drive control section is shown in *Figure 6*. A 0V to 4V DC voltage is applied at the drive control input (pin 9). Transistors Q49, Q50 and Q54 buffer and level shift the contrast voltage to the base of Q56. The voltage at the emitter of Q56 equals the drive voltage,  $V_{drive}$  and the current through Q56's collector is given by  $I_{C56} = V_{drive}/R43$ .

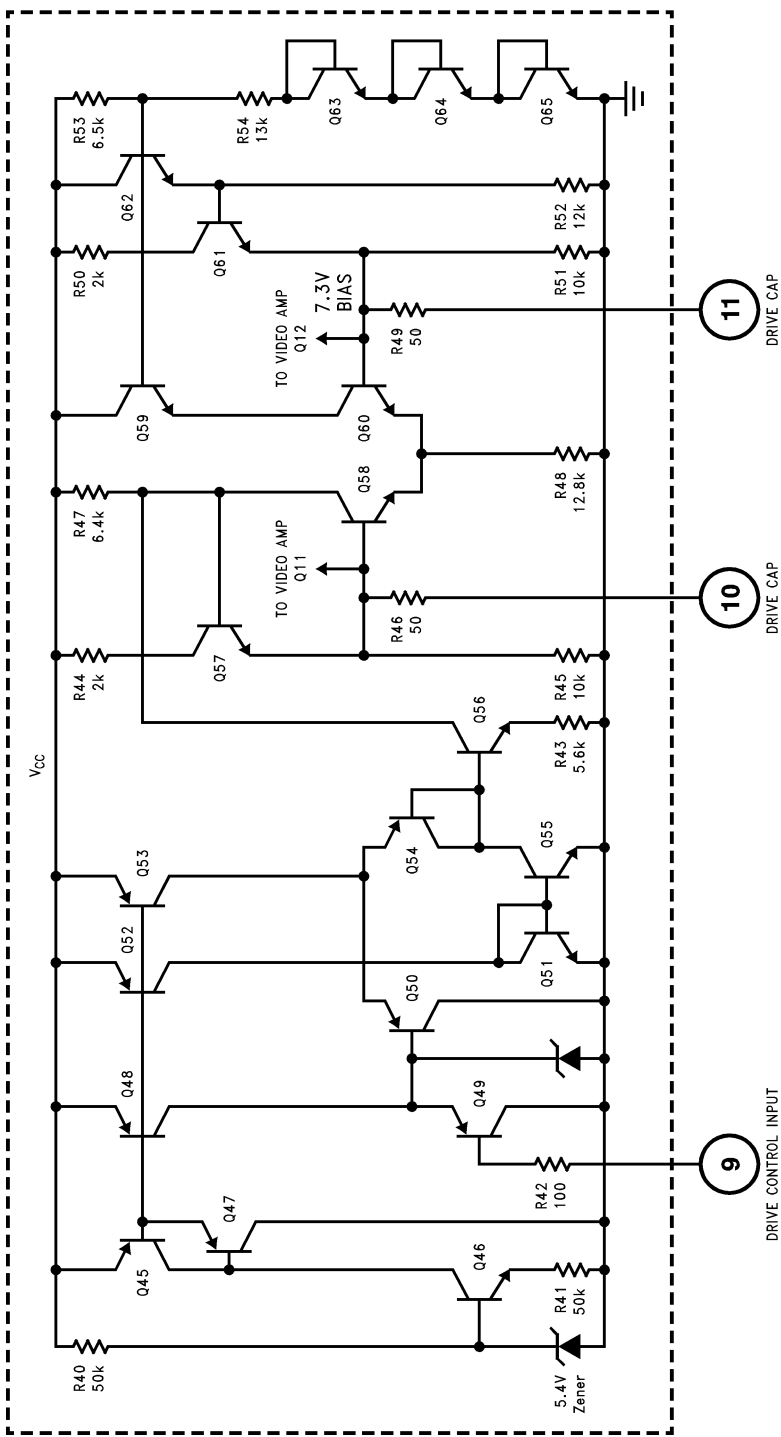
Transistor Q56's collector current is used to unbalance the current through the differential pair comprised of Q58 and Q60. Q60's base is internally biased at 7.3V and connected to the base of Q12 (see *Figure 3*). Q58's base is internally connected to the base of Q11 (see *Figure 3*). With  $V_{cont} = 2V$ , the differential pair (Q58, Q60) is balanced and the voltage at the bases of Q11 and Q12 is 7.3V. Under this condition, Q10's collector current is equally split between Q11 and Q12 (see *Figure 3*). If the drive voltage at pin 9 is greater than 2V then Q56's collector current increases, thus pulling Q58's collector node lower and consequently moving Q58's base below 7.3V. With base of Q11 below 7.3V, current through Q12 (see *Figure 3*) increases and the amplifier's gain increases. With  $V_{drive} = 4V$ , the amplifier's gain is maximum under maximum contrast condition (i.e.,  $V_{cont} = 4V$ ).

If the drive voltage at pin 8 is less than 2V then Q56's collector current decreases and Q58's base is pulled above 7.3V. With base of Q11 greater than 7.3V, less current flows through Q12 (see *Figure 3*), consequently the amplifier's gain decreases. With  $V_{drive} = 0V$ , the amplifier's gain is 6 dB less than the maximum gain.

### CLAMP GATE AND CLAMP COMPARATOR SECTION

*Figures 7* and *8* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit (*Figure 7*) consists of a PNP input buffer transistor (Q82), a PNP emitter coupled pair (Q85 and Q86) referenced on one side to 2.1V and an output switch transistor Q89. When the clamp gate input at pin 14 is high ( $> 1.5V$ ) the Q89 switch is on and shunts the 200  $\mu A$  current from current source Q90 to ground. When pin 14 is low ( $< 1.3V$ ) the Q89 switch is off and the 200  $\mu A$  current is mirrored by the current mirror comprised of Q91 and Q75 (see *Figure 8*). Consequently the clamp comparator comprised of the differential pair Q74 and Q77 is enabled. The input of the clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitor externally connected from pin 12 to ground. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNP's will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage ( $BV_{ebo}$ ). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the  $BV_{ebo}$  of NPN transistors, a resistor (R63) with a value one half that of R60 or R68 is connected between the bases of Q71 and Q79. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is  $V_{CC}$ .

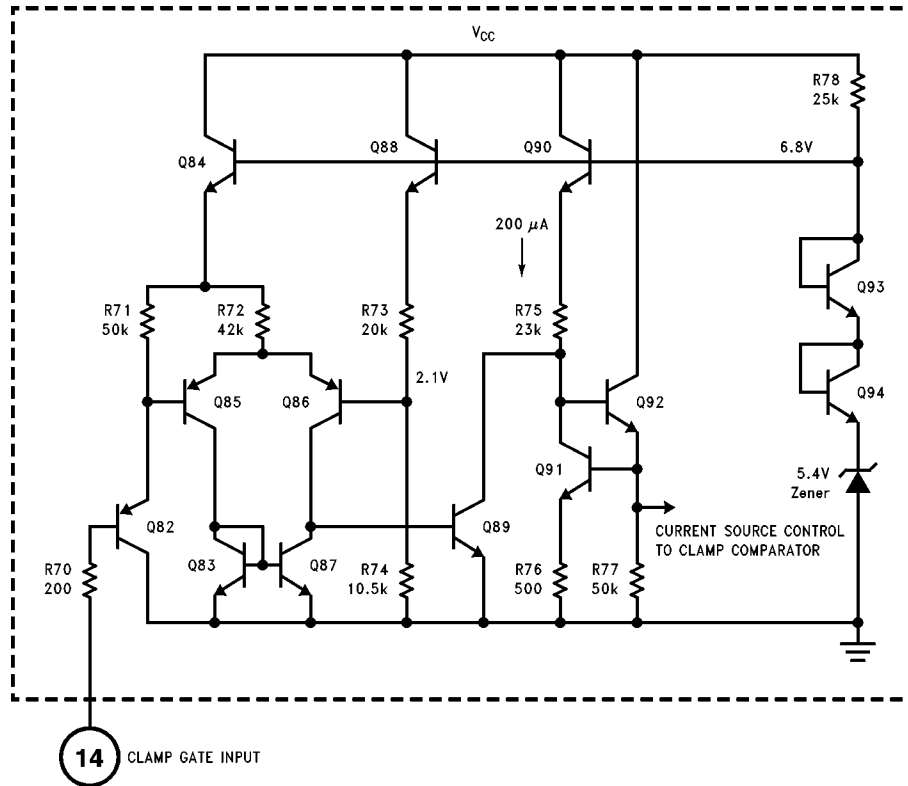
Circuit Description (Continued)



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FIGURE 6. Simplified Schematic of the LM1202 Drive Control

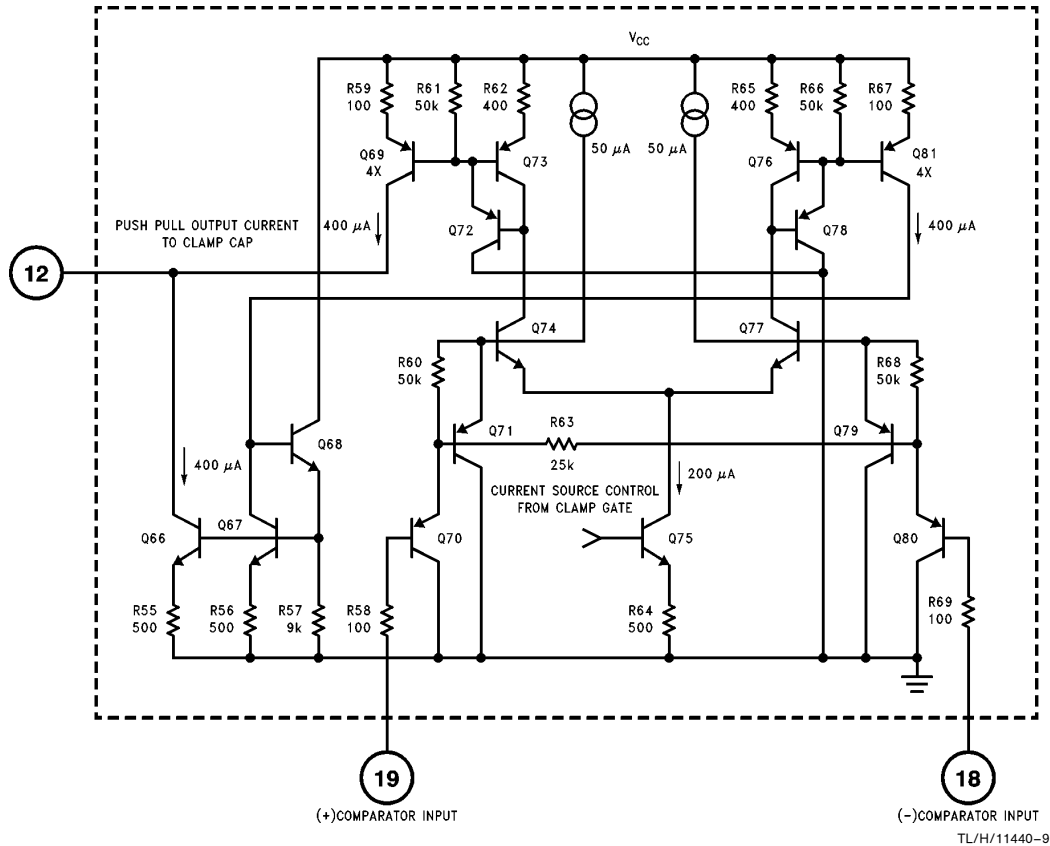
**Circuit Description** (Continued)



**FIGURE 7. Simplified Schematic of the LM1202 Clamp Gate Circuit**

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**Circuit Description** (Continued)



**FIGURE 8. Simplified Schematic of the LM1202 Clamp Comparator Circuit**

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## Applications of the LM1202

### SINGLE VIDEO CHANNEL

A typical application for a single video channel is shown in *Figure 9*. The video signal is AC coupled to pin 6. The LM1202 internally biases the video signal to  $2.6 V_{DC}$ . Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifier's gain is minimum (i.e., maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval (see *Figure 2*). The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A  $510\Omega$  load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than  $510\Omega$ .

### RGB VIDEO PREAMPLIFIER

*Figure 10* shows an RGB video preamplifier circuit using three LM1202s. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC-coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC-coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 to the black level voltage by using a voltage divider at pin 19.

# Applications of the LM1202 (Continued)

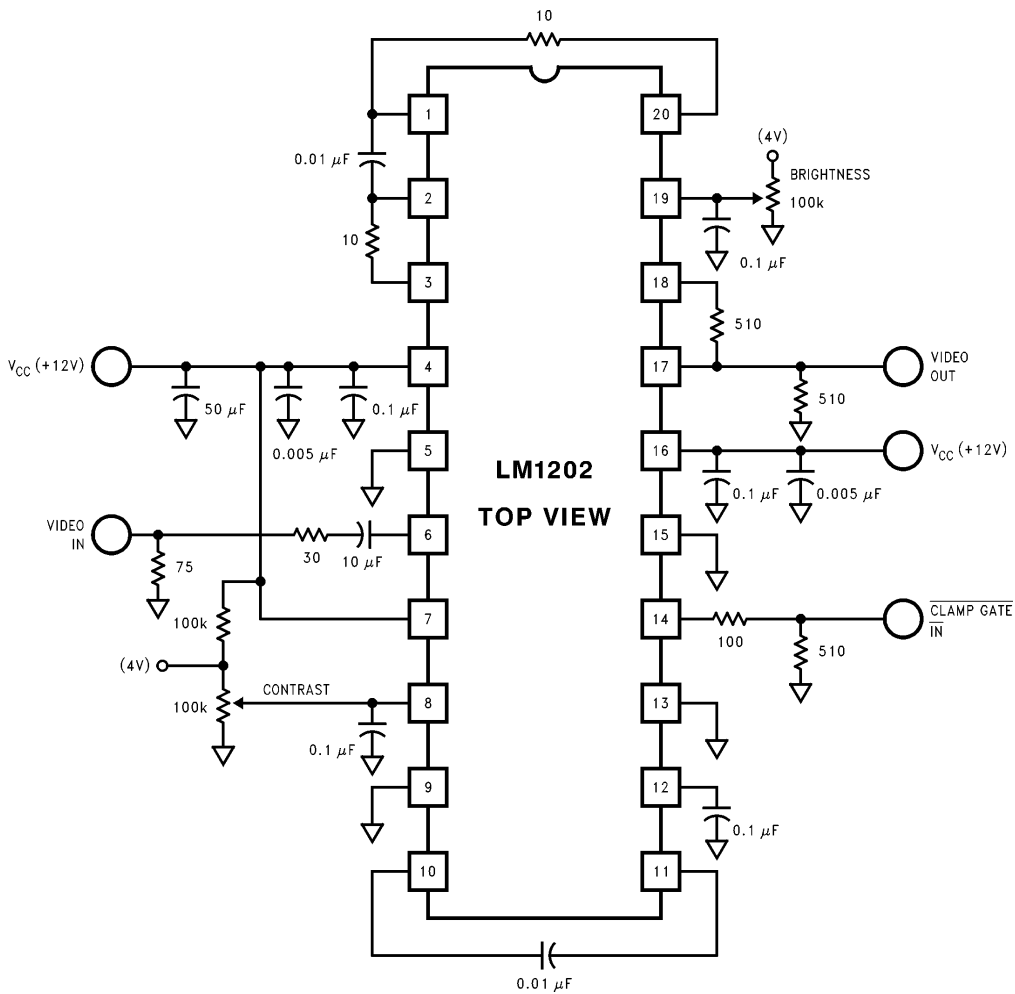


FIGURE 9. Typical LM1202 Application (Single Video Channel)

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## Applications of the LM1202 (Continued)

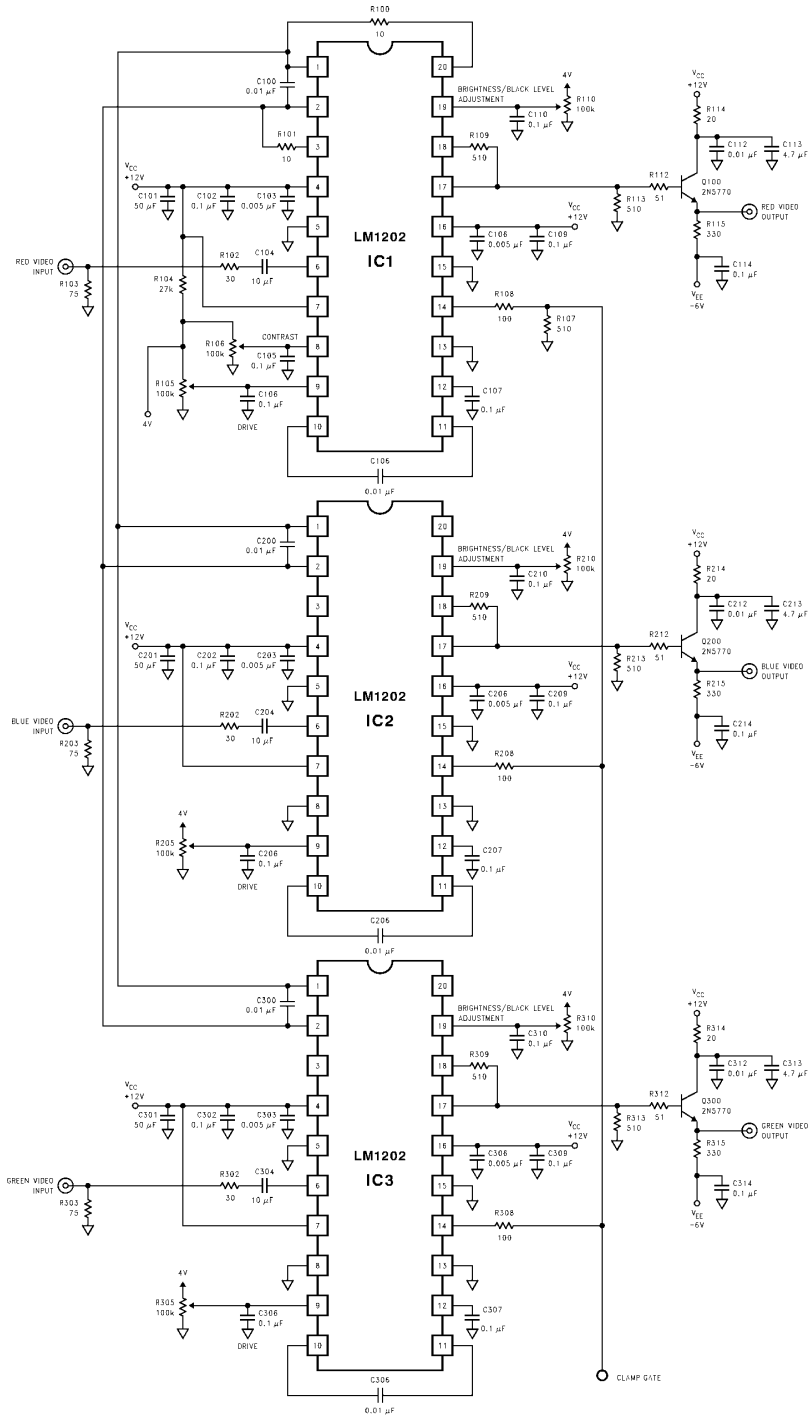


FIGURE 10. Typical RGB Application with Contrast, Drive and Black Level (Cutoff) Control

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### **Power Down Characteristics**

The LM1202 includes a built-in power down spot killer to prevent a flash on the screen upon power down. The LM1202's output voltage decreases as the device is being powered down, thus preventing a flash on the screen. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter-than-white level at the output of the CRT driver, thus causing a flash on the screen.

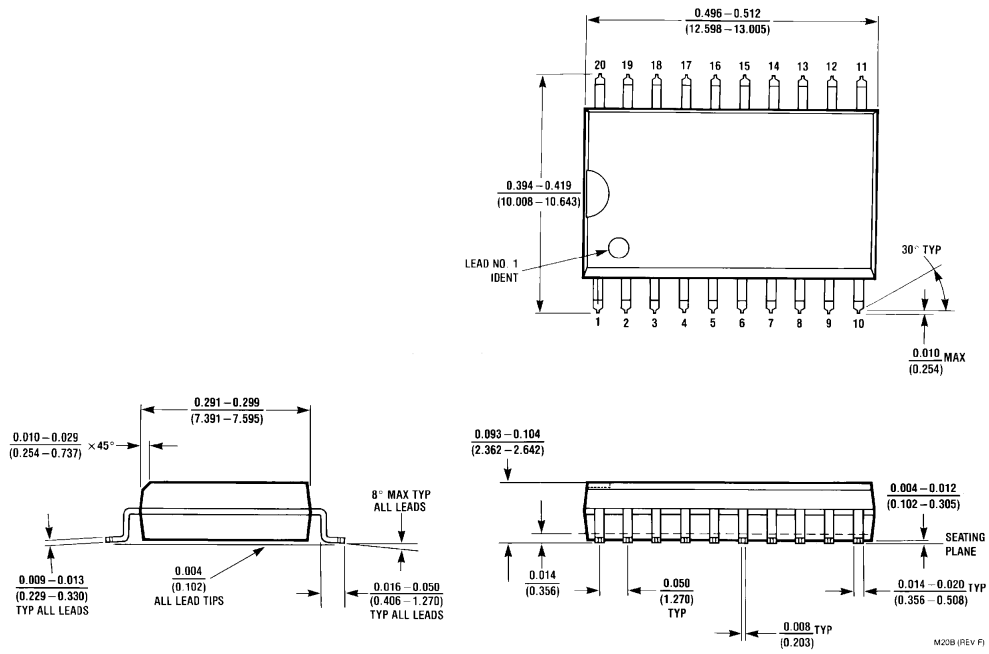
### **PC Board Layout Considerations**

For optimum performance and stable operation, a double-sided printed circuit board with adequate ground plane and power supply decoupling as close to the  $V_{CC}$  pins as possible is recommended. For suggestions on optimum PC board layout, please see the reference section below.

### **Reference**

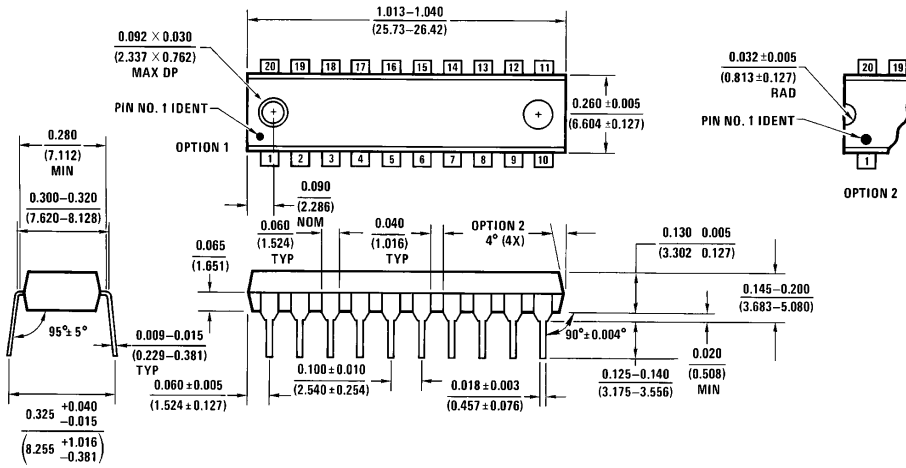
Ott, Henry W, *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, New York, 1976.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**Order Number LM1202M**  
**NS Package Number M20B**

**Physical Dimensions** inches (millimeters) unless otherwise noted



**Order Number LM1202N**  
**NS Package Number N20A**

N20A (REV G)

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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