LM2705 Micropower Step-up DC/DC Converter with 150mA Peak Current Limit

Check for Samples: LM2705

FEATURES

- **150mA, 0.7Ω, internal switch**
- **Uses small surface mount components**
- **Adjustable output voltage up to 20V**
- **2.2V to 7V input range**
- **Input undervoltage lockout**
- **0.01µA shutdown current**
- **Small 5-Lead SOT-23 package**

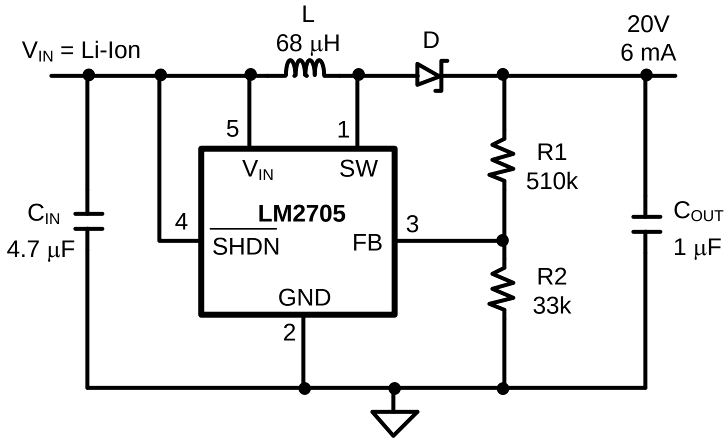
APPLICATIONS

- **LCD Bias Supplies**
- **White LED Back-Lighting**
- **Handheld Devices**
- **Digital Cameras**
- **Portable Applications**

DESCRIPTION

The LM2705 is a micropower step-up DC/DC in a small 5-lead SOT-23 package. A current limited, fixed off-time control scheme conserves operating current resulting in high efficiency over a wide range of load conditions. The 21V switch allows for output voltages as high as 20V. The low 400ns off-time permits the use of tiny, low profile inductors and capacitors to minimize footprint and cost in space-conscious portable applications. The LM2705 is ideal for LCD panels requiring low current and high efficiency as well as white LED applications for cellular phone back-lighting. The LM2705 can drive up to 3 white LEDs from a single Li-Ion battery. The low peak inductor current of the LM2705 makes it ideal for USB applications.

Typical Application Circuit

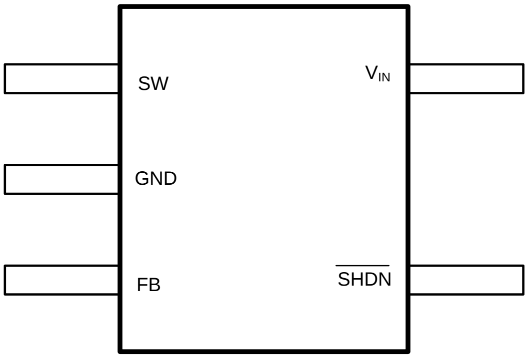


C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-683
D: ON Semiconductor MBRM130LT3

Figure 1. Typical 20V Application

Connection Diagram

Top View



The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = $(T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

Figure 2. SOT23-5
T_{Jmax} = 125°C, θ_{JA} = 220°C/W

PIN DESCRIPTIONS

Pin	Name	Function
1	SW	Power Switch input.
2	GND	Ground.
3	FB	Output voltage feedback input.
4	$\overline{SHDN}$	Shutdown control input, active low.
5	V_{IN}	Analog and Power input.

SW(Pin 1): Switch Pin.

This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.

GND(Pin 2): Ground Pin.

Tie directly to ground plane.

FB(Pin 3): Feedback Pin.

Set the output voltage by selecting values for R1 and R2 using:

$$R1 = R2 \left(\frac{V_{OUT}}{1.237V} - 1 \right) \quad (1)$$

Connect the ground of the feedback network to an AGND plane which should be tied directly to the GND pin.

$\overline{SHDN}$(Pin 4): Shutdown Pin.

The shutdown pin is an active low control. Tie this pin above 1.1V to enable the device. Tie this pin below 0.3V to turn off the device.

V_{IN}(Pin 5): Input Supply Pin.

Bypass this pin with a capacitor as close to the device as possible.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

V_{IN}	7.5V
SW Voltage	21V
FB Voltage	2V
$\overline{\text{SHDN}}$ Voltage	7.5V
Maximum Junction Temp. T_J (3)	150°C
Lead Temperature (Soldering 10 sec.)	300°C
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Ratings (4) Human Body Model Machine Model (5)	 2kV 200V

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = $(T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

(5) ESD susceptibility using the machine model is 150V for SW pin.

Operating Conditions

Junction Temperature (1)	−40°C to +125°C
Supply Voltage	2.2V to 7V
SW Voltage Max.	20.5V

(1) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are 100% production tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

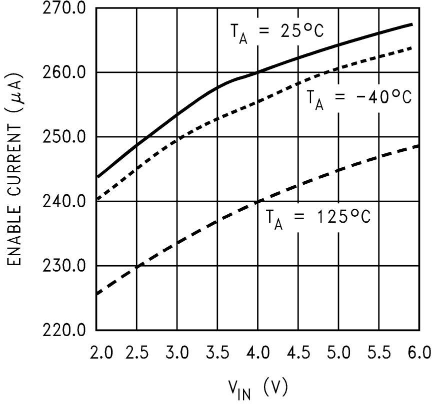
Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified V_{IN} =2.2V.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_Q	Device Disabled	FB = 1.3V		40	**70**	µA
	Device Enabled	FB = 1.2V		235	**300**	
	Shutdown	$\overline{\text{SHDN}}$ = 0V		0.01	2.5	
V_{FB}	FeedbackTrip Point		**1.189**	1.237	**1.269**	V
I_{CL}	Switch Current Limit		**100**	150	**180**	mA
I_B	FB Pin Bias Current	FB = 1.23V (3)		30	**120**	nA
V_{IN}	Input Voltage Range		**2.2**		**7.0**	V
R_{DSON}	Switch R_{DSON}			0.7	**1.6**	Ω
T_{OFF}	Switch Off Time			400		ns
I_{SD}	$\overline{\text{SHDN}}$ Pin Current	$\overline{\text{SHDN}}$ = V_{IN}, T_J = 25°C		0	80	nA
		$\overline{\text{SHDN}}$ = V_{IN}, T_J = 125°C		15		
		$\overline{\text{SHDN}}$ = GND		0		
I_L	Switch Leakage Current	V_{SW} = 20V		0.05	5	µA
UVP	Input Undervoltage Lockout	ON/OFF Threshold		1.8		V
V_{FB} Hysteresis	Feedback Hysteresis			8		mV
$\overline{\text{SHDN}}$ Threshold	$\overline{\text{SHDN}}$ low			0.7	**0.3**	V
	$\overline{\text{SHDN}}$ High		**1.1**	0.7		
θ_{JA} SOT23-5	Thermal Resistance			220		°C/W

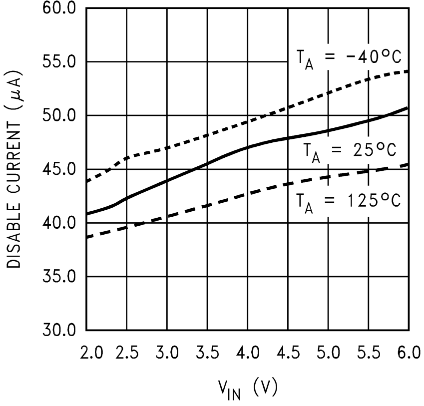
(1) All limits specified at room temperature and at **temperature extremes**. All room temperature limits are 100% production tested or specified through statistical analysis. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Feedback current flows into the pin.

Typical Performance Characteristics



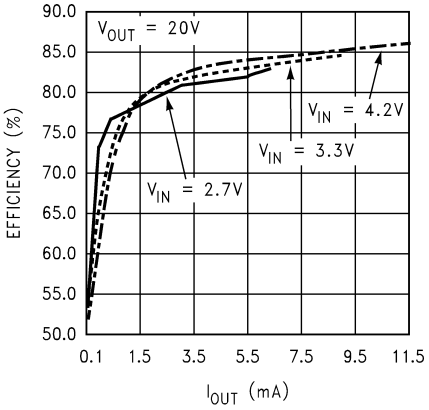
Enable Current vs V_{IN} (Part Switching)

Figure 3.



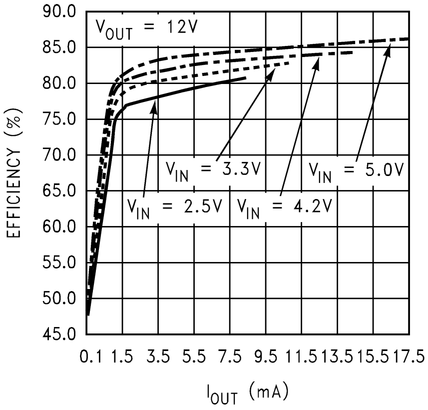
Disable Current vs V_{IN} (Part Not Switching)

Figure 4.



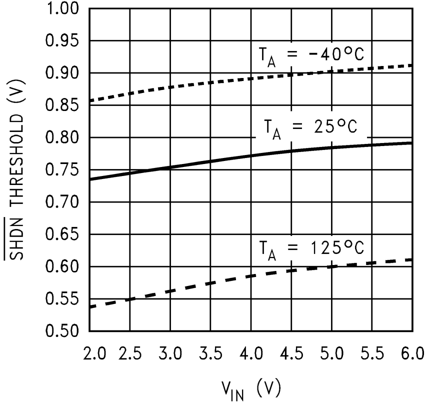
Efficiency vs Load Current

Figure 5.



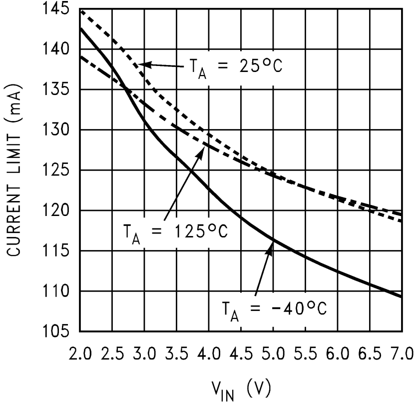
Efficiency vs Load Current

Figure 6.



$\overline{\text{SHDN}}$ Threshold vs V_{IN}

Figure 7.



Switch Current Limit vs V_{IN}

Figure 8.

Typical Performance Characteristics (continued)

Switch R_{DSON} vs V_{IN}

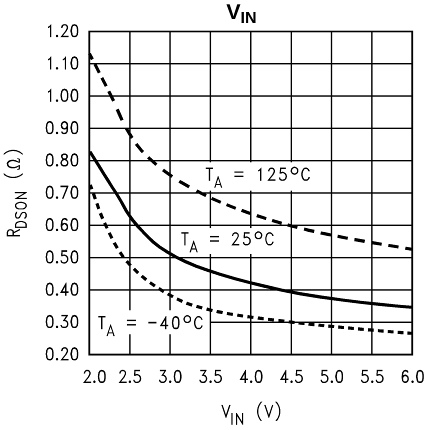


Figure 9.

FB Trip Point and FB Pin Current vs Temperature

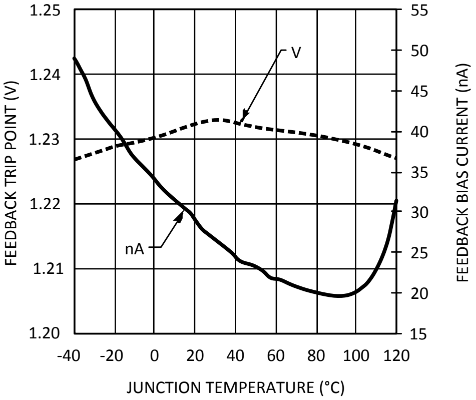


Figure 10.

Output Voltage vs Load Current

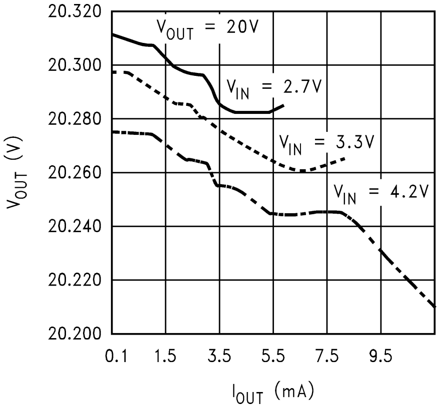


Figure 11.

Off Time vs Temperature

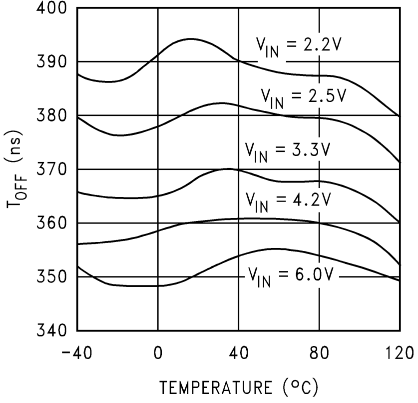
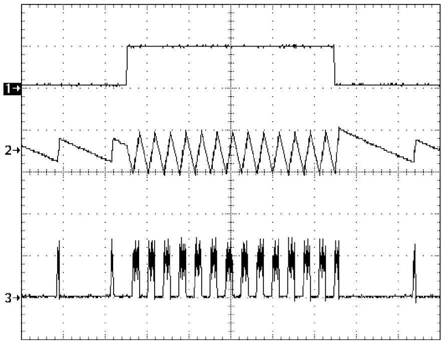


Figure 12.

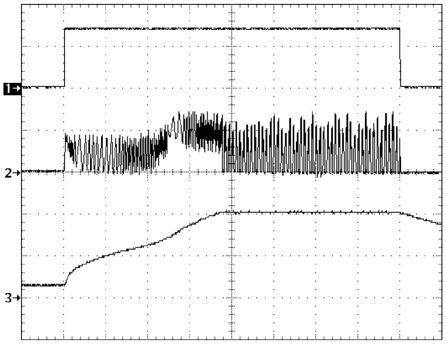
Step Response



V_{OUT} = 20V, V_{IN} = 3.0V
1) Load, 0.5mA to 5mA to 0.5mA, DC
2) V_{OUT}, 200mV/div, AC
3) I_L, 100mA/div, DC
T = 100µs/div

Figure 13.

Start-Up/Shutdown



V_{OUT} = 20V, V_{IN} = 3.0V
1) $\overline{SHDN}$, 1V/div, DC
2) I_L, 100mA/div, DC
3) V_{OUT}, 10V/div, DC
T = 400µs/div
R_L = 3.9kΩ

Figure 14.

OPERATION

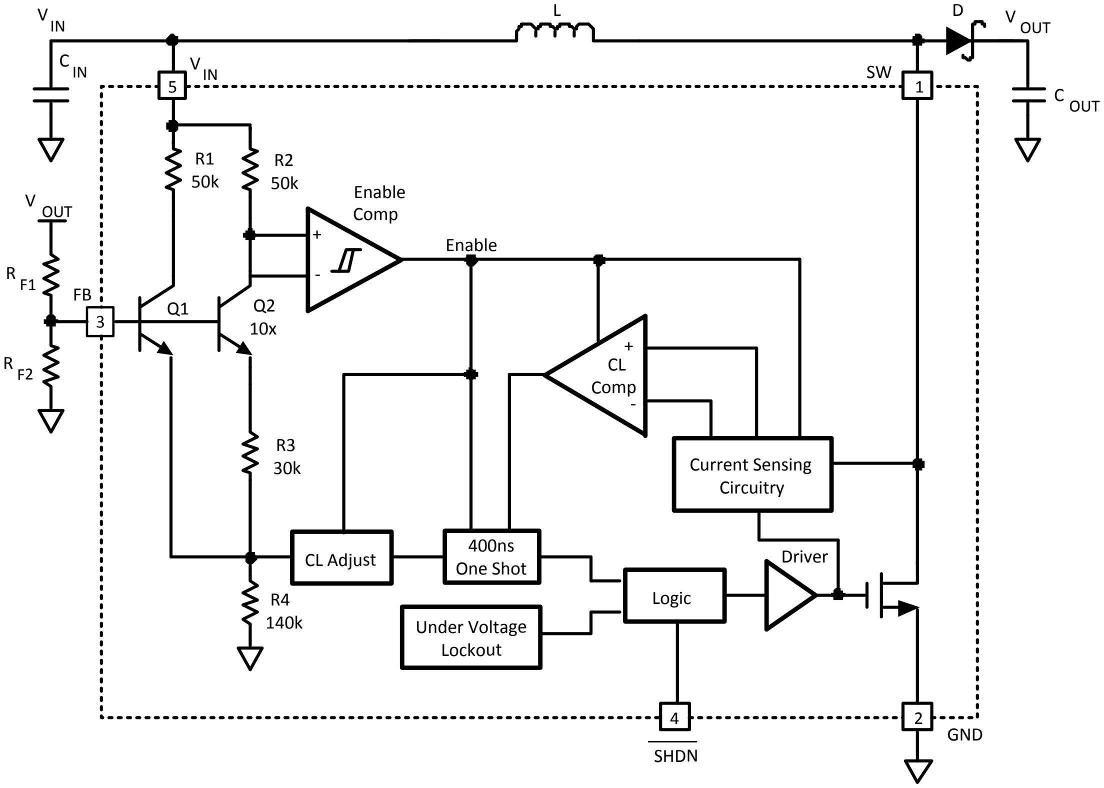
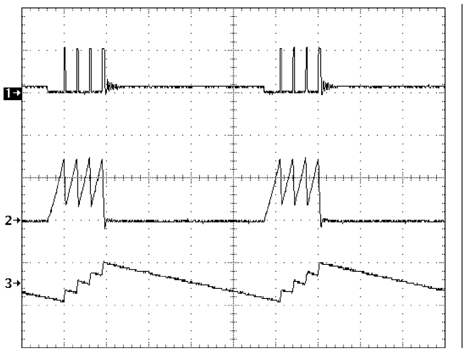


Figure 15. LM2705 Block Diagram



V_{OUT} = 20V, V_{IN} = 2.7V, I_{OUT} = 2.5mA
1) V_{SW}, 20V/div, DC
2) Inductor Current, 100mA/div, DC
3) V_{OUT}, 200mV/div, AC
T = 10µs/div

Figure 16. Typical Switching Waveform

The LM2705 features a constant off-time control scheme. Operation can be best understood by referring to Figure 15 and Figure 16. Transistors Q1 and Q2 and resistors R3 and R4 of Figure 15 form a bandgap reference used to control the output voltage. When the voltage at the FB pin is less than 1.237V, the Enable Comp in Figure 15 enables the device and the NMOS switch is turned on pulling the SW pin to ground. When the NMOS switch is on, current begins to flow through inductor L while the load current is supplied by the output capacitor C_{OUT}. Once the current in the inductor reaches the current limit, the CL Comp trips and the 400ns One Shot turns off the NMOS switch.The SW voltage will then rise to the output voltage plus a diode drop and the inductor current will begin to decrease as shown in Figure 16. During this time the energy stored in the inductor is transferred to C_{OUT} and the load. After the 400ns off-time the NMOS switch is turned on and energy is stored in the inductor again. This energy transfer from the inductor to the output causes a stepping effect in the output ripple as shown in Figure 16.

This cycle is continued until the voltage at FB reaches 1.237V. When FB reaches this voltage, the enable comparator then disables the device turning off the NMOS switch and reducing the Iq of the device to 40uA. The load current is then supplied solely by C_{OUT} indicated by the gradually decreasing slope at the output as shown in Figure 16. When the FB pin drops slightly below 1.237V, the enable comparator enables the device and begins the cycle described previously. The $\overline{\text{SHDN}}$ pin can be used to turn off the LM2705 and reduce the I_q to 0.01µA. In shutdown mode the output voltage will be a diode drop lower than the input voltage.

APPLICATION INFORMATION

INDUCTOR SELECTION - BOOST REGULATOR

The appropriate inductor for a given application is calculated using the following equation:

$$L = \left(\frac{V_{OUT} - V_{IN(min)} + V_D}{I_{CL}}\right) T_{OFF} \tag{2}$$

where V_D is the schottky diode voltage, I_{CL} is the switch current limit found in the Typical Performance Characteristics section, and T_{OFF} is the switch off time. When using this equation be sure to use the minimum input voltage for the application, such as for battery powered applications. For the LM2705 constant-off time control scheme, the NMOS power switch is turned off when the current limit is reached. There is approximately a 100ns delay from the time the current limit is reached in the NMOS power switch and when the internal logic actually turns off the switch. During this 100ns delay, the peak inductor current will increase. This increase in inductor current demands a larger saturation current rating for the inductor. This saturation current can be approximated by the following equation:

$$I_{PK} = I_{CL} + \left(\frac{V_{IN(max)}}{L}\right) 100\text{ ns} \tag{3}$$

Choosing inductors with low ESR decrease power losses and increase efficiency.

Care should be taken when choosing an inductor. For applications that require an input voltage that approaches the output voltage, such as when converting a Li-Ion battery voltage to 5V, the 400ns off time may not be enough time to discharge the energy in the inductor and transfer the energy to the output capacitor and load. This can cause a ramping effect in the inductor current waveform and an increased ripple on the output voltage. Using a smaller inductor will cause the I_{PK} to increase and will increase the output voltage ripple further.

For typical curves and evaluation purposes the DT1608C series inductors from Coilcraft were used. Other acceptable inductors would include, but are not limited to, the SLF6020T series from TDK, the NP05D series from Taiyo Yuden, the CDRH4D18 series from Sumida, and the P1166 series from Pulse.

INDUCTOR SELECTION - SEPIC REGULATOR

The following equation can be used to calculate the approximate inductor value for a SEPIC regulator:

$$L2 = 2\left(\frac{V_{OUT} + V_D}{I_{CL}}\right) T_{OFF} \tag{4}$$

The boost inductor, L1, can be smaller or larger but is generally chosen to be the same value as L2. See Figure 23 and Figure 24 for typical SEPIC applications.

DIODE SELECTION

To maintain high efficiency, the average current rating of the schottky diode should be larger than the peak inductor current, I_{PK}. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage.

CAPACITOR SELECTION

Choose low ESR capacitors for the output to minimize output voltage ripple. Multilayer ceramic capacitors are the best choice. For most applications, a 1µF ceramic capacitor is sufficient. For some applications a reduction in output voltage ripple can be achieved by increasing the output capacitor. Output voltage ripple can further be reduced by adding a 4.7pF feed-forward capacitor in the feedback network placed in parallel with RF1, see Figure 15.

Local bypassing for the input is needed on the LM2705. Multilayer ceramic capacitors are a good choice for this as well. A 4.7µF capacitor is sufficient for most applications. For additional bypassing, a 100nF ceramic capacitor can be used to shunt high frequency ripple on the input.

LAYOUT CONSIDERATIONS

The input bypass capacitor C_{IN}, as shown in Figure 1, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN} to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the Cout capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R1 and R2, should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network should connect directly to an analog ground plane. The analog ground plane should tie directly to the GND pin. If no analog ground plane is available, the ground connection for the feedback network should tie directly to the GND pin. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.

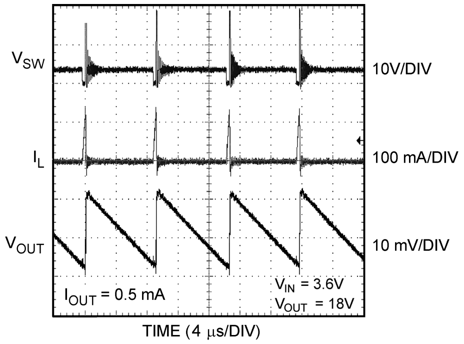


Figure 17. Output Ripple Voltage Copt / Ropt included

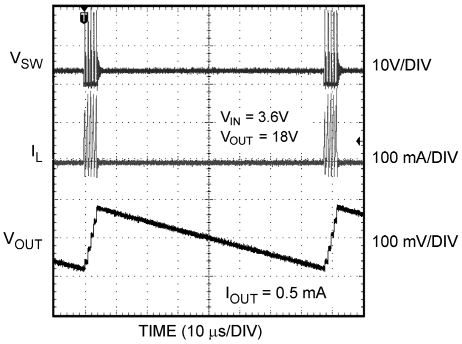
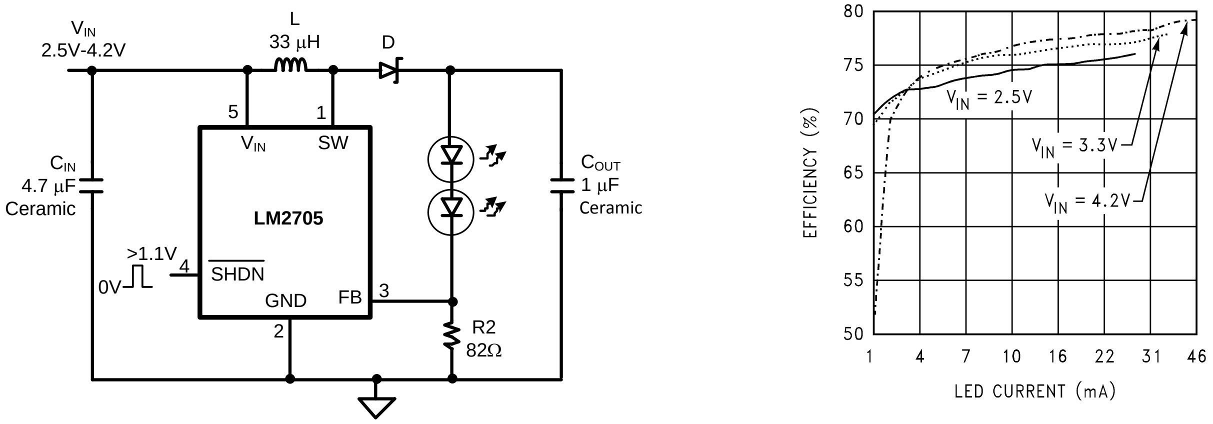


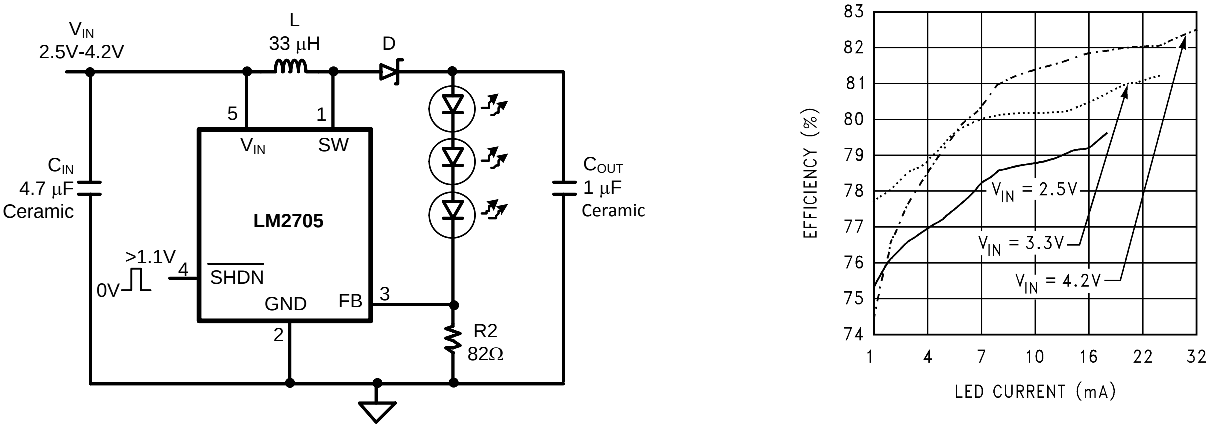
Figure 18. Output Ripple Voltage Copt / Ropt excluded

Figure 19. 2 White LED Application and Efficiency

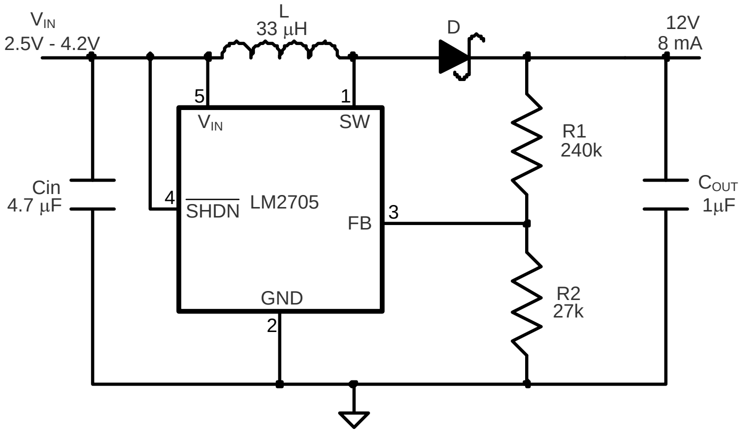


C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-333
D: ON Semiconductor MBRM130LT3

Figure 20. 3 White LED Application and Efficiency

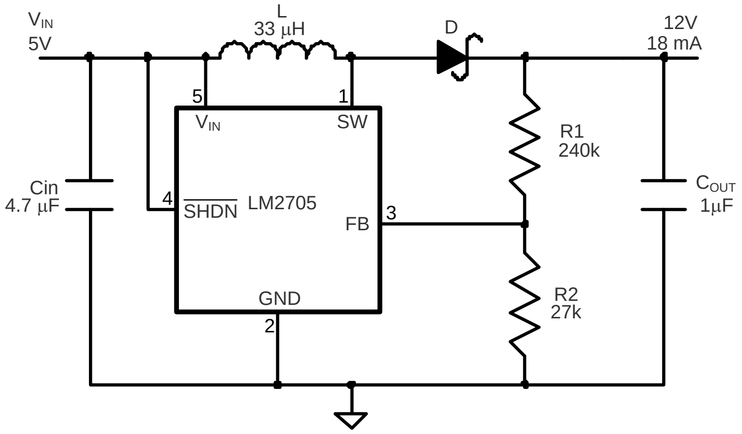


C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-333
D: ON Semiconductor MBRM130LT3



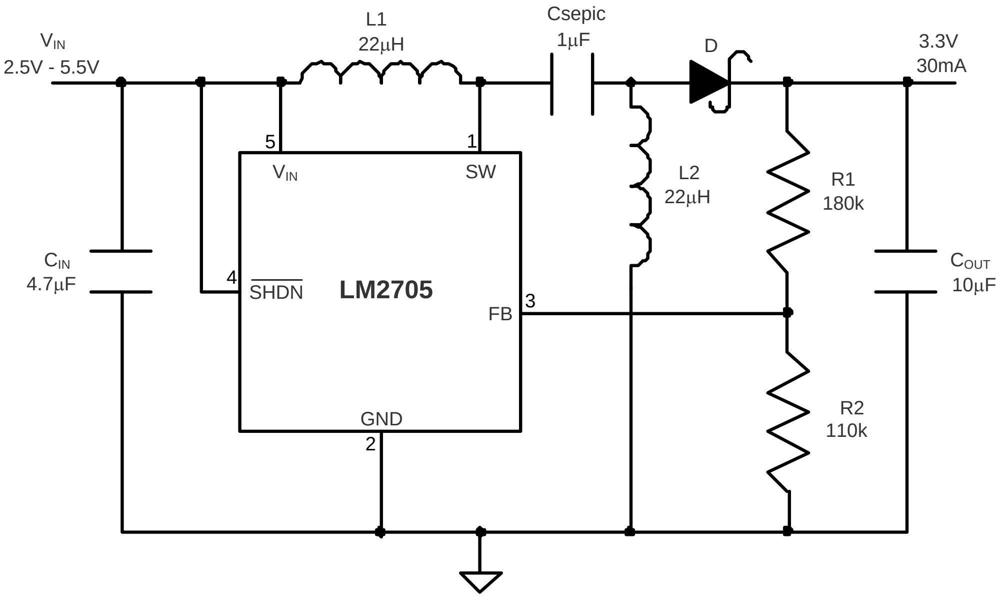
C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-333
D: ON Semiconductor MBRM130LT3

Figure 21. Li-Ion 12V Application



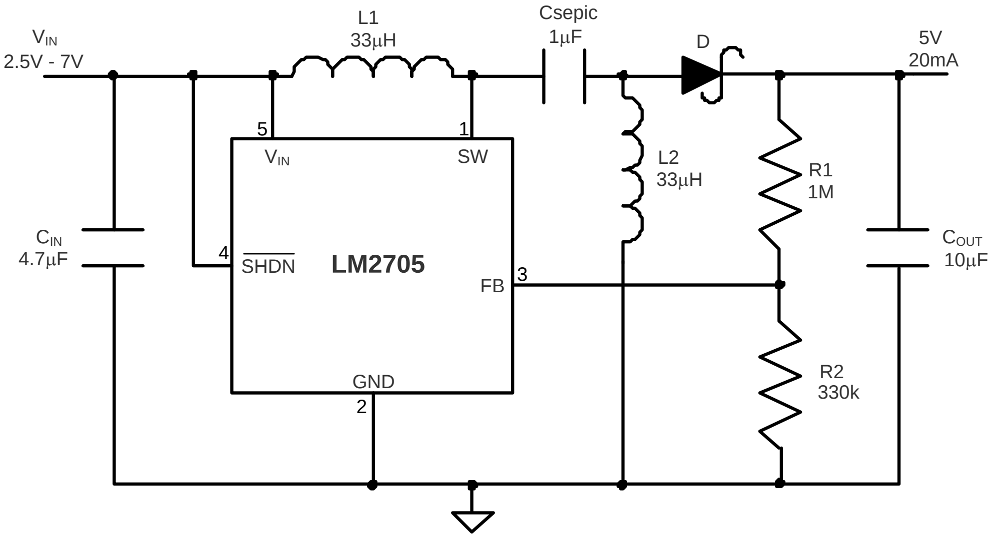
C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-333
D: ON Semiconductor MBRM130LT3

Figure 22. 5V to 12V Application



Csepic: Taiyo Yuden Ceramic
C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L1, L2: Coilcraft DT1608C-223
D: ON Semiconductor MBRM130LT3

Figure 23. 3.3V SEPIC Application



Csepic: Taiyo Yuden Ceramic
C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L1, L2: Coilcraft DT1608C-333
D: ON Semiconductor MBRM130LT3

Figure 24. 5V SEPIC Application

REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2705MF-ADJ	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	S59B	Samples
LM2705MF-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S59B	Samples
LM2705MFX-ADJ	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	S59B	Samples
LM2705MFX-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S59B	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

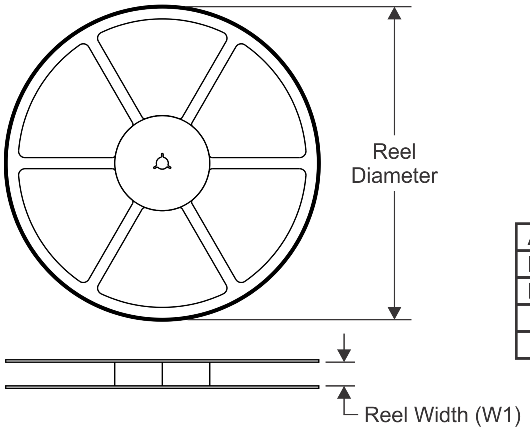
[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

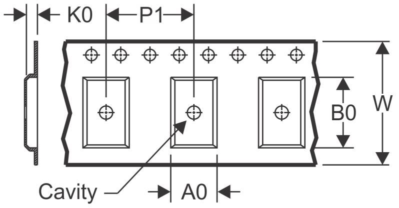
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

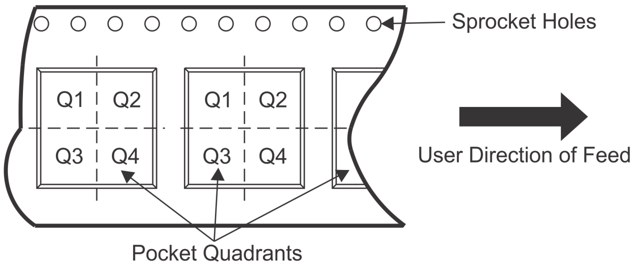


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

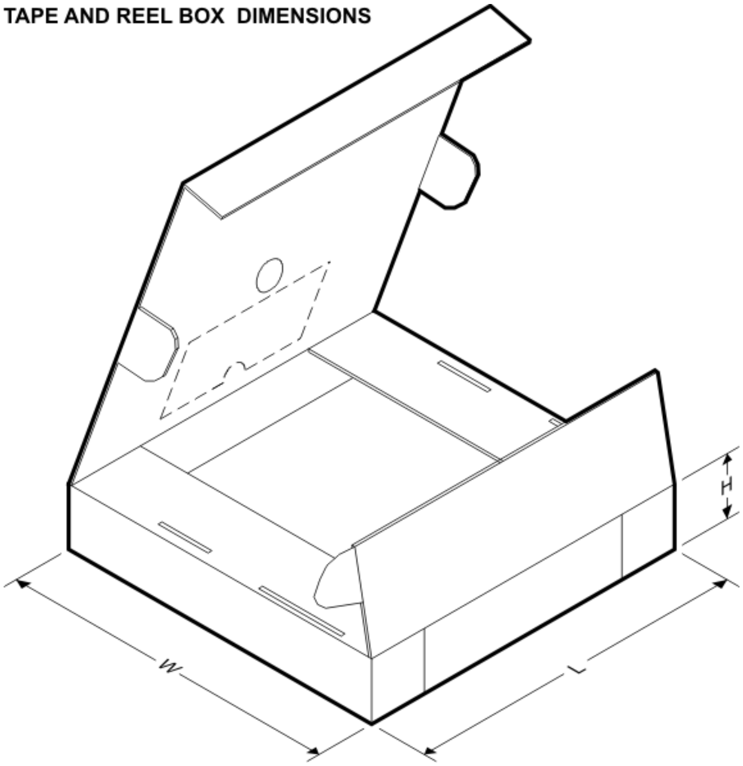
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2705MF-ADJ	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2705MF-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2705MFX-ADJ	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2705MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

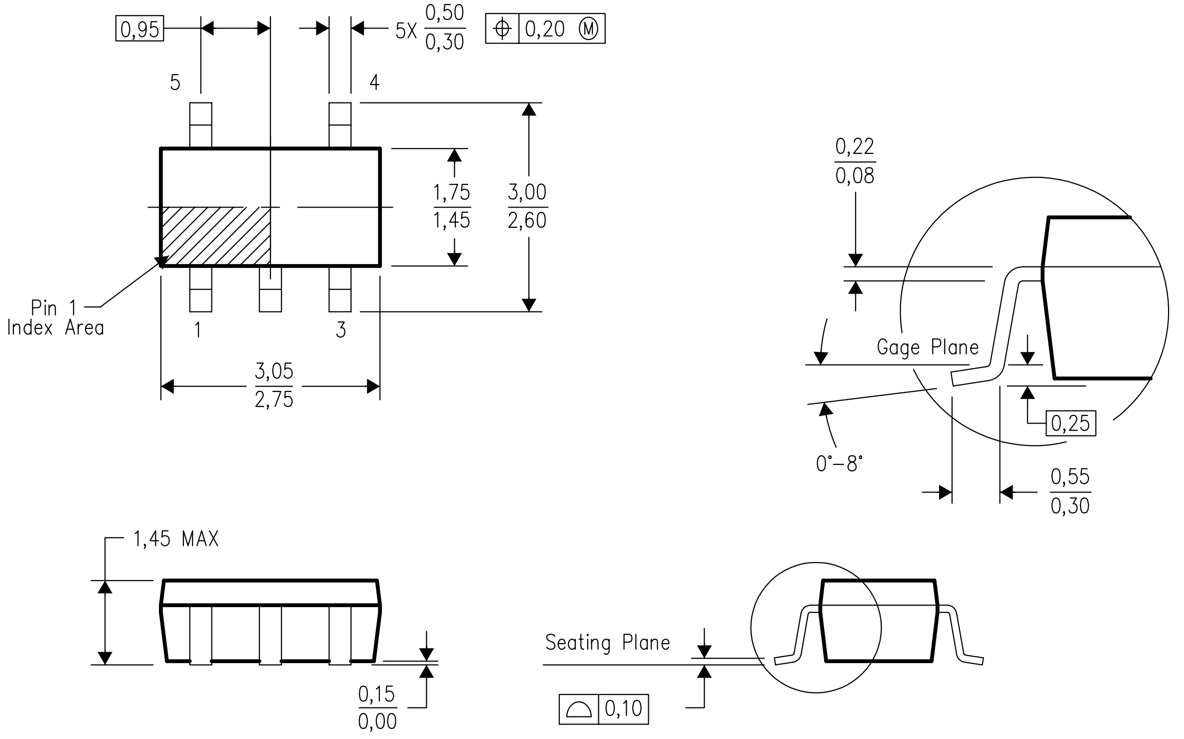
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2705MF-ADJ	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2705MF-ADJ/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2705MFX-ADJ	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2705MFX-ADJ/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

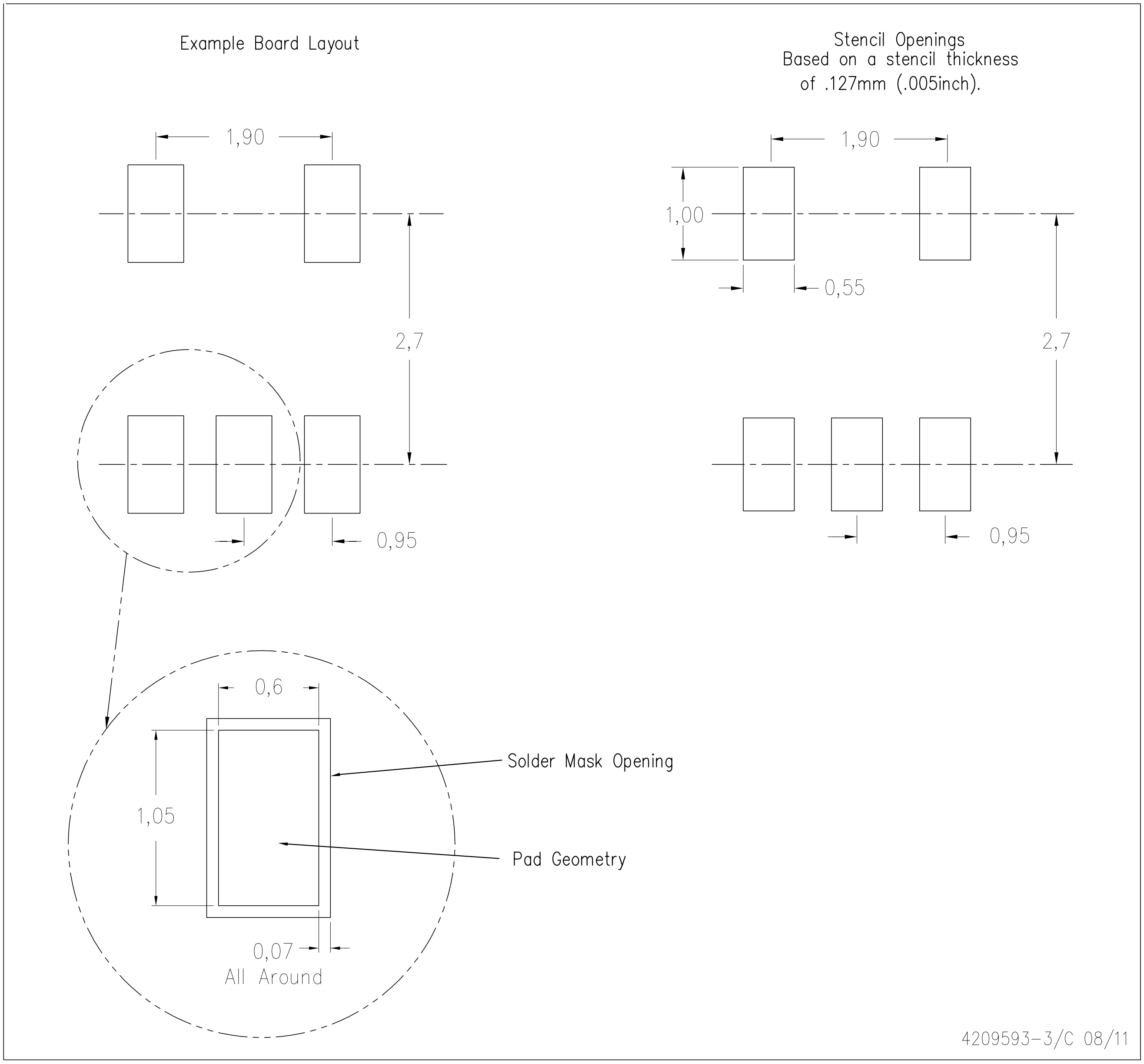
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated