LP3943 RGB/White/Blue 16-LED Fun Light Driver

Check for Samples: LP3943

FEATURES

- **Internal Power-On Reset**
- **Active Low Reset**
- **Internal Precision Oscillator**
- **Variable Dim Rates (from 6.25 ms to 1.6s; 160 Hz–0.625 Hz)**

APPLICATIONS

- **Customized Flashing LED Lights for Cellular Phones**
- **Portable Applications**
- **Digital Cameras**
- **Indicator Lamps**
- **General Purpose I/O Expander**
- **Toys**

KEY SPECIFICATIONS

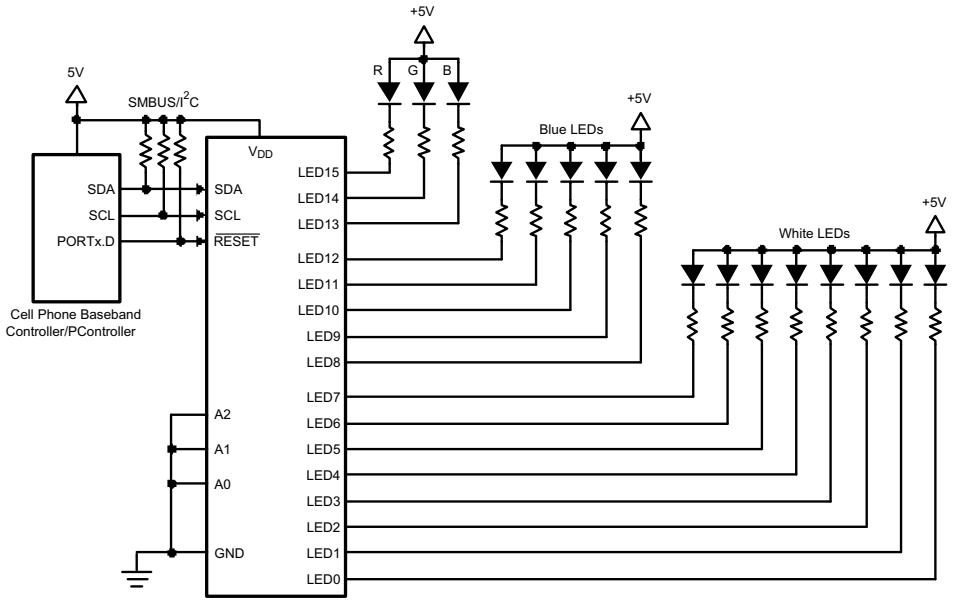
- **16 LED driver (multiple programmable states—on, off, input, and dimming at a specified rate)**
- **16 Open drain outputs capable of driving up to 25 mA per LED**

DESCRIPTION

LP3943 is an integrated device capable of independently driving 16 LEDs. This device also contains an internal precision oscillator that provides all the necessary timing required for driving each LED. Two prescaler registers along with two PWM registers provide a versatile duty cycle control. The LP3943 contains the ability to dim LEDs in SMBUS/I^{2}C applications where it is required to cut down on bus traffic.

Traditionally, to dim LEDs using a serial shift register such as 74LS594/5 would require a large amount of traffic to be on the serial bus. LP3943 instead requires only the setup of the frequency and duty cycle for each output pin. From then on, only a single command from the host is required to turn each individual open drain output ON, OFF, or to cycle a programmed frequency and duty cycle. Maximum output sink current is 25 mA per pin and 200 mA per package. Any ports not used for controlling the LEDs can be used for general purpose input/output expansion.

Typical Application Circuit



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Connection Diagram

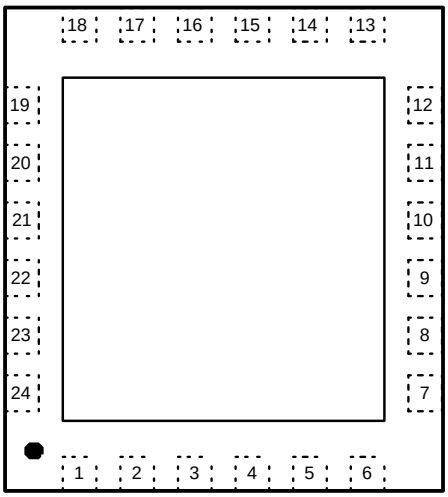


Figure 1. QFN Package – Top View
See Package Number RTW0024C

Table 1. LP3943 Pin Description

Pin #	Name	Description
1	LED0	Output of LED0 Driver
2	LED1	Output of LED1 Driver
3	LED2	Output of LED2 Driver
4	LED3	Output of LED3 Driver
5	LED4	Output of LED4 Driver
6	LED5	Output of LED5 Driver
7	LED6	Output of LED6 Driver
8	LED7	Output of LED7 Driver
9	GND	Ground
10	LED8	Output of LED8 Driver
11	LED9	Output of LED9 Driver
12	LED10	Output of LED10 Driver
13	LED11	Output of LED11 Driver
14	LED12	Output of LED12 Driver
15	LED13	Output of LED13 Driver
16	LED14	Output of LED14 Driver
17	LED15	Output of LED15 Driver
18	$\overline{RST}$	Active Low Reset Input
19	SCL	Clock Line for I^2C Interface
20	SDA	Serial Data Line for I^2C Interface
21	V_{DD}	Power Supply
22	A0	Address Input 0
23	A1	Address Input 1
24	A2	Address Input 2

Architectural Block Diagram

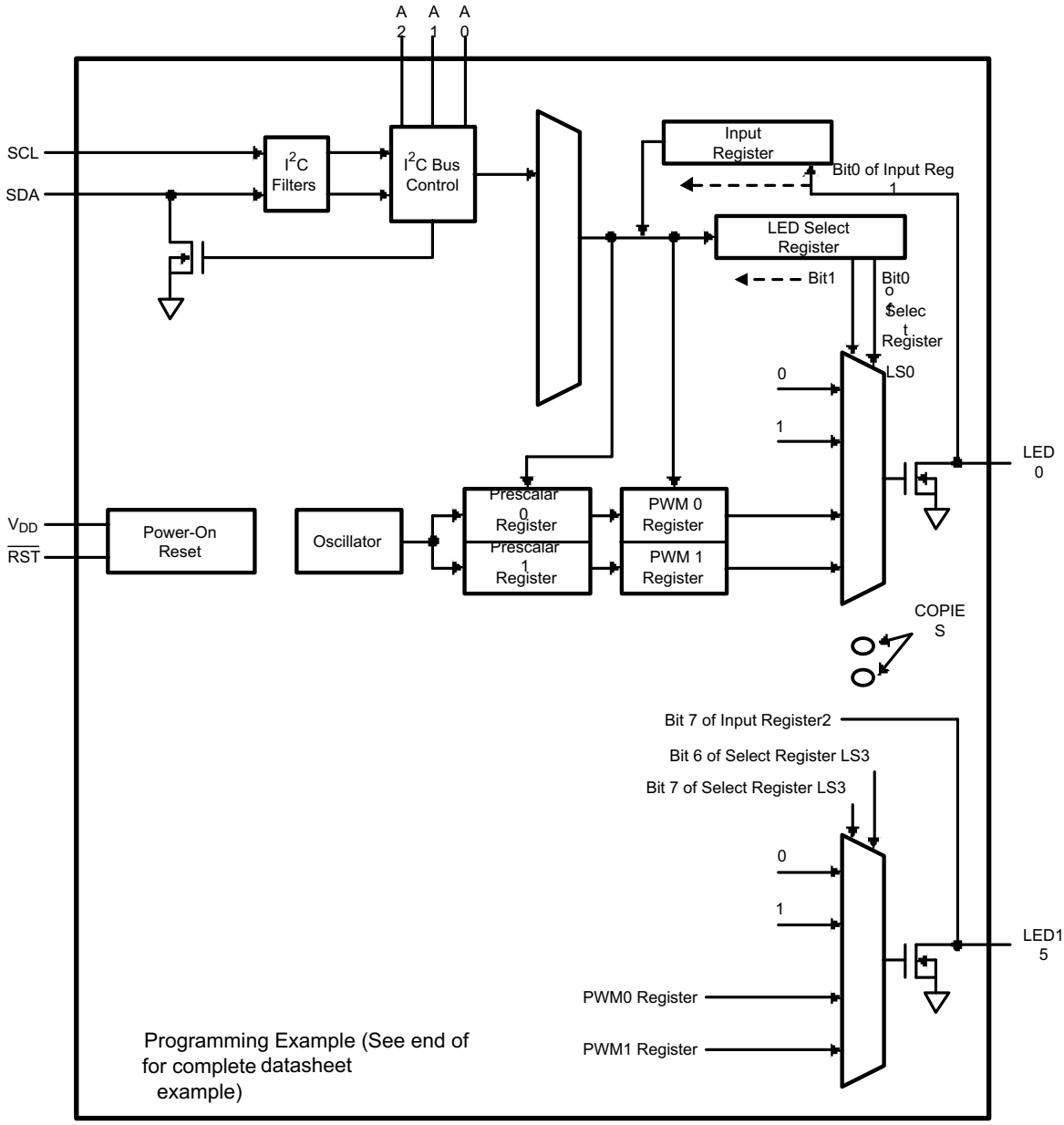


Figure 2. For Explanation of LP3943 Operation, see THEORY OF OPERATION

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

V_{DD}		−0.5V to 6V
A0, A1, A2, SCL, SDA, $\overline{RST}$ (Collectively called digital pins)		6V
Voltage on LED pins		V_{SS}−0.5V to 6V
Junction Temperature		150°C
Storage Temperature		−65°C to 150°C
Power Dissipation(4)		400
ESD(5)	Human Body Model	2 kV
	Machine Model	200V
	Charge Device Model	1 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The part cannot dissipate more than 400mW.
(5) The human-body model is 100 pF discharged through 1.5 kΩ. The machine model is 0Ω in series with 100 pF.

Operating Ratings(1)(2)

V_{DD}		2.3V to 5.5V
Junction Temperature		−40°C to +125°C
Operating Ambient Temperature		−40°C to +85°C
Thermal Resistance (θ_{JA})	LLP24(3)	37°C/W

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) The part cannot dissipate more than 400mW.

Electrical Characteristics

Unless otherwise noted, V_{DD} = 5.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
POWER SUPPLY						
V_{DD}	Supply Voltage		5	**2.3**	**5.5**	V
I_Q	Supply Current	No Load	350		**550**	µA
		Standby	2.0		**5**	
ΔI_Q	Additional Standby Current	V_{DD} = 5.5V, every LED pin at 4.3V			**2**	mA
V_{POR}	Power-On Reset Voltage		1.8		**1.96**	V
t_w	Reset Pulse Width		10			ns
LED						
V_{IL}	LOW Level Input Voltage			**−0.5**	**0.8**	V
V_{IH}	HIGH Level Input Voltage			**2.0**	**5.5**	V

(1) Limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Electrical Characteristics (continued)

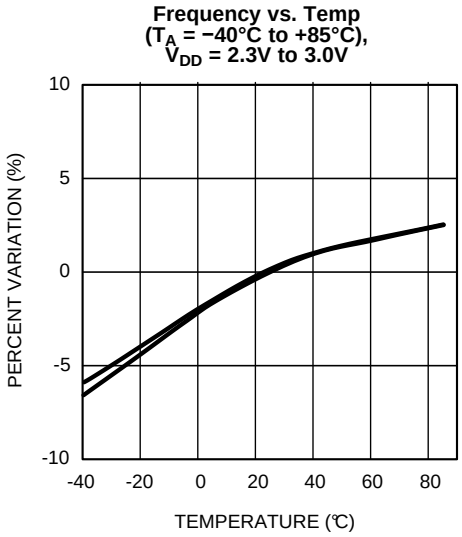
Unless otherwise noted, V_{DD} = 5.5V. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.(1)

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{OL}	Low Level Output Current(2)	V_{OL} = 0.4V, V_{DD} = 2.3V		**9**		mA
		V_{OL} = 0.4V, V_{DD} = 3.0V		**12**		
		V_{OL} = 0.4V, V_{DD} = 5.0V		**15**		
		V_{OL} = 0.7V, V_{DD} = 2.3V		**15**		
		V_{OL} = 0.7V, V_{DD} = 3.0V		**20**		
		V_{OL} = 0.7V, V_{DD} = 5.0V		**25**		
I_{LEAK}	Input Leakage Current	V_{DD} = 3.6, V_{IN} = 0V or V_{DD}		**−1**	**1**	µA
$C_{I/O}$	Input/Output Capacitance	See(3)	2.6		**5**	pF
ALL DIGITAL PINS (EXCEPT SCL AND SDA PINS)						
V_{IL}	LOW Level Input Voltage			**−0.5**	**0.8**	V
V_{IH}	HIGH Level Input Voltage			**2.0**	**5.5**	V
I_{LEAK}	Input Leakage Current			**−1**	**1**	µA
C_{IN}	Input Capacitance	V_{IN} = 0V(3)	2.3		**5**	pF
I^2C INTERFACE (SCL AND SDA PINS)						
V_{IL}	LOW Level Input Voltage			**-0.5**	**$0.3V_{DD}$**	V
V_{IH}	HIGH Level Input Voltage			**$0.7V_{DD}$**	**5.5**	V
V_{OL}	LOW Level Output Voltage			**0**	**$0.2V_{DD}$**	V
I_{OL}	LOW Level Output Current	V_{OL} = 0.4V	6.5	**3**		mA
F_{CLK}	Clock Frequency	See(3)			**400**	kHz
t_{HOLD}	Hold Time Repeated START Condition	See(3)		**0.6**		µs
t_{CLK-LP}	CLK Low Period	See(3)		**1.3**		µs
t_{CLK-HP}	CLK High Period	See(3)		**0.6**		µs
t_{SU}	Set-Up Time Repeated START Condition	See(3)		**0.6**		µs
$t_{DATA-HOLD}$	Data Hold Time	See(3)		**300**		ns
$t_{DATA-SU}$	Data Set-Up Time	See(3)		**100**		ns
t_{SU}	Set-Up Time for STOP Condition	See(3)		**0.6**		µs
t_{TRANS}	Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA & CLK Signals	See(3)	50			ns

(2) Each LED pin should not exceed 25 mA and each octal (LED0–LED7; LED8–LED15) should not exceed 100 mA. The package should not exceed a total of 200 mA.
(3) Guaranteed by design.

Typical Performance Characteristics

Figure 3.



APPLICATION NOTES

THEORY OF OPERATION

The LP3943 takes incoming data from the baseband controller and feeds them into several registers that control the frequency and the duty cycle of the LEDs. Two prescaler registers and two PWM registers provide two individual rates to dim or blink the LEDs (for more information on these registers, refer to Table 2). Each LED can be programmed in one of four states—on, off, DIM0 rate or DIM1 rate. Two read-only registers provide status on all 16 LEDs. The LP3943 can be used to drive RGB LEDs and/or single-color LEDs to create a colorful, entertaining, and informative setting. Alternatively, it can also drive RGB LED as a flashlight. This is particularly suitable for accessory functions in cellular phones and toys. Any LED pins not used to drive LED can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The LP3943 is equipped with Power-On Reset that holds the chip in a reset state until V_{DD} reaches V_{POR} during power up. Once V_{POR} is achieved, the LP3943 comes out of reset and initializes itself to the default state.

To bring the LP3943 into reset, hold the $\overline{RST}$ pin LOW for a period of TW. This will put the chip into its default state. The LP3943 can only be programmed after $\overline{RST}$ signal is HIGH again.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

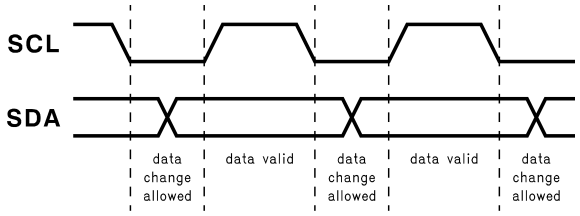


Figure 4. I²C Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

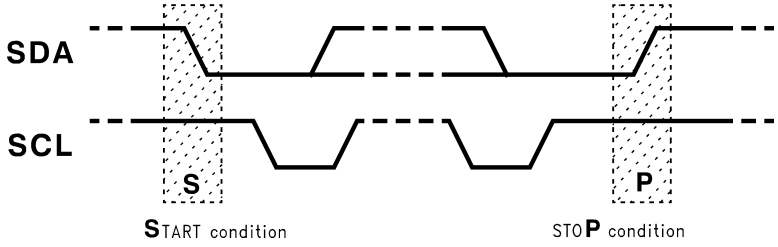


Figure 5. I²C START and STOP Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, a chip address is sent by the I^2C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3943 hardwires bits 7 to 4 and leaves bits 3 to 1 selectable, as shown in Figure 6. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The LP3943 supports only a WRITE during chip addressing. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

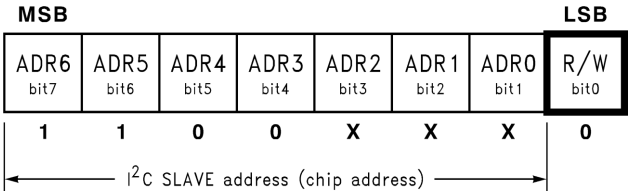
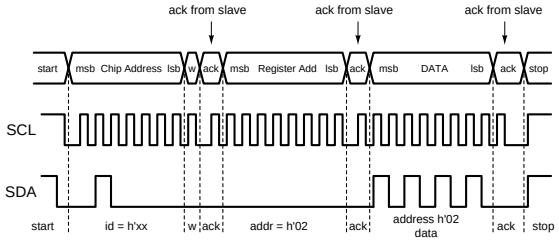


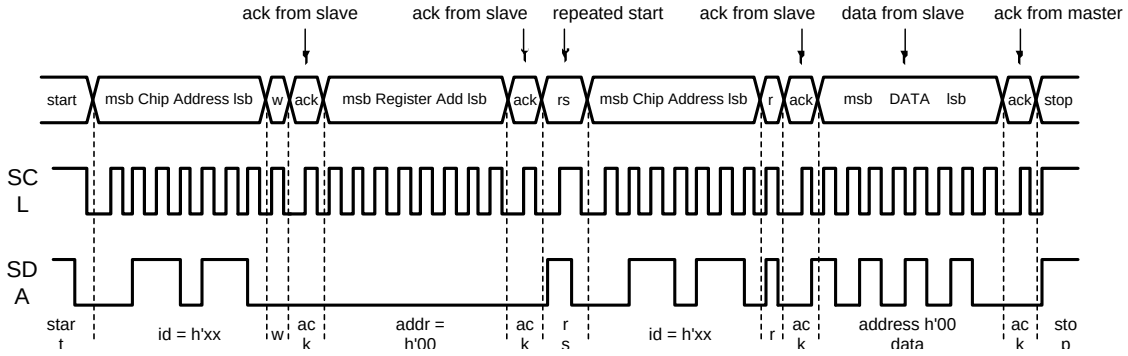
Figure 6. Chip Address Byte



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled LOW by either master or slave)
rs = repeated start
xx = 60 to 67

Figure 7. LP3943 Register Write

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in Figure 8.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled LOW by either master or slave)
rs = repeated start
xx = 60 to 67

Figure 8. LP3943 Register Read

AUTO INCREMENT

Auto increment is a special feature supported by the LP3943 to eliminate repeated chip and register addressing when data are to be written to or read from registers in sequential order. The auto increment bit is inside the register address byte, as shown in Figure 9. Auto increment is enabled when this bit is programmed to “1” and disabled when it is programmed to “0”.

Bits 5, 6 and 7 in the register address byte should always be zero.

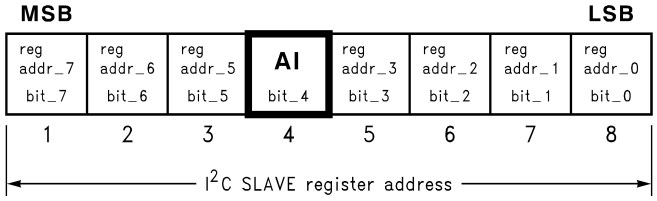


Figure 9. Register Address Byte

In the READ mode, when auto increment is enabled, I^2C master could receive any number of bytes from LP3943 without selecting chip address and register address again. Every time the I^2C master reads a register, the LP3943 will increment the register address and the next data register will be read. When I^2C master reaches the last register (09H), the register address will roll over to 00H.

In the WRITE mode, when auto increment is enabled, the LP3943 will increment the register address every time I^2C master writes to register. When the last register (09H register) is reached, the register address will roll over to 02H, not 00H, because the first two registers in LP3943 are read-only registers. It is possible to write to the first two registers independently, and the LP3943 will acknowledge, but the data will be ignored.

If auto increment is disabled, and the I^2C master does not change register address, it will continue to write data into the same register.

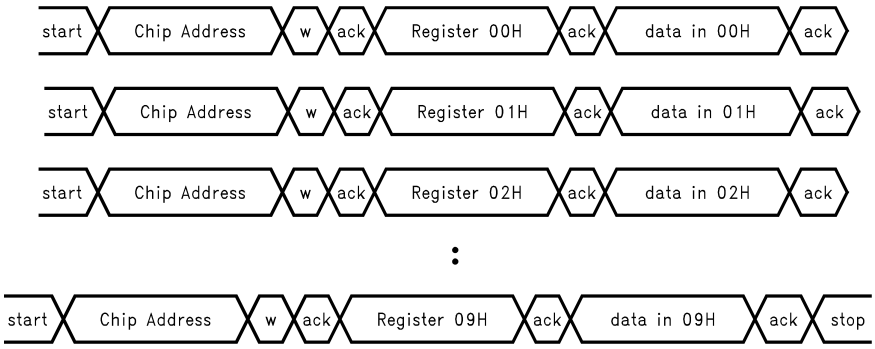


Figure 10. Programming with Auto Increment Disabled (in WRITE Mode)

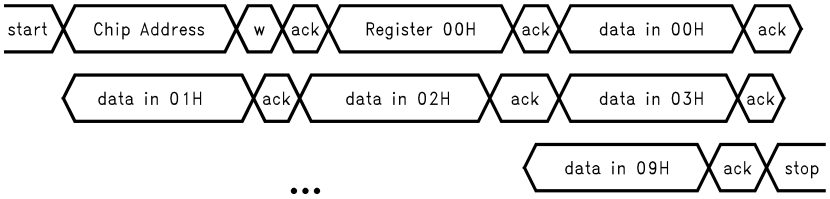


Figure 11. Programming with Auto Increment Enabled (in WRITE Mode)

Table 2. LP3943 REGISTER TABLE

Address (Hex)	Register Name	Read/Write	Register Function
0x00	Input 1	Read Only	LED0–7 Input Register
0x01	Input 2	Read Only	LED8–15 Input Register
0x02	PSC0	R/W	Frequency Prescaler 0
0x03	PWM0	R/W	PWM Register 0
0x04	PSC1	R/W	Frequency Prescaler 1
0x05	PWM1	R/W	PWM Register 1
0x06	LS0	R/W	LED0–3 Selector
0x07	LS1	R/W	LED4–7 Selector
0x08	LS2	R/W	LED8–11 Selector
0x09	LS3	R/W	LED12–15 Selector

BINARY FORMAT FOR INPUT REGISTERS (READ ONLY)—ADDRESS 0x00 and 0x01

Table 3. Address 0x00

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

Table 4. Address 0x01

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8

BINARY FORMAT FOR FREQUENCY PRESCALER AND PWM REGISTERS — ADDRESS 0x02 to 0x05

Table 5. Address 0x02 (PSC0)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

Table 6. Address 0x03 (PWM0)

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

Table 7. Address 0x04 (PSC1)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

Table 8. Address 0x05 (PWM1)

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

BINARY FORMAT FOR SELECTOR REGISTERS — ADDRESS 0x06 to 0x09

Table 9. Address 0x06 (LS0)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED3		LED2		LED1		LED0	

Table 10. Address 0x07 (LS1)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED7		LED6		LED5		LED4	

Table 11. Address 0x08 (LS2)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED11		LED10		LED9		LED8	

Table 12. Address 0x09 (LS3)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED15		LED14		LED13		LED12	

Table 13. LED States With Respect To Values in "B1" and "B0"

B1	B0	Function
0	0	Output Hi-Z (LED off)
0	1	Output LOW (LED on)
1	0	Output dims (DIM0 rate)
1	1	Output dims (DIM1 rate)

Programming Example:

Dim LEDs 0 to 7 at 1 Hz at 25% duty cycle

Dim LEDs 8 to 12 at 5 Hz at 50% duty cycle

Set LEDs 13, 14 and 15 off

Step 1: Set PSC0 to achieve DIM0 of 1s

Step 2: Set PWM0 duty cycle to 25%

Step 3: Set PSC1 to achieve DIM1 of 0.2s

Step 4: Set PWM1 duty cycle to 50%

Step 5: Set LEDs 13, 14 and 15 off by loading the data into LS3 register

Step 6: Set LEDs 0 to 7 to point to DIM0

Step 7: Set LEDs 8 to 12 to point to DIM1

Step	Description	Register Name	Set to (Hex)
1	Set DIM0 = 1s 1 = (PSC0 + 1)/160 PSC0 = 159	PSC0	0x09F
2	Set duty cycle to 25% Duty Cycle = PWM0/256 PWM0 = 64	PWM0	0x40
3	Set DIM1 = 0.2s 0.2 = (PSC1 + 1)/160 PSC1 = 31	PSC1	0x1F
4	Set duty cycle to 50% Duty Cycle = PWM1/256 PWM1 = 128	PWM1	0x80
5	LEDs 13, 14 and 15 off Output = HIGH	LS3	0x03
6	LEDs 0 to 7 Output = DIM0	LS0, LS1	LS0 = 0xAA LS1 = 0xAA
7	LEDs 8 to 12 Output = DIM1	LS2, LS3	LS2 = 0xFF LS3 = 0x03

REDUCING I_Q WHEN LEDS ARE OFF

In many applications, the LEDs and the LP3943 share the same V_{DD}, as shown in Typical Application Circuit. When the LEDs are off, the LED pins are at a lower potential than V_{DD}, causing extra supply current (ΔI_Q). To minimize this current, consider keeping the LED pins at a voltage equal to or greater than V_{DD}.

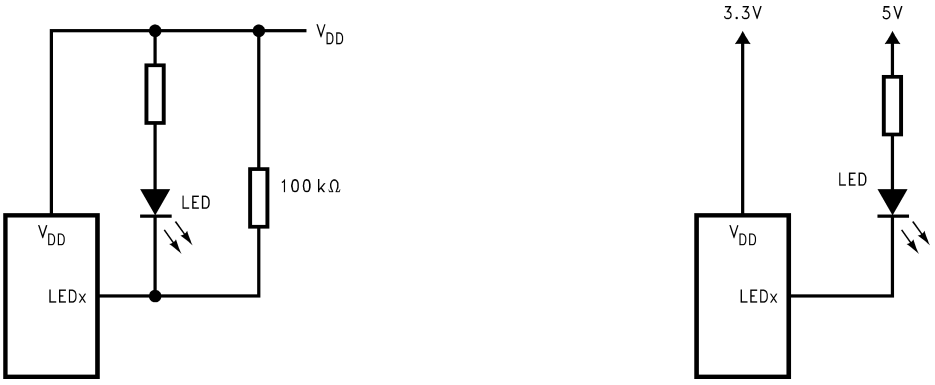


Figure 12. Methods to Reduce I_Q When LEDs Are Off

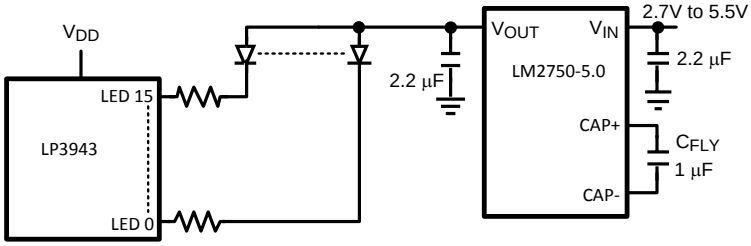


Figure 13. LP3943 With 5V Booster

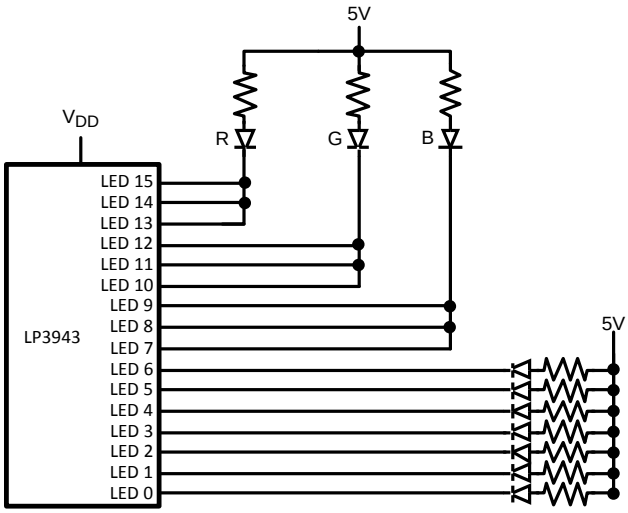


Figure 14. LP3943 Driving RGB LED As A Flash

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3943ISQ	ACTIVE	WQFN	RTW	24	1000	TBD	Call TI	Call TI	-40 to 85	3943SQ	Samples
LP3943ISQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	3943SQ	Samples
LP3943ISQX	ACTIVE	WQFN	RTW	24	4500	TBD	Call TI	Call TI	-40 to 85	3943SQ	Samples
LP3943ISQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	3943SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

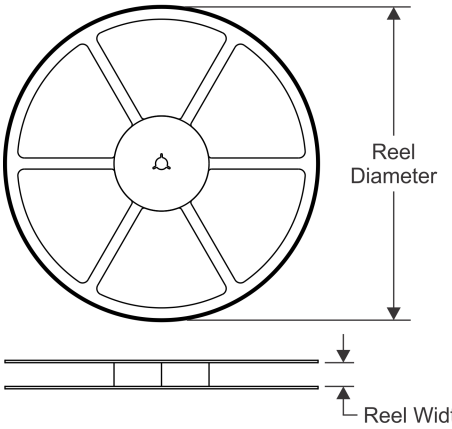
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

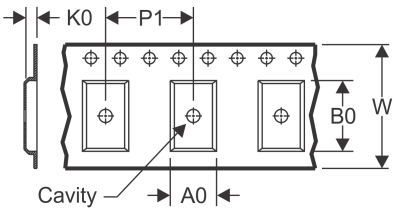
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

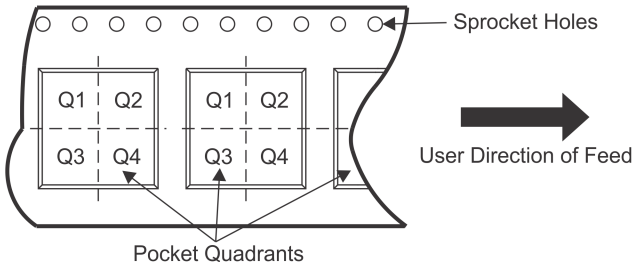


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

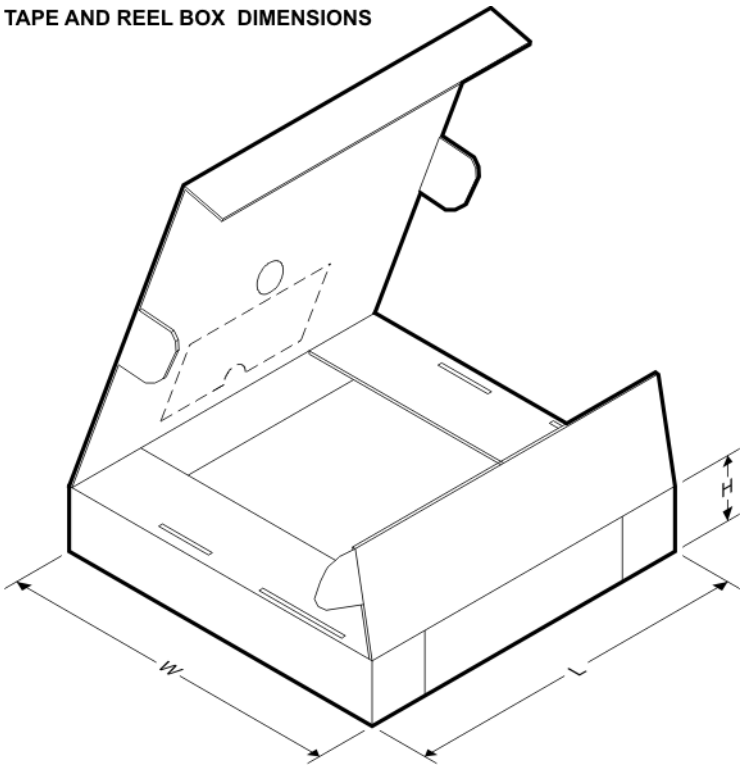
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3943ISQ	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3943ISQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3943ISQX	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3943ISQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

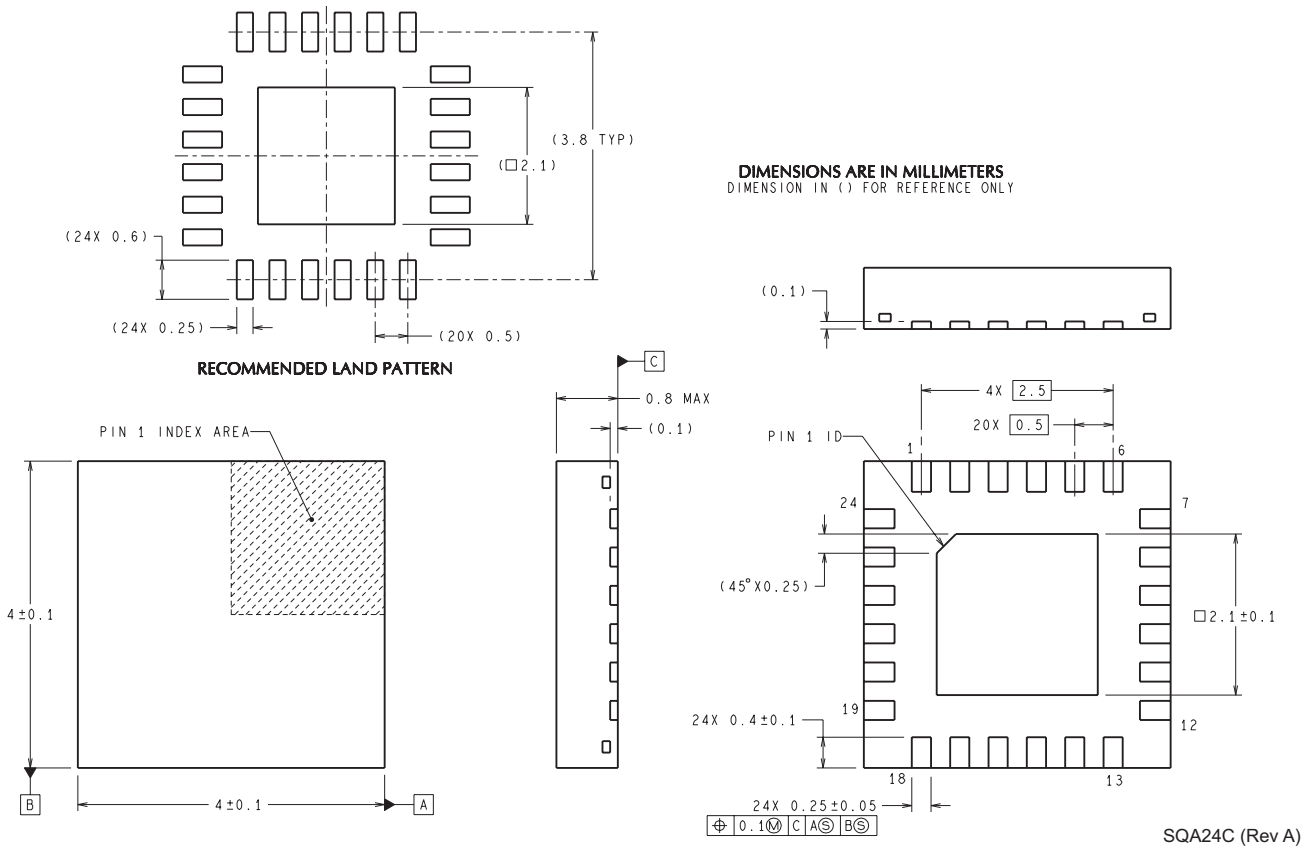
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3943ISQ	WQFN	RTW	24	1000	203.0	190.0	41.0
LP3943ISQ/NOPB	WQFN	RTW	24	1000	203.0	190.0	41.0
LP3943ISQX	WQFN	RTW	24	4500	367.0	367.0	35.0
LP3943ISQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

RTW0024C


(3.8 TYP)
(□2.1)
(24X 0.6)
(24X 0.25)
(20X 0.5)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSION IN () FOR REFERENCE ONLY
(0.1)
4X 2.5
20X 0.5
PIN 1 ID
1
6
7
12
13
18
19
24
(45°X0.25)
□2.1±0.1
24X 0.4±0.1
24X 0.25±0.05
0.1 M C A S B S
C
0.8 MAX
(0.1)
PIN 1 INDEX AREA
4±0.1
4±0.1
B
A
SQA24C (Rev A)

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