LP3962EP/LP3965EP 1.5A Fast Ultra Low Dropout Linear Regulators

Check for Samples: LP3962EP, LP3965EP

FEATURES

- **Ultra Low Dropout Voltage**
- **Low Ground Pin Current**
- **Load Regulation of 0.04%**
- **15µA Quiescent Current in Shutdown Mode**
- **Specified Output Current of 1.5A DC**
- **Available in SOT-223, DDPAK and TO-220 Packages**
- **Output Voltage Accuracy ± 1.5%**
- **$\overline{\text{Error}}$ Flag Indicates Output Status (LP3962EP)**
- **Sense Option Improves Better Load Regulation (LP3965EP)**
- **Extremely Low Output Capacitor Requirements**
- **Overtemperature/Overcurrent Protection**

APPLICATIONS

- **Microprocessor Power Supplies**
- **GTL, GTL+, BTL, and SSTL Bus Terminators**
- **Power Supplies for DSPs**
- **SCSI Terminator**
- **Post Regulators**
- **High Efficiency Linear Regulators**
- **Selected Military Applications**
- **Selected Avionics Applications**

DESCRIPTION

The LP3962EP/LP3965EP series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very fast to step changes in load which makes them suitable for low voltage microprocessor applications. The LP3962EP/LP3965EP are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3962EP/LP3965EP to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 38mV at 150mA load current and 380mV at 1.5A load current.

Ground Pin Current: Typically 5mA at 1.5A load current.

Shutdown Mode: Typically 15µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3962EP).

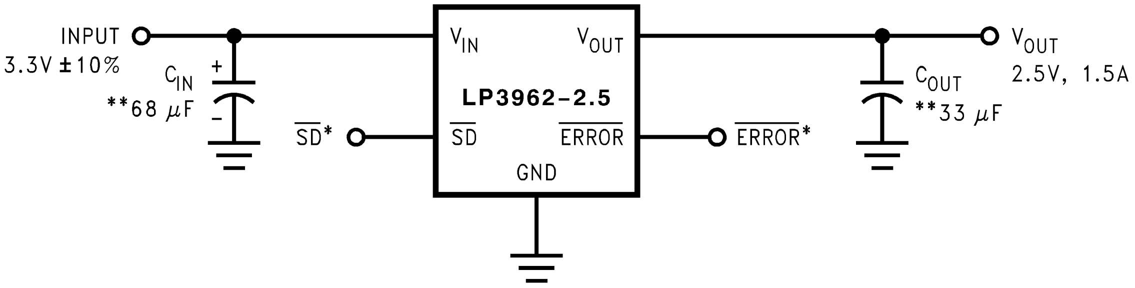
SENSE: Sense pin improves regulation at remote loads. (For LP3965EP)

Precision Output Voltage: Multiple output voltage options are available ranging from 1.2V to 5.0V and adjustable (LP3965EP), with a specified accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

ENHANCED PLASTIC

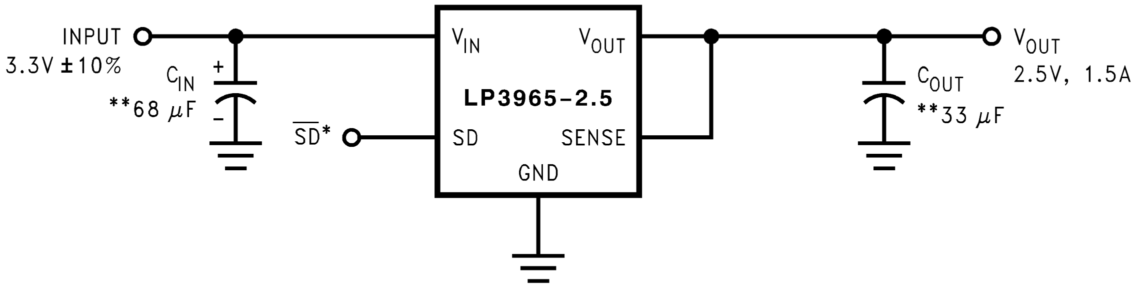
- Extended Temperature Performance of −40°C to +125°C
- Baseline Control - Single Fab & Assembly Site
- Process Change Notification (PCN)
- Qualification & Reliability Data
- Solder (PbSn) Lead Finish is standard
- Enhanced Diminishing Manufacturing Sources (DMS) Support

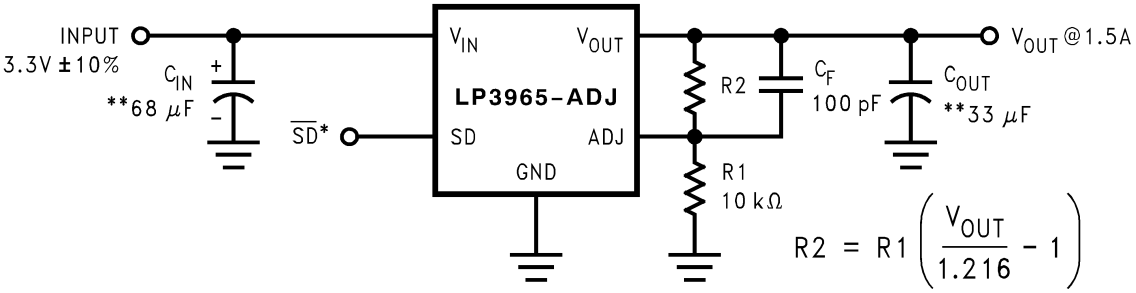
TYPICAL APPLICATION CIRCUITS



*$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints.

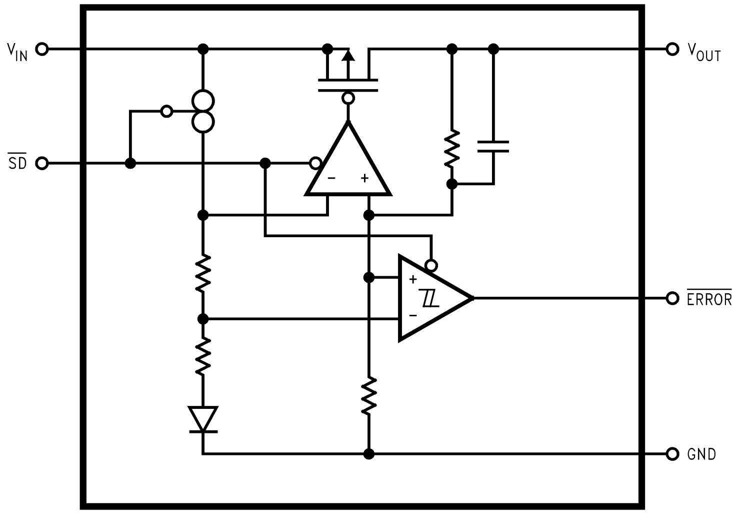




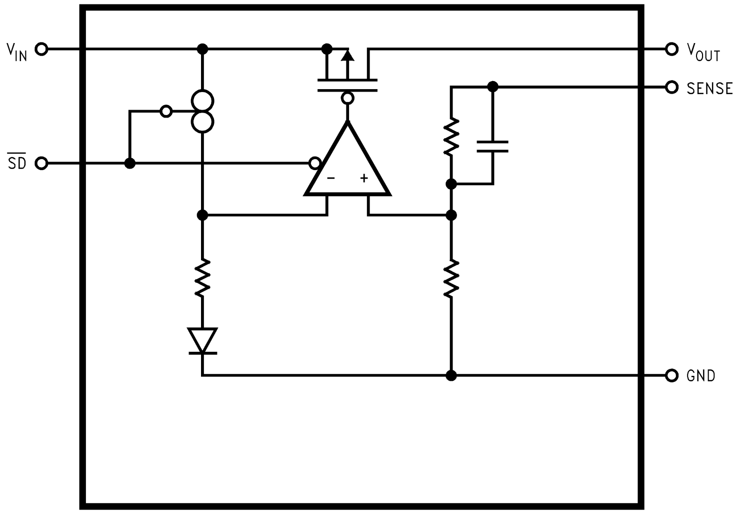
*$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints.

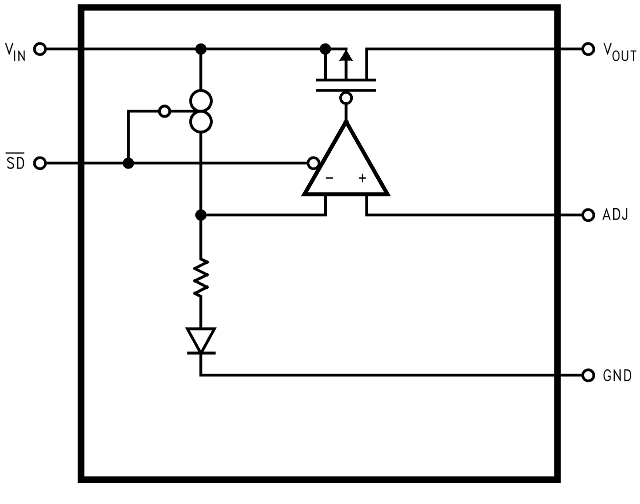
BLOCK DIAGRAM LP3962EP



BLOCK DIAGRAM LP3965EP



BLOCK DIAGRAM LP3965-ADJEP



CONNECTION DIAGRAM

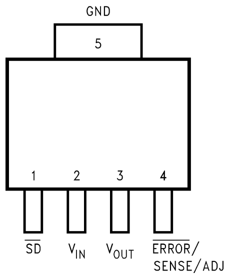


Figure 1. SOT-223 Package
(Top View)
See Package Number NDC

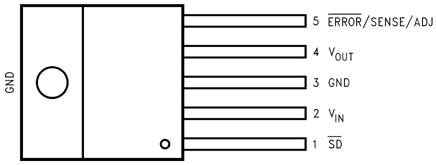


Figure 2. TO-220 Package
(Top View)
Bent, Staggered Leads
See Package Number NDH

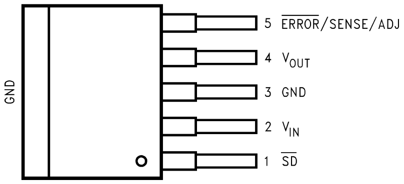


Figure 3. DDPAK Package
(Top View)
See Package Number KTT

PIN DESCRIPTION FOR SOT-223 PACKAGE

Pin #	LP3962EP		LP3965EP	
	Name	**Function**	**Name**	**Function**
1	$\overline{\text{SD}}$	Shutdown	$\overline{\text{SD}}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
4	$\overline{\text{ERROR}}$	$\overline{\text{ERROR}}$ Flag	SENSE/ADJ	Remote Sense Pin or Output Adjust Pin
5	GND	Ground	GND	Ground

PIN DESCRIPTION FOR TO-220 AND DDPAK PACKAGES

Pin #	LP3962EP		LP3965EP	
	Name	**Function**	**Name**	**Function**
1	$\overline{\text{SD}}$	Shutdown	$\overline{\text{SD}}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	$\overline{\text{ERROR}}$	$\overline{\text{ERROR}}$ Flag	SENSE/ADJ	Remote Sense Pin or Output Adjust Pin

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range	−65°C to +150°C
Lead Temperature(Soldering, 5 sec.)	260°C
ESD Rating (3)	2 kV
Power Dissipation (4)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +7.5V
Shutdown Input Voltage (Survival)	−0.3V to V_{IN}+0.3V
Output Voltage (Survival), (5), (6)	−0.3V to +7.5V
I_{OUT} (Survival)	Short Circuit Protected
Maximum Voltage for $\overline{\text{ERROR}}$ Pin	V_{IN}+0.3V
Maximum Voltage for SENSE Pin	V_{OUT}+0.3V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see Electrical Charateristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

(4) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at θ_{jA} = 50°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the DDPAK surface-mount package must be derated at θ_{jA} = 60°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient. The devices in SOT223 package must be derated at θ_{jA} = 90°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient.

(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP396X output must be diode-clamped to ground.

(6) The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

OPERATING RATINGS

Input Supply Voltage (Operating), (1)	2.5V to 7.0V
Shutdown Input Voltage (Operating)	−0.3V to V_{IN}+0.3V
Maximum Operating Current (DC)	1.5A
Operating Junction Temp. Range	−40°C to +125°C

(1) The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5V, whichever is greater.

ELECTRICAL CHARACTERISTICS LP3962ES-2.5EP/LP3965ES-ADJEP

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} = 33µF, $V_{SD} = V_{IN}$-0.3V. (1)

Symbol	Parameter	Conditions	Typ(2)	LP3962EP/5EP(3)		Units
				Min	Max	
V_O	Output Voltage Tolerance(4)	10 mA ≤ I_L ≤ 1.5A V_{OUT} +1 ≤ V_{IN}≤ 7.0V	0	-1.5 **-3.0**	+1.5 **+3.0**	%
V_{ADJ}	Adjust Pin Voltage (ADJ version)	10 mA ≤ I_L ≤ 1.5A V_{OUT} +1.5V ≤ V_{IN}≤ 7.0V	1.216	1.198 **1.180**	1.234 **1.253**	V
ΔV_{OL}	Output Voltage Line Regulation(4)	V_{OUT}+1V<V_{IN}<7.0V	0.02 **0.06**			%
$\Delta V_O / \Delta I_{OUT}$	Output Voltage Load Regulation(4)	10 mA < I_L < 1.5 A	0.04 **0.09**			%
V_{IN} - V_{OUT}	Dropout Voltage(5)	I_L = 150 mA	38		45 **55**	mV
		I_L = 1.5 A	380		450 **550**	
I_{GND}	Ground Pin Current In Normal Operation Mode	I_L = 150 mA	4		9 **10**	mA
		I_L = 1.5 A	5		14 **15**	
I_{GND}	Ground Pin Current In Shutdown Mode(6)	V_{SD} ≤ 0.2V	15		25 **75**	µA
$I_{O(PK)}$	Peak Output Current	(7)	2.5	2.0 **1.7**		A
SHORT CIRCUIT PROTECTION						
I_{SC}	Short Circuit Current		4.5			A
OVER TEMPERATURE PROTECTION						
Tsh(t)	Shutdown Threshold		165			°C
Tsh(h)	Thermal Shutdown Hysteresis		10			°C
SHUTDOWN INPUT						
V_{SDT}	Shutdown Threshold	Output = High	V_{IN}	**V_{IN}–0.3**		V
		Output = Low	0		**0.2**	
T_{dOFF}	Turn-off delay	I_L = 1.5 A	20			µs
T_{dON}	Turn-on delay	I_L = 1.5 A	25			µs
I_{SD}	$\overline{SD}$ Input Current	$V_{SD} = V_{IN}$	1			nA

(1) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."

(2) Typical numbers are at 25°C and represent the most likely parametric norm.

(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

(4) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

(5) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.

(6) This specification has been tested for −40°C ≤ T_J ≤ 85°C since the temperature rise of the device is negligible under shutdown conditions.

(7) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at θ_{jA} = 50°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the DDPAK surface-mount package must be derated at θ_{jA} = 60°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient. The devices in SOT223 package must be derated at θ_{jA} = 90°C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient.

ELECTRICAL CHARACTERISTICS LP3962ES-2.5EP/LP3965ES-ADJEP (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1V$, I_L = 10 mA, C_{OUT} = 33µF, $V_{SD} = V_{IN}$-0.3V. (1)

Symbol	Parameter	Conditions	Typ (2)	LP3962EP/5EP (3)		Units
				Min	Max	
ERROR FLAG COMPARATOR						
V_T	Threshold	(8)	10	**5**	**16**	%
V_{TH}	Threshold Hysteresis	(8)	5	**2**	**8**	%
$V_{EF(Sat)}$	$\overline{\text{Error}}$ Flag Saturation	I_{sink} = 100µA	0.02		**0.1**	V
Td	Flag Reset Delay		1			µs
I_{lk}	$\overline{\text{Error}}$ Flag Pin Leakage Current		1			nA
I_{max}	$\overline{\text{Error}}$ Flag Pin Sink Current	V_{Error} = **0.5V** (over temp.)	1			mA
AC PARAMETERS						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1.5V C_{OUT} = 100uF V_{OUT} = 3.3V	60			dB
		$V_{IN} = V_{OUT}$ + 0.3V C_{OUT} = 100uF V_{OUT} = 3.3V	40			
$\rho_{n(l/f}$	Output Noise Density	f = 120Hz	0.8			µV
e_n	Output Noise Voltage (rms)	BW = 10Hz – 100kHz	150			µV (rms)
		BW = 300Hz – 300kHz	100			

(8) $\overline{\text{Error}}$ Flag threshold and hysteresis are specified as percentage of regulated output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 2.5V$, $C_{OUT} = 33\mu F$, $I_{OUT} = 10mA$, $C_{IN} = 68\mu F$, $V_{SD} = V_{IN}$, and $T_A = 25°C$.

Drop-Out Voltage vs Temperature for Different Load Currents

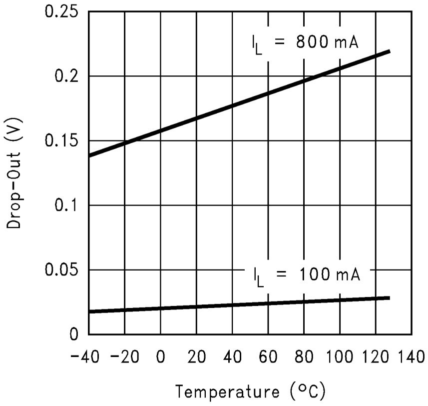


Figure 4.

Drop-Out Voltage vs Temperature for Different Output Voltages (I_{OUT} = 800mA)

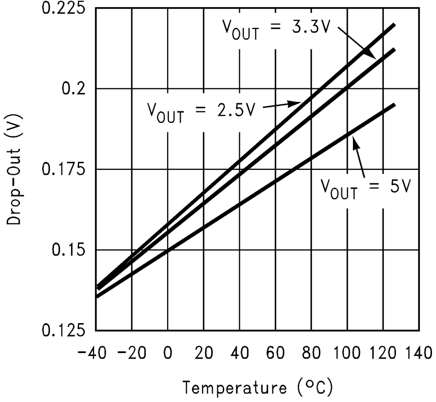


Figure 5.

Ground Pin Current vs Input Voltage (V_{SD}=V_{IN})

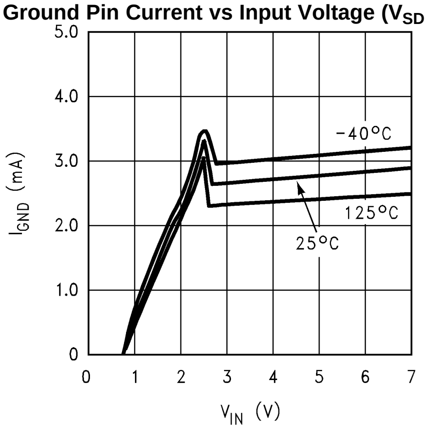


Figure 6.

Ground Pin Current vs Input Voltage (V_{SD}=100mV)

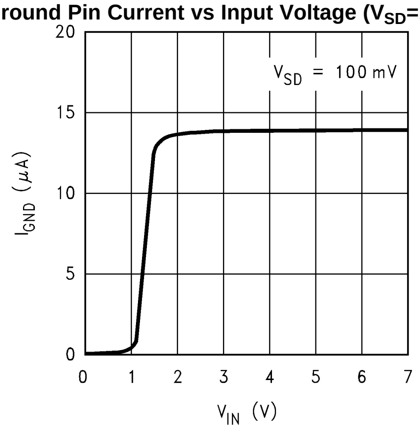


Figure 7.

Ground Current vs Temperature (V_{SD}=V_{IN})

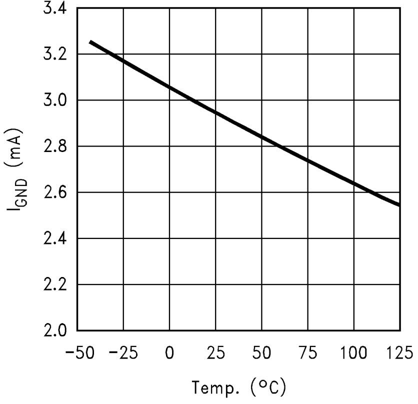


Figure 8.

Ground Current vs Temperature (V_{SD}=0V)

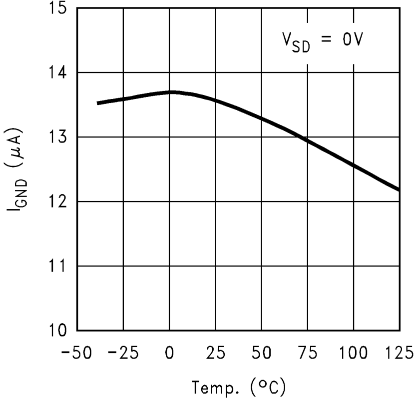


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 2.5V$, $C_{OUT} = 33\mu F$, $I_{OUT} = 10mA$, $C_{IN} = 68\mu F$, $V_{SD} = V_{IN}$, and $T_A = 25°C$.

Ground Pin Current vs Shutdown Pin Voltage

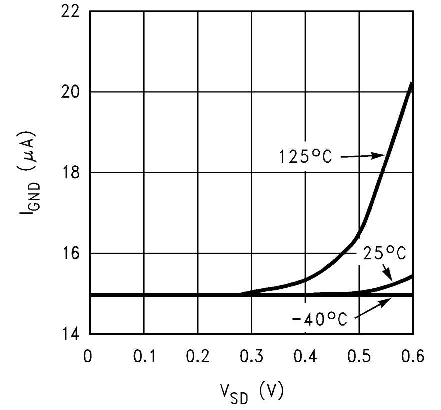


Figure 10.

Input Voltage vs Output Voltage

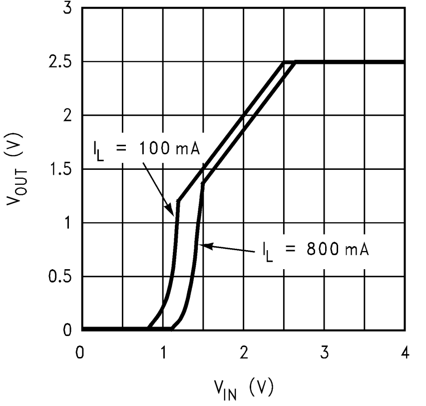


Figure 11.

Output Noise Density, V_{OUT}= 2.5V

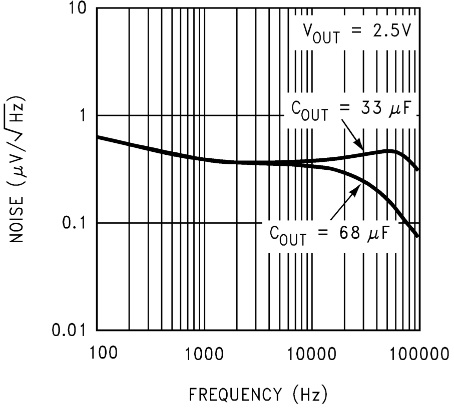


Figure 12.

Output Noise Density, V_{OUT}= 5V

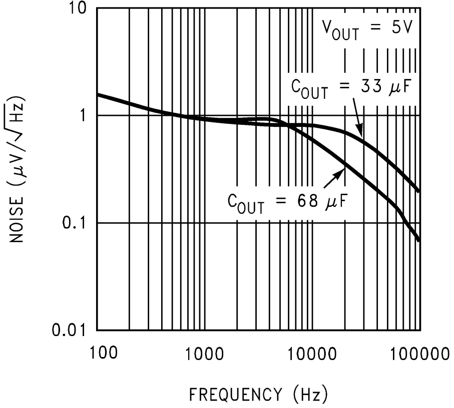


Figure 13.

Load Transient Response

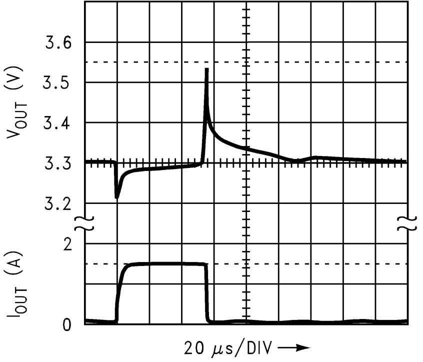


Figure 14.

Ripple Rejection vs Frequency

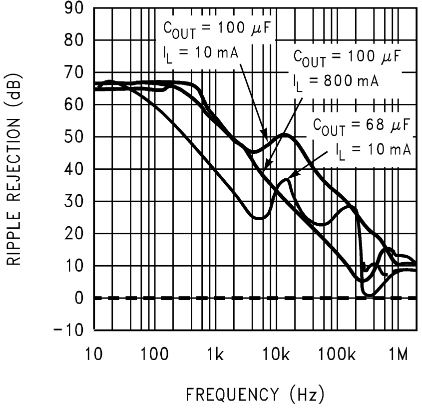
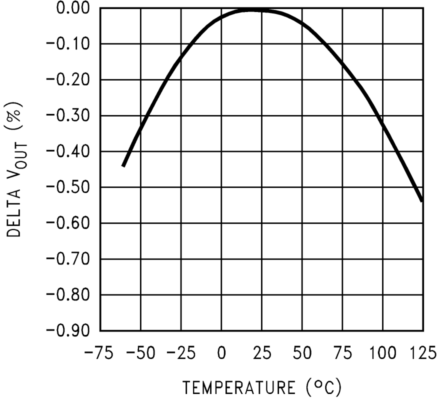


Figure 15.

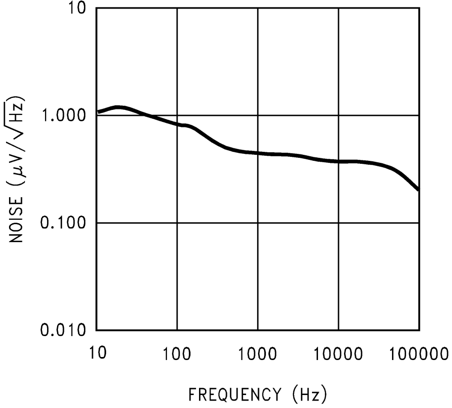
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, $V_{IN} = V_{O(NOM)} + 1V$, $V_{OUT} = 2.5V$, $C_{OUT} = 33\mu F$, $I_{OUT} = 10mA$, $C_{IN} = 68\mu F$, $V_{SD} = V_{IN}$, and $T_A = 25°C$.



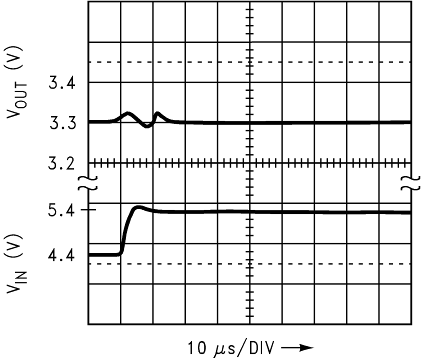
δV_{OUT} vs Temperature

Figure 16.



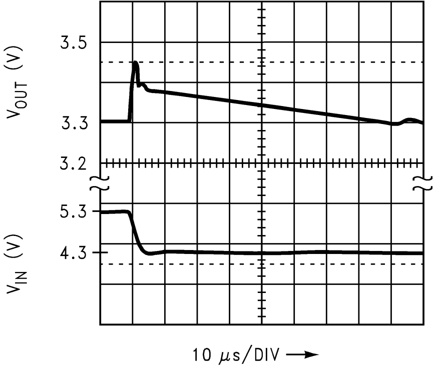
Noise Density $V_{IN} = 3.5V$, $V_{OUT} = 2.5V$, $I_L = 10$ mA

Figure 17.



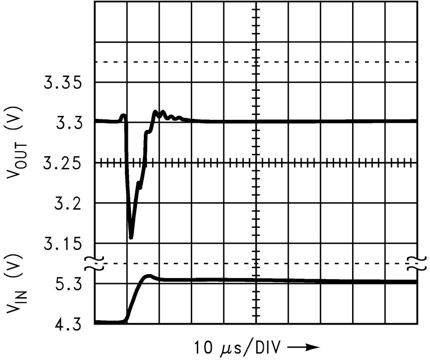
Line Transient Response

Figure 18.



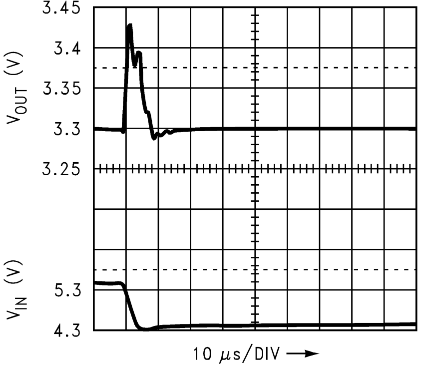
Line Transient Response

Figure 19.



Line Transient Response (I_{OUT} = 1.5A)

Figure 20.



Line Transient Response (I_{OUT} = 1.5A)

Figure 21.

APPLICATIONS INFORMATION

V_{IN} RESTRICTIONS FOR PROPER START-UP

Because the LP396XEP devices use on-chip CMOS logic for analog trimming of the output voltage, care must be taken not to apply an input voltage which can allow this logic to shift into random undefined logic states, as this can adversely affect the regulated output voltage. This will most likely occur if an input voltage between about 50mV and 200mV is applied to V_{IN} for a significant amount of time (more than several seconds). To prevent misoperation, ensure that V_{IN} is below 50mV before start-up is initiated. This problem can occur in systems with a backup battery using reverse-biased "blocking" diodes which may allow enough leakage current to flow into the V_{IN} node to raise it's voltage slightly above ground when the main power is removed. Using low leakage diodes or a resistive pull down can prevent the voltage at V_{IN} from rising above the sensitive threshold. Large bulk capacitors connected to V_{IN} may also cause a start-up problem if they do not discharge fully before re-start is initiated (but only if V_{IN} is allowed to fall below 1V). A resistor connected across the capacitor will allow it to discharge more quickly. It should be noted that the probability of a "false start" caused by incorrect logic states is extremely low .

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. these capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: The LP3962EP/5EP requires a low source impedance to maintain regulator stability because the internal bias circuitry is connected directly to V_{IN}. The input capacitor must be located less than 1 cm from the LP3962EP/5EP device and connected directly to the input and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum allowable input capacitance for a given application depends on the type of the capacitor and ESR (equivalent series resistance). A lower ESR capacitor allows the use of less capacitance, while higher ESR types (like aluminum electrolytics) require more capacitance.

The lowest value of input capacitance that can be used for stable full-load operation is 68 µF (assuming it is a ceramic or low-ESR Tantalum with ESR less than 100 mΩ).

To determine the minimum input capacitance amount and ESR value, an approximation which should be used is:

$$C_{IN}\ \text{ESR}\ (\text{m}\Omega)\ /\ C_{IN}\ (\mu\text{F}) \le 1.5 \tag{1}$$

This shows that input capacitors with higher ESR values can be used if sufficient total capacitance is provided. Capacitor types (aluminum, ceramic, and tantalum) can be mixed in parallel, but the total equivalent input capacitance/ESR must be defined as above to assure stable operation.

IMPORTANT: The input capacitor must maintain its ESR and capacitance in the "stable range" over the entire temperature range of the application to assure stability (see Capacitor Characteristics Section).

OUTPUT CAPACITOR: An output capacitor is also required for loop stability. It must be located less than 1 cm from the LP3962EP/5EP device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see PCB Layout section).

The minimum value of the output capacitance that can be used for stable full-load operation is 33 µF, but it may be increased without limit. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability. The ESR must fall within the specified range:

$$0.2\Omega \le C_{OUT}\ \text{ESR} \le 5\Omega \tag{2}$$

The lower limit of 200 mΩ means that ceramic capacitors are not suitable for use as LP3962EP/5EP output capacitors (but can be used on the input). Some ceramic capacitance can be used on the output if the total equivalent ESR is in the stable range: when using a 100 µF Tantalum as the output capacitor, approximately 3 µF of ceramic capacitance can be applied before stability becomes marginal.

IMPORTANT: The output capacitor must meet the requirements for minimum amount of capacitance and also have an appropriate ESR value over the full temperature range of the application to assure stability (see Capacitor Characteristics Section).

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good Tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see Capacitor Characteristics Section).

CAPACITOR CHARACTERISTICS

CERAMIC: For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM: Solid Tantalum capacitors are recommended for use on the output because their typical ESR is very close to the ideal value required for loop compensation. They also work well as input capacitors if selected to meet the ESR requirements previously listed.

Tantalums also have good temperature stability: a good quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to −40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

ALUMINUM: This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either Tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to −40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP396XEP. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the LP3962EP/5EP using traces which do not have other currents flowing in them Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the LP3962EP/5EP IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem.

Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the LP396XEP regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the LP396XEP.

If a load is connected to the LP396XEP output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the LP396XEP output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. The means the effective output impedance of the LP396XEP at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the LP396XEP may need RF isolation from the load. It is recommended that some inductance be placed between the LP396XEP output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT ADJUSTMENT

An adjustable output device has output voltage range of 1.215V to 5.1V. To obtain a desired output voltage, the following equation can be used with R1 always a 10kΩ resistor.

$$R2 = R1\left(\frac{V_{OUT}}{1.216} - 1\right) \tag{3}$$

For output stability, C_F must be between 68pF and 100pF.

OUTPUT NOISE

Noise is specified in two ways-

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output Noise or **Broad-band noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/√Hz or nV/√Hz and total output noise is measured in µV(rms).

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3962EP/LP3965EP achieves low noise performance and low quiescent current operation.

The total output noise specification for LP3962EP/LP3965EP is presented in the Electrical Characteristics table. The Output noise density at different frequencies is represented by a curve under typical performance characteristics.

SHORT-CIRCUIT PROTECTION

The LP3962and LP3965 is short circuit protected and in the event of a peak over-current condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the section on thermal information for power dissipation calculations.

ERROR FLAG OPERATION

The LP3962EP/LP3965EP produces a logic low signal at the Error Flag pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in Figure 22 shows the relationship between the ERROR and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the Error Flag.

The internal Error flag comparator has an open drain output stage. Hence, the ERROR pin should be pulled high through a pull up resistor. Although the ERROR pin can sink current of 1mA, this current is energy drain from the input supply. Hence, the value of the pull up resistor should be in the range of 10kΩ to 1MΩ. **The ERROR pin must be connected to ground if this function is not used.** It should also be noted that when the shutdown pin is pulled low, the ERROR pin is forced to be invalid for reasons of saving power in shutdown mode.

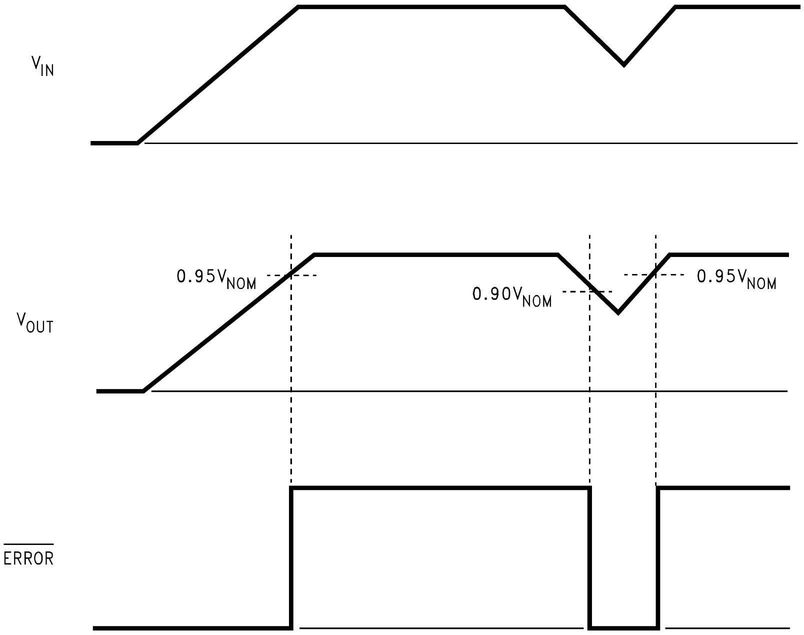


Figure 22. Error Flag Operation

SENSE PIN

In applications where the regulator output is not very close to the load, LP3965EP can provide better remote load regulation using the SENSE pin. Figure 23 depicts the advantage of the SENSE option. LP3962EP regulates the voltage at the output pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3V output, if the trace resistance is 100mΩ, the voltage at the remote load will be 3.15V with 1.5 A of load current, I_{LOAD}. The LP3965EP regulates the voltage at the sense pin. Connecting the sense pin to the remote load will provide regulation at the remote load, as shown in Figure 23. If the sense option pin is not required, the sense pin must be connected to the V_{OUT} pin.

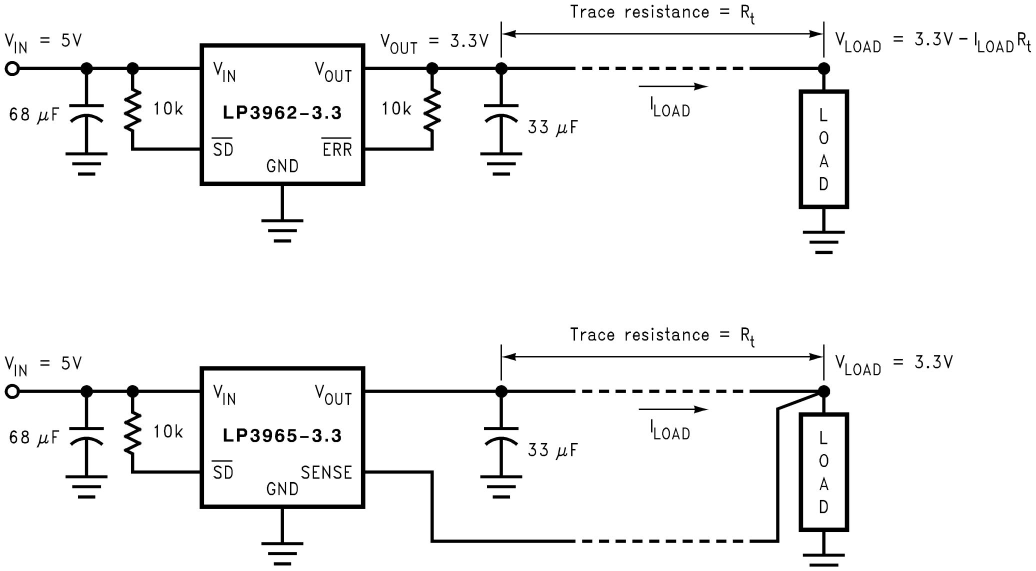


Figure 23. Improving remote load regulation using LP3965EP

SHUTDOWN OPERATION

A CMOS Logic level signal at the shutdown ($\overline{SD}$) pin will turn-off the regulator. Pin $\overline{SD}$ must be actively terminated through a 10kΩ pull-up resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

DROPOUT VOLTAGE

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the output voltage. The LP3962EP/LP3965EP use an internal MOSFET with an Rds(on) of 240mΩ (typically). For CMOS LDOs, the dropout voltage is the product of the load current and the Rds(on) of the internal MOSFET.

REVERSE CURRENT PATH

The internal MOSFET in LP3962EP and LP3965EP has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200mA continuous and 1A peak.

MAXIMUM OUTPUT CURRENT CAPABILITY

LP3962 and LP3965 can deliver a continuous current of 1.5 A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$P_D = (V_{IN}-V_{OUT})I_{OUT} + (V_{IN})I_{GND}$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature(T_{Jmax}):

$T_{Rmax} = T_{Jmax} - T_{Amax}$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$\theta_{JA} = T_{Rmax} / P_D$

LP3962 and LP3965 are available in TO-220, DDPAK, and SOT-223 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package, ≥60 °C/W for DDPAK package, and ≥ 140 °C/W for SOT-223 package, no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEATSINKING TO-220 PACKAGES

The thermal resistance of a TO220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be same as shown in next section for DDPAK package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$\theta_{HA} \leq \theta_{JA} - \theta_{CH} - \theta_{JC}$.

In this equation, θ_{CH} is the thermal resistance from the junction to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. θ_{JC} is about 3°C/W for a TO220 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEATSINKING DDPAK AND SOT-223 PACKAGES

The DDPAK and SOT223 packages use the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. Figure 24 shows a curve for the θ_{JA} of DDPAK package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

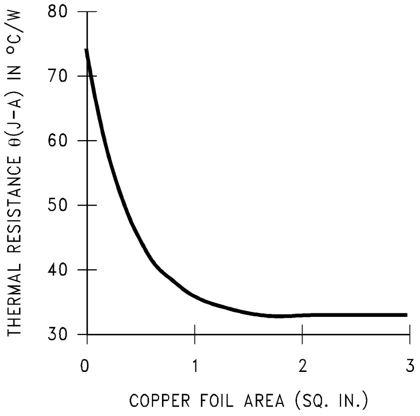


Figure 24. θ_{JA} vs Copper(1 Ounce) Area for DDPAK package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK packag mounted to a PCB is 32°C/W.

Figure 25 shows the maximum allowable power dissipation for DDPAK packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

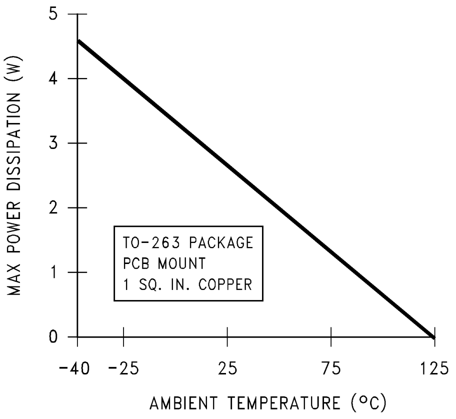


Figure 25. Maximum power dissipation vs ambient temperature for DDPAK package

Figure 26 shows a curve for the θ_{JA} of SOT-223 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

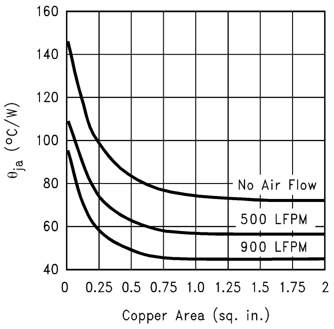


Figure 26. θ_{JA} vs Copper(1 Ounce) Area for SOT-223 package

The following figures show different layout scenarios for SOT-223 package.

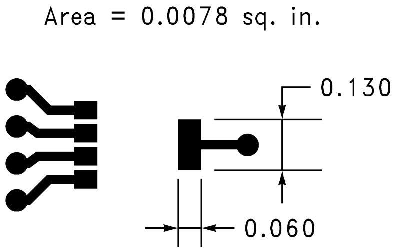


Figure 27. SCENARIO A, θ_{JA} = 148°C/W

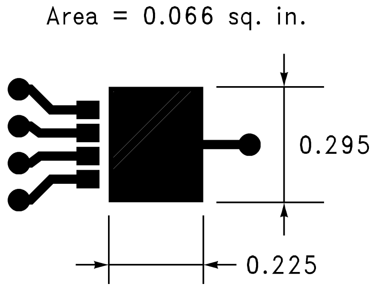


Figure 28. SCENARIO B, θ_{JA} = 125°C/W

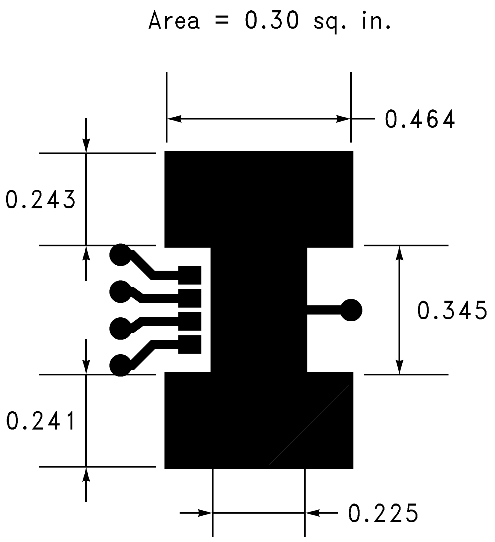


Figure 29. SCENARIO C, θ_{JA} = 92°C/W

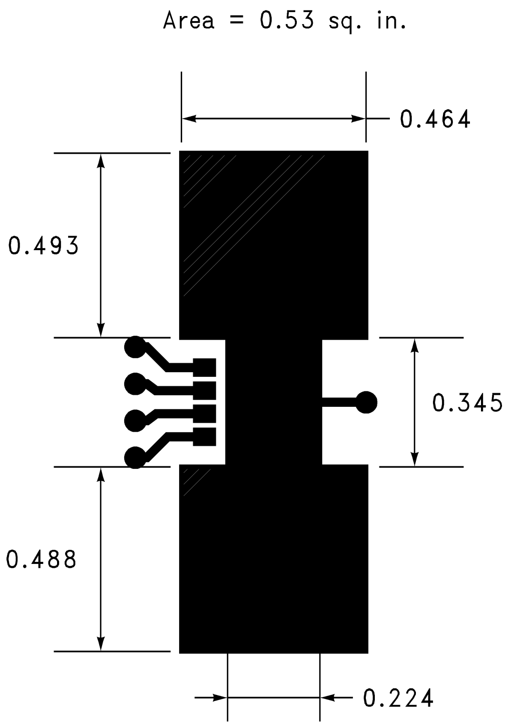


Figure 30. SCENARIO D, θ_{JA} = 83°C/W

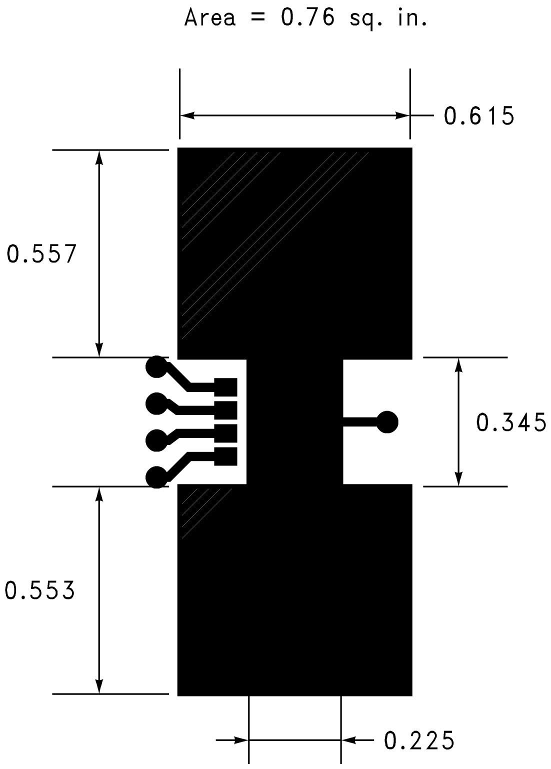


Figure 31. SCENARIO E, θ_{JA} = 77°C/W

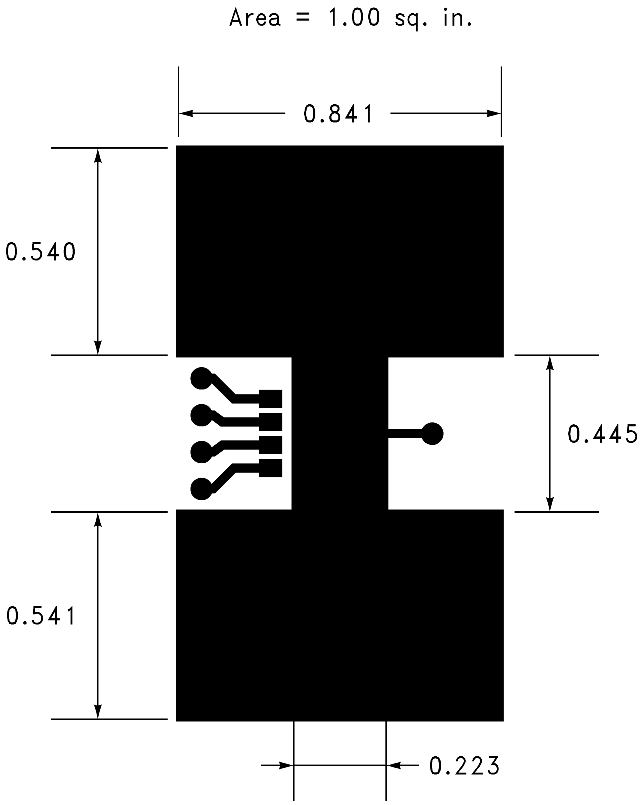


Figure 32. SCENARIO F, θ_{JA} = 75°C/W

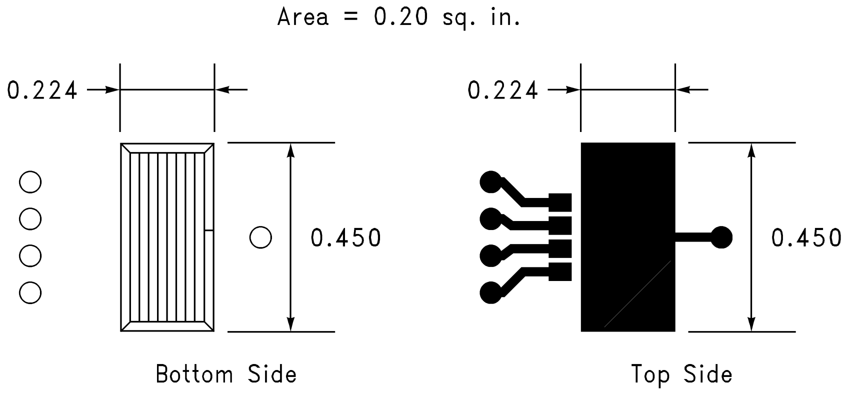


Figure 33. SCENARIO G, θ_{JA} = 113°C/W

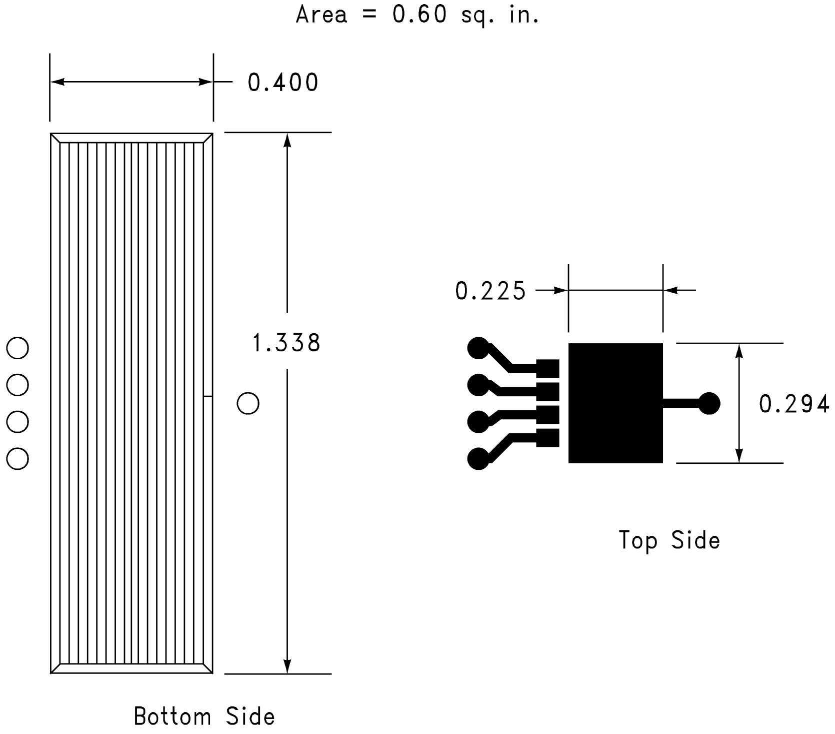


Figure 34. SCENARIO H, θ_{JA} = 79°C/W

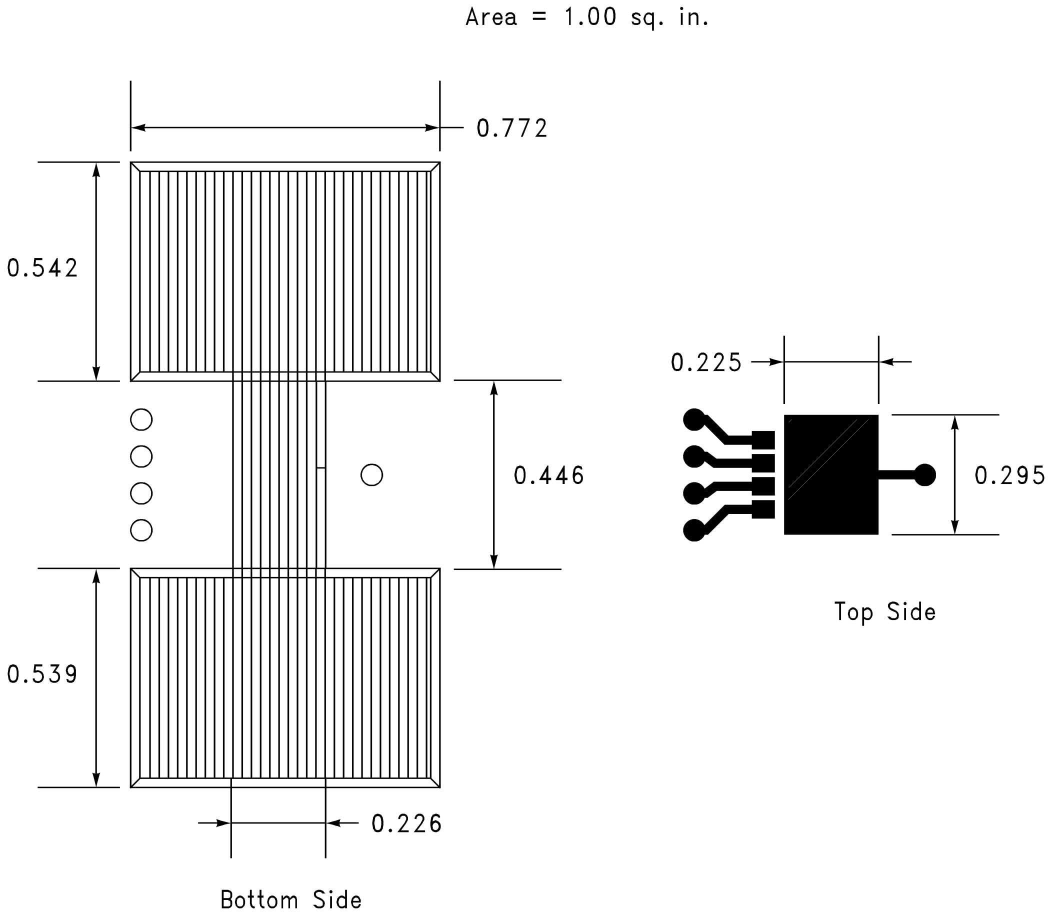


Figure 35. SCENARIO I, θ_{JA} = 78.5°C/W

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	20

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