LM27241 Synchronous Buck Regulator Controller for Mobile Systems

Check for Samples: LM27241

FEATURES

- **Input Voltage Range from 5.5V to 28V**
- **Forced-PWM or Pulse-Skip Modes**
- **Lossless Bottom-Side FET Current Sensing**
- **Adaptive Duty Cycle Clamping**
- **High Current N-Channel FET Drivers**
- **Low Shutdown Supply Currents**
- **Reference Voltage Accurate to Within ±1.5%**
- **Output Voltage Adjustable Down to 0.6V**
- **Power Good Flag and Chip Enable**
- **Under-Voltage Lockout**
- **Over-Voltage/Under-Voltage Protection**
- **Soft-Start and Soft-Shutdown**
- **Switching Frequency Adjustable 200kHz-500kHz**

APPLICATIONS

- **Notebook Chipset Power Supplies**
- **Low Output Voltage High Efficiency Buck Regulators**

DESCRIPTION

The LM27241 is an adjustable 200kHz-500kHz single channel voltage-mode controlled high-speed synchronous buck regulator controller. It is ideally suited for battery powered applications such as laptop and notebook computers. The LM27241 requires only N-channel FETs for both the upper and lower positions of the synchronous stage. It features line feedforward to improve the response to input transients. At very light loads, the user can choose between the high-efficiency Pulse-skip mode or the constant frequency Forced-PWM mode. Lossless current limiting without the use of external sense resistor is made possible by sensing the voltage drop across the bottom FET. A unique adaptive duty cycle clamping technique is incorporated to significantly reduce peak currents under abnormal load conditions. The input voltage range is 5.5V to 28V while the output voltage is adjustable down to 0.6V.

Standard supervisory and control features include soft-start, power good, output under-voltage and over-voltage protection, under-voltage lockout, soft-shutdown and enable.

Connection Diagram

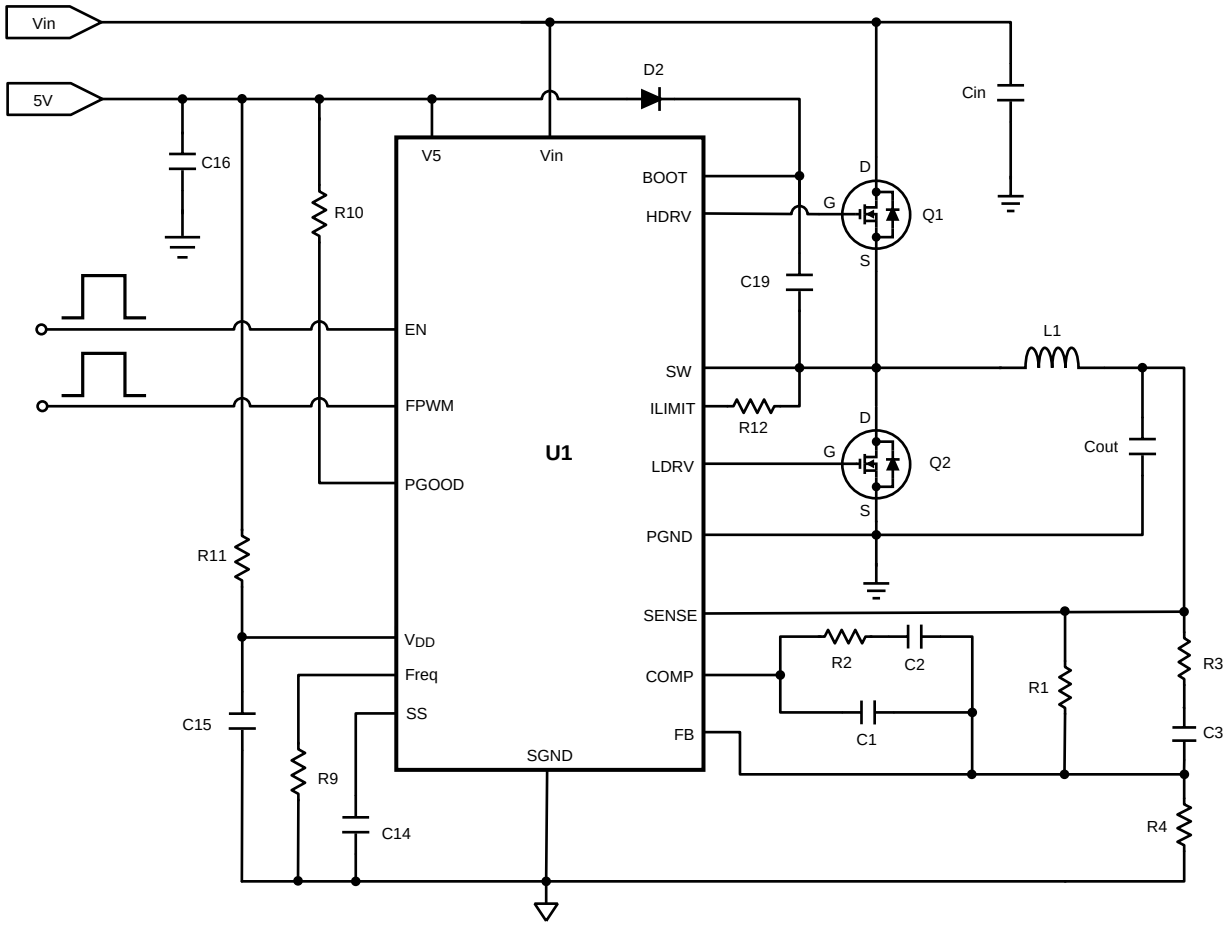


Figure 1. Typical Application
See Figure 23 for expanded view.

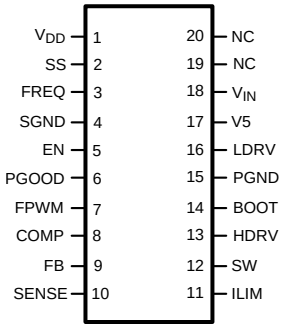


Figure 2. Top View
20-Lead TSSOP (PW)

PIN DESCRIPTION

Pin 1, VDD: 5V supply rail for the control and logic sections. For normal operation the voltage on this pin must be brought above 4.5V. Subsequently, the voltage on this pin (including any ripple component) should not be allowed to fall below 4V for a duration longer than 7µs. Since this pin is also the supply rail for the internal control sections, it should be well-decoupled particularly at high frequencies. A minimum 0.1µF-0.47µF (ceramic) capacitor should be placed on the component side very close to the IC with no intervening vias between this capacitor and the VDD/SGND pins. If the voltage on Pin 1 falls below the lower UVLO threshold, upper FET(s) are latched OFF and the lower FET(s) are latched ON. Power Not Good is then signaled immediately (on Pin 6). To initiate recovery, the EN pin must be taken below 0.8V and then back above 2V (with VDD held above 4.5V). Or the voltage on the VDD pin must be taken below 1.0V and then back again above 4.5V (with EN pin held above 2V). Normal operation will then resume assuming that the fault condition has been cleared.

Pin 2, SS: Soft-start pin. A Soft-start capacitor is placed between this pin and ground. A typical capacitance of 0.1µF is recommended between this pin and ground. The IC connects an internal 1.8 kΩ resistor (R_{SS_DCHG}, see Electrical Characteristics table) between this pin and ground to discharge any remaining charge on the Soft-start capacitor under several conditions. These conditions include the initial power-up sequence, start-up by toggling the EN pin, and also recovery from a fault condition. The purpose is to bring down the voltage on the Soft-start pin to below 100mV for obtaining reset. Reset having thus been obtained, an 11µA current source at this pin charges up the Soft-start capacitor. The voltage on this pin controls the maximum duty cycle, and this produces a gradual ramp-up of the output voltage, thereby preventing large inrush currents into the output capacitors. The voltage on this pin finally clamps close to 5V. This pin is connected to an internal 115µA current sink whenever a current limit event is in progress. This sink current discharges the Soft-start capacitor and forces the duty cycle low to protect the power components. When a fault condition is asserted (See Pin 9) the SS pin is internally connected to ground via the 1.8 kΩ resistor.

Pin 3, FREQ: Frequency adjust pin. The switching frequency is set by a resistor connected between this pin and ground. A value of 22.1kΩ sets the frequency to 300kHz (nominal). If the resistance is increased, the switching frequency decreases. An approximate relationship is that for every 7.3kΩ increase or decrease in the value of the frequency set resistor, the total switching period increases or decreases by 1µs.

Pin 4, SGND: Signal Ground pin. This is the lower rail for the control and logic sections. SGND should be connected on the PCB to the system ground, which in turn is connected to PGND. The layout is important and the recommendations in the section *Layout Guidelines* should be followed.

Pin 5, EN: IC Enable pin. When EN is taken high, the output is enabled by means of a Soft-start power-up sequence. When EN is brought low, Power Not Good is signaled within 100ns. This causes Soft-shutdown to occur (see Pins 2 and 6). The Soft-start capacitor is then discharged by an internal 1.8kΩ resistor (R_{SS_DCHG}, see Electrical Characteristics table). When the Enable pin is toggled, a fault condition is not asserted. Therefore in this case, the lower FET is not latched ON, even as the output voltage ramps down, eventually falling below the under-voltage threshold. In fact, in this situation, both the upper and the lower FETs are latched OFF, until the Enable pin is taken high again. If a fault shutdown has occurred, taking the Enable pin low and then high again (toggling), resets the internal latches, and the IC will resume normal switching operation.

Pin 6, PGOOD: Power Good output pin. An open-drain logic output that is pulled high with an external pull-up resistor, indicating that the output voltage is within a pre-defined Power Good window. Outside this window, the pin is internally pulled low (Power Not Good signaled) provided the output error lasts for more than 7µs. The pin is also pulled low within 100ns of the Enable pin being taken low, irrespective of the output voltage level. PGOOD must always first be "high" before it can respond to a proper fault "low" condition. Under fault assertion, the low-side MOSFET is always latched ON. This will not happen if regulation has not already been achieved.

Pin 7, FPWM: Logic input for selecting either the Forced PWM (FPWM) Mode or Pulse-skip Mode (SKIP). When the pin is driven high, the IC operates in the FPWM mode, and when pulled low or left floating, the SKIP mode is enabled. In FPWM mode, the lower FET is always ON whenever the upper FET is OFF (except for a narrow shoot-through protection deadband). This leads to continuous conduction mode of operation, which has a fixed frequency and (almost) fixed duty cycle down to very light loads. But this does reduce efficiency at light loads. The alternative mode is SKIP mode. This mode forces the lower MOSFET ON only until the voltage on the Switch pin is more negative than 2.2mV (typical). As an example, for a 21mΩ FET, this translates to a current threshold of 2.2mV/21mΩ = 0.1A. Therefore, if the (instantaneous) inductor current falls below this value, the lower FET will turn OFF every cycle at this point (when operated in SKIP mode). This threshold is set by the zero-cross Comparator in the Block Diagram. Note that if the inductor current is high enough to be always above this zero-cross threshold (V_{SW_ZERO}, see Electrical Characteristics table), there will be no observable difference between FPWM and SKIP mode settings (in steady-state). SKIP mode is clearly a discontinuous mode of operation. However, in conventional discontinuous mode, the duty cycle keeps falling (towards zero) as the load decreases. But the LM27241 does not allow the duty cycle to fall by more than 15% of its original value (at the CCM-DCM boundary). This forces pulse-skipping, and the average frequency is effectively decreased as the load decreases. This mode of operation improves efficiency at light loads, but the frequency is effectively no longer a constant. Note that *a minimum pre-load of 0.1mA should be maintained on the output to ensure regulation in SKIP mode.* The resistive divider from output to ground used to set the output voltage could be designed to serve as part or all of this required pre-load.

Pin 8, COMP: Compensation pin. This is also the output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to set the duty cycle for normal regulation. Since the Feedback pin is the inverting input of the same error amplifier, appropriate control loop compensation components are placed between this pin and the Feedback pin. The COMP pin is internally pulled low during Soft-start so as to limit the duty cycle. Once Soft-start is completed, the voltage on this pin can take up the value required to maintain output regulation. An internal voltage clamp at this pin forms an adaptive duty cycle clamp feature. This serves to limit the maximum allowable duty cycles and peak currents under sudden overloads. But at the same time it has enough headroom to permit an adequate response to step loads within the normal operating range.

Pin 9, FB: Feedback pin. This is the inverting input of the error amplifier. The voltage on this pin under regulation is nominally at 0.6V. A Power Good window on this pin determines if the output voltage is within regulation limits (±13%). If the voltage falls outside this window for more than 7µs, Power Not Good is signaled on the PGOOD pin (Pin 6). Output over-voltage and under-voltage conditions are also detected by comparing the voltage on the Feedback pin with appropriate internal reference voltage levels. If the voltage exceeds the safe window (±30%) for longer than 7µs, a fault condition is asserted. Then lower FET is latched ON and the upper FET is latched OFF.

PIN DESCRIPTION (continued)

Pin 10, SENSE: Output voltage sense pin. It is tied directly to the output rail. The SENSE pin voltage is used together with the VIN voltage (on Pin 18) to (internally) calculate the CCM (continuous conduction mode) duty cycle. This calculation is used by the IC to set the minimum duty cycle in the SKIP mode to 85% of the CCM value. It is also used to set the adaptive duty cycle clamp. An internal 20Ω resistor from the SENSE pin to ground discharges the output capacitor gently (Soft-shutdown) whenever Power Not Good is signaled on Pin 6.
Pin 11, ILIM: Current Limit pin. When the bottom FET is ON, a 62µA (typical) current flows out of the ILIM pin and into an external resistor that is connected to the drain of the lower MOSFET. This current through the resistor creates a voltage on the ILIM pin. However, the drain voltage of the lower MOSFET will go more negative as the load current is increased through the R_{DS_ON} of the MOSFET. At some value of instantaneous current, the voltage on this pin will transit from positive to negative. The point where it is zero is the current limiting condition and is detected by the Current Limit Comparator. When a current limit condition has been detected, the next ON-pulse of the upper FET will be omitted. The lower FET will again be monitored to determine if the current has fallen below the threshold. If it has, the next ON-pulse will be permitted. If not, the upper FET will be turned OFF and will stay so for several cycles if necessary, until the current returns to normal. Eventually, if the overcurrent condition persists, and the upper FET has not been turned ON, the output will clearly start to fall. Ultimately the output will fall below the under-voltage threshold, and a fault condition will be asserted by the IC.
Pin 12, SW: The Switching node of the buck regulator. Also serves as the lower rail of the floating driver of the upper FET.
Pin 13, HDRV: Gate drive pin for the upper FET. The top gate driver is interlocked with the bottom gate driver to prevent shoot-through/cross-conduction.
Pin 14, BOOT: Bootstrap pin. This is the upper supply rail for the floating driver of the upper FET. It is bootstrapped by means of a ceramic capacitor connected to the channel Switching node. This capacitor is charged up by the IC to a value of about 5V as derived from the V5 pin (Pin 17).
Pin 15, PGND: Power Ground pin. This is the return path for the bottom FET gate drive. The PGND is to be connected on the PCB to the system ground and also to the Signal ground (Pin 4) in accordance with the recommended Layout Guidelines .
Pin 16, LDRV: Gate drive pin for the bottom FET (Low-side drive). The bottom gate driver is interlocked with the top gate driver to prevent shoot-through/cross-conduction. It is always latched high when a fault condition is asserted by the IC.
Pin 17, V5: Upper rail of the lower FET driver. Also used to charge up the bootstrap capacitor of the upper FET driver. This is connected to an external 5V supply. The 5V rail may be the same as the rail used to provide power to the VDD pin (Pin 1), but the VDD pin will then require to be well-decoupled so that it does not interact with the V5 pin. A low-pass RC filter consisting of a ceramic 0.1µF capacitor (preferably 0.22µF) and a 10Ω resistor will suffice as shown in the Typical Applications circuit.
Pin 18, VIN: The input to the Buck regulator power stage. It is also used by the internal ramp generator to implement the line feedforward feature. The VIN pin is also used with the SENSE pin voltage to predict the CCM (continuous conduction mode) duty cycle and to thereby set the minimum allowed DCM duty cycle to 85% of the CCM value. This is a high input impedance pin, drawing only about 100µA (typical) from the input rail.
Pin 19, 20 NC: No Connect.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Voltages from the indicated pins to SGND/PGND unless otherwise indicated[3]	VIN	-0.3V to 30V
	V5	-0.3V to 7V
	VDD	-0.3V to 7V
	BOOT	-0.3V to 36V
	BOOT to SW	-0.3V to 7V
	SW	-0.3V to 30V
	ILIM	-0.3V to 30V
	SENSE, FB	-0.3V to 7V
	PGOOD	-0.3V to 7V
	EN	-0.3V to 7V
Power Dissipation (T_A = 25°C)[4]		0.75W
Junction Temperature		+150°C
ESD Rating[5]		2kV
Ambient Storage Temperature Range		-65°C to +150°C
Soldering Dwell Time, Temperature	Wave	4 sec, 260°C
	Infrared	10 sec, 240°C
	Vapor Phase	75 sec, 219°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. For ensured performance limits and associated test conditions, see the Electrical Characteristics table.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) PGND and SGND are all electrically connected together on the PCB.

(4) The maximum allowable power dissipation is calculated by using $P_{Dmax} = (T_{JMAX} - T_A) / \theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 0.75W rating of the TSSOP-20 package for example results from using 125°C, 25°C, and 118°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. The rated power dissipation should be derated by 10mW/°C above 25°C ambient for the TSSOP package. The θ_{JA} value above represents the worst-case condition with no heat sinking. Heat sinking will permit more power to be dissipated at higher ambient temperatures. For detailed information on soldering plastic TSSOP package, refer to http://www.ticom/packaging/.

(5) ESD is applied by the human body model, which is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings[1]

VIN	5.5V to 28V
VDD, V5	4.5V to 5.5V
Junction Temperature	-5°C to +125°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. For ensured performance limits and associated test conditions, see the Electrical Characteristics table.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** apply over full Operating Junction Temperature range. VDD = V5 = 5V, V_{SGND} = V_{PGND} = 0V, VIN = 15V, V_{EN} = 3V, R_{FADJ} = 22.1K unless otherwise stated (1). Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typical (2)	Max	Units
Reference						
V_{FB_REG}	FB Pin Voltage at Regualtion	VDD = 4.5V to 5.5V, VIN = 5.5V to 28V	**591**	600	**609**	mV
$V_{FB\_LINE\ REG}$	V_{FB} Line Regulation	VDD = 4.5V to 5.5V, VIN = 5.5V to 28V		0.5		
I_{FB}	FB Pin Current (sourcing)	V_{FB} at regulation		20	**100**	nA
Chip Supply						
I_{Q_VIN}	VIN Quiescent Current	V_{FB} = 0.7V		100	**200**	µA
I_{SD_VIN}	VIN Shutdown Current	V_{EN} = 0V		0	**5**	µA
I_{Q_VDD}	VDD Quiescent Current	V_{FB}= 0.7V		1.75	**3**	mA
I_{SD_VDD}	VDD Shutdown Current	V_{EN} = 0V		8	**15**	µA
I_{Q_V5}	V5 Normal Operating Current	V_{FB} = 0.7V		0.3	**0.5**	mA
		V_{FB} = 0.5V		0.5	**1.25**	
I_{SD_V5}	V5 Shutdown Current	V_{EN} = 0V		0	**5**	µA
I_{Q_BOOT}	BOOT Quiescent Current	V_{FB} = 0.7V		2	**5**	µA
		V_{FB} = 0.5V		300	**500**	
I_{SD_BOOT}	BOOT Shutdown Current	V_{EN} = 0V		1	**5**	µA
V_{DD_UVLO}	VDD UVLO Threshold	VDD rising from 0V	**3.9**	4.2	**4.5**	V
HYS_{VDD_UVLO}	VDD UVLO Hysteresis	VDD = V5 falling from V_{DD_UVLO}	**0.5**	0.7	**0.9**	V
Logic						
I_{EN}	EN Input Current	V_{EN} = 0 to 5V		0		µA
V_{EN_HI}	EN Input Logic High		**2**	1.8		V
V_{EN_LO}	EN Input Logic Low			1.3	**0.8**	V
R_{FPWM}	FPWM Pull-down	V_{FPWM} = 2V	**100**	200	**1000**	kΩ
V_{FPWM_HI}	FPWM Input Logic High		**2**	1.8		V
V_{FPWM_LO}	FPWM Input Logic Low			1.3	**0.8**	V
Power Good						
V_{PGOOD_HI}	Power Good Upper Threshold as a Percentage of Internal Reference	FB voltage rising above V_{FB_REG}	**110**	113	**116**	%
V_{PGOOD_LOW}	Power Good Lower Threshold as a Percentage of Internal Reference	FB voltage falling below V_{FB_REG}	**84**	87	**90**	%
HYS_{PGOOD}	Power Good Hysteresis			7		%
Δt_{PG_OK}	Power Good Delay	From output voltage “good” to PGOOD assertion.	**10**	20	**30**	µs
Δt_{PG_NOK}		From the output voltage “bad” to PGOOD de-assertion	**4**	7	**10**	
Δt_{SD}		From Enable low to PGOOD low		0.03	**0.1**	
V_{PGND_SAT}	PGOOD Saturation Voltage	PGOOD de-asserted (Power Not Good) and sinking 1.5mA		0.12	**0.4**	V
I_{PGOOD_LEAK}	PGOOD Leakage Current	PGOOD = 5V and asserted		0	**1**	µA
OV and UV Protection						
V_{OVP_RISING}	Fault OVP Latch Threshold as a Percentage of Internal Reference	FB voltage rising above V_{FB_REG}	**125**	130	**135**	%
$V_{OVP\_FALLING}$	Fault UVP Latch Threshold as a Percentage of Internal Reference	FB voltage falling below V_{FB_REG}	**65**	70	**75**	%

(1) R_{FADJ} is the frequency adjust resistor between FREQ pin and Ground.
(2) Typical numbers are at 25°C and represent the most likely norm.

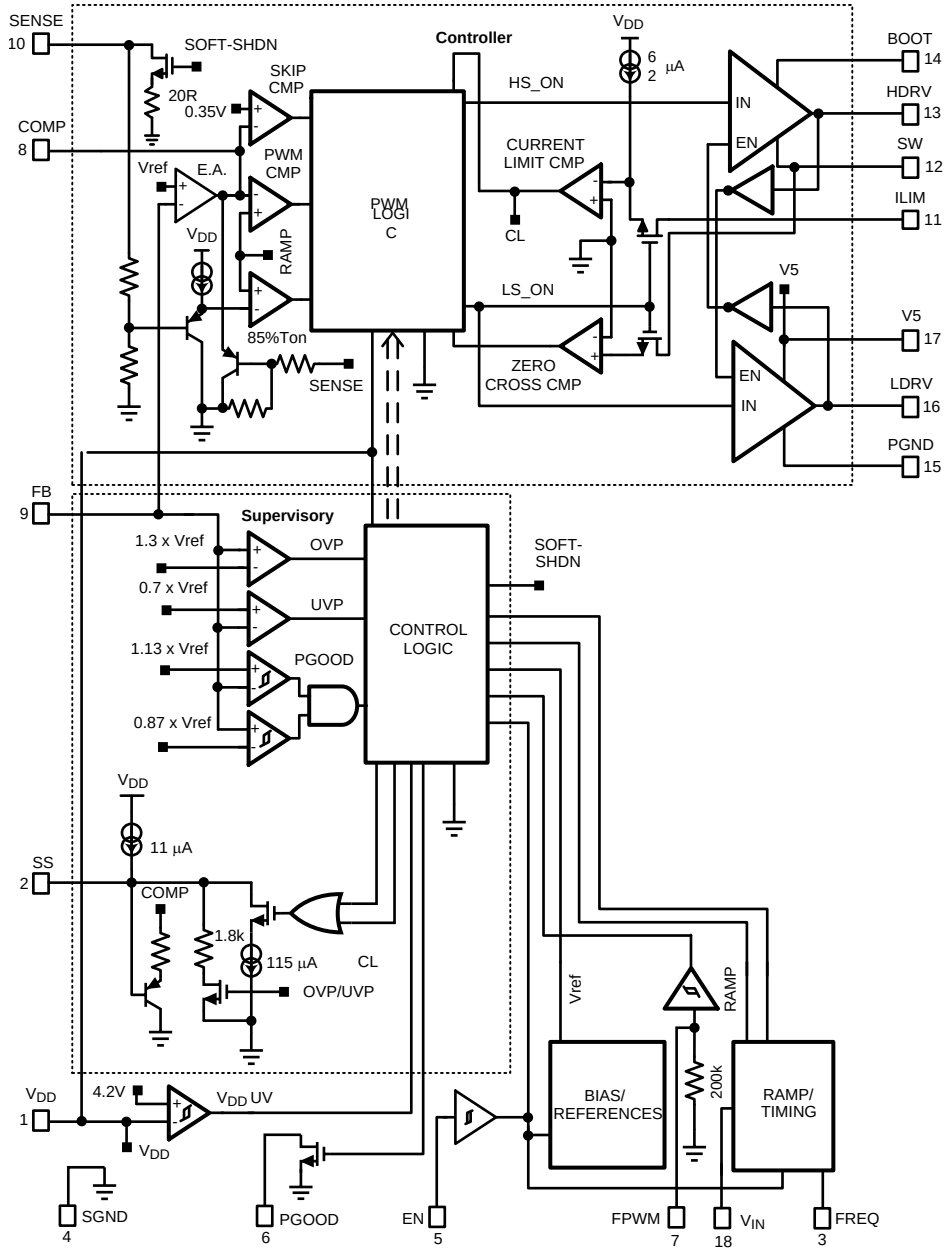
Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** apply over full Operating Junction Temperature range. VDD = V5 = 5V, V_{SGND} = V_{PGND} = 0V, VIN = 15V, V_{EN} = 3V, R_{FADJ} = 22.1K unless otherwise stated (1). Datasheet min/max specification limits are ensured by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typical (2)	Max	Units
Δt_{FAULT}	Fault Delay	From Fault detection (any output) to Fault assertion		7		µs
Soft-start						
I_{SS_CHG}	Soft-start Charging Current	V_{SS} = 1V	**8**	11	**14**	µA
R_{SS_DCHG}	Soft-shutdown Resistance (SS pin to SGND)	V_{EN} = 0V, V_{SS} = 1V		1800		Ω
I_{SS_DCHG}	Soft-start Discharge Current	In Current Limit	**80**	115	**160**	µA
V_{SS_RESET}	Soft-start pin reset voltage (3)	SS charged to 0.5V, EN low to high		100		mV
V_{OS}	SS to COMP Offset Voltage	V_{SS} = 0.5V and 1V, V_{FB} = 0V		600		mV
Error Amplifier						
GAIN	DC Gain			70		dB
V_{SLEW}	Voltage Slew Rate	COMP rising		4.45		V/µs
		COMP falling		2.25		
BW	Unity Gain Bandwidth			6.5		MHz
I_{COMP_SOURCE}	COMP Source Current	V_{FB} < V_{FB_REG} V_{COMP} = 0.5V	**2**	5		mA
I_{COMP_SINK}	COMP Sink Current	V_{FB} > V_{FB_REG} V_{COMP} = 0.5V	**7**	14		mA
Current Limit and Zero-Cross						
I_{ILIM}	ILIM Pin Current (sourcing)	V_{ILIM} = 0V	**46**	62	**76**	µA
V_{ILIM_TH}	I_{ILIM} Threshold Voltage		**-10**	0	**10**	mV
V_{SW_ZERO}	Zero-cross Threshold (SW Pin)	LDRV goes low		-2.2		mV
Oscillator						
F_{OSC}	PWM Frequency	R_{FADJ} = 22.1kΩ	**255**	300	**345**	kHz
		R_{FADJ} = 12.4kΩ		500		
		R_{FADJ} = 30.9kΩ		200		
V_{RAMP}	PWM Ramp Peak-to-peak Amplitude	VIN = 15V		1.6		V
		VIN = 24V		2.95		
V_{VALLEY}	PWM Ramp Valley			0.8		V
ΔF_{OSC_VIN}	Frequency Change with VIN	VIN = 5.5V to 24V		±1		%
ΔF_{OSC_VDD}	Frequency Change with VDD	VDD = 4.5V to 5.5V		±2		%
V_{FREQ_VIN}	FREQ Pin Voltage vs. VIN			0.105		V/V
System						
t_{ON_MIN}	Minimum ON Time	V_{FPWM} = 3V		30		ns
D_{MAX}	Maximum Duty Cycle	VIN = 5.5V	**60**	75		%
		VIN = 15V	**40**	50		%
		VIN = 28V, VDD= 4.5V	**22**	28		%
Gate Drivers						
R_{HDRV_SOURCE}	HDRV Source Impedance	HDRV Pin Current (sourcing)= 1.2A		7		Ω
R_{HDRV_SINK}	HDRV Sink Impedance	HDRV Pin Current (sinking) = 1A		2		Ω
R_{LDRV_SOURCE}	LDRV Source Impedance	LDRV Pin Current (sourcing) = 1.2A		7		Ω
R_{LDRV_SINK}	LDRV Sink Impedance	LDRV Pin Current (sinking) = 2A		1		Ω
t_{DEAD}	Cross-conduction Protection Delay (deadtime)	HDRV Falling to LDRV Rising		40		ns
		LDRV Falling to HDRV Rising		70		

(3) If the LM27241 starts up with a pre-charged soft start capacitor, it will first discharge the capacitor to V_{SS_RESET} and then begin the normal Soft-start process.

Block Diagram



Typical Performance Characteristics

Input Voltage is 12V, 18V, 24V (in order) starting from uppermost curve to lowermost curve in each of the Efficiency plots below.

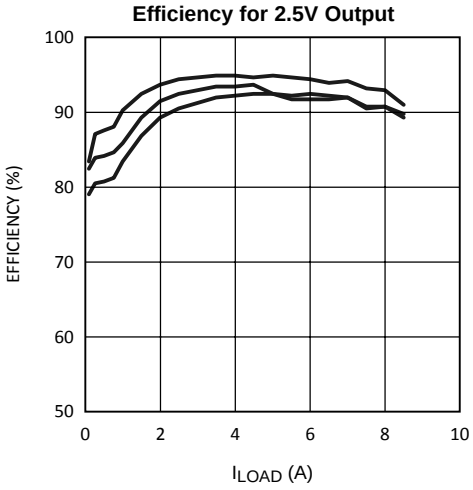


Figure 3.

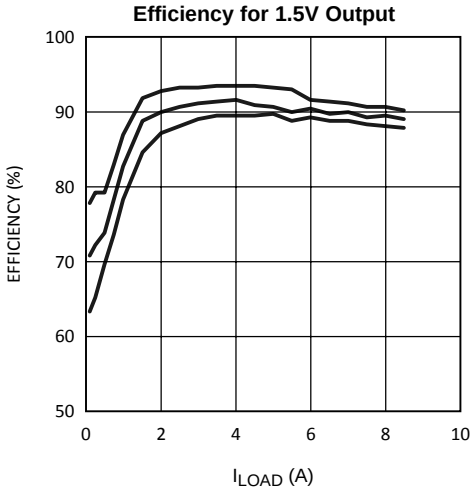


Figure 4.

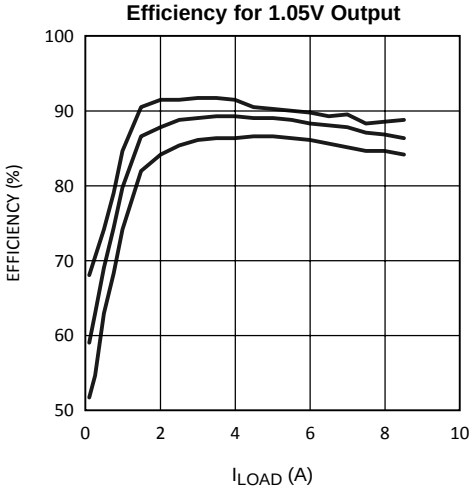


Figure 5.

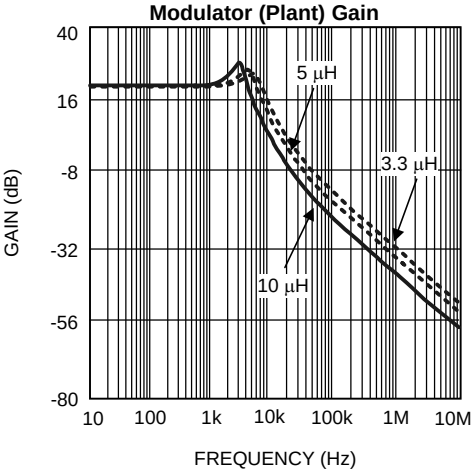


Figure 6.

OPERATION DESCRIPTIONS

GENERAL

The LM27241 is a synchronous buck controller using a voltage-mode control topology. This topology was selected to provide fixed-frequency PWM regulation at very low duty cycles, in preference to current-mode control, because the latter has inherent limitations in being able to achieve low pulse widths due to blanking time requirements. Because of a minimum pulse width of about 30ns for the LM27241, very low duty cycles (low output, high input) are possible. The main advantage of current-mode control is the fact that the slope of its ramp (derived from the switch current), automatically increases with increase in input voltage. This leads to improved line rejection and fast response to line variations. In typical voltage-mode control, the ramp is derived from the clock, not from the switch current. But by using the input voltage together with the clock signal to generate the ramp as in the LM27241, this advantage of current-mode control can in fact be completely replicated. The technique is called line feedforward. In addition, the LM27241 features a user-selectable Pulse-skip mode that significantly improves efficiency at light loads by reducing switching losses, and driver consumption, both of which are proportional to switching frequency.

INPUT VOLTAGE FEEDFORWARD

The feedforward circuit of the LM27241 adjusts the slope of the internal PWM ramp in proportion to the regulator input voltage. See Figure 7 for an illustration of how the duty cycle changes as a result of the change in the slope of the ramp, even though the error amplifier output has not had time to react to the line disturbance. The almost instantaneous duty cycle correction provided by the feedforward circuit significantly improves line transient rejection.

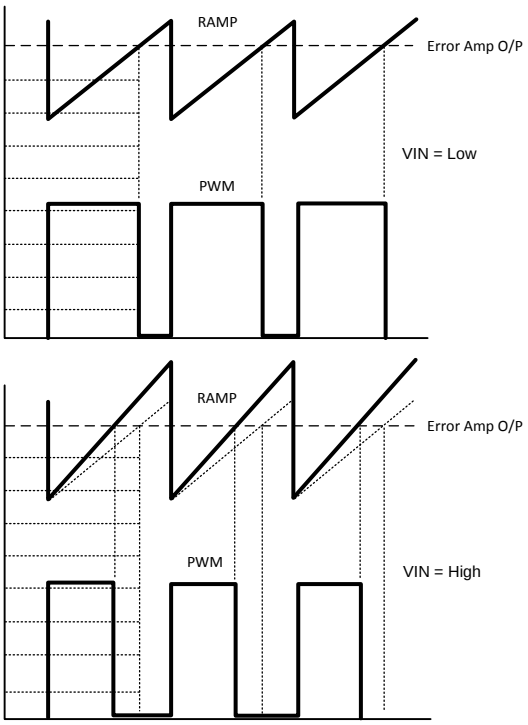
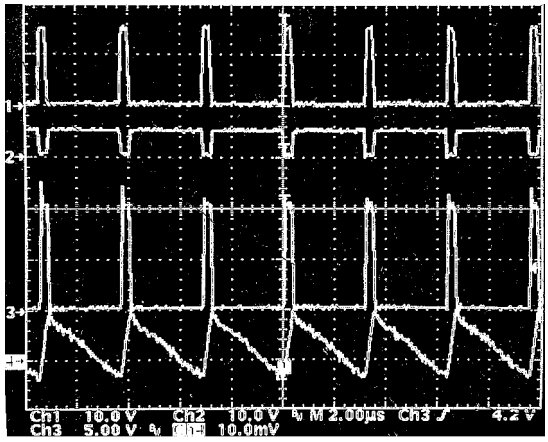


Figure 7. Voltage Feedforward

FORCED-PWM MODE AND PULSE-SKIP MODE

Forced-PWM mode (FPWM) leads to Continuous Conduction Mode (CCM) even at very light loads. It is one of two user-selectable modes of operation provided by the LM27241. When FPWM is chosen (FPWM pin high), the bottom FET will always be turned ON whenever the top FET is OFF. See Figure 8 for a typical FPWM plot.



CH1: HDRV, CH2: LDRV, CH3: SW, CH4: I_L (0.2A/div)
Output 1V @ 0.04A, VIN = 10V, FPWM, L = 10µH, f = 300kHz

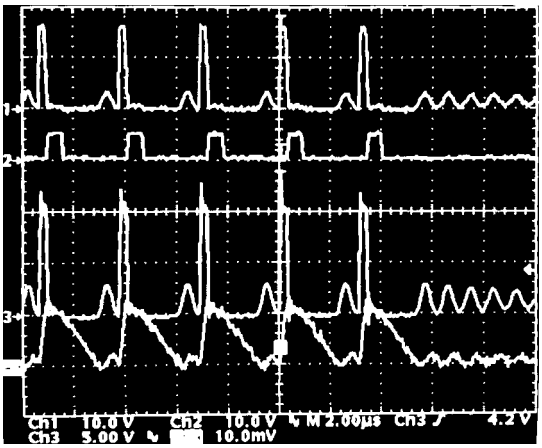
Figure 8. Normal FPWM Mode Operation at Light Loads

In a conventional converter, as the load is decreased to about 10% - 30% of maximum load current, DCM (Discontinuous Conduction Mode) occurs. In this condition the inductor current falls to zero during the OFF-time, and stays there until the start of the next switching cycle. In this mode, if the load is decreased further, the duty cycle decreases (pinches off), and ultimately may decrease to the point where the required pulse width becomes less than the minimum ON-time achievable by the converter (controller + FETs). Then a sort of random skipping behavior occurs as the error amplifier struggles to maintain regulation. This is not the most desirable type of behavior. There are two modes of operation that address this issue.

The first method is to keep the lower FET ON until the start of the next cycle (as in the LM27241 operated in FPWM mode). This allows the inductor current to drop to zero and then actually reverse direction (negative direction through inductor, passing from Drain to Source of lower FET, see Channel 4 in Figure 8). Now the current can continue to flow continuously till the end of the switching cycle. This maintains CCM and therefore the duty cycle does not start to pinch off as in typical DCM. Nor does it lead to the undesirable random skipping described above. Note that the pulse width (duty cycle) for CCM is virtually constant for any load and therefore does not usually run into the minimum ON-time restriction. The LM27241 can exhibit skip pulsing in FPWM when the Duty-Cycle is very low, and the switching frequency is high (minimum ON-Time). Let us check the LM27241 to rule out this remote possibility. For example, with an input of 24V, an output of 1V, the duty cycle is 1/24 = 4.2%. This leads to a required ON-time of 0.042* 3.3 = 0.14 µs at a switching frequency of 300kHz (T=3.3 µs). Since 140ns exceeds the minimum ON-time of 30ns of the LM27241, normal constant frequency CCM mode of operation is assured in FPWM mode, at virtually any load.

Another way out of the problematic spontaneous DCM operation is the second operating mode of the LM27241, the Pulse-skip (SKIP) Mode. In SKIP Mode, a zero-cross detector at the SW pin turns off the bottom FET when the inductor current decays to zero (actually at V_{SW_ZERO}, see Electrical Characteristics table). This would however still amount to conventional DCM, with its associated problems at extremely light loads as described earlier. The LM27241 however avoids the random skipping behavior described earlier, and replaces it with a more defined or formal SKIP mode. In conventional DCM, a converter would try to reduce its duty cycle from the CCM value as the load decreases, as explained previously. So it would start with the CCM duty cycle value (at the CCM-DCM boundary), but as the load decreases, the duty cycle would try to shrink to zero. However, in the LM27241, the DCM duty cycle is not allowed to fall below 85% of the CCM value. So when the theoretically required DCM duty cycle value falls below what the LM27241 is allowed to deliver (in this mode), pulse-skipping starts. It will be seen that several of these excess pulses may be delivered, until the output capacitors charge up enough to notify the error amplifier and cause its output to reverse. Thereafter several pulses could be skipped entirely until the output of the error amplifier again reverses. The SKIP mode leads to a reduction in the average switching frequency. Switching losses and FET driver losses, both of which are proportional to switching frequency, are significantly reduced at very light loads and efficiency is boosted. SKIP mode also reduces the circulating currents and energy associated with the FPWM mode. See Figure 9 for a typical plot of SKIP mode at

very light loads. Note the bunching of several fixed-width pulses followed by skipped pulses. The average frequency can actually fall very low at very light loads. Note however that when this happens the inductor core is seeing only very mild flux excursions, and so no significant audible noise is created. If EMI is a particularly sensitive issue for the particular application, the user can simply opt for the slightly less efficient, though constant frequency FPWM mode.



CH1: HDRV, CH2: LDRV, CH3: SW, CH4: I_L (0.2A/div)
Output 1V @ 0.04A, VIN = 10V, SKIP, L = 10µH, f = 300kHz

Figure 9. Normal SKIP Mode Operation at Light Loads

The SKIP mode is enabled when the FPWM pin is held low (or left floating). Note that at higher loads, and under steady state conditions (above CCM-DCM boundary), there will be absolutely no difference in the behavior of the LM27241 or the associated converter waveforms based on the voltage applied on the FPWM pin. The differences show up only at light loads.

Under startup, the peak current through the inductor is higher than the steady state peak current. This is due to the output capacitors being charged up to the regulated output voltage. There will be no observable difference in the shape of the ramp-up of the output rails in either SKIP mode or FPWM mode. The design has thus forced the startup waveforms to be identical irrespective of whether the FPWM mode or the SKIP mode has been selected.

The designer must realize that even at zero load condition, there is circulating current when operating in FPWM mode. This is illustrated in Figure 10. Duty cycle remains fairly constant in CCM, therefore $V = L \times \Delta I / \Delta t$. It can be seen that I (or I_{pp} in Figure 10) must remain constant for any load, including zero load current. At zero load, the average current through the inductor is zero, so the geometric center of the sawtooth waveform (the center being always equal to load current) is along the x-axis. At critical conduction (boundary between conventional CCM and what should have been DCM were it not in FPWM mode), the load current is equal to Ipp/2. Note that excessively low values of inductance will produce much higher current ripple and this will lead to higher circulating currents and power dissipation.

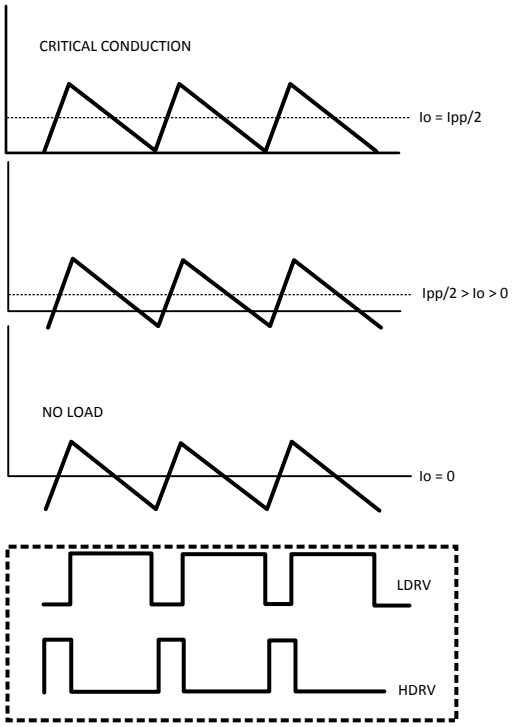
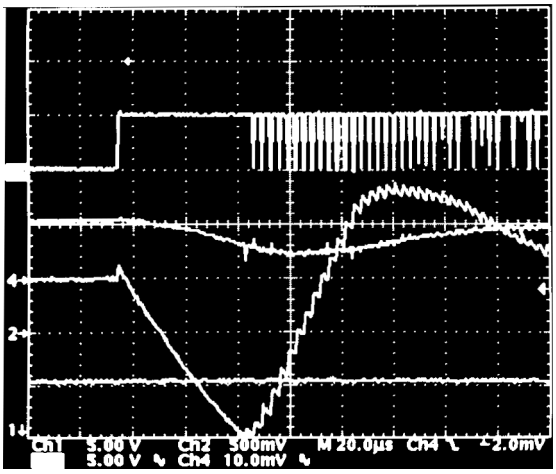


Figure 10. Inductor Current in FPWM Mode

STATE-TRANSITIONS AT LIGHT LOADS

A situation can occur if the converter transitions from SKIP mode to FPWM mode under a light load condition (converter is operating below the DCM boundary). This can occur after startup if FPWM mode is selected for use in a light load condition or if the FPWM pin is toggled high during normal operation at light load. The problem occurs because in SKIP mode the converter is operating at a set duty cycle and a lower average frequency. When the converter is forced into FPWM mode, this represents a change to the system. The pulse widths and frequencies need to re-adjust suddenly and in the process momentary imbalances can be created. Like the case of a pre-biased load, there can be negative surge current passing from drain to source of the lower FET. It must be kept in mind that though the LM27241 has current limiting for current passing in the 'positive' direction (i.e. passing from source to drain of the lower FET), there is no limit for reverse currents. The amount of reverse current when the FPWM pin is toggled 'on the fly' can be very high. This current is determined by several factors. One key factor is the output capacitance. Large output capacitances will lead to higher peak reverse currents. The reverse swing will be higher for lighter loads because of the bigger difference between the duty cycles/average frequency in the two modes. See Figure 11 for a plot of what happened in going from SKIP to FPWM mode at 0A load (worst case). The peak reverse current was as high as 3A, lasting about 0.1ms. The inductor could also saturate severely at this point if designed for light loads. In general, if the designer wants to toggle the FPWM pin while the converter is operating or if FPWM mode is required for a light load application, the low side FET and inductor should be closely evaluated under this specific condition. If the part is operated in FPWM mode with a light load the user will experience lower efficiency and negative current during the transition (as discussed). The user may also experience a momentary drop on Vout when the transition is made from SKIP to FPWM mode. This only occurs for no load or very light load conditions (above the DCM boundary there is no difference between SKIP FPWM modes).

In some cases, such as low Vout (< 1.5V), a glitch may be present on PGOOD. If this is problematic, the glitch may be eliminated by either operating in SKIP mode or using a small sized soft start capacitor. See the following section for selecting soft start capacitors .



CH1: PGOOD, CH2: Vo, CH3: LDRV, CH4: I_L (1A/div)
Output 1V @ 0A, VIN = 10V, L = 10µH, f = 300kHz

Figure 11. SKIP to FPWM 'On The Fly'

SOFT-START

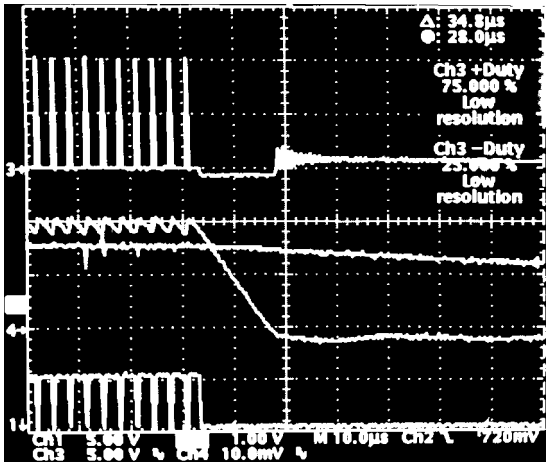
The maximum output voltage of the error amplifier is limited during start-up by the voltage on the 0.1µF capacitor connected between the SS pin and ground. When the controller is enabled (by taking EN pin high) the following steps may occur. First the SS capacitor is discharged (if it has a pre-charge) by a 1.8 kΩ internal resistor (R_{SS_DCHG}, see Electrical Characteristics table). This ensures that reset is obtained. Then a charging current source I_{SS_CHG} of 11µA is applied at this pin to bring up the voltage of the Soft-start capacitor voltage gradually. This causes the (maximum allowable) duty cycle to increase slowly, thereby limiting the charging current into the output capacitor and also ensuring that the inductor does not saturate. The Soft-start capacitor will eventually charge up close to the 5V input rail. When EN is pulled low the Soft-start capacitor is discharged by the same 1.8 kΩ internal resistor and the controller is shutdown. Now the sequence is allowed to repeat the next time EN is taken high.

The above Soft-start sequence is actually initiated not only whenever EN is taken high, but also under a normal power-up or during recovery from a fault condition (more on this later).

As mentioned in the section ‘Forced-PWM Mode and Pulse-skip Mode’ under startup, since the current is high until the output capacitors have charged up, there will be no observable difference in the shape of the ramp-up of the output rail in either SKIP mode or FPWM mode. The design has thus forced the startup waveforms to be identical irrespective of whether the FPWM mode or the SKIP mode has been selected.

SHUTDOWN/SOFT-SHUTDOWN

When the EN pin is driven low, the LM27241 initiates shutdown by turning OFF both upper and lower FETs completely (this occurs irrespective of FPWM or SKIP modes). See Figure 12 for a typical shutdown plot and note that the LDRV goes to zero (and stays there). Though not displayed, Power Good also goes low within less than 100ns of the EN pin going low (t_{SD}, see Electrical Characteristics table). Therefore in this case, the controller is NOT waiting for the output to actually fall out of the Power Good window before it signals Power Not Good. When the part is shutdown with a constant current load, the time taken for the output to decay may be calculated using the equation V/t = i/C. For example, there is a constant current 2A load applied at the output and the charge stored on the output capacitor continues to discharge into the load. From V/t = i/C = 2A/330µF, it can be seen that the output voltage (say 1V) will fall to zero in about 165µs.



CH1: LDRV, CH2: Vo, CH3: SW, CH4: I_L (1A/div)
Output 1V @ 2A, VIN = 10V, FPWM/SKIP, L = 10µH, f = 300kHz, C_{OUT} = 330µF

Figure 12. Shutdown

POWER GOOD/NOT GOOD SIGNALING

PGOOD is an open-drain output pin with an external pull-up resistor connected to 5V. It goes high (non-conducting) when the output is within the regulation band as determined by the Power Good window detector stage on the feedback pin (see Block Diagram). PGOOD goes low (conducting) when the output falls out of this window. This signal is referred to as Power Not Good here. A glitch filter of 7µs filters out noise, and helps to prevent spurious PGOOD responses. So Power Not Good is not asserted until 7µs after the output has fallen out of the Power Good window (see Δt_{PG_NOK} in Electrical Characteristics table). With the feedback pin voltage rising towards regulation value, there is a 20µs delay between the output being in regulation and the signaling of Power Good (see Δt_{PG_OK} in Electrical Characteristics table). Power Not Good is signaled within 100ns of the Enable pin being pulled low (see Δt_{SD} in Electrical Characteristics table), irrespective of the fact that the output could still be in regulation. The Soft-start capacitor is also then discharged as explained earlier.

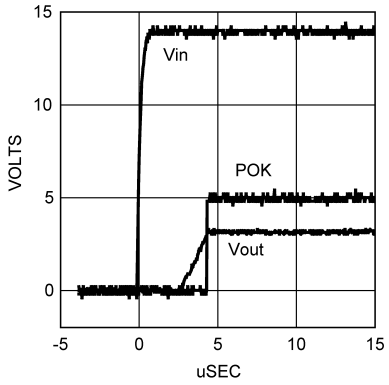


Figure 13. Startup Power OK

FAULT AND RECOVERY

If the output falls outside the Power Good window, the response is a 'Power Not Good' signal. The FET drive signals are not affected. But under a fault condition assertion, LDRV goes high immediately turning the low-side FET ON and discharging the output capacitors. The inductor current will then invariably slew momentarily negative (passing from drain to source of low-side FET), before it settles down to zero. A fault will be detected when the output falls below the Under-voltage threshold, or rises above the Over-voltage threshold. From its detection to assertion, there is a 7µs delay to help to prevent spurious responses. A fault condition is also asserted during a loss of the VIN rail or the VDD rail. If the Enable pin is brought low prior to this fault, a soft shutdown will occur. To recover from a fault, either of the following options is available:

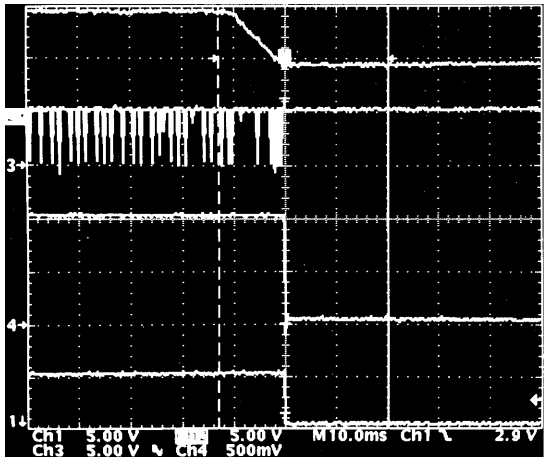
1) Enable pin is toggled: i.e. taken low (below 0.8V), then high again (2V to 5V). This must be done with VDD between 4.5V to 5V and VIN within normal range (5.5V to 28V).

2) VDD is brought below 1.0V and then brought back up between 4.5V to 5V. This must be done with the Enable pin held high (2V to 5V) and VIN within normal range (5.5V to 28V).

Recovery will initiate a Soft-start sequence (see description under section 'Soft-start' above).

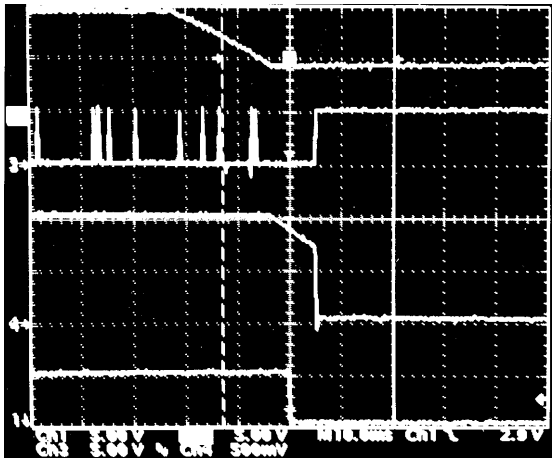
VIN POWER-OFF (UVLO)

The LM27241 has an internal comparator that monitors VIN. If VIN falls to approximately 4.4V, switching ceases and both top and bottom FETs are turned OFF. 'Power Not Good' has meanwhile already been signaled and a fault condition asserted shortly thereafter.



CH1: PGOOD, CH2: VIN, CH3: LDRV, CH4: Vo
Output 1V @ 0.02A, VIN = 9.75V, FPWM, L = 10µH, f = 300kHz, C_{OUT} = 660µF

Figure 14. VIN Removal in FPWM Mode



CH1: PGOOD, CH2: VIN, CH3: LDRV, CH4: Vo
Output 1V @ 0.02A, VIN = 9.75V, SKIP, L = 10µH, f = 300kHz, C_{OUT} = 660µF

Figure 15. VIN Removal in SKIP Mode

The recovery procedure from a VIN Power-off is the same as for any fault condition.

VDD POWER-OFF (UVLO)

Whenever VDD starts to fall, and drops below about 3.5V, LDRV goes high immediately, 'Power Not Good' is signaled and in effect a fault condition (in this case an Under-voltage lockout) is asserted. Recovery from a fault is discussed in the "Fault and Recovery" section.

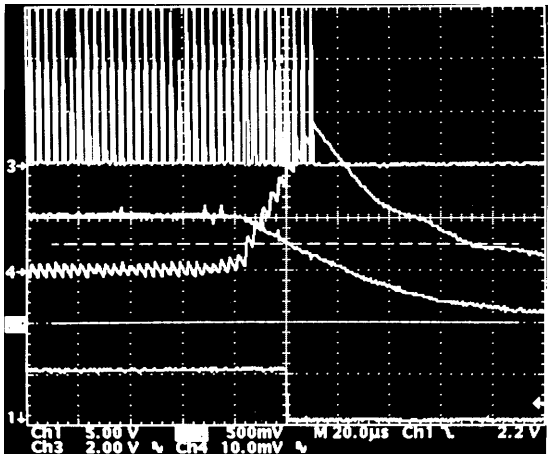
OVER-VOLTAGE PROTECTION

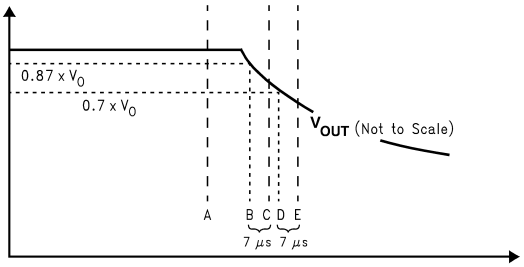
If the voltage on the FB pin exceeds 113% of 0.60V, a Power Not Good signal is asserted. If the voltage on the FB pin exceeds 130% of 0.60V, a fault condition is declared, and the LDRV goes high. If the fault persists, the low-side FET will stay on and the high-side FET will not turn back on until the FB pin falls within the power good window, and the Enable pin is toggled.

CURRENT LIMIT AND PROTECTION

Output current limiting is achieved by sensing the negative Vds drop across the low-side FET when the FET is turned ON. The Current Limit Comparator (see Block Diagram) monitors the voltage at the ILIM pin with 62µA (typical value) of current being sourced from the pin. The 62µA source flows through an external resistor connected between ILIM and the drain of the low-side FET. The voltage drop across the ILIM resistor is compared with the drop across the low-side FET and the current limit comparator trips when the two are of the same magnitude. This determines the threshold of current limiting. For example, if excessive inductor current causes the voltage across the low-side FET to exceed the voltage drop across the ILIM resistor, the ILIM pin will go negative (with respect to ground) and trip the comparator. The comparator then sets a latch that prevents the high-side FET from turning ON during the next PWM clock cycle. The high-side FET will resume switching only if the current limit comparator was not tripped in the previous switching cycle. Additionally, the Soft-start capacitor at the SS pin is discharged with a 115µA current source when an overcurrent event is in progress. The purpose of discharging the Softstart capacitor during an overcurrent event is to eventually allow the voltage on the SS pin to fall low enough to cause additional duty cycle limiting.

$$R_{LIMIT} = (R_{DS\_ON} \times I_{LIMIT} / 62\ \mu A) \quad (1)$$

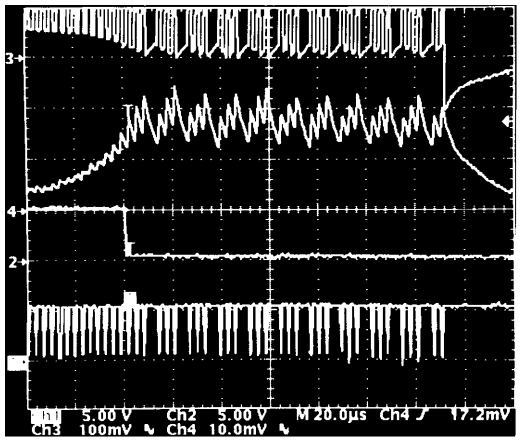


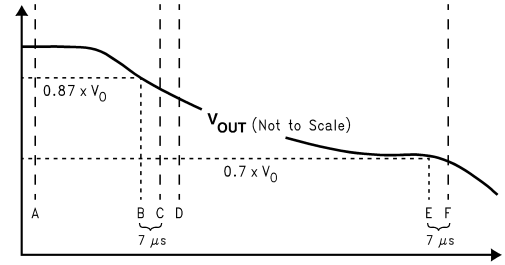


	Description	Comments
A	Short applied on Output	Inductor current starts to ramp up
B	Power Not Good detected	Output falls to 87% set voltage
C	Power Not Good asserted	'Soft-shutdown' initiated
D	Output UV detected	Output falls to 70% set voltage
E	Fault asserted	LDRV latches high. HDRV latches low.

CH1: PGOOD, CH2: Vo, CH3: ILIM Pin, CH4: I_L (1A/div)
Output 1V, 0.04A to Overload, VIN = 10V, FPWM, L = 10µH, f = 300kHz, RLIM = 1k

Figure 16. Response to Severe Overload (Type A: fault threshold first)





	Description	Comments
A	Short applied on Output	Inductor current starts to ramp up
B	Power Not Good detected	Output falls to 87% set voltage
C	Power Not Good asserted	'Soft-shutdown' initiated
D	Current Limit reached	ON-pulses may now get skipped
E	Output UV detected	Output falls to 70% set voltage
F	Fault asserted	LDRV latches high. HDRV latches low.

CH1: LDRV, CH2: PGOOD, CH3: ILIM Pin, CH4: I_L (5A/div)
Output 1V, 2A to Overload, VIN = 10V, L = 10µH, f = 300kHz, RLIM = 2k

Figure 17. Response to Severe Overload (Type B: current limit threshold first)

Application Information

CURRENT LIMIT RESISTOR

The timing scheme implemented in the LM27241 makes it possible for the IC to continue monitoring an over current condition and to respond appropriately every cycle. This is explained as follows.

Consider the LM27241 working under normal conditions, just before an overload occurs. After the end of a given ON-pulse (say 'ton1'), the LM27241 starts sampling the current in the low-side FET. This is the OFF-duration called 'toff1' in this analysis. Therefore, if an over-current condition is detected during this OFF-duration 'toff1', the controller will decide to omit the next ON-pulse (which would have occurred during the duration 'ton2'). This is done by setting an internal 'over-current latch' which will keep HDRV low. The LDRV will now not only stay high during the present OFF-duration ('toff1') but during the duration of the next (omitted) ON-pulse ('ton2'), and then as expected also during the succeeding OFF-duration ('toff2'). But the 'over-current latch' is reset at the very start of the next OFF-duration 'toff2'. Therefore if the over-current condition persists, it can be recognized during 'toff2' and a decision to skip the next ON-pulse (duration 'ton3') can be taken. Finally, several ON-pulses may get skipped until the current in the low-side FET falls below the current limit threshold.

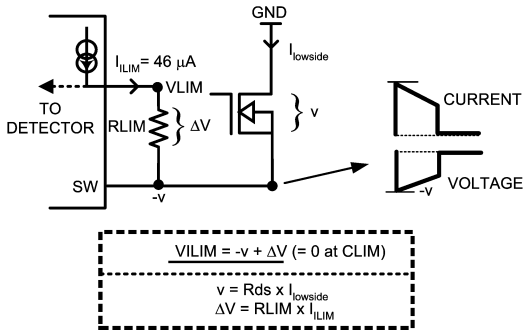


Figure 18. Understanding Current Sensing

For this analysis, the nominal value of current sourced ILIM, (see Electrical Characteristics table) and the R_{DS_ON} of the low-side FET at 100°C should be used. This will ensure adequate headroom without the need for excessively large components. From the MOSFET data sheet typical R_{DS_ON} at 25°C is given to be 3.7mΩ. This value is not to be used in the current limit calculation. The maximum FET R_{DS_ON} at room temperature is 4.8mΩ. During normal circuit operation, the FET temperature will rise to a temperature greater than 25°C. Therefore R_{DS_ON} at 100°C is obtained. From the datasheet, at 100°C the R_{DS_ON} goes up typically 1.3 times its 25°C value. Therefore, the R_{DS_ON} to be used in the actual current limit calculation is:

$$R_{DS\_ON} = 1.3 \times 4.8\ m\Omega = 6.42\ m\Omega \quad (2)$$

Using I_{ILIM} = 62µA and a value of 6.42mΩ for maximum R_{DS_ON} will provide the lowest possible value of current limit considering tolerances and temperature (for a given R_{LIM} resistor). In order to allow for output load transients, it is a good design practice to add margin to this calculation.

At the point where current limiting occurs (peak inductor current becomes equal to current limit) the resistor for setting the current limit can be calculated. The (peak) current limit value depends on two factors:

1) The peak current in the inductor with the converter delivering maximum rated load. This should be calculated at VIN_{MAX}

2) The 'overload margin' (above maximum load) that needs to be maintained. This will depend on the step loads likely to be seen in the application and the response expected. The peak inductor current under normal operation (maximum load) depends on the load and the inductance. It is given by:

$$I_{PEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (3)$$

where I_{RIPPLE} was determined in the output filter section.

Example: Let I_{RIPPLE} be 2A. The peak current under normal operation is

$$I_{PEAK} = 10A + \frac{2A}{2} = 11A \quad (4)$$

Usually it is necessary to set the current limit about 20% higher than the peak inductor current. This overload margin helps handle sudden load changes. A 20% margin will require a current limit of 11A x 1.2 = 13.2A.

$$R_{ILIMIT} = \frac{6.42\ m\Omega \times 11A \times 1.2}{62\ \mu A} = 1.37\ k\Omega \quad (5)$$

A standard value of 1.37kΩ may be chosen.

A larger overload margin greater than 20% (say 40%) would help in obtaining good dynamic response. This is necessary if the load steps from an extremely low value (say zero) up to maximum load current. A larger current limit will, however, generate stresses in the FETs during abnormal load condition (such as a shorted output).

$$R_{ILIMIT} = \frac{6.42\ m\Omega \times 11A \times 1.4}{62\ \mu A} = 1.59\ k\Omega \quad (6)$$

A standard value of 1.58kΩ may be chosen.

Summarizing, for a 1.2V/10A rated output, using a 1.9µH inductor and any low side equivalent FET (same R_{DS_ON} as IRF7832).

- For 20% overload margin, select current limit resistor to be 1.37kΩ
- For 40% overload margin, select current limit resistor to be 1.58kΩ

INDUCTOR AND OUTPUT CAPACITOR

The designer is again referred to AN-1197 (SNVA038) for the equations required here. The design table in the referenced Application Note uses V_D as the drop across the diode in an asynchronous configuration. Also, V_{SW} is the drop across the switch (high-side FET). In the case of the LM27241 a reasonable approximation is to set V_D = V_{SW} = 0 in the design table available in AN-1197. Then the table can be used easily for selection of the inductor and output capacitor. A step by step example is also provided for a general buck regulator in the Application Note AN-1207 (SNOA406).

Only in the case of the input capacitor, the situation may be different as is explained next.

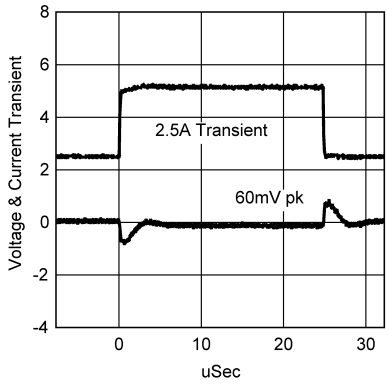


Figure 19. Evaluation Board Transient Response
V_{OUT} = 1.50VDC, V_{IN} = 14V
Iout step = 2.5A to 5A, and 5A to 2.5A Load Step.

INPUT CAPACITOR

In a buck regulator, the input capacitor provides most of the pulsed current waveform demanded by the switch. However the DC (average) value of the current through a capacitor in steady state must be zero. Otherwise, the capacitor would start accumulating charge every cycle, and that would clearly not represent a 'steady state' by definition.

The equation for the RMS current through the input capacitor is then

$$I_{IN} = Io\sqrt{D(1-D)} \quad (7)$$

The function D(1-D) has a maxima at D = 0.5. This would correspond to an input voltage of 5V/0.5 = 10V. And the input capacitor current at this worst case input voltage would be

$$I_{IN} = 3\sqrt{0.5\ (1-0.5)} = 3 \times 0.5 = 1.5A \quad (8)$$

The input capacitors must be positioned physically close to the power stage.

MOSFETs

Selection of FETs for the controller must be done carefully taking into account efficiency, thermal dissipation and drive requirements. Typically the component selection is made according to the most efficient FET for a given price.

When looking for a FET, it is often helpful to compose a spreadsheet of key parameters. These parameters may be summarized as ON resistance (R_{DS_ON}), gate charge (Q_{GS}), rise and fall times (t_r and t_f). The power dissipated in a given device may then be calculated according to the following equations:

High-side FET:

$P = P_C + P_{GC} + P_{SW}$

Where

$P_C = D \times (I_{OUT}^2 \times R_{DS\_ON})$

$P_{GC} = 5V \times Q_{GS} \times f$

$P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f$

Low-side FET:

$P = P_C + P_{GC}$

Where

$P_C = (1 - D) \times (I_{OUT}^2 \times R_{DS\_ON})$

$P_{GC} = 5V \times Q_{GS} \times f$

One will note that the gate charge requirements should be low to ensure good efficiency. However, if a FET's gate charge requirement is too low (less than 8nC), the FET can turn on spuriously. A good starting point for a 10A load is to use a high-side and low-side FET each with an on resistance of 5mΩ (FET on resistance is a function of temperature, therefore it is advisable to apply the appropriate correction factor provided in the FET datasheet), gate to source charge of 8nC (total gate charge of 36 nC), t_r = 11ns, t_f = 47ns, and temperature coefficient of 1.4. For a 5V input and 1.2V/10A output (f = 300kHz), this yields a power dissipation of 0.62 W (high-side FET) and 0.54 W (low-side FET). The efficiency is then 91%. While the same FET may be used for both the high side and low side, optimal performance may not be realized.

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LS\_FET} + P_{HS\_FET} + V_{IN} \times I_Q} \quad (9)$$

FREQUENCY SET RESISTOR (TYPICAL VALUE)

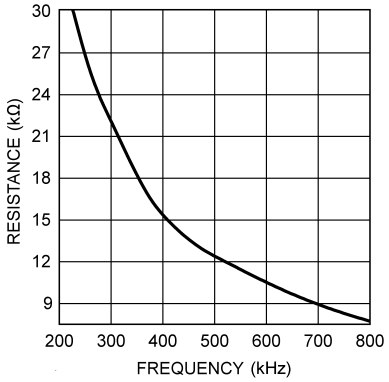


Figure 20. Frequency Adjust Resistor Guideline

R_{FREQ} (Ω)	Frequency (kHz)
30100	226
25500	261
22100	300
16200	388
15000	411
12700	485
12400	510
10000	630
8660	720
7500	820

LAYOUT GUIDELINES

For a deeper understanding of Buck converters and the 'critical traces' please see Application Note AN-1229 (SNVA054).

Figure 21 is based on such an understanding of the critical sections and also the pin functions of the LM27241. Refer to the Typical Applications circuit and the LM27241 TSSOP pinouts to understand the layout suggestions more thoroughly.

The components shown in Figure 21 are most critical and must be placed with the following guidelines.

There are three separate Ground shapes on the top layer, and one ground plane that is either on the bottom layer, or on an internal layer. The ground shapes are connected to the ground plane through vias.

Input Capacitor Ground Shape: This ground shape connects the input capacitors and the source of the synchronous MOSFET (Q2). This ground shape contains high Δi/Δt current waveforms. Therefore effort should be taken to keep sensitive ground connections away from this ground shape. The input capacitors should be placed as close as possible to the MOSFET, and the vias to the ground plane should be as close to the capacitors ground pad as possible. Ensure that this ground plane shape is not directly connected to the Output Capacitors Ground Shape. Note that the current limit detector circuit compares the voltage on the ILIM pin with respect to the PGND pin. Therefore, if the power ground is noisy it can lead to erroneous triggering of the current limit detector. This will manifest itself as an inability to meet the load requirement despite over sizing the current limit resistor. It can also lead to failure of the output to recover after encountering an overload condition. Connect the LM27241 PGND pin to this shape, and place two vias from the pin pad to the ground plane.

Output Capacitor Ground Shape: The Output Capacitor Ground Shape should be large as possible. Place the vias that connect this shape to the ground plane as close to the capacitor pads as possible.

SGND Ground Shape: A small ground shape should be created so that all noise sensitive components such as the lower feedback resistor, V_{DD} supply capacitor, frequency adjust resistor and SKIP/FPWM Mode select resistor can be connected to. Two to three vias should connect this ground shape to the ground plane. Place all the components mentioned as close as possible to the controller. Route the feedback resistors from Vout to the controller as far away from the MOSFETs and SW-node as possible.

SW-Node Shape: This shape connects the top MOSFET source to the synchronous MOSFET drain, and then connects to the output inductor. This shape should be kept small due to the high frequency content found at this node. Enough copper area must be left around the MOSFET for thermal dissipation. More details on this are also provided in AN-1229.

HDRV & LDRV connections: Try to keep the trace lengths from the controller to the gate of the MOSFET as short as possible. Both these traces contain fast rise and fall times, and low inductance trace lengths should be maintained.

C_{V5} & C_{VDD} Capacitors: These two capacitors should be placed very close to the controller and their respective pins for best performance.

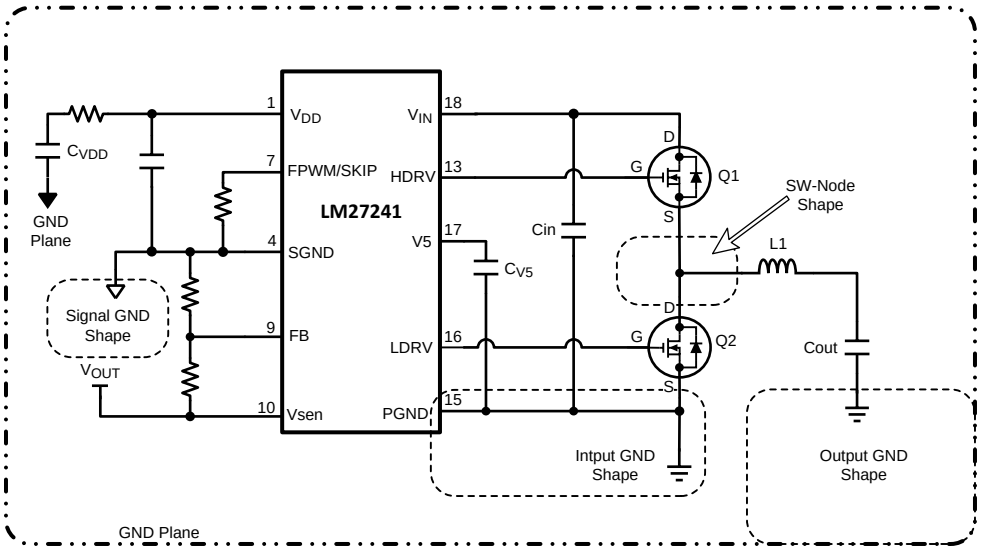
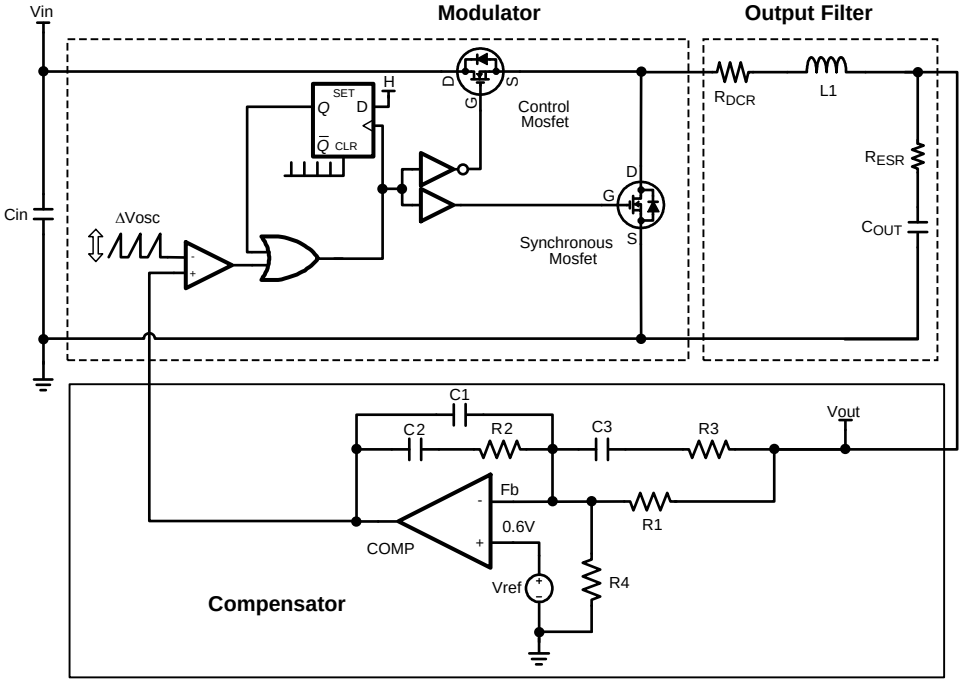


Figure 21. Critical Component placement (TSSOP)

COMPENSATION



Modulator Gain

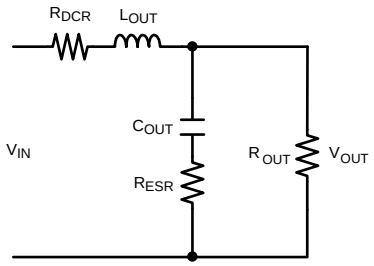
The LM27241 input voltage feed forward mechanism changes the Error Amp ramp slope, and peak to peak voltage. The DC gain of the Modulator is dependent on the peak to peak voltage of the oscillator's ramp. The oscillator peak to peak voltage can be determined by referring back to the Oscillator section in the Electrical Characteristics table.

$$MOD_{DC\text{-}Gain} = \frac{V_{IN}}{\Delta V_{OSC}} \tag{10}$$

This ratio for the above equation is usually between 9.5 for lower input voltages and as low as 8 higher input voltages.

The DC Gain of the power stage for a Buck-Converter is equal to V_{OUT}/D, which is equal to V_{IN}, and this is where the term in the numerator in the above equation is obtained.

Output Filter Gain



Exact Filter Gain

$$Filter_{AC\text{-}Gain} = \frac{R_O \times (1 + s \times R_{ESR} \times C_O)}{(R_{DCR} + R_O) + s(C_O \times R_{ESR} \times R_O + L_O) + s^2 L_O \times C_O(R_O + R_{ESR})}$$

Reduces to proper form with the understanding that:

$$\frac{L_{OUT}}{R_O} >> C \times R_{ESR}, 1 >> \frac{R_{DCR}}{R_O} \;\&\; 1 >> \frac{R_{ESR}}{R_O} \tag{11}$$

$$\text{Output - Filter}_{AC\text{-}Gain} = \frac{1 + s \times R_{ESR} \times C_{OUT}}{1 + s\left(\frac{L_{OUT}}{R_O}\right) + s^2 L_{OUT} \times C_{OUT}} \tag{12}$$

$$GAIN_{SYSTEM} = \left((G_{CM}) \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right) \times \left(1 + \frac{s}{\omega_{Z2}}\right)}{S_0 \times \left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right)} \right) \times \frac{1 + s \times R_{ESR} \times C_{OUT}}{1 + s(R_{ESR} + R_{LDCR}) \times C_{OUT} + s^2 L \times C_{OUT}} \times \frac{V_{IN}}{\Delta V_{OSC}} \tag{13}$$

Zero Frequency due to R_{ESR}:

$$F_Z = \frac{1}{2\pi(R_{ESR} \times C_{OUT})} \tag{14}$$

Complex Poles due to output inductor and output capacitors:

$$F_P = \frac{1}{2\pi\sqrt{(L_{OUT} \times C_{OUT})}} \tag{15}$$

Type III Compensator (PID)

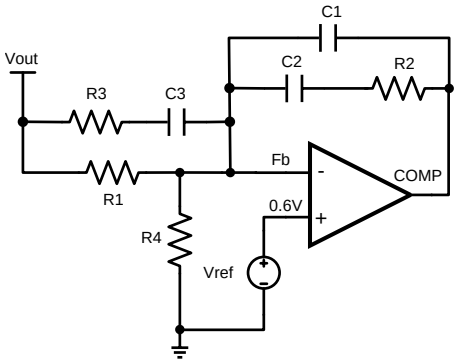


Figure 22. Type III Compensator (PID)

$$G_{COMP\text{-}III} = (G_{CM}) \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right) \times \left(1 + \frac{s}{\omega_{Z2}}\right)}{S_0 \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \tag{16}$$

Type III Compensator Transfer Function

The Type III compensation is needed in designs where output ceramic capacitors are used, and therefore is very small. The Zero frequency, due to R_{ESR}, is usually much larger than the crossover frequency when ceramic capacitors are used. Rule of thumb is if $F_{ZERO} > F_{BW}$ use type III compensation.

ω_{Z1} and ω_{Z2}: +20dB/DEC and +45DEG/DEC phase.

ω_{Z2}: Adds phase lead in the vicinity of the crossover frequency.

ω_{PZ1} and ω_{P2}: -20dB/DEC and -45DEG/DEC phase.

Must be present to in the compensation to ensure the gain rolls off at high frequency and prevent switching ripple from disrupting the regulation of the converter.

The Loop Bandwidth (F_{BW}) or known as the crossover frequency (F_{CROSS}) is usually set by the designer, with the basic guideline:

$$F_{SW}/10 \le F_{BW} \le F_{SW}/5 \quad (17)$$

COMPENSATION DESIGN STEPS

Output Filter:

1) Choose crossover frequency

2) Determine complex pole frequency due to output filter:

$$F_{P\text{-}COMPLEX} = \frac{1}{2\pi\sqrt{(L_{OUT} \times C_{OUT})}} \quad (18)$$

3) Determine zero frequency due to R_{ESR}

$$F_{ESR\text{-}ZERO} = \frac{1}{2\pi(R_{ESR} \times C_{OUT})} \quad (19)$$

Type III Compensator:

1) Frequency at which maximum phase boost occurs is at the average between the frequency of F_{P2} and F_{Z2}

$$Freq_{\phi\text{-}max} = \sqrt{F_{P2} \times F_{Z2}} \quad (20)$$

Place this at the Crossover frequency:

$$Freq_{\phi\text{-}max} = \sqrt{F_{P2} \times F_{Z2}} = F_{BW} \quad (21)$$

$$\frac{F_{P2}}{F_{Z2}} = \frac{1 - \sin(\phi)}{1 + \sin(\phi)} \quad (22)$$

where $60° \ge \Phi_{MAX} \ge 45°$

$$F_{Z2} = F_{BW} \times \sqrt{\frac{1 - \sin(\phi)_{MAX}}{1 + \sin(\phi)_{MAX}}} \quad (23)$$

$$F_{P2} = F_{BW} \times \sqrt{\frac{1 + \sin(\phi)_{MAX}}{1 - \sin(\phi)_{MAX}}} \quad (24)$$

$$F_{Z1} = \frac{1}{2} F_{Z2} \quad (25)$$

$$F_{Z1} < F_{Z2} \text{ and } F_{Z1} < F_{P\text{-}COMPLEX} \quad (26)$$

$$F_{P3} = \frac{1}{2} F_{SW} \quad (27)$$

DESIGN EXAMPLE

V_{IN} = 15V

V_{OUT} = 1.5V

F_{BW} = 300kHz

BW = = 30kHz

L_{OUT} = 2.2µH

L_{OUT} = 2x100µF Tantalum + 2x47µF Ceramic

R_{ESR} Tantalum = 100mΩ

R_{ESR} Ceramic = 15mΩ

C_{OUT} total = 294µF

R_{ESR} total = 13mΩ

$$F_{P\text{-}COMPLEX} = \frac{1}{2\pi\sqrt{(L_{OUT} \times C_{OUT})}} = 6.26\ kHz \quad (28)$$

$$F_{ESR\text{-}ZERO} = \frac{1}{2\pi(R_{ESR} \times C_{OUT})} = 42\ kHz \quad (29)$$

Notice that F-zero due to the R_{ESR} is greater than the cross-over frequency (F_{SW}). TYPE III Compensation is required.

$$F_{Z2} = F_{BW} \times \sqrt{\frac{1 - Sin(\phi)_{MAX}}{1 + Sin(\phi)_{MAX}}} = 12\ kHz \quad (30)$$

$$F_{P2} = F_{BW} \times \sqrt{\frac{1 + Sin(\phi)_{MAX}}{1 - Sin(\phi)_{MAX}}} = 72\ kHz \quad (31)$$

Φ_{MAX} 45°

$$F_{Z1} = \frac{1}{2} F_{Z2} = 6\ kHz$$

$$F_{P3} = \frac{1}{2} F_{SW} = 150\ kHz$$

$$F_{Z1} = \frac{1}{2\pi(R_2 \times C_2)} = 6\ kHz \quad (32)$$

Pick C_2 to be 4700pF, and calculate R_2. C_2 = 4700 pF, & R_2= 5.6 kΩ

$$F_{P3} = \frac{1}{2\pi\left(\frac{C_1 \times C_2}{C_1 + C_2}\right) \times R_2} = 150\ kHz \quad (33)$$

C_1 = 190p F (use 220pF).

C_3 sets F_{BW}:

$$F_{P2} = F_{BW} \times \sqrt{\frac{1 + Sin(\phi)_{MAX}}{1 - Sin(\phi)_{MAX}}} = 72\ kHz \quad (34)$$

$$F_{P2} = \frac{1}{2\pi(R_3 \times C_3)} \quad (35)$$

R_3 = 1kΩ

$$F_{Z2} = F_{BW} \times \sqrt{\frac{1 - Sin(\phi)_{MAX}}{1 + Sin(\phi)_{MAX}}} = 12\ kHz \quad (36)$$

$$F_{Z2} = \frac{1}{2\pi \times C_3(R_3 + R_1)} \quad (37)$$

R_1 = 5kΩ

Set output voltage:

$$V_{OUT} = \left(\frac{0.60V \times (R_1 + R_4)}{R_4}\right) \quad (38)$$

$$R_4 = \left(\frac{0.6 \times R_1}{V_{OUT} - 0.6V}\right) \quad (39)$$

R_4 = 3.32kΩ

EVALUATION BOARD DETAILS

The Bill of Materials (BOM) is now provided for the LM27241 evaluation board. The schematic is the typical application circuit. See *Layout Guidelines* for more guidance on preferred layout practices and also refer to Application Note AN-1229. Note that a dual FET pack has been chosen for the evaluation board.

The evaluation board has its output set to 1.5V. The rated load 6A continuous, and 7A peak. A minimum load of 0.1mA should be maintained on each output in SKIP mode, to ensure regulation.

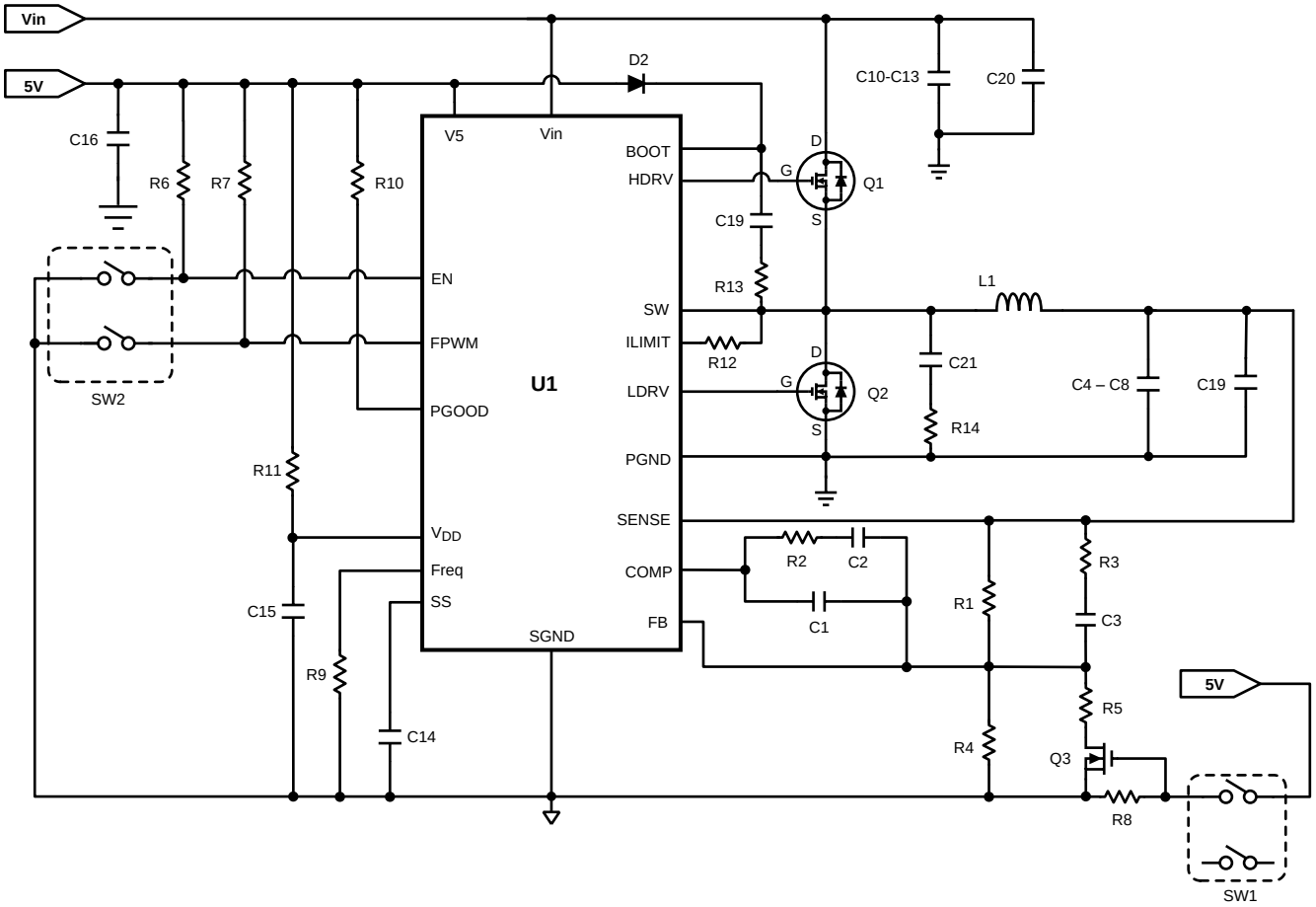


Figure 23. Typical Application (Expanded View)

Bill of Materials

Designator	Function	Description	Vendor
U1	Synchronous Buck Controller	PWM Controller	NSC
R1	Feedback Resistor	4.99 kΩ 1% 0805	VISHAY
R2	Compensation Resistor	5.62 kΩ 1% 0805	VISHAY
R3	Compensation Resistor	1.00 kΩ 1% 0805	VISHAY
R4	Feedback Resistor	3.32 kΩ 1% 0805	VISHAY
R5	Dynamic Feedback Resistor	40.2 kΩ 1% 0805 (Optional)	VISHAY
R6	Enable pull up resistor	12.7 kΩ 1% 0805	VISHAY
R7	FPWM pull up resistor	12.7 kΩ 1% 0805	VISHAY
R8	Q3 Gate to GND resistor	10 kΩ 1% 0805 (Optional)	VISHAY
R9	Freq Set Resistor	22.1 kΩ 1% 0805	VISHAY
R10	PGOOD pull up resistor	12.7 kΩ 1% 0805	VISHAY
R11	VDD filter resistor	10Ω 1% 0805	VISHAY
R12	Ilimit Resistor	1.33 kΩ 1% 0805	VISHAY
R13	Resistor (Optional)	0Ω	VISHAY
R14	Snubber Resistor (Optional)	10Ω 5% 0805	VISHAY

Designator	Function	Description	Vendor
C1	Compensation Capacitor	220 pF 0805	TDK
C2	Compensation Capacitor	4700 pF 0805	TDK
C3	Compensation Capacitor	2200 pF 0805	TDK
C4, C6, C8, C17	Ceramic Output Capacitor	47 µF 2220 6.3V	TDK
C5, C8	Tantalum Output Capacitor	100 µF 4V B45192	EPCOS
C10 - C13	Ceramic/Tantalum Input Capacitors		TDK/EPCOS
C14	Soft Start Capacitor	0.1 µF 0805	TDK
C15, C16	VDD Filter Capacitor	0.22 µF 0805	TDK
C19	VBOOST Capacitor	0.1 µF 0805	TDK
C20	Ceramic Input Capacitor	10 µF	TDK
C21	Snubber Capacitor (Optional)	470 pF	TDK
D2	VBOOST Diode	BAT54 SOT23	Diodes INC
L1	Output Inductor	HC1216	Falco Electronics
Q1	Top MOSFET	IRF7821	International Rectifier
Q2	Synchronous MOSFET	IRF7832	International Rectifier
Q3	Small Signal FET VDYNAMIC	BSS138 SOT23	ON Semi
SW1	V-enable & FPWM/SKIP Set		
SW2	Vdynamic Set		

PCB Layout Diagrams

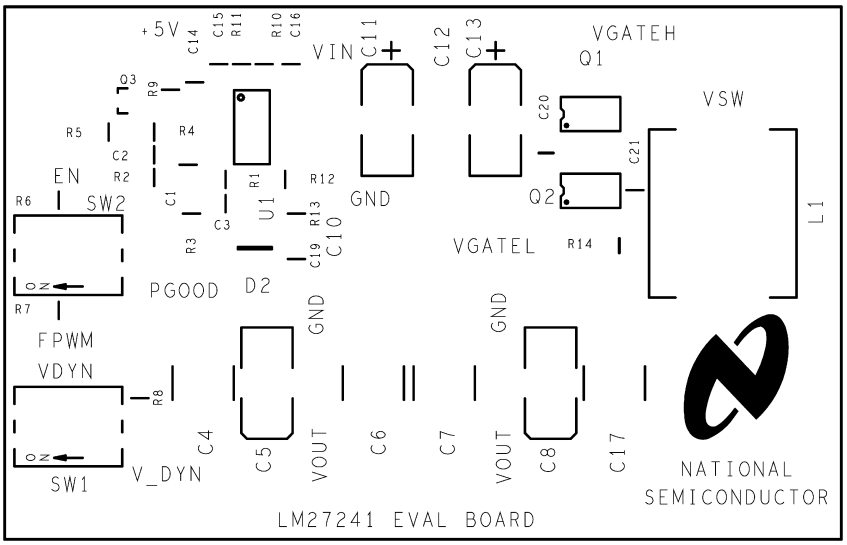


Figure 24. Top Overlay

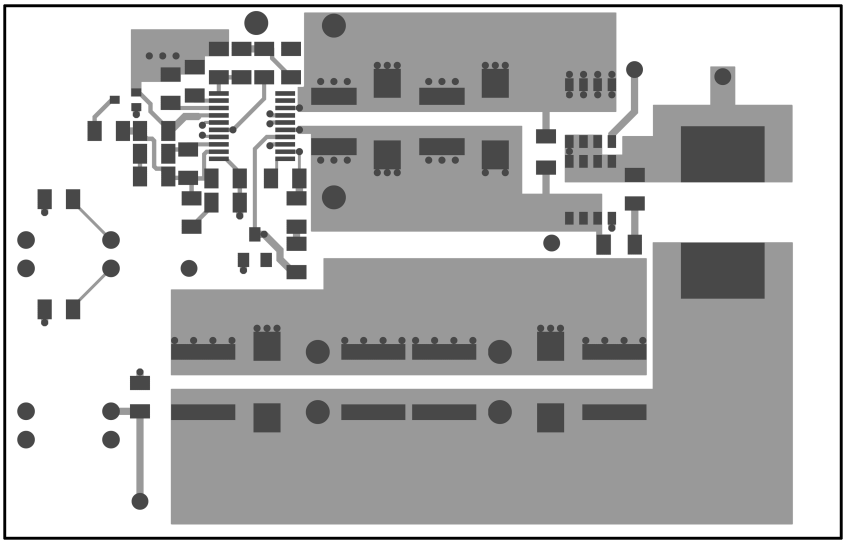


Figure 25. Top Layer

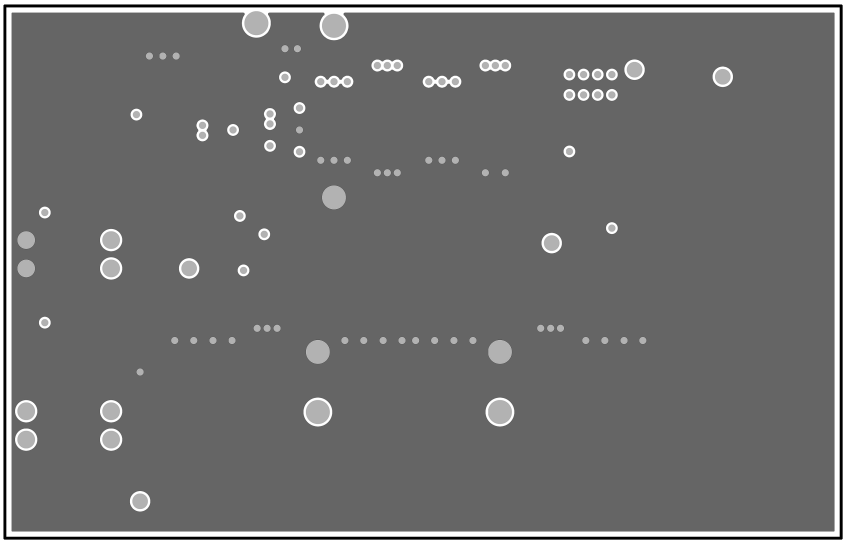


Figure 26. Internal Plane 1 (GND)

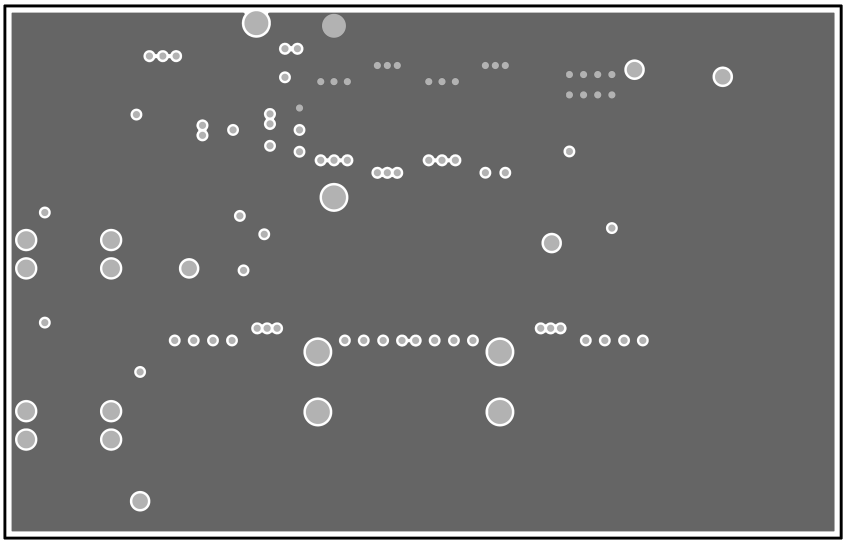


Figure 27. Internal Plane 2

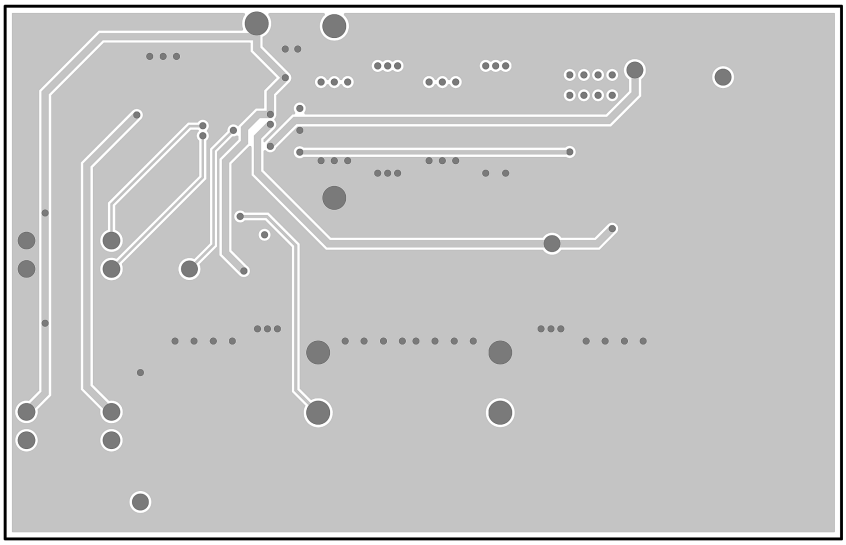


Figure 28. Bottom Layer

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