LP38513-1.8 3A Fast Response Ultra Low Dropout Linear Regulator

Check for Samples: LP38513

FEATURES

- **Conversions from 2.5V Rail to 1.8V**
- **Stable with Ceramic Capacitors**
- **Low Ground Pin Current**
- **Load Regulation of 0.1% for 10 mA to 3A Load Current**
- **60 µA Typical Quiescent Current in Shutdown Mode**
- **Specified Output Current of 3A**
- **Available in 5-Lead TO-220 and DDPAK/TO-263 Packages**
- **Specified V_{OUT} Accuracy of ±2.6% with T_J from 0°C to +125°C**
- **$\overline{\text{ERROR}}$ Flag Indicates V_{OUT} Status**
- **Over-Temperature and Over-Current Protection**
- **−40°C to +125°C Operating T_J Range**

APPLICATIONS

- **Microprocessor Power Supplies**
- **GTL, GTL+, BTL, and SSTL Bus Terminators**
- **Power Supplies for DSPs**
- **SCSI Terminator**
- **Post Regulators**
- **Battery Chargers**
- **Other Battery Powered Applications**

DESCRIPTION

The LP38513 fast response ultra low dropout linear regulator operates from a +2.25V to +5.50V input supply. This ultra low dropout linear regulator responds very quickly to step changes in line or load conditions, which makes it suitable for low voltage microprocessor applications. Developed on a CMOS process, with a PMOS pass transistor, the LP38513 has low quiescent current operation that is independent of the output load current.

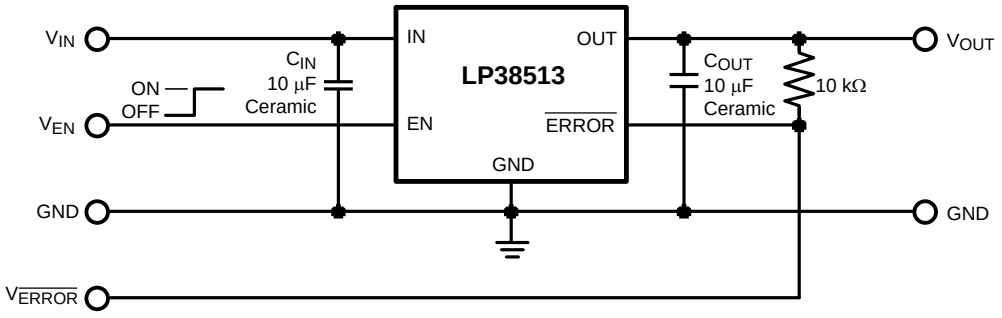
Ground Pin Current: Typically 12 mA at 3A load current.

Disable Mode: Typically 60 µA quiescent current when the Enable pin is pulled low.

$\overline{\text{ERROR}}$ Flag: The $\overline{\text{ERROR}}$ Flag goes low if V_{OUT} falls more than typically 15% below the nominal value.

Precision Output Voltage: A specified V_{OUT} accuracy of ±2.6% with T_J from 0°C to 125°C.

Typical Application Circuit



Connection Diagrams

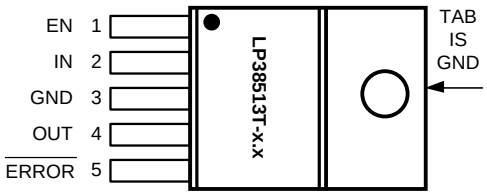


Figure 1. 5-Lead TO-220, Top View
See NDH005D Package

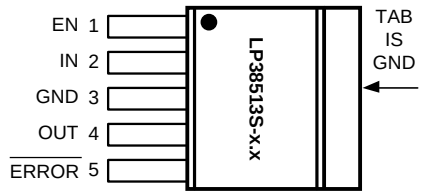


Figure 2. 5-Lead DDPAK/TO-263, Top View
See KTT0005B Package

Pin Descriptions for TO-220 and DDPAK/TO-263 5-Pin Packages

Pin #	TO-220 and DDPAK/TO-263	Function
1	EN	Enable. Pull high to enable the output, low to disable the output. This pin has no internal bias and must be tied to the input voltage, or actively driven.
2	IN	Input Supply Pin
3	GND	Ground
4	OUT	Regulated Output Voltage Pin
5	$\overline{\text{ERROR}}$	$\overline{\text{ERROR}}$ Flag. A high level indicates that V_{OUT} is within (tbd)% of the nominal regulated voltage.
TAB	TAB	The TO-220 and DDPAK/TO-263 TAB is used as a thermal connection to remove heat from the device to an external heatsink. The TAB is internally connected to device pin 3.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Storage Temperature Range		−65°C to +150°C
Soldering Temperature[3]	TO-220, Wave	260°C, 10s
	DPAK/TO-263	235°C, 30s
ESD Rating[4]		±2 kV
Power Dissipation[5]		Internally Limited
Input Pin Voltage (Survival)		−0.3V to +6.0V
Enable Pin Voltage (Survival)		−0.3V to +6.0V
Output Pin Voltage (Survival)		−0.3V to +6.0V
$\overline{\text{ERROR}}$ Pin Voltage (Survival)		0.3V to +6.0V
I_{OUT} (Survival)		Internally Limited

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperatures and times are for Sn-Pb (STD) only.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method is per JESD22-A114.
(5) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).

Operating Ratings(1)

Input Supply Voltage, V_{IN}	2.25V to 5.5V
Enable Input Voltage, V_{EN}	0.0V to 5.5V
$\overline{\text{ERROR}}$ Pin Voltage	0.0V to V_{IN}
Output Current (DC)	0 mA to 3A
Junction Temperature(2)	−40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and conditions, see the Electrical Characteristics.

(2) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).

Electrical Characteristics

Unless otherwise specified: V_{IN} = 2.5V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = 2.0V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage Tolerance(1)	2.25V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 3A	-1.6 **−4.1**	0	+1.6 **+2.6**	%
		2.25V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 3A 0°C ≤ T_J ≤ 125°C	-2.6	0	+2.6	
$\Delta V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation(2)(1)	2.25V ≤ V_{IN} ≤ 5.5V	-	0.03 **0.06**	-	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation(3)(1)	10 mA ≤ I_{OUT} ≤ 3A	-	0.10 **0.20**	-	%/A
V_{DO}	Dropout Voltage(4)	I_{OUT} = 3A	-	-	**425.**	mV
I_{GND}	Ground Pin Current, Output Enabled	I_{OUT} = 10 mA $\overline{\text{ERROR}}$ pin = GND	-	10	12 **15**	mA
		I_{OUT} = 3A $\overline{\text{ERROR}}$ pin = GND	-	12	15 **20**	
	Ground Pin Current, Output Disabled	V_{EN} = 0.50V $\overline{\text{ERROR}}$ pin = GND	-	60	100 **110**	µA
I_{SC}	Short Circuit Current	V_{OUT} = 0V	-	5.6	-	A
Enable Input						
$V_{EN(TH)}$	Enable On/Off Threshold	V_{EN} rising from 0.0V until the output turns On, or V_{EN} falling from ≥ 2.0V until the output turns Off	0.74 **0.56**	0.85	0.92 **1.00**	V
$t_{d(OFF)}$	Turn-off delay	Time from V_{EN} < $V_{EN(TH)}$ to V_{OUT} = OFF, I_{LOAD} = 3A	-	5	-	µs
$t_{d(ON)}$	Turn-on delay	Time from V_{EN} >$V_{EN(TH)}$ to V_{OUT} = ON, I_{LOAD} = 3A	-	5	-	
I_{EN}	Enable Pin Current	V_{EN} = V_{IN}	-	1	-	nA
		V_{EN} = 0V	-	-1	-	

(1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

(2) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the voltage at the input.

(3) Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in the load current at the output.

(4) Dropout voltage (V_{DO}) is typically defined as the input to output voltage differential (V_{IN} - V_{OUT}) where the input voltage is low enough to cause the output voltage to drop 2% from the nominal value. For the LP38513, the minimum operating voltage of 2.25V is the limiting factor and the maximum dropout voltage is defined as: $V_{DO(MAX)}$ = $V_{IN(MIN)}$ - $V_{OUT(MIN)}$ = (i.e. 2.25V - (1.80V x 95.9%) = 524 mV)

Electrical Characteristics (continued)

Unless otherwise specified: V_{IN} = 2.5V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = 2.0V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{ERROR}}$ Flag						
V_{TH}	$\overline{\text{ERROR}}$ Flag Threshold(5)	V_{OUT} falling from $V_{OUT(NOM)}$ until $\overline{\text{ERROR}}$ Flag goes low	**77**	85	**94**	%
ΔV_{TH}	$\overline{\text{ERROR}}$ Flag Threshold Hysteresis(5)	V_{OUT} rising from V_{TH} until $\overline{\text{ERROR}}$ Flag goes high	**2.2**	4	**5.8**	
$V_{ERROR(SAT)}$	$\overline{\text{ERROR}}$ Flag Saturation Voltage	I_{SINK} = 1 mA	-	20	**100**	mV
I_{lk}	$\overline{\text{ERROR}}$ Flag Pin Leakage Current	$V_{\overline{\text{ERROR}}}$ = 5.5V	-	100	-	nA
t_d	$\overline{\text{ERROR}}$ Flag Delay time		-	1	-	µs
AC Parameters						
PSRR	Ripple Rejection	V_{IN} = 2.5V f = 120Hz	-	73	-	dB
		V_{IN} = 2.5V f = 1 kHz	-	70	-	
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz	-	0.8	-	µV/$\sqrt{\text{Hz}}$
e_n	Output Noise Voltage	BW = 100Hz – 100kHz V_{OUT} = 1.8V	-	45	-	μV_{RMS}
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	-	165	-	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	-	10	-	
θ_{J-A}	Thermal Resistance Junction to Ambient	TO-220(6)	-	60	-	°C/W
		DDPAK/TO-263(6)	-	60	-	
θ_{J-C}	Thermal Resistance Junction to Case	TO-220	-	3	-	°C/W
		DDPAK/TO-263	-	3	-	

(5) The $\overline{\text{ERROR}}$ Flag thresholds are specified as percentage of the nominal regulated output voltage. See Application Information.
(6) Device operation must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}).

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2.0V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

V_{OUT} vs Temperature

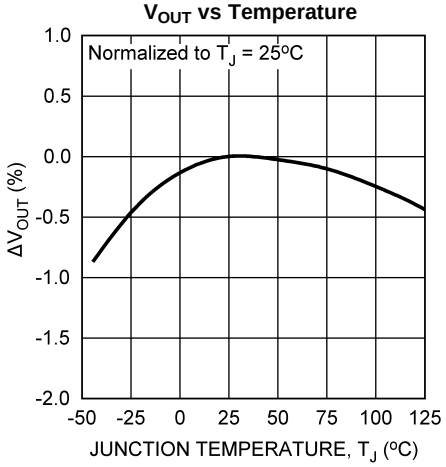


Figure 3.

V_{OUT} vs V_{IN}

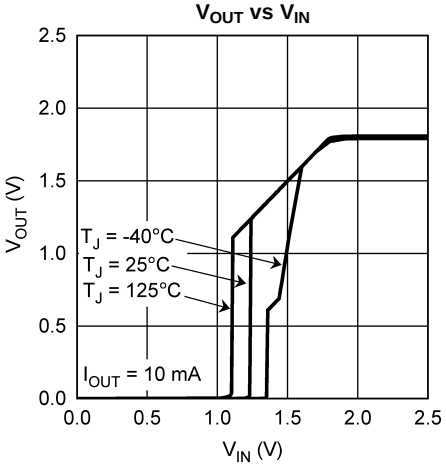


Figure 4.

Ground Pin Current (I_{GND}) vs V_{IN}

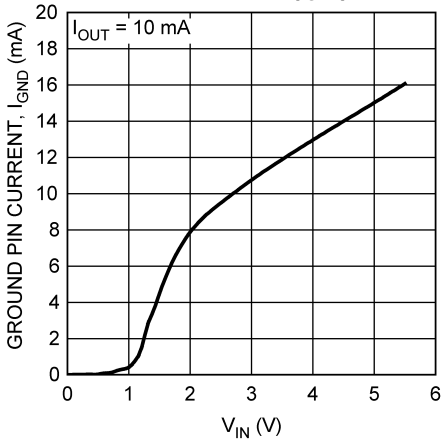


Figure 5.

Ground Pin Current (I_{GND}) vs Temperature

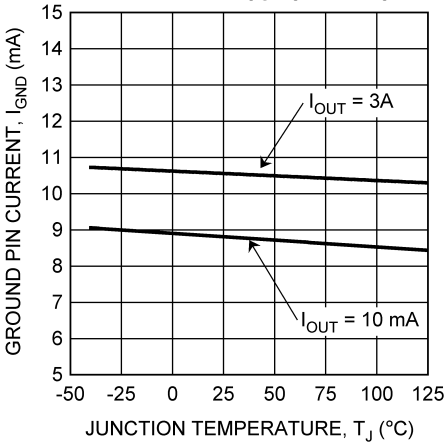


Figure 6.

Ground Pin Current(I_{GND}) vs Temperature

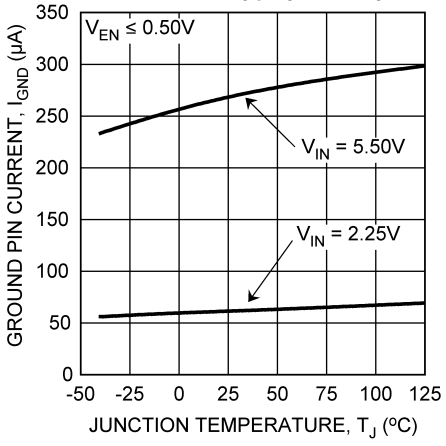


Figure 7.

Enable Threshold vs Temperature

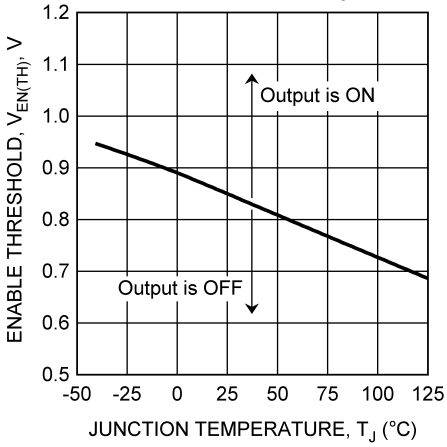


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2.0V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

V_{OUT} vs V_{EN}

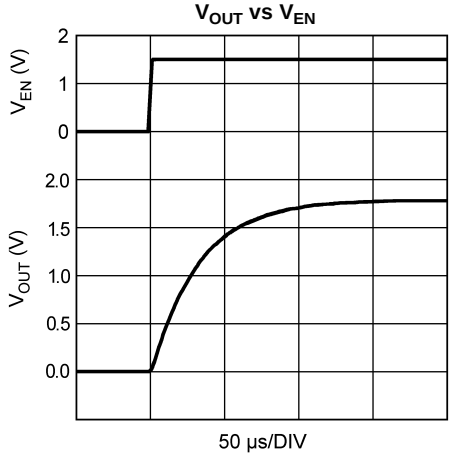


Figure 9.

V_{OUT} ERROR Flag Threshold vs Temperature

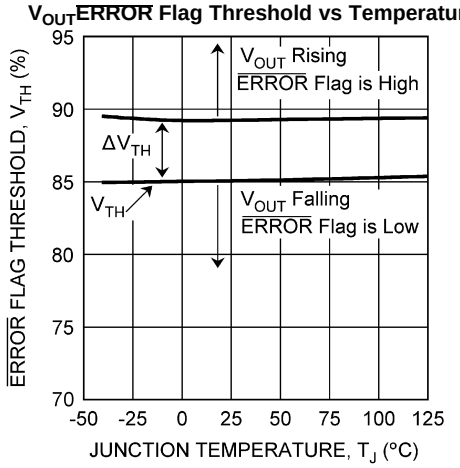


Figure 10.

ERROR Flag Low vs Temperature

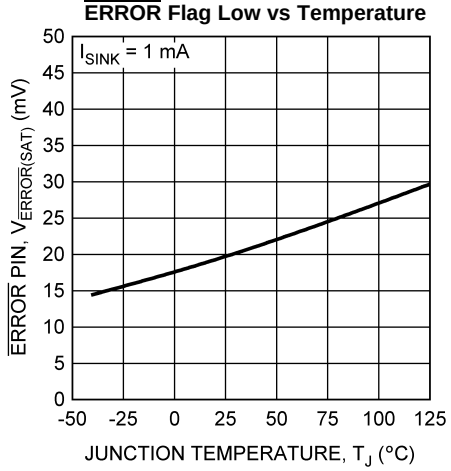


Figure 11.

ERROR Flag Leakage vs Temperature

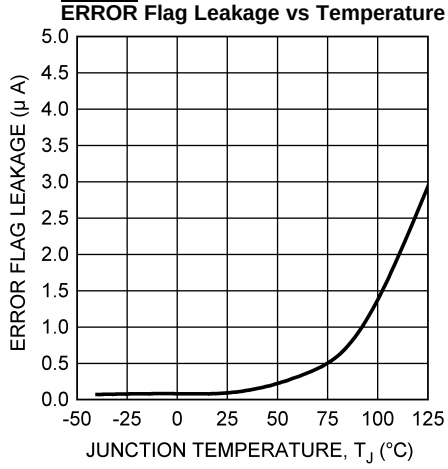


Figure 12.

Load regulation vs Temperature

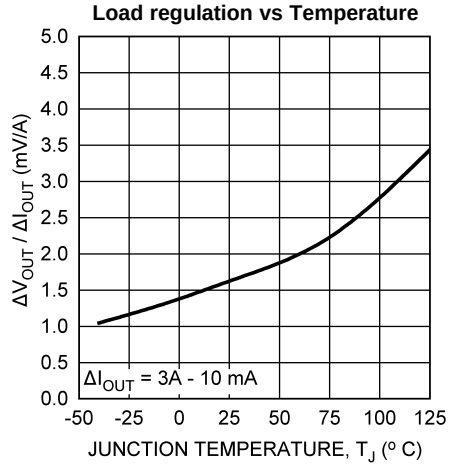


Figure 13.

Line Regulation vs Temperature

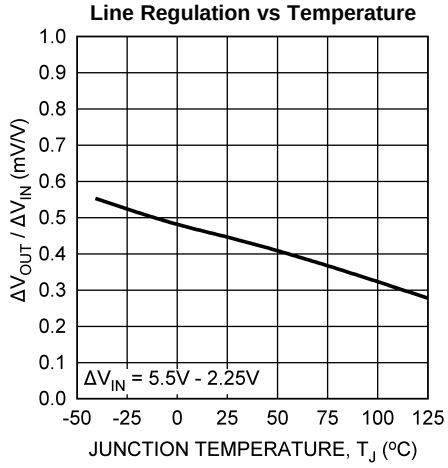


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2.0V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

Current Limit vs Temperature

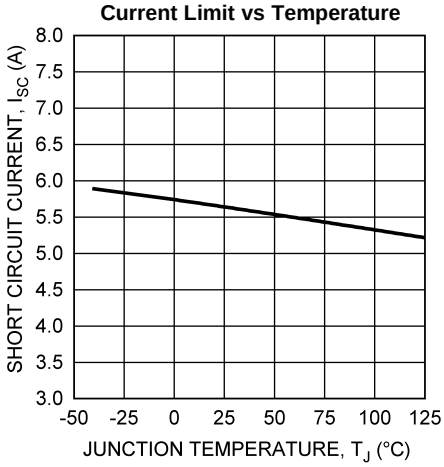


Figure 15.

Load Transient 10mA to 3A, C_{OUT} = 10 µF Ceramic

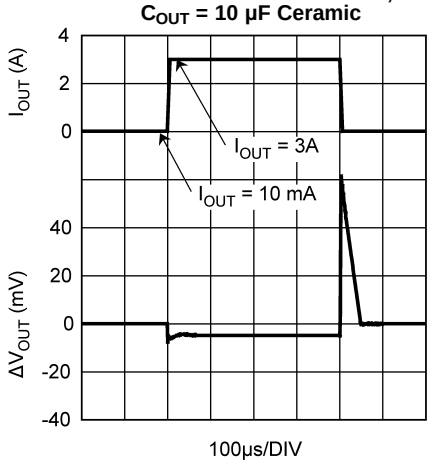


Figure 16.

Load Transient 10 mA to 3A, C_{OUT} = 10 µF Ceramic + 100 µF Aluminum

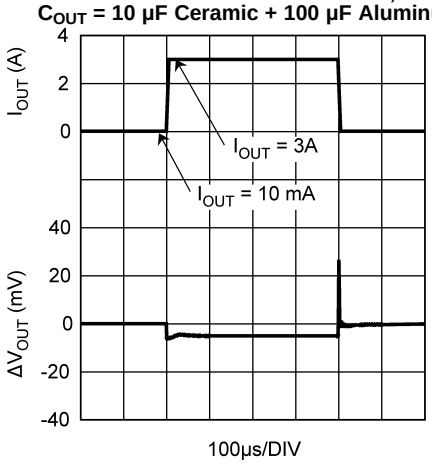


Figure 17.

Load Transient 1A to 3A, C_{OUT} = 10 µF Ceramic

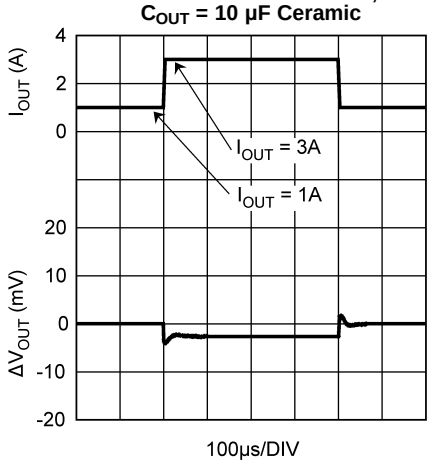


Figure 18.

Load Transient 1A to 3A, C_{OUT} = 10 µF Ceramic + 100 µF Aluminum

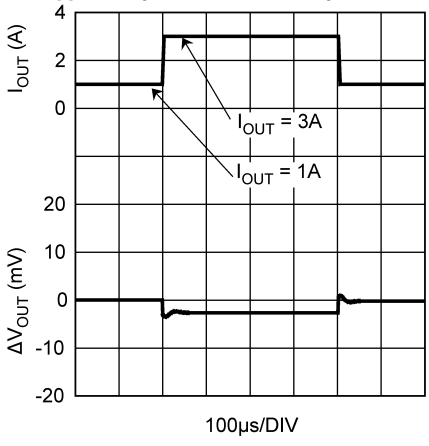


Figure 19.

Line Transient

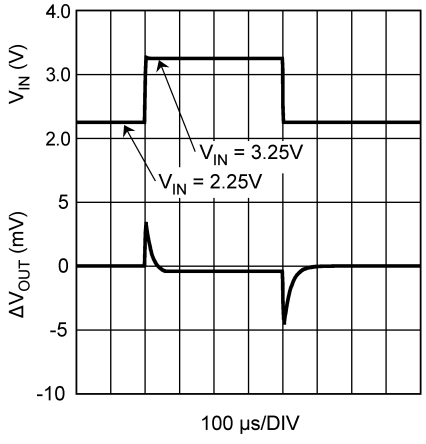


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.5V, V_{EN} = 2.0V, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA.

PSRR

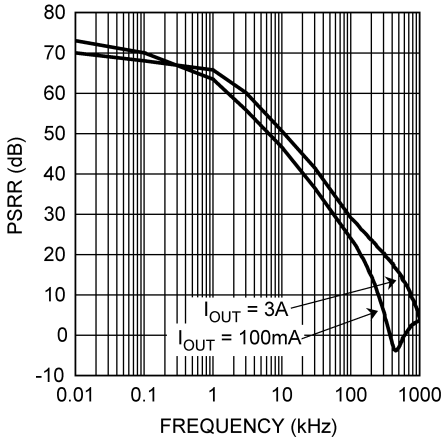


Figure 21.

Noise

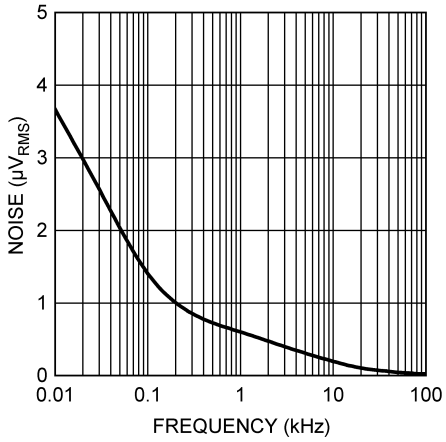
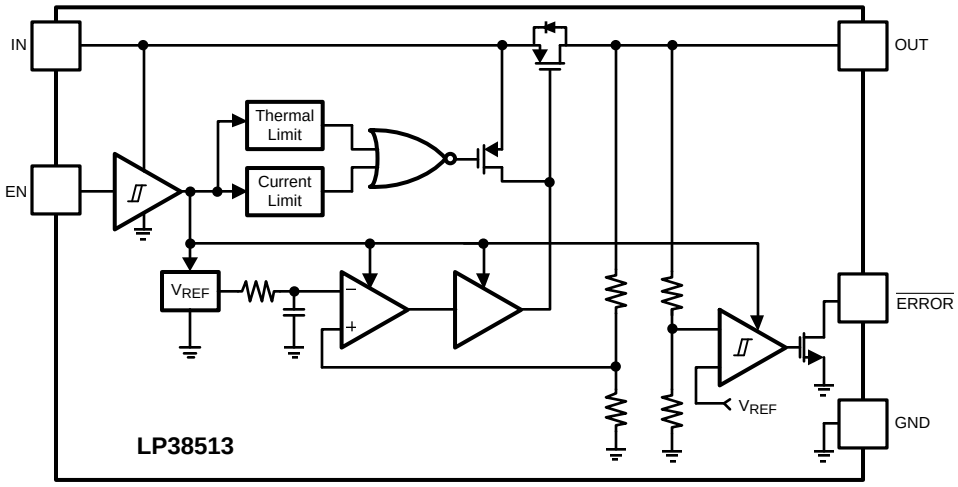


Figure 22.

Block Diagram



APPLICATION INFORMATION

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR:

A ceramic input capacitor of at least 10 µF is required. For general usage across all load currents and operating conditions, a 10 µF ceramic input capacitor will provide satisfactory performance.

OUTPUT CAPACITOR:

A ceramic capacitor with a minimum value of 10 µF is required at the output pin for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pin using traces which have no other currents flowing through them. As long as the minimum of 10 µF ceramic is met, there is no limitation on any additional capacitance.

X7R and X5R dielectric ceramic capacitors are strongly recommended, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

Z5U and Y5V dielectric ceramics are not recommended as the capacitance will drop severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

While V_{IN} is high enough to keep the control circuity alive, and the Enable pin is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. Since the input voltage is less than the output voltage the control circuit will drive the gate of the pass element to the full on condition when the output voltage begins to fall. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided.

The internal PFET pass element in the LP38513 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output voltage to input voltage differential is more than 500 mV (typical) the parasitic diode becomes forward biased and current flows from the output pin to the input through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground. A Schottky diode is recommended for this protective clamp.

SHORT-CIRCUIT PROTECTION

The LP38513 is short circuit protected, and in the event of a peak over-current condition the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to the POWER DISSIPATION/HEAT-SINKING section for power dissipation calculations.

ENABLE OPERATION

The Enable On/Off threshold is typically 850 mV, and has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through this threshold.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

If the Enable pin is driven from a single ended device (such as the collector of a discrete transistor) a pull-up resistor to V_{IN}, or a pull-down resistor to ground, will be required for proper operation. A 1 kΩ to 100 kΩ resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the pin should be connected directly to the adjacent V_{IN} pin.

The status of the Enable pin also affects the behavior of the $\overline{\text{ERROR}}$ Flag. While the Enable pin is high the regulator control loop will be active and the $\overline{\text{ERROR}}$ Flag will report the status of the output voltage. When the Enable pin is taken low the regulator control loop is shutdown, the output is turned off, and the internal logic will immediately force the $\overline{\text{ERROR}}$ Flag pin low.

$\overline{\text{ERROR}}$ FLAG OPERATION

When the LP38513 Enable pin is high, the $\overline{\text{ERROR}}$ Flag pin will produce a logic low signal when the output drops by more than 15% (V_{TH}, typical) from the nominal output voltage. The drop in output voltage may be due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The output voltage will need to rise to greater than typically 89% of the nominal output voltage for the $\overline{\text{ERROR}}$ Flag to return to a logic high state. It should also be noted that when the Enable pin is pulled low, the $\overline{\text{ERROR}}$ Flag pin is forced to be low as well.

The internal $\overline{\text{ERROR}}$ flag comparator has an open drain output stage. Hence, the $\overline{\text{ERROR}}$ pin requires an external pull-up resistor. The value of the pull-up resistor should be in the range of 2 kΩ to 20 kΩ, and should be connected to the LP38513 output voltage pin. The $\overline{\text{ERROR}}$ Flag pin should not be pulled-up to any voltage source higher than V_{IN} as current flow through an internal parasitic diode may cause unexpected behavior. When the input voltage is less than typically 1.25V the status of the $\overline{\text{ERROR}}$ flag output will not be reliable. The $\overline{\text{ERROR}}$ Flag pin must be connected to ground if this function is not used.

The timing diagram in Figure 23 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage when the pull-up resistor is connected to the output voltage pin.

The timing diagram in Figure 24 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage when the pull-up resistor is connected to the input voltage.

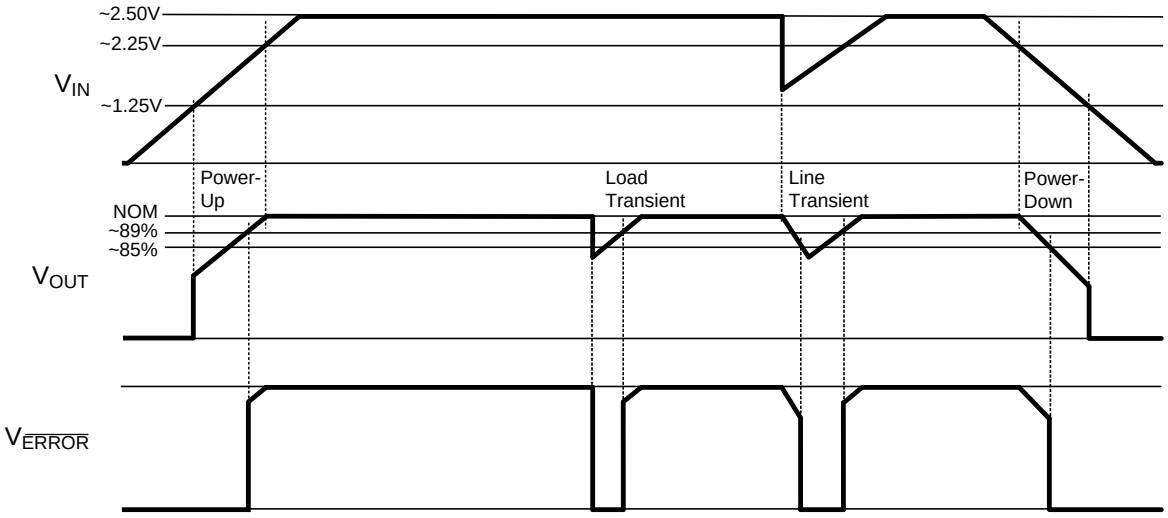


Figure 23. $\overline{\text{ERROR}}$ Flag Operation, see Typical Application Circuit

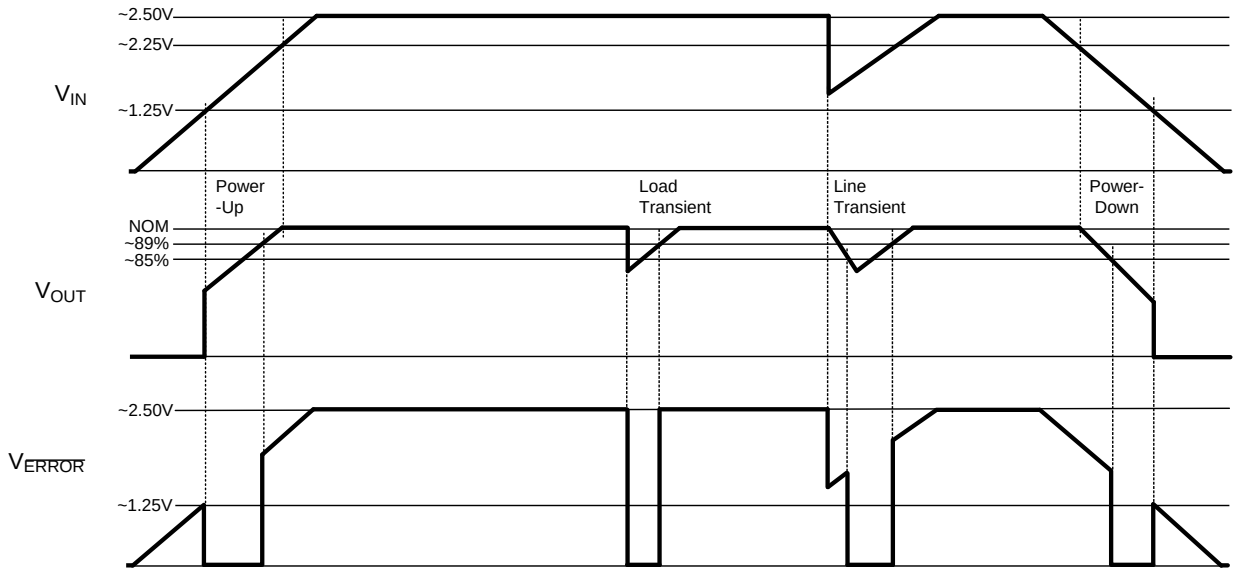


Figure 24. $\overline{\text{ERROR}}$ Flag Operation, biased from V_{IN}

POWER DISSIPATION/HEAT-SINKING

A heat-sink may be required depending on the maximum power dissipation ($P_{D(MAX)}$), maximum ambient temperature ($T_{A(MAX)}$)of the application, and the thermal resistance (θ_{JA}) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + ((V_{IN}) \times I_{GND})$$

where

- I_{GND} is the operating ground current of the device (specified under Electrical Characteristics). (1)

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (2)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (3)$$

LP38513 is available in TO-220 and DDPAk/TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 60 °C/W for TO-220 package and ≥ 60 °C/W for DDPAK/TO-263 package no heat-sink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required.

HEAT-SINKING THE TO-220 PACKAGE

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat-sink or a copper plane on a PC board. If a copper plane is to be used, the values of θ_{JA} will be the same as shown in the next section for the DDPAK/TO-263 package.

The heatsink to be used in the application should have a heat-sink to ambient thermal resistance,

$$\theta_{HA} \le \theta_{JA} - \theta_{CH} - \theta_{JC} \quad (4)$$

In this equation, θ_{CH} is the thermal resistance from the case to the surface of the heat sink and θ_{JC} is the thermal resistance from the junction to the surface of the case. The rated θ_{JC} is about 3°C/W for a 5-lead TO-22 package. The value for θ_{CH} depends on method of attachment, insulator, etc. θ_{CH} varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

HEAT-SINKING THE DDPAK/TO-263 PACKAGE

The DDPAK/TO-263 package uses the copper plane on the PCB as a heat-sink. The tab of this package is soldered to the copper plane for heat sinking. Figure 25 shows a curve for the θ_{JA} of DDPAK/TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

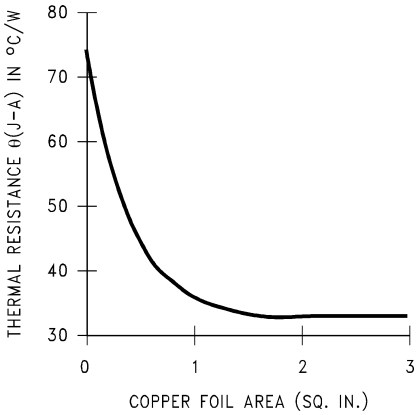


Figure 25. θ_{JA} vs Copper (1 Ounce) Area for the DDPAK/TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for θ_{JA} for the DDPAK/TO-263 package mounted to a PCB is 32°C/W.

Figure 26 shows the maximum allowable power dissipation for DDPAK/TO-263 packages for different ambient temperatures, assuming θ_{JA} is 35°C/W and the maximum junction temperature is 125°C.

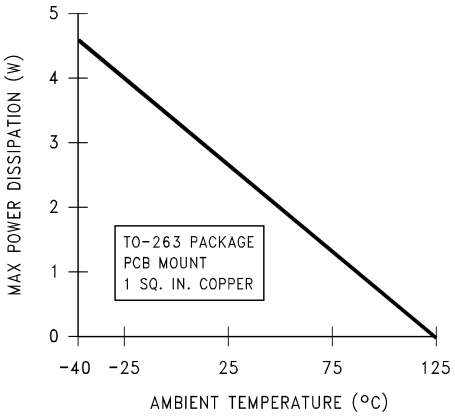


Figure 26. Maximum Power Dissipation vs Ambient Temperature for the DDPAK/TO-263 Package

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP38513S-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP38513S -1.8	Samples
LP38513SX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP38513S -1.8	Samples
LP38513T-1.8/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP38513T -1.8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

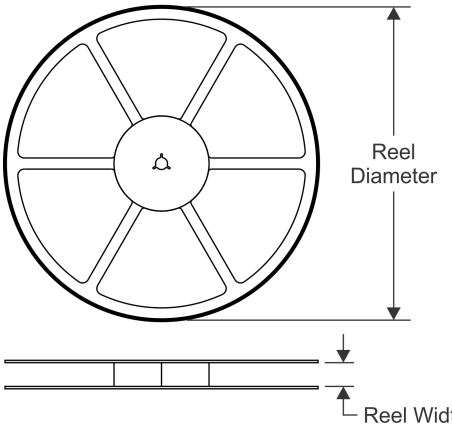
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

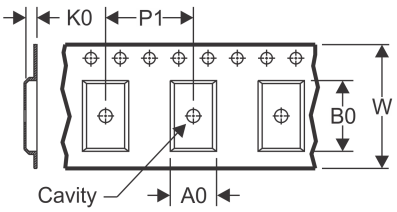
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

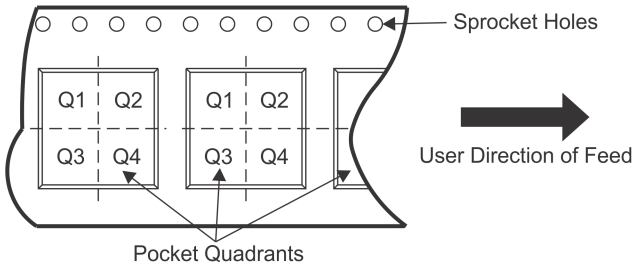


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

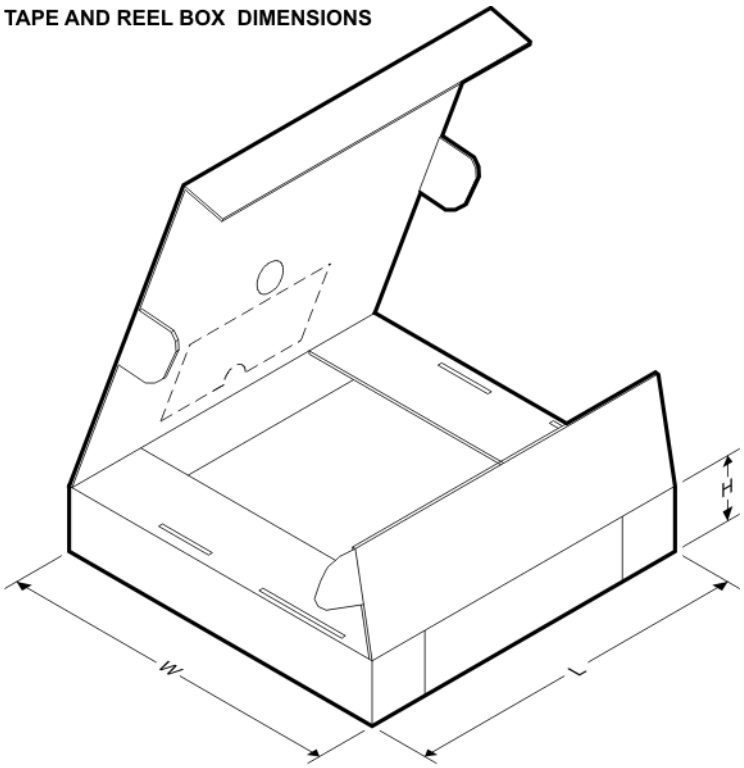
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38513SX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

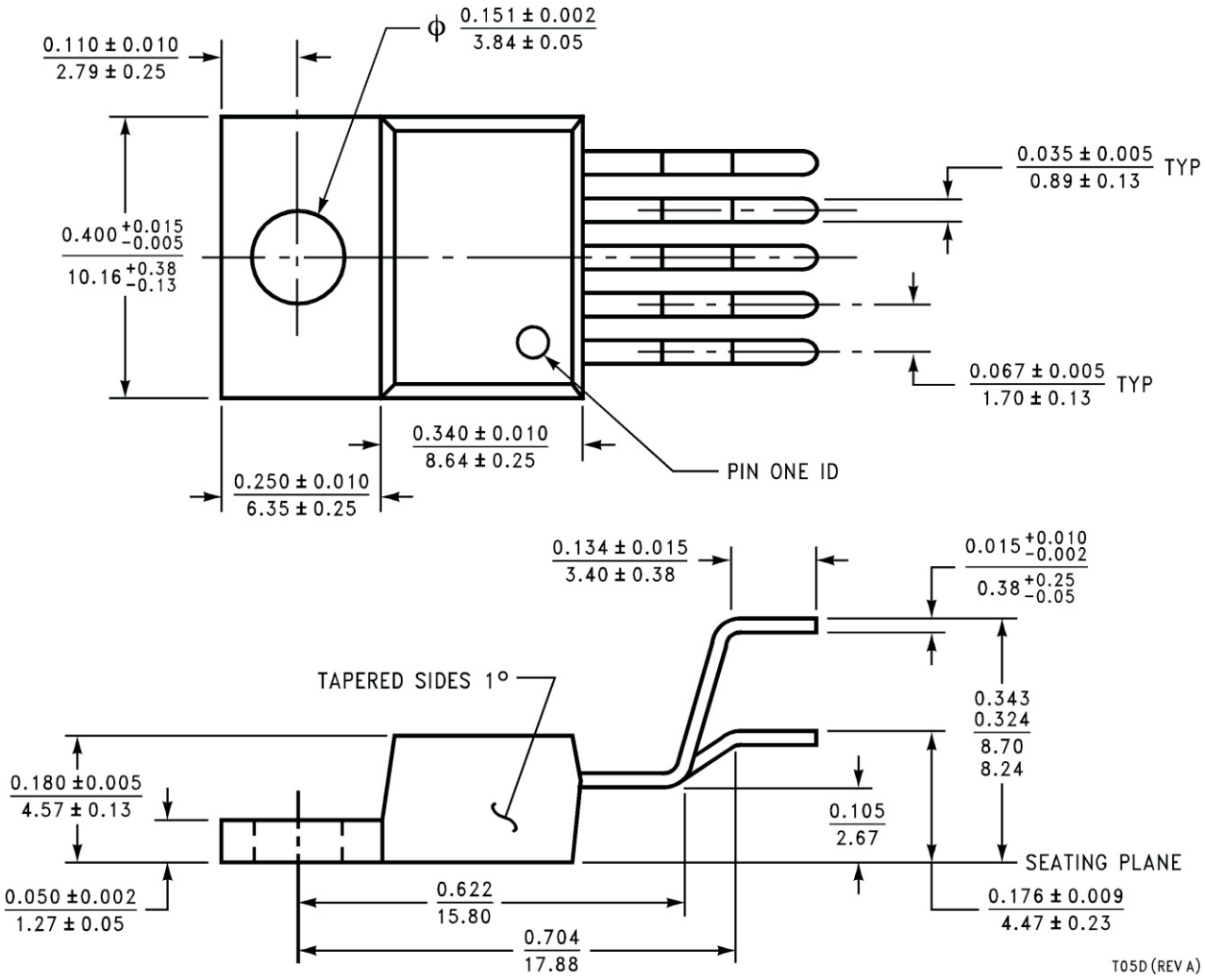
TAPE AND REEL BOX DIMENSIONS



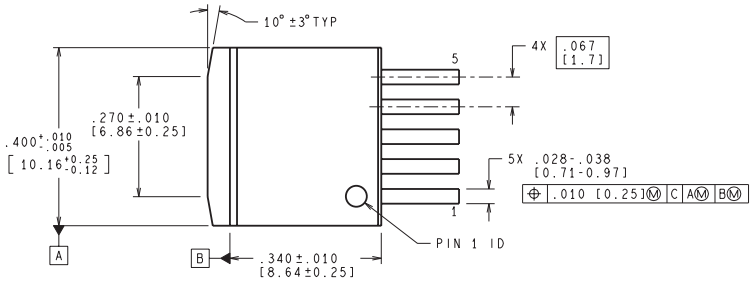
*All dimensions are nominal

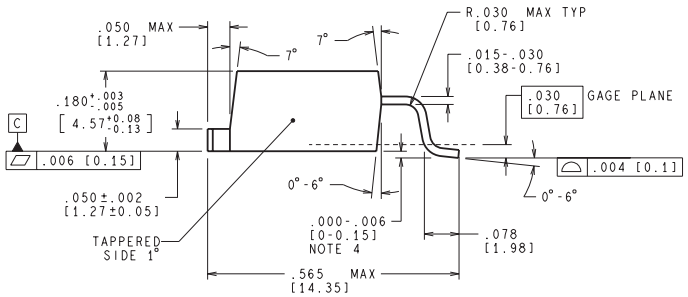
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38513SX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

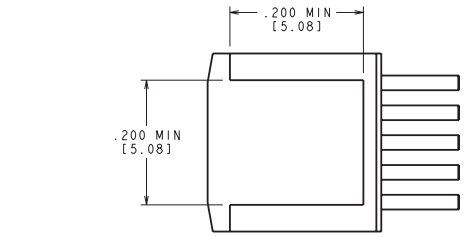
NDH0005D


0.110 ± 0.010
2.79 ± 0.25
ϕ 0.151 ± 0.002
3.84 ± 0.05
0.035 ± 0.005
0.89 ± 0.13
TYP
0.400 +0.015 −0.005
10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
0.340 ± 0.010
8.64 ± 0.25
PIN ONE ID
0.250 ± 0.010
6.35 ± 0.25
0.134 ± 0.015
3.40 ± 0.38
0.015 +0.010 −0.002
0.38 +0.25 −0.05
TAPERED SIDES 1°
0.343
0.324
8.70
8.24
0.180 ±0.005
4.57 ± 0.13
0.105
2.67
SEATING PLANE
0.050 ±0.002
1.27 ± 0.05
0.622
15.80
0.176 ± 0.009
4.47 ± 0.23
0.704
17.88
T05D (REV A)

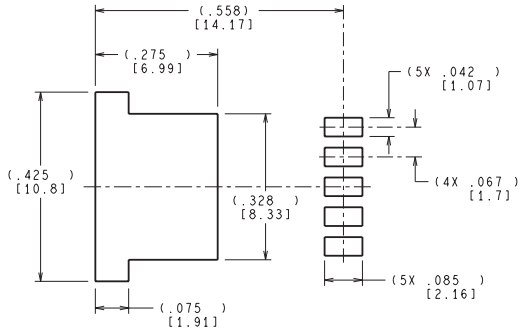
KTT0005B







BOTTOM SIDE OF PACKAGE



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