LM3075 High Efficiency, Synchronous Current Mode Buck Controller

Check for Samples: LM3075

FEATURES

- **Input Voltage Range of 4.5V-36V**
- **Current Mode Control**
- **Skip Mode Operation Available**
- **Cycle by Cycle Current Limit**
- **1.24V ±2% Reference**

APPLICATIONS

- **Automotive Power Supplies**
- **Distributed Power Systems**

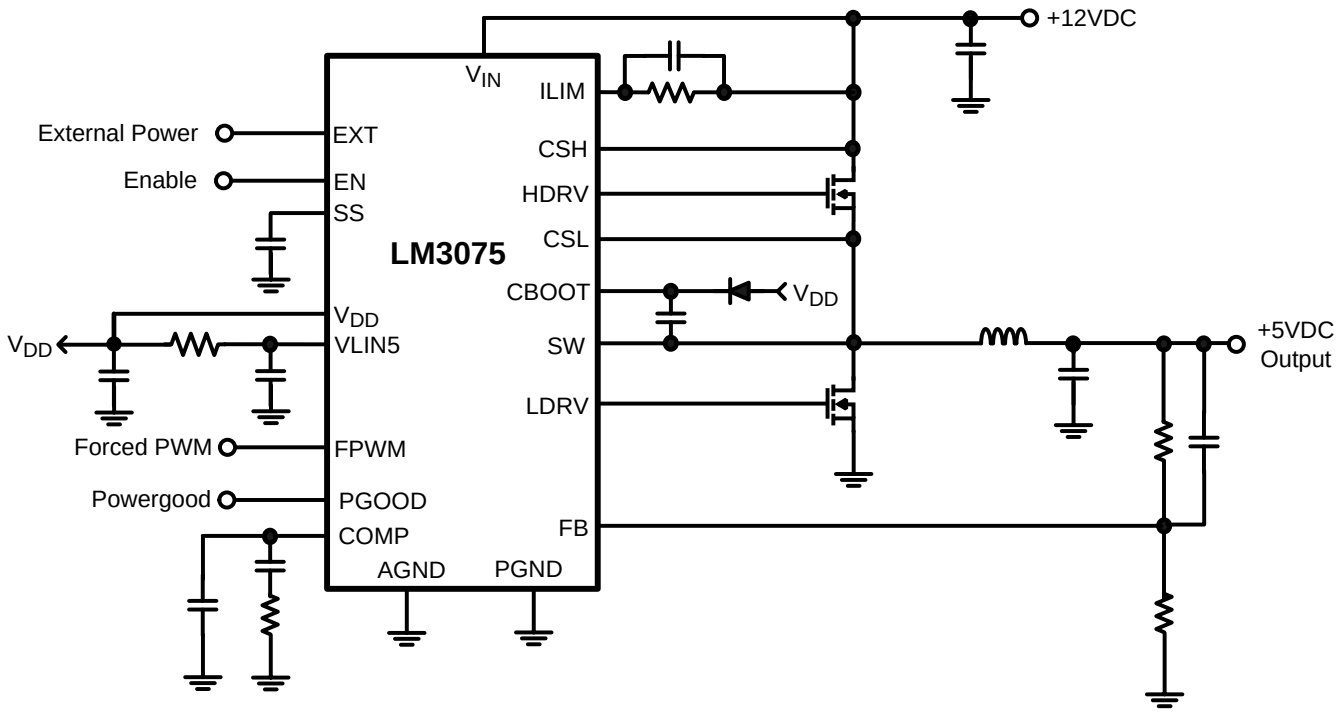
DESCRIPTION

The LM3075 is a current mode control, synchronous buck controller IC. Use of synchronous rectification and pulse-skipping operation at light load achieves high efficiency over a wide load range. Fixed frequency operation can be obtained by disabling the pulse-skipping mode. Current mode control assures excellent line and load regulation and a wide loop bandwidth for fast response to load transients.

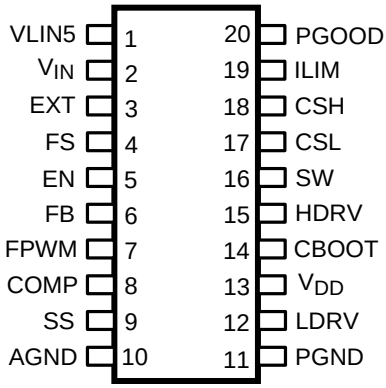
Current mode control can be achieved by either sensing across the high side NFET or a sense resistor. The switching frequency can be selected as either 200 kHz or 300 kHz from an internal clock.

The LM3075 is available with an adjustable output in a TSSOP-20 package.

Typical Application Circuit



Connection Diagram



20-Lead TSSOP - (Top View)
See Package Number PW

PIN DESCRIPTIONS

LM3075 Pin #	Name	Function
1	VLIN5	5V linear regulator output
2	VIN	Input voltage supply
3	EXT	External power connection for VLIN5
4	FS	Frequency select
5	EN	Enable pin
6	FB	Feedback pin
7	FPWM	Forced PWM selection
8	COMP	Compensation pin
9	SS	Output enable / soft-start pin
10	AGND	Analog ground
11	PGND	Power ground
12	LDRV	Low side gate drive
13	VDD	Low side gate drive supply
14	CBOOT	Bootstrap capacitor connection
15	HDRV	High side gate drive
16	SW	Switch node
17	CSL	Current sense low
18	CSH	Current sense high
19	ILIM	Current limit threshold adjustment
20	PGOOD	Power good flag

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Voltages from the indicated pins to GND:	VIN, ILIM, CSH	−0.3V to 38V
	SW, CSL	−0.3 to (V_{IN} + 0.3V)
	PGOOD, FB, VDD, EXT, EN	−0.3V to +7V
	COMP, SS, FPWM, FS	−0.3V to (V_{LIN5} +0.3)V
	CBOOT	-0.3V to +43V
	CBOOT to SW	−0.3V to 7V
	LDRV	−0.3V to (V_{DD}+0.3V)
	HDRV to SW	−0.3V
	HDRV to CBOOT	+0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature		150°C
Lead Temperature (Soldering, 10 sec)		260°C
ESD Rating[3]		1.5kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI's Sales Office/ Distributors for availability and specifications.
(3) For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Operating Ratings[1]

Junction Temperature	−40°C to +125°C
VIN to GND	4.5V to 36V
EXT	6V Max

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics (1)

Limits in standard type are for T_J = 25°C only, and limits in **boldface type** apply over the junction temperature T_J range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified V_{IN} = 12V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{FB}	Feedback pin voltage	V_{IN} = 4.5V to 36V	**1.213**	1.238	**1.259**	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	V_{COMP} = 0.5V to 1.5V		0.04		%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	V_{IN} = 4.5V to 36V		0.04		%
I_Q	Operating Quiescent current	V_{IN} = 4.5V to 36V		1.0	**2**	mA
I_{SD}	Shutdown Quiescent current	V_{EN} = 0V		60	**100**	µA
V_{LIN5}	V_{LIN5} Output Voltage	I_{VLIN5} = 0 to 25mA V_{IN} = 5.5V to 36V	**4.7**	5	**5.3**	V
V_{UVLO}	V_{LIN5} Under Voltage Lockout		**3.7**	3.9	**4.1**	V
V_{UVLO_HYS}	V_{LIN5} Under Voltage Lockout Hysteresis			0.2		V
V_{CL_OS}	Current Limit Comparator Offset ($V_{ILIM} - V_{CSL}$)			±0.2		mV
I_{ILIM}	I_{LIM} sink current		**8.3**	10	**11.3**	µA
I_{SS_SRC}	Soft-Start Pin Source Current	V_{SS} = 1.2V	**1**	2	**3**	µA
I_{SS_SNK}	Soft-Start Pin Sink Current	V_{SS} = 2V		4		µA
V_{SS_TO}	Soft-Start Timeout Threshold			2		V
V_{OVP}	Over Voltage Protection Rising Threshold	With respect to V_{FB}	**105**	111	**117**	%
V_{OVP_HYS}	Over Voltage Protection Hysteresis	With respect to V_{FB}		2.8		%
POWERGOOD						
V_{PWR_GOOD}	PGOOD Rising Threshold		**92.5**	95.5	**98.5**	%
V_{PWR_BAD}	PGOOD Falling Threshold		**87**	90.5	**95**	%
T_{PGOOD}	PGOOD delay	PGOOD pin de-asserting		10		µs
I_{OL}	PGOOD Low Sink Current	V_{PGOOD} = 0.4V	**0.6**	1		mA
I_{OH}	PGOOD High Leakage Current	V_{PGOOD} = 5V		5	**200**	nA

(1) For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Electrical Characteristics[1] (continued)

Limits in standard type are for T_J = 25°C only, and limits in **boldface type** apply over the junction temperature T_J range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified V_{IN} = 12V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GATE DRIVE						
I_{CBOOT}	C_{BOOT} Leakage Current	V_{CBOOT} = 7V		10		nA
$R_{ds\_on\ 1}$	HDRV FET driver pull-up On resistance			2.9		Ω
$R_{ds\_on\ 2}$	HDRV FET driver pull-down On resistance			1.7		Ω
$R_{ds\_on\ 3}$	LDRV FET driver pull-up On resistance			2.4		Ω
$R_{ds\_on\ 4}$	LDRV FET driver pull-down On resistance			0.8		Ω
OSCILLATOR						
f_{OSC}	Oscillator Frequency	V_{FS} = 5V	**255**	300	**330**	kHz
		V_{FS} = 0V	**165**	200	**215**	
D_{MAX}	Maximum Dutycycle	V_{FB} = 1V	**95.5**	98		%
T_{ON_MIN}	Minimum On Time			180	**260**	ns
ERROR AMPLIFIER						
I_{FB}	Feedback pin bias current	V_{FB} = 1.5V		50		nA
I_{COMP_SRC}	COMP Output Source Current	V_{FB} = 1V V_{COMP} = 1V		120		µA
I_{COMP_SNK}	COMP Output Sink Current	V_{FB} = 1.5V V_{COMP} = 0.5V		110		µA
Gm	Error Amplifier Transconductance			620		µmho
A_{VOL}	Error Amplifier Voltage Gain			1250		V/V
V_{SL}	Slope Compensation (referred to the internal summing node)	V_{FS} = 0V		0.051		V/µs
		V_{FS} = 5V		0.076		
A_{CS}	Current Sense Amplifier Gain	V_{COMP} = 1.25V	**4**	5	**6**	V/V
LOGIC						
V_{IL}	FS, /FPWM Pin Maximum Low Level Input Level				**0.8**	V
V_{IH}	FS, /FPWM Pin Minimum High Level Input Level		**2**			V
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown			160		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			10		°C

Electrical Characteristics[1] (continued)

Limits in standard type are for T_J = 25°C only, and limits in **boldface type** apply over the junction temperature T_J range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified V_{IN} = 12V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EXT						
R_{EXT}	EXT pin on resistance	V_{EXT} = 5V I_{VLIN5} = 50 mA		4		Ω
TH_{EXT}	VLIN5 to EXT Switch Over Rising Threshold			4.6		V

Typical Performance Characteristics

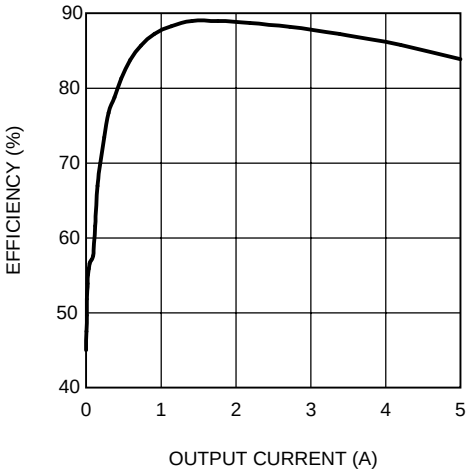


Figure 1.

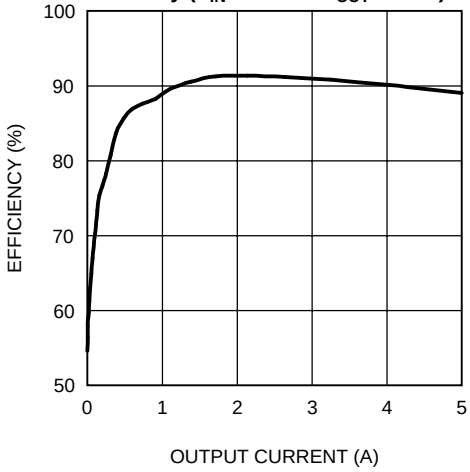


Figure 2.

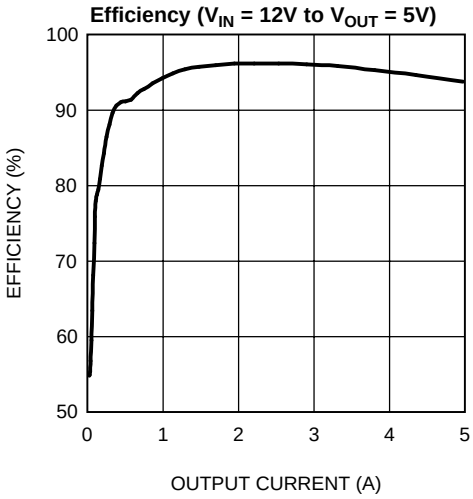


Figure 3.

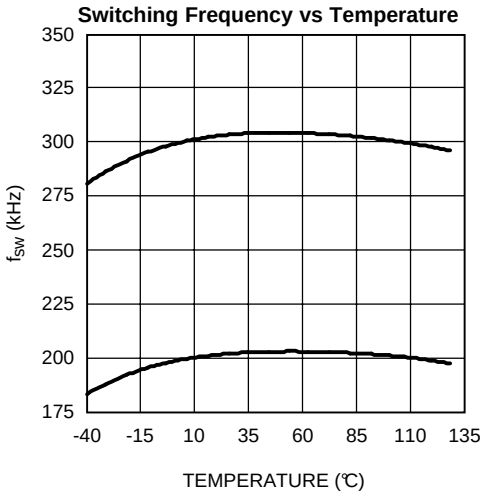


Figure 4.

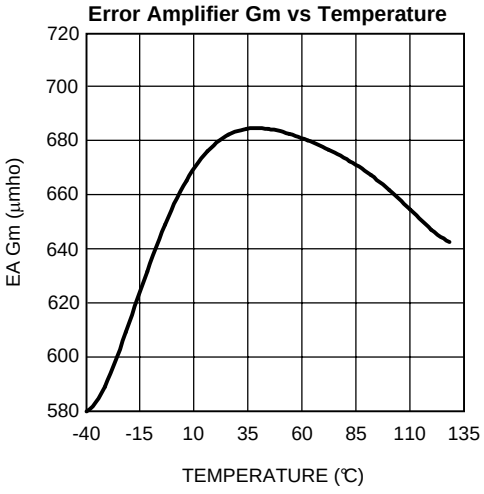


Figure 5.

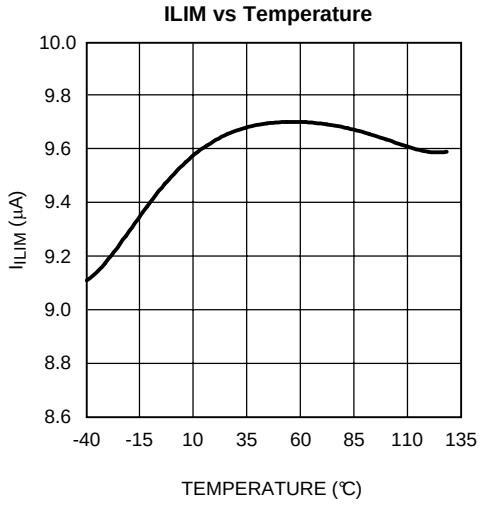


Figure 6.

Typical Performance Characteristics (continued)

ILIM vs V_{IN}

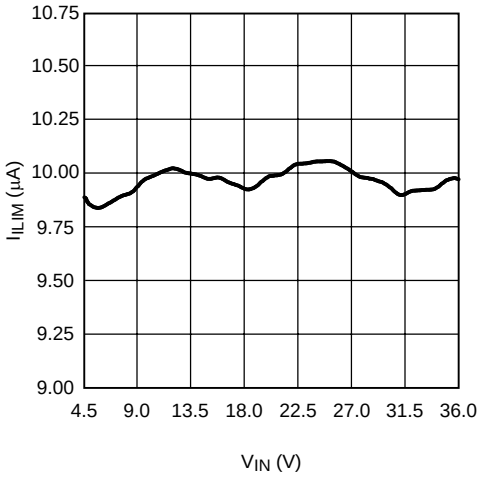


Figure 7.

I_Q vs Temperature (Normal Operation)

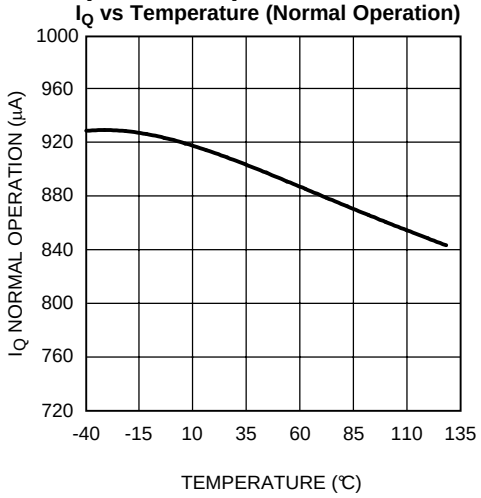


Figure 8.

I_Q vs Temperature (Shutdown)

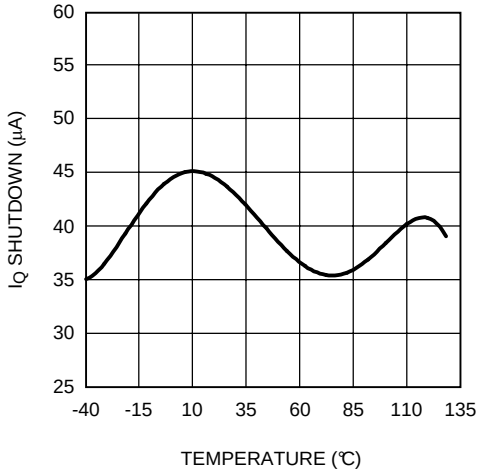


Figure 9.

I_Q vs V_{IN} (Shutdown)

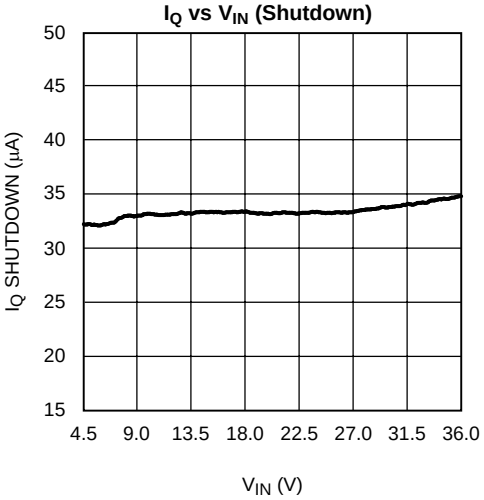


Figure 10.

V_{FB} vs Temperature

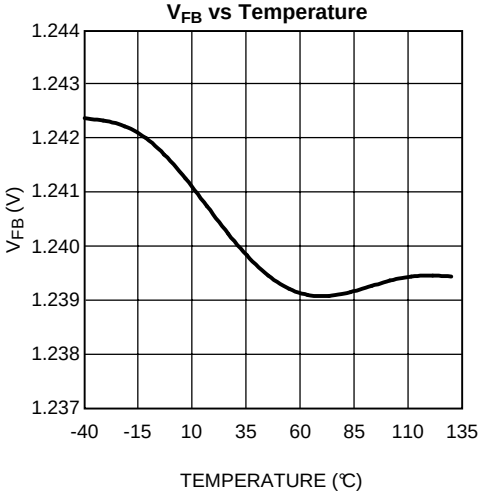


Figure 11.

V_{LIN5} vs V_{IN}

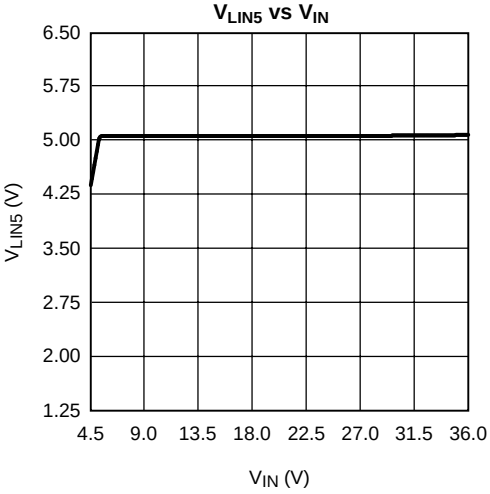


Figure 12.

Typical Performance Characteristics (continued)

Line Regulation

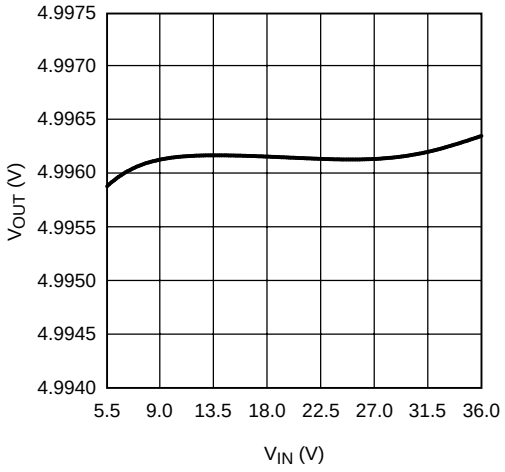


Figure 13.

Load Regulation

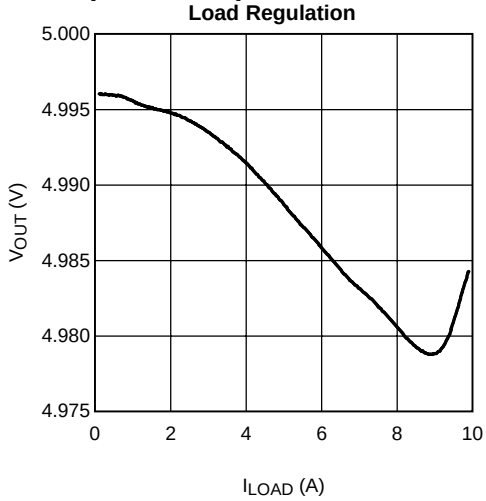
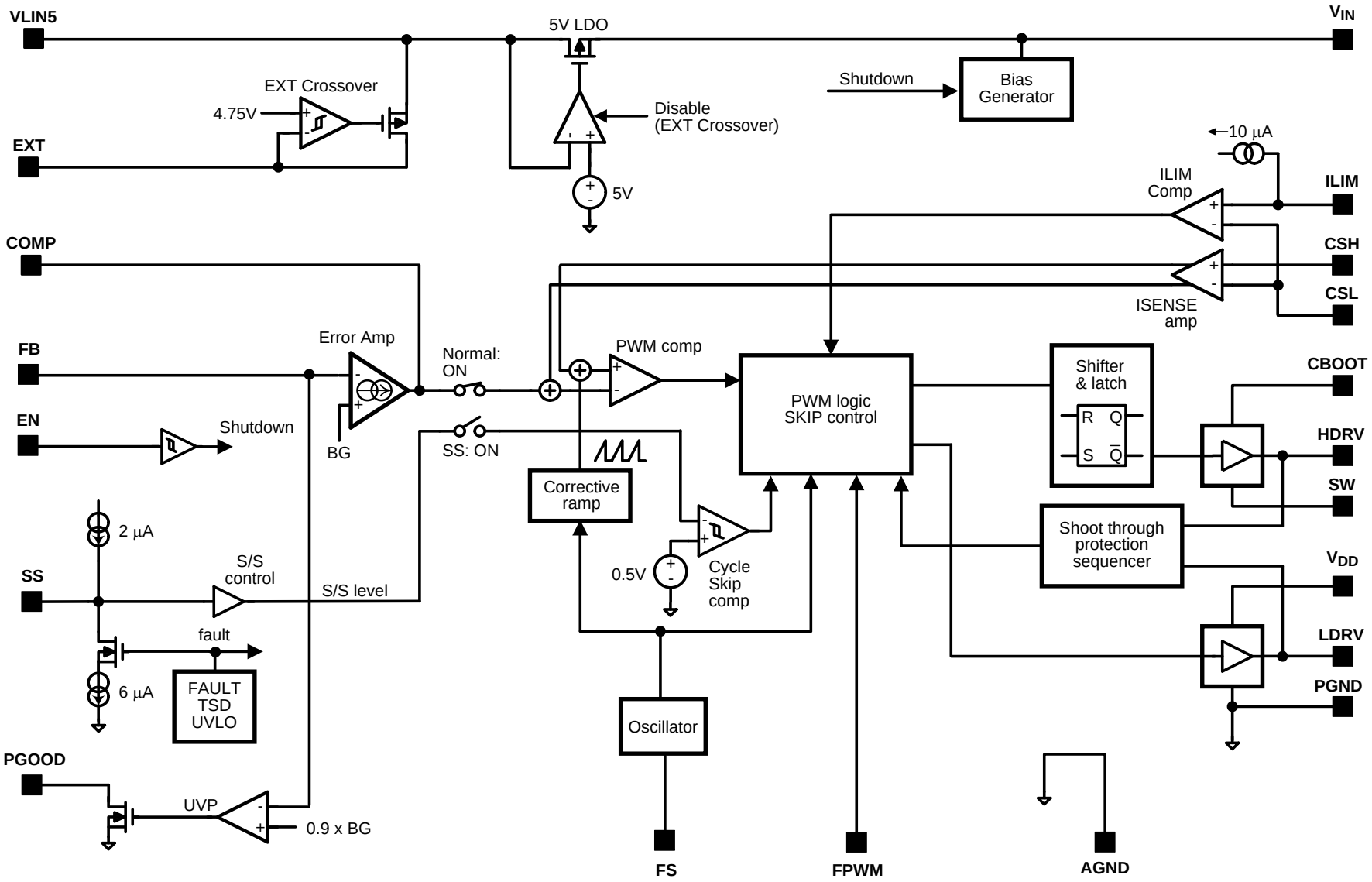


Figure 14.

Block Diagram



OPERATING DESCRIPTIONS

GENERAL

The LM3075 solves the need within many portable systems for 5V, 3.3V, 3.3V stand-by and 12V legacy power supplies. The controller (IC) uses synchronous rectification and employs a peak current mode control scheme. Protection Features include over-voltage protection (OVP), under-voltage protection (UVP), thermal protection, and positive and negative peak current limiting. UVP functionality is automatically disabled during soft-start and then enabled once the IC has correctly started. The device operates with a wide input voltage range from 4.5V to 36V.

SOFT START

In normal operation the soft-start functions as follows:

As the input voltage rises above the 4.2V UVLO threshold, where the internal circuitry is powered on, an internal 2 µA current starts to charge the capacitor connected between the SS pin and ground. A minimum on-time comparator generates the soft-start PWM pulses. As the SS pin voltage ramps up, the duty cycle increases, causing the output voltage to ramp up. During this time, the error amplifier output voltage is clamped at 2V, and the duty cycle generated by the PWM comparator is ignored. When the output voltage exceeds 98.5% (typical) of the set target voltage, the regulator transitions from soft-start to operating mode. Beyond this point, once the PWM pulses generated by the PWM comparator are narrower than those generated by the minimum on-time comparator, the PWM comparator takes over and starts to regulate the output voltage. Peak current mode control now takes place. The rate at which the duty cycle increases depends on the capacitance of the soft-start capacitor. The higher the capacitance, the slower the output voltage ramps up.

A unique feature of the LM3075 is that the rate at which the duty cycle grows is independent of the input voltage. This is because the ramp signal used to generate the soft-start duty cycle has a peak value proportional to the input voltage, making the product of duty cycle and input voltage a constant. This makes the soft-start process more predictable and reliable.

During soft-start, under-voltage protection is temporarily suspended but over-voltage protection and current limit remain in effect. When the SS pin voltage exceeds 2V, a soft-start time out signal is issued. This signal sets the under-voltage protection into ready mode. This is discussed more in the Under-Voltage Protection section.

If the SS pin is short-circuited to ground before startup, the LM3075 operates at minimum duty cycle when it is enabled, and the under-voltage protection is disabled.

FAULT STATE

When a fault condition is detected, a "fault" signal is generated internally. This signal discharges the capacitor connected between the SS pin and ground with 4 µA of current until the SS pin reaches 60mV. Once a level of 60mV is reached at the SS pin, the IC restarts normally and resumes operation assuming the cause of the fault condition has been removed.

FORCE PWM MODE

Pulling the FPWM pin to logic low activates the force PWM mode. In this mode, the top FET and the bottom FET gate signals are always complementary to each other and the Negative Current Limit comparator is activated (see Negative Current Limit section). In force PWM mode, the regulator always operates in Continuous Conduction Mode (CCM) and the duty cycle, which is approximately V_{OUT}/V_{IN} in this mode, is almost independent of load. The force PWM mode is good for applications where fixed switching frequency is required. In forced PWM mode, the top FET has to be turned on for a minimum of typically 180 ns each cycle. However, if the required duty cycle is less than the minimum value, the IC is unable to reach the desired voltage output in FPWM mode. This causes the chip to enter a fault state and the IC attempts to restart until the cause of the fault has been removed (see the Fault State section).

SKIP COMPARATOR

Whenever the output voltage of the error amplifier (COMP pin) goes below a 0.5V threshold, the PWM cycles are "skipped" until that voltage exceeds the threshold again. Due to the time required for the system loop to respond to changes, it is unlikely that the system will oscillate around the threshold and thus the system remains stable.

PULSE-SKIP MODE

Pulse-skip mode is activated by pulling the FPWM pin to a TTL-compatible logic high. In this mode, the Zero-Crossing / Negative Current Limit comparator detects the bottom FET current. Once the bottom FET current flows from drain to source, the bottom FET is turned off. This prevents negative inductor current.

In force PWM operation, the inductor current is allowed to go negative, so the regulator is always in Continuous Conduction Mode (CCM), no matter what the load is. In pulse-skip mode, the regulator enters Discontinuous Conduction Mode (DCM) under light loads. Once the regulator enters DCM, its switching frequency drops as the load current decreases. The minimum on-time comparator takes over causing the output voltage to continuously rise and COMP pin voltage (the error amplifier output voltage) to continuously drop. When the COMP pin voltage hits the 0.5V level, the Cycle Skip comparator toggles, causing the present switching cycle to be "skipped", i.e., both FETs remain off during the whole cycle. As long as the COMP pin voltage is below 0.5V, no switching of the FETs happens. As a result, the output voltage drops, and the COMP pin voltage rises. When the COMP pin goes above the 0.5V level, the Cycle Skip comparator flips and allows a series of on-time pulses to happen. If the load current is so small that this series of pulses is enough to bring the output voltage up to such a level that the COMP pin drops below 0.5V again, the pulse skipping happens again. Otherwise it may take a number of consecutive pulses to bring the COMP pin voltage down to 0.5V again. As the load current increases, it takes more and more consecutive pulses to drive the COMP voltage to 0.5V. The pulse-skipping stops when the load current is sufficiently high. In pulse-skip mode, the frequency of the burst of switching pulses varies directly with the load current. Since the load is usually very light in pulse-skip mode, conducted noise is very low and the variable operating frequency should cause no EMI problems in the system.

The LM3075 pulse-skip mode helps the light load efficiency for two reasons. First, the bottom FET is turned on only when inductor current is in the positive conduction region, this eliminates circulating energy loss. Second, the FETs switch only when necessary, rather than every cycle, thus reducing the FETs switching losses and gate drive power losses.

CURRENT SENSING

The inductor current information is extracted by the current sense pins CSH and CSL. As shown in Figure 15 and Figure 16, current sensing is accomplished by either sensing the V_{ds} of the top FET, or sensing the voltage across a current sense resistor connected from V_{IN} to the drain of the top FET. Both approaches have advantages and disadvantages that need to be weighed for each specific application. The advantage of sensing current through the top FET is reduced parts count, board space, and cost but it also has the disadvantage of accuracy. Using a current sense resistor is the opposite, improving current sense accuracy but requiring additional parts, cost, and board space. The use of a current sense resistor has the additional disadvantage of increasing power loss and thus decreasing efficiency.

To ensure linear operation of the current amplifier, the current sense voltage input should not exceed 200 mV. Therefore, the R_{dson} of the top FET or the current sense resistor must be calculated carefully to ensure that, when the top FET is conducting the maximum current for that application, the current sense voltage does not exceed 200 mV.

Assuming a maximum of 200 mV across the CSL/R_{dson} resistor, the maximum allowable resistance can be calculated as follows:

$$R_{MAX} = \frac{200\ mV}{I_{MAX} + \frac{1}{2}\Delta I_L} \quad (1)$$

Where I_{MAX} is the maximum expected load current, including an overload multiplier (typically 120%), and ΔI_L is the inductor ripple current.

Note that the above equation defines only the maximum allowable value and not necessarily the recommended value. As the resistance increases, so do the switching losses.

CURRENT LIMITING

There is a leading edge blanking circuit that forces the top FET to be on for at least 180 ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. With an external resistor connected between the ILIM pin and the CSH pin the 10 µA current sink on the ILIM pin produces a voltage across the resistor to serve as the reference voltage for current limit. Adding a 10 nF capacitor across this resistor filters unwanted noise that could improperly trip the current limit comparator. Current limit is activated if the inductor current is too high causing the voltage at the CSL pin to be lower than that of the ILIM pin, toggling the comparator thus turning off the top FET immediately. The comparator is disabled either when the top FET is turned off or during the leading edge blanking time. The equation for the current limit resistor, RLIM, is as follows:

$$R_{LIM} = \frac{\left(I_{LIM} + \frac{1}{2}\Delta I_L\right) R_{SNS}}{10\ \mu A} \quad (2)$$

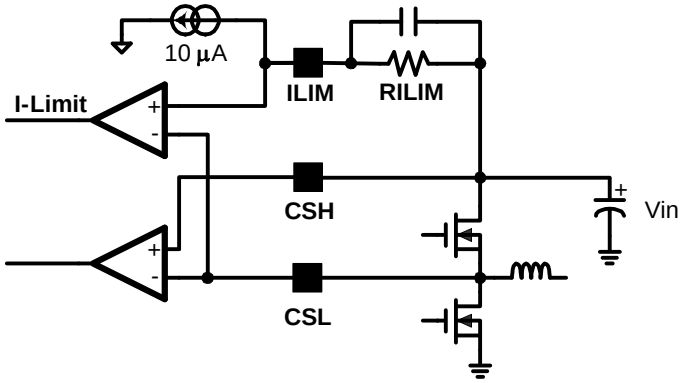


Figure 15. Current Sensing by Vds of the Top FET

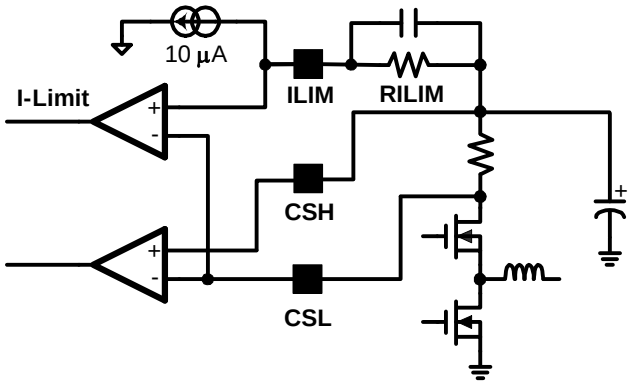


Figure 16. Current Sensing by External Sense Resistor

NEGATIVE CURRENT LIMIT

The purpose of negative current limit is to ensure that the inductor does not saturate during negative current flow causing excessive current to flow through the bottom FET. The negative current limit is realized through sensing the bottom FET V_{ds}. An internally generated 100mV (typical) reference is used to compare with the bottom FET V_{ds} when it is on. Upon sensing too high a V_{ds}, the bottom FET is turned off. The negative current limit is only activated in force PWM mode.

OVER VOLTAGE PROTECTION (OVP)

The LM3075 responds to over-voltage events by attempting to recover without the need to restart the IC. There is a trip point at approximately 111% (typical) of V_{OUT} that, once reached, causes the circuit to shut off the HDRV FET and turn on the LDRV FET immediately to drive the bottom FET to discharge the output capacitor through the filter inductor. The system stays in this configuration until the output falls below approximately 108% (typical) of V_{OUT}. Once this lower level has been reached, the system resumes operation in either DCM or CCM. This scenario repeats until the cause of the over-voltage condition is removed.

UNDER VOLTAGE PROTECTION

When an under-voltage event is detected by the LM3075 and the under-voltage protection (UVP) is in ready mode, the IC attempts to restart the entire system. It does so by shutting off both the LDRV and HDRV FETs until the soft-start capacitor has discharged below a level of 60mV (typical). At this point, the IC shuts off the UVP and restarts the system as though it had just been powered up. The UVP is re-engaged once the soft-start capacitor voltage reaches a level of 2V (typical) and it enters ready mode as it does when the IC first was powered up. The UVP stays in ready mode until a new under-voltage event is detected.

POWER GOOD FUNCTION

A power good signal is available for indicating the general state of the IC. The function is realized through the internal MOSFET tied from the PGOOD pin to ground. The power good signal is asserted by turning off the MOSFET. The on resistance of the power good MOSFET is about 300Ω. The internal power good MOSFET is not turned on unless at least one of the following occurs:

1. There is an output over-voltage event.
2. The output voltage is below the power good lower limit (UVP event).
3. System is in shutdown mode, i.e. the EN pin voltage is below 0.6V.

As with the other protection responses, the power good signal has built-in hysteresis. See V_{PWR_GOOD} in the Electrical Characteristics table.

FREQUENCY SELECT

The operating frequency may be set at 200 kHz or 300 kHz by the voltage on the frequency select (FS) pin. A voltage of 0V corresponds to a frequency of 200 kHz and a voltage of 5V corresponds to a frequency of 300 kHz. See the Electrical Characteristics table for more information.

VLIN5, VDD and EXT

An internal 5V supply (V_{LIN5}) is generated from the V_{IN} voltage through an internal linear regulator. This 5V supply is mainly for internal circuitry use, but can also be used externally. When used externally, it is recommended that the V_{LIN5} voltage only be used for powering the gate drivers, i.e. supplying the bias for the top drivers' bootstrap circuit and the bottom drivers' VDD pins. When the voltage applied to the EXT pin is below 4.7V, an internal 5V low dropout regulator supplies the power for the V_{LIN5}. If the EXT voltage is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on to connect the EXT pin to the VLIN5 pin. This allows the VLIN5 power to be derived from a high efficiency source such as the output of the switching channel, when the channel is configured to operate in fixed 5V mode. The V_{LIN5} voltage output comes from the EXT pin whenever the voltage applied to the EXT pin is higher than 4.7V. The externally applied voltage is required to be less than the voltage applied to the VIN pin at all times. This prevents a voltage feedback situation from the EXT pin to the VIN pin. When the input voltage must be ensured to be within 4.5V to 5.5V, tie the VLIN5 pin directly to the VIN pin and tie the EXT pin to ground. In this mode, the V_{LIN5} current directly comes from power stage input rail and power loss due to the internal linear regulation is no longer an issue. Always connect the VDD pin to the VLIN5 pin through a 4.7Ω resistor and connect a ceramic capacitor of at least 1 µF to bypass the VDD pin to ground.

THERMAL PROTECTION

The LM3075 IC enters thermal protection mode if the die temperature exceeds 160°C. In this mode, the top and bottom FETs are turned off immediately. The IC then behaves in a manner as described in the Fault State section.

OUTPUT CAPACITORS FOR LINEAR REGULATORS

Like any linear regulator, the linear output that is either generated or controlled by the LM3075 requires an output capacitor to ensure stability. The output of VLIN5 needs a minimum of 4.7 µF.

SWITCHING NOISE REDUCTION

Power MOSFETs are very fast switching devices. In a synchronous rectifier converter, the rapid drain current rise rate of the top FET coupled with parasitic inductance generates unwanted Ldi/dt spike noise at the source node of the FET (SW pin). The magnitude of the spike noise increases as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI) that may cause trouble to the system performance. Therefore, it is vital to correct system performance to suppress this kind of noise. As shown in Figure 17, adding a resistor in series with the CBOOT pin scales the spikes and slow down the gate drive (HDRV) rise time of the top FET to yield a desired drain current transition time. Usually a 3.3Ω to 5.1Ω resistor is sufficient to suppress the noise. It is important to note that the addition of these resistors does increase the power loss in the system and thus decreases the efficiency. It is therefore important to choose the size of the resistor carefully; the top FET switching losses increases with higher resistance values.

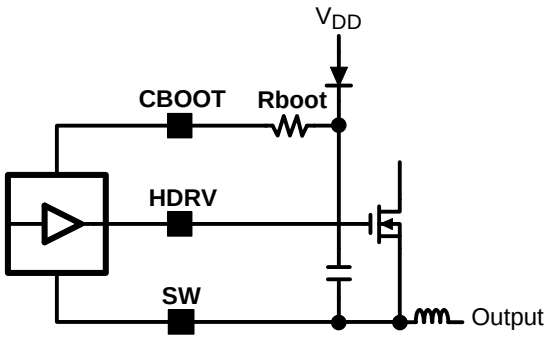


Figure 17. Adding a resistor in series with the CBOOT pin to suppress the turn-on switching noise

Component Selection

OUTPUT VOLTAGE SETTING

The output voltage for each channel is set by the ratio of a voltage divider as shown in Figure 18. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{OUT}}{V_{FB}} - 1\right)} \quad (3)$$

where

- V_{FB} is the typical value of feedback pin voltage and V_{OUT} is the nominal output voltage .

Although increasing the value of R_1 and R_2 increases efficiency, this also decreases accuracy. Therefore, a maximum value is recommended for R_2 in order to keep the output within 0.3% of V_{OUT}. This maximum R_2 value should be calculated first with the following equation:

$$R_{2\_MAX} = \frac{0.3\% \times V_{OUT}}{I_{FB\_MAX}} \quad (4)$$

where

- I_{FB_MAX} is the maximum current drawn by the FB pin.

Example: V_{OUT} = 5V, V_{FB} = 1.238V, I_{FB_MAX} = 200 nA.

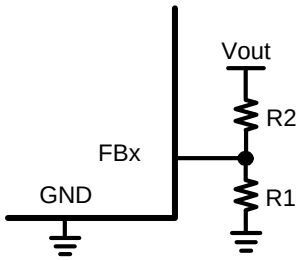


Figure 18. Output Voltage Setting

$$R_{2\_MAX} = \frac{0.3\% \times 5V}{200\ nA} = 75\ k\Omega \quad (5)$$

R_2 is chosen to be 60.4 kΩ±1%. To calculate R1:

$$R_1 = \frac{60.4\ k\Omega}{\left(\frac{5V}{1.238V} - 1\right)} = 19.87\ k\Omega \cong 20\ k\Omega \quad (6)$$

The output voltage is limited by the maximum duty cycle as well as the minimum on time. Figure 19 shows the limits for input and output voltages. The recommended maximum output voltage is approximately 1V less than the nominal input voltage. At 30V input, the minimum output is approximately 2.3V and the maximum is approximately 27V. For input voltages below 5.5V, VLIN5 must be connected to VIN through a small resistor (approximately 4.7Ω). Doing this ensures that VLIN5 does not fall below the UVLO threshold.

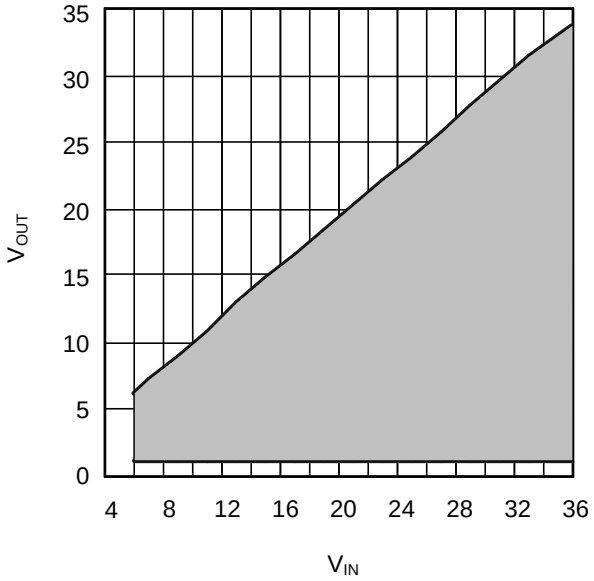


Figure 19. Available Output Voltage Range

Output Capacitor Selection

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple (ΔV_{OUT}) often results in fewer design iterations.

ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient (ΔV_{TRANS}) is:

$$\Delta V_{TRANS} = (\delta\% - \varepsilon\%) \times V_{OUT} - \frac{1}{2}\Delta V_{OUT} \quad (7)$$

where

- $\delta\%$ is the output voltage regulation window, $\varepsilon\%$ is the output voltage initial accuracy V_{OUT} is the nominal output voltage, and ΔV_{OUT} is the output voltage ripple.

Example: V_{OUT} = 5V, $\delta\%$ = 7%, $\varepsilon\%$ = 3.4%, ΔV_{OUT} = 40 mV peak-to-peak.

$$\Delta V_{TRANS} = (7\% - 3.4\%) \times 5V - \frac{40\ mV}{2} = 160\ mV. \quad (8)$$

Since the ripple voltage is included in the calculation of ΔV_{TRANS}, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, ΔI_{TRANS}.

MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (R_{esr}) is too high, the load transient requirement is not met, no matter how large the capacitance. The maximum allowed total combined ESR is:

$$R_{ESR\_MAX} = \frac{\Delta V_{TRANS}}{\Delta I_{TRANS}} \quad (9)$$

Example: ΔV_{TRANS} = 160mV, ΔI_{TRANS} = 3A. Then R_{esr_max} = 53.3mΩ.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{MIN} = \frac{L \times \left[\Delta V_{TRANS} - \sqrt{(\Delta V_{TRANS})^2 - (\Delta I_{TRANS} \times R_{ESR})^2}\right]}{V_{OUT} \times R_{ESR}^2} \quad (10)$$

Notice it is already assumed the total ESR, R_{esr}, is no greater than R_{esr_max}, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be calculated before C_{MIN} and after R_{esr} (see Inductor Selection section). Example: R_{esr} = 20mΩ, V_{OUT} = 5V, ΔV_{TRANS} = 160mV, ΔI_{TRANS} = 3A, L = 8µH

$$C_{MIN} = \frac{8\ \mu H \times \left[160\ mV - \sqrt{(160\ mV)^2 - (5A \times 20\ m\Omega)^2}\right]}{5 \times (20\ m\Omega)^2} = 140\ \mu F. \quad (11)$$

Generally speaking, C_{MIN} decreases with decreasing R_{esr}, ΔI_{TRANS}, and L, but with increasing V_{OUT} and ΔV_{TRANS}. The output capacitance can therefore be chosen to be slightly larger than the calculated value so that it is more easily available. Here we would likely be fine choosing 220 µF.

Inductor Selection

The size of the output inductor can be determined from the desired output ripple voltage, ΔV_{OUT}, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times V_{IN}} \times \frac{V_{OUT} \times R_{ESR}}{\Delta V_{OUT}} \quad (12)$$

In the above equation, R_{esr} is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to R_{esr}. In the case of ceramic capacitors, replace R_{esr} with the true impedance.

Example: V_{IN_MAX} = 36V, V_{OUT} = 5.0V, ΔV_{OUT} = 40 mV, R_{esr} = 20 mΩ, f_{SW} = 300 kHz,

$$L_{MIN} = \frac{36V - 5.0V}{300\ kHz \times 36V} \times \frac{5.0V \times 20\ m\Omega}{40\ mV}$$

$$= 7.17\ \mu H \quad (13)$$

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load transient requirements should be considered. If an inductance value larger than L_{MIN} is selected, make sure that the C_{MIN} requirement is not violated.

Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times L} \times D$$

where

- D is the duty cycle, defined by V_{OUT}/V_{IN} (14)

Also important is the ripple current, which is defined by $\Delta I_L / I_{NOM}$., where I_{NOM} is the nominal output current. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content causes excessive losses in the inductor.

Example: V_{IN} = 12V, V_{OUT} = 5.0V, f_{SW} = 300 kHz, L = 8 µH

$$\Delta I_L = \frac{12V - 5.0V}{300\ kHz \times 8\ \mu H} \times \frac{5.0V}{12V} = 1.22A \quad (15)$$

Given a maximum load current of 5A, the ripple content is 1.2A / 5A = 24%. When choosing an inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

Input Capacitor Selection

The input capacitor must be selected such that it can handle both the maximum ripple RMS current at highest ambient temperature and the maximum input voltage. The equation for the RMS current through the input capacitor is then

$$I_{IRMS} = I_{MAX} \sqrt{D(1-D)}$$

where

- I_{MAX} is maximum load current and D is the duty cycle. (16)

Example: I_{MAX} = 5A and D = 0.42

$$I_{IRMS} = 5A \sqrt{0.42 \times (1 - 0.42)} = 2.46A \quad (17)$$

The function D(1-D) has a maxima at D = 0.5. This duty cycle corresponds to the maximum RMS input current that may be used as a worst case in selecting an input capacitor. Input capacitors must meet the minimum requirements of voltage and ripple current capacity. The size of the capacitor should then be selected based on hold up time requirements. Bench testing for individual applications is still the best way to determine a reliable input capacitor value. The input capacitor should always be placed as close as possible to the current sense resistor or the drain of the top FET.

MOSFET Selection

BOTTOM FET SELECTION

During normal operation, the bottom FET is switching at almost zero voltage and therefore only conduction losses are present in the bottom FET. This makes the on resistance (R_{dson}) the most important parameter when selecting the bottom FET; the lower the on resistance, the lower the power loss. The bottom FETs' power losses peak at the maximum input voltage and load current. The equation for the maximum allowable on resistance at room temperature for a given FET package, is:

$$R_{dson\_max} = \frac{1}{I_{MAX}^2 \times \left(1 - \frac{V_{OUT}}{V_{IN\_MAX}}\right)} \times \frac{T_{J\_MAX} - T_{A\_MAX}}{\left[1 + T_C \times (T_{J\_MAX} - 25°C)\right] \times R_{\theta JA}}$$

where

- T_{J_MAX} is the maximum allowed junction temperature in the FET.
- T_{A_MAX} is the maximum ambient temperature, $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the FET.
- T_C is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/°C. (18)

If the calculated R_{dson_max} is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the I_{MAX} term in the above equation, thus reducing R_{dson}. When using two FETs in parallel, multiply the calculated R_{dson_max} by 4 to obtain the R_{dson_max} for each FET. In the case of three FETs, multiply by 9.

Example: T_{J_MAX} = 100°C, T_{A_MAX} = 60°C, $R_{\theta JA}$ = 60°C/W, V_{IN_MAX} = 36V, V_{OUT} = 5V, and I_{MAX} = 5A

$$R_{dson\_max} = \frac{1}{(5A)^2 \times \left(1 - \frac{5V}{36V}\right)} \times \frac{100°C - 60°C}{\left[1 + 0.01/°C \times (100°C - 25°C)\right] \times 60°C/W} = 17.7\ m\Omega \quad (19)$$

If the selected FET has an R_{dson} value higher than 17.7Ω, then two FETs with an R_{dson} less than 30mΩ can be used in parallel. In this case, the temperature rise on each FET will not go to T_{J_MAX} because each FET is now dissipating only half of the total power.

TOP FET SELECTION

The output resistance for the top FET driver is 3.1Ω (maximum). The bias voltage is developed by an external bootstrap supply circuit, which is comprised of a diode and a capacitor. Before selecting the top FET, it is recommended to select the driving voltage for the bootstrap circuit first (see more in the Bootstrap Component Selection section).

If VLIN5 is chosen to drive the bootstrap circuit, care must be taken to ensure that the gate threshold voltage of the top FET is less than 3V (maximum). The top FET starts to turn on when the input voltage exceeds the threshold voltage of the UVLO, which has a minimum threshold of 3.8V. In this case, VLIN5 follows at approximately 3.8V also and thus the bias voltage to the top FET driver is about 3V after the bootstrap diode.

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

$$R_{dson\_max} = \frac{V_{IN\_MIN} \times 0.4}{I^2_{MAX} \times V_{OUT}} \times \frac{T_{J\_MAX} - T_{A\_MAX}}{\left[1 + T_C \times (T_{J\_MAX} - 25^{\circ}C)\right] \times R_{\theta JA}} \quad (20)$$

Example: T_{J_MAX} = 100°C, T_{A_MAX} = 60°C, $R_{\theta JA}$ = 60°C/W, V_{IN_MIN} = 5.5V, V_{NOM} = 5V, and I_{MAX} = 5A.

$$R_{DSON\_MAX} = \frac{5.5V \times 0.4}{(5A)^2 \times 5V} \times \frac{100^{\circ}C - 60^{\circ}C}{\left[1 + 0.01/^{\circ}C \times (100^{\circ}C - 25^{\circ}C)\right] \times 60^{\circ}C/W} = 6.7\ m\Omega \quad (21)$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

BOOTSTRAP COMPONENT SELECTION

Selection of the bootstrap components can be done after top FET and driving voltage are chosen. V_{LIN5} or another supply such as input may be used as the driving voltage. Once chosen, the bootstrap components can be selected .

Typically a 0.1µF ceramic (X5R, X7R) works well.

Any suitably sized Schottky diode works well for the bootstrap Diode. If excessive leakage current is seen, the a larger bootstrap capacitance may be needed .

Loop Compensation

The purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is usually checked to determine small-signal performance. Loop gain is equal to the product of the control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking, it is a good idea to have a loop gain slope that is -20dB/decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency. The higher the bandwidth, the faster the load transient response speed unless duty cycle saturates during a load transient. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain is relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot. As shown in Figure 20, the control-output transfer function consists of one pole (f_p), one zero (f_z), and a double pole at f_n (half the switching frequency). The following can be done to create a -20dB/decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at f_p, the second pole at f_z, and the second zero at f_n. The resulting output-control transfer function is shown in Figure 21.

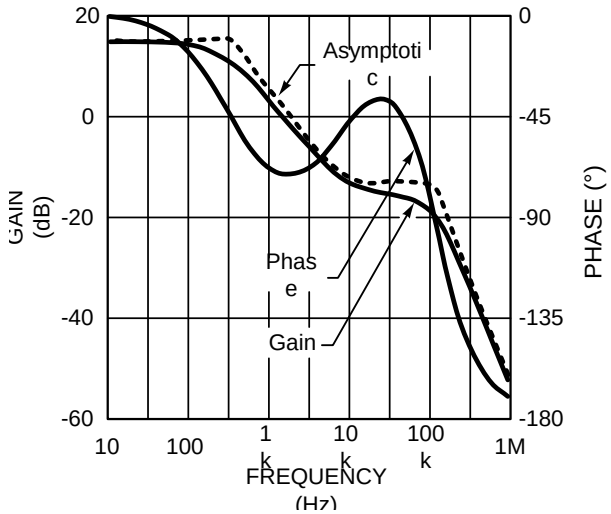


Figure 20. Control-Output Transfer Function

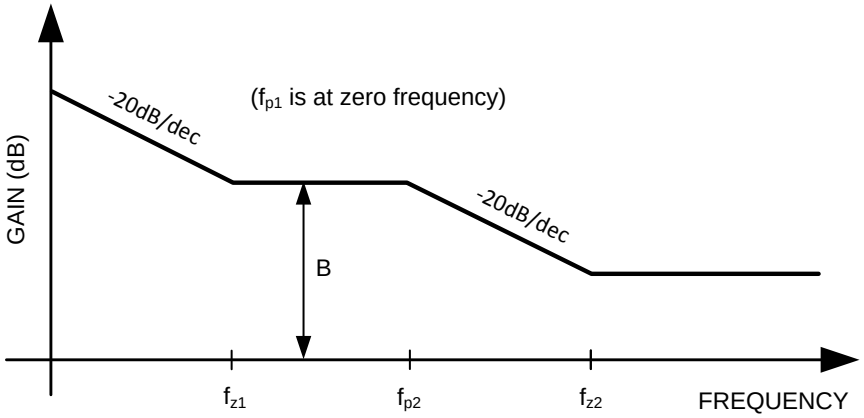


Figure 21. Output-Control Transfer Function

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_Z = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (22)$$

$$f_P = \frac{1}{2\pi R_O C_O} + \frac{0.5}{2\pi L f_{SW} C_O} \quad (23)$$

Since f_p is determined by the output network, it shifts with loading (R_o) and duty cycle. First determine the range of frequencies ($f_{pmin/max}$) of the pole across the expected load range and then place the first compensation zero within that range.

Example: R_{esr} = 20mΩ, C_o = 100uF, R_{omax} = 5V/100mA=50Ω, R_{omin} = 5V/5A = 1Ω, L = 8 µH.

$$f_Z = \frac{1}{2\pi \times 20m\Omega \times 220\,\mu F} = 36\ kHz \quad (24)$$

$$f_{PMIN} = \frac{1}{2\pi \times 50\Omega \times 220\,\mu F} + \frac{0.5}{2\pi \times 300\,kHz \times 8\,\mu H \times 220\,\mu F} = 165\ Hz \quad (25)$$

$$f_{PMAX} = \frac{1}{2\pi \times 1\Omega \times 220\,\mu F} + \frac{0.5}{2\pi \times 300\,kHz \times 8\,\mu H \times 220\,\mu F} = 874\ Hz \quad (26)$$

Once the f_p range is determined, R_{c1} should be calculated using:

$$R_{C1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right) \times 10^3 \quad (27)$$

where

- B is the desired gain in V/V at f_p (f_{z1}), gm is the transconductance of the error amplifier, and R_1 and R_2 are the feedback resistors.

A gain value around 10dB (3.3V/V) is generally a good starting point.

Example: B = 3.3 V/V, gm = 0.650 µmho, R_1 = 20 kΩ, R_2 = 60.4 kΩ:

$$R_{c1} = \frac{3.3}{0.650}\left(\frac{20\,k\Omega + 60.4\,k\Omega}{20\,k\Omega}\right) = 20.4\,k\Omega \cong 20\,k\Omega \quad (28)$$

Bandwidth varies proportionally to the value of R_{c1}. Next, C_{c1} can be determined with the following equation :

$$C_{c1} = \frac{1}{2\pi \cdot f_{p\ min} \cdot R_{c1}} \quad (29)$$

Example: fpmin = 313Hz, R_{c1} = 20kΩ:

$$C_{c1} = \frac{1}{2\pi \times 165\ Hz \times 20\ k\Omega} = 48\ nF \cong 47\ nF \quad (30)$$

The value of C_{c1} should be within the range determined by $f_{pmin/max}$. A higher value generally provides a more stable loop, but too high a value slows the transient response time.

The compensation network also introduces a low frequency pole that is close to 0Hz. A second pole should also be placed at f_z. This pole can be created with a single capacitor C_{c2} and a shorted R_{c2} (see Figure 22). The minimum value for this capacitor can be calculated by:

$$C_{c2\ min} = \frac{1}{2\pi \cdot f_z \cdot R_{c1}} \quad (31)$$

C_{c2} may not be necessary, however it does create a more stable control loop. This is especially important with high load currents and in current sharing mode.

Example: f_z = 36kHz, R_{c1} = 20kΩ:

$$C_{C2MIN} = \frac{1}{2\pi \times 36\,kHz \times 20\,k\Omega} = 221\,pF \quad (32)$$

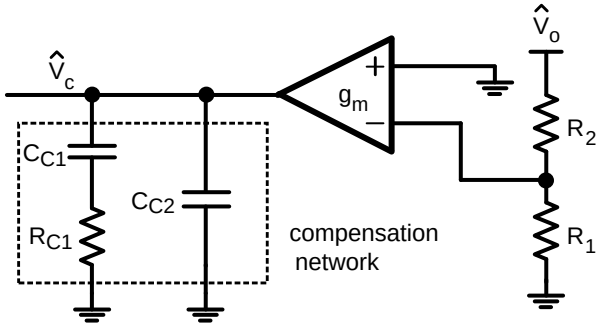


Figure 22. Compensation Network

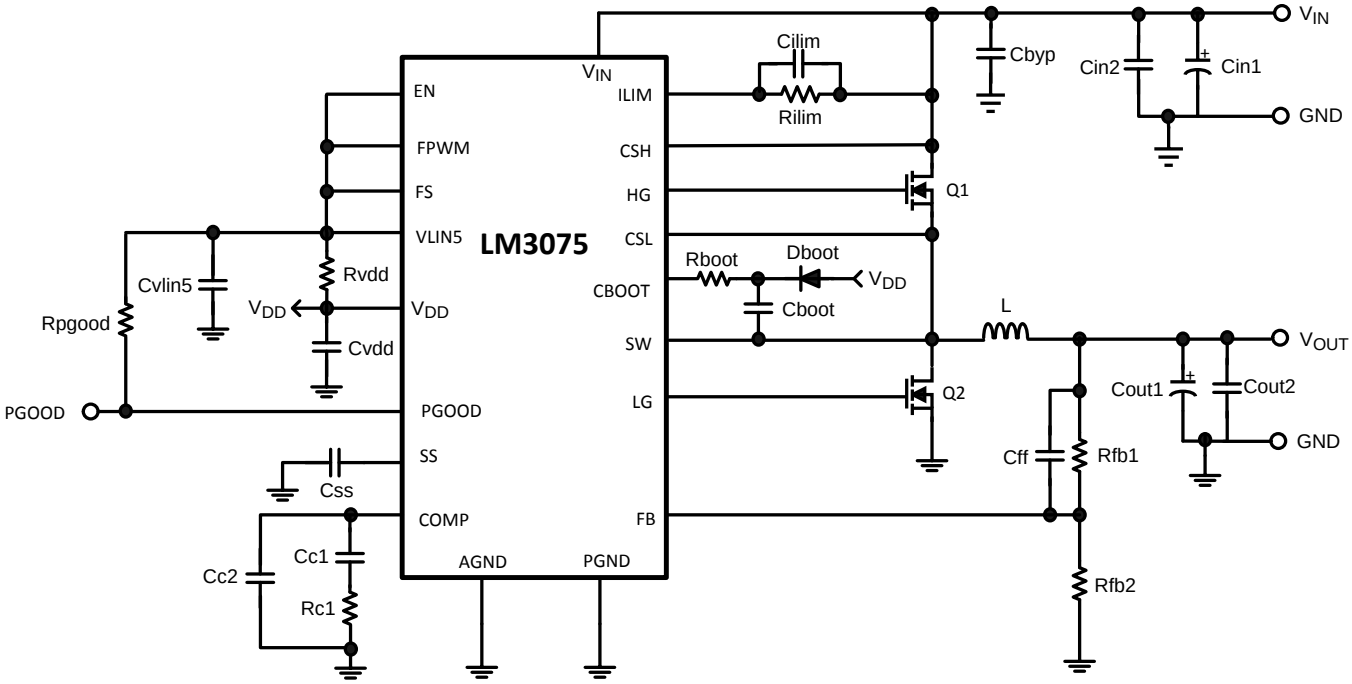


Figure 23. Typical Application Circuit

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	22

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265