LP5520 RGB Backlight LED Driver

Check for Samples: LP5520

FEATURES

- **Temperature Compensated LED Intensity and Color**
- **Individual Calibration Coefficients for Each Color**
- **Color Accuracy ΔX and ΔY ≤ 0.003**
- **12 Bit ADC for Measurement of 2 Sensors**
- **Adjustable Current Outputs for R, G and B LED**
- **0.2% Typical LED Output Current Matching**
- **PWM Control Inputs for Each Color**
- **SPI and I²C Compatible Interface**
- **Stand-Alone Mode with 1 Wire Control**
- **Sequential Mode for One Color at a Time**
- **Magnetic High Efficiency Boost Converter**
- **Programmable Output Voltage from 5V to 20V**
- **Adaptive Output Voltage Control Option**
- **< 2 µA Typical Shutdown Current**
- **DSBGA-25 Package, 2.77 × 2.59 × 0.6mm**

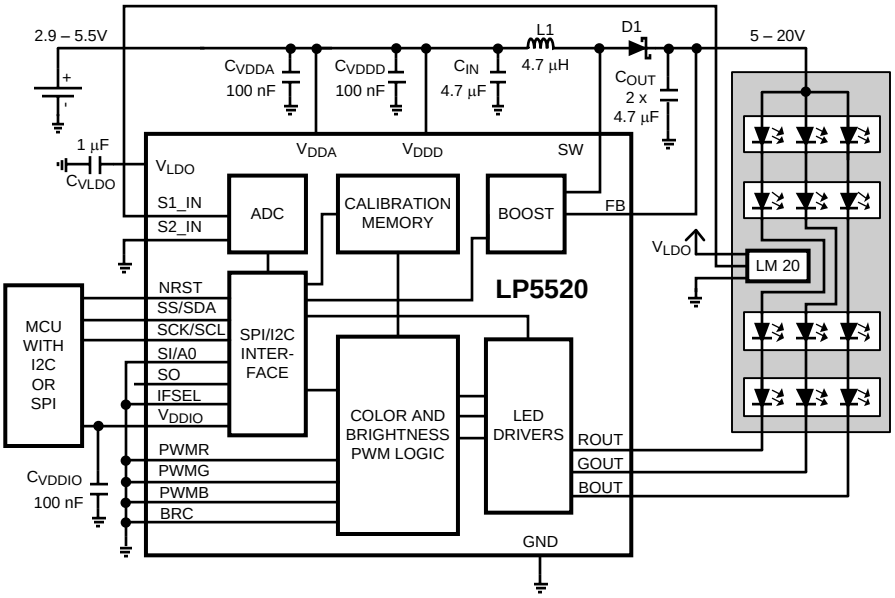
APPLICATIONS

- **Color LCD Display Backlighting**
- **LED Lighting Applications**
- **Non-Linear Temperature Compensation**
- **Ambient Light Compensation**

DESCRIPTION

The LP5520 is an RGB backlight LED driver for small format color LCDs. RGB backlight enables better colors on the display and power savings compared with white LED backlight. LP5520 offers small and simple driver solution without need for optical feedback. Calibration in display module production can be done in one temperature. LP5520 produces true white light over wide temperature range. Three independent LED drivers have accurate programmable current sinks and PWM modulation control. Using internal calibration memory and external temperature sensor, the RGB LED currents are adjusted for perfect white balance independent of the brightness setting or temperature. The user programmable calibration memory has intensity vs. temperature data for each color. This white balance calibration data can be programmed to the memory on the production line of a backlight module.

Typical Application



DESCRIPTION (CONTINUED)

The device has a magnetic boost converter that creates up to 20V LED supply voltage from the battery voltage. The output can be set at 1V step from 5V to 20V. In adaptive mode the circuit automatically adjusts the output voltage to minimum sufficient level for lowest power consumption.

Temperature is measured using an external temperature sensor placed close to the LEDs. The second ADC input can be used e.g. for ambient light measurement.

LP5520 is available in a 25-pin DSBGA package.

Connection Diagrams

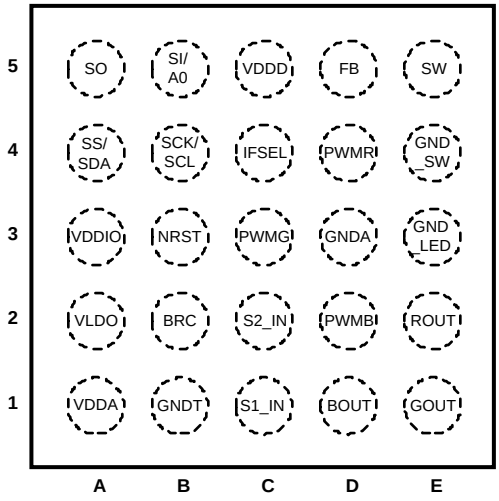


Figure 1. DSBGA-25 Package, Large Bump Top View
Package Number YZR0025EMA

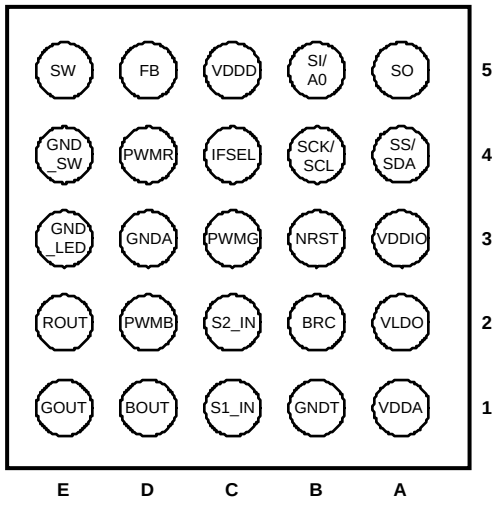


Figure 2. DSBGA-25 Package, Large Bump Bottom View
Package Number YZR0025EMA

PIN DESCRIPTIONS

Pin	Name	Type	Description
5E	SW	Output	Boost Converter Power Switch
5D	FB	Input	Boost Converter Feedback
5C	VDDD	Power	Supply Voltage for Digital Circuitry
5B	SI/A0	Logic Input	Serial Input (SPI), Address Select (I^2C)
5A	SO	Logic Output	Serial Data Out (SPI)
4E	GND_SW	Ground	Power Switch Ground
4D	PWMR	Logic Input	PWM control for Output R
4C	IFSEL	Logic Input	Interface Selection (SPI or I^2C compatible, IF_SEL = 1 for SPI)
4B	SCK/SCL	Logic Input	Clock (SPI/I^2C)
4A	SS/SDA	Logic Input/Output	Slave Select (SPI), Serial Data In/Out (I^2C)
3E	GND_LED	Ground	Ground for LED Currents
3D	GNDA	Ground	Ground for Analog Circuitry
3C	PWMG	Logic Input	PWM control for Output G
3B	NRST	Logic Input	Master Reset, Active Low
3A	VDDIO	Power	Supply Voltage for Input/output Buffers and Drivers
2E	ROUT	Output	Red LED Output
2D	PWMB	Logic Input	PWM control for Output B
2C	S2_IN	Input	ADC input 2, input for optional second sensor
2B	BRC	Logic Input	Brightness Control for All LED Outputs, Pseudo-PWM
2A	VLDO	Power	Internal LDO Output
1E	GOUT	Output	Green LED Output
1D	BOUT	Output	Blue LED Output
1C	S1_IN	Input	ADC input 1, input for temperature sensor
1B	GNDT	Ground	Ground/Test
1A	VDDA	Power	Supply Voltage for Analog Circuitry

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V (SW, FB, ROUT, GOUT, BOUT)	-0.3V to 22V
V_{DDA}, V_{DDD}, V_{DDIO}, V_{LDO}	-0.3V to 6.0V
Voltage on Logic Pins	-0.3V to V_{DDIO} 0.3V with 6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	125°C
Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering) (5)	
ESD Rating (6)	
Human Body Model:	2 kV
Machine Model:	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typ.) and disengages at T_J=140°C (typ.).
(5) For detailed soldering specifications and information, please refer to Note AN-1112 : DSBGA Wafer Level Chip Scale Package (SNVA009)
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1) (2)

V (SW, FB, MAIN, SUB)	0 to 21V
$V_{DDA,DDD}$	2.9 to 5.5V
V_{DDIO}	1.65V to V_{DDA}
Recommended Load Current (ROUT, GOUT, BOUT)	0 mA to 60 mA /driver
Junction Temperature (T_J) Range	-30°C to 125°C
Ambient Temperature (T_A) Range (3)	-30°C to 85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance(θ_{JA}), YZR0025EMA Package (1)	60 - 100°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

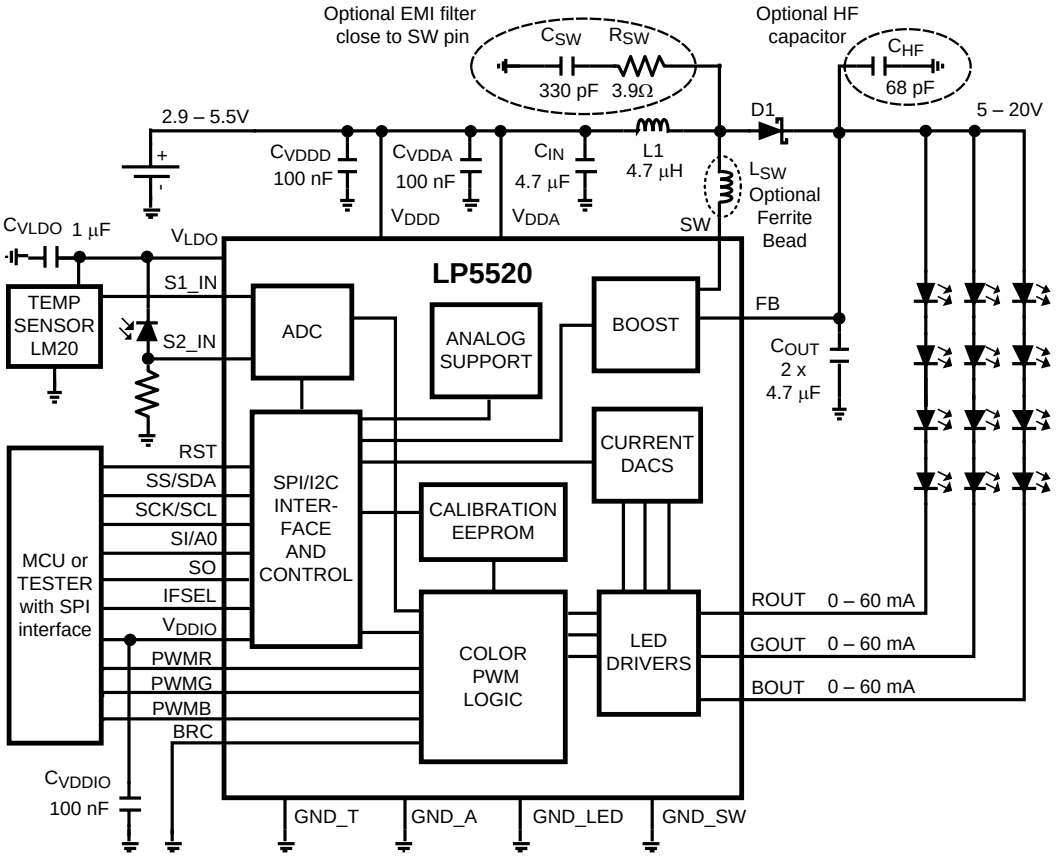
Electrical Characteristics (1)(2)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (-30°C < T_J < 85°C). Unless otherwise noted, specifications apply to the LP5520 Block Diagram with: $C_{VDDA/D}$ = 100 nF, C_{OUT} = 2 x 4.7 µF/ 25V, C_{IN}= 10 µF / 6.3V, L1 = 4.7 µH (3).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{VDD}	Standby supply current (V_{DDA} + V_{DDD})	NSTBY = L, V_{DDIO} ≥ 1.65V		1.7	**7**	µA
		NSTBY = L , V_{DDIO} = 0V		1		µA
	No-boost supply current (V_{DDA} + V_{DDD})	NSTBY = H, EN_BOOST = L		0.9		mA
	No-load supply current (V_{DDA} + V_{DDD})	NSTBY = H, EN_BOOST = H AUTOLOAD = L		1.4		mA
I_{VDDIO}	V_{DDIO} Standby Supply current	NSTBY = L			**1**	µA
V_{LDO}	Internal LDO output voltage	V_{IN} ≥ 2.9V	2.77	2.80	2.84	V
I_{LDO}	Internal LDO output current	Current to external load			**1**	mA

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers represent the most likely norm.
(3) Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

BLOCK DIAGRAM



MODES OF OPERATION

LP5520 has three different operating modes: Manual mode, Automatic mode and Stand-Alone mode. The Automatic mode has two sub modes, normal mode and sequential mode. In manual and automatic modes the chip is controlled through the serial interface. In standalone mode only BRC input needs to be controlled and all registers have the default values.The modes are controlled according to the following table.

<RGB_auto> (RBG control bit 3)	**<seq_mode[0:1]>** (RBG control bits 6 and 7)	**LP5520 Operating Mode**
0	**00**	Manual mode
1	**00**	Automatic mode, normal operation (overlapping)
1	**01, 10 or 11**	Automatic mode, sequential operation with 2, 3 or 4 pulses per sequence

MANUAL MODE

In the manual mode the automatic LED intensity adjustment is not in use. The internal PWM control is disabled and the LEDs are driven with DC current. The user can set the LED currents through the serial port using three Current Control registers, **current_control_R/G/B**, and use the external PWM control inputs to adjust LED intensities if needed. There is an independent PWM control pin for each output. If PWM control is not used, the PWMR, PWMG and PWMR inputs should be tied to the V_{DDIO}. All the functions implemented with the internal PWM control are unavailable in manual mode (logarithmic brightness control from PWM Control register, temperature compensation, fading, sequential mode).

AUTOMATIC MODE

In the automatic mode the LED intensities are controlled with the 12-bit PWM values obtained from the EEPROM memory according to the temperature information. PWM values are stored at 16°C intervals for the –40 to 120°C temperature range, and the PWM values for the intermediate temperatures are linearly interpolated.

When creating white light from a RGB LED, the intention is to program PWM values, which keep the individual LED intensities constant in all temperatures. For possible other applications, other kind of PWM behavior can be programmed, and also the variable can be other than temperature if the sensor is changed to e.g. a light sensor.

12-bit ADC is used for the measurements. The ADC has two inputs S1_IN and S2_IN. The temperature measurement result from the S1_IN input is converted to EEPROM address using the sensor calibration data from EEPROM. This EEPROM address is then used to get the PWM values for each output. The second input S2_IN can be used for example for ambient light measurement. The ADC data from selected input can be read through the serial interface. Control bit **<comp_sel>** can be used to select which input is used for compensation.

Current setting for each LED comes from EEPROM in the automatic mode. The same current values should be programmed as were used in the calibration. Current control range is from 0 to 60 mA with 8-bit resolution and the step size is 235 µA.

Common Brightness Control for all LEDs can be done using the pwm_brightness (05H) register. The **pwm_brightness register** makes 8 level logarithmic brightness control with 3 bits. An automatic fade function makes possible smooth turn-on, turn-off and brightness changes of the LEDs. White balance is maintained during fading.

A brightness correction value can be given for each LED. The PWM value obtained from the EEPROM memory will be multiplied by this correction value. This feature can be used for example for LED aging compensation or for color adjustment by user. These values are kept in **R_correction** (0AH), **G_correction** (0BH) and **B_correction** (0CH) registers. The correction multiplier can be between 0 and 2.

Due to LED self-heating, the temperature sensor and the LED temperatures will differ. The difference depends on the thermal structure of the display module and the distance between the sensor and the LEDs. This temperature difference can be compensated by storing the temperature difference value at highest power (100% red LED PWM) in the EEPROM memory. The system then corrects the measured temperature based on the actual PWM value used. The correction assumes that the red LED PWM value is representing the whole RGB LED power consumption.

Sequential (non-overlapping) drive is possible using external PWM control inputs to trigger a new sequence in each LED output. 60 mA maximum current setting makes possible 20 mA maximum averaged current for each output in the non-overlapping mode.

STAND-ALONE MODE

In stand-alone mode the operation is controlled through a single PWM brightness input, BRC. After power-up or reset the LP5520 is ready for stand-alone operation without any setup through the serial interface. The stand-alone mode is entered with a rising edge in the BRC input. The boost converter will operate in adaptive mode. The LED current settings are read from EEPROM. The LED brightness is controlled with a PWM signal in the BRC input. The BRC PWM frequency should be between 2 and 10 kHz. The PWM signal in the BRC input is not used as such for the LED outputs, but it is converted to 3-bit value and a logarithmic brightness control is based on this 3-bit value, as shown in the following table. There is hysteresis in the conversion to avoid blinking when the BRC duty cycle is close to a threshold. When the PWM pulses end in the BRC input and the input stays low, the circuit will go to the stand-by mode.

The following picture shows the waveforms in BRC input and ROUT output in the stand-alone mode. The circuit is in stand-by mode until the first rising edge in BRC input is detected. The circuit starts up and the outputs activate after 30 ms from the first rising edge in BRC. The BRC frequency is assumed to 2 kHz in this example giving 0.5 ms BRC period. When the duty cycle changes in BRC, it takes two BRC periods before the change is reflected in the output. When BRC goes permanently low, the circuit will enter stand-by mode after 15 ms from the last BRC pulse.

All controls through the serial interface can be used in the stand-alone mode. The stand-alone mode must be inhibited in automatic and manual modes by writing the control bit **<brc_off>** high and by keeping BRC input low.

BRC duty cycle threshold values (%)		Intensity (% of maximum)	Recommended BRC PWM control values	
increasing	**decreasing**		**increasing**	**decreasing**
	0	off		0
1	15	0.8	10	10
20	28	1.6	28	22
35	42	3.1	40	32
48	52	6.3	53	47
58	62	12.5	63	58
68	75	25	75	70
82	90	50	88	85
97		100	99	

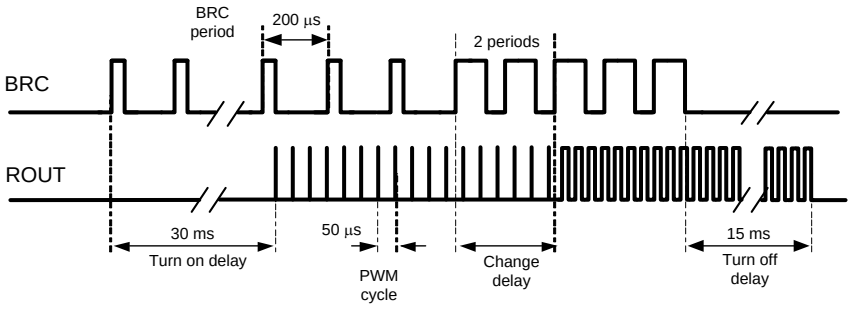


Figure 3. LP5520 control and output waveforms in stand-alone mode

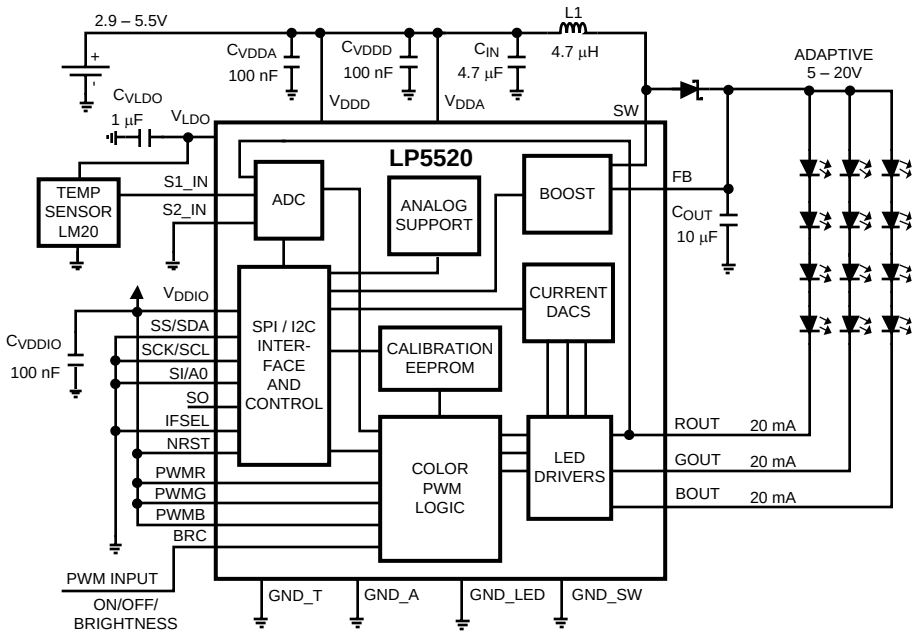


Figure 4. LP5520 connection in stand-alone mode

Start-Up

START-UP POWERING

V_{DDD} and V_{DDA} should be tied together and turned on first. V_{DDIO} must be turned on at the same time as V_{DDD} or later. In the power off sequence V_{DDIO} must be turned off before V_{DDD} or at the same time.

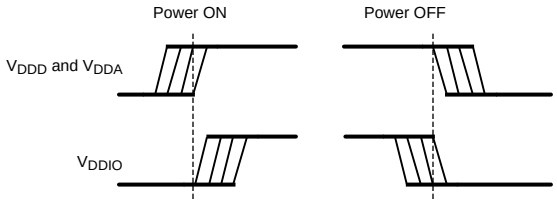


Figure 5. Power-on signal timing

START-UP SEQUENCE

RESET: In the RESET mode all the internal registers are reset to the default values and the chip goes to STANDBY mode after reset. <NSTBY> control bit is low after reset by default. Reset is entered always if NRST input is low or internal Power On Reset is active. Power On Reset (POR) will activate during the chip startup or when the supply voltage VDD falls below 1.5V. Once VDD rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode.

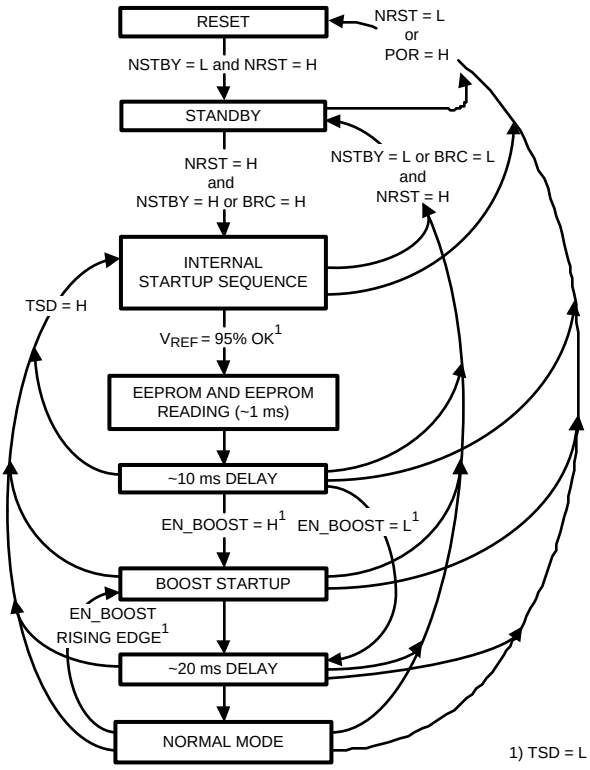
STANDBY: The STANDBY mode is entered if the register bit <NSTBY> is LOW. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after power up.

STARTUP: When <NSTBY> bit is written high or there is a rising edge in the BRC input, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (Vref, Bias, Oscillator etc..). To ensure the correct initialization, a 10 ms delay is generated by the internal state-machine after the trim EEPROM values are read. If the chip temperature rises too high, the Thermal Shutdown (TSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is

raised in PWM mode during the 20 ms delay generated by the state-machine. All LED outputs are off during the 20 ms delay to ensure smooth startup. The Boost startup is entered from Internal Startup Sequence if <EN_BOOST> is HIGH or from Normal mode when <EN_BOOST> is written HIGH.

NORMAL: During NORMAL mode the user controls the chip using the Control Registers or the BRC input in stand-alone mode. The registers can be written in any sequence and any number of bits can be altered in a register in one write.



RGB Driver Functionality

WHITE BALANCE CONTROL

LP5520 is designed to provide spectrally rich white light using a three color RGB LED. White light is obtained when the Red, Green and Blue LED intensities are in proper balance. The LED intensities change independently with temperature. For maintaining the purity of the white color and the targeted total intensity, precise temperature dependent intensity control for each LED is required. The color coordinates in this document refer to the CIE 1931 color graph (x,y system).

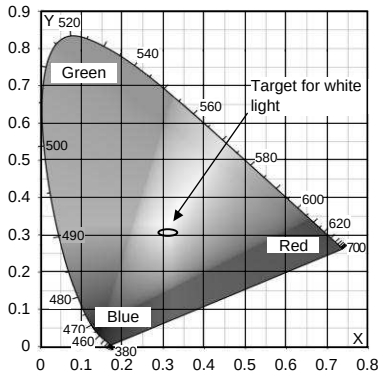


Figure 6. CIE 1931 Color Graph

The Intensity vs. Temperature graph shows a typical RGB LED intensity behavior on a 12-bit scale (0 to 4095) at constant 20mA LED currents. The next graph shows the typical color coordinate change for an uncompensated RGB LED. The Compensation PWM Values graph shows the corresponding PWM values for achieving constant intensity white light across the temperature range. The PWM values have been saturated at 104°C to avoid overheating the LED and to better utilize the PWM range. The white balance is not maintained above 104°C in this case.

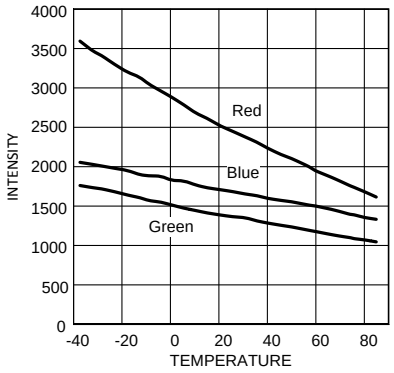


Figure 7. LED Intensity vs. Temperature

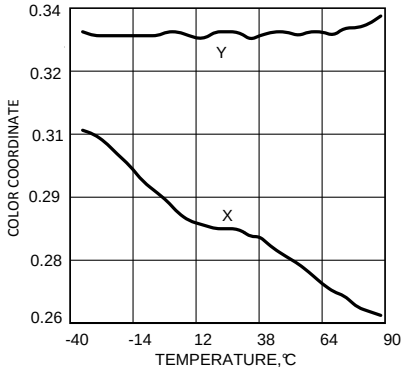


Figure 8. Typical Color Coordinates vs. Temperature for uncompensated RGB LED

The compensation values for the measured temperatures can be easily calculated when the intensity vs. temperature information is available. For the best accuracy the iterative calibration approach should be used. The calibration procedure is described in the Application Note AN1459, LP5520 RGB Backlight Driver Calibration.

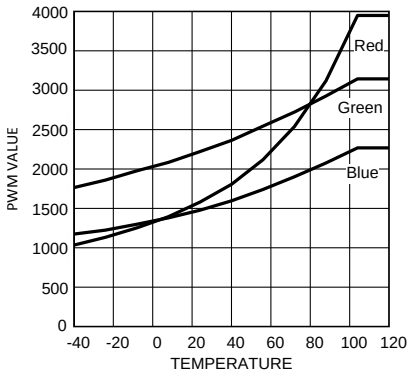


Figure 9. Compensation PWM Values

The compensation values need to be converted to 16°C intervals when they are programmed to the calibration EEPROM. The evaluation software has import function, which can be used to convert the measured compensation data to the 16°C interval format. The measured data can have any temperature points and the software will fit a curve through the measured points and calculate new PWM values in fixed temperatures using the curves. The procedure is explained in the Application Note AN1462, LP5520 RGB Backlight Driver Evaluation Kit. By using the evaluation software to convert the measurement results to EEPROM memory map the user does not need to care about the details of the EEPROM structure.

Typical color coordinate and intensity stability over temperature are shown in the following two graphs.

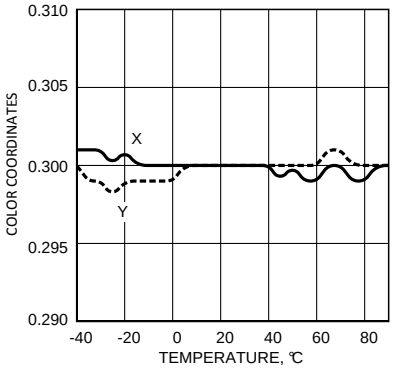


Figure 10. Compensated Color Coordinates vs. Temperature

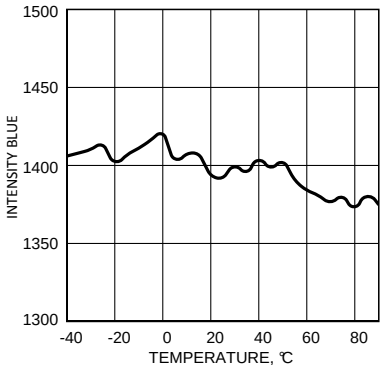


Figure 11. Compensated Blue LED Intensity vs. Temperature

CALIBRATION MEMORY

The 1 kbit calibration EEPROM memory is organized as 128 x 8 bits. It stores the 12-bit calibration PWM values for each output at 16°C intervals. 10 temperature points are used to cover the range from –40 to 120°C. The temperature or light sensor calibration data, self heating factor and LED currents are also stored in the memory. The memory contents and detailed memory map are shown in the following tables.

Table 1. The EEPROM contents

Data	Length	Total bits
10 PWM values for red	12	120
10 coefficients for red between the points	8	80
10 PWM values for green	12	120
10 coefficients for green between the points	8	80
10 PWM values for blue	12	120
10 coefficients for blue between the points	8	80
0°C reading for temperature sensor	12	12
Coefficient for temperature sensor	12	12
Maximum self-heating (100% red PWM)	8	8
Default current for ROUT	8	8
Default current for GOUT	8	8
Default current for BOUT	8	8
Free memory for user data	8	368

Table 2. EEPROM memory map

Address	Bits [7:4]	Bits [3:0]	Definition	
00	RB0[7:0]		Base PWM-value for red (8 LSB bits)	-40...-25
01	RB1[7:0]			-24...-9
02	RB2[7:0]			-8...+7
03	RB3[7:0]			+8...+23
04	RB4[7:0]			+24...+39
05	RB5[7:0]			+40...+55
06	RB6[7:0]			+56...+71
07	RB7[7:0]			+72...+87
08	RB8[7:0]			+88...+103
09	RB9[7:0]			From +104
0a	GB0[7:0]		Base PWM-value for green (8 LSB bits)	-40...-25
0b	GB1[7:0]			-24...-9
0c	GB2[7:0]			-8...+7
0d	GB3[7:0]			+8...+23
0e	GB4[7:0]			+24...+39
0f	GB5[7:0]			+40...+55
10	GB6[7:0]			+56...+71
11	GB7[7:0]			+72...+87
12	GB8[7:0]			+88...+103
13	GB9[7:0]			From +104

Table 2. EEPROM memory map (continued)

Address	Bits [7:4]	Bits [3:0]	Definition	
14	BB0[7:0]		Base PWM-value for blue (8 LSB bits)	-40...-25
15	BB1[7:0]			-24...-9
16	BB2[7:0]			-8...+7
17	BB3[7:0]			+8...+23
18	BB4[7:0]			+24...+39
19	BB5[7:0]			+40...+55
1a	BB6[7:0]			+56...+71
1b	BB7[7:0]			+72...+87
1c	BB8[7:0]			+88...+103
1d	BB9[7:0]			From +104
1e	LM20K[7:0]		Scaling values for LM20 sensor	K
1f	LM20B[7:0]			B
20			Not used	
...				
3f				
40	RC0[7:0]		Coefficient PWM-value for red	-40...-25
41	RC1[7:0]			-24...-9
42	RC2[7:0]			-8...+7
43	RC3[7:0]			+8...+23
44	RC4[7:0]			+24...+39
45	RC5[7:0]			+40...+55
46	RC6[7:0]			+56...+71
47	RC7[7:0]			+72...+87
48	RC8[7:0]			+88...+103
49	RC9[7:0]			From +104
4a	GC0[7:0]		Coefficient PWM-value for green	-40...-25
4b	GC1[7:0]			-24...-9
4c	GC2[7:0]			-8...+7
4d	GC3[7:0]			+8...+23
4e	GC4[7:0]			+24...+39
4f	GC5[7:0]			+40...+55
50	GC6[7:0]			+56...+71
51	GC7[7:0]			+72...+87
52	GC8[7:0]			+88...+103
53	GC9[7:0]			From +104
54	BC0[7:0]		Coefficient PWM-value for blue	-40...-25
55	BC1[7:0]			-24...-9
56	BC2[7:0]			-8...+7
57	BC3[7:0]			+8...+23
58	BC4[7:0]			+24...+39
59	BC5[7:0]			+40...+55
5a	BC6[7:0]			+56...+71
5b	BC7[7:0]			+72...+87
5c	BC8[7:0]			+88...+103
5d	BC9[7:0]			From +104
5e	SHF[7:0]		Self heating factor	
5f	RED_CUR		Red LED current	

Table 2. EEPROM memory map (continued)

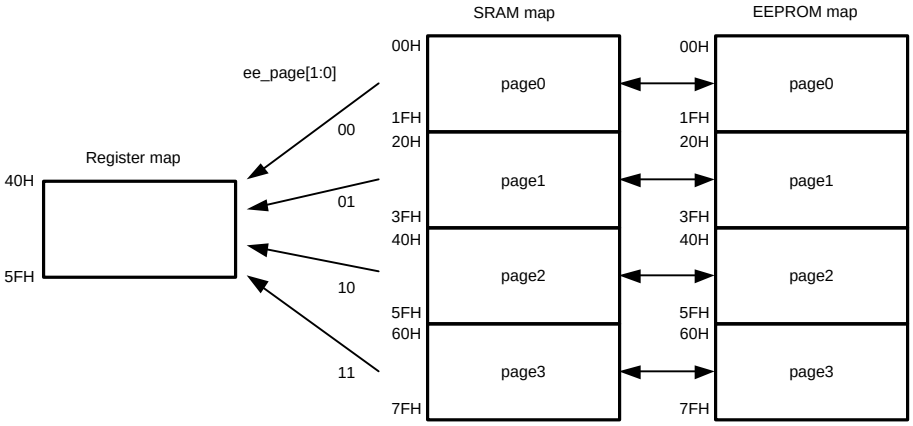
Address	Bits [7:4]	Bits [3:0]	Definition
60	GREEN_CUR		Green LED current
61	BLUE_CUR		Blue LED current
62			Not used
...			
6f			
70	LM20B[11:8]	LM20K[11:8]	Scaling values for LM20 sensor
71	BB9[11:8]	BB8[11:8]	Base PWM-value for blue (high bits)
72	BB7[11:8]	BB6[11:8]	
73	BB5[11:8]	BB4[11:8]	
74	BB3[11:8]	BB2[11:8]	
75	BB1[11:8]	BB0[11:8]	
76	GB9[11:8]	GB8[11:8]	Base PWM-value for green (high bits)
77	GB7[11:8]	GB6[11:8]	
78	GB5[11:8]	GB4[11:8]	
79	GB3[11:8]	GB2[11:8]	
7a	GB1[11:8]	GB0[11:8]	
7b	RB9[11:8]	RB8[11:8]	Base PWM-value for red (high bits)
7c	RB7[11:8]	RB6[11:8]	
7d	RB5[11:8]	RB4[11:8]	
7e	RB3[11:8]	RB2[11:8]	
7f	RB1[11:8]	RB0[11:8]	

The EEPROM data can be read, written and erased through the serial interface. The boost converter is used to generate the write and erase voltage for the memory. All operations are done in page mode. The page address has to be written in the **EEPROM_control** register before access to the EEPROM. Incremental access can be used both in I2C and SPI modes to speed up access. During EEPROM access the **<rgb_auto>** control bit in **rgb control** register must be low.

The EEPROM has 4 pages; only one page at time can be mirrored at the register map. For getting access to page, the number of page must be set by **<ee_page[1:0]>** bits in the **EEPROM_control** register(0DH). The page register address range is from 40H to 5FH.

<ee_page[1:0]> (bits1-0)	**00**	page0 (00H-1FH)
	01	page1 (20H-3FH)
	10	page2 (40H-5FH)
	11	page3 (60H-7FH)

Actually the EEPROM consist of two type of memory, 128 x 8 EEPROM (Non Volatile Memory) and 128 x 8 SRAM (Synchronous Random Access Memory). The EEPROM is used to store calibrated RGB control values when the system is powered off. SRAM is used as working memory during operation.



EEPROM content is copied into SRAM always when the chip is taken from stand-by mode to active mode. Copying to SRAM can also be made during operation by writing the **<ee_read>** bit high and low in the **EEPROM control** (0DH) register. For reading the data from the SRAM, the page number must be set with **<ee_page[1:0]>** bits and the page read from addresses 40H – 5FH.

The EEPROM must be erased before programming. The erase command will erase one page at time, which must be selected with **<ee_page[1:0]>** bits. This operation starts after setting and resetting **<ee_erase>** and takes about 100 ms after rising **<ee_erase>** bit. During erasing **<ee_prog>** bit of the **EEPROM_CONTROL** register is low. Corresponding SRAM area will be erased with this operation also. **<ee_erase>** and **<ee_prog>** can be set only one command at a time (erase or program).

During programming the content of SRAM is copied to EEPROM. EEPROM programming cycle has two steps. At first, write the whole content of the SRAM, all 4 pages. The whole page can be written during one SPI/I^2C cycle in the auto-increment mode. Second step is programming the EEPROM. This operation starts after writing **<ee_prog>** high and back low and takes about 100 ms after rising **<ee_prog>** bit. During programming **<ee_prog>** bit of the **EEPROM_CONTROL** register is low. For EEPROM erasing and programming the chip has to be in active mode (**<NSTBY>** high), the boost must be off (**<in_boost>** low) and the boost voltage set to 18V (**boost output** register value 12H).

LED BRIGHTNESS CONTROL

The LED brightness is defined by two factors, the current through the LED and the PWM duty cycle. The constant current outputs ROUT, GOUT and BOUT can be independently set to sink between 0 and 60 mA. The 8-bit current control has 255 levels and the step size is 235 µA. In manual mode the current is defined with the **current control (R/G/B)** registers (01H, 02H and 03H). In automatic mode the current settings come from the EEPROM.

The PWM control has 12-bit resolution, which means 4095 steps. The minimum pulse width is 200 ns and the frequency can be set to either 1.2 kHz or 19.2 kHz. The duty cycle range is from 0 to 100% (0 to 4095). The output PWM value is obtained by multiplication of three factors. The first factor is the temperature-based value from the EEPROM. The second factor is the correction register setting, which is independent for each color. The third factor is the brightness register setting, which is common to all colors.

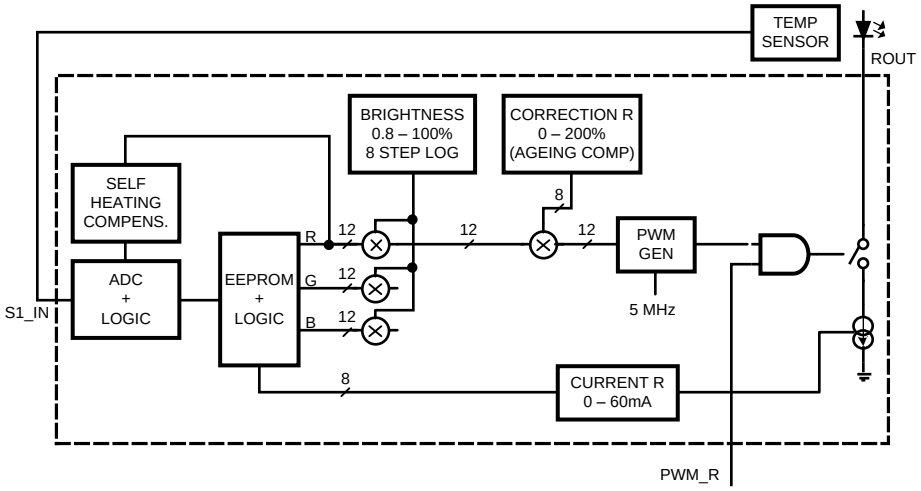
The temperature based PWM values are stored in the EEPROM at 16°C intervals starting from -40°C and ending to 120°C. PWM values for the temperatures between the stored points are interpolated.

LED brightness has 3-bit logarithmic control. The control bits are in the pwm_brightness (04H) register. The 3-bit value defines a multiplier for the 12-bit PWM value obtained from the memory according to the following table.

Control byte <bri[2:0]>(1)	Multiplier	Intensity %
0	0.008	0.8
1	0.016	1.6
2	0.031	3.1
3	0.063	6.3
4	0.125	12.5
5	0.250	25.0
6	0.500	50.0
7	1.000	100.0

(1) PWM Brightness register control

The brightness correction can be used for aging compensation or other fine-tuning. There is an 8-bit correction register for each output. The PWM value obtained from the memory is multiplied by the correction value. The default correction value is 1. Correction range is from 0 to 2 and the lsb is 0.78% (1/128).



Shown complete only for red channel

Figure 12. LED control principle

LED PWM CONTROL

The PWM frequency can be selected of two alternatives, slow and fast, with the control bit **<pwm_fast>**. The slow frequency is 1.2 kHz. In the fast mode the PWM frequency is multiplied by 16 and the frequency is 19.2 kHz. Fast mode is the default mode after reset. The single pulse in normal PWM is split in 16 narrow pulses in fast PWM. Higher frequency helps eliminate possible noise from the ceramic capacitors and it also reduces the ripple in the boost voltage. Minimum pulse length is 200 ns in both modes.

The PWM pulses of each output do not start simultaneously in order to avoid high current spike. Red starts in the beginning of the PWM cycle, Green is symmetric with the cycle center and Blue ends in the end of the cycle. For PWM values less than 33% for each output, the output currents are completely non-overlapping. With higher PWM values the overlapping increases.

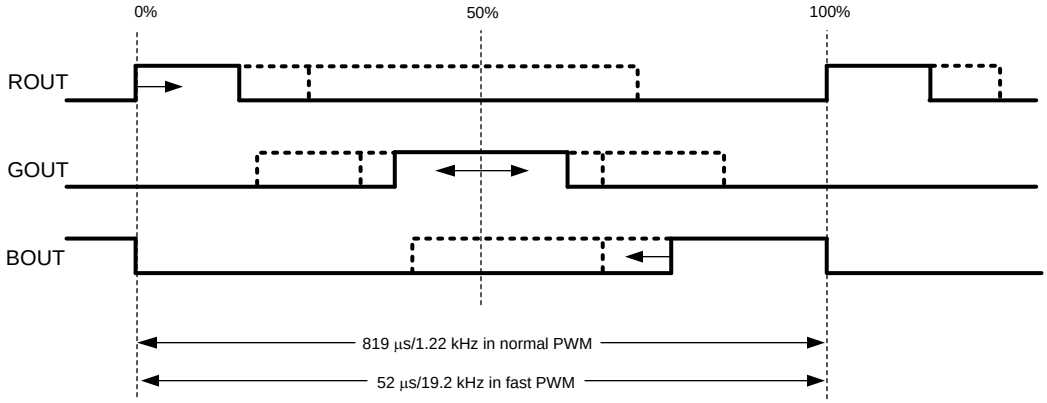


Figure 13. Pulse positions in the PWM cycle

SEQUENTIAL MODE

Completely non-overlapping timing can be obtained by using the sequential mode as shown in the graph below. The timing is defined with external PWM control inputs. The minimum trigger pulse width in the PWM inputs is 1 µs. There is no limitation on the maximum width of the pulse as long as it is shorter than the whole sequence.

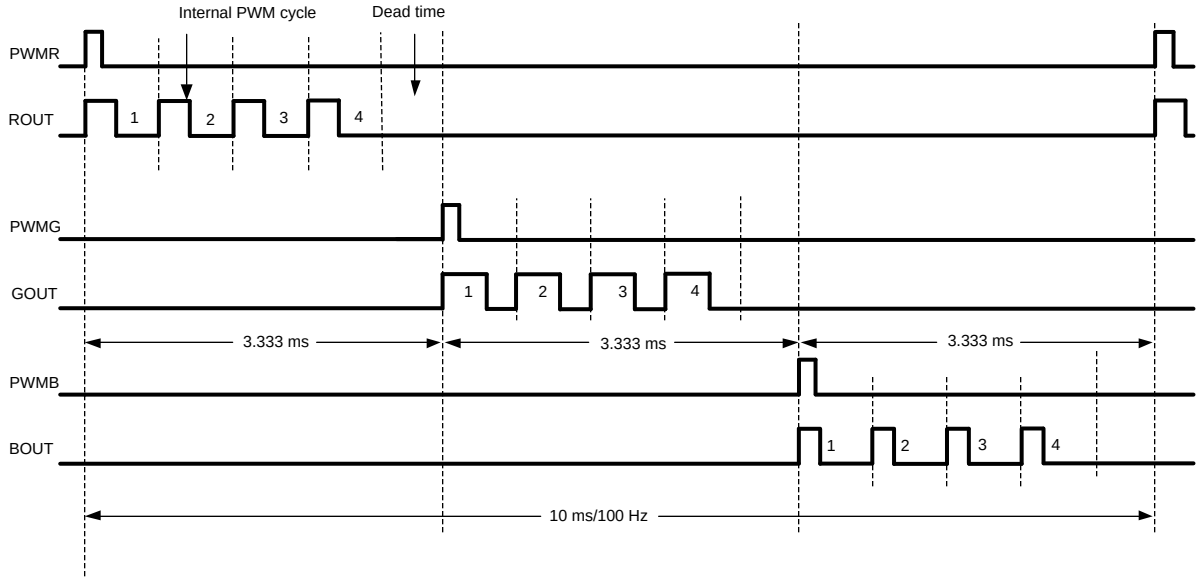


Figure 14. Non-overlapping external synchronized sequential mode

In sequential mode the PWM cycle is synchronized to trigger pulses and the amount of PWM pulses per trigger can be defined to 2, 3 or 4 using the **<seq_mode0>** and **<seq_mode1>** control bits. This makes possible to use sequence lengths of about 5 ms, 7.5 ms or 10 ms. Fast PWM can be used in sequential mode, but the frame timing is as with normal PWM.

The PWM timing and synchronization timing originate from different clock sources. Some margin should be allowed for clock tolerances. This margin shows as a dead time in the waveform graph. Some dead time should be allowed so that no PWM pulse will be clipped. Clipping would distort the intensity balance between the LEDs. The dead time will cause some intensity reduction, but will assure the current balance.

PWM mode defined by **<seq_mode1>** and **<seq_mode2>** control bits of **rgb_control** (00H) register:

<seq_mode1> (bit 7)	<seq_mode0> (bit 6)	Mode
0	0	Normal mode
0	1	Sequential mode with 2 PWM pulses per trigger
1	0	Sequential mode with 3 PWM pulses per trigger
1	1	Sequential mode with 4 PWM pulses per trigger

CURRENT CONTROL OF THE LEDS

LP5520 has separate 8-bit current control for each LED output. In manual mode the current for red LED is controlled with **current_control_r** (01H) register, for green LED with **current_control_g** (02H) and for blue LED with **current_control_b** (03H). Output current can be calculated with formula: **current (mA) = code x 0.235**, for example 20 mA current is obtained with code 85 (55H).

In automatic and stand-alone modes the LED current values programmed in EEPROM are used, and the current control registers have no effect. There are two ways to change the default current if needed. The defaults can be changed permanently by programming new values to the EEPROM. The other option is to make a temporary change by writing new current values in SRAM. Since this is not normally needed, it is only described in the Calibration Application Note AN1459.

OUTPUT ENABLES

R_{OUT}, G_{OUT} and B_{OUT} output activity is controlled with 3 enable bits of the **rgb_control** (00H) register:

<en_b> (bit 2)	**0**	Blue LED output B_{OUT} disabled
	1	Blue LED output B_{OUT} enabled
<en_g> (bit 1)	**0**	Green LED output G_{OUT} disabled
	1	Green LED output G_{OUT} enabled
<en_r> (bit 0)	**0**	Red LED output R_{OUT} disabled
	1	Red LED output R_{OUT} enabled

PWM control inputs PWMR, PWMG and PWMB can be used as external output enables in normal and automatic mode. In the sequential mode these inputs are the trigger inputs for respective outputs.

FADE IN / FADE OUT

LP5520 has an automatic fade in and out for the LED outputs. Fading makes the transitions smooth in on/off switching or when brightness is changed. It is not applied for the changes caused by the compensation algorithm. The fade can be turned on and off using the **<en_fade>** bit in the **rgb_control** (00H) register. The fade time is constant 520 ms and it does not depend on how big the brightness change is. The white balance is maintained during fading. Fading is off in the Stand-alone mode.

<en_fade>(bit 5)	**0**	Automatic fade disabled
	1	Automatic fade enabled

Fading only works in automatic mode. The LED current registers should be written to 0 for proper Fade operation. When the LEDs are turned on with Fading, it is best to set the brightness first and then enable the outputs and automatic mode. The LEDs can be turned off then by turning off the automatic mode (write rgb_auto to 0).

RGB DRIVER ELECTRICAL CHARACTERISTICS (R_{OUT}, G_{OUT}, B_{OUT} Outputs)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	R_{OUT}, G_{OUT} and B_{OUT} pin leakage current			0.1	**1**	µA
I_{MAX}	Maximum Sink Current	Outputs R_{OUT}, G_{OUT} and B_{OUT} Control = 255 (FFH)			60	mA

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_R	Current accuracy of R_{OUT}, G_{OUT} and B_{OUT}	Output current set to 20 mA	**19** **-5**	20	**21** **+5**	mA %
		Output current set to 60 mA	**54** **-10**	60	**66** **+10**	mA %
I_{MATCH}	Matching (1)	Between R_{OUT}, G_{OUT} and B_{OUT} at 20 mA current		±0.2	±2	%
t_{PWM}	PWM cycle time	Accuracy proportional to internal clock frequency		820		µs
f_{RGB}	RGB switching frequency	<pwm_fast> = 0		1.22		kHz
		<pwm_fast> = 1		19.52		kHz
V_{SAT}	Saturation voltage (2)	$I_{(LED)}$ = 60 mA		550		mV
f_{MAX}	External PWM maximum frequency	$I_{(LED)}$ = 60 mA			1	MHz

(1) Matching is the maximum difference from the average when all outputs are set to same current.
(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 2V.

RGB DRIVER TYPICAL PERFORMANCE CHARACTERISTICS

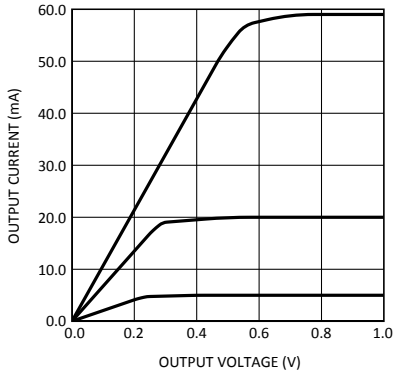


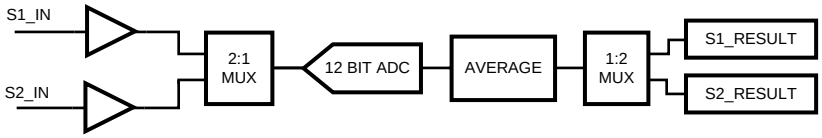
Figure 15. V_{SAT} vs I_{LED}

Temperature and Light Measurement

LP5520 has a 12-bit Analog-to-Digital Converter for the measurements. The ADC has two inputs. S1_IN input is intended for the LM20 temperature sensor and S2_IN input for light measurement or any DC voltage measurement. The conversion results are filtered with average filter for 134 ms. The **<adc_ch>** bit in the **Control** register selects, which conversion result can be read out from the registers **ADC_hi_byte** and **ADC_low_byte**. The **ADC_hi_byte** has to be read first. The **<comp_ch>** bit selects, which input is used for compensation. The ADC uses the LDO voltage 2.8V as the reference voltage. The input signal range is 0 – 2.8V and the inputs are buffered on the chip.

If S2_IN is used for light measurement using TDK optical sensor BCS2015G1 as shown in the Block Diagram on page 5, the measurement range is from 10 to 20.000 lux when using 100k resistor.

adc_ch(bit5)	**0**	S1 input can be read
	1	S2 input can be read
comp_sel(bit4)	**0**	S1 input is used for compensation
	1	S2 input is used for compensation



Magnetic High Voltage Boost DC/DC Converter

The LP5520 Boost DC/DC Converter generates a 5 to 20V supply voltage for the LEDs from single Li-Ion battery (2.9 to 4.5V). The output voltage is controlled with four bits in 18 steps. In adaptive mode the output voltage is automatically adjusted so that the LED drivers have enough voltage for proper operation. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. Switching frequency is 1 MHz. Boost converter options are controlled with few bits of **Control** (06H) register.

<en_autoload> (bit 3)	**0**	Internal boost converter loader off
	1	Internal boost converter loader on
<vout_auto> (bit 2)	**0**	Manual boost output adjustment
	1	Adaptive boost output adjustment
<en_boost> (bit 1)	**0**	Boost converter standby mode
	1	Boost converter active mode
<nstby> (bit 0)	**0**	LP5520 standby mode
	1	LP5520 active mode

The LP5520 Boost Converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An active load is used to remove the excess charge from the output capacitor at very light loads. Active load can be disabled with the **<en_autoload>** bit. Disabling active load will increase slightly the efficiency at light loads, but the downside is that pulse skipping will occur. The Boost Converter should be stopped when there is no load to minimize the current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop.

The following figure shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
   - Keeps the output below breakdown voltage.
   - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
   - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection. Prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.

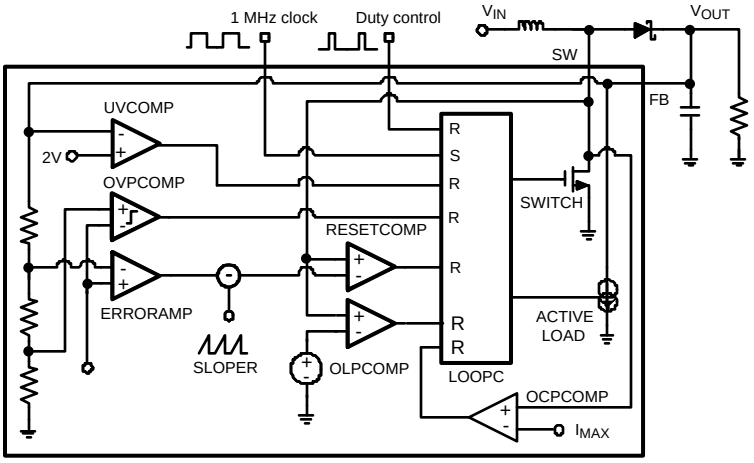


Figure 16. Boost Converter Topology

MAGNETIC BOOST DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LOAD}	Maximum Continuous Load Current	2.9V = V_{IN} V_{OUT} = 20V	70			mA
V_{OUT}	Output Voltage Accuracy (FB Pin)	2.9V ≤ V_{IN} ≤ 5.5V V_{OUT} = 20V	-1.7 **-5**		1.7 **+5**	%
RDS_{ON}	Switch ON Resistance	I_{SW} = 0.5A		0.3		Ω
f_{PWM}	Frequency Accuracy		−6 **−9**	±3	+6 **+9**	%
t_{PULSE}	Switch Pulse Minimum Width	no load		50		ns
$t_{STARTUP}$	Startup Time			20		ms
I_{MAX}	SW Pin Current Limit			1100		mA

BOOST CONTROL

User can set the Boost Converter to STANDBY mode by writing the register bit **<en_boost>** low. When **<en_boost>** is written high, the converter starts for 50 ms in low current PWM mode and then goes to normal PWM mode.

User can control the boost output voltage by boost output **boost_output** (05H) register.

Boost Output [7:0] Register 0DH		Boost Output Voltage (typical)
Bin	Dec	
00101	5	5.0V
00110	6	6.0V
00111	7	7.0V
...	...	...
01100	12	12.0V
01101	13	13.0V
01110	14	14.0V
...	...	...
10010	18	18.0V
10011	19	19.0V
10100	20	20.0V

If register value is lower than 5, then value of 5 is used internally. If register value is higher than 20, then value of 20 is used internally.

ADAPTIVE OUTPUT VOLTAGE CONTROL

When automatic boost voltage control is selected using the **<vout_auto>** bit in **Control** (06H) register, the user defined boost output voltage is ignored. The boost output voltage is adjusted for sufficient operating headroom by monitoring all enabled LED driver outputs. The boosted voltage is adjusted so that the lowest driver voltage is between 0.85 and 1.35V when the LED output currents are below 30 mA and to 1.0 – 1.5V when any LED current is above 30 mA. The output voltage range is from 5.0 to 20V in adaptive mode.

The adaptive voltage control helps saving energy by always setting the boost voltage to minimum sufficient value. It eliminates the need for extra voltage margins due to LED forward voltage variation or temperature variation. With very small brightness settings, when the PWM pulses in LED outputs are very narrow, the adaptive voltage setting will give higher than necessary boost voltage. This does not harm the overall efficiency, since this happens only when the power used is very small.

After reset the adaptive control is on by default. In stand-alone mode the adaptive output voltage is always used.

Boost Converter Typical Performance Characteristics

V_{IN} = 3.6V, V_{OUT} = 15.0V if not otherwise stated

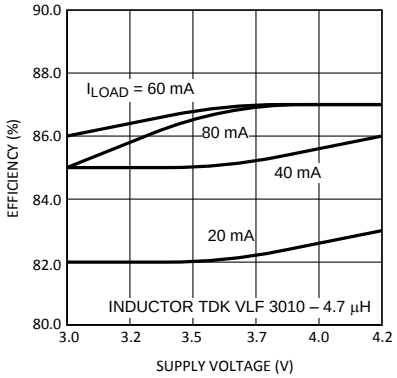


Figure 17. Boost Converter Efficiency

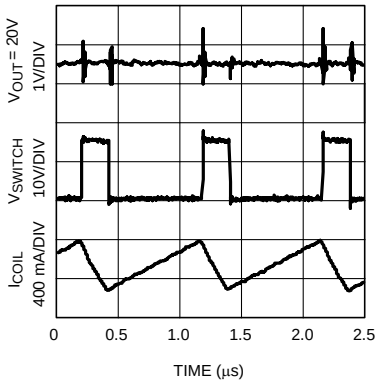


Figure 18. Boost Typical Waveforms at 60 mA Load

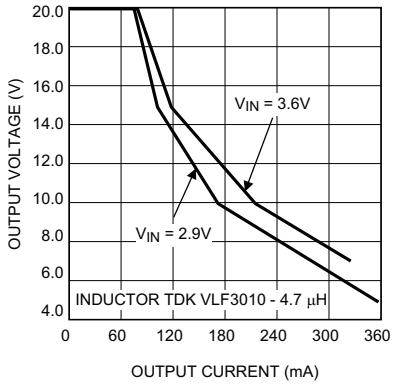


Figure 19. Boost Max. Output Voltage vs. Current

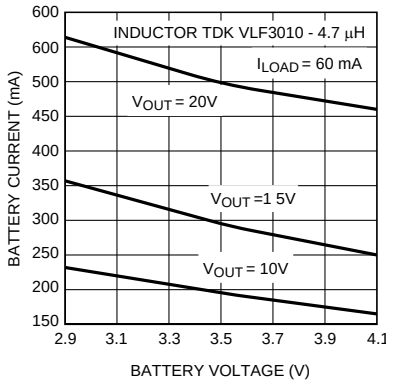


Figure 20. Battery Current vs. Voltage

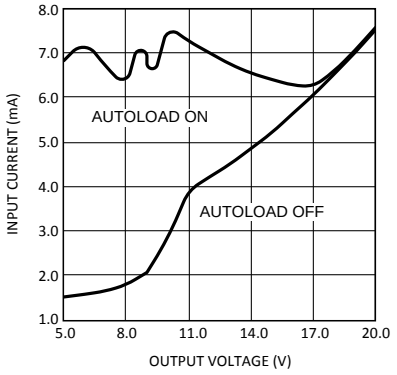


Figure 21. Autoload Effect on Input Current, No Load

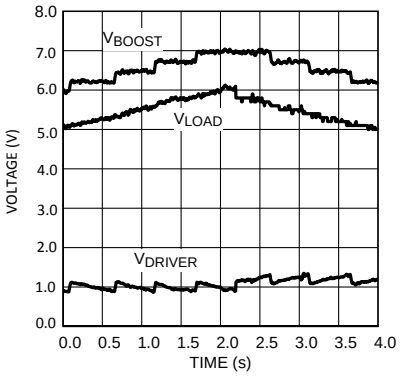


Figure 22. Adaptive Output Voltage Operation

Table 3. Logic Interface Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Logic Inputs SS, SI/A0, SCK/SCL, IFSEL, NRST, PWMR, PWMG, PWMB and BRC						

Table 3. Logic Interface Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Level				**0.2 × V_{DDIO}**	V
V_{IH}	Input High Level		**0.8 × V_{DDIO}**			V
I_I	Logic Input Current		**−1.0**		**1.0**	µA
$f_{SCK/SLC}$	Clock Frequency	I^2C Mode			**0.4**	MHz
		SPI Mode V_{DDIO} > 1.8V			**13**	
		SPI Mode 1.65V < V_{DDIO} < 1.8V			**5**	
Logic input NRST						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Logic Input Current		**-1.0**		**1.0**	µA
t_{NRST}	Reset Pulse Width		**10**			µs
Logic Output SO						
V_{OL}	Output Low Level	I_{SO} = 3 mA V_{DDIO} > 1.8V		0.3	**0.5**	V
		I_{SO} = 2 mA 1.65V < V_{DDIO} < 1.8V		0.3	**0.5**	V
V_{OH}	Output High Level	I_{SO} = -3 mA V_{DDIO} > 1.8V	**V_{DDIO} − 0.5**	V_{DDIO} − 0.3		V
		I_{SO} = -2 mA 1.65V < V_{DDIO} < 1.8V	**V_{DDIO} − 0.5**	V_{DDIO} − 0.3		V
I_L	Output Leakage Current	V_{SO} = 2.8V			**1.0**	µA
Logic Output SDA						
V_{OL}	Output Low Level	I_{SDA} = 3 mA		0.3	**0.5**	V

Control Interface

LP5520 supports two different interface modes:

- SPI interface (4 wire, serial)
- I^2C compatible interface (2 wire, serial)

User can define the serial interface by IF_SEL pin. IF_SEL = 0 selects the I^2C mode.

SPI Interface

LP5520 is compatible with SPI serial bus specification and it operates as a slave. The transmission consists of 16-bit Write and Read Cycles. One cycle consists of 7 Address bits, 1 Read/Write (RW) bit and 8 Data bits. RW bit high state defines a Write Cycle and low defines a Read Cycle. SO output is normally in high-impedance state and it is active only when Data is sent out during a Read Cycle. The Address and Data are transmitted MSB first. The Slave Select signal SS must be low during the Cycle transmission. SS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the SCK clock signal, while data is clocked out on the falling edge of SCK.

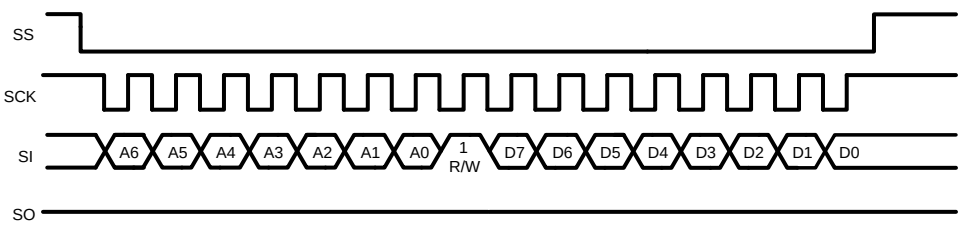


Figure 23. SPI Write Cycle

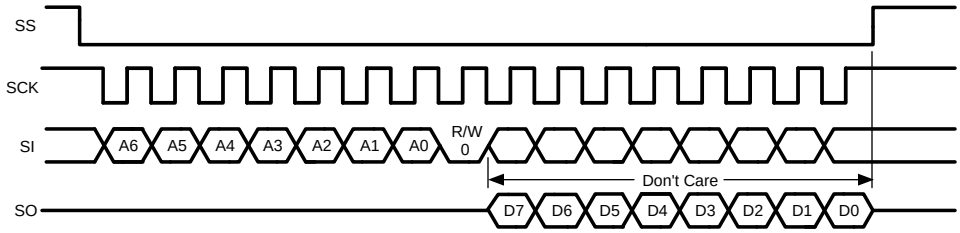


Figure 24. SPI Read Cycle

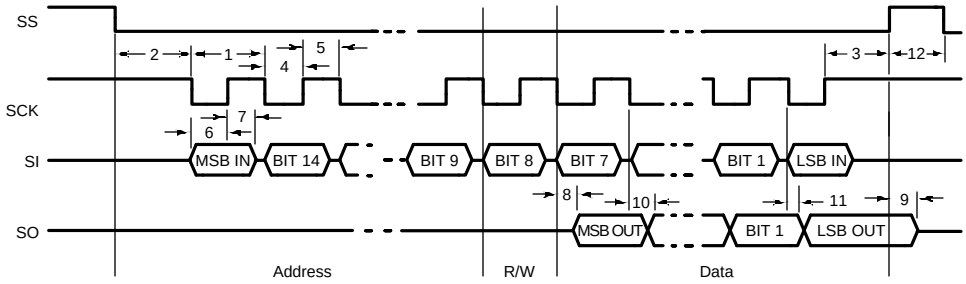


Figure 25. SPI Timing Diagram

SPI TIMING PARAMETERS

$V_{DDA} = V_{DDD} = V_{DD\_IO} = 2.775V$

Symbol	Parameter	Limit		Units
		Min	Max	
1	Cycle Time	70		ns
2	Enable Lead Time	35		ns
3	Enable Lag Time	35		ns
4	Clock Low Time	35		ns
5	Clock High Time	35		ns
6	Data Setup Time	0		ns
7	Data Hold Time	25		ns
8	Data Access Time		30	ns
9	Disable Time		20	ns
10	Data Valid		40	ns
11	Data Hold Time	0		ns

SPI INCREMENTAL ADDRESSING

LP5520 supports incremental addressing for memory read and write.

I²C Compatible Interface

I²C SIGNALS

The serial interface is in I²C mode when IF_SEL = 0. The SCL pin is used for the I²C clock and the SDA pin is used for bidirectional data transfer. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus (typical resistance is 1.8k). Signal timing specifications are shown in I²C TIMING PARAMETERS ($V_{DD1,2}$ = 3.0 to 4.5V, V_{DDIO} = 1.8V to $V_{DD1,2}$).

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

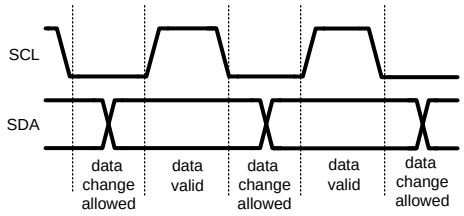


Figure 26. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

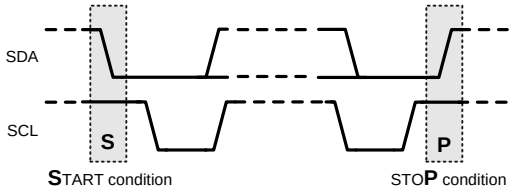


Figure 27. I²C Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). **The LP5520 address is 20h when SI=0 and 21h when SI=1.** For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

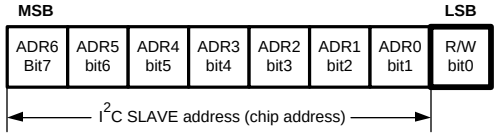
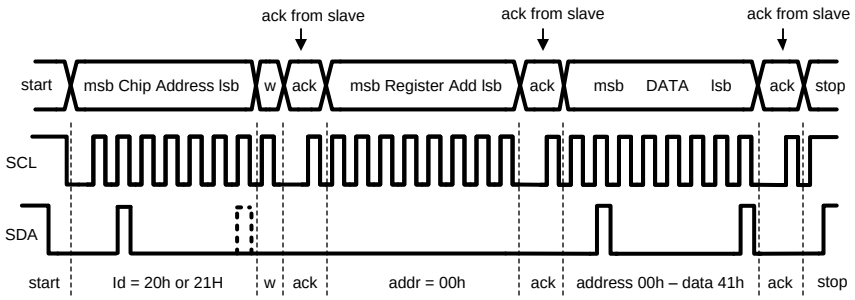


Figure 28. I²C Chip Address



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = 7-bit chip address, 20h when SI=0 and 21h when SI=1 for LP5520.

Figure 29. I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the I²C Read Cycle waveform.

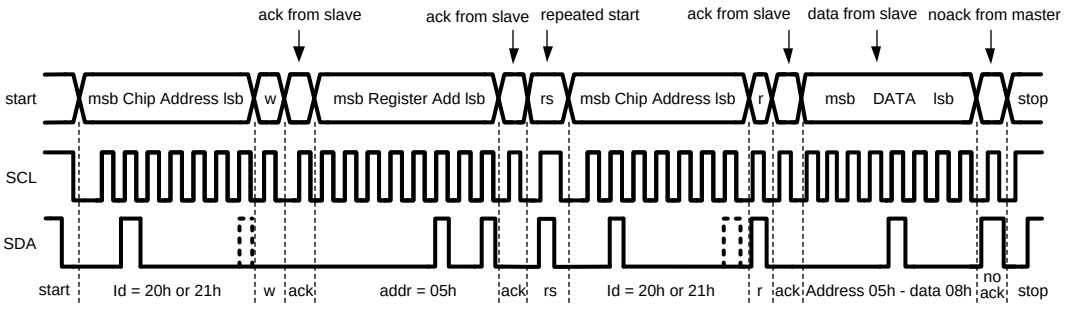


Figure 30. I²C Read Cycle

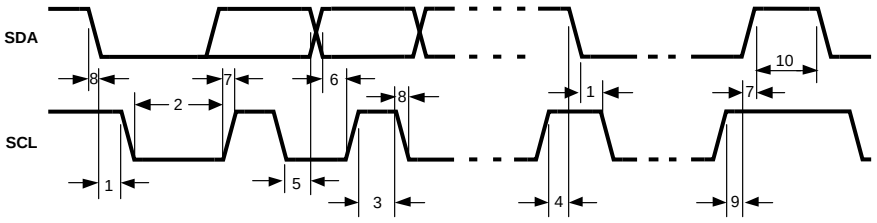


Figure 31. I²C Timing Diagram

I²C TIMING PARAMETERS ($V_{DD1,2}$ = 3.0 to 4.5V, V_{DDIO} = 1.8V to $V_{DD1,2}$)

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LP5520)	300	900	ns
5	Data Hold Time (Input direction, delay generated by Master)	0	900	ns

Symbol	Parameter	Limit		Units
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20 + 0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15 + 0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

Recommended External Components

OUTPUT CAPACITOR: C_{OUT}

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. Capacitor voltage rating must be sufficient, 25V or greater is recommended. Examples of suitable capacitors are: TDK C3216X5R1E475K, Panasonic ECJ3YB1E475K and ECJ4YB1E475K.

Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. Too low output capacitance can make the boost converter unstable. Output capacitor value reduction due to DC bias should be less than 70% at 20V (minimum 3 µF of real capacitance remaining).

INPUT CAPACITOR: C_{IN}

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple.

OUTPUT DIODE: D_{OUT}

A schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode should be greater than the peak inductor current (1A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the schottky diode significantly larger (~30V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer. A schottky diode with low parasitic capacitance helps in reducing EMI noise. Examples of suitable diodes are: Central Semiconductor CMMSH1-40 and Infineon BAS52-02V.

EMI FILTER COMPONENTS: C_{SW}, R_{SW}, L_{SW} and C_{HF}

EMI filter (R_{SW}, C_{SW} and L_{SW}) on the SW pin may be needed to slow down the fast switching edges and reduce ringing. These components should be as near as possible to the SW pin to ensure reliable operation. High frequency capacitor (C_{SW}) in the boost output helps in suppressing the high frequency noise from the switcher. 50V or greater voltage rating is recommended for the capacitors. The ferrite bead DC resistance should be less than 0.1Ω and current rating 1A or above. The impedance at 100 MHz should be 30 – 300Ω. Examples of suitable types are TDK MPZ1608S101A and Taiyo-Yuden FBMH 1608HM600-T.

INDUCTOR: L_1

A 4.7 µH shielded inductor is suggested for LP5520 boost converter. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (0.5 – 1.0A depending on the output current). Less than 500 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible. Examples of suitable inductors are: TDK VLF3010AT-4R7MR70 and Coilcraft LPS3010-472NL.

LIST OF RECOMMENDED EXTERNAL COMPONENTS

Symbol	Symbol Explanation	Value	Unit	Type
C_{VDDA}	C between V_{DDA} and GND	100	nF	Ceramic, X7R / X5R
C_{VDDD}	C between V_{DDD} and GND	100	nF	Ceramic, X7R, X5R
C_{VLDO}	C between V_{LDO} and GND	1	µF	Ceramic, X7R / X5R
C_{VDDIO}	C between VDDIO and GND	100	nF	Ceramic, X7R / X5R
C_{OUT}	C between FB and GND	2 x 4.7	µF	Ceramic, X7R / X5R, tolerance ±10%, DC bias effect ~ –30% at 20V
C_{IN}	C between battery voltage and GND	10	µF	Ceramic, X7R / X5R
L_1	L between SW and V_{BAT}	4.7	µH	Shielded, low ESR, I_{SAT} 0.5A
D_1	Rectifying Diode (Vf @ maxload)	0. 3 - 0.5	V	Schottky diode, reverse voltage 30V, repetitive peak current 0.5A
C_{SW}	Optional C in EMI filter	330	pF	Ceramic, X7R / X5R, 50V
R_{SW}	Optional R in EMI filter	3.9	Ω	±1%
C_{HF}	Optional high frequency output C	33 - 100	pF	Ceramic, X7R, X5R, 50V
L_{SW}	Ferrite bead in SW pin	30 - 300	Ω at 100 Mhz	
LEDs		User Defined		

LP5520 Registers, Control Bits and Default Values

All registers will have their default value after power-on or reset. Default value for correction registers is 1000 0000 (multiplier = 1). Default value for adaptive voltage control and fast PWM is on. Default value for current set registers is 55H which will set the current to 20 mA. Default value for all other register bits is 0. Note, that in automatic compensation mode the LED currents are obtained from the EEPROM.

Bits with **r/o** are read-only bits.

ADR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00H	**rgb control**	seq_ mode[1]	seq_ mode[0]	en_fade	pwm_ fast	rgb_auto	en_b	en_g	en_r	0001 0000
01H	**current control (R)**	cc_r[7]	cc_r[6]	cc_r[5]	cc_r[4]	cc_r[3]	cc_r[2]	cc_r[1]	cc_r[0]	0101 0101
02H	**current control (G)**	cc_g[7]	cc_g[6]	cc_g[5]	cc_g[4]	cc_g[3]	cc_g[2]	cc_g[1]	cc_g[0]	0101 0101
03H	**current control (B)**	cc_b[7]	cc_b[6]	cc_b[5]	cc_b[4]	cc_b[3]	cc_b[2]	cc_b[1]	cc_b[0]	0101 0101
04H	**pwm brightness**					brc_off	bri2	bri1	bri0	0000 0000
05H	**boost output**				vprog[4]	vprog[3]	vprog[2]	vprog[1]	vprog[0]	0000 0000
06H	**control**			adc_ch	comp_ sel	en_ autoload	vout_ auto	en_boost	nstby	0000 0100
08H	**ADC_ hi_byte**					bit11 **(r/o)**	bit10 **(r/o)**	bit9 **(r/o)**	bit8 **(r/o)**	
09H	**ADC_ low_byte**	bit7 **(r/o)**	bit6 **(r/o)**	bit5 **(r/o)**	bit4 **(r/o)**	bit3 **(r/o)**	bit2 **(r/o)**	bit1 **(r/o)**	bit0 **(r/o)**	
0AH	**R correction**	corr_r[7]	corr_r[6]	corr_r[5]	corr_r[4]	corr_r[3]	corr_r[2]	corr_r[1]	corr_r[0]	1000 0000
0BH	**G correction**	corr_g[7]	corr_g[6]	corr_g[5]	corr_g[4]	corr_g[3]	corr_g[2]	corr_g[1]	corr_g[0]	1000 0000
0CH	**B correction**	corr_b[7]	corr_b[6]	corr_b[5]	corr_b[4]	corr_b[3]	corr_b[2]	corr_b[1]	corr_b[0]	1000 0000
0DH	**EEPROM Control**	ee_ready **(r/o)**	ee_erase	ee_prog	ee_read			ee_page[1]	ee_page[0]	0000 0000

Register addresses from 40H to 5FH contain the EEPROM page. EEPROM access is described in the Calibration Memory chapter.

REGISTER BIT CONVENTIONS

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

Table 4. Register Bit Accessibility and Initial Condition

Key	Bit Accessibility
rw	Read/write
r	Read only
–0, –1	Condition after POR

rgb_control (00H) – RGB LEDs Control Register

7	6	5	4	3	2	1	0
seq_mode1	**seq_mode0**	**en_fade**	**pwm_fast**	**rgb_auto**	**en_b**	**en_g**	**en_r**
rw-0	rw-0	rw-0	rw-1	rw-0	rw-0	rw-0	rw-0

seq_mode[1:0]	Bits 6 - 7	0 0 – overlapping PWM mode 0 1 – sequential mode with 2 PWM pulses 1 0 – sequential mode with 3 PWM pulses 1 1 – sequential mode with 4 PWM pulses
en_fade	Bit 5	0 – automatic fade disabled 1 – automatic fade enabled
pwm_fast	Bit 4	0 – normal PWM frequency 1.22 kHz 1 – high PWM frequency 19.52 kHz
rgb_auto	Bit 3	0 – automatic compensation disabled 1 – automatic compensation enabled
en_b	Bit 2	0 – blue LED output B_{OUT} disabled 1 – blue LED output B_{OUT} enabled
en_g	Bit 1	0 – green LED output G_{OUT} disabled 1 – green LED output G_{OUT} enabled
en_r	Bit 0	0 – red LED output R_{OUT} disabled 1 – red LED output R_{OUT} enabled

current_control_R (01H) – Red LED Current Control Register

7	6	5	4	3	2	1	0
cc_r[7]	**cc_r[6]**	**cc_r[5]**	**cc_r[4]**	**cc_r[3]**	**cc_r[2]**	**cc_r[1]**	**cc_r[0]**
rw-0	rw-1	rw-0	rw-1	rw-0	rw-1	rw-0	rw-1

		Adjustment	
		cc_r[7:0]	**Typical driver current (mA)**
cc_r[7:0]	Bits 7 - 0	0000 0000	0
		0000 0001	0.234
		0000 0010	0.468
		0000 0011	0.702
		...	...
		1111 1101	59.202
		1111 1110	59.436
		1111 1111	59.670

current_control_G (02H) – Green LED Current Control Register

7	6	5	4	3	2	1	0
cc_g[7]	**cc_g[6]**	**cc_g[5]**	**cc_g[4]**	**cc_g[3]**	**cc_g[2]**	**cc_g[1]**	**cc_g[0]**
rw-0	rw-1	rw-0	rw-1	rw-0	rw-1	rw-0	rw-1

current_control_B (03H) – Blue LED Current Control Register

7	6	5	4	3	2	1	0
cc_b[7]	**cc_b[6]**	**cc_b[5]**	**cc_b[4]**	**cc_b[3]**	**cc_b[2]**	**cc_b[1]**	**cc_b[0]**
rw-0	rw-1	rw-0	rw-1	rw-0	rw-1	rw-0	rw-1

pwm_brightness (04H) – Brightness Control Register

7	6	5	4	3	2	1	0
				brc_off	**bri[2]**	**bri[1]**	**bri[0]**
r-0	r-0	r-0	rw-0	r-0	rw-0	rw-0	rw-0

<table>
<tr><td rowspan="11">brc_off
bri[2:0]</td><td rowspan="11">Bit 4
Bits 2-0</td><td colspan="3">brc_off = 0 - stand-alone mode,
brightness is defined with external BRC signal</td></tr>
<tr><td colspan="3">brc_off = 1 - brightness is defined with bri[2:0]</td></tr>
<tr><td>Control</td><td>Multiplier</td><td>Intensity %</td></tr>
<tr><td>0</td><td>0.008</td><td>0.8</td></tr>
<tr><td>1</td><td>0.016</td><td>1.6</td></tr>
<tr><td>10</td><td>0.031</td><td>3.1</td></tr>
<tr><td>11</td><td>0.063</td><td>6.3</td></tr>
<tr><td>100</td><td>0.125</td><td>12.5</td></tr>
<tr><td>101</td><td>0.250</td><td>25</td></tr>
<tr><td>110</td><td>0.500</td><td>50</td></tr>
<tr><td>111</td><td>1.000</td><td>100</td></tr>
</table>

boost_output (05H) – Boost Output Voltage Control Register

7	6	5	4	3	2	1	0
			vprog[4]	**vprog[3]**	**vprog[2]**	**vprog[1]**	**vprog[0]**
r-0	r-0	r-0	r-0	rw-0	rw-0	rw-0	rw-0

vprog[4:0]	Bits 4 - 0	**Adjustment**	
		vprog[4:0]	**Typical boost output voltage (V)**
		00101	5.0
		00110	6.0
		00111	7.0
		01000	8.0
		01001	9.0
		01010	10.0
		01011	11.0
		01100	12.0
		01101	13.0
		01110	14.0
		01111	15.0
		10000	16.0
		10001	17.0
		10010	18.0
		10011	19.0
		10100	20.0

control (06H) – Control Register

7	6	5	4	3	2	1	0
		adc_ch	**comp_sel**	**en_autoload**	**vout_auto**	**en_boost**	**nstby**
r-0	r-0	rw-0	rw-0	rw-0	rw-1	rw-0	rw-0

adc_ch	Bit 5	0 – compensation depends from the external LM20 temperature sensor 1 – compensation depends from forward voltage of the red LED as temperature sensor
comp_sel	Bit 4	0 – compensation based on S1_IN input 1 – compensation based on S2_IN input
en_autoload	Bit 3	0 – internal boost converter loader off 1 – internal boost converter loader off
vout_auto	Bit 2	0 – manual boost output adjustment with boost_output register 1 – automatic adaptive boost output adjustment
en_boost	Bit 1	0 – boost converter disabled 1 – boost converter enabled
nstby	Bit 0	0 – LP5520 standby mode 1 – LP5520 active mode

ADC_hi_byte (08H) – Analog Digital Converter Output, bits 8-11

7	6	5	4	3	2	1	0
				adc[11]	**adc[10]**	**adc[9]**	**adc[8]**
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

ADC_low_byte (09H) – Analog Digital Converter Output, bits 0-7

7	6	5	4	3	2	1	0
adc[7]	**adc[6]**	**adc[5]**	**adc[4]**	**adc[3]**	**adc[2]**	**adc[1]**	**adc[0]**
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

r_correction (0AH) – Additional Brightness Correction Value Register for Red LED

7	6	5	4	3	2	1	0
corr_r[7]	**corr_r[6]**	**corr_r[5]**	**corr_r[4]**	**corr_r[3]**	**corr_r[2]**	**corr_r[1]**	**corr_r[0]**
rw-1	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

corr_r[7:0]	Bits 7-0	**Correction**	
		corr_r[7:0]	**Multiplier**
		0000 0000	0
		0000 0001	0.0078
		0000 0010	0.0156
		...	...
		1000 0000	1.000
		...	...
		1111 1101	1.991
		1111 1110	1.999
		1111 1111	2.000

g_correction (0BH) – Additional Brightness Correction Value Register for Green LED

7	6	5	4	3	2	1	0
corr_g[7]	**corr_g[6]**	**corr_g[5]**	**corr_g[4]**	**corr_g[3]**	**corr_g[2]**	**corr_g[1]**	**corr_g[0]**
rw-1	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

b_correction (0CH) – Additional Brightness Correction Value Register for Blue LED

7	6	5	4	3	2	1	0
corr_b[7]	**corr_b[6]**	**corr_b[5]**	**corr_b[4]**	**corr_b[3]**	**corr_b[2]**	**corr_b[1]**	**corr_b[0]**
rw-1	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

EEPROM_control (0DH) – EEPROM Control Register

7	6	5	4	3	2	1	0
ee_ready	**ee_erase**	**ee_prog**	**ee_read**			**ee_page[1]**	**ee_page[0]**
r-1	rw-0	rw-0	r-0	r-0	r-0	rw-0	rw-0

ee_ready	Bit 7	EEPROM operations ready bit (read only)			
ee_erase	Bit 6	Start bit for erasing sequence			
ee_prog	Bit 5	Start bit for programming sequence			
ee_read	Bit 4	Read EEPROM data to SRAM			
ee_page[1:0]	Bits 1-0	**ee_page[1]**	**ee_page[0]**	**page**	**EEPROM addresses**
		0	0	0	00H-1FH (0-31)
		0	1	1	20H-3FH (32-63)
		1	0	2	40H-5FH (64-95)
		1	1	4	60H-7FH (96-127)

REVISION HISTORY

Changes from Original (April 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	32

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP5520TL/NOPB	ACTIVE	DSBGA	YZR	25	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	5520	Samples
LP5520TLX/NOPB	ACTIVE	DSBGA	YZR	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	5520	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

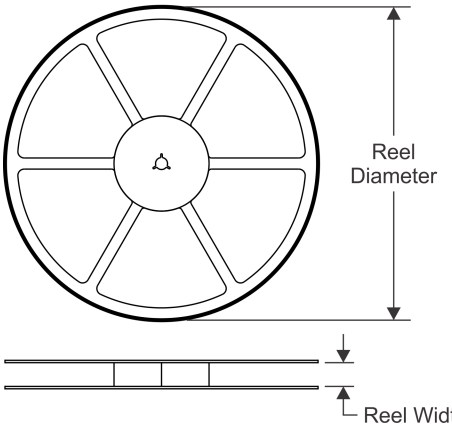
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

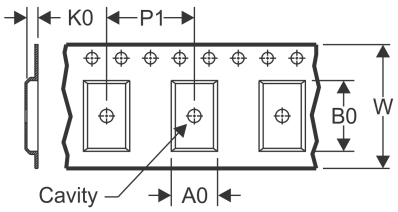
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

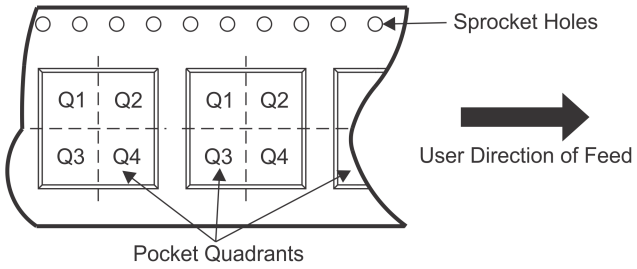


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

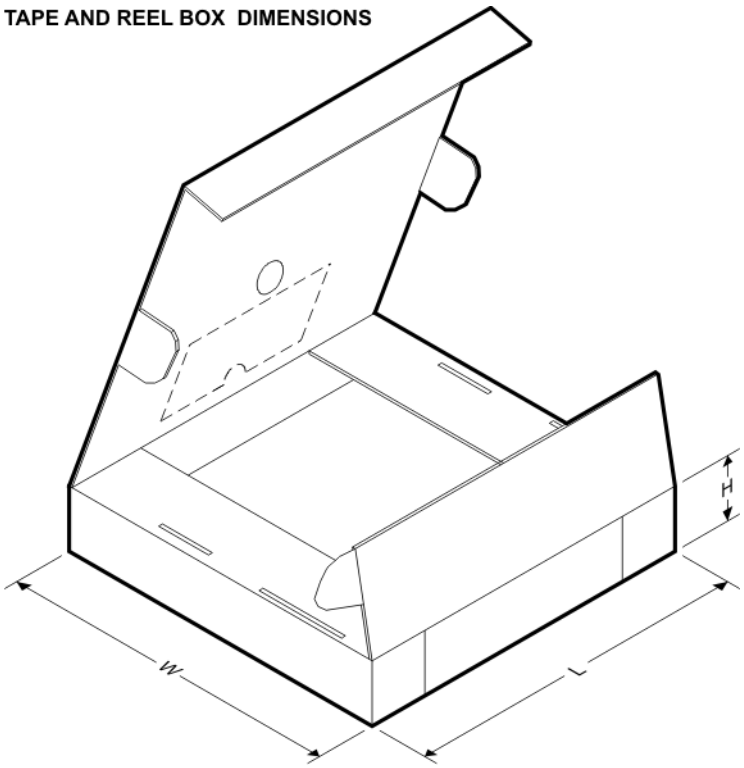
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5520TL/NOPB	DSBGA	YZR	25	250	178.0	8.4	2.67	2.95	0.76	4.0	8.0	Q1
LP5520TLX/NOPB	DSBGA	YZR	25	3000	178.0	8.4	2.67	2.95	0.76	4.0	8.0	Q1

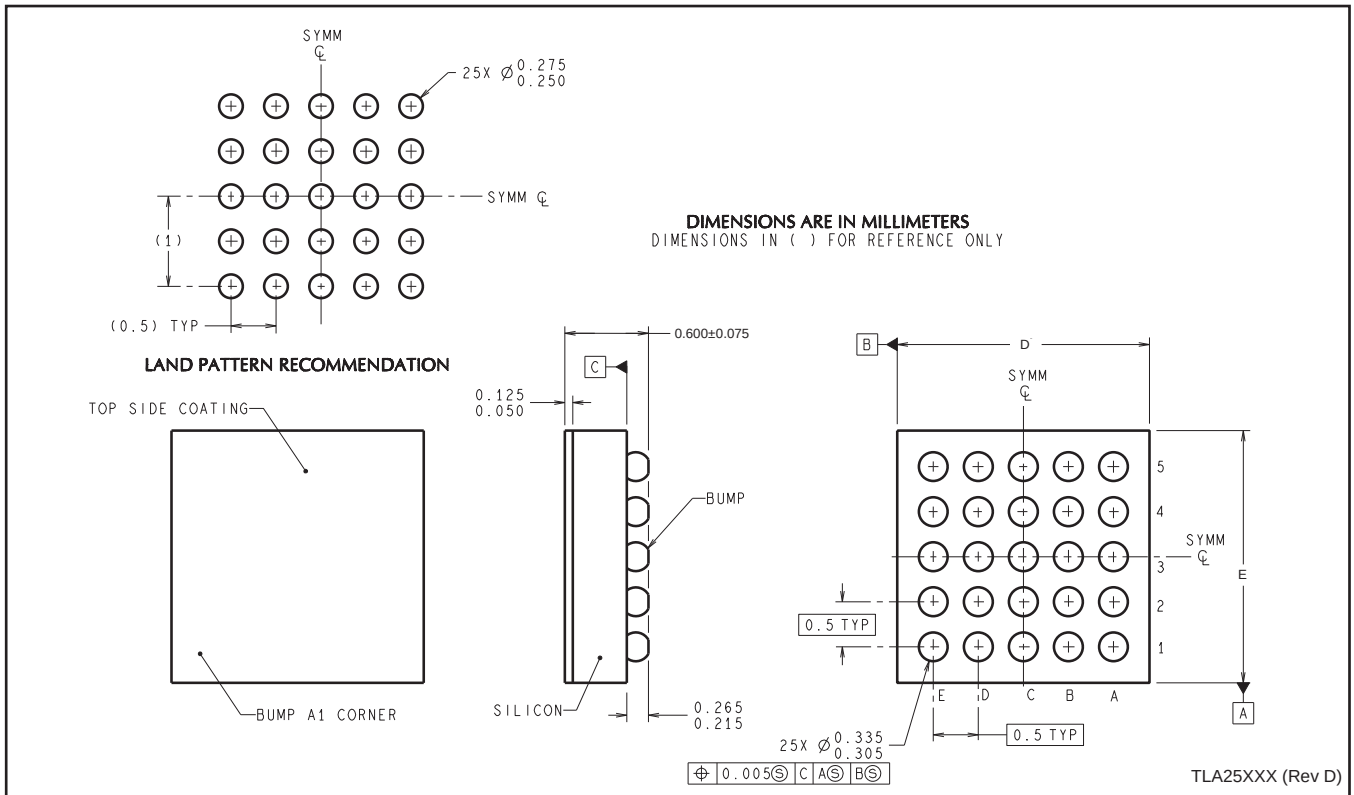
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5520TL/NOPB	DSBGA	YZR	25	250	210.0	185.0	35.0
LP5520TLX/NOPB	DSBGA	YZR	25	3000	210.0	185.0	35.0

YZR0025



D: Max = 2.787 mm, Min =2.727 mm

E: Max = 2.621 mm, Min =2.561 mm

4215055/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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