Ultra Low Noise, Dual 200mA Linear Regulator for RF/Analog Circuits

Check for Samples: LP8900

FEATURES

- **Operation from 1.8V to 5.5V Input**
- **1% Accuracy Over Temperature**
- **Output Voltage from 1.2V to 3.6V**
- **6μV_{RMS}Output Voltage Noise**
- **PSRR 75dB at 1kHz**
- **110mV Dropout at 200mA Load**
- **48μA Quiescent Current per Regulator**
- **80μs Start-Up Time**
- **Stable with Ceramic Capacitors as Small as 0402**
- **Thermal-Overload and Short-Circuit Protection**

APPLICATIONS

- **Battery Operated Devices**
- **Hand-Held Information Appliances**
- **Noise Sensitive RF Applications**
- **DC/DC Convertor Post Regulation/Filter**

PACKAGE

- **6 pin DSBGA (1.5mm x 1.1mm)**

DESCRIPTION

The LP8900 is a dual linear regulator capable of supplying 200mA output current per regulator. Designed to meet the requirements of RF/Analog circuits, the LP8900 provides low device noise, High PSRR, low quiescent current and superior line transient response figures.

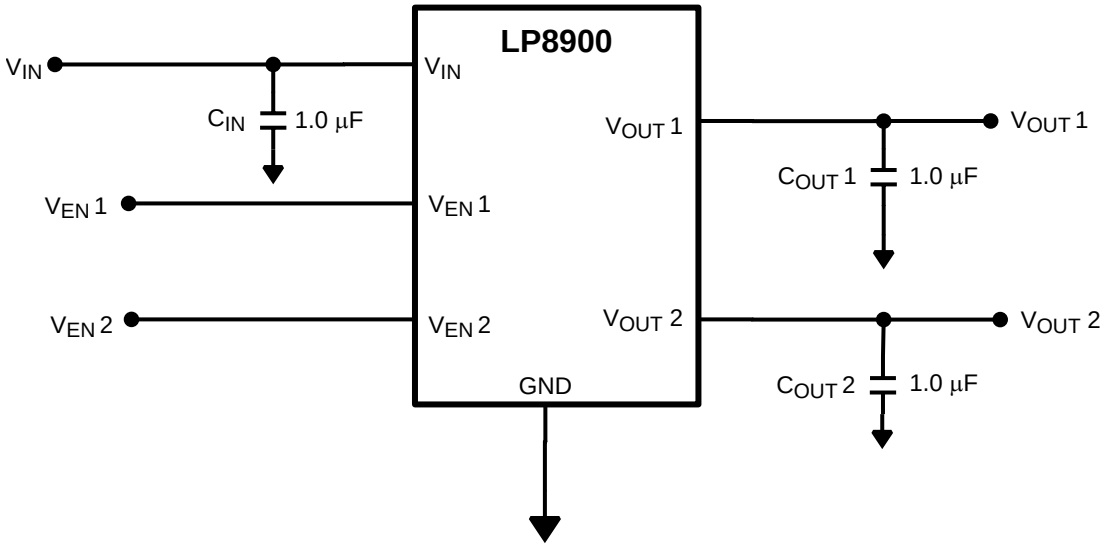
Using new innovative design techniques the LP8900 offers class-leading device noise performance without a noise bypass capacitor.

The LP8900 is designed to be stable with space saving ceramic capacitors as small as 0402 case size, enabling a solution size <4mm ^{2}.

Performance is specified for a -40°C to 125°C junction temperature range.

Output voltage options are available between 1.2V and 3.6V, for availability please contact your local TI sales office.

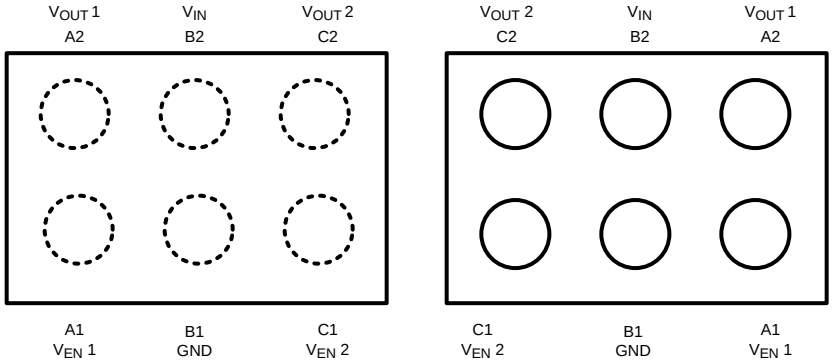
Typical Application Circuit



Pin Descriptions

Pin No.	Symbol	Name and Function
A1	V_{EN} 1	Enable Input; Enables the Regulator when ≥ 1.2V. Disables the Regulator when ≤ 0.4V. Enable Input has an internal 3MΩ pull-down resistor to GND.
B1	GND	Common Ground.
C1	V_{EN} 2	Enable Input; Enables the Regulator when ≥ 1.2V. Disables the Regulator when ≤ 0.4V. Enable Input has an internal 3MΩ pull-down resistor to GND.
C2	V_{OUT} 2	Voltage output. A Low ESR Ceramic Capacitor should be connected from this pin to GND. (See Application Information) Connect this output to the load circuit.
B2	V_{IN}	Voltage Supply Input. A 1.0µF capacitor should be connected from this pin to GND.
A2	V_{OUT} 1	Voltage output. A Low ESR Ceramic Capacitor should be connected from this pin to GND. (See Application Information) Connect this output to the load circuit.

Connection Diagram



Top View **Bottom View**

Figure 1. 6 Bump Thin DSBGA, Large Bump
See package number YZR0006CZA

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V_{IN}, V_{OUT} Pins: Voltage to GND		-0.3 to 6.5V
V_{EN} : Voltage to GND		-0.3 to (V_{IN} + 0.3V) to 6.5V (max)
Junction Temperature		150°C
Lead/Pad Temp. (4)	DSBGA	260°C
Storage Temperature		-65 to 150°C
Continuous Power Dissipation (5)		Internally Limited
ESD (6)	Human Body Model	2KV
	Machine Model	200V

(1) All Voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) For further information on these packages please refer to the following application notes, AN-1112 (SNVA009) DSBGA Wafer Level Chip Scale Package.
(5) Internal thermal shutdown circuitry protects the device from permanent damage.
(6) The human body model is 100pF discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

OPERATING RATINGS (1)

Input Voltage Range	1.8 to 5.5V
Recommended Load Current per channel	200mA
Junction Temperature	-40°C to 125°C
Ambient Temperature T_A Range (2)	-40°C to 85°C

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max\text{-}op)}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part / package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max\text{-}op)} - (\theta_{JA} \times P_{D(max)})$.

THERMAL PROPERTIES (1)

Junction To Ambient Thermal Resistance(2)	θ_{JA} JEDEC Board (3)	108°C/W
	θ_{JA} 4 Layer Board	172°C/W

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.
(3) Full details can be found in JESD61-7

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{EN} =1.2V, V_{IN} = V_{OUT} + 0.5V, or 1.8V, whichever is higher , where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = C_{OUT} = 1µF, I_{OUT} = 1.0mA .
Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125°C. (1)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
V_{IN}	Input Voltage	See (2)			1.8	5.5	V
ΔV_{OUT}	Output Voltage Tolerance	V_{IN} = $V_{OUT(NOM)}$ + 0.5V to 5.5V I_{LOAD} = 1mA			**-1.0**	**1.0**	%
		V_{IN} = 1.8V to 5.5V I_{LOAD} = 1mA, V_{OUT} = 1.2V			**-2.25**	**2.25**	%
	Line Regulation Error	V_{IN} = $V_{OUT(NOM)}$ +0.5V to 5.5V, I_{OUT} = 1mA		0.05			%/V
	Load Regulation Error	I_{OUT} = 1mA to 200mA		4		**9**	mV
V_{DO}	Dropout Voltage(3)	I_{OUT} = 200mA	V_{OUT} = 3.6V	55		**82**	mV
			V_{OUT} = 2.8V	110		**164**	
			V_{OUT} = 1.8V	185		**260**	
I_{LOAD}	Load Current	See (4)			0	**200**	mA
I_Q	Quiescent Current	V_{EN1} = 1.2V, V_{EN2} = 0V I_{OUT} = 0mA		48		**120**	µA
		V_{EN1} = 1.2V, V_{EN2} = 1.2V I_{OUT} = 0mA		85		**200**	
		V_{EN1} = 1.2V, V_{EN2} = 1.2V I_{OUT} = 200mA		210			
		V_{EN} ≤ 0.4V		0.003		**1.0**	
I_{SC}	Short Circuit Current Limit	V_{IN} = 3.6V (5)		600		**900**	mA
PSRR	Power Supply Rejection Ratio (6)	f = 1kHz, I_{OUT} = 200mA		75			dB
		f = 10kHz, I_{OUT} = 200mA		65			
		f = 100kHz, I_{OUT} = 200mA		45			
		f = 1MHz, I_{OUT} = 200mA		30			
e_n	Output noise Voltage (6)	BW = 10Hz to 100kHz, V_{IN} = 4.2V, C_{OUT} = 1.0µF	I_{OUT} = 0mA	6			μV_{RMS}
			I_{OUT} = 1mA	10			
			I_{OUT} = 200mA	6			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		155			°C
		Hysteresis		15			
Enable Control Characteristics							
I_{EN}	Maximum Input Current at V_{EN} Input(7)	V_{EN} = 0V, V_{IN} = 5.5V		0.003			µA
		V_{EN} = V_{IN} = 5.5V				**4**	
V_{IL}	Low Input Threshold	V_{IN} = 1.8V to 5.5V				**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 1.8V to 5.5V			**1.2**		V
Timing\Transient Characteristics(6)							
T_{ON}	Turn On Time	To 95% Level $V_{OUT(nom)}$		80		**200**	µs
T_{OFF}	Turn Off Time	5% of $V_{OUT(NOM)}$,I_{OUT}= 0mA		0.4		**1**	ms
	Line Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 30µs δV_{IN} = 600mV		1			mV (pk - pk)

(1) All limits are specified. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The minimum input voltage = $V_{OUT(NOM)}$ + 0.5V or 1.8V, whichever is greater.
(3) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100mV below its nominal value. This parameter is only specified for output voltages above 1.8V.
(4) The device maintains the regulated output voltage without a load.
(5) Short circuit current is measured with V_{OUT} pulled to 0V.
(6) This electrical specification is ensured by design.
(7) Enable Pin has an internal 3MΩ typical, resistor connected to GND.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, V_{EN} =1.2V, V_{IN} = V_{OUT} + 0.5V, or 1.8V, whichever is higher , where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = C_{OUT} = 1µF, I_{OUT} = 1.0mA .
Typical values and limits appearing in normal type apply for T_A = 25°C. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125°C. (1)

Symbol	Parameter	Conditions		Typ	Limit		Units
					Min	Max	
Transient Response	Load Transient Response $\|\delta V_{OUT}\|$	T_{rise} = T_{fall} = 1µs	I_{OUT} = 1 mA to 200mA	80			mV
			I_{OUT} = 200mA to 1mA	70			
	Overshoot on Start-up			0		**1**	%

RECOMMENDED CAPACITOR SPECIFICATIONS

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_{IN}	Input Capacitor	Capacitance (1)	1.0	**0.33**	**10**	µF
C_{OUT}	Output Capacitor		1.0	**0.33**	**4.7**	
		ESR		**5**	**500**	mΩ

(1) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R or X5R. (See capacitor section in Application Hints)

TYPICAL PERFORMANCE CHARACTERISTICS.

Unless otherwise specified, C_{IN} = C_{OUT}=1.0µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 2.85V , Enable pin is tied to V_{IN}.

Power Supply Rejection Ratio

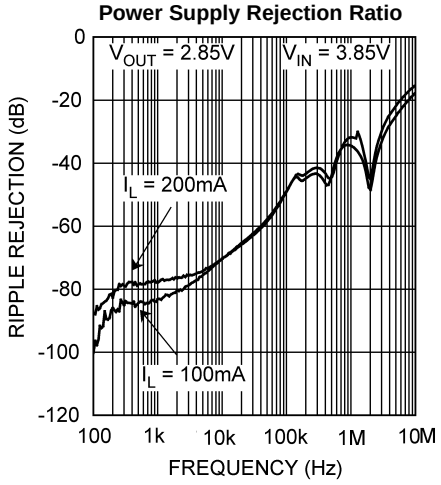


Figure 2.

Power Supply Rejection Ratio

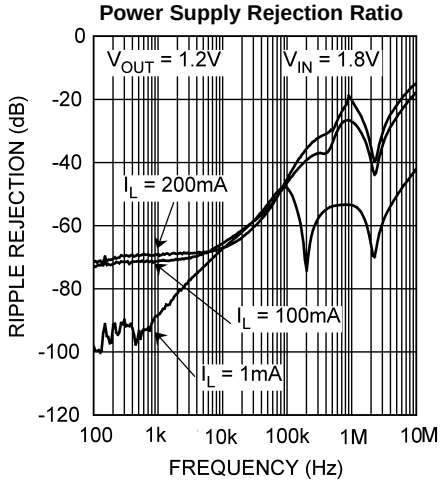


Figure 3.

Noise Density

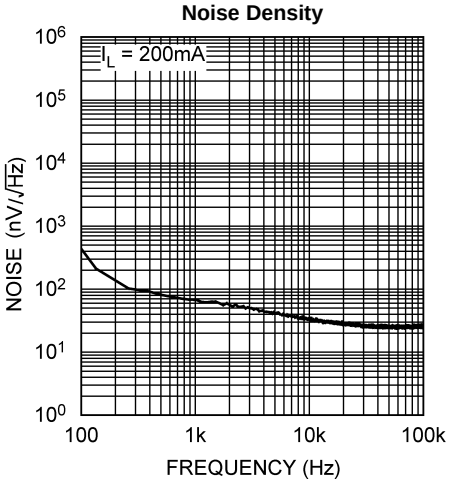


Figure 4.

Output Voltage Change vs Temperature

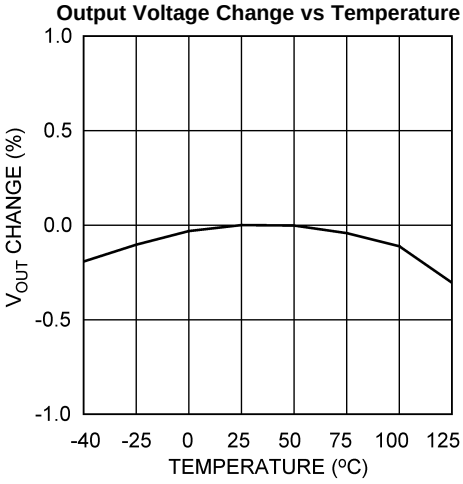


Figure 5.

Ground Current vs Load Current

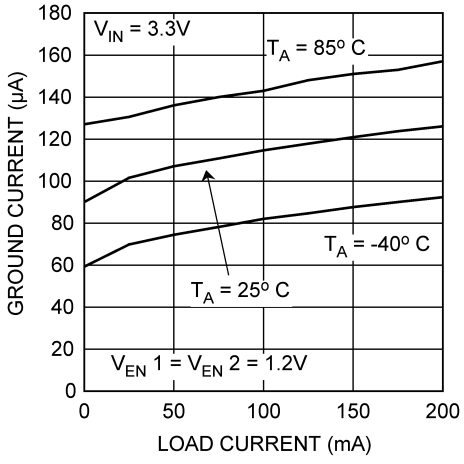


Figure 6.

Ground Current vs Load Current

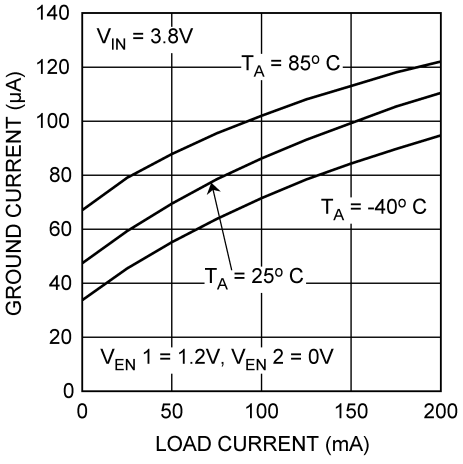


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS. (continued)

Unless otherwise specified, C_{IN} = C_{OUT}=1.0µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 2.85V , Enable pin is tied to V_{IN}.

Ground Current vs V_{IN}

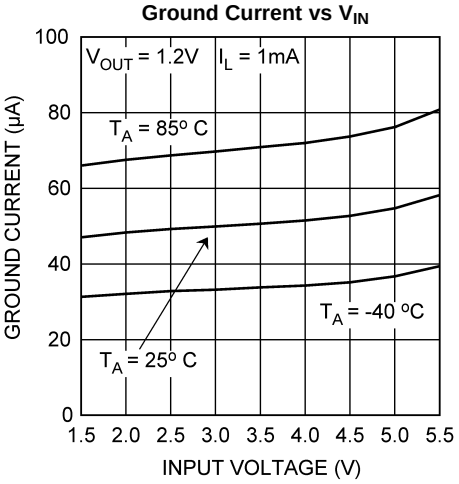
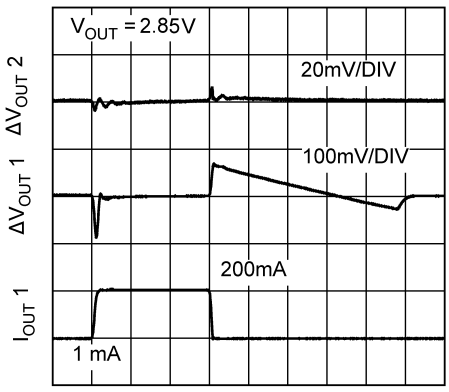


Figure 8.

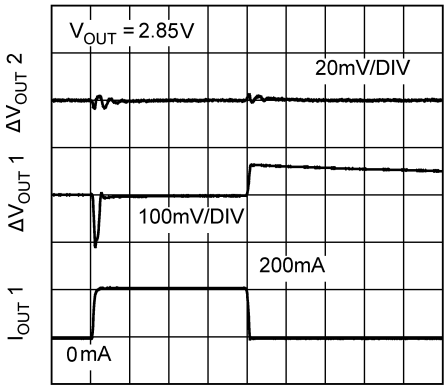
Vout 1 Load Transient 1 to 200mA



TIME (10µs/DIV)

Figure 9.

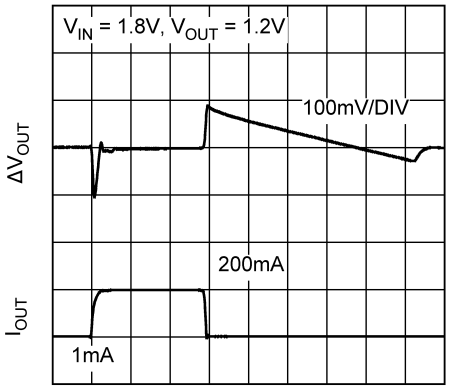
Vout 1 Load Transient 0 to 200mA



TIME (10µs/DIV)

Figure 10.

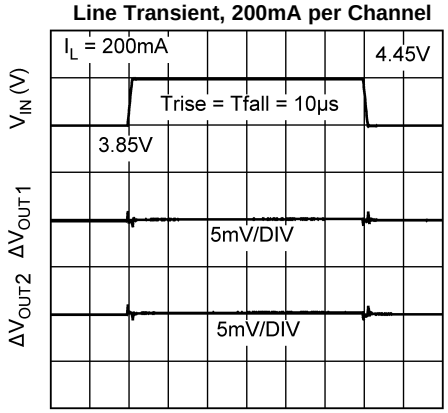
Load Transient. Vin = 1.8V, Vout = 1.2V



TIME (10µs/DIV)

Figure 11.

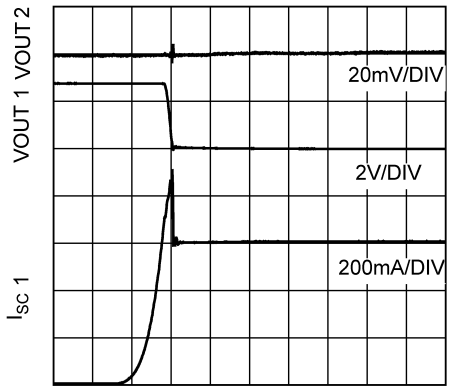
Line Transient, 200mA per Channel



TIME (100µs)

Figure 12.

Short Circuit Current



TIME (50µs/DIV)

Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS. (continued)

Unless otherwise specified, C_{IN} = C_{OUT}=1.0µF Ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1.0V or 1.8V whichever is greater, T_A = 25°C, $V_{OUT(NOM)}$ = 2.85V , Enable pin is tied to V_{IN}.

Enable Start-up Characteristics

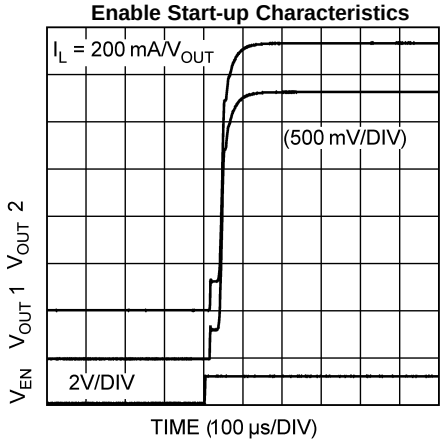


Figure .

Vin and Enable Tied Together

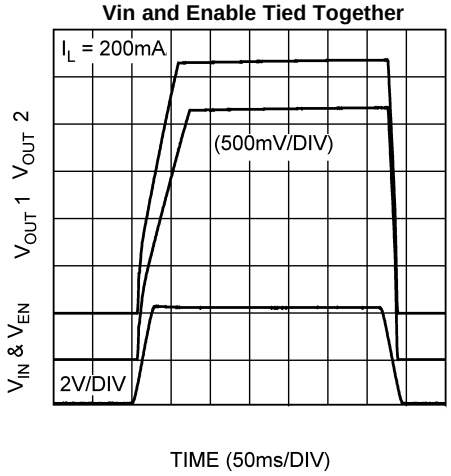


Figure 14.

Shutdown Characteristics

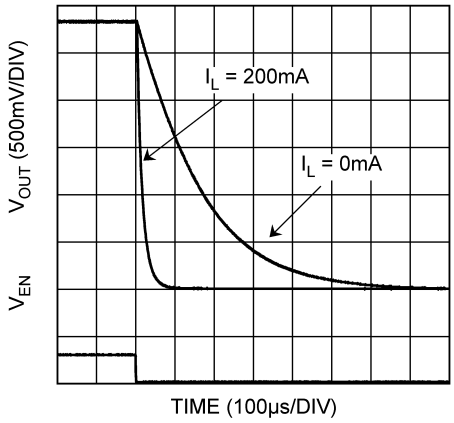


Figure 15.

Dropout Voltage

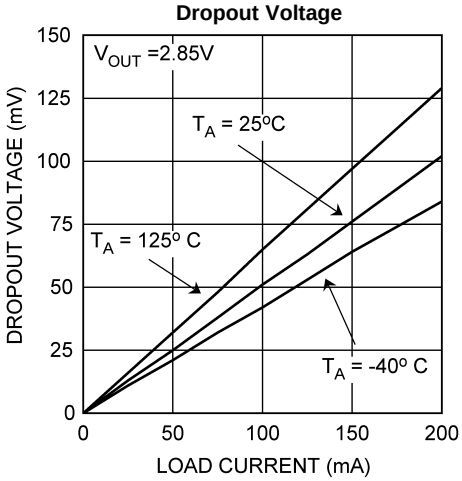


Figure 16.

Dropout Voltage vs Output Voltage

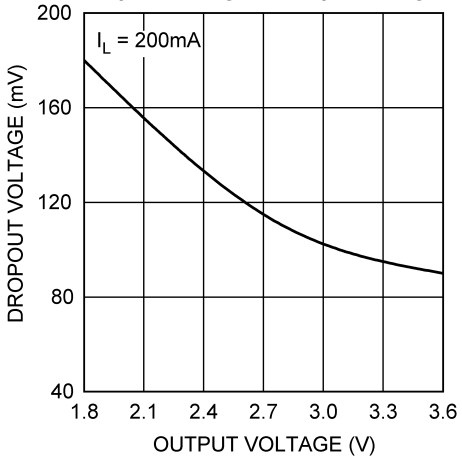


Figure 17.

APPLICATION INFORMATION

EXTERNAL CAPACITORS

In common with most regulators, the LP8900 requires external capacitors for regulator stability. The LP8900 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP8900 input pin and ground (this capacitance value may be increased to 10µF).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance, temperature, and voltage coefficients must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

Correct selection of the output capacitor is critical to ensure stable operation in the intended application.

The output capacitor must meet all the requirements specified in the recommended capacitor table over all conditions in the application. These conditions include DC bias, frequency and temperature. Unstable operation will result if the capacitance drops below the minimum specified value.

The LP8900 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (dielectric type X7R or X5R) with an ESR between 5mΩ to 500mΩ, is suitable in the LP8900 application circuit.

Other ceramic types such as Y5V and Z5U are less suitable owing to their inferior temperature characteristics. (See section on Capacitor Characteristics).

It is also recommended that the output capacitor is placed within 1cm of the output pin and returned to a clean, low impedance, ground connection.

It is possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section Capacitor Characteristics).

NO-LOAD STABILITY

The LP8900 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP8900 is designed to work with ceramic capacitors on the input and outputs to take advantage of the benefits they offer. For capacitance values around 1.0µF, ceramic capacitors give the circuit designer the best design options in terms of low cost and minimal area.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular, to ensure stability, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general.

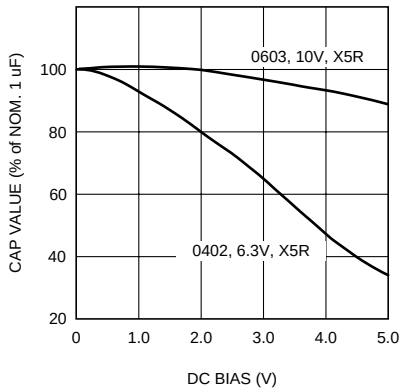


Figure 18. Effect of DC bias on Capacitance Value.

As an example Figure 18 shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application. Ceramic capacitors have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 4.7µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP8900. The temperature performance of ceramic capacitors varies by type. Capacitor type X7R is specified with a tolerance of ±15% over the temperature range -55°C to +125°C. The X5R has a similar tolerance over the reduced temperature range of -55°C to +85°C. Some large value ceramic capacitors (4.7µF) are manufactured with Z5U or Y5V temperature characteristics, which can result in the capacitance dropping by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R or X5R types are recommended in applications where the temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

ENABLE CONTROL

The LP8900 may be switched ON or OFF by a logic input at the ENABLE pin.A high voltage at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 3nA. However if the application does not require the shutdown feature, the V_{EN} pin can be tied to V_{IN} to keep the regulator permanently on. To ensure fast start-up is achieved, V_{EN} should be driven separately.

A 3MΩ pulldown resister ties the V_{EN} input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the ELECTRICAL CHARACTERISTICS section under V_{IL} and V_{IH}.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in the TI Application Note (AN-1112) SNVA009. Referring to the section *Surface Mount Technology (SMT) Assenbly Considerations*, it should be noted that the pad style which must be used with the 6 pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PCB may be used to facilitate placement of the DSBGA device.

DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight may cause mis-operation of the device. Light sources such as halogen lamps can affect the electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that fluorescent lighting, used inside most buildings will have little effect on performance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP8900TLE-3333/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		B	Samples
LP8900TLE-AAAH/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		3	Samples
LP8900TLE-AAEB/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	A	Samples
LP8900TLE-AAEC/NOPB	ACTIVE	DSBGA	YZR	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D	Samples
LP8900TLX-3333/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		B	Samples
LP8900TLX-AAAH/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3	Samples
LP8900TLX-AAEB/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		A	Samples
LP8900TLX-AAEC/NOPB	ACTIVE	DSBGA	YZR	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

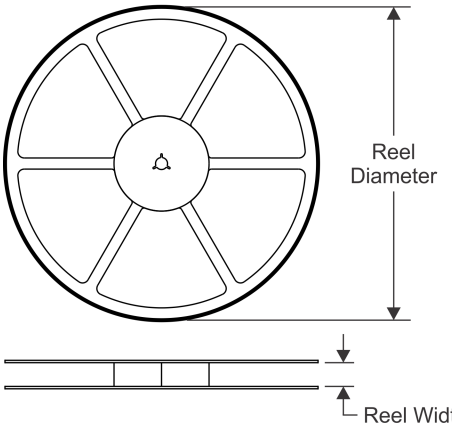
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

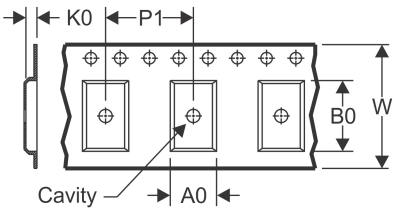
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

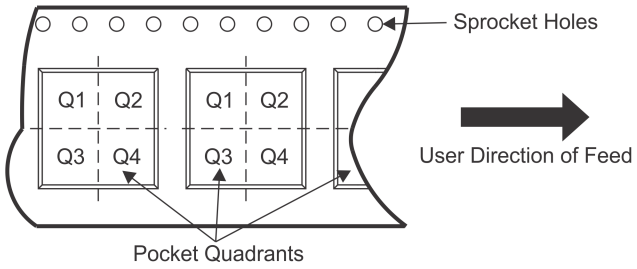


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

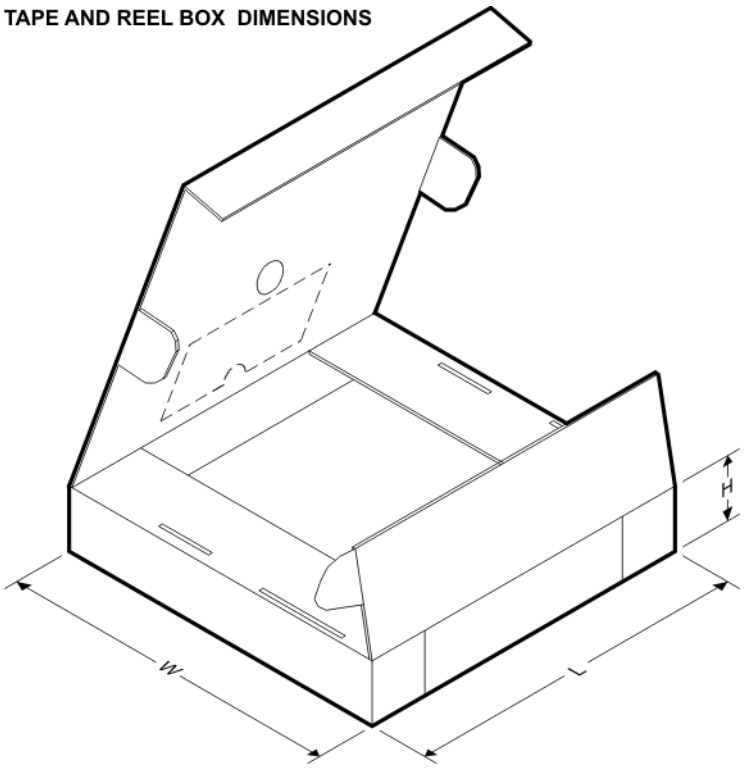
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8900TLE-3333/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLE-AAAH/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLE-AAEB/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLE-AAEC/NOPB	DSBGA	YZR	6	250	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLX-3333/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLX-AAAH/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLX-AAEB/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1
LP8900TLX-AAEC/NOPB	DSBGA	YZR	6	3000	178.0	8.4	1.15	1.63	0.7	4.0	8.0	Q1

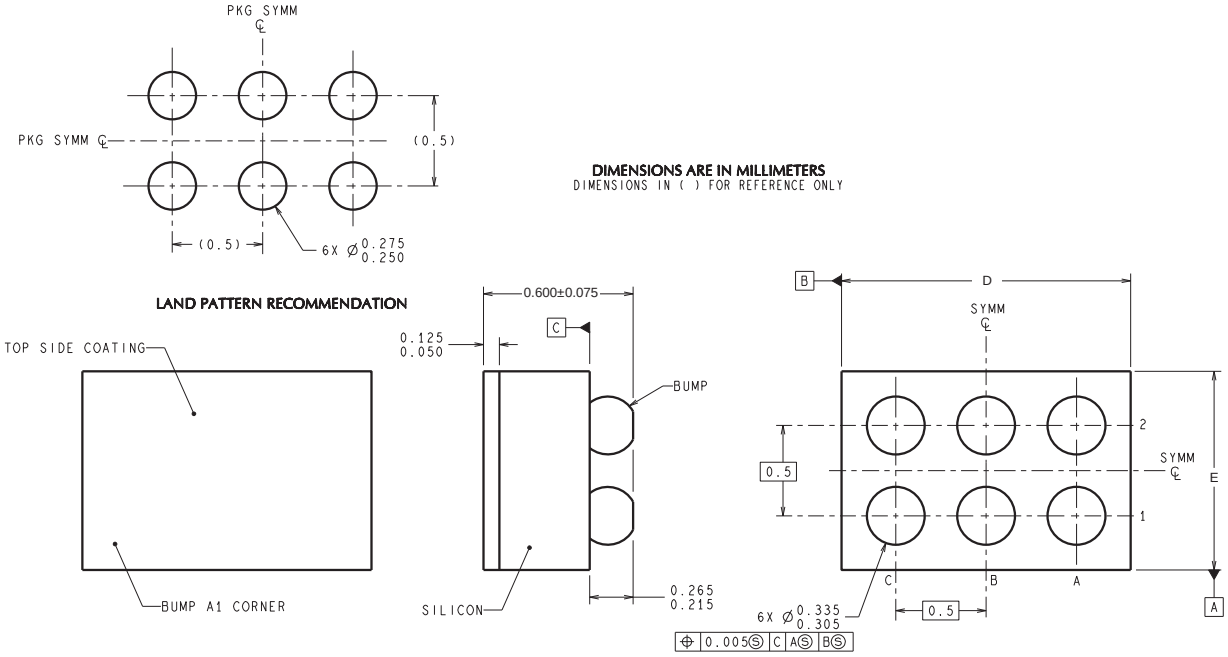
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8900TLE-3333/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LP8900TLE-AAAH/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LP8900TLE-AAEB/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LP8900TLE-AAEC/NOPB	DSBGA	YZR	6	250	210.0	185.0	35.0
LP8900TLX-3333/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LP8900TLX-AAAH/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LP8900TLX-AAEB/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0
LP8900TLX-AAEC/NOPB	DSBGA	YZR	6	3000	210.0	185.0	35.0

YZR0006



TLA06XXX (Rev C)

D: Max = 1.49 mm, Min = 1.43 mm

E: Max = 1.09 mm, Min = 1.03 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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