

## N-Channel Controllers for Constant Current LED Drivers

 Check for Samples: [LM3421](#), [LM3421-Q1](#), [LM3423](#), [LM3423-Q1](#)

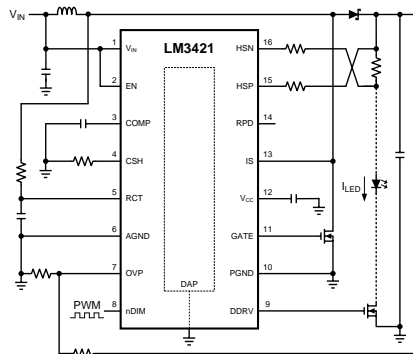
### FEATURES

- **LM3421Q1/LM3423Q1 are Automotive Grade Products That are AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature) and Similarly LM3421Q0/LM3423Q0 are AEC-Q100 Grade 0 Qualified (-40°C to +150°C Operating Junction Temperature)**
- **V<sub>IN</sub> Range From 4.5V to 75V**
- **High-Side Adjustable Current Sense**
- **2Ω, 1A Peak MosFET Gate Driver**
- **Input Under-Voltage and Output Over-Voltage Protection**
- **PWM and Analog Dimming**
- **Cycle-by-Cycle Current Limit**
- **Programmable Switching Frequency**
- **"Zero Current" Shutdown and Thermal Shutdown**
- **LED Output Status Flag (LM3423/23Q1/23Q0 Only)**
- **Fault Status Flag and Timer (LM3423/23Q1/23Q0 Only)**

### APPLICATIONS

- **LED Drivers - Buck, Boost, Buck-Boost, and SEPIC**
- **Indoor and Outdoor Area SSL**
- **Automotive**
- **General Illumination**
- **Constant-Current Regulators**

### Typical Boost Application Circuit



### DESCRIPTION

The LM3421/23 are versatile high voltage N-channel MosFET controllers for LED drivers. They can be easily configured in buck, boost, buck-boost and SEPIC topologies. This flexibility, along with an input voltage rating of 75V, makes the LM3421/23 ideal for illuminating LEDs in a large family of applications.

Adjustable high-side current sense voltage allows for tight regulation of the LED current with the highest efficiency possible. The LM3421/23 uses Predictive Off-time (PRO) control, which is a combination of peak current-mode control and a predictive off-timer. This method of control eases the design of loop compensation while providing inherent input voltage feed-forward compensation.

The LM3421/23 devices include a high-voltage startup regulator that operates over a wide input range of 4.5V to 75V. The internal PWM controller is designed for adjustable switching frequencies of up to 2.0 MHz, thus enabling compact solutions. Additional features include "zero current" shutdown, analog dimming, PWM dimming, over-voltage protection, under-voltage lock-out, cycle-by-cycle current limit, and thermal shutdown.

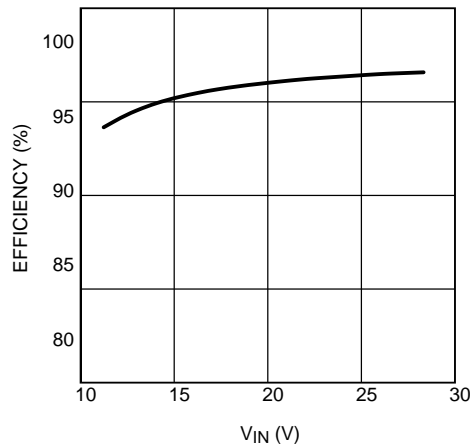
The LM3423 also includes an LED output status flag, a fault flag, a programmable fault timer, and a logic input to select the polarity of the dimming output driver.

The LM3421Q1/23Q1 are AEC-Q100 grade 1 qualified and LM3421Q0/23Q0 are AEC-Q100 grade 0 qualified.



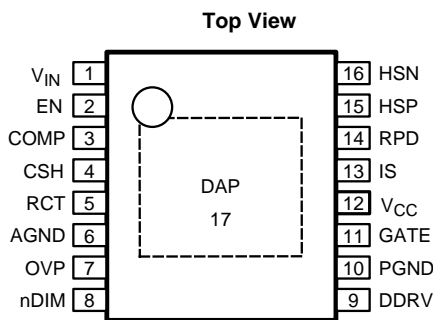
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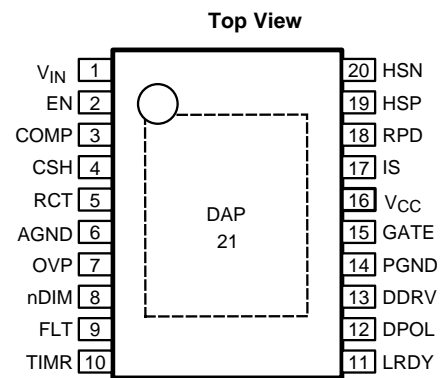


**Figure 1. Boost Evaluation Board  
9 Series LEDs at 1A**

**Connection Diagrams**



**Figure 2. 16-Lead TSSOP  
Package Number PWP**



**Figure 3. 20-Lead TSSOP  
Package Number PWP**

**PIN DESCRIPTIONS**

LM3423	LM3421	Name	Description	Function
1	1	V <sub>IN</sub>	Input Voltage	Bypass with 100 nF capacitor to AGND as close to the device as possible in the circuit board layout.
2	2	EN	Enable	Connect to AGND for zero current shutdown or apply > 2.4V to enable device.
3	3	COMP	Compensation	Connect a capacitor to AGND to set the compensation.
4	4	CSH	Current Sense High	Connect a resistor to AGND to set the signal current. For analog dimming, connect a controlled current source or a potentiometer to AGND as detailed in the <a href="#">ANALOG DIMMING</a> section.
5	5	RCT	Resistor Capacitor Timing	External RC network sets the predictive “off-time” and thus the switching frequency.
6	6	AGND	Analog Ground	Connect to PGND through the DAP copper pad to provide ground return for CSH, COMP, RCT, and TIMR.
7	7	OVP	Over-Voltage Protection	Connect to a resistor divider from V <sub>O</sub> to program output over-voltage lockout (OVLO). Turn-off threshold is 1.24V and hysteresis for turn-on is provided by 23 μA current source.

**PIN DESCRIPTIONS (continued)**

LM3423	LM3421	Name	Description	Function
8	8	nDIM	Dimming Input / Under-Voltage Protection	Connect a PWM signal for dimming as detailed in the <a href="#">PWM DIMMING</a> section and/or a resistor divider from $V_{IN}$ to program input under-voltage lockout (UVLO). Turn-on threshold is 1.24V and hysteresis for turn-off is provided by 23 $\mu$ A current source.
9	-	FLT	Fault Flag	Connect to pull-up resistor from $V_{IN}$ and N-channel MosFET open drain output is high when a fault condition is latched by the timer.
10	-	TIMR	Fault Timer	Connect a capacitor to AGND to set the time delay before a sensed fault condition is latched.
11	-	LRDY	LED Ready Flag	Connect to pull-up resistor from $V_{IN}$ and N-channel MosFET open drain output pulls down when the LED current is not in regulation.
12	-	DPOL	Dim Polarity	Connect to AGND if dimming with a series P-channel MosFET or leave open when dimming with series N-channel MosFET.
13	9	DDRV	Dim Gate Drive Output	Connect to the gate of the dimming MosFET.
14	10	PGND	Power Ground	Connect to AGND through the DAP copper pad to provide ground return for GATE and DDRV.
15	11	GATE	Main Gate Drive Output	Connect to the gate of the main switching MosFET.
16	12	$V_{CC}$	Internal Regulator Output	Bypass with 2.2 $\mu$ F–3.3 $\mu$ F ceramic capacitor to PGND.
17	13	IS	Main Switch Current Sense	Connect to the drain of the main N-channel MosFET switch for $R_{DS-ON}$ sensing or to a sense resistor installed in the source of the same device.
18	14	RPD	Resistor Pull Down	Connect the low side of all external resistor dividers ( $V_{IN}$ UVLO, OVP) to implement “zero-current” shutdown.
19	15	HSP	LED Current Sense Positive	Connect through a series resistor to the positive side of the LED current sense resistor.
20	16	HSN	LED Current Sense Negative	Connect through a series resistor to the negative side of the LED current sense resistor.
DAP (21)	DAP (17)	DAP	Thermal PAD on bottom of IC	Star ground, connecting AGND and PGND. For thermal considerations please refer to <sup>(1)</sup> .

- (1) Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for an reference layout wherein the 16L TSSOP package has its EP pad populated with 9 vias and the 20L TSSOP has its EP pad populated with 12 vias. In applications where high maximum power dissipation exists, namely driving a large MosFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^{\circ}\text{C}$  for Q1, or  $150^{\circ}\text{C}$  for Q0), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$ . In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be 104  $^{\circ}\text{C}/\text{W}$  for the 16L TSSOP and 86.7  $^{\circ}\text{C}/\text{W}$  for the 20L TSSOP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)(2)</sup>

$V_{IN}$ , EN, RPD, nDIM		-0.3V to 76.0V -1 mA continuous
OVP, HSP, HSN, LRDY, FLT, DPOL		-0.3V to 76.0V -100 $\mu$ A continuous
RCT		-0.3V to 76.0V -1 mA to +5 mA continuous
IS		-0.3V to 76.0V -2V for 100 ns -1mA continuous
$V_{CC}$		-0.3V to 8.0V
TIMR		-0.3V to 7.0V -100 $\mu$ A to +100 $\mu$ A Continuous
COMP, CSH		-0.3V to 6.0V -200 $\mu$ A to +200 $\mu$ A Continuous
GATE, DDRV		-0.3V to $V_{CC}$ -2.5V for 100 ns $V_{CC}$ +2.5V for 100 ns -1 mA to +1 mA continuous
PGND		-0.3V to 0.3V -2.5V to 2.5V for 100 ns
Maximum Junction Temperature		Internally Limited
Storage Temperature Range		-65°C to +150°C
Maximum Lead Temperature (Solder and Reflow) <sup>(3)</sup>		260°C
Continuous Power Dissipation		Internally Limited
ESD Susceptibility <sup>(4)</sup>	Human Body Model	2 kV
	Charge Device Model	500V CSH pin 750V all other pins

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the AGND pin, unless otherwise specified.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Refer to <http://www.ti.com/packaging> for more detailed information and mounting techniques.
- (4) The human body model is a 100 pF capacitor discharged through a 1.5 k $\Omega$  resistor into each pin. The applicable standard is JESD22-A114C.

### Operating Conditions <sup>(1)</sup>

Operating Junction Temperature Range	LM3421, LM3421Q1, LM3423, LM3423Q1	-40°C to +125°C
	LM3421Q0, LM3423Q0	-40°C to +150°C
Input Voltage $V_{IN}$		4.5V to 75V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the AGND pin, unless otherwise specified.

## Electrical Characteristics <sup>(1)</sup>

Specifications in standard type face are for  $T_J = 25^\circ\text{C}$  and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  for LM3421Q0/LM3423Q0,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for all others). Specifications that differ between the two operating ranges will be identified in the **Temp Range** column as Q0 for  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  and as Q1 for  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . If no temperature range is indicated then the specification holds for both Q1 and Q0. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = +25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise stated the following condition applies:  $V_{IN} = +14\text{V}$ .

Symbol	Parameter	Conditions	Temp Range	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
<b>STARTUP REGULATOR</b>							
$V_{CCREG}$	$V_{CC}$ Regulation	$I_{CC} = 0\text{ mA}$		<b>6.30</b>	6.90	<b>7.35</b>	V
$I_{CCLIM}$	$V_{CC}$ Current Limit	$V_{CC} = 0\text{V}$		<b>20</b>	25		mA
$I_Q$	Quiescent Current	EN = 3.0V, Static	Q1		2	<b>3</b>	
			Q0			<b>3.5</b>	
$I_{SD}$	Shutdown Current	EN = 0V			0.1	1.0	$\mu\text{A}$
<b><math>V_{CC}</math> SUPPLY</b>							
$V_{CCUV}$	$V_{CC}$ UVLO Threshold	$V_{CC}$ Increasing			4.17	<b>4.50</b>	V
		$V_{CC}$ Decreasing		<b>3.70</b>	4.08		
$V_{CCHYS}$	$V_{CC}$ UVLO Hysteresis				0.1		
<b>EN THRESHOLDS</b>							
$EN_{ST}$	EN Startup Threshold	EN Increasing	Q1		1.75	<b>2.40</b>	V
			Q0			<b>2.75</b>	
		EN Decreasing		<b>0.80</b>	1.63		
$EN_{STHYS}$	EN Startup Hysteresis				0.1		
$R_{EN}$	EN Pulldown Resistance	EN = 1V	Q1	<b>0.45</b>	0.82	<b>1.30</b>	M $\Omega$
			Q0			<b>1.80</b>	
<b>CSH THRESHOLDS</b>							
	CSH High Fault	CSH Increasing			1.6		V
	CSH Low Condition on LRDY Pin (LM3423)	CSH increasing			1.0		
<b>OV THRESHOLDS</b>							
$OVP_{CB}$	OVP OVLO Threshold	OVP Increasing		<b>1.185</b>	1.240	<b>1.285</b>	V
$OVP_{HYS}$	OVP Hysteresis Source Current	OVP Active (high)	Q1	<b>20</b>	23	<b>25</b>	$\mu\text{A}$
			Q0			<b>26</b>	
<b>DPOL THRESHOLDS</b>							
$DPOL_{THRES_H}$	DPOL Logic Threshold	DPOL Increasing		<b>2.0</b>	2.3	<b>2.6</b>	V
$R_{DPOL}$	DPOL Pullup Resistance				500	<b>1200</b>	k $\Omega$
<b>FAULT TIMER</b>							
$V_{FLTTH}$	Fault Threshold		Q1	<b>1.185</b>	1.240	<b>1.285</b>	V
			Q0			<b>1.290</b>	
$I_{FLT}$	Fault Pin Source Current		Q1	<b>10.0</b>	11.5	<b>13.0</b>	$\mu\text{A}$
			Q0			<b>13.5</b>	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the AGND pin, unless otherwise specified.
- (2) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
- (3) Typical numbers are at  $25^\circ\text{C}$  and represent the most likely norm.

## Electrical Characteristics <sup>(1)</sup> (continued)

Specifications in standard type face are for  $T_J = 25^\circ\text{C}$  and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  for LM3421Q0/LM3423Q0,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for all others). Specifications that differ between the two operating ranges will be identified in the **Temp Range** column as Q0 for  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  and as Q1 for  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . If no temperature range is indicated then the specification holds for both Q1 and Q0. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = +25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise stated the following condition applies:  $V_{IN} = +14\text{V}$ .

Symbol	Parameter	Conditions	Temp Range	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
<b>ERROR AMPLIFIER</b>							
$V_{REF}$	CSH Reference Voltage	With Respect to AGND		<b>1.210</b>	1.235	<b>1.260</b>	V
	Error Amplifier Input Bias Current			-0.6	0	0.6	$\mu\text{A}$
	COMP Sink / Source Current		Q1	<b>22</b>	30	<b>35</b>	
			Q0			<b>36</b>	
	Transconductance				100		$\mu\text{A/V}$
	Linear Input Range	<sup>(4)</sup>			$\pm 125$		mV
	Transconductance Bandwidth	-6dB Unloaded Response <sup>(4)</sup>		0.5	1.0		MHz
<b>OFF TIMER</b>							
	Minimum Off-time	RCT = 1V through 1 k $\Omega$	Q1		35	<b>75</b>	ns
			Q0			<b>90</b>	
$R_{RCT}$	RCT Reset Pull-down Resistance		Q1		36	<b>120</b>	$\Omega$
			Q0			<b>125</b>	
$V_{RCT}$	$V_{IN}/25$ Reference Voltage	$V_{IN} = 14\text{V}$	Q1	<b>540</b>	565	<b>585</b>	mV
			Q0			<b>590</b>	
f	Continuous Conduction Switching Frequency	$2.2 \text{ nF} > C_T > 470 \text{ pF}$			$25/(C_T R_T)$		Hz
<b>PWM COMPARATOR</b>							
	COMP to PWM Offset			<b>700</b>	800	<b>900</b>	mV
<b>CURRENT LIMIT (IS)</b>							
$I_{LIM}$	Current Limit Threshold			<b>215</b>	245	<b>275</b>	mV
	$I_{LIM}$ Delay to Output		Q1		35	<b>75</b>	ns
			Q0			<b>90</b>	
	Leading Edge Blanking Time			<b>115</b>	210	<b>325</b>	
<b>HIGH SIDE TRANSCONDUCTANCE AMPLIFIER</b>							
	Input Bias Current				11.5		$\mu\text{A}$
	Transconductance			<b>20</b>	119		mA/V
	Input Offset Current			<b>-1.5</b>	0	<b>1.5</b>	$\mu\text{A}$
	Input Offset Voltage			<b>-7</b>	0	<b>7</b>	mV
	Transconductance Bandwidth	$I_{CSH} = 100 \mu\text{A}$ <sup>(4)</sup>		250	500		kHz
<b>GATE DRIVER (GATE)</b>							
$R_{SRC(GATE)}$	GATE Sourcing Resistance	GATE = High			2.0	<b>6.0</b>	$\Omega$
$R_{SNK(GATE)}$	GATE Sinking Resistance	GATE = Low			1.3	<b>4.5</b>	
<b>DIM DRIVER (DIM, DDRV)</b>							
$nDIM_{VTH}$	nDIM / UVLO Threshold			<b>1.185</b>	1.240	<b>1.285</b>	V
$nDIM_{HYS}$	nDIM Hysteresis Current		Q1	<b>20</b>	23	<b>25</b>	$\mu\text{A}$
			Q0			<b>26</b>	
$R_{SRC(DDRV)}$	DDRV Sourcing Resistance	DDRV = High			13.5	<b>30.0</b>	$\Omega$
$R_{SNK(DDRV)}$	DDRV Sinking Resistance	DDRV = Low			3.5	<b>10.0</b>	

(4) These electrical parameters are specified by design, and are not verified by test.

## Electrical Characteristics <sup>(1)</sup> (continued)

Specifications in standard type face are for  $T_J = 25^\circ\text{C}$  and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  for LM3421Q0/LM3423Q0,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  for all others). Specifications that differ between the two operating ranges will be identified in the **Temp Range** column as Q0 for  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  and as Q1 for  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ . If no temperature range is indicated then the specification holds for both Q1 and Q0. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = +25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise stated the following condition applies:  $V_{IN} = +14\text{V}$ .

Symbol	Parameter	Conditions	Temp Range	Min <sup>(2)</sup>	Typ <sup>(3)</sup>	Max <sup>(2)</sup>	Units
<b>PULL-DOWN N-CHANNEL MosFETS</b>							
R <sub>RPD</sub>	RPD Pull-down Resistance		Q1		145	<b>300</b>	Ω
			Q0			<b>350</b>	
R <sub>FLT</sub>	FLT Pull-down Resistance		Q1		145	<b>300</b>	
			Q0			<b>350</b>	
R <sub>LRDY</sub>	LRDY Pull-down Resistance		Q1		135	<b>300</b>	
			Q0			<b>350</b>	
<b>THERMAL SHUTDOWN</b>							
T <sub>SD</sub>	Thermal Shutdown Threshold	<sup>(4)</sup>	Q1		165		°C
			Q0		210		
T <sub>HYS</sub>	Thermal Shutdown Hysteresis	<sup>(4)</sup>			25		
<b>THERMAL RESISTANCE</b>							
θ <sub>JA</sub>	Junction to Ambient <sup>(5)</sup>	16L TSSOP			37.4		°C/W
		20L TSSOP			34.0		
θ <sub>JC</sub>	Junction to Exposed Pad (EP)	16L TSSOP			2.3		°C/W
		20L TSSOP			2.3		

- (5) Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for an reference layout wherein the 16L TSSOP package has its EP pad populated with 9 vias and the 20L TSSOP has its EP pad populated with 12 vias. In applications where high maximum power dissipation exists, namely driving a large MosFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^\circ\text{C}$  for Q1, or  $150^\circ\text{C}$  for Q0), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$ . In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be  $104^\circ\text{C/W}$  for the 16L TSSOP and  $86.7^\circ\text{C/W}$  for the 20L TSSOP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.

## Typical Performance Characteristics

$T_A = +25^\circ\text{C}$  and  $V_{IN} = 14\text{V}$  unless otherwise specified

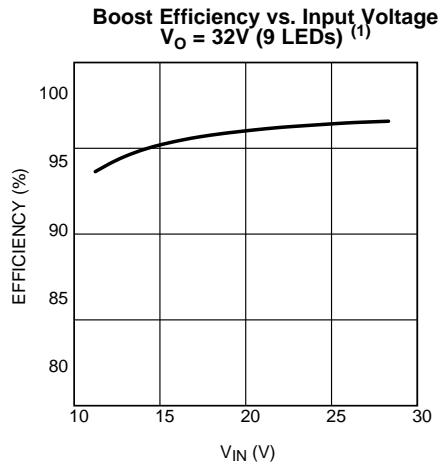


Figure 4.

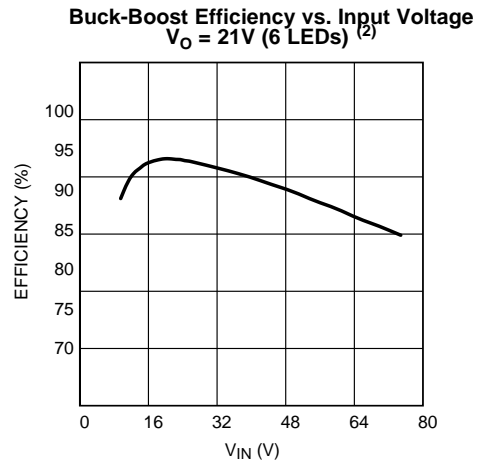


Figure 5.

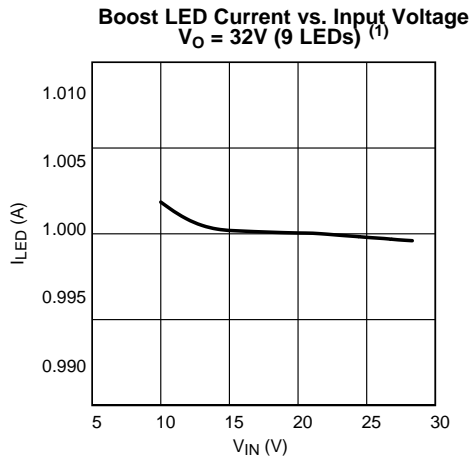


Figure 6.

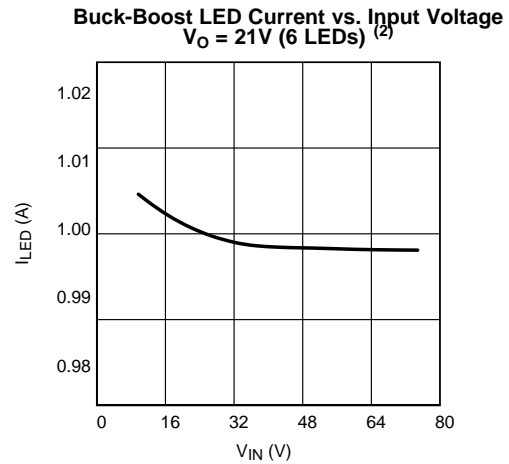


Figure 7.

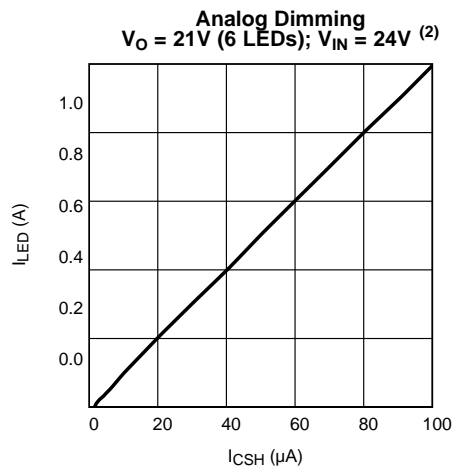


Figure 8.

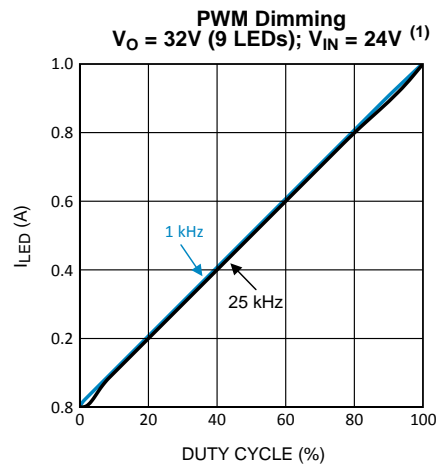


Figure 9.

(1) The measurements were made using the standard boost evaluation board from SNVA416.

(2) The measurements were made using the standard buck-boost evaluation board from .



Typical Performance Characteristics (continued)

T<sub>A</sub>=+25°C and V<sub>IN</sub> = 14V unless otherwise specified

V<sub>CSH</sub> vs. Junction Temperature

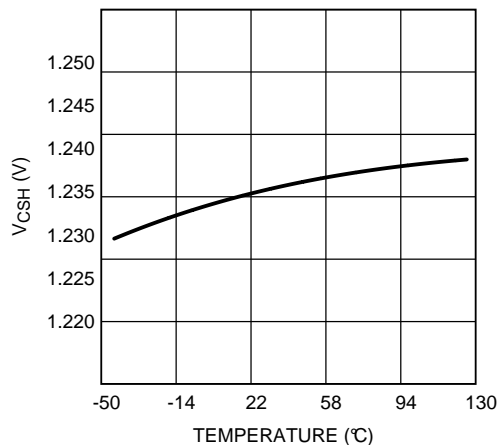


Figure 10.

V<sub>CC</sub> vs. Junction Temperature

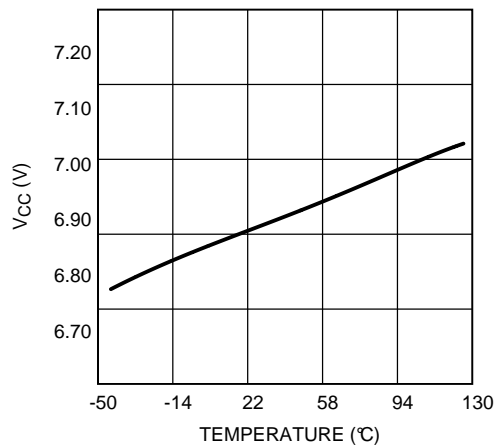


Figure 11.

V<sub>RCT</sub> vs. Junction Temperature

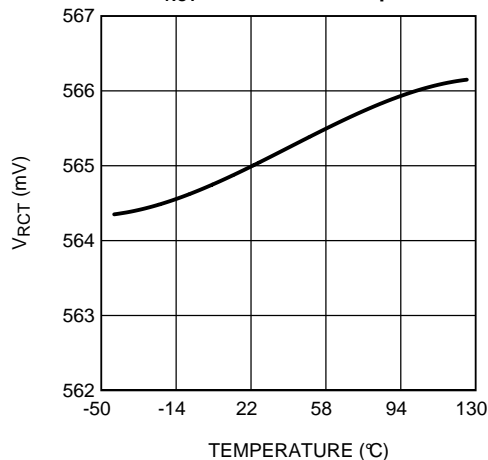


Figure 12.

V<sub>LIM</sub> vs. Junction Temperature

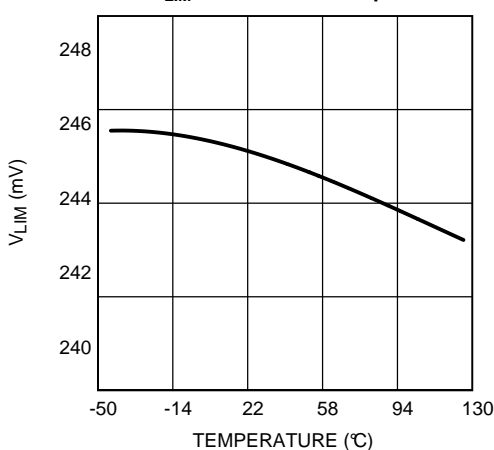


Figure 13.

t<sub>ON-MIN</sub> vs. Junction Temperature

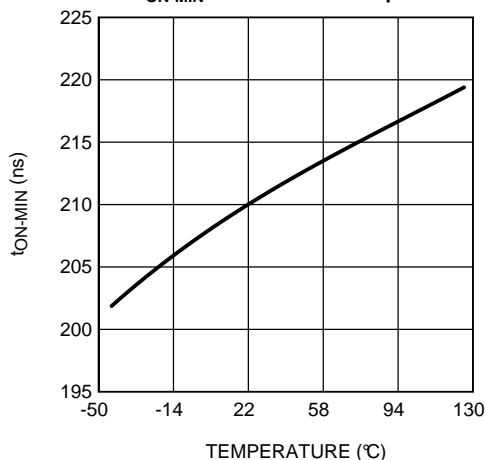
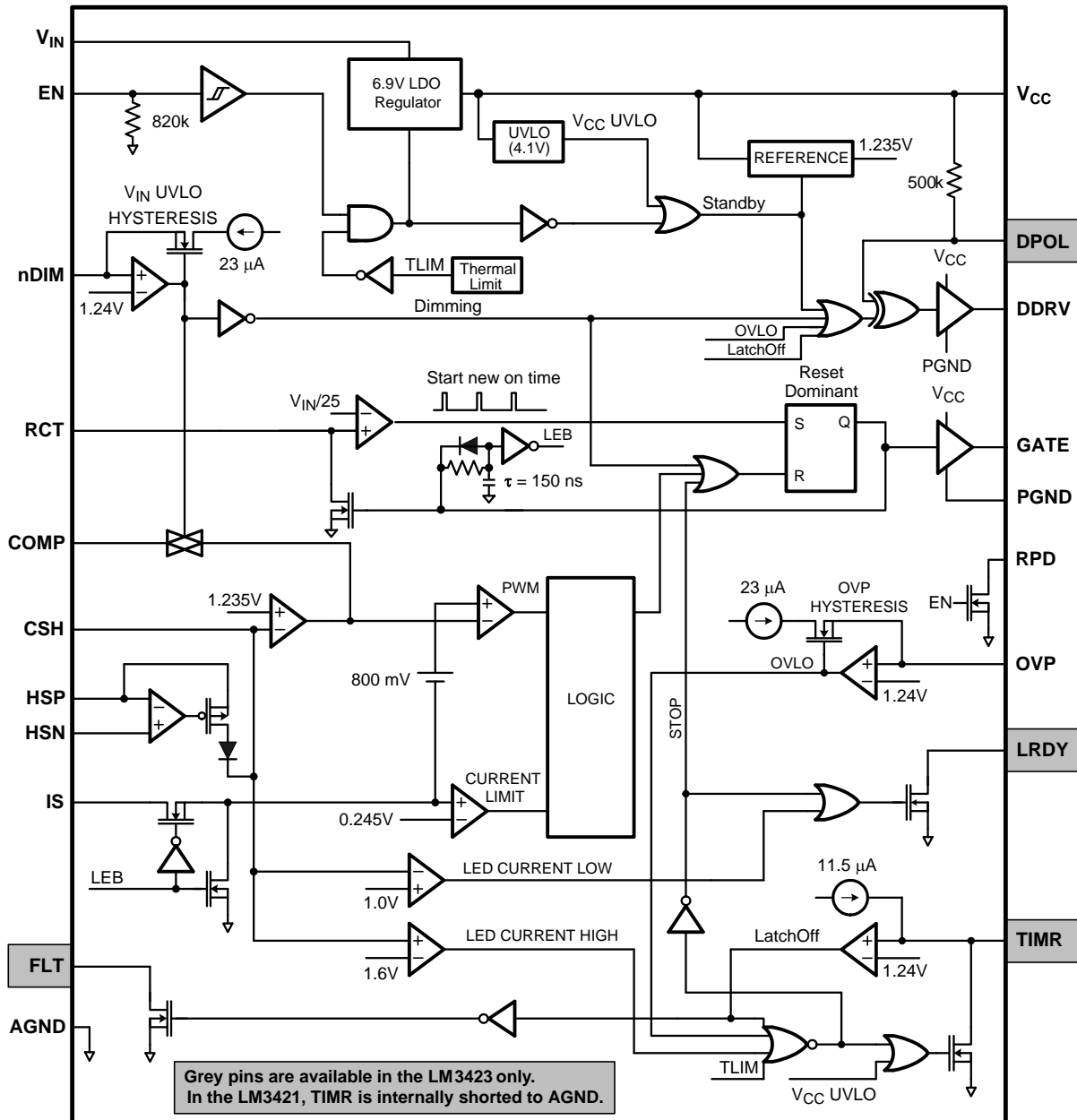


Figure 14.

## BLOCK DIAGRAM



## THEORY OF OPERATION

The LM3421/23 are N-channel MosFET (NFET) controllers for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency. The LM3421/23 uses a Predictive Off-time (PRO) control architecture that allows the regulator to be operated using minimal external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the output enable/disable

function with external dimming FET driver allows for fast PWM dimming of the LED load. When designing, the maximum attainable LED current is not internally limited because the LM3421/23 is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM3421/23 to easily provide constant currents up to 5A. This controller contains all the features necessary to implement a high efficiency versatile LED driver.

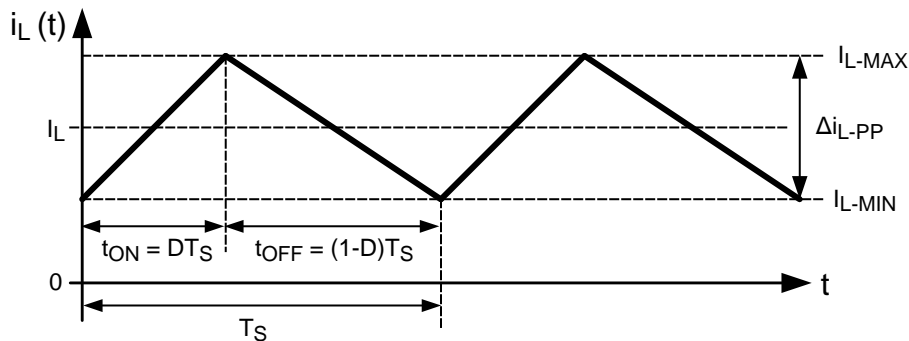


Figure 15. Ideal CCM Regulator Inductor Current  $i_L(t)$

## CURRENT REGULATORS

Current regulators can be designed to accomplish three basic functions: buck, boost, and buck-boost. All three topologies in their most basic form contain a main switching MosFET, a recirculating diode, an inductor and capacitors. The LM3421/23 is designed to drive a ground referenced NFET which is perfect for a standard boost regulator. Buck and buck-boost regulators, on the other hand, usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch can be used to drive a floating load instead. The LM3421/23 can then be used to drive all three basic topologies as shown in the [Basic Topology Schematics](#) section. Other topologies such as the SEPIC and flyback converter (both derivatives of the buck-boost) can be implemented as well.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the NFET (Q1) is turned on ( $t_{ON}$ ), the input voltage source stores energy in the inductor (L1) while the output capacitor ( $C_O$ ) provides energy to the LED load. When Q1 is turned off ( $t_{OFF}$ ), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both  $C_O$  and the LED load. [Figure 15](#) shows the inductor current ( $i_L(t)$ ) waveform for a regulator operating in CCM.

The average output LED current ( $I_{LED}$ ) is proportional to the average inductor current ( $I_L$ ), therefore if  $I_L$  is tightly controlled,  $I_{LED}$  will be well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate  $I_L$  and ultimately  $I_{LED}$ . For any current regulator, D is a function of the conversion ratio:

### Buck

$$D = \frac{V_O}{V_{IN}} \quad (1)$$

### Boost

$$D = \frac{V_O - V_{IN}}{V_O} \quad (2)$$

### Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \quad (3)$$

## PREDICTIVE OFF-TIME (PRO) CONTROL

PRO control is used by the LM3421/23 to control  $I_{LED}$ . It is a combination of average peak current control and a one-shot off-timer that varies with input voltage. The LM3421/23 uses peak current control to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MosFET path or the MosFET  $R_{DS-ON}$  for both cycle-by-cycle current limit and input voltage feed forward. D is indirectly controlled by changes in both  $t_{OFF}$  and  $t_{ON}$ , which vary depending on the operating point.

Even though the off-time control is quasi-hysteretic, the input voltage proportionality in the off-timer creates an essentially constant switching frequency over the entire operating range for boost and buck-boost topologies. The buck topology can be designed to give constant ripple over either input voltage or output voltage, however switching frequency is only constant at a specific operating point.

This type of control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. The averaging mechanism in the peak detection control loop provides extremely accurate LED current regulation over the entire operating range.

PRO control was designed to mitigate “current mode instability” (also called “sub-harmonic oscillation”) found in standard peak current mode control when operating near or above 50% duty cycles. When using standard peak current mode control with a fixed switching frequency, this condition is present, regardless of the topology. However, using a constant off-time approach, current mode instability cannot occur, enabling easier design and control.

Predictive off-time advantages:

- There is no current mode instability at any duty cycle.
- Higher duty cycles / voltage transformation ratios are possible, especially in the boost regulator.

The only disadvantage is that synchronization to an external reference frequency is generally not available.

## SWITCHING FREQUENCY

An external resistor ( $R_T$ ) connected between the RCT pin and the switch node (where D1, Q1, and L1 connect), in combination with a capacitor ( $C_T$ ) between the RCT and AGND pins, sets the off-time ( $t_{OFF}$ ) as shown in [Figure 16](#). For boost and buck-boost topologies, the  $V_{IN}$  proportionality ensures a virtually constant switching frequency ( $f_{SW}$ ).

For a buck topology,  $R_T$  and  $C_T$  are also used to set  $t_{OFF}$ , however the  $V_{IN}$  proportionality will not ensure a constant switching frequency. Instead, constant ripple operation can be achieved. Changing the connection of  $R_T$  in [Figure 16](#) from  $V_{SW}$  to  $V_{IN}$  will provide a constant ripple over varying  $V_{IN}$ . Adding a PNP transistor as shown in [Figure 17](#) will provide constant ripple over varying  $V_O$ .

The switching frequency is defined:

### Buck (Constant Ripple vs. $V_{IN}$ )

$$f_{SW} = \frac{25 \times (V_{IN} - V_O)}{R_T \times C_T \times V_{IN}} \quad (4)$$

### Buck (Constant Ripple vs. $V_O$ )

$$f_{SW} = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{R_T \times C_T \times V_{IN}^2} \quad (5)$$

### Boost and Buck-boost

$$f_{SW} = \frac{25}{R_T \times C_T} \quad (6)$$

For all topologies, the  $C_T$  capacitor is recommended to be 1 nF and should be located very close to the LM3421/23.

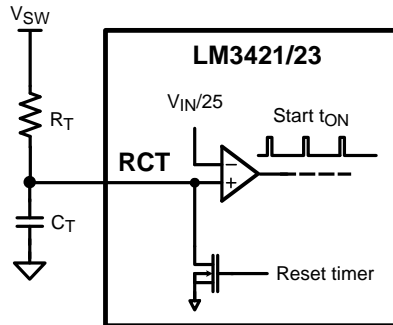


Figure 16. Off-timer Circuitry for Boost and Buck-boost Regulators

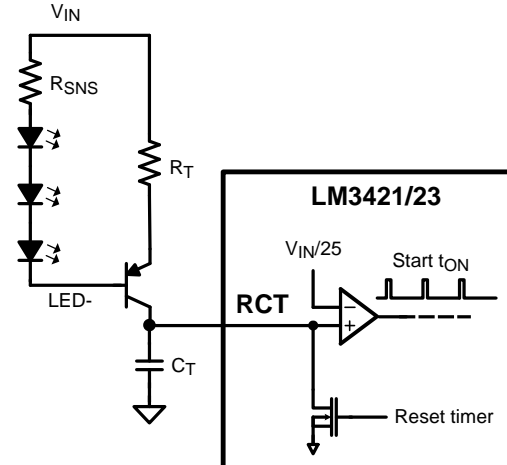


Figure 17. Off-timer Circuitry for Buck Regulators

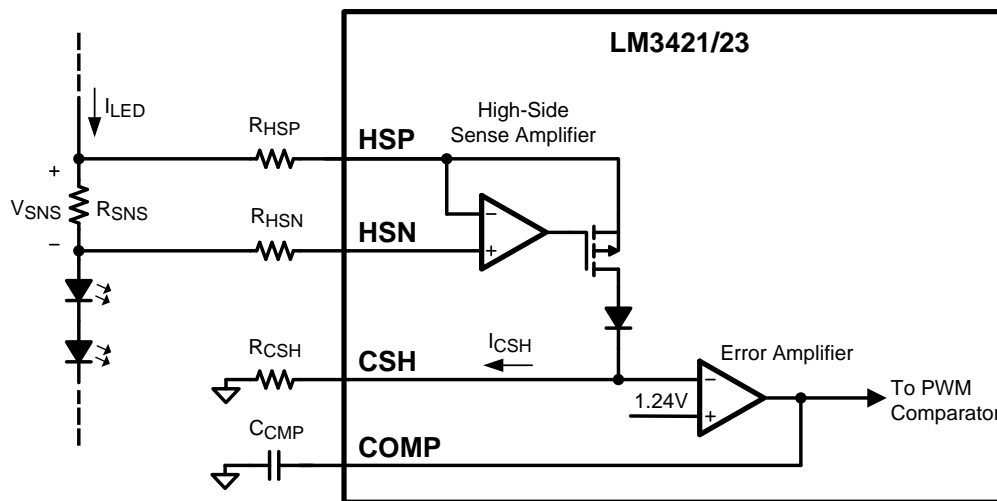


Figure 18. LED Current Sense Circuitry

## AVERAGE LED CURRENT

The LM3421/23 uses an external current sense resistor ( $R_{SNS}$ ) placed in series with the LED load to convert the LED current ( $I_{LED}$ ) into a voltage ( $V_{SNS}$ ) as shown in Figure 18. The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential ( $V_{HSP}=V_{HSN}$ ) through negative feedback. Because of this, the  $V_{SNS}$  voltage is forced across  $R_{HSP}$  to generate the signal current ( $I_{CSH}$ ) which flows out of the CSH pin and through the  $R_{CSH}$  resistor. The error amplifier will regulate the CSH pin to 1.24V, therefore  $I_{CSH}$  can be calculated:

$$I_{CSH} = \frac{V_{SNS}}{R_{HSP}} \quad (7)$$

This means  $V_{SNS}$  will be regulated as follows:

$$V_{SNS} = 1.24V \times \frac{R_{HSP}}{R_{CSH}} \quad (8)$$

$I_{LED}$  can then be calculated:

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{1.24V}{R_{SNS}} \times \frac{R_{HSP}}{R_{CSH}} \quad (9)$$

The selection of the three resistors ( $R_{SNS}$ ,  $R_{CSH}$ , and  $R_{HSP}$ ) is not arbitrary. For matching and noise performance, the suggested signal current  $I_{CSH}$  is approximately 100  $\mu$ A. This current does not flow in the LEDs and will not affect either the off-state LED current or the regulated LED current.  $I_{CSH}$  can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum  $V_{SNS}$  is suggested to be 50 mV. Finally, a resistor ( $R_{HSN} = R_{HSP}$ ) should be placed in series with the HSN pin to cancel out the effects of the input bias current ( $\sim 10 \mu$ A) of both inputs of the high-side sense amplifier.

The sense resistor ( $R_{SNS}$ ) can be placed anywhere in the series string of LEDs as long as the voltage at the HSN and HSP pins ( $V_{HSP}$  and  $V_{HSN}$ ) satisfies the following conditions.

$$\begin{aligned} V_{HSP} &< 76V \\ V_{HSN} &> 3.5V \end{aligned} \tag{10}$$

Typically, for a buck-boost configuration,  $R_{SNS}$  is placed at the bottom of the string (LED-) which allows for greater flexibility of input and output voltage. However, if there is substantial input voltage ripple allowed, it can help to place  $R_{SNS}$  at the top of the string (LED+) which limits the output voltage of the string to:

$$V_O = 76V - V_{IN} \tag{11}$$

Note that the CSH pin can also be used as a low-side current sense input regulated to 1.24V. The high-side sense amplifier is disabled if HSP and HSN are tied to AGND (or  $V_{HSN} > V_{HSP}$ ).

## ANALOG DIMMING

The CSH pin can be used to analog dim the LED current by adjusting the current sense voltage ( $V_{SNS}$ ). There are several different methods to adjust  $V_{SNS}$  using the CSH pin:

1. External variable resistance : Adjust a potentiometer placed in series with  $R_{CSH}$  to vary  $V_{SNS}$ .
2. External variable current source: Source current (0  $\mu$ A to  $I_{CSH}$ ) into the CSH pin to adjust  $V_{SNS}$ .

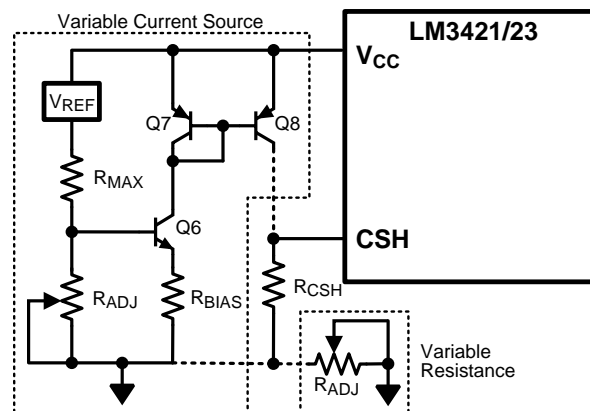


Figure 19. Analog Dimming Circuitry

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 19 shows how both CSH methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin since the potentiometer increases the size of the signal current loop.

Method 2 provides a complete dimming range and better noise performance, though it is more complex. It consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer ( $R_{ADJ}$ ), where  $R_{ADJ}$  controls the amount of current sourced into the CSH pin. A higher resistance value will source more current into the CSH pin causing less regulated signal current through  $R_{HSP}$ , effectively dimming the LEDs.  $V_{REF}$  should be a precise external voltage reference, while Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current ( $I_{ADD}$ ) sourced into the CSH pin can be calculated:

$$I_{ADD} = \frac{\left( \frac{R_{ADJ} \times V_{REF}}{R_{ADJ} + R_{MAX}} \right) - V_{BE-Q6}}{R_{BIAS}} \quad (12)$$

The corresponding  $I_{LED}$  for a specific  $I_{ADD}$  is:

$$I_{LED} = (I_{CSH} - I_{ADD}) \times \left( \frac{R_{HSP}}{R_{SNS}} \right) \quad (13)$$

### CURRENT SENSE/CURRENT LIMIT

The LM3421/23 achieves peak current mode control using a comparator that monitors the main MosFET (Q1) transistor current, comparing it with the COMP pin voltage as shown in Figure 20. Further, it incorporates a cycle-by-cycle over-current protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MosFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 210 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time ( $t_{ON-MIN}$ ).

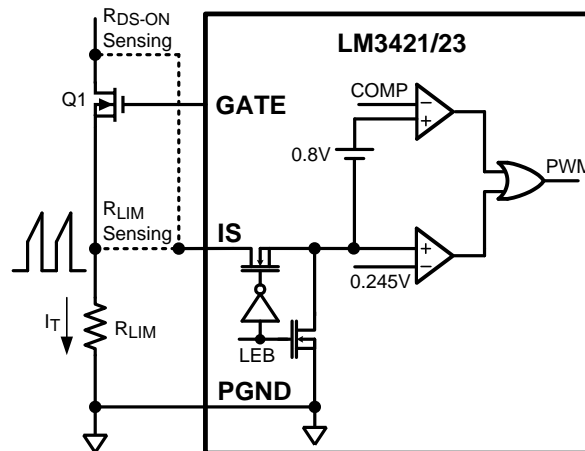


Figure 20. Current Sense / Current Limit Circuitry

There are two possible methods to sense the transistor current. The  $R_{DS-ON}$  of the main power MosFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MosFET is in the off state. Alternatively, a sense resistor located in the source of the MosFET may be used for current sensing, however a low inductance (ESL) type is suggested. The cycle-by-cycle current limit ( $I_{LIM}$ ) can be calculated using either method as the limiting resistance ( $R_{LIM}$ ):

$$I_{LIM} = \frac{245 \text{ mV}}{R_{LIM}} \quad (14)$$

## OVER-CURRENT PROTECTION

The LM3421/23 devices have a secondary method of over-current protection. Switching action is disabled whenever the current in the LEDs is more than 30% above the regulation set point. The dimming MosFET switch driver (DDRV) is not disabled however as this would immediately remove the fault condition and cause oscillatory behavior.

## ZERO CURRENT SHUTDOWN

The LM3421/23 devices implement "zero current" shutdown via the EN and RPD pins. When pulled low, the EN pin places the devices into near-zero current state, where only the leakage currents will be observed at the pins (typical 0.1  $\mu$ A). The applications circuits, frequently have resistor dividers to set UVLO, OVLO, or other similar functions. The RPD pin is an open drain N-channel MosFET that is enabled only when the device is enabled. Tying the bottom of all resistor dividers to the RPD pin as shown in [Figure 21](#) allows them to float during shutdown, thus removing their current paths and providing true application-wide zero current shutdown.

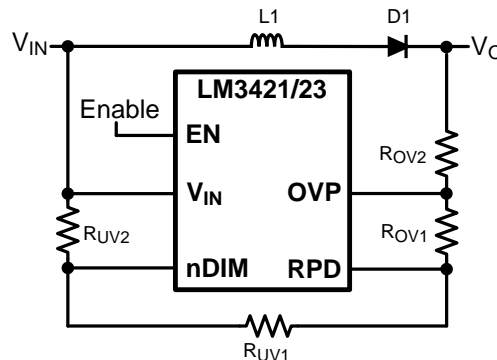


Figure 21. Zero Current Shutdown Circuit

## CONTROL LOOP COMPENSATION

The LM3421/23 control loop is modeled like any current mode controller. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high frequency pole in the model, however it is near the switching frequency and plays no part in the compensation design process therefore it will be neglected. Since ceramic capacitance is recommended for use with LED drivers due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. Finally, there is a DC gain of the uncompensated loop which is dependent on internal controller gains and the external sensing network.

A buck-boost regulator will be used as an example case. See the [Design Guide](#) section for compensation of all topologies.

The uncompensated loop gain for a buck-boost regulator is given by the following equation:

$$T_U = T_{U0} \times \left( \frac{1 - \frac{s}{\omega_{Z1}}}{1 + \frac{s}{\omega_{P1}}} \right) \quad (15)$$

Where the uncompensated DC loop gain of the system is described as:

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \quad (16)$$

And the output pole ( $\omega_{P1}$ ) is approximated:

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \quad (17)$$



And the right half plane zero ( $\omega_{z1}$ ) is:

$$\omega_{z1} = \frac{r_D \times D^2}{D \times L1} \tag{18}$$

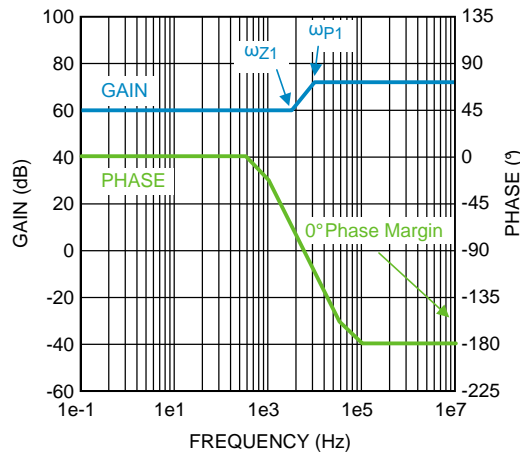


Figure 22. Uncompensated Loop Gain Frequency Response

Figure 22 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while losing 45°/decade of phase which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high frequency pole (not modeled or shown in figure). The phase will be below  $-180^\circ$  at the crossover frequency which means there is no phase margin ( $180^\circ + \text{phase at crossover frequency}$ ) causing system instability. Even if the output pole is below the RHP zero, the phase will still reach  $-180^\circ$  before the crossover frequency in most cases yielding instability.

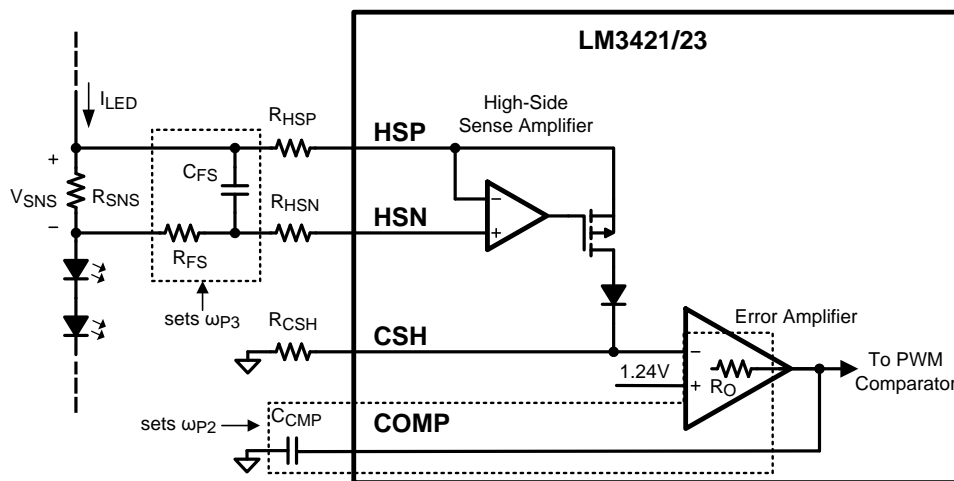


Figure 23. Compensation Circuitry

To mitigate this problem, a compensator should be designed to give adequate phase margin (above  $45^\circ$ ) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin ( $C_{CMP}$ ) will add a dominant pole to the system, which will ensure adequate phase margin if placed low enough. At high duty cycles (as shown in Figure 22), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach. The dominant compensation pole ( $\omega_{p2}$ ) is determined by  $C_{CMP}$  and the output resistance ( $R_O$ ) of the error amplifier (typically 5 M $\Omega$ ):

$$\omega_{P2} = \frac{1}{5e^6 \Omega \times C_{CMP}} \quad (19)$$

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate switching noise and, in some cases, provide better gain margin. This pole can be placed across  $R_{SNS}$  to filter the ESL of the sense resistor at the same time. Figure 23 shows how the compensation is physically implemented in the system.

The high frequency pole ( $\omega_{P3}$ ) can be calculated:

$$\omega_{P3} = \frac{1}{R_{FS} \times C_{FS}} \quad (20)$$

The total system transfer function becomes:

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (21)$$

The resulting compensated loop gain frequency response shown in Figure 24 indicates that the system has adequate phase margin (above  $45^\circ$ ) if the dominant compensation pole is placed low enough, ensuring stability:

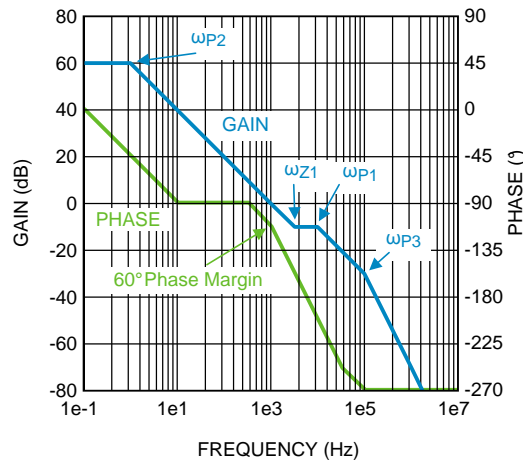


Figure 24. Compensated Loop Gain Frequency Response

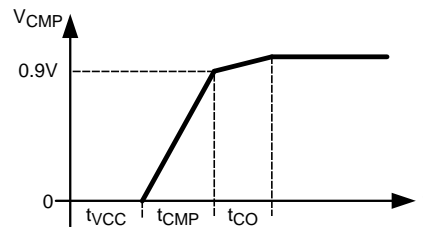


Figure 25. Start-Up Waveforms

## START-UP REGULATOR

The LM3421/23 includes a high voltage, low dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor ( $C_{BYP}$ ) connected to the  $V_{CC}$  pin. The recommended bypass capacitance for the  $V_{CC}$  regulator is 2.2  $\mu$ F to 3.3  $\mu$ F. The output of the  $V_{CC}$  regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited. Figure 25 shows the typical start-up waveforms for the LM3421/23.

First,  $C_{BYP}$  is charged to be above  $V_{CC}$  UVLO threshold ( $\sim 4.2$ V). The  $C_{VCC}$  charging time ( $t_{VCC}$ ) can be estimated as:

$$t_{VCC} = \frac{4.2V}{25 \text{ mA}} \times C_{BYP} = 168\Omega \times C_{BYP} \quad (22)$$

$C_{CMP}$  is then charged to 0.9V over the charging time ( $t_{CMP}$ ) which can be estimated as:

$$t_{CMP} = \frac{0.9V}{25 \mu A} \times C_{CMP} = 36 \text{ k}\Omega \times C_{CMP} \quad (23)$$

Once  $C_{CMP} = 0.9$ V, the part starts switching to charge  $C_O$  until the LED current is in regulation. The  $C_O$  charging time ( $t_{CO}$ ) can be roughly estimated as:

$$t_{CO} = C_O \times \frac{V_O}{I_{LED}} \quad (24)$$

The system start-up time ( $t_{SU}$ ) is defined as:

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \quad (25)$$

In some configurations, the start-up waveform will overshoot the steady state COMP pin voltage. In this case, the LED current and output voltage will overshoot also, which can trip the over-voltage or protection, causing a race condition. The easiest way to prevent this is to use a larger compensation capacitor ( $C_{CMP}$ ), thereby slowing down the control loop.

## OVER-VOLTAGE LOCKOUT (OVLO)

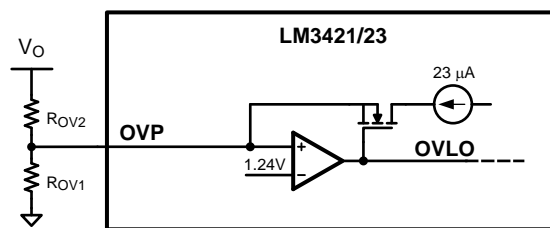


Figure 26. Over-Voltage Protection Circuitry

The LM3421/23 can be configured to detect an output (or input) over-voltage condition via the OVP pin. The pin features a precision 1.24V threshold with 23  $\mu$ A (typical) of hysteresis current as shown in Figure 26. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 23  $\mu$ A current source provides hysteresis to the lower threshold of the OVLO hysteric band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage ( $V_O$ ) should be sensed and translated to ground by using a single PNP as shown in Figure 27.

The over-voltage turn-off threshold ( $V_{TURN-OFF}$ ) is defined:

### Ground Referenced

$$V_{TURN-OFF} = 1.24V \times \left( \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right) \quad (26)$$

## Floating

$$V_{\text{TURN-OFF}} = 1.24\text{V} \times \left( \frac{0.5 \times R_{\text{OV1}} + R_{\text{OV2}}}{R_{\text{OV1}}} \right) \quad (27)$$

In the ground referenced configuration, the voltage across  $R_{\text{OV2}}$  is  $V_{\text{O}} - 1.24\text{V}$  whereas in the floating configuration it is  $V_{\text{O}} - 620\text{ mV}$  where  $620\text{ mV}$  approximates  $V_{\text{BE}}$  of the PNP.

The over-voltage hysteresis ( $V_{\text{HYSO}}$ ) is defined:

$$V_{\text{HYSO}} = 23\ \mu\text{A} \times R_{\text{OV2}} \quad (28)$$

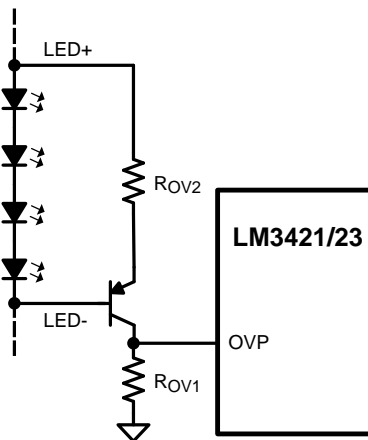


Figure 27. Floating Output OVP Circuitry

The OVLO feature can cause some interesting results if the OVLO trip-point is set too close to  $V_{\text{O}}$ . At turn-on, the converter has a modest amount of voltage overshoot before the control loop gains control of  $I_{\text{LED}}$ . If the overshoot exceeds the OVLO threshold, the controller shuts down, opening the dimming MosFET. This isolates the LED load from the converter and the output capacitance. The voltage will then discharge very slowly through the HSP and HSN pins until  $V_{\text{O}}$  drops below the lower threshold, where the process repeats. This looks like the LEDs are blinking at around 2 Hz. This mode can be escaped if the input voltage is reduced.

## INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24V threshold with programmable hysteresis as shown in Figure 28. This pin functions as both the PWM dimming input for the LEDs and as a  $V_{\text{IN}}$  UVLO. When the pin voltage rises and exceeds the 1.24V threshold,  $23\ \mu\text{A}$  (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

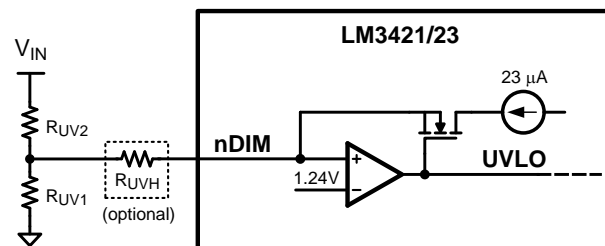


Figure 28. UVLO Circuit

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pull-down MosFET at the nDIM pin (see PWM DIMMING section). In general, at least 3V of hysteresis is preferable when PWM dimming, if operating near the UVLO threshold.

The turn-on threshold ( $V_{\text{TURN-ON}}$ ) is defined as follows:

$$V_{\text{TURN ON}} = 1.24\text{V} \times \left( \frac{R_{\text{UV1}} + R_{\text{UV2}}}{R_{\text{UV1}}} \right) \quad (29)$$

The hysteresis ( $V_{\text{HYS}}$ ) is defined as follows:

#### UVLO only

$$V_{\text{HYS}} = 23 \mu\text{A} \times R_{\text{UV2}} \quad (30)$$

#### PWM dimming and UVLO

$$V_{\text{HYS}} = 23 \mu\text{A} \times \left( R_{\text{UV2}} + \frac{R_{\text{UVH}} \times (R_{\text{UV1}} + R_{\text{UV2}})}{R_{\text{UV1}}} \right) \quad (31)$$

When "zero current" shutdown and UVLO are implemented together, the EN pin can be used to escape UVLO. The nDIM pin will pull-up to  $V_{\text{IN}}$  when EN is pulled low, therefore if  $V_{\text{IN}}$  is within the UVLO hysteretic window when EN is pulled high again, the controller will start-up even though  $V_{\text{TURN-ON}}$  is not exceeded.

#### PWM DIMMING

The active low nDIM pin can be driven with a PWM signal which controls the main NFET and the dimming FET (dimFET). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, (i.e. 30% duty cycle ~ 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a  $V_{\text{IN}}$  UVLO input as described in the [INPUT UNDER-VOLTAGE LOCKOUT \(UVLO\)](#) section or by tying it directly to  $V_{\text{CC}}$  or  $V_{\text{IN}}$ .

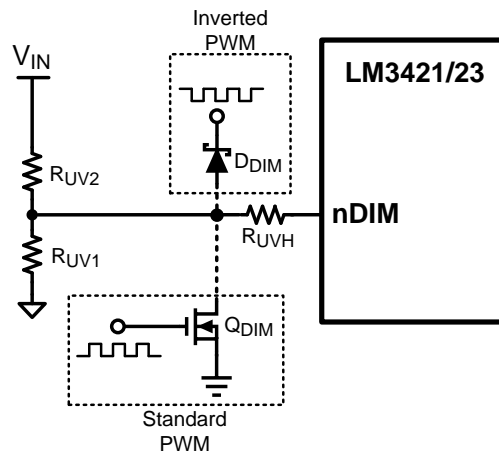


Figure 29. PWM Dimming Circuit

Figure 29 shows how the PWM signal is applied to nDIM:

1. Connect the dimming MosFET ( $Q_{\text{DIM}}$ ) with the drain to the nDIM pin and the source to AGND. Apply an external logic-level PWM signal to the gate of  $Q_{\text{DIM}}$ .
2. Connect the anode of a Schottky diode ( $D_{\text{DIM}}$ ) to the nDIM pin. Apply an inverted external logic-level PWM signal to the cathode of the same diode.

The DDRV pin is a PWM output that follows the nDIM PWM input signal. When the nDIM pin rises, the DDRV pin rises and the PWM latch reset signal is removed allowing the main MosFET Q1 to turn on at the beginning of the next clock set pulse. In boost and buck-boost topologies, the DDRV pin is used to control a N-channel MosFET placed in series with the LED load, while it would control a P-channel MosFET in parallel with the load for a buck topology.

The series dimFET will open the LED load, when nDIM is low, effectively speeding up the rise and fall times of the LED current. Without any dimFET, the rise and fall times are limited by the inductor slew rate and dimming frequencies above 1 kHz are impractical. Using the series dimFET, dimming frequencies up to 30 kHz are achievable. With a parallel dimFET (buck topology), even higher dimming frequencies are achievable.

When using the PWM functionality in a boost regulator, the PWM signal can drive a ground referenced FET. However, with buck-boost and buck topologies, level shifting circuitry is necessary to translate the PWM dim signal to the floating dimFET as shown in [Figure 30](#) and [Figure 31](#). If high side dimming is necessary in a boost regulator using the LM3423, level shifting can be added providing the polarity inverting DPOL pin is pulled low (see *LM3423 ONLY: DPOL, FLT, TIMR, and LRDY* section) as shown in [Figure 32](#).

When using a series dimFET to PWM dim the LED current, more output capacitance is always better. A general rule of thumb is to use a minimum of 40 μF when PWM dimming. For most applications, this will provide adequate energy storage at the output when the dimFET turns off and opens the LED load. Then when the dimFET is turned back on, the capacitance helps source current into the load, improving the LED current rise time.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the minimum dimming pulse length in seconds ( $t_{PULSE}$ ) is:

$$t_{PULSE} = \frac{2 \times I_{LED} \times V_O \times L1}{V_{IN}^2} \quad (32)$$

Even maintaining a dimming pulse greater than  $t_{PULSE}$ , preserving linearity at low dimming duty cycles is difficult.

The second helpful modification is to remove the  $C_{FS}$  capacitor and  $R_{FS}$  resistor, eliminating the high frequency compensation pole. This should not affect stability, but it will speed up the response of the CSH pin, specifically at the rising edge of the LED current when PWM dimming, thus improving the achievable linearity at low dimming duty cycles.

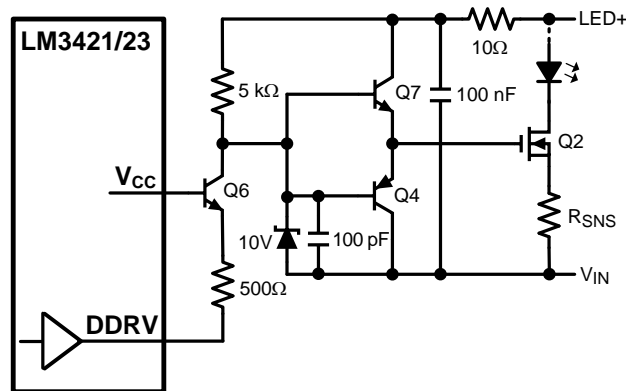


Figure 30. Buck-boost Level-Shifted PWM Circuit

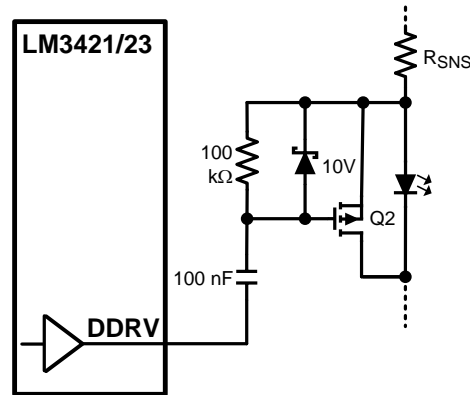


Figure 31. Buck Level-Shifted PWM Circuit

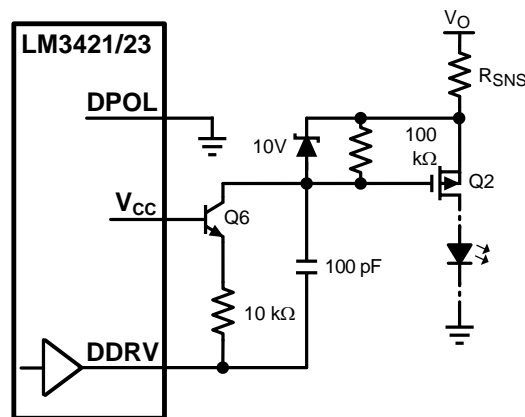


Figure 32. Boost Level-Shifted PWM Circuit

### LM3423 ONLY: DPOL, FLT, TIMR, and LRDY

The LM3423 has four additional pins: DPOL, FLT, TIMR, and LRDY. The DPOL pin is simply used to invert the DDRV polarity. If DPOL is left open, then it is internally pulled high and the polarity is correct for driving a series N-channel dimFET. If DPOL is pulled low then the polarity is correct for using a series P-channel dimFET in high-side dimming applications. For a parallel P-channel dimFET, as used in the buck topology, leave DPOL open for proper polarity.

Among the LM3423's other additional pins are TIMR and FLT which can be used in conjunction with an input disconnect MosFET switch as shown in [Figure 33](#) to protect the module from various fault conditions.

A fault is detected and an 11.5  $\mu\text{A}$  (typical) current is sourced from the TIMR pin whenever any of the following conditions exist:

1. LED current is above regulation by more than 30%.
2. OVLO has engaged.
3. Thermal shutdown has engaged.

An external capacitor ( $C_{\text{TMR}}$ ) from TIMR to AGND programs the fault filter time as follows:

$$C_{\text{TMR}} = \frac{t_{\text{FLT}} \times 11.5 \mu\text{A}}{1.24\text{V}} \quad (33)$$

When the voltage on the TIMR pin reaches 1.24V, the device is latched off and the N-channel MosFET open drain FLT pin transitions to a high impedance state. The TIMR pin will be immediately pulled to ground (reset) if the fault condition is removed at any point during the filter period. Otherwise, if the timer expires, the fault will remain latched until one of three things occurs:

1. The EN pin is pulled low long enough for the  $V_{CC}$  pin to drop below 4.1V (approximately 200 ms).
2. The TIMR pin is pulled to ground.
3. A complete power cycle occurs.

When using the EN and OVP pins in conjunction with the RPD pull-down pin, a race condition exists when exiting the disabled (EN low) state. When disabled, the OVP pin is pulled up to the output voltage because the RPD pull-down is disabled, and this will appear to be a real OVLO condition. The timer pin will immediately rise and latch the controller to the fault state. To protect against this behavior, a minimum timer capacitor ( $C_{TMR} = 220\text{pF}$ ) should be used. If fault latching is not required, short the TMR pin to AGND which will disable the FLT flag function.

The LM3423 also includes an LED Ready (LRDY) flag to notify the system that the LEDs are in proper regulation. The N-channel MosFET open drain LRDY pin is pulled low whenever any of the following conditions are met:

1.  $V_{CC}$  UVLO has engaged.
2. LED current is below regulation by more than 20%.
3. LED current is above regulation by more than 30%.
4. Over-voltage protection has engaged
5. Thermal shutdown has engaged.
6. A fault has latched the device off.

Note that the LRDY pin is pulled low during startup of the device and remains low until the LED current is in regulation.

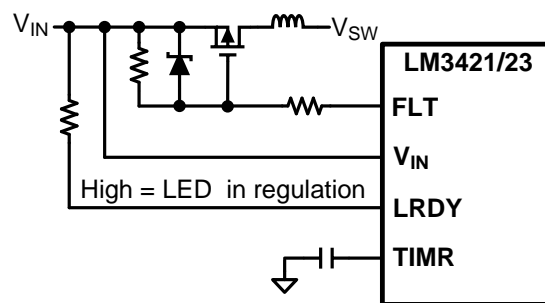


Figure 33. Fault Detection and LED Status Circuit

## Design Considerations

This section describes the application level considerations when designing with the LM3421/23. For corresponding calculations, refer to the [Design Guide](#) section.

### INDUCTOR

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transferred to the load in different ways (as an example, buck-boost operation is detailed in the [CURRENT REGULATORS](#) section). The size of the inductor, the voltage across it, and the length of the switching subinterval ( $t_{ON}$  or  $t_{OFF}$ ) determines the inductor current ripple ( $\Delta i_{L-PP}$ ). In the design process, L1 is chosen to provide a desired  $\Delta i_{L-PP}$ . For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore  $\Delta i_{L-PP}$  is basically equal to the LED ripple current  $\Delta i_{LED-PP}$ . However, for boost and buck-boost regulators, there is always an output capacitor which reduces  $\Delta i_{LED-PP}$ , therefore the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.



In general,  $\Delta i_{LED-PP}$  is recommended by manufacturers to be less than 40% of the average LED current ( $I_{LED}$ ). Therefore, for the buck regulator with no output capacitance,  $\Delta i_{L-PP}$  should also be less than 40% of  $I_{LED}$ . For the boost and buck-boost topologies,  $\Delta i_{L-PP}$  can be much higher depending on the output capacitance value. However,  $\Delta i_{L-PP}$  is suggested to be less than 100% of the average inductor current ( $I_L$ ) to limit the RMS inductor current.

L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ( $I_{L-RMS}$ ).

## LED DYNAMIC RESISTANCE

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus  $R_{SNS}$ . LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED ( $V_{LED}$ ) by the forward current ( $I_{LED}$ ) leads to an incorrect calculation of the dynamic resistance of a single LED ( $r_{LED}$ ). The result can be 5 to 10 times higher than the true  $r_{LED}$  value.

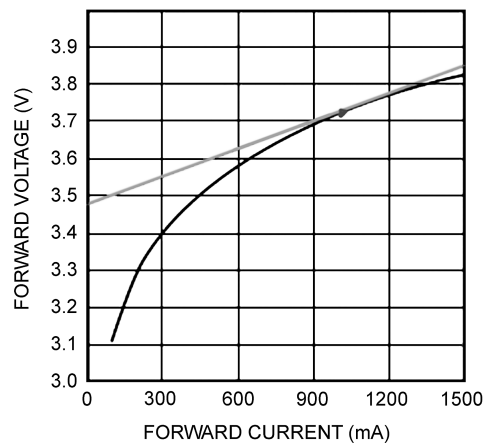


Figure 34. Dynamic Resistance

Obtaining  $r_{LED}$  is accomplished by referring to the manufacturer's LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 34. For any application with more than 2 series LEDs,  $R_{SNS}$  can be neglected allowing  $r_D$  to be approximated as the number of LEDs multiplied by  $r_{LED}$ .

## OUTPUT CAPACITOR

For boost and buck-boost regulators, the output capacitor ( $C_O$ ) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple ( $\Delta i_{LED-PP}$ ) below the inductor current ripple ( $\Delta i_{L-PP}$ ). In all cases,  $C_O$  is sized to provide a desired  $\Delta i_{LED-PP}$ . As mentioned in the **INDUCTOR** section,  $\Delta i_{LED-PP}$  is recommended by manufacturers to be less than 40% of the average LED current ( $I_{LED-PP}$ ).

$C_O$  should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

## INPUT CAPACITORS

The input capacitance ( $C_{IN}$ ) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators,  $C_{IN}$  provides energy during  $t_{ON}$  and during  $t_{OFF}$ , the input voltage source charges up  $C_{IN}$  with the average input current ( $I_{IN}$ ). For boost regulators,  $C_{IN}$  only needs to provide the ripple current due to the direct connection to the inductor.  $C_{IN}$  is selected given the maximum input voltage ripple ( $\Delta V_{IN-PP}$ ) which can be tolerated.  $\Delta V_{IN-PP}$  is suggested to be less than 10% of the input voltage ( $V_{IN}$ ).

An input capacitance at least 100% greater than the calculated  $C_{IN}$  value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

For most applications, it is recommended to bypass the  $V_{IN}$  pin with an 0.1  $\mu\text{F}$  ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the LM3421/23 device, a 10  $\Omega$  series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150 kHz filter to eliminate undesired high frequency noise.

## MAIN MosFET / DIMMING MosFET

The LM3421/23 requires an external NFET (Q1) as the main power MosFET for the switching regulator. Q1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the NFET on-resistance ( $R_{DS-ON}$ ).

When PWM dimming, the LM3421/23 requires another MosFET (Q2) placed in series (or parallel for a buck regulator) with the LED load. This MosFET should have a voltage rating equal to the output voltage ( $V_O$ ) and a current rating at least 10% higher than the nominal LED current ( $I_{LED}$ ). The power rating is simply  $V_O$  multiplied by  $I_{LED}$ , assuming 100% dimming duty cycle (continuous operation) will occur.

In general, the NFETs should be chosen to minimize total gate charge ( $Q_g$ ) when  $f_{SW}$  is high and minimize  $R_{DS-ON}$  otherwise. This will minimize the dominant power losses in the system. Frequently, higher current NFETs in larger packages are chosen for better thermal performance.

## RE-CIRCULATING DIODE

A re-circulating diode (D1) is required to carry the inductor current during  $t_{OFF}$ . The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product datasheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

## BOOST INRUSH CURRENT

When configured as a boost converter, there is a “phantom” power path comprised of the inductor, the output diode, and the output capacitor. This path will cause two things to happen when power is applied. First, there will be a very large inrush of current to charge the output capacitor. Second, the energy stored in the inductor during this inrush will end up in the output capacitor, charging it to a higher potential than the input voltage.

Depending on the state of the EN pin, the output capacitor would be discharged by:

1.  $EN < 1.3V$ : no discharge path (leakage only).
2.  $EN > 1.3V$ , the OVP divider resistor path, if present, and 10 $\mu\text{A}$  into each of the HSP & HSN pins.

In applications using the OVP divider and with  $EN > 1.3V$ , the output capacitor voltage can charge higher than  $V_{TURN-OFF}$ . In this situation, the FLT pin (LM3423 only) is open and the PWM dimming MosFET is turned off. This condition (the system appearing disabled) can persist for an undesirably long time. Possible solutions to this condition are:

- Add an inrush diode from  $V_{IN}$  to the output as shown in [Figure 35](#).
- Add an NTC thermistor in series with the input to prevent the inrush from overcharging the output capacitor too high.
- Use a current limited source supply.
- Raise the OVP threshold.

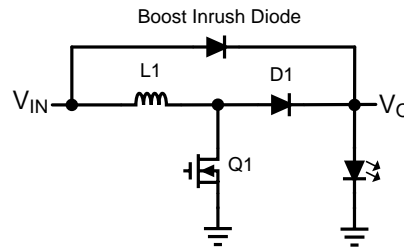


Figure 35. Boost Topology with Inrush Diode

## CIRCUIT LAYOUT

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximize noise rejection and minimize the generation of EMI within the circuit.

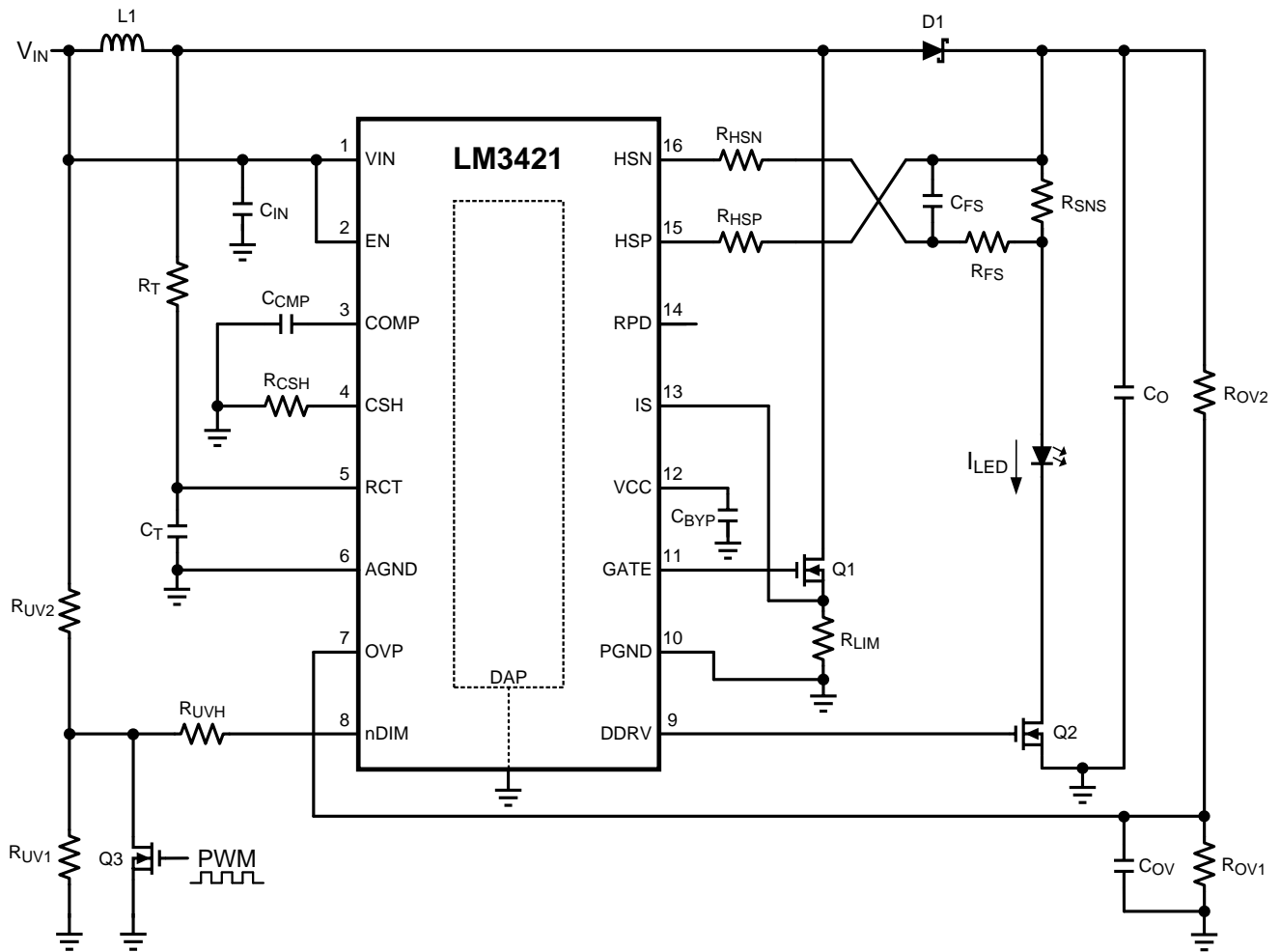
Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM3421/23 buck regulator contains the input capacitor ( $C_{IN}$ ), the recirculating diode (D1), the N-channel MosFET (Q1), and the sense resistor ( $R_{LIM}$ ). In the LM3421/23 boost regulator, the discontinuous current flows through the output capacitor ( $C_O$ ), D1, Q1, and  $R_{LIM}$ . In the buck-boost regulator both loops are discontinuous and should be carefully laid out. These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RT, COMP, CSH, IS, HSP and HSN pins are all high-impedance inputs which couple external noise easily, therefore the loops containing these nodes should be minimized whenever possible.

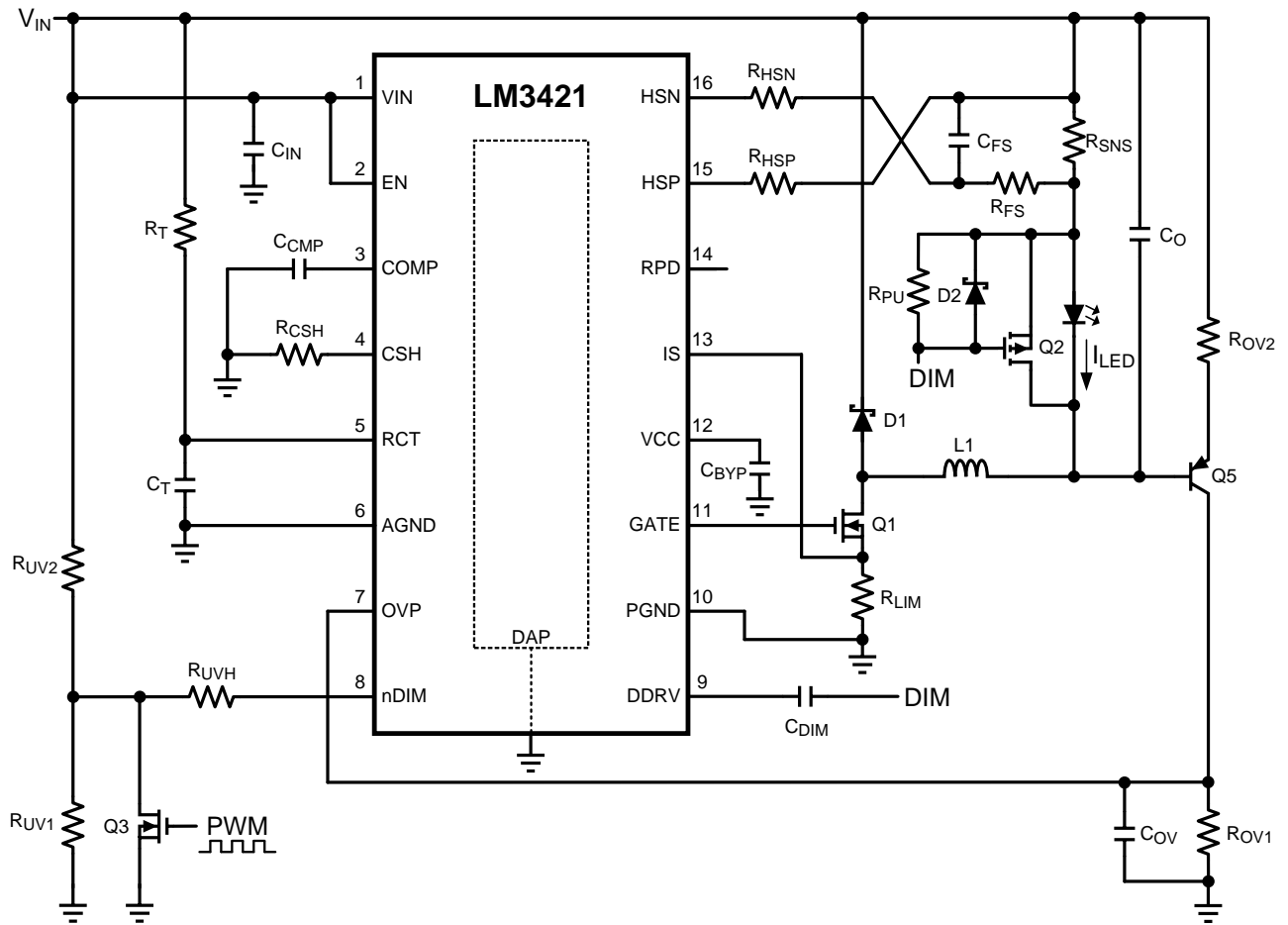
In some applications the LED or LED array can be far away (several inches or more) from the LM3421/23, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

## Basic Topology Schematics

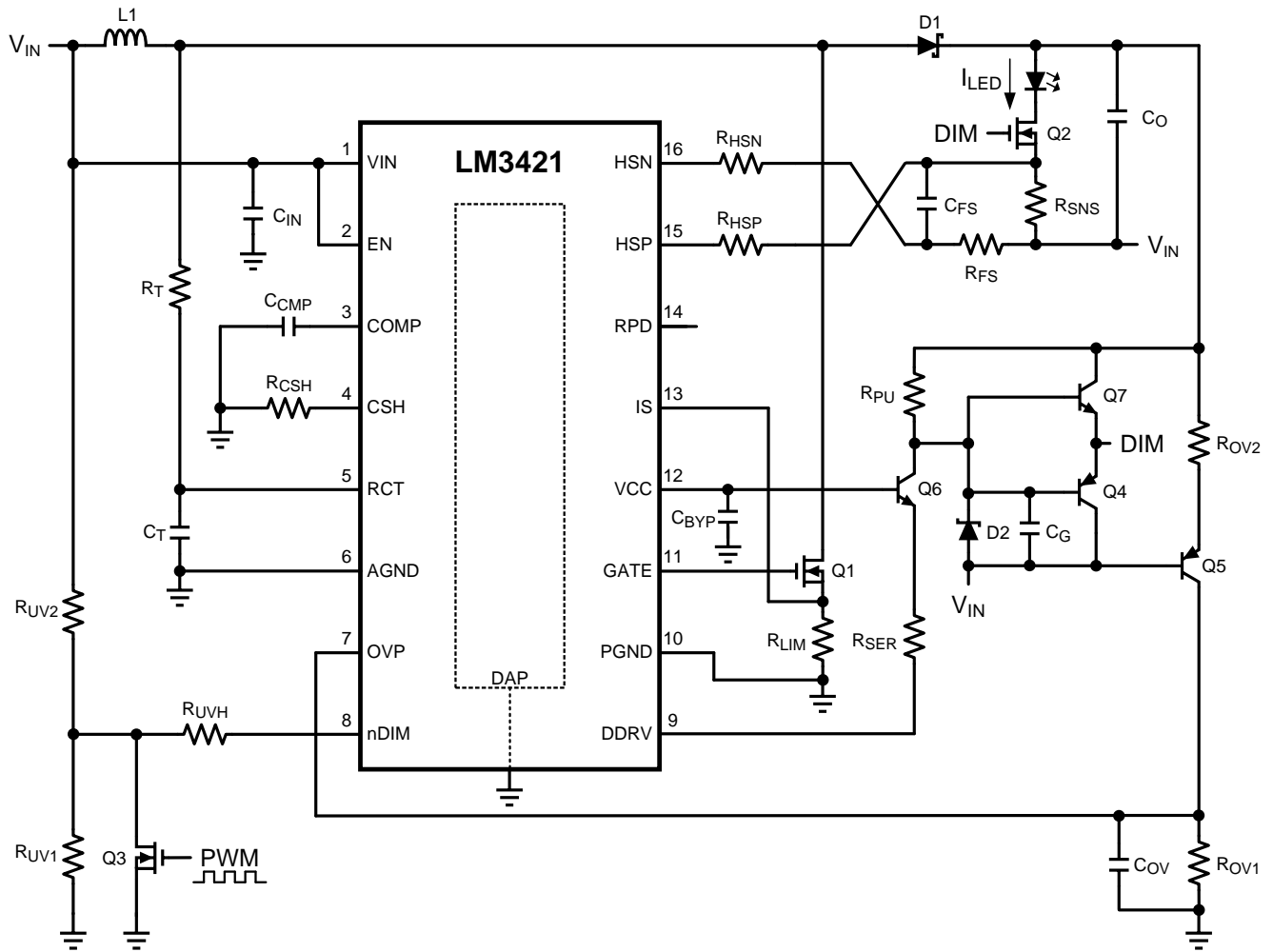
### BOOST REGULATOR ( $V_{IN} < V_O$ )



BUCK REGULATOR ( $V_{IN} > V_O$ )



**BUCK-BOOST REGULATOR**



## Design Guide

Refer to the [Basic Topology Schematics](#) section.

### SPECIFICATIONS

Number of series LEDs: N

Single LED forward voltage:  $V_{LED}$

Single LED dynamic resistance:  $r_{LED}$

Nominal input voltage:  $V_{IN}$

Input voltage range:  $V_{IN-MAX}$ ,  $V_{IN-MIN}$

Switching frequency:  $f_{SW}$

Current sense voltage:  $V_{SNS}$

Average LED current:  $I_{LED}$

Inductor current ripple:  $\Delta i_{L-PP}$

LED current ripple:  $\Delta i_{LED-PP}$

Peak current limit:  $I_{LIM}$

Input voltage ripple:  $\Delta v_{IN-PP}$

Output OVLO characteristics:  $V_{TURN-OFF}$ ,  $V_{HYSO}$

Input UVLO characteristics:  $V_{TURN-ON}$ ,  $V_{HYS}$

### 1. OPERATING POINT

Given the number of series LEDs (N), the forward voltage ( $V_{LED}$ ) and dynamic resistance ( $r_{LED}$ ) for a single LED, solve for the nominal output voltage ( $V_O$ ) and the nominal LED string dynamic resistance ( $r_D$ ):

$$V_O = N \times V_{LED} \quad (34)$$

$$r_D = N \times r_{LED} \quad (35)$$

Solve for the ideal nominal duty cycle (D):

#### Buck

$$D = \frac{V_O}{V_{IN}} \quad (36)$$

#### Boost

$$D = \frac{V_O - V_{IN}}{V_O} \quad (37)$$

#### Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \quad (38)$$

Using the same equations, find the minimum duty cycle ( $D_{MIN}$ ) using maximum input voltage ( $V_{IN-MAX}$ ) and the maximum duty cycle ( $D_{MAX}$ ) using the minimum input voltage ( $V_{IN-MIN}$ ). Also, remember that  $D' = 1 - D$ .

### 2. SWITCHING FREQUENCY

Set the switching frequency ( $f_{SW}$ ) by assuming a  $C_T$  value of 1 nF and solving for  $R_T$ :

### Buck (Constant Ripple vs. $V_{IN}$ )

$$R_T = \frac{25 \times (V_{IN} - V_O)}{f_{SW} \times C_T \times V_{IN}} \quad (39)$$

$$R_T = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{f_{SW} \times C_T \times V_{IN}^2} \quad (40)$$

### Boost and Buck-boost

$$R_T = \frac{25}{f_{SW} \times C_T} \quad (41)$$

## 3. AVERAGE LED CURRENT

For all topologies, set the average LED current ( $I_{LED}$ ) knowing the desired current sense voltage ( $V_{SNS}$ ) and solving for  $R_{SNS}$ :

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} \quad (42)$$

If the calculated  $R_{SNS}$  is too far from a desired standard value, then  $V_{SNS}$  will have to be adjusted to obtain a standard value.

Setup the suggested signal current of 100  $\mu$ A by assuming  $R_{CSH} = 12.4 \text{ k}\Omega$  and solving for  $R_{HSP}$ :

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} \quad (43)$$

If the calculated  $R_{HSP}$  is too far from a desired standard value, then  $R_{CSH}$  can be adjusted to obtain a standard value.

## 4. INDUCTOR RIPPLE CURRENT

Set the nominal inductor ripple current ( $\Delta i_{L-PP}$ ) by solving for the appropriate inductor ( $L1$ ):

### Buck

$$L1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L-PP} \times f_{SW}} \quad (44)$$

### Boost and Buck-boost

$$L1 = \frac{\tilde{V}_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} \quad (45)$$

To set the worst case inductor ripple current, use  $V_{IN-MAX}$  and  $D_{MIN}$  when solving for  $L1$ .

The minimum allowable inductor RMS current rating ( $I_{L-RMS}$ ) can be calculated as:

### Buck

$$I_{L-RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP}}{I_{LED}}\right)^2} \quad (46)$$



### Boost and Buck-boost

$$I_{L-RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left( \frac{\Delta I_{L-PP} \times D'}{I_{LED}} \right)^2} \quad (47)$$

## 5. LED RIPPLE CURRENT

Set the nominal LED ripple current ( $\Delta i_{LED-PP}$ ), by solving for the output capacitance ( $C_O$ ):

### Buck

$$C_O = \frac{\Delta i_{L-PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED-PP}} \quad (48)$$

### Boost and Buck-boost

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED-PP} \times f_{SW}} \quad (49)$$

To set the worst case LED ripple current, use  $D_{MAX}$  when solving for  $C_O$ . Remember, when PWM dimming it is recommended to use a minimum of 40  $\mu F$  of output capacitance to improve performance.

The minimum allowable RMS output capacitor current rating ( $I_{CO-RMS}$ ) can be approximated:

### Buck

$$I_{CO-RMS} = \frac{\Delta i_{LED-PP}}{\sqrt{12}} \quad (50)$$

### Boost and Buck-boost

$$I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (51)$$

## 6. PEAK CURRENT LIMIT

Set the peak current limit ( $I_{LIM}$ ) by solving for the transistor path sense resistor ( $R_{LIM}$ ):

$$R_{LIM} = \frac{245 \text{ mV}}{I_{LIM}} \quad (52)$$

## 7. LOOP COMPENSATION

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain ( $T_U$ ) of the regulator can be approximated:

### Buck

$$T_U = T_{U0} \times \frac{1}{\left( 1 + \frac{s}{\omega_{P1}} \right)} \quad (53)$$

### Boost and Buck-boost

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad (54)$$

Where the pole ( $\omega_{P1}$ ) is approximated:

#### Buck

$$\omega_{P1} = \frac{1}{r_D \times C_O} \quad (55)$$

#### Boost

$$\omega_{P1} = \frac{2}{r_D \times C_O} \quad (56)$$

#### Buck-boost

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \quad (57)$$

And the RHP zero ( $\omega_{Z1}$ ) is approximated:

#### Boost

$$\omega_{Z1} = \frac{r_D \times D^2}{L1} \quad (58)$$

#### Buck-boost

$$\omega_{Z1} = \frac{r_D \times D^2}{D \times L1} \quad (59)$$

And the uncompensated DC loop gain ( $T_{U0}$ ) is approximated:

#### Buck

$$T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \quad (60)$$

#### Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \quad (61)$$

#### Buck-boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \quad (62)$$

For all topologies, the primary method of compensation is to place a low frequency dominant pole ( $\omega_{P2}$ ) which will ensure that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor ( $C_{CMP}$ ) from the COMP pin to AGND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} \quad (63)$$

$$C_{\text{CMP}} = \frac{1}{\omega_{\text{P2}} \times 5e^6} \quad (64)$$

If analog dimming is used,  $C_{\text{CMP}}$  should be approximately 4x larger to maintain stability as the LEDs are dimmed to zero.

A high frequency compensation pole ( $\omega_{\text{P3}}$ ) can be used to attenuate switching noise and provide better gain margin. Assuming  $R_{\text{FS}} = 10\Omega$ ,  $C_{\text{FS}}$  is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

$$\omega_{\text{P3}} = \max(\omega_{\text{P1}}, \omega_{\text{Z1}}) \times 10 \quad (65)$$

$$C_{\text{FS}} = \frac{1}{10 \times \omega_{\text{P3}}} \quad (66)$$

The total system loop gain (T) can then be written as:

#### **Buck**

$$T = T_{\text{U0}} \times \frac{1}{\left(1 + \frac{s}{\omega_{\text{P1}}}\right) \times \left(1 + \frac{s}{\omega_{\text{P2}}}\right) \times \left(1 + \frac{s}{\omega_{\text{P3}}}\right)} \quad (67)$$

#### **Boost and Buck-boost**

$$T = T_{\text{U0}} \times \frac{\left(1 - \frac{s}{\omega_{\text{Z1}}}\right)}{\left(1 + \frac{s}{\omega_{\text{P1}}}\right) \times \left(1 + \frac{s}{\omega_{\text{P2}}}\right) \times \left(1 + \frac{s}{\omega_{\text{P3}}}\right)} \quad (68)$$

## **8. INPUT CAPACITANCE**

Set the nominal input voltage ripple ( $\Delta V_{\text{IN-PP}}$ ) by solving for the required capacitance ( $C_{\text{IN}}$ ):

#### **Buck**

$$C_{\text{IN}} = \frac{I_{\text{LED}} \times (1 - D) \times D}{\Delta V_{\text{IN-PP}} \times f_{\text{SW}}} \quad (69)$$

#### **Boost**

$$C_{\text{IN}} = \frac{\Delta i_{\text{L-PP}}}{8 \times \Delta V_{\text{IN-PP}} \times f_{\text{SW}}} \quad (70)$$

#### **Buck-boost**

$$C_{\text{IN}} = \frac{I_{\text{LED}} \times D}{\Delta V_{\text{IN-PP}} \times f_{\text{SW}}} \quad (71)$$

Use  $D_{\text{MAX}}$  to set the worst case input voltage ripple, when solving for  $C_{\text{IN}}$  in a buck-boost regulator and  $D_{\text{MID}} = 0.5$  when solving for  $C_{\text{IN}}$  in a buck regulator.

The minimum allowable RMS input current rating ( $I_{\text{CIN-RMS}}$ ) can be approximated:

#### **Buck**

$$I_{\text{CIN-RMS}} = I_{\text{LED}} \times \sqrt{D_{\text{MID}} \times (1 - D_{\text{MID}})} \quad (72)$$

### Boost

$$I_{\text{CIN-RMS}} = \frac{\Delta i_{\text{L-PP}}}{\sqrt{12}} \quad (73)$$

### Buck-boost

$$I_{\text{CIN-RMS}} = I_{\text{LED}} \times \sqrt{\frac{D_{\text{MAX}}}{1-D_{\text{MAX}}}} \quad (74)$$

## 9. NFET

The NFET voltage rating should be at least 15% higher than the maximum NFET drain-to-source voltage ( $V_{\text{T-MAX}}$ ):

### Buck

$$V_{\text{T-MAX}} = V_{\text{IN-MAX}} \quad (75)$$

### Boost

$$V_{\text{T-MAX}} = V_{\text{O}} \quad (76)$$

### Buck-boost

$$V_{\text{T-MAX}} = V_{\text{IN-MAX}} + V_{\text{O}} \quad (77)$$

The current rating should be at least 10% higher than the maximum average NFET current ( $I_{\text{T-MAX}}$ ):

### Buck

$$I_{\text{T-MAX}} = D_{\text{MAX}} \times I_{\text{LED}} \quad (78)$$

### Boost and Buck-boost

$$I_{\text{T-MAX}} = \frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}} \times I_{\text{LED}} \quad (79)$$

Approximate the nominal RMS transistor current ( $I_{\text{T-RMS}}$ ):

### Buck

$$I_{\text{T-RMS}} = I_{\text{LED}} \times \sqrt{D} \quad (80)$$

### Boost and Buck-boost

$$I_{\text{T-RMS}} = \frac{I_{\text{LED}}}{D'} \times \sqrt{D} \quad (81)$$

Given an NFET with on-resistance ( $R_{\text{DS-ON}}$ ), solve for the nominal power dissipation ( $P_{\text{T}}$ ):

$$P_{\text{T}} = I_{\text{T-RMS}}^2 \times R_{\text{DS-ON}} \quad (82)$$

## 10. DIODE

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage ( $V_{\text{RD-MAX}}$ ):

### Buck

$$V_{\text{RD-MAX}} = V_{\text{IN-MAX}} \quad (83)$$

**Boost**

$$V_{RD-MAX} = V_O \quad (84)$$

**Buck-boost**

$$V_{RD-MAX} = V_{IN-MAX} + V_O \quad (85)$$

The current rating should be at least 10% higher than the maximum average diode current ( $I_{D-MAX}$ ):

**Buck**

$$I_{D-MAX} = (1 - D_{MIN}) \times I_{LED} \quad (86)$$

**Boost and Buck-boost**

$$I_{D-MAX} = I_{LED} \quad (87)$$

Replace  $D_{MAX}$  with  $D$  in the  $I_{D-MAX}$  equation to solve for the average diode current ( $I_D$ ). Given a diode with forward voltage ( $V_{FD}$ ), solve for the nominal power dissipation ( $P_D$ ):

$$P_D = I_D \times V_{FD} \quad (88)$$

## 11. OUTPUT OVLO

For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage ( $V_{TURN-OFF}$ ) and the desired hysteresis ( $V_{HYSO}$ ). To set  $V_{HYSO}$ , solve for  $R_{OV2}$ :

$$R_{OV2} = \frac{V_{HYSO}}{23 \mu A} \quad (89)$$

To set  $V_{TURN-OFF}$ , solve for  $R_{OV1}$ :

**Boost**

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 1.24V} \quad (90)$$

**Buck-boost**

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 620 \text{ mV}} \quad (91)$$

A small filter capacitor ( $C_{OVP} = 47 \text{ pF}$ ) should be added from the OVP pin to ground to reduce coupled switching noise.

## 12. INPUT UVLO

For all topologies, input UVLO is programmed with the turn-on threshold voltage ( $V_{TURN-ON}$ ) and the desired hysteresis ( $V_{HYS}$ ).

**Method #1:** If no PWM dimming is required, a two resistor network can be used. To set  $V_{HYS}$ , solve for  $R_{UV2}$ :

$$R_{UV2} = \frac{V_{HYS}}{23 \mu A} \quad (92)$$

To set  $V_{TURN-ON}$ , solve for  $R_{UV1}$ :

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} \quad (93)$$

**Method #2:** If PWM dimming is required, a three resistor network is suggested. To set  $V_{\text{TURN-ON}}$ , assume  $R_{\text{UV}2} = 10 \text{ k}\Omega$  and solve for  $R_{\text{UV}1}$  as in Method #1. To set  $V_{\text{HYS}}$ , solve for  $R_{\text{UVH}}$ :

$$R_{\text{UVH}} = \frac{R_{\text{UV}1} \times (V_{\text{HYS}} - 23 \mu\text{A} \times R_{\text{UV}2})}{23 \mu\text{A} \times (R_{\text{UV}1} + R_{\text{UV}2})} \quad (94)$$

### 13. PWM DIMMING METHOD

PWM dimming can be performed several ways:

**Method #1:** Connect the dimming MosFET ( $Q_3$ ) with the drain to the nDIM pin and the source to AGND. Apply an external PWM signal to the gate of  $Q_{\text{DIM}}$ . A pull down resistor may be necessary to properly turn off  $Q_3$ .

**Method #2:** Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

The DDRV pin should be connected to the gate of the dimFET with or without level-shifting circuitry as described in the [PWM DIMMING](#) section. The dimFET should be rated to handle the average LED current and the nominal output voltage.

### 14. ANALOG DIMMING METHOD

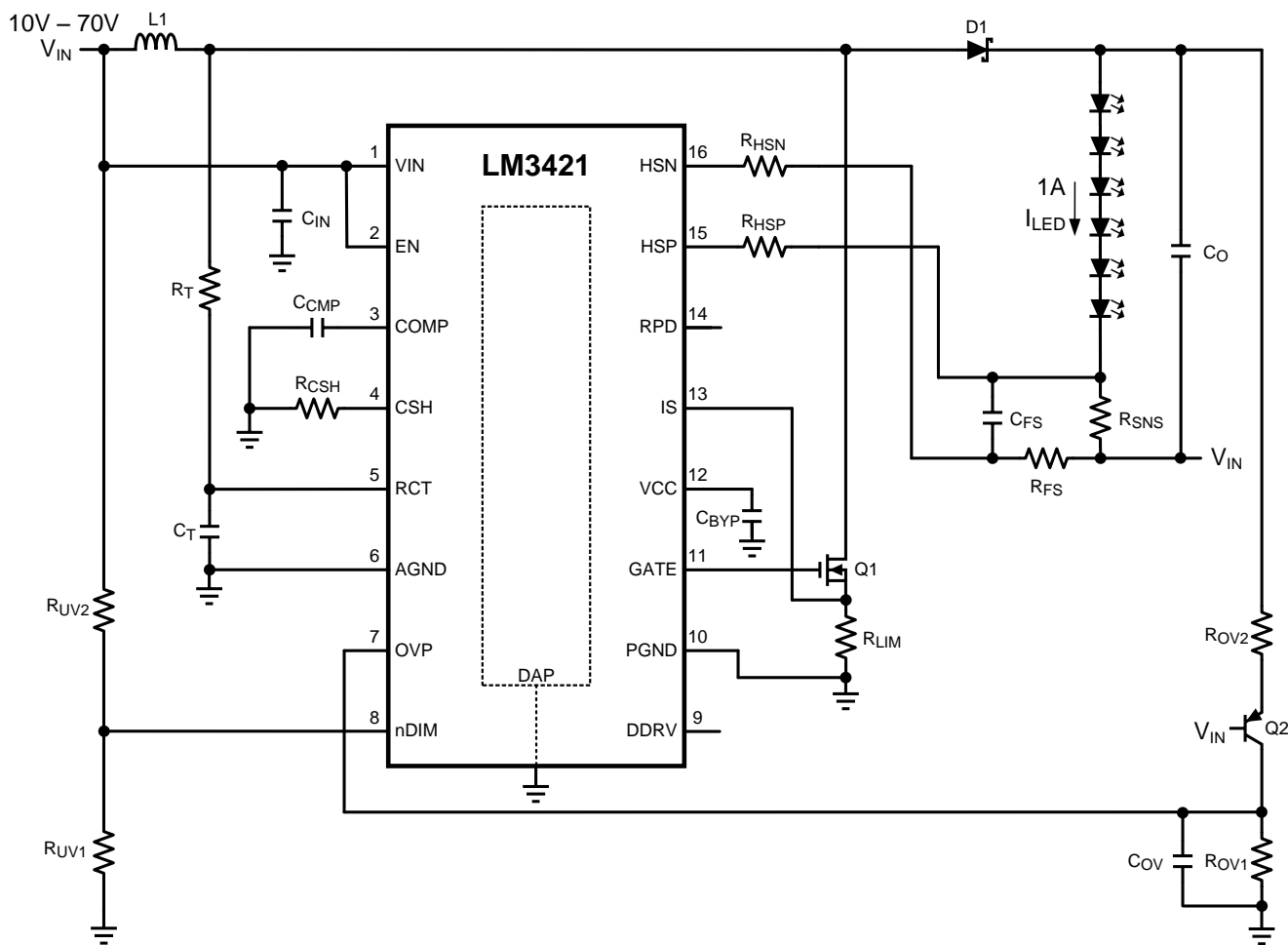
Analog dimming can be performed several ways:

**Method #1:** Place a potentiometer in series with the  $R_{\text{CSH}}$  resistor to dim the LED current from the nominal  $I_{\text{LED}}$  to near zero.

**Method #2:** Connect a controlled current source as detailed in the [ANALOG DIMMING](#) section to the CSH pin. Increasing the current sourced into the CSH node will decrease the LEDs from the nominal  $I_{\text{LED}}$  to zero current in the same manner as the thermal foldback circuit.

## Design Example

### DESIGN #1 - LM3421 BUCK-BOOST Application



### SPECIFICATIONS

$N = 6$

$V_{LED} = 3.5V$

$r_{LED} = 325\text{ m}\Omega$

$V_{IN} = 24V$

$V_{IN-MIN} = 10V$

$V_{IN-MAX} = 70V$

$f_{SW} = 500\text{ kHz}$

$V_{SNS} = 100\text{ mV}$

$I_{LED} = 1A$

$\Delta i_{L-PP} = 700\text{ mA}$

$\Delta i_{LED-PP} = 12\text{ mA}$

$\Delta V_{IN-PP} = 100\text{ mV}$

$I_{LIM} = 6A$

$$V_{\text{TURN-ON}} = 10\text{V}$$

$$V_{\text{HYS}} = 3\text{V}$$

$$V_{\text{TURN-OFF}} = 40\text{V}$$

$$V_{\text{HYSO}} = 10\text{V}$$

## 1. OPERATING POINT

Solve for  $V_O$  and  $r_D$ :

$$V_O = N \times V_{\text{LED}} = 6 \times 3.5\text{V} = 21\text{V} \quad (95)$$

$$r_D = N \times r_{\text{LED}} = 6 \times 325 \text{ m}\Omega = 1.95\Omega \quad (96)$$

Solve for  $D$ ,  $D'$ ,  $D_{\text{MAX}}$ , and  $D_{\text{MIN}}$ :

$$D = \frac{V_O}{V_O + V_{\text{IN}}} = \frac{21\text{V}}{21\text{V} + 24\text{V}} = 0.467 \quad (97)$$

$$D' = 1 - D = 1 - 0.467 = 0.533 \quad (98)$$

$$D_{\text{MIN}} = \frac{V_O}{V_O + V_{\text{IN-MAX}}} = \frac{21\text{V}}{21\text{V} + 70\text{V}} = 0.231 \quad (99)$$

$$D_{\text{MAX}} = \frac{V_O}{V_O + V_{\text{IN-MIN}}} = \frac{21\text{V}}{21\text{V} + 10\text{V}} = 0.677 \quad (100)$$



## 2. SWITCHING FREQUENCY

Assume  $C_T = 1$  nF and solve for  $R_T$ :

$$R_T = \frac{25}{f_{SW} \times C_T} = \frac{25}{500 \text{ kHz} \times 1 \text{ nF}} = 50 \text{ k}\Omega \quad (101)$$

The closest standard resistor is 49.9 k $\Omega$  therefore  $f_{SW}$  is:

$$f_{SW} = \frac{25}{R_T \times C_T} = \frac{25}{49.9 \text{ k}\Omega \times 1 \text{ nF}} = 501 \text{ kHz} \quad (102)$$

The chosen component from step 2 is:

$$\begin{aligned} C_T &= 1 \text{ nF} \\ R_T &= 49.9 \text{ k}\Omega \end{aligned} \quad (103)$$

## 3. AVERAGE LED CURRENT

Solve for  $R_{SNS}$ :

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} = \frac{100 \text{ mV}}{1 \text{ A}} = 0.1 \Omega \quad (104)$$

Assume  $R_{CSH} = 12.4$  k $\Omega$  and solve for  $R_{HSP}$ :

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24 \text{ V}} = \frac{1 \text{ A} \times 12.4 \text{ k}\Omega \times 0.1 \Omega}{1.24 \text{ V}} = 1.0 \text{ k}\Omega \quad (105)$$

The closest standard resistor for  $R_{SNS}$  is actually 0.1 $\Omega$  and for  $R_{HSP}$  is actually 1 k $\Omega$  therefore  $I_{LED}$  is:

$$I_{LED} = \frac{1.24 \text{ V} \times R_{HSP}}{R_{SNS} \times R_{CSH}} = \frac{1.24 \text{ V} \times 1.0 \text{ k}\Omega}{0.1 \Omega \times 12.4 \text{ k}\Omega} = 1.0 \text{ A} \quad (106)$$

The chosen components from step 3 are:

$$\begin{aligned} R_{SNS} &= 0.1 \Omega \\ R_{CSH} &= 12.4 \text{ k}\Omega \\ R_{HSP} &= R_{HSN} = 1 \text{ k}\Omega \end{aligned} \quad (107)$$

## 4. INDUCTOR RIPPLE CURRENT

Solve for  $L1$ :

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} = \frac{24 \text{ V} \times 0.467}{700 \text{ mA} \times 501 \text{ kHz}} = 32 \mu\text{H} \quad (108)$$

The closest standard inductor is 33  $\mu\text{H}$  therefore  $\Delta i_{L-PP}$  is:

$$\Delta i_{L-PP} = \frac{V_{IN} \times D}{L1 \times f_{SW}} = \frac{24 \text{ V} \times 0.467}{33 \mu\text{H} \times 501 \text{ kHz}} = 678 \text{ mA} \quad (109)$$

Determine minimum allowable RMS current rating:

$$\begin{aligned} I_{L-RMS} &= \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left( \frac{\Delta i_{L-PP} \times D'}{I_{LED}} \right)^2} \\ I_{L-RMS} &= \frac{1 \text{ A}}{0.533} \times \sqrt{1 + \frac{1}{12} \times \left( \frac{678 \text{ mA} \times 0.533}{1 \text{ A}} \right)^2} = 1.89 \text{ A} \end{aligned} \quad (110)$$

The chosen component from step 4 is:

$$\boxed{L1 = 33 \mu\text{H}}$$
 (111)

## 5. OUTPUT CAPACITANCE

Solve for  $C_O$ :

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED-PP} \times f_{SW}}$$

$$C_O = \frac{1\text{A} \times 0.467}{1.95\Omega \times 12 \text{ mA} \times 501 \text{ kHz}} = 39.8 \mu\text{F}$$
 (112)

The closest capacitance totals 40  $\mu\text{F}$  therefore  $\Delta i_{LED-PP}$  is:

$$\Delta i_{LED-PP} = \frac{I_{LED} \times D}{r_D \times C_O \times f_{SW}}$$

$$\Delta i_{LED-PP} = \frac{1\text{A} \times 0.467}{1.95\Omega \times 40 \mu\text{F} \times 501 \text{ kHz}} = 12 \text{ mA}$$
 (113)

Determine minimum allowable RMS current rating:

$$I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1\text{A} \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45\text{A}$$
 (114)

The chosen components from step 5 are:

$$\boxed{C_O = 4 \times 10 \mu\text{F}}$$
 (115)

## 6. PEAK CURRENT LIMIT

Solve for  $R_{LIM}$ :

$$R_{LIM} = \frac{245 \text{ mV}}{I_{LIM}} = \frac{245 \text{ mV}}{6\text{A}} = 0.041\Omega$$
 (116)

The closest standard resistor is 0.04  $\Omega$  therefore  $I_{LIM}$  is:

$$I_{LIM} = \frac{245 \text{ mV}}{R_{LIM}} = \frac{245 \text{ mV}}{0.04\Omega} = 6.13\text{A}$$
 (117)

The chosen component from step 6 is:

$$\boxed{R_{LIM} = 0.04\Omega}$$
 (118)

## 7. LOOP COMPENSATION

$\omega_{P1}$  is approximated:

$$\omega_{P1} = \frac{1 + D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 40 \mu\text{F}} = 19\text{k} \frac{\text{rad}}{\text{sec}}$$
 (119)

$\omega_{Z1}$  is approximated:

$$\omega_{Z1} = \frac{r_D \times D^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33 \mu\text{H}} = 36\text{k} \frac{\text{rad}}{\text{sec}}$$
 (120)

$T_{U0}$  is approximated:

$$T_{U0} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \quad (121)$$

To ensure stability, calculate  $\omega_{P2}$ :

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{P1}}{5 \times 5630} = \frac{19k \frac{\text{rad}}{\text{sec}}}{5 \times 5630} = 0.675 \frac{\text{rad}}{\text{sec}} \quad (122)$$

Solve for  $C_{CMP}$ :

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5e^6 \Omega} = \frac{1}{0.675 \frac{\text{rad}}{\text{sec}} \times 5e^6 \Omega} = 0.30 \mu\text{F} \quad (123)$$

To attenuate switching noise, calculate  $\omega_{P3}$ :

$$\begin{aligned} \omega_{P3} &= (\max \omega_{P1}, \omega_{Z1}) \times 10 = \omega_{Z1} \times 10 \\ \omega_{P3} &= 36k \frac{\text{rad}}{\text{sec}} \times 10 = 360k \frac{\text{rad}}{\text{sec}} \end{aligned} \quad (124)$$

Assume  $R_{FS} = 10\Omega$  and solve for  $C_{FS}$ :

$$C_{FS} = \frac{1}{10\Omega \times \omega_{P3}} = \frac{1}{10\Omega \times 360k \frac{\text{rad}}{\text{sec}}} = 0.28 \mu\text{F} \quad (125)$$

The chosen components from step 7 are:

$C_{CMP} = 0.33 \mu\text{F}$
$R_{FS} = 10\Omega$
$C_{FS} = 0.27 \mu\text{F}$

(126)

## 8. INPUT CAPACITANCE

Solve for the minimum  $C_{IN}$ :

$$C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} = \frac{1A \times 0.467}{100 \text{ mV} \times 504 \text{ kHz}} = 9.27 \mu\text{F} \quad (127)$$

To minimize power supply interaction a 200% larger capacitance of approximately 20  $\mu\text{F}$  is used, therefore the actual  $\Delta V_{IN-PP}$  is much lower. Since high voltage ceramic capacitor selection is limited, four 4.7  $\mu\text{F}$  X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

$$I_{IN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \quad (128)$$

The chosen components from step 8 are:

$C_{IN} = 4 \times 4.7 \mu\text{F}$
-------------------------------------

(129)

## 9. NFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \quad (130)$$

$$I_{T-MAX} = \frac{0.677}{1-0.677} \times 1A = 2.1A \quad (131)$$

A 100V NFET is chosen with a current rating of 32A due to the low  $R_{DS-ON} = 50 \text{ m}\Omega$ . Determine  $I_{T-RMS}$  and  $P_T$ :

$$I_{T-RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \quad (132)$$

$$P_T = I_{T-RMS}^2 \times R_{DS-ON} = 1.28A^2 \times 50 \text{ m}\Omega = 82 \text{ mW} \quad (133)$$

The chosen component from step 9 is:

$$\boxed{Q1 \rightarrow 32A, 100V, DPAK} \quad (134)$$

## 10. DIODE

Determine minimum D1 voltage rating and current rating:

$$V_{RD-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \quad (135)$$

$$I_{D-MAX} = I_{LED} = 1A \quad (136)$$

A 100V diode is chosen with a current rating of 12A and  $V_D = 600 \text{ mV}$ . Determine  $P_D$ :

$$P_D = I_D \times V_{FD} = 1A \times 600 \text{ mV} = 600 \text{ mW} \quad (137)$$

The chosen component from step 10 is:

$$\boxed{D1 \rightarrow 12A, 100V, DPAK} \quad (138)$$

## 11. INPUT UVLO

Solve for  $R_{UV2}$ :

$$R_{UV2} = \frac{V_{HYS}}{23 \mu A} = \frac{3V}{23 \mu A} = 130 \text{ k}\Omega \quad (139)$$

The closest standard resistor is 130 k $\Omega$  therefore  $V_{HYS}$  is:

$$V_{HYS} = R_{UV2} \times 23 \mu A = 130 \text{ k}\Omega \times 23 \mu A = 2.99V \quad (140)$$

Solve for  $R_{UV1}$ :

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} = \frac{1.24V \times 130 \text{ k}\Omega}{10V - 1.24V} = 18.4 \text{ k}\Omega \quad (141)$$

The closest standard resistor is 18.2 k $\Omega$  making  $V_{TURN-ON}$ :

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}} \quad (142)$$

$$V_{TURN-ON} = \frac{1.24V \times (18.2 \text{ k}\Omega + 130 \text{ k}\Omega)}{18.2 \text{ k}\Omega} = 10.1V$$

The chosen components from step 11 are:

$$\boxed{\begin{matrix} R_{UV1} = 18.2 \text{ k}\Omega \\ R_{UV2} = 130 \text{ k}\Omega \end{matrix}} \quad (143)$$

## 12. OUTPUT OVLO

Solve for  $R_{OV2}$ :

$$R_{OV2} = \frac{V_{HYSO}}{23 \mu A} = \frac{10V}{23 \mu A} = 435 \text{ k}\Omega \quad (144)$$

The closest standard resistor is 432 k $\Omega$  therefore  $V_{HYSO}$  is:

$$V_{HYSO} = R_{OV2} \times 23 \mu A = 432 \text{ k}\Omega \times 23 \mu A = 9.94V \quad (145)$$

Solve for  $R_{OV1}$ :

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 0.62V} = \frac{1.24V \times 432 \text{ k}\Omega}{40V - 0.62V} = 13.6 \text{ k}\Omega \quad (146)$$

The closest standard resistor is 13.7 k $\Omega$  making  $V_{TURN-OFF}$ :

$$V_{TURN-OFF} = \frac{1.24V \times (0.5 \times R_{OV1} + R_{OV2})}{R_{OV1}}$$

$$V_{TURN-OFF} = \frac{1.24V \times (0.5 \times 13.7 \text{ k}\Omega + 432 \text{ k}\Omega)}{13.7 \text{ k}\Omega} = 39.7V \quad (147)$$

The chosen components from step 12 are:

$R_{OV1} = 13.7 \text{ k}\Omega$
$R_{OV2} = 432 \text{ k}\Omega$

(148)

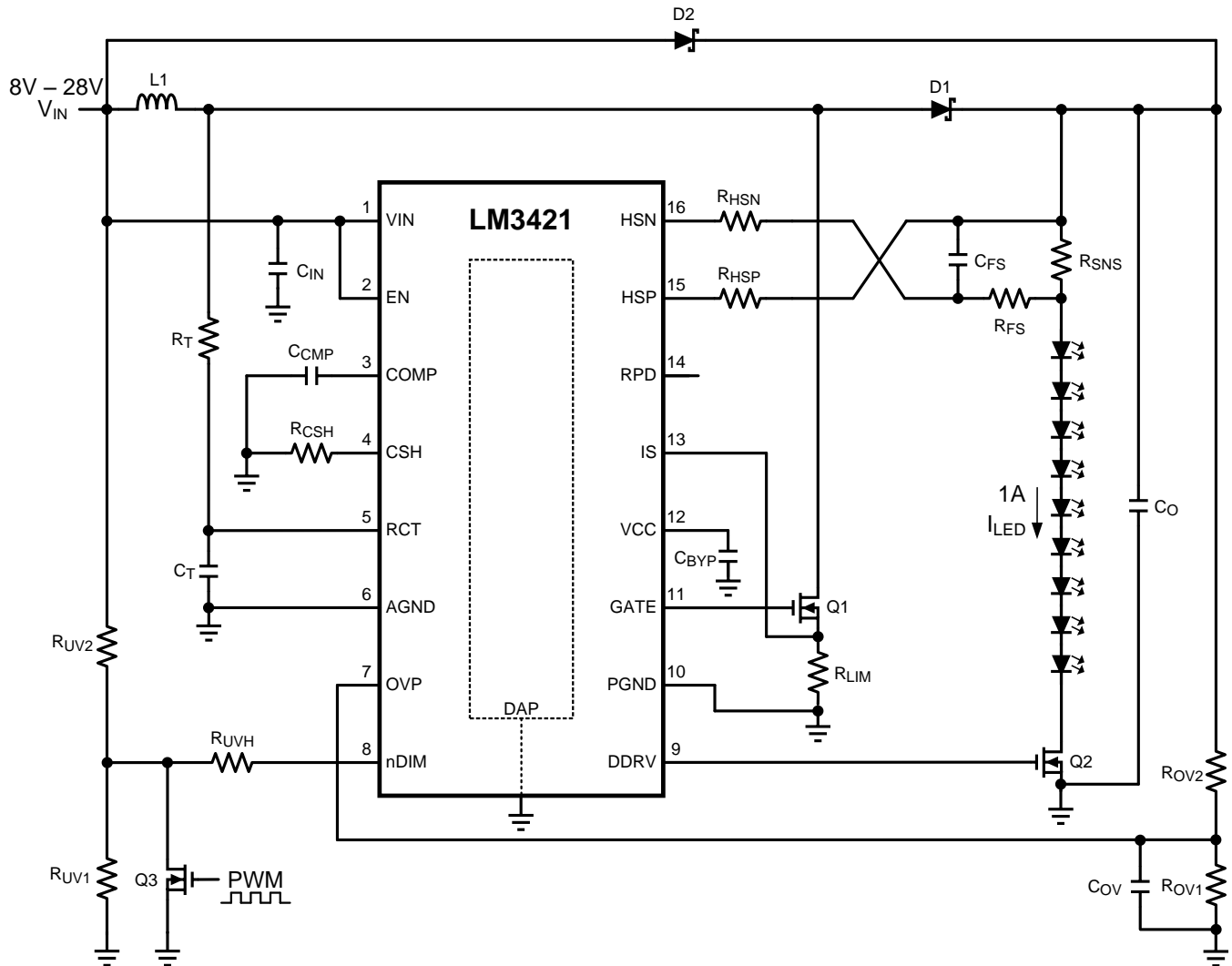
## DESIGN #1 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3421	Buck-boost controller	TI	LM3421MH
1	C <sub>BYP</sub>	2.2 $\mu$ F X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C <sub>COMP</sub>	0.33 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E334KA01L
1	C <sub>FS</sub>	0.27 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E274KA01L
4	C <sub>IN</sub>	4.7 $\mu$ F X7R 10% 100V	TDK	C5750X7R2A475K
4	C <sub>O</sub>	10 $\mu$ F X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	L1	33 $\mu$ H 20% 6.3A	COILCRAFT	MSS1278-333MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R <sub>CSH</sub>	12.4 k $\Omega$ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	10 $\Omega$ 1%	VISHAY	CRCW080510R0FKEA
2	R <sub>HSP</sub> , R <sub>HSN</sub>	1.0 k $\Omega$ 1%	VISHAY	CRCW08051K00FKEA
1	R <sub>LIM</sub>	0.04 $\Omega$ 1% 1W	VISHAY	WSL2512R0400FEA
1	R <sub>OV1</sub>	13.7 k $\Omega$ 1%	VISHAY	CRCW080513K7FKEA
1	R <sub>OV2</sub>	432 k $\Omega$ 1%	VISHAY	CRCW0805432KFKEA
1	R <sub>SNS</sub>	0.1 $\Omega$ 1% 1W	VISHAY	WSL2512R1000FEA
1	R <sub>T</sub>	49.9 k $\Omega$ 1%	VISHAY	CRCW080549K9FKEA
1	R <sub>UV1</sub>	18.2 k $\Omega$ 1%	VISHAY	CRCW080518K2FKEA
1	R <sub>UV2</sub>	130 k $\Omega$ 1%	VISHAY	CRCW0805130KFKEA

## APPLICATIONS INFORMATION

The following designs are provided as reference circuits. For a specific design, the steps in the *Design Procedure* section should be performed. In all designs, an RC filter (0.1  $\mu$ F, 10 $\Omega$ ) is recommended at VIN placed as close as possible to the LM3421/23 device. This filter is not shown in the following designs.

### DESIGN #2 - LM3421 BOOST Application



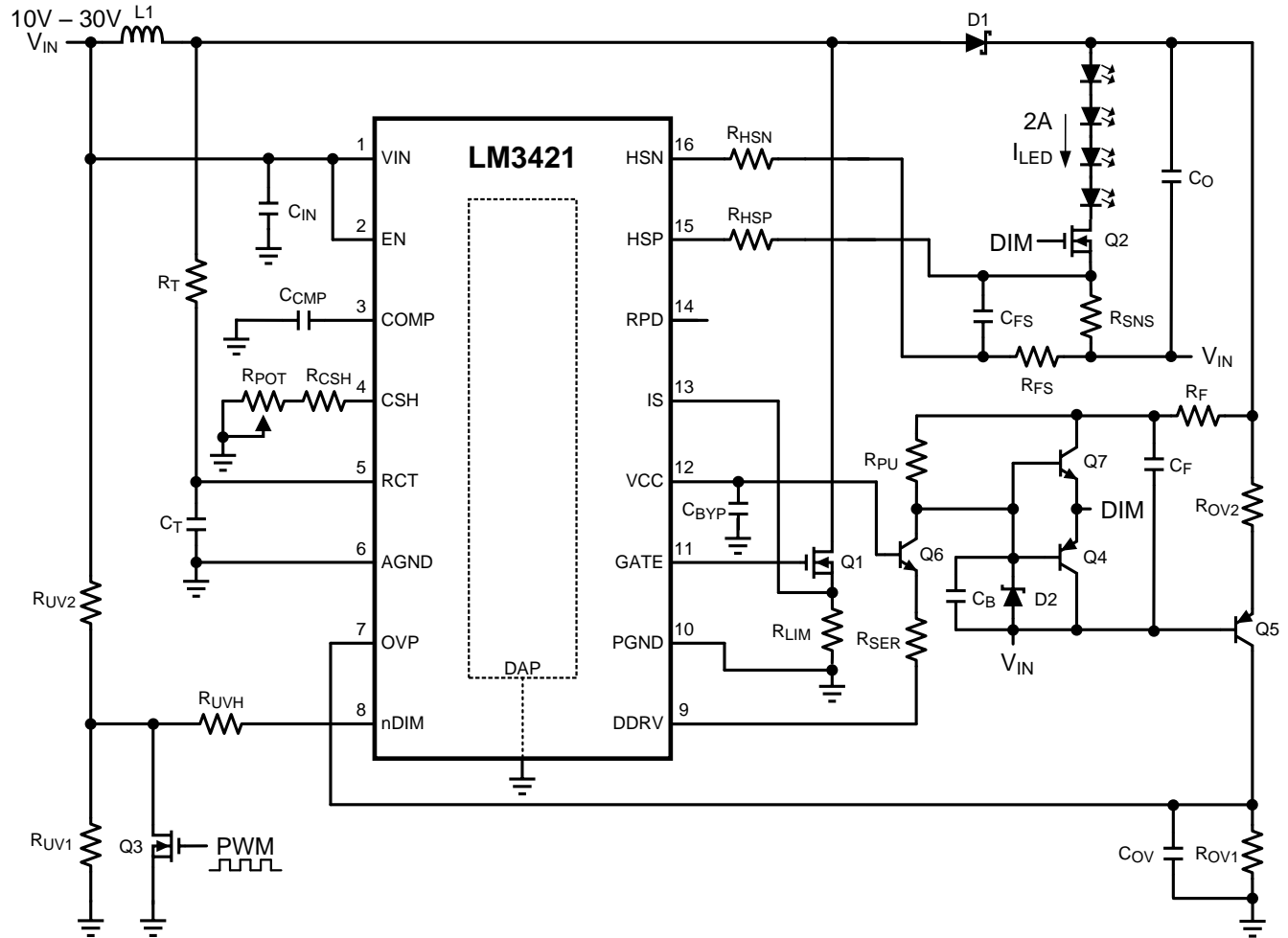
### Features

- Input: 8V to 28V
- Output: 9 LEDs at 1A
- PWM Dimming up to 30kHz
- 700 kHz Switching Frequency

**DESIGN #2 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3421	Boost controller	TI	LM3421MH
1	C <sub>BYP</sub>	2.2 $\mu$ F X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C <sub>COMP</sub>	0.1 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C <sub>FS</sub>	DNP		
4	C <sub>IN</sub>	4.7 $\mu$ F X7R 10% 100V	TDK	C5750X7R2A475K
4	C <sub>O</sub>	10 $\mu$ F X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
2	D1, D2	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1	33 $\mu$ H 20% 6.3A	COILCRAFT	MSS1278-333MLB
2	Q1, Q2	NMOS 60V 8A	VISHAY	SI4436DY
1	Q3	NMOS 60V 115mA	ON-SEMI	2N7002ET1G
2	R <sub>CSH</sub> , R <sub>OV1</sub>	12.4 k $\Omega$ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	0 $\Omega$ 1%	VISHAY	CRCW08050000Z0EA
2	R <sub>HSP</sub> , R <sub>HNS</sub>	1.0 k $\Omega$ 1%	VISHAY	CRCW08051K00FKEA
1	R <sub>LIM</sub>	0.06 $\Omega$ 1% 1W	VISHAY	WSL2512R0600FEA
1	R <sub>OV2</sub>	499 k $\Omega$ 1%	VISHAY	CRCW0805499KFKEA
1	R <sub>SNS</sub>	0.1 $\Omega$ 1% 1W	VISHAY	WSL2512R1000FEA
1	R <sub>UV2</sub>	10.0 k $\Omega$ 1%	VISHAY	CRCW080510K0FKEA
1	R <sub>T</sub>	35.7 k $\Omega$ 1%	VISHAY	CRCW080535K7FKEA
1	R <sub>UV1</sub>	1.82 k $\Omega$ 1%	VISHAY	CRCW08051K82FKEA
1	R <sub>UVH</sub>	17.8 k $\Omega$ 1%	VISHAY	CRCW080517K8FKEA

DESIGN #3 - LM3421 BUCK-BOOST Application



Features

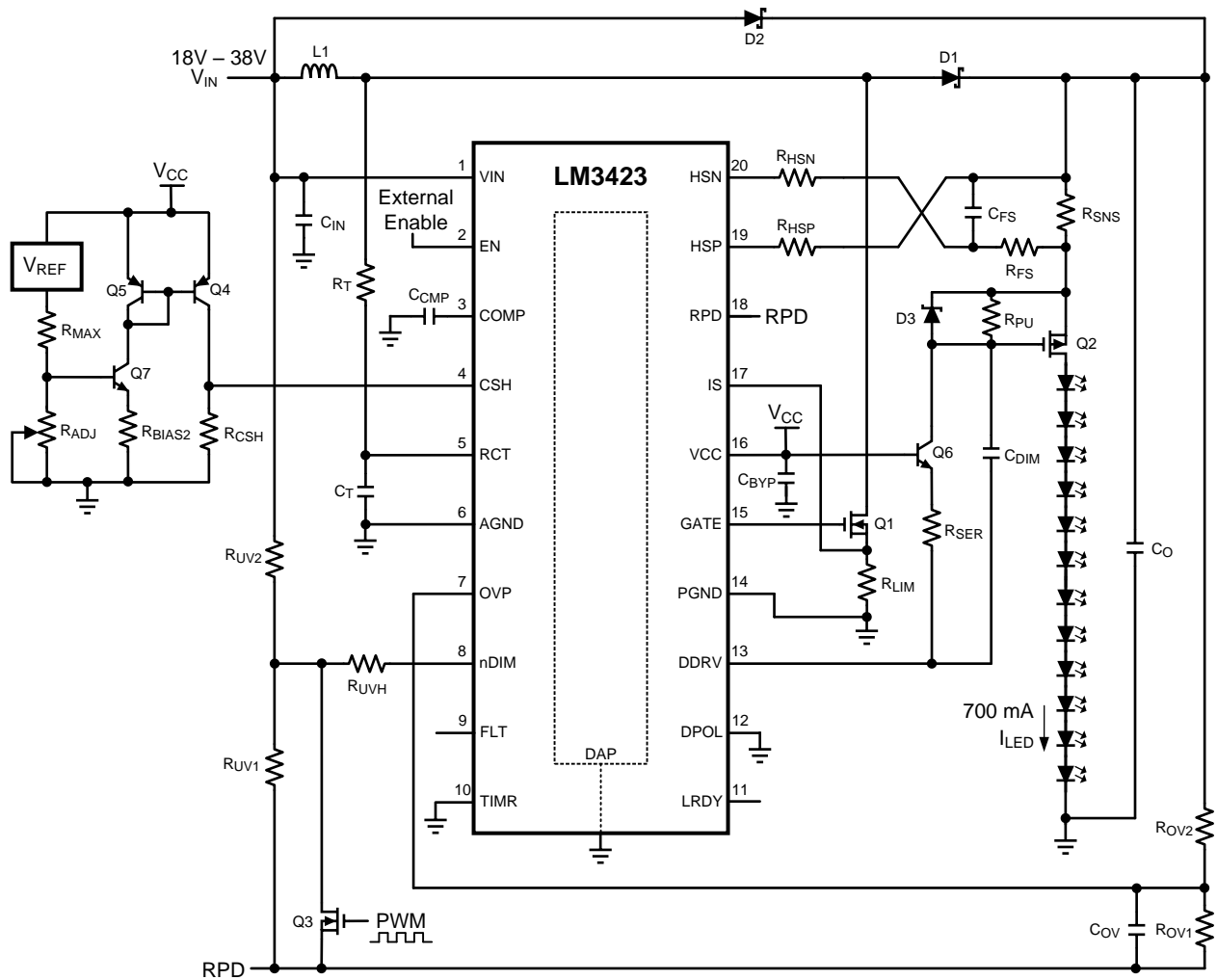
- Input: 10V to 30V
- Output: 4 LEDs at 2A
- PWM Dimming up to 10kHz
- Analog Dimming
- 600 kHz Switching Frequency



**DESIGN #3 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3421	Buck-boost controller	TI	LM3421MH
1	C <sub>B</sub>	100 pF COG/NPO 5% 50V	MURATA	GRM2165C1H101JA01D
1	C <sub>BYP</sub>	2.2 μF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
3	C <sub>COMP</sub> , C <sub>REF</sub> , C <sub>SS</sub>	1 μF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	C <sub>F</sub>	0.1 μF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C <sub>FS</sub>	DNP		
4	C <sub>IN</sub>	6.8 μF X7R 10% 50V	TDK	C5750X7R1H685K
4	C <sub>O</sub>	10 μF X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	22 μH 20% 7.2A	COILCRAFT	MSS1278-223MLB
2	Q1, Q2	NMOS 60V 8A	VISHAY	SI4436DY
1	Q3	NMOS 60V 260mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 40V 200 mA	FAIRCHILD	MMBT5087
1	Q5	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	Q6	NPN 300V 600 mA	FAIRCHILD	MMBTA42
1	Q7	NPN 40V 200 mA	FAIRCHILD	MMBT6428
1	R <sub>CSH</sub>	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>F</sub>	10Ω 1%	VISHAY	CRCW080510R0FKEA
1	R <sub>FS</sub>	0Ω 1%	VISHAY	CRCW08050000Z0EA
1	R <sub>UV2</sub>	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R <sub>HSP</sub> , R <sub>HSN</sub>	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R <sub>LIM</sub>	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R <sub>OV1</sub>	18.2 kΩ 1%	VISHAY	CRCW080518K2FKEA
1	R <sub>OV2</sub>	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R <sub>POT</sub>	1 MΩ potentiometer	BOURNS	3352P-1-105
1	R <sub>PU</sub>	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R <sub>SER</sub>	499Ω 1%	VISHAY	CRCW0805499RFKEA
1	R <sub>SNS</sub>	0.05Ω 1% 1W	VISHAY	WSL2512R0500FEA
1	R <sub>T</sub>	41.2 kΩ 1%	VISHAY	CRCW080541K2FKEA
1	R <sub>UV1</sub>	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R <sub>UVH</sub>	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

DESIGN #4 - LM3423 BOOST Application



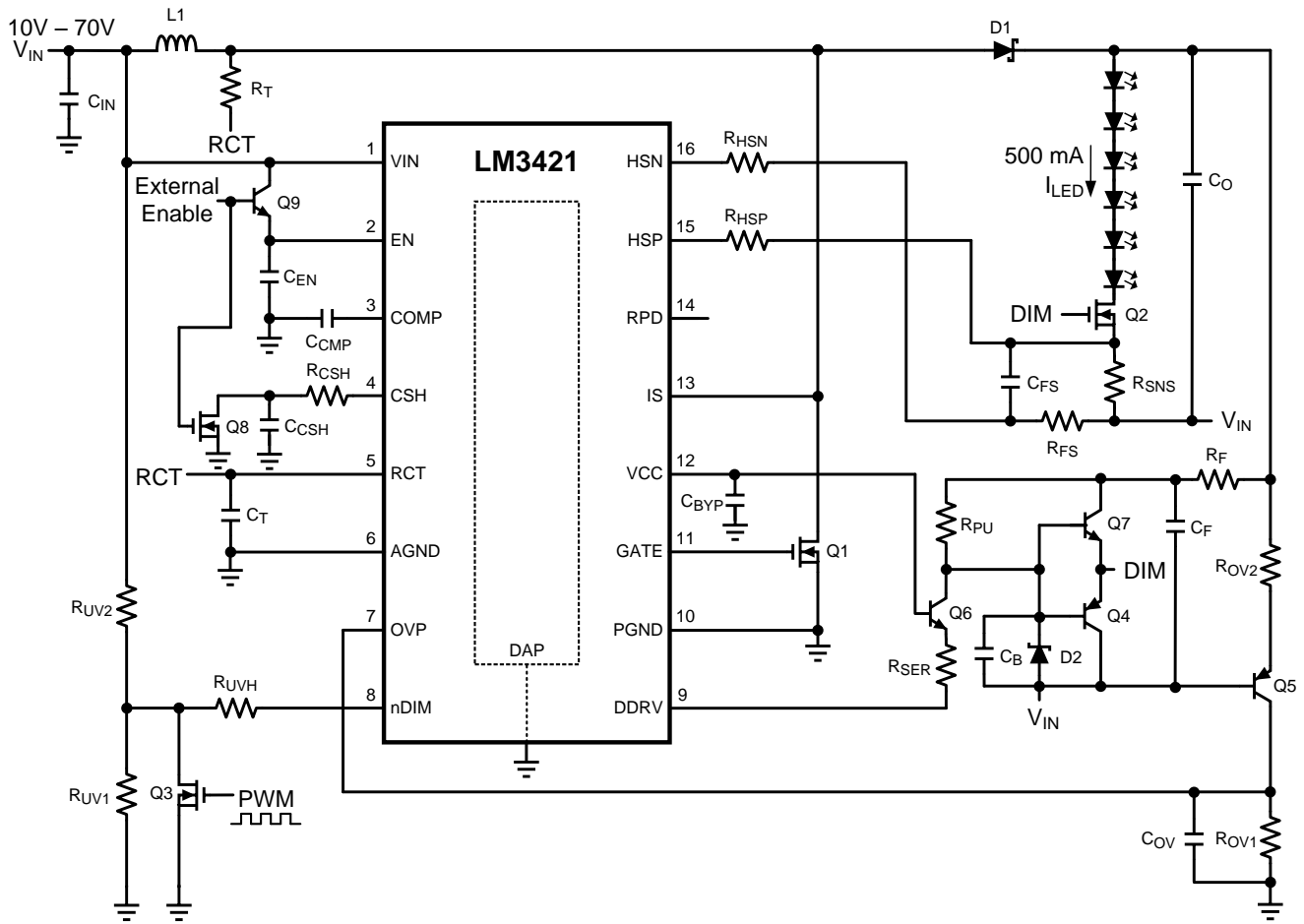
Features

- Input: 18V to 38V
- Output: 12 LEDs at 700mA
- High Side PWM Dimming up to 30 kHz
- Analog Dimming
- Zero Current Shutdown
- 700 kHz Switching Frequency

**DESIGN #4 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3423	Boost controller	TI	LM3423MH
1	C <sub>BYP</sub>	2.2 $\mu$ F X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C <sub>COMP</sub>	1 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	C <sub>FS</sub>	0.1 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E104KA01L
4	C <sub>IN</sub>	4.7 $\mu$ F X7R 10% 100V	TDK	C5750X7R2A475K
4	C <sub>O</sub>	10 $\mu$ F X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
2	D1, D2	Schottky 60V 5A	COMCHIP	CDBC560-G
1	D3	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	47 $\mu$ H 20% 5.3A	COILCRAFT	MSS1278-473MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	PMOS 70V 5.7A	ZETEX	ZXMP7A17K
1	Q3	NMOS 60V 260mA	ON-SEMI	2N7002ET1G
1	Q4, Q5 (dual pack)	Dual PNP 40V 200mA	FAIRCHILD	FFB3906
1	Q6	NPN 300V 600mA	FAIRCHILD	MMBTA42
1	Q7	NPN 40V 200 mA	FAIRCHILD	MMBT3904
1	R <sub>ADJ</sub>	100 k $\Omega$ potentiometer	BOURNS	3352P-1-104
1	R <sub>BIAS2</sub>	17.4 k $\Omega$ 1%	VISHAY	CRCW080517K4FKEA
2	R <sub>CSH</sub> , R <sub>OV1</sub>	12.4 k $\Omega$ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	10 $\Omega$ 1%	VISHAY	CRCW080510R0FKEA
3	R <sub>HSP</sub> , R <sub>HSN</sub> , R <sub>MAX</sub>	1.0 k $\Omega$ 1%	VISHAY	CRCW08051K00FKEA
1	R <sub>LIM</sub>	0.06 $\Omega$ 1% 1W	VISHAY	WSL2512R0600FEA
1	R <sub>OV2</sub>	499 k $\Omega$ 1%	VISHAY	CRCW0805499KFKEA
1	R <sub>SNS</sub>	0.15 $\Omega$ 1% 1W	VISHAY	WSL2512R1500FEA
1	R <sub>T</sub>	35.7 k $\Omega$ 1%	VISHAY	CRCW080535K7FKEA
1	R <sub>UV1</sub>	1.43 k $\Omega$ 1%	VISHAY	CRCW08051K43FKEA
1	R <sub>UV2</sub>	10.0 k $\Omega$ 1%	VISHAY	CRCW080510K0FKEA
1	R <sub>UVH</sub>	16.9 k $\Omega$ 1%	VISHAY	CRCW080516K9FKEA

DESIGN #5 - LM3421 BUCK-BOOST Application



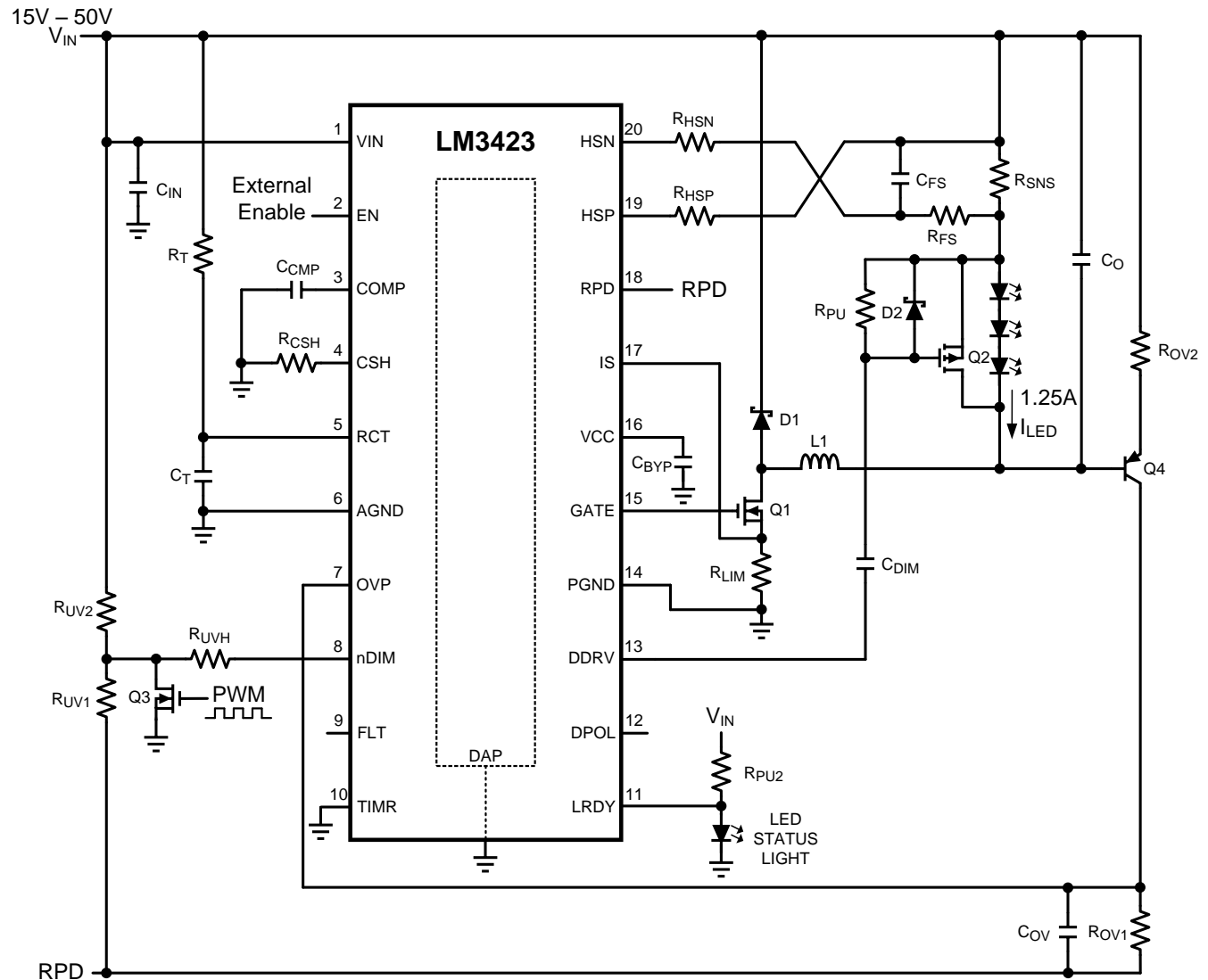
Features

- Input: 10V to 70V
- Output: 6 LEDs at 500mA
- PWM Dimming up to 10 kHz
- Slow Fade Out
- MosFET R<sub>DS-ON</sub> Sensing
- 700 kHz Switching Frequency

**DESIGN #5 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3421	Buck-boost controller	TI	LM3421MH
1	C <sub>B</sub>	100 pF COG/NPO 5% 50V	MURATA	GRM2165C1H101JA01D
1	C <sub>BYP</sub>	2.2 μF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C <sub>COMP</sub>	1 μF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	C <sub>F</sub>	0.1 μF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C <sub>F5</sub>	DNP		
4	C <sub>IN</sub>	4.7 μF X7R 10% 100V	TDK	C5750X7R2A475K
4	C <sub>O</sub>	10 μF X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	68 μH 20% 4.3A	COILCRAFT	MSS1278-683MLB
2	Q1, Q2	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q3	NMOS 60V 260mA	ON-SEMI	2N7002ET1G
2	Q4, Q8	PNP 40V 200mA	FAIRCHILD	MMBT5087
1	Q5	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	Q6	NPN 300V 600mA	FAIRCHILD	MMBTA42
2	Q7, Q9	NPN 40V 200mA	FAIRCHILD	MMBT6428
1	R <sub>CSH</sub>	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	0Ω 1%	VISHAY	CRCW08050000Z0EA
1	R <sub>UV2</sub>	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R <sub>HSP</sub> , R <sub>H5N</sub>	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R <sub>OV1</sub>	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R <sub>OV2</sub>	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R <sub>PU</sub>	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R <sub>SER</sub>	499Ω 1%	VISHAY	CRCW0805499RFKEA
1	R <sub>SNS</sub>	0.2Ω 1% 1W	VISHAY	WSL2512R2000FEA
1	R <sub>T</sub>	35.7 kΩ 1%	VISHAY	CRCW080535K7FKEA
1	R <sub>UV1</sub>	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R <sub>UVH</sub>	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

## DESIGN #6 - LM3423 BUCK Application



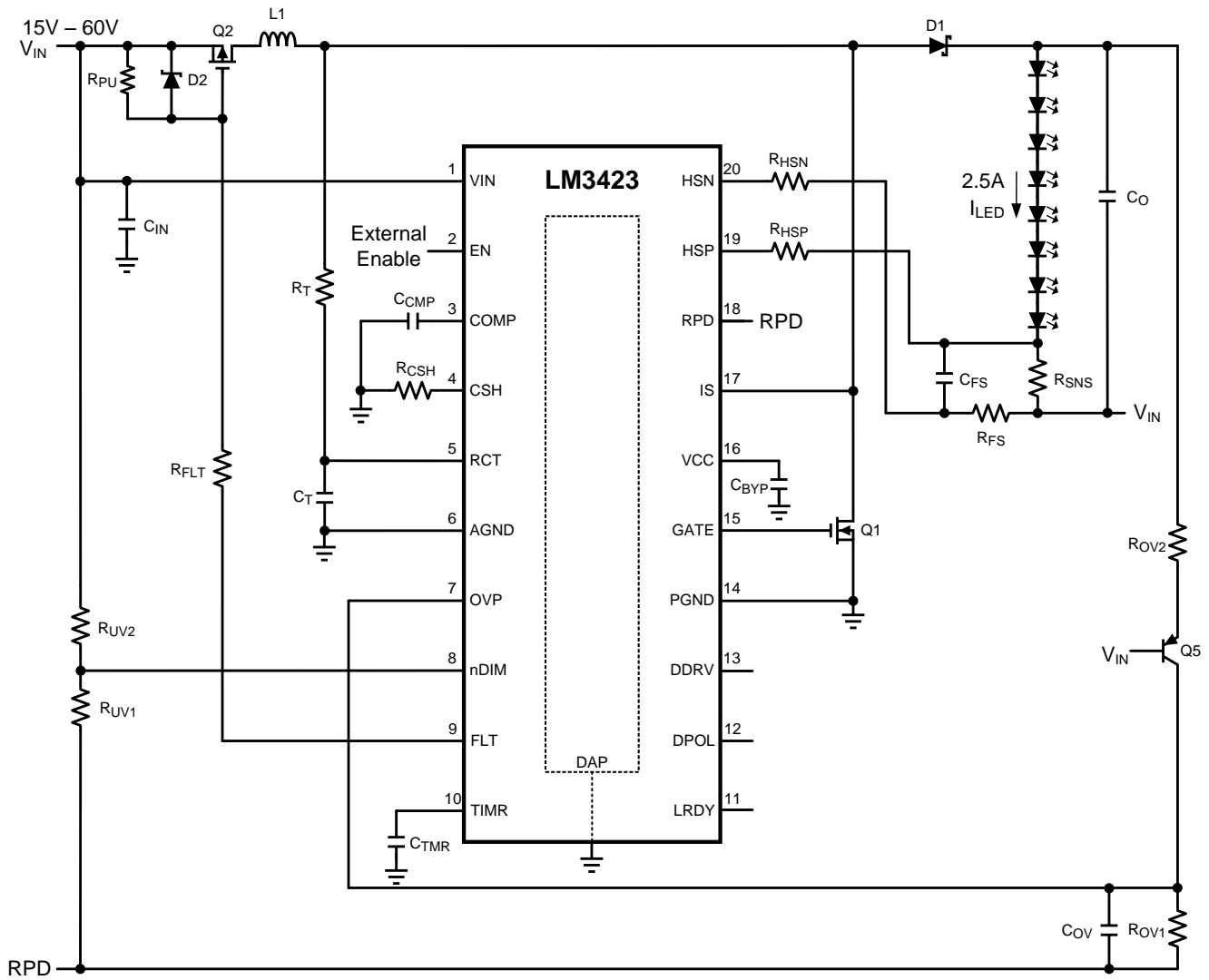
### Features

- Input: 15V to 50V
- Output: 3 LEDs at 1.25A
- PWM Dimming up to 50 kHz
- LED Status Indicator
- Zero Current Shutdown
- 700 kHz Switching Frequency

**DESIGN #6 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3423	Buck controller	TI	LM3423MH
1	C <sub>BYP</sub>	2.2 $\mu$ F X7R 10% 16V	MURATA	GRM21BR71C225KA12L
2	C <sub>COMP</sub> , C <sub>DIM</sub>	0.1 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C <sub>FS</sub>	DNP		
4	C <sub>IN</sub>	4.7 $\mu$ F X7R 10% 100V	TDK	C5750X7R2A475K
0	C <sub>O</sub>	DNP		
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	22 $\mu$ H 20% 7.3A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	PMOS 30V 6.2A	VISHAY	SI3483DV
1	Q3	NMOS 60V 115mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R <sub>CSH</sub>	12.4 k $\Omega$ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	0 $\Omega$ 1%	VISHAY	CRCW08050000OZEA
2	R <sub>HSP</sub> , R <sub>HSN</sub>	1.0 k $\Omega$ 1%	VISHAY	CRCW08051K00FKEA
1	R <sub>LIM</sub>	0.04 $\Omega$ 1% 1W	VISHAY	WSL2512R0400FEA
1	R <sub>OV1</sub>	21.5 k $\Omega$ 1%	VISHAY	CRCW080521K5FKEA
1	R <sub>OV2</sub>	499 k $\Omega$ 1%	VISHAY	CRCW0805499KFKEA
3	R <sub>PU</sub> , R <sub>PU2</sub> , R <sub>UV2</sub>	100 k $\Omega$ 1%	VISHAY	CRCW0805100KFKEA
1	R <sub>T</sub>	35.7 k $\Omega$ 1%	VISHAY	CRCW080535K7FKEA
1	R <sub>SNS</sub>	0.08 $\Omega$ 1% 1W	VISHAY	WSL2512R0800FEA
1	R <sub>UV1</sub>	11.5 k $\Omega$ 1%	VISHAY	CRCW080511K5FKEA

## DESIGN #7 - LM3423 BUCK-BOOST Application



### Features

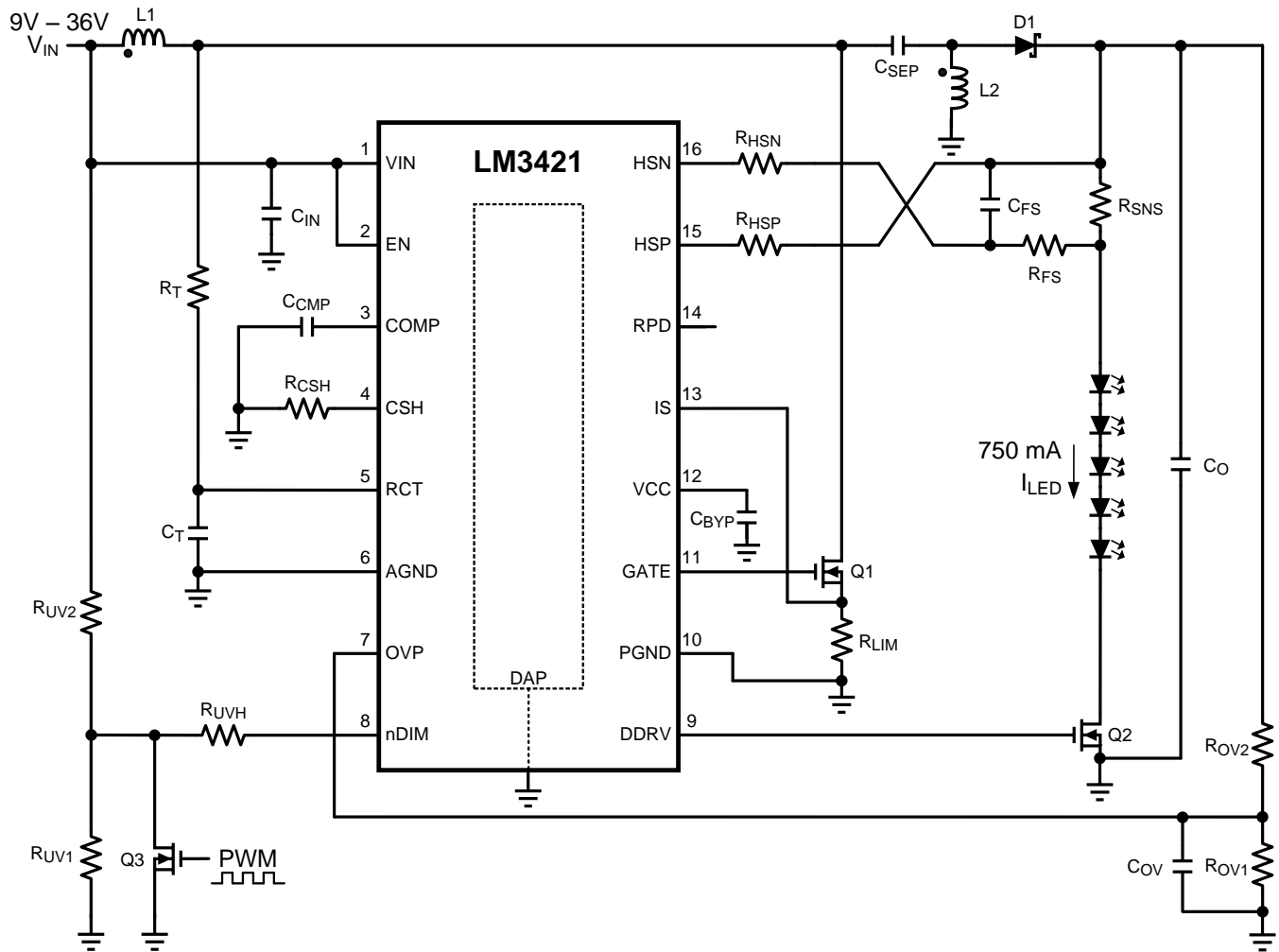
- Input: 15V to 60V
- Output: 8 LEDs at 2.5A
- Fault Input Disconnect
- Zero Current Shutdown
- 500 kHz Switching Frequency



**DESIGN #7 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3423	Buck-boost controller	TI	LM3423MH
1	C <sub>BYP</sub>	2.2 $\mu$ F X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C <sub>CMP</sub>	0.33 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E334KA01L
1	C <sub>FS</sub>	0.1 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E104KA01L
4	C <sub>IN</sub>	4.7 $\mu$ F X7R 10% 100V	TDK	C5750X7R2A475K
4	C <sub>O</sub>	10 $\mu$ F X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	C <sub>TMR</sub>	220 pF COG/NPO 5% 50V	MURATA	GRM2165C1H221JA01D
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	22 $\mu$ H 20% 7.2A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	PMOS 70V 5.7A	ZETEX	ZXMP7A17K
1	Q5	PNP 150V 600 mA	FAIRCHILD	MMBT5401
2	R <sub>CSH</sub> , R <sub>OV1</sub>	12.4 k $\Omega$ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	10 $\Omega$ 1%	VISHAY	CRCW080510R0FKEA
2	R <sub>FLT</sub> , R <sub>PU2</sub>	100 k $\Omega$ 1%	VISHAY	CRCW0805100KFKEA
2	R <sub>HSP</sub> , R <sub>HSN</sub>	1.0 k $\Omega$ 1%	VISHAY	CRCW08051K00FKEA
2	R <sub>LIM</sub> , R <sub>SNS</sub>	0.04 $\Omega$ 1% 1W	VISHAY	WSL2512R0400FEA
1	R <sub>OV1</sub>	15.8 k $\Omega$ 1%	VISHAY	CRCW080515K8FKEA
1	R <sub>OV2</sub>	499 k $\Omega$ 1%	VISHAY	CRCW0805499KFKEA
1	R <sub>T</sub>	49.9 k $\Omega$ 1%	VISHAY	CRCW080549K9FKEA
1	R <sub>UV1</sub>	13.7 k $\Omega$ 1%	VISHAY	CRCW080513K7FKEA
1	R <sub>UV2</sub>	150 k $\Omega$ 1%	VISHAY	CRCW0805150KFKEA

DESIGN #8 - LM3421 SEPIC Application



Features

- Input: 9V to 36V
- Output: 5 LEDs at 750mA
- PWM Dimming up to 30 kHz
- 500 kHz Switching Frequency

**DESIGN #8 Bill of Materials**

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3421	SEPIC controller	TI	LM3421MH
1	C <sub>BYP</sub>	2.2 $\mu$ F X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C <sub>CMP</sub>	0.47 $\mu$ F X7R 10% 25V	MURATA	GRM21BR71E474KA01L
0	C <sub>FS</sub>	DNP		
4	C <sub>IN</sub>	4.7 $\mu$ F X7R 10% 100V	TDK	C5750X7R2A475K
4	C <sub>O</sub>	10 $\mu$ F X7R 10% 50V	TDK	C4532X7R1H106K
1	C <sub>SEP</sub>	1.0 $\mu$ F X7R 10% 100V	TDK	C4532X7R2A105K
1	C <sub>OV</sub>	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C <sub>T</sub>	1000 pF COG/NPO 5% 50V	MURATA	GRM2165C1H102JA01D
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
2	L1, L2	68 $\mu$ H 20% 4.3A	COILCRAFT	DO3340P-683
2	Q1, Q2	NMOS 60V 8A	VISHAY	SI4436DY
1	Q3	NMOS 60V 115 mA	ON-SEMI	2N7002ET1G
1	R <sub>CSH</sub>	12.4 k $\Omega$ 1%	VISHAY	CRCW080512K4FKEA
1	R <sub>FS</sub>	0 $\Omega$ 1%	VISHAY	CRCW08050000OZEA
2	R <sub>HSP</sub> , R <sub>HSN</sub>	750 $\Omega$ 1%	VISHAY	CRCW0805750RFKEA
1	R <sub>LIM</sub>	0.04 $\Omega$ 1% 1W	VISHAY	WSL2512R0400FEA
1	R <sub>OV1</sub>	15.8 k $\Omega$ 1%	VISHAY	CRCW080515K8FKEA
1	R <sub>OV2</sub>	499 k $\Omega$ 1%	VISHAY	CRCW0805499KFKEA
2	R <sub>REF1</sub> , R <sub>REF2</sub>	49.9 k $\Omega$ 1%	VISHAY	CRCW080549K9FKEA
1	R <sub>SNS</sub>	0.1 $\Omega$ 1% 1W	VISHAY	WSL2512R1000FEA
1	R <sub>T</sub>	49.9 k $\Omega$ 1%	VISHAY	CRCW080549K9FKEA
1	R <sub>UV1</sub>	1.62 k $\Omega$ 1%	VISHAY	CRCW08051K62FKEA
1	R <sub>UV2</sub>	10.0 k $\Omega$ 1%	VISHAY	CRCW080510K0FKEA
1	R <sub>UVH</sub>	16.9 k $\Omega$ 1%	VISHAY	CRCW080516K9FKEA

## REVISION HISTORY

Changes from Revision D (May 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	59

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3421MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH	<a href="#">Samples</a>
LM3421MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3421 MH	<a href="#">Samples</a>
LM3421Q0MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	LM3421 Q0MH	<a href="#">Samples</a>
LM3421Q0MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	LM3421 Q0MH	<a href="#">Samples</a>
LM3421Q1MH/NOPB	ACTIVE	HTSSOP	PWP	16	92	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3421 Q1MH	<a href="#">Samples</a>
LM3421Q1MHX/NOPB	ACTIVE	HTSSOP	PWP	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3421 Q1MH	<a href="#">Samples</a>
LM3423MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH	<a href="#">Samples</a>
LM3423MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3423 MH	<a href="#">Samples</a>
LM3423Q0MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	LM3423 Q0MH	<a href="#">Samples</a>
LM3423Q0MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 150	LM3423 Q0MH	<a href="#">Samples</a>
LM3423Q1MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3423 Q1MH	<a href="#">Samples</a>
LM3423Q1MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3423 Q1MH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF LM3421, LM3421-Q1, LM3423, LM3423-Q1 :**

● Catalog: [LM3421](#), [LM3423](#)

● Automotive: [LM3421-Q1](#), [LM3423-Q1](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3421MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM3421Q0MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM3421Q1MHX/NOPB	HTSSOP	PWP	16	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM3423MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM3423Q0MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM3423Q1MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

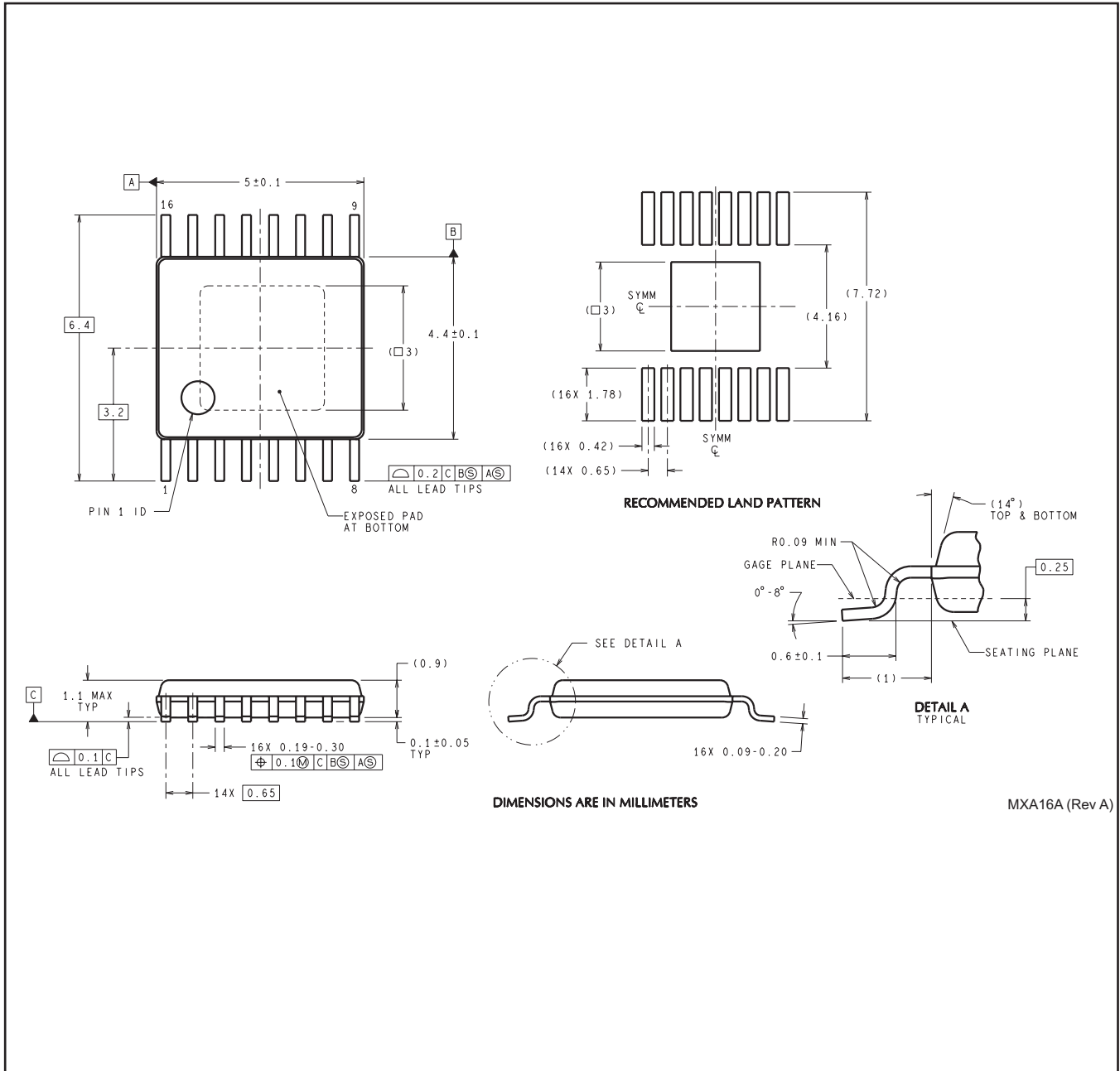

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3421MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM3421Q0MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM3421Q1MHX/NOPB	HTSSOP	PWP	16	2500	367.0	367.0	35.0
LM3423MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM3423Q0MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM3423Q1MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0





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