LM26420/LM26420Q Dual 2.0A, High Frequency Synchronous Step-Down DC-DC Regulator

Check for Samples: LM26420

FEATURES

- **Input Voltage Range of 3.0V to 5.5V**
- **Output Voltage Range of 0.8V to 4.5V**
- **2.0A Output Current per Output**
- **High Switching Frequencies**
  - **2.2MHz (LM26420X)**
  - **0.55MHz (LM26420Y)**
- **75mΩ PMOS Switch**
- **50mΩ NMOS Switch**
- **0.8V, 1.5% Internal Voltage Reference**
- **Internal Soft-start**
- **Independent Power Good for Each Output**
- **Independent Precision Enable for Each Output**
- **Current Mode, PWM Operation**
- **Thermal Shutdown**
- **Over Voltage Protection**
- **Start-up into Pre-biased Output Loads**
- **Outputs are 180° Out of Phase**
- **LM26420Q is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)**

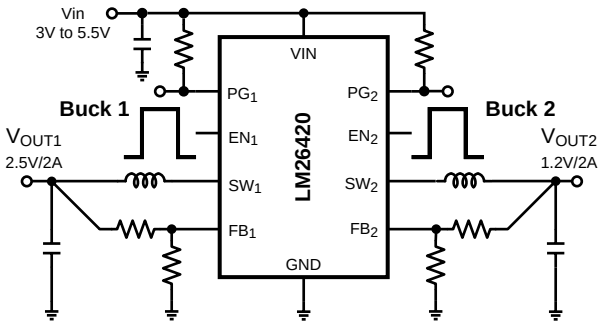
APPLICATIONS

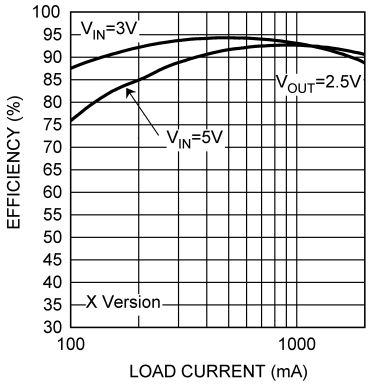
- **Local 5V to Vcore Step-Down Converters**
- **Core Power in HDDs**
- **Set-Top Boxes**
- **USB Powered Devices**
- **DSL Modems**
- **Powering Core and I/O Voltages for FPGAs, CPLDs, and ASICs**

DESCRIPTION

The LM26420 regulator is a monolithic, high frequency, dual PWM step-down DC/DC converter in a 16 Pin WQFN and a 20 Pin TSSOP package. It provides all the active functions to provide local DC/DC conversion with fast transient response and accurate regulation in the smallest possible PCB area. With a minimum of external components, the LM26420 is easy to use. The ability to drive two 2.0A loads with an internal 75 mΩ PMOS top switch and an internal 50 mΩ NMOS bottom switch using state-of-the-art 0.5 µm BiCMOS technology results in the best power density available. The world-class control circuitry allows on-times as low as 30ns, thus supporting exceptionally high frequency conversion over the entire 3V to 5.5V input operating range down to the minimum output voltage of 0.8V. Switching frequency is internally set to 550 kHz or 2.2 MHz, allowing the use of extremely small surface mount inductors and chip capacitors. Even though the operating frequency is high, efficiencies up to 93% are easy to achieve. External shutdown is included, featuring an ultra-low stand-by current. The LM26420 utilizes current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce inrush current, pulse-by-pulse current limit, thermal shutdown, power good indicators, precision enables, and output over-voltage protection.

Typical Application Circuit





Connection Diagram

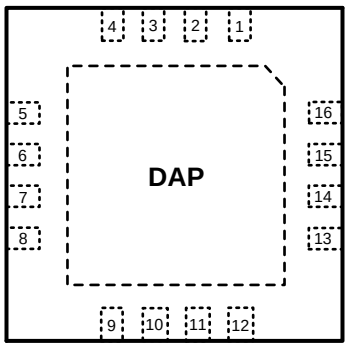


Figure 1. 16-Pin WQFN (TOP VIEW)

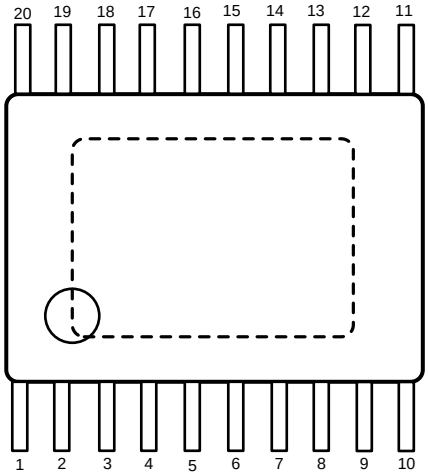


Figure 2. 20-Pin TSSOP (TOP VIEW)

PIN DESCRIPTIONS 20-PIN TSSOP

Pin	Name	Function
3, 4	$VIND_1$	Power Input supply for Buck 1.
17, 18	$VIND_2$	Power Input supply for Buck 2.
1	VINC	Input supply for control circuitry.
6,7	$PGND_1$	Power ground pin for Buck 1.
14, 15	$PGND_2$	Power ground pin for Buck 2.
20	AGND	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to pin.
9	PG_1	Power Good Indicator for Buck 1. Pin is connected through a resistor to an external supply (open drain output).
12	PG_2	Power Good Indicator for Buck 2. Pin is connected through a resistor to an external supply (open drain output).
8	FB_1	Feedback pin for Buck 1. Connect to external resistor divider to set output voltage.
13	FB_2	Feedback pin for Buck 2. Connect to external resistor divider to set output voltage.
5	SW_1	Output switch for Buck 1. Connect to the inductor.
16	SW_2	Output switch for Buck 2. Connect to the inductor.
2	EN_1	Enable control input. Logic high enable operation for Buck 1. Do not allow this pin to float or be greater than VIN + 0.3V.

PIN DESCRIPTIONS 20-PIN TSSOP (continued)

Pin	Name	Function
19	EN_2	Enable control input. Logic high enable operation for Buck 2. Do not allow this pin to float or be greater than VIN + 0.3V.
10, 11, DAP	Die Attach Pad	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.

PIN DESCRIPTIONS 16-PIN WQFN

Pin	Name	Function
1,2	$VIND_1$	Power Input supply for Buck 1.
11, 12	$VIND_2$	Power Input supply for Buck 2.
15	VINC	Input supply for control circuitry.
4	$PGND_1$	Power ground pin for Buck 1.
9	$PGND_2$	Power ground pin for Buck 2.
14	AGND	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to pin.
6	PG_1	Power Good Indicator for Buck 1. Pin is connected through a resistor to an external supply (open drain output).
7	PG_2	Power Good Indicator for Buck 2. Pin is connected through a resistor to an external supply (open drain output).
5	FB_1	Feedback pin for Buck 1. Connect to external resistor divider to set output voltage.
8	FB_2	Feedback pin for Buck 2. Connect to external resistor divider to set output voltage.
3	SW_1	Output switch for Buck 1. Connect to the inductor.
10	SW_2	Output switch for Buck 2. Connect to the inductor.
16	EN_1	Enable control input. Logic high enable operation for Buck 1. Do not allow this pin to float or be greater than VIN + 0.3V.
13	EN_2	Enable control input. Logic high enable operation for Buck 2. Do not allow this pin to float or be greater than VIN + 0.3V.
DAP	Die Attach Pad	Connect to system ground for low thermal impedance and as a primary electrical GND connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

V_{IN}		-0.5V to 7V
FB Voltage		-0.5V to 3V
EN Voltage		-0.5V to 7V
SW Voltage		-0.5V to 7V
ESD Susceptibility	Human Body Model[3]	2 kV
Junction Temperature[4]		150°C
Storage Temperature		−65°C to +150°C
Soldering Information	Infrared or Convection Reflow (15 sec)	220°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-A114.
(4) Thermal shutdown will occur if the junction temperature exceeds the maximum junction temperature of the device.

Operating Ratings

V_{IN}	3V to 5.5V
Junction Temperature	−40°C to +125°C

Electrical Characteristics Per Buck

VIN = 5V unless otherwise indicated under the **Conditions** column. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage		**0.788**	0.800	**0.812**	V
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3V to 5.5V		0.05		%/V
I_B	Feedback Input Bias Current			0.40	**100**	nA
UVLO	Under-voltage Lockout	V_{IN} Rising		2.628	**2.90**	V
		V_{IN} Falling	**2.0**	2.3		V
	UVLO Hysteresis			330		mV
F_{SW}	Switching Frequency	LM26420-X	**1.85**	2.2	**2.65**	MHz
		LM26420-Y	**0.4**	0.55	**0.7**	
F_{FB}	Frequency Fold-back	LM26420-X		300		kHz
		LM26420-Y		150		
D_{MAX}	Maximum Duty Cycle	LM26420-X	**86**	91.5		%
		LM26420-Y	**90**	98		
R_{DSON_TOP}	TOP Switch On Resistance	WQFN-16 Package		75	**135**	mΩ
		TSSOP-20 Package		70	**135**	
R_{DSON_BOT}	BOTTOM Switch On Resistance	WQFN-16 Package		55	**100**	mΩ
		TSSOP-20 Package		45	**80**	
I_{CL_TOP}	TOP Switch Current Limit	V_{IN} = 3.3V	**2.4**	3.3		A
I_{CL_BOT}	BOTTOM Switch Reverse Current Limit	V_{IN} = 3.3V	**0.4**	0.75		A
ΔΦ	Phase Shift Between SW_1 and SW_2		**160**	180	**200**	°
V_{EN_TH}	Enable Threshold Voltage		**0.97**	1.04	**1.12**	V
	Enable Threshold Hysteresis			0.15		
I_{SW_TOP}	Switch Leakage			-0.7		µA
I_{EN}	Enable Pin Current	Sink/Source		5.0		nA
$V_{PG\text{-}TH\text{-}U}$	Upper Power Good Threshold	FB Pin Voltage Rising	**848**	925	**1,008**	mV
	Upper Power Good Hysteresis			40		mV
$V_{PG\text{-}TH\text{-}L}$	Lower Power Good Threshold	FB Pin Voltage Rising	**656**	710	**791**	mV
	Lower Power Good Hysteresis			40		mV
I_{QVINC}	VINC Quiescent Current (non-switching) with both outputs on	LM26420X/Y V_{FB} = 0.9		3.3	**5.0**	mA
	VINC Quiescent Current (switching) with both outputs on	LM26420X/Y V_{FB} = 0.7		4.7	**6.2**	
	VINC Quiescent Current (shutdown)	All Options V_{EN} = 0V		0.05		µA
I_{QVIND}	VIND Quiescent Current (non-switching)	LM26420X/Y V_{FB} = 0.9		0.9	**1.5**	mA
	VIND Quiescent Current (switching)	LM26420X V_{FB} = 0.7		11.0	**15.0**	
		LM26420Y V_{FB} = 0.7		3.7	**7.5**	
	VIND Quiescent Current (shutdown)	All Options V_{EN} = 0V		0.1		µA
θ_{JA}	Junction to Ambient 0 LFPM Air Flow(1)	WQFN-16		40		°C/W
		TSSOP-20		35		
θ_{JC}	Junction to Case(1)	WQFN-16		6.8		
		TSSOP-20		3.9		
T_{SD}	Thermal Shutdown Temperature			165		°C

(1) Applies to a 4-layer standard JEDEC thermal test board or 4LJEDEC is 4"x3" in size. The board has 2 imbedded copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one, is 2 oz./1oz./1oz./2 oz. For WQFN, thermal vias are placed between the die attach pad in the 1st. copper layer and 2nd. copper layer.

Typical Performance Characteristics

All curves taken at V_{IN} = 5.0V with configuration in typical application circuit shown in Application Information section of this datasheet. T_J = 25°C, unless otherwise specified.

η vs Load "X" V_{IN} = 5V, V_{OUT} = 3.3V

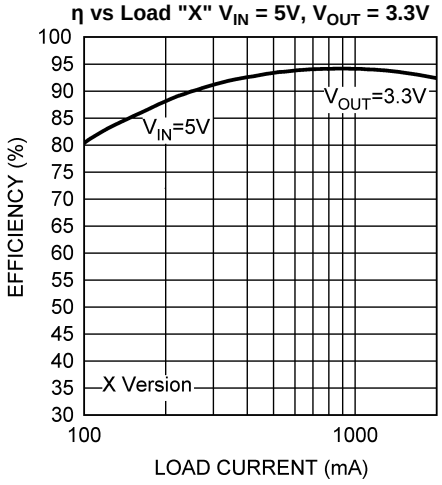


Figure 3.

η vs Load "Y" V_{IN} = 5V, V_{OUT} = 3.3V

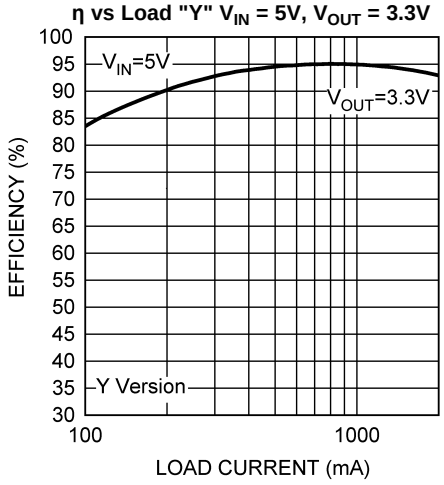


Figure 4.

η vs Load - "X" V_{IN} = 5V & 3V, V_{OUT} = 2.5V

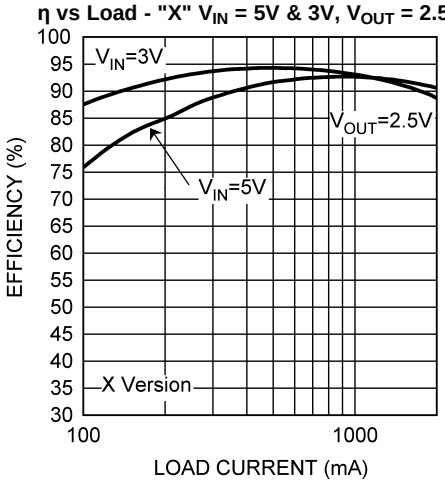


Figure 5.

η vs Load "Y" V_{IN} = 5V & 3V, V_{OUT} = 2.5V

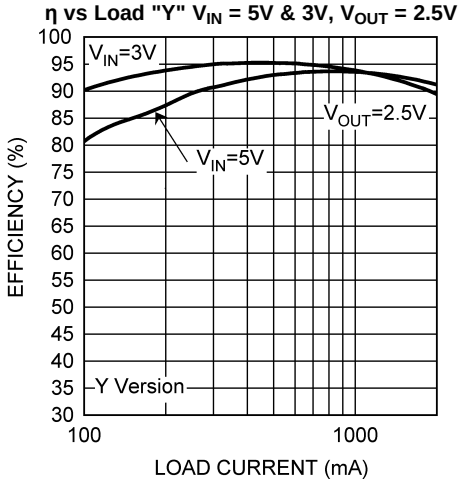


Figure 6.

η vs Load "X" V_{IN} = 5V & 3V, V_{OUT} = 1.8V

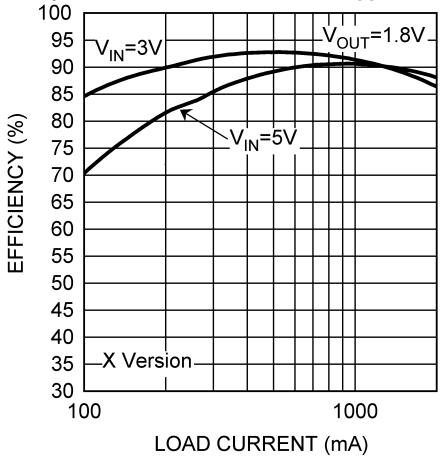


Figure 7.

η vs Load "Y" V_{IN} = 5V & 3V, V_{OUT} = 1.8V

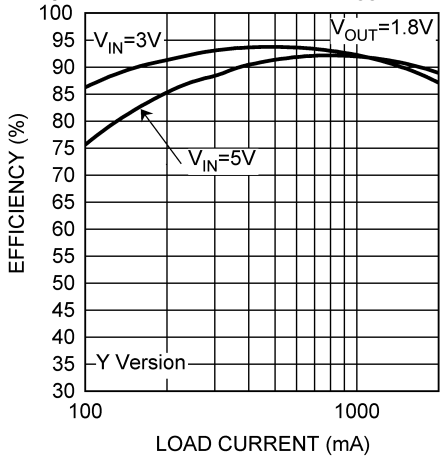


Figure 8.

Typical Performance Characteristics (continued)

All curves taken at V_{IN} = 5.0V with configuration in typical application circuit shown in Application Information section of this datasheet. T_J = 25°C, unless otherwise specified.

η vs Load "X" V_{IN}= 5V & 3V, V_{OUT} = 1.2V

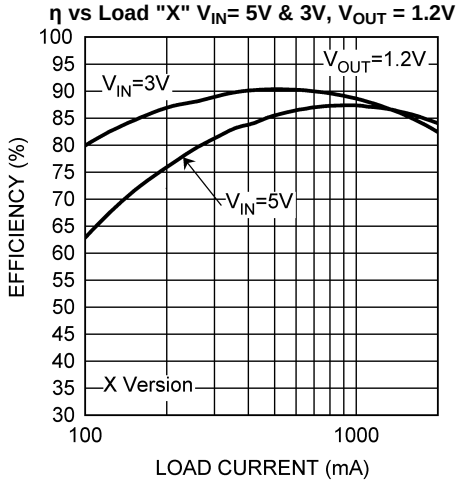


Figure 9.

η vs Load "Y" V_{IN} = 5V & 3V, V_{OUT} = 1.2V

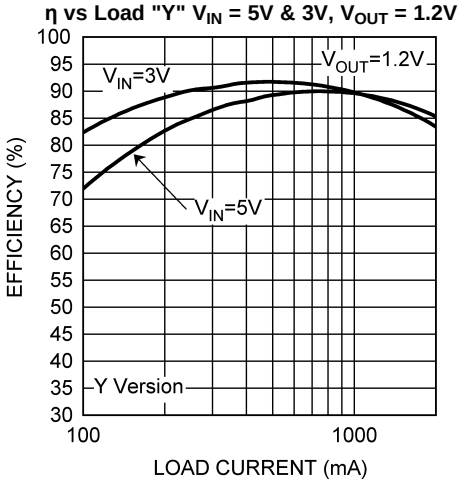


Figure 10.

η vs Load "X" V_{IN} = 5V & 3V, V_{OUT} = 0.8V

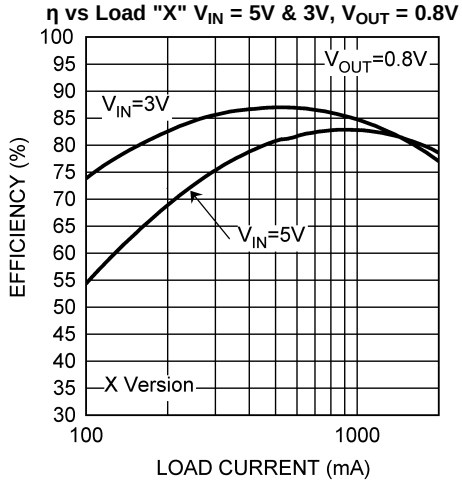


Figure 11.

η vs Load "Y" V_{IN} = 5V & 3V, V_{OUT} = 0.8V

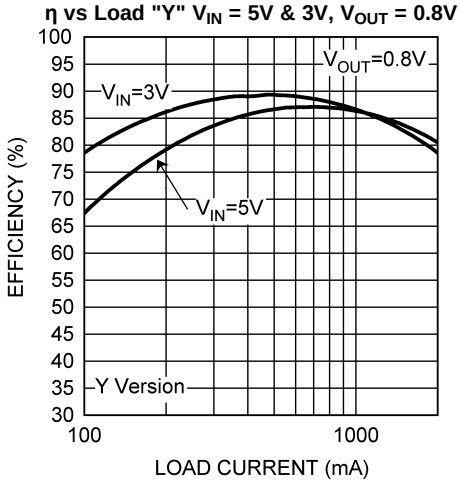


Figure 12.

Load Regulation
V_{IN} = 5V, V_{OUT} = 1.8V (All Options)

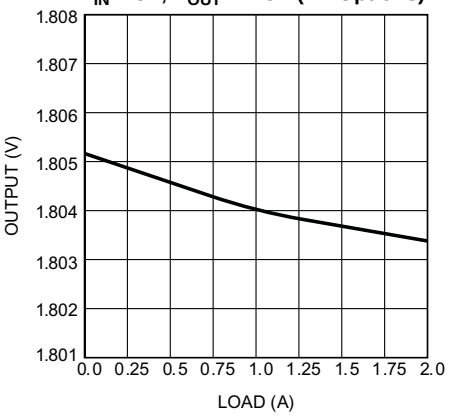


Figure 13.

Load Regulation
V_{IN} = 3V, V_{OUT} = 1.8V (All Options)

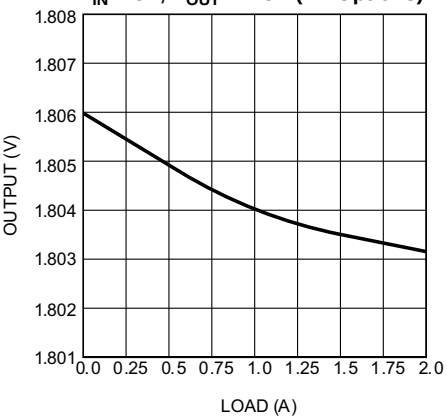


Figure 14.

Typical Performance Characteristics (continued)

All curves taken at V_{IN} = 5.0V with configuration in typical application circuit shown in Application Information section of this datasheet. T_J = 25°C, unless otherwise specified.

Line Regulation - "X"
V_{OUT} = 1.8V, I_{OUT} = 1,000mA

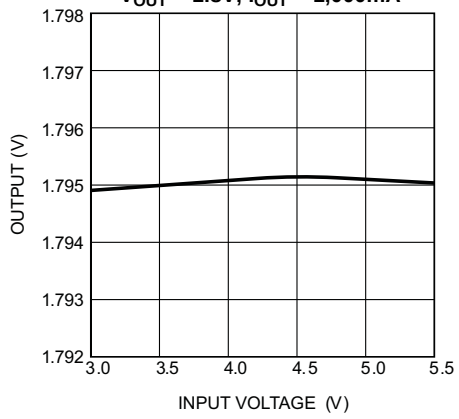


Figure 15.

Line Regulation - "Y"
V_{OUT} = 1.8V, I_{OUT} = 1,000mA

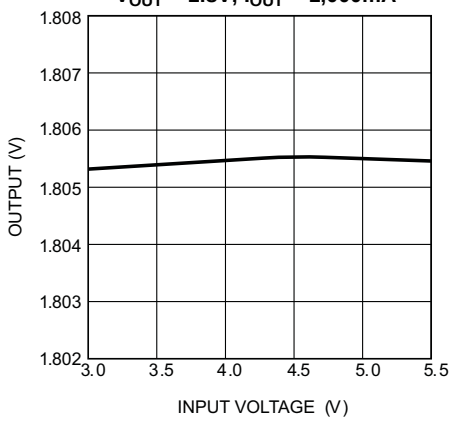


Figure 16.

Oscillator Frequency vs Temperature - "X"

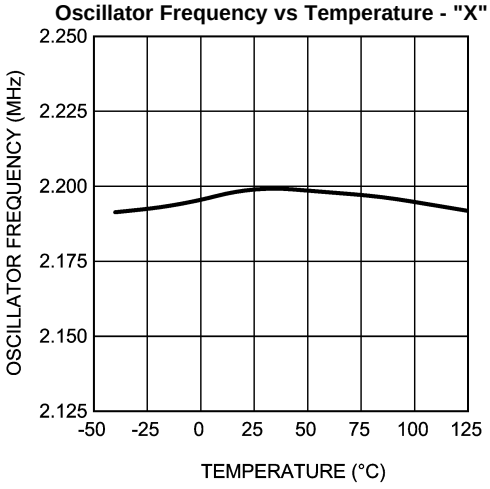


Figure 17.

Oscillator Frequency vs Temperature - "Y"

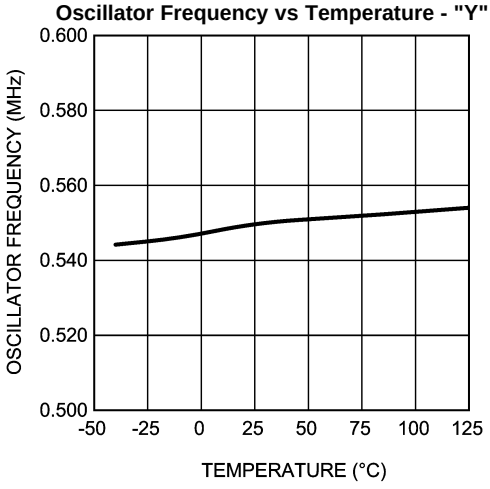


Figure 18.

R_{DSON} TOP vs Temperature (WQFN-16 Package)

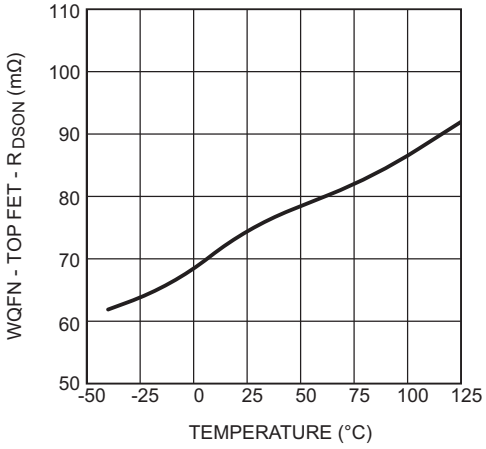


Figure 19.

R_{DSON} BOTTOM vs Temperature (WQFN-16 Package)

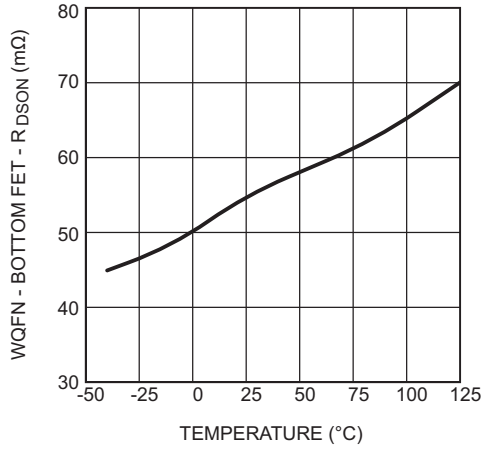


Figure 20.

Typical Performance Characteristics (continued)

All curves taken at V_{IN} = 5.0V with configuration in typical application circuit shown in Application Information section of this datasheet. T_J = 25°C, unless otherwise specified.

R_{DSON} TOP vs Temperature (TSSOP-20 Package)

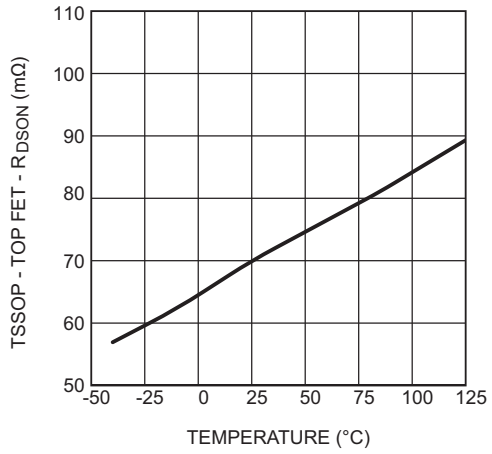


Figure 21.

R_{DSON} BOTTOM vs Temperature (TSSOP-20 Package)

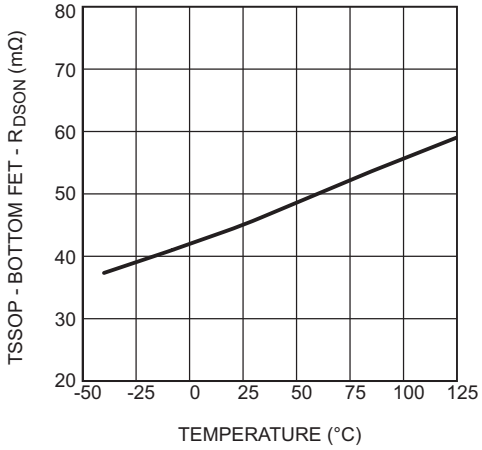


Figure 22.

I_Q (Quiescent Current Switching) - "X"

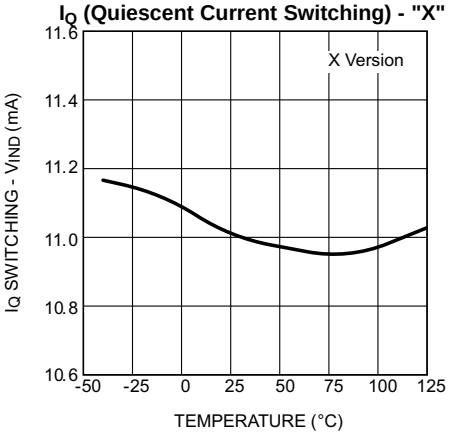


Figure 23.

I_Q (Quiescent Current Switching) - "Y"

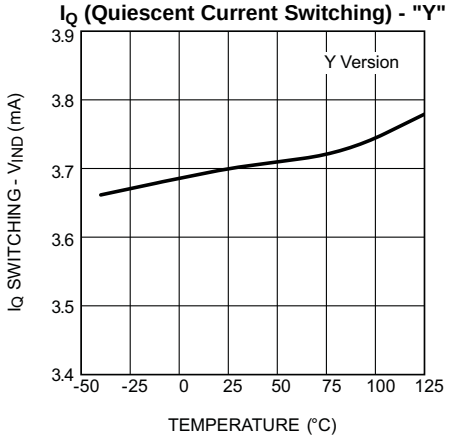


Figure 24.

Load Transient Response - X Version (V_{OUT} = 1.2V, 25-100% Load Transient)

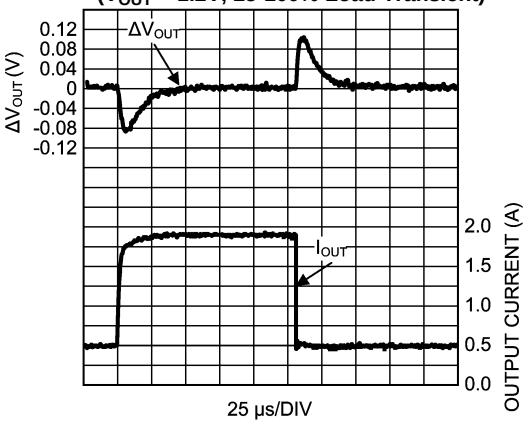


Figure 25.

Load Transient Response - Y Version (V_{OUT} = 1.2V, 25-100% Load Transient)

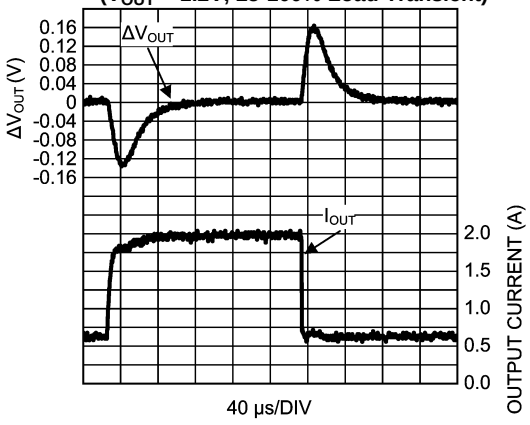


Figure 26.

Typical Performance Characteristics (continued)

All curves taken at V_{IN} = 5.0V with configuration in typical application circuit shown in Application Information section of this datasheet. T_J = 25°C, unless otherwise specified.

Start-Up (Soft-Start)
(V_{OUT} = 1.8V @ 1A, V_{IN} = 5V)

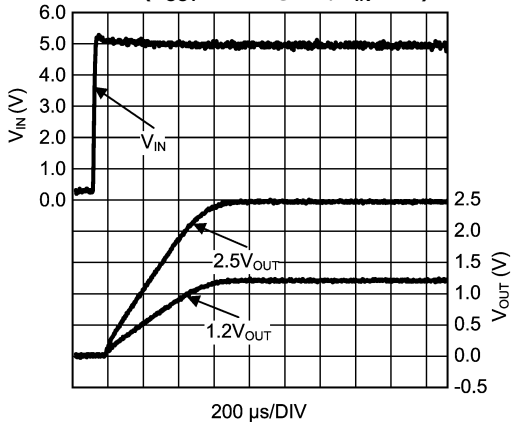


Figure 27.

Enable - Disable
(V_{OUT} = 1.8V @ 1A, V_{IN} = 5V)

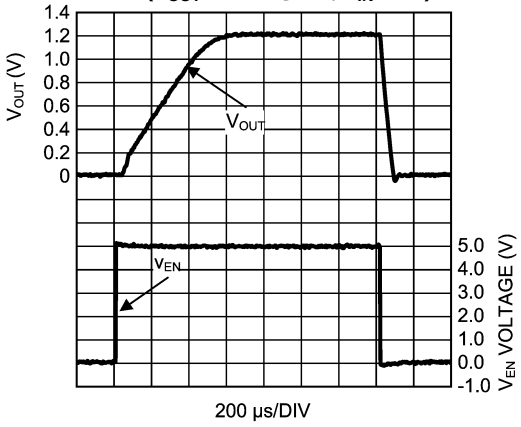


Figure 28.

V_{FB} vs Temperature

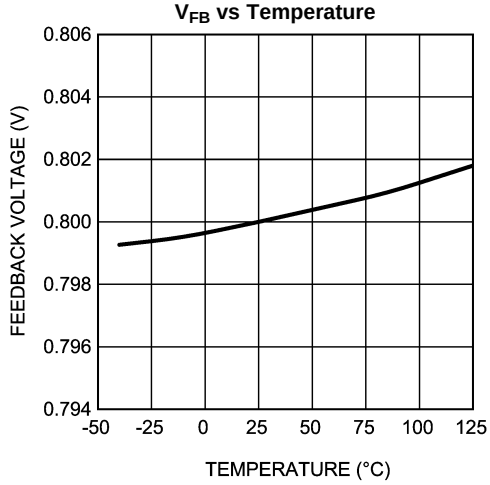


Figure 29.

Current Limit vs Temperature
(V_{IN} = 5V and 3.3V)

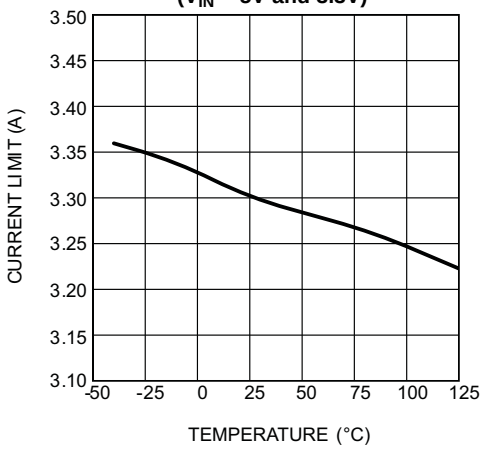


Figure 30.

Reverse Current Limit vs Temperature

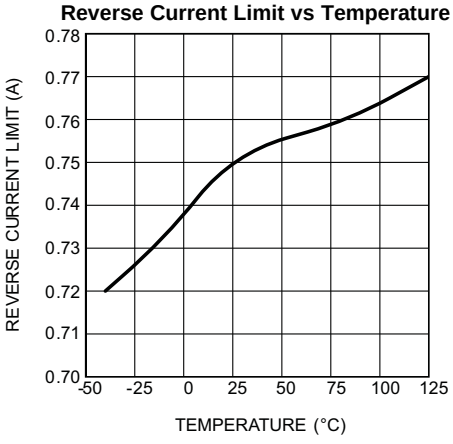


Figure 31.

Short Circuit Waveforms

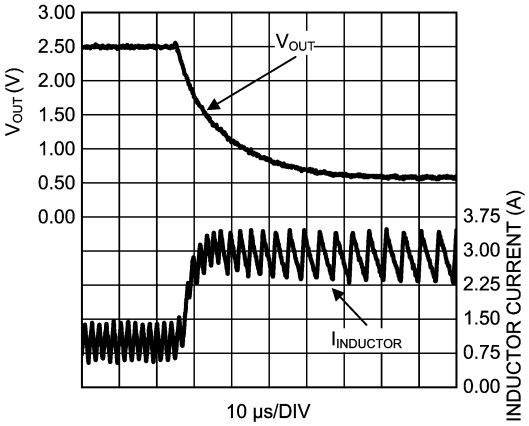
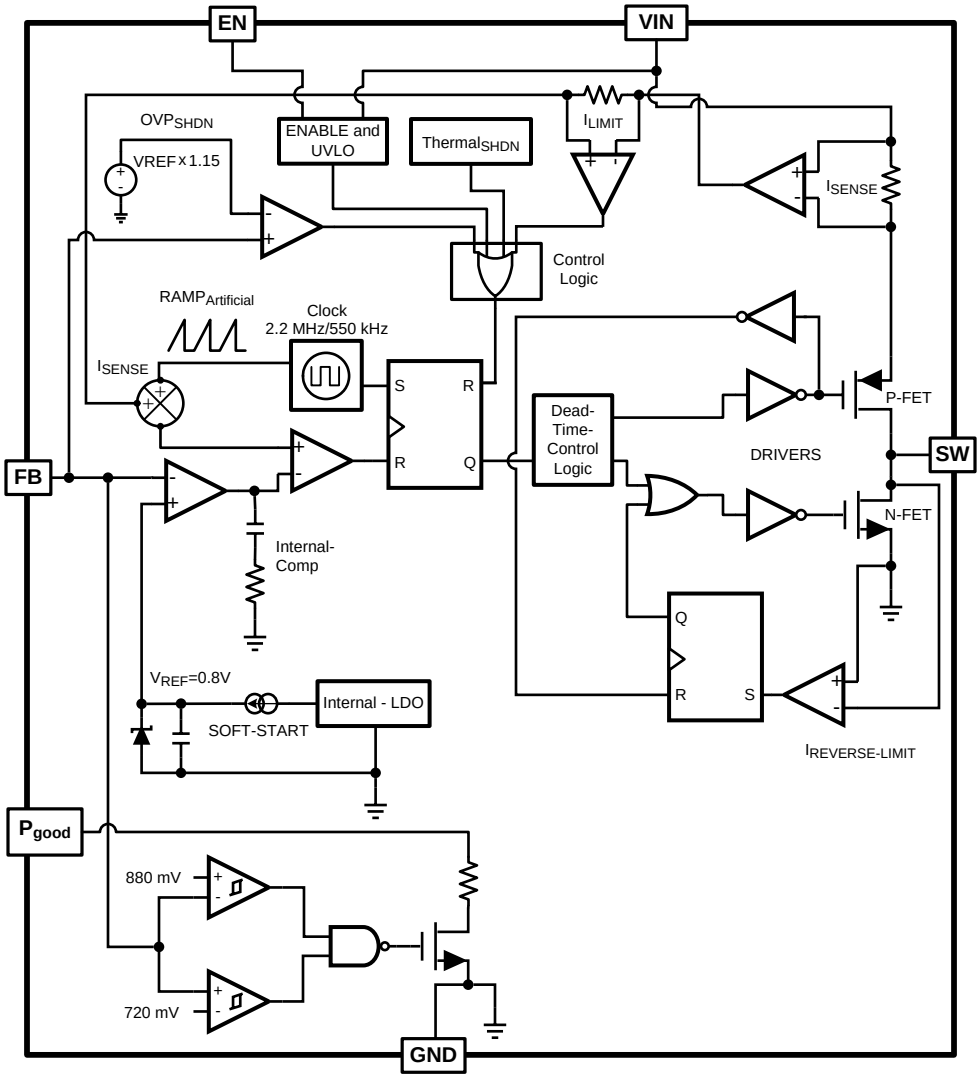


Figure 32.

Simplified Block Diagram Per Buck



APPLICATIONS INFORMATION

THEORY OF OPERATION

The LM26420 is a constant frequency dual PWM buck synchronous regulator IC that delivers two 2.0A load currents. The regulator has a preset switching frequency of 2.2MHz or 550kHz. This high frequency allows the LM26420 to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space. The LM26420 is internally compensated, so it is simple to use and requires few external components. The LM26420 uses current-mode control to regulate the output voltage. The following operating description of the LM26420 will refer to the Simplified Block Diagram, which depicts the functional blocks for one of the two channels, and to the waveforms in Figure 33. The LM26420 supplies a regulated output voltage by switching the internal PMOS and NMOS switches at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal clock. When this pulse goes low, the output control logic turns on the internal PMOS control switch (TOP Switch). During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the TOP Switch turns off and the NMOS switch (BOTTOM Switch) turns on after a short delay, which is controlled by the Dead-Time-Control Logic, until the next switching cycle begins. During the top switch off-time, inductor current discharges through the BOTTOM Switch, which forces the SW pin to swing to ground. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

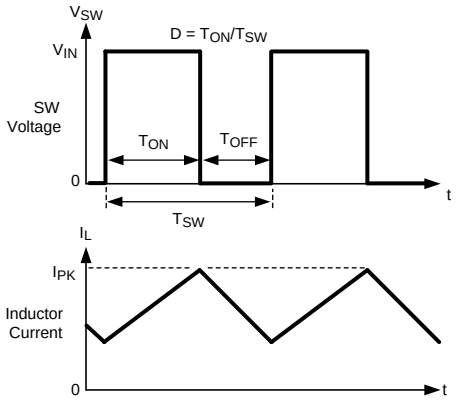


Figure 33. Typical Waveforms

SOFT-START

This function forces V_{OUT} to increase at a controlled rate during start up in a controlled fashion, which helps reduce inrush current and eliminate overshoot on V_{OUT}. During soft-start, the error amplifier's reference voltage ramps from 0V to its nominal value of 0.8V in approximately 600 µs. If the converter is turned on into a pre-biased condition then the feedback will begin ramping from the pre-bias voltage but at the same rate as if it had started from 0V. The two outputs startup ratiometrically if enabled at the same time, see Figure 34 below.

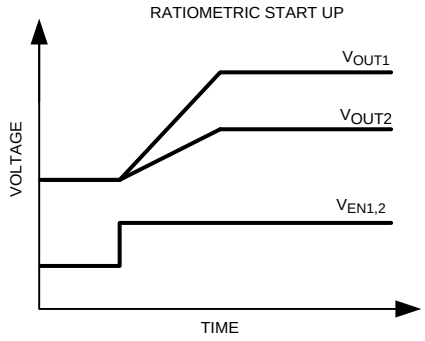


Figure 34.

OUTPUT OVER-VOLTAGE PROTECTION

The over-voltage comparator compares the FB pin voltage to a voltage that is approximately 15% higher than the internal reference V_{REF}. Once the FB pin voltage goes 15% above the internal reference, the internal PMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

UNDER-VOLTAGE LOCKOUT

Under-voltage lockout (UVLO) prevents the LM26420 from operating until the input voltage exceeds 2.628V (typ). The UVLO threshold has approximately 330 mV of hysteresis, so the part will operate until V_{IN} drops below 2.3V (typ). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

CURRENT LIMIT

The LM26420 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 3.3A (typ), and turns off the switch until the next switching cycle begins.

THERMAL SHUTDOWN

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 150°C.

POWER GOOD

The LM26420 features an open drain power good (PG) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull PG high when the output is within the PG tolerance window. Typical values for this resistor range from 10 kΩ to 100 kΩ.

PRECISION ENABLE

The LM26420 features independent precision enables that allow the converter to be controlled by an external signal. This feature allows the device to be sequenced either by a external control signal or the output of another converter in conjunction with a resistor divider network. It can also be set to turn on at a specific input voltage when used in conjunction with a resistor divider network connected to the input voltage. The device is enabled when the EN pin exceeds 1.04V and has a 150mV hysteresis.

Design Guide

INDUCTOR SELECTION

The Duty Cycle (D) can be approximated quickly using the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

The voltage drop across the internal NMOS (SW_BOT) and PMOS (SW_TOP) must be included to calculate a more accurate duty cycle. Calculate D by using the following formulas:

$$D = \frac{V_{OUT} + V_{SW\_BOT}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}} \quad (2)$$

V_{SW_TOP} and V_{SW_BOT} can be approximated by:

$$V_{SW\_TOP} = I_{OUT} \times R_{DSON\_TOP} \quad (3)$$

$$V_{SW\_BOT} = I_{OUT} \times R_{DSON\_BOT} \quad (4)$$

The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value will decrease the output ripple current.

One must ensure that the minimum current limit (2.4A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L \quad (5)$$

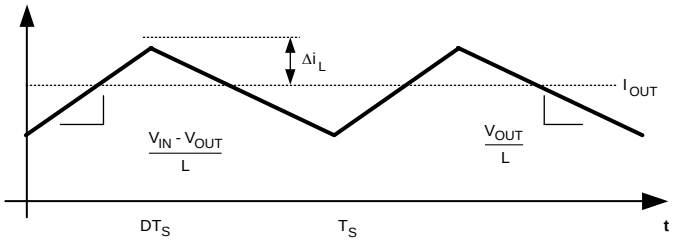


Figure 35. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S} \quad (6)$$

In general,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT}) \quad (7)$$

If Δi_L = 20% of 2A, the peak current in the inductor will be 2.4A. The minimum ensured current limit over all operating conditions is 2.4A. One can either reduce Δi_L, or make the engineering judgment that zero margin will be safe enough. The typical current limit is 3.3A.

The LM26420 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the output capacitor section for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by:

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times (V_{IN} - V_{OUT}) \quad (8)$$

Where

$$T_S = \frac{1}{f_S} \quad (9)$$

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation will result in a sudden reduction in inductance and prevent the regulator from operating correctly. The peak current of the inductor is used to specify the maximum output current of the inductor and saturation is not a concern due to the exceptionally small delay of the internal current limit signal. For example, if the designed maximum output current is 2.0A and the peak current is 2.3A, then the inductor should be specified

with a saturation current limit of > 2.3A. There is no need to specify the saturation or peak current of the inductor at the 3.25A typical switch current limit. The difference in inductor size is a factor of 5. Ferrite based inductors are preferred to minimize core losses when opperating with the frequencies used by the LM26420. This presents little restriction since the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (R_{DCR}) will provide better operating efficiency. For recommended inductors see Example Circuits.

INPUT CAPACITOR SELECTION

The input capacitors provide the AC current needed by the nearby power switch so that current provided by the upstream power supply does not carry a lot of AC content, generating less EMI. To the buck regulator in question, the input capacitor also prevents the drain voltage of the FET switch from dipping when the FET is turned on, therefore providing a healthy line rail for the LM26420 to work with. Since typically most of the AC current is provided by the local input capacitors, the power loss in those capacitors can be a concern. In the case of the LM26420 regulator, since the two channels operate 180° out of phase, the AC stress in the input capacitors is less than if they operated in phase. The measure for the AC stress is called input ripple RMS current. It is strongly recommended that at least one 10µF ceramic capacitor be placed next to each of the VIND pins. Bulk capacitors such as electrolytic capacitors or OSCON capacitors can be added to help stabilize the local line voltage, especially during large load transient events. As for the ceramic capacitors, use X7R or X5R types. They maintain most of their capacitance over a wide temperature range. Try to avoid sizes smaller than 0805. Otherwise significant drop in capacitance may be caused by the DC bias voltage. See OUTPUT CAPACITOR SELECTION section for more information. The DC voltage rating of the ceramic capacitor should be higher than the highest input voltage.

Capacitor temperature is a major concern in board designs. While using a 10µF or higher MLCC as the input capacitor is a good starting point, it is a good idea to check the temperature in the real thermal environment to make sure the capacitors are not over heated. Capacitor vendors may provide curves of ripple RMS current vs. temperature rise, based on a designated thermal impedance. In reality, the thermal impedance may be very different. So it is always a good idea to check the capacitor temperature on the board.

Since the duty cycles of the two channels may overlap, calculation of the input ripple RMS current is a little tedious. Use the following equation.

$$I_{irrms} = \sqrt{(I_1 - I_{av})^2 d1 + (I_2 - I_{av})^2 d2 + (I_1 + I_2 - I_{av})^2 d3} \quad (10)$$

I_1 is Channel 1's maximum output current. I_2 is Channel 2's maximum output current. d1 is the non-overlapping portion of Channel 1's duty cycle D_1. d2 is the non-overlapping portion of Channel 2's duty cycle D_2. d3 is the overlapping portion of the two duty cycles. I_{av} is the average input current. $I_{av} = I_1 \cdot D_1 + I_2 \cdot D_2$. To quickly determine the values of d1, d2 and d3, refer to the decision tree in Figure 36. To determine the duty cycle of each channel, use $D = V_{OUT}/V_{IN}$ for a quick result or use the following equation for a more accurate result.

$$D = \frac{V_{OUT} + V_{SW\_BOT} + I_{OUT} \times R_{DC}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}} \quad (11)$$

R_{DC} is the winding resistance of the inductor. R_{DS} is the ON resistance of the MOSFET switch.

Example:

V_{IN} = 5V, V_{OUT1} = 3.3V, I_{OUT1} = 2A, V_{OUT2} = 1.2V, I_{OUT2} = 1.5A, R_{DS} = 170mΩ, R_{DC} = 30mΩ. (I_{OUT1} is the same as I_1 in the input ripple RMS current equation, I_{OUT2} is the same as I_2).

First, find out the duty cycles. Plug the numbers into the duty cycle equation and we get D1 = 0.75, and D2 = 0.33. Next, follow the decision tree in Figure 36 to find out the values of d1, d2 and d3. In this case, d1 = 0.5, d2 = D2 + 0.5 - D1 = 0.08, and d3 = D1 - 0.5 = 0.25. $I_{av} = I_{OUT1} \cdot D1 + I_{OUT2} \cdot D2$ = 1.995A. Plug all the numbers into the input ripple RMS current equation and the result is I_{irrms} = 0.77A.

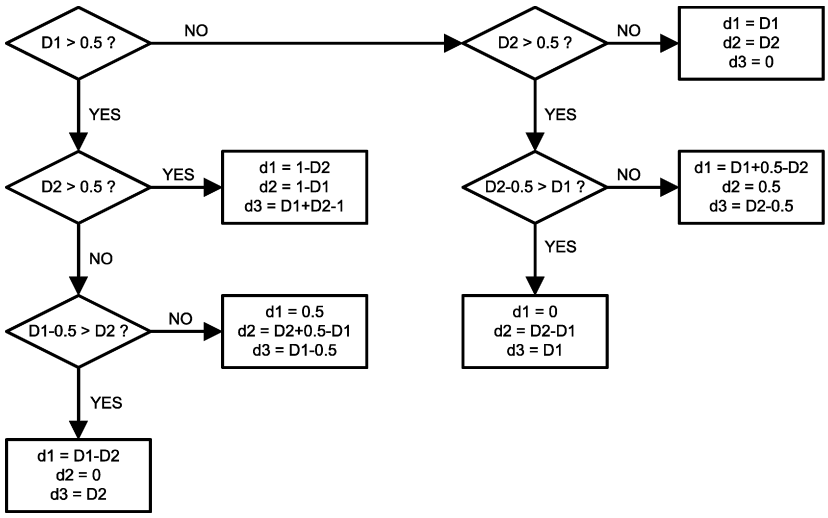


Figure 36. Determining d1, d2 and d3

OUTPUT CAPACITOR

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}} \right) \quad (12)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple will be approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM26420, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise will couple through parasitic capacitances in the inductor to the output. A ceramic capacitor will bypass this noise while a tantalum will not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications will require a minimum of 22 µF of output capacitance. Capacitance often, but not always, can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types.

PROGRAMMING OUTPUT VOLTAGE

The output voltage is set using the following equation where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good value for R2 is 10kΩ. When designing a unity gain converter (V_{OUT} = 0.8V), R1 should be between 0Ω and 100Ω, and R2 should be on the order of 5kΩ to 50kΩ, 10kΩ is the suggested value.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (13)$$

$$V_{REF} = 0.80V \quad (14)$$

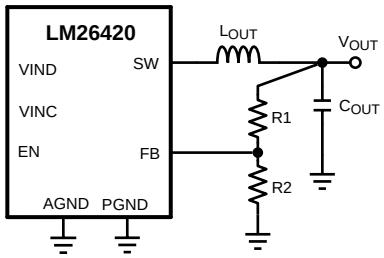


Figure 37. Programming V_{OUT}

To determine the maximum allowed resistor tolerance , use the following equation:

$$\sigma = \left(\frac{1}{1 + 2x \frac{1 - \frac{V_{FB}}{V_{OUT}}}{TOL - \phi}} \right) \quad (15)$$

where TOL is the set point accuracy of the regulator, Φ is the tolerance of V_{FB}.

Example:

VOUT = 2.5V, with a set point accuracy of +/- 3.5%.

$$\sigma = \left(\frac{1}{1 + 2x \frac{1 - \frac{0.8V}{2.5V}}{3.5\% - 1.5\%}} \right) = 1.4\% \quad (16)$$

Choose 1% resistors. If R2 = 10kΩ, then R1 is 21.25kΩ.

VINC FILTERING COMPONENTS

Additional filtering is required between VINC and AGND in order to prevent high frequency noise on VIN from disturbing the sensitive circuitry connected to VINC. A small RC filter can be used on the VINC pin as shown in Figure 38.

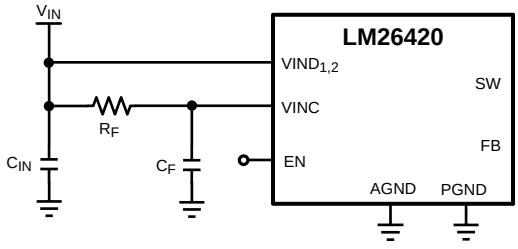


Figure 38. RC filter on VINC

In general, R_F is typically between 1Ω and 10Ω so that the steady state voltage drop across the resistor due to the VINC bias current does not affect the UVLO level. C_F can range from 0.22 µF to 1.0 µF in X7R or X5R dielectric, where the RC time constant should be at least 2 µS. C_F should be placed as close as possible to IC with a direct connection from VINC and AGND.

USING PRECISION ENABLE AND POWER GOOD

The LM26420's precision enable and power good pins address many of the sequencing requirements required in today's challenging applications. Each output can be controlled independently and have independent power goods. This allows for a multitude of ways to control each output. Typically, the enables to each output are tied together to the input voltage and the outputs will ratiometrically ramp up when the input voltage reaches above UVLO rising threshold. There may be instances where it is desired that the second output (V_{OUT2}) does not turn on until the first output (V_{OUT1}) has reached 90% of the desired set-point. This achieved easily with an external resistor divider attached from V_{OUT1} to EN_2, see Figure 39.

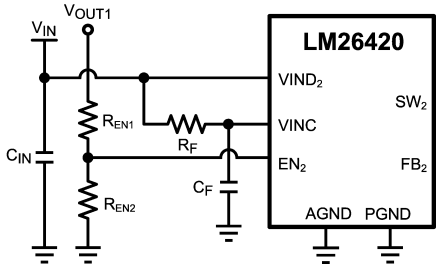


Figure 39. V_{OUT1} controlling V_{OUT2} with resistor divider.

If it is not desired to have a resistor divider to control V_{OUT2} with V_{OUT1}, then the PG_1 can be connected to the EN_2 pin to control V_{OUT2}, see Figure 40. R_{PG1} is a pull up resistor on the range of 10kΩ to 100kΩ, 50kΩ is the suggested value. This will turn on V_{OUT2} when V_{OUT1} is approximately 90% of the programmed output. NOTE, this will also turn off V_{OUT2} when V_{OUT1} is outside the +/-10% of the programmed output.

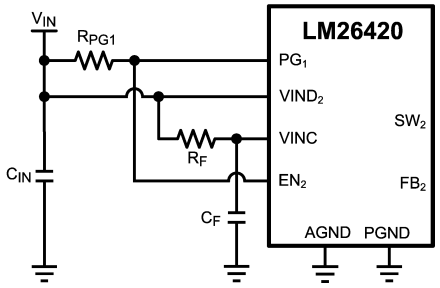


Figure 40. PG_1 controlling V_{OUT2}.

Another example might be that the output is not to be turned on until the input voltage reaches 90% of desired voltage set-point. This verifies that the input supply is stable before turning on the output. Select R_{EN1} and R_{EN2} such that the the voltage at the EN pin is greater than 1.12V when reaching the 90% desired set-point.

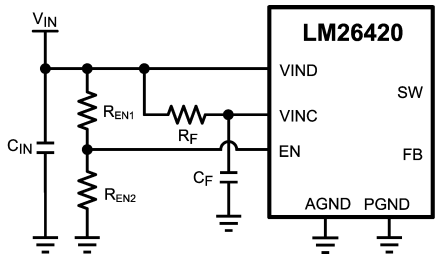


Figure 41. V_{IN} controlling V_{OUT}

The LM26420's power good feature is design with hysterysis in order to insure no false power good flags are asserted during large transient. Once power good is asserted high, it will not be pulled low until the output voltage exceeds +/-14% of the setpoint for a during of ~7.5µS (typ.), see Figure 42.

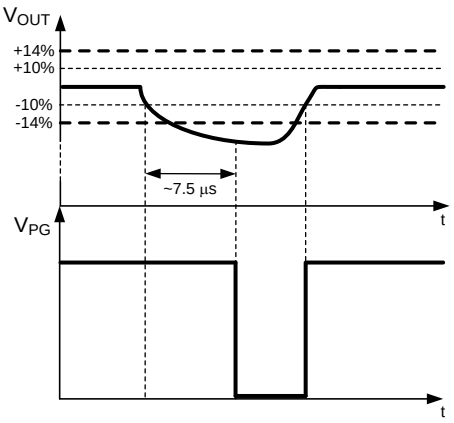


Figure 42. Power Good Hysterysis Operation

OVER-CURRENT PROTECTION

When the switch current reaches the current limit value, it immediately is turned off. This effectively reduces the duty cycle and therefore the output voltage dips and continues to droop until the output load matches the peak current limit inductor current. As the FB voltage drops below 480mV the operating frequency begins to decrease until it hits full on frequency fold-back which is set to approximately 150kHz for the Y version and 300kHz for the X version. Frequency fold back helps reduce the thermal stress in the IC by reducing the switching losses and to prevent runaway of the inductor current when the output is shorted to ground.

It is important to note that when recovering from a over-current condition the converter does not go through the soft-start process. There may be an over shoot due to the sudden removal of the over-current fault. The reference voltage at the non-inverting input of the error amplifier always sits at 0.8V during the over-current condition, therefore when the fault is removed the converter bring the FB voltage back to 0.8V as quickly as possible. The over-shoot depend on whether there is a load on the output after the removal of the over-current fault, the size of the inductor, and the amount of capacitance on the output. The smaller the inductor and the larger the capacitance on the output the smaller the overshoot. Note, over-current protection for each output is independent.

PCB LAYOUT CONSIDERATIONS

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor and the PGND pin. These ground ends should be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the IC as possible. Next in importance is the location of the GND connection of the output capacitor, which should be near the GND connections of VIND and PGND. There should be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high impedance node and care should be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors should be placed as close as possible to the IC, with the GND of R1 placed as close as possible to the GND of the IC. The V_{OUT} trace to R2 should be routed away from the inductor and any other traces that are switching. High AC currents flow through the V_{IN}, SW and V_{OUT} traces, so they should be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components should also be placed as close as possible to the IC. Please see Application Note AN-1229 SNVA054 for further considerations and the LM26420 demo board as an example of a four-layer layout.

Calculating Efficiency, and Junction Temperature

The complete LM26420 DC/DC converter efficiency can be calculated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}} \tag{17}$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (18)$$

Calculations for determining the most significant power losses are shown below. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter: switching and conduction. Conduction losses usually dominate at higher output loads, whereas switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_{SW\_BOT}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}} \quad (19)$$

V_{SW_TOP} is the voltage drop across the internal PFET when it is on, and is equal to:

$$V_{SW\_TOP} = I_{OUT} \times R_{DSON\_TOP} \quad (20)$$

V_{SW_BOT} is the voltage drop across the internal NFET when it is on, and is equal to:

$$V_{SW\_BOT} = I_{OUT} \times R_{DSON\_BOT} \quad (21)$$

If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_{SW\_BOT} + V_{DCR}}{V_{IN} + V_{SW\_BOT} + V_{DCR} - V_{SW\_TOP}} \quad (22)$$

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (23)$$

The LM26420 conduction loss is mainly associated with the two internal FETs:

$$P_{COND\_TOP} = (I_{OUT}^2 \times D)\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON\_TOP}$$

$$P_{COND\_BOT} = (I_{OUT}^2 \times (1\text{-}D))\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON\_BOT} \quad (24)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND\_TOP} = (I_{OUT}^2 \times R_{DSON\_TOP} \times D) \quad (25)$$

$$P_{COND\_BOT} = (I_{OUT}^2 \times R_{DSON\_BOT} \times (1\text{-}D)) \quad (26)$$

$$P_{COND} = P_{COND\_TOP} + P_{COND\_BOT} \quad (27)$$

Switching losses are also associated with the internal FETs. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE}) \quad (28)$$

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL}) \quad (29)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (30)$$

(31)

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (32)$$

I_Q is the quiescent operating current, and is typically around 8.4mA (I_{QVINC} = 4.7mA + I_{QVIND}=3.7mA) for the 550 kHz frequency option.

Due to Dead-Time-Control Logic in the converter, there is a small delay (~4nS) between the turn ON and OFF of the TOP and BOTTOM FET. During this time, the body diode of the BOTTOM FET is conducting with a voltage drop of V_{BDIODE} (~.65V). This allows the inductor current to circulate to the output, until the BOTTOM FET is turned ON and the inductor current passes through the FET. There is a small amount of power loss due to this body diode conducting and it can be calculated as follows:

$$P_{BDIODE} = 2x(V_{BDIODE} \times I_{OUT} \times F_{SW} \times T_{BDIODE}) \quad (33)$$

Typical Application power losses are:

$$P_{LOSS} = \Sigma P_{COND} + P_{SW} + P_{BDIODE} + P_{IND} + P_Q \quad (34)$$

$$P_{INTERNAL} = \Sigma P_{COND} + P_{SW} + P_{BDIODE} + P_Q \quad (35)$$

Table 1. Power Loss Tabulation

V_{IN}	5.0V	V_{OUT}	1.2V
I_{OUT}	2.0A	P_{OUT}	2.4W
F_{SW}	550kHz		
V_{BDIODE}	0.65V	P_{BDIODE}	5.7mW
I_Q	8.4mA	P_Q	42mW
T_{RISE}	1.5nS	P_{SWR}	4.1mW
T_{FALL}	1.5nS	P_{SWF}	4.1mW
R_{DSON_TOP}	75mΩ	P_{COND_TOP}	81mW
R_{DSON_BOT}	55mΩ	P_{COND_BOT}	167mW
IND_{DCR}	20mΩ	P_{IND}	80mW
D	0.262	P_{LOSS}	384mW
η	86.2%	$P_{INTERNAL}$	304mW

These calculations assume a junction temperature of 25°C. The R_{DSON} values will be larger due to internal heating and therefore the internal power loss ($P_{INTERNAL}$) must be first calculated to estimate the rise in junction temperature.

Thermal Definitions

T_J = Chip junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from chip junction to device case

$R_{\theta JA}$ = Thermal resistance from chip junction to ambient air

Heat in the LM26420 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs. conductor).

Heat Transfer goes as:

Silicon → package → lead frame → PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{\text{Power}} \quad (36)$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{INTERNAL}} \quad (37)$$

The PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB can greatly effect $R_{\theta JA}$. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Five to eight thermal vias should be placed under the exposed pad to the ground plane if the WQFN package is used. Up to 12 thermal vias should be used in the TSSOP-20 package for optimum heat transfer from the device to the ground plane.

Thermal impedance also depends on the thermal properties of the application's operating conditions (V_{IN}, V_{OUT}, I_{OUT} etc), and the surrounding circuitry.

Method 1: Silicon Junction Temperature Determination

To accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to top case temperature.

Some clarification needs to be made before we go any further.

$R_{\theta JC}$ is the thermal impedance from all six sides of an IC package to silicon junction.

$R_{\Phi JC}$ is the thermal impedance from top case to the silicon junction.

In this data sheet we will use $R_{\Phi JC}$ so that it allows the user to measure top case temperature with a small thermocouple attached to the top case.

$R_{\Phi JC}$ is approximately 20°C/Watt for the 16-pin WQFN package with the exposed pad. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench we have:

$$R_{\Phi JC} = \frac{T_J - T_C}{P_{INTERNAL}} \tag{38}$$

Therefore:

$$T_j = (R_{\Phi JC} \times P_{INTERNAL}) + T_C \tag{39}$$

From the previous example:

$$T_j = 20°C/W \times 0.304W + T_C \tag{40}$$

Method 2: Thermal Shutdown Temperature Determination

The second method, although more complicated, can give a very accurate silicon junction temperature.

The first step is to determine $R_{\theta JA}$ of the application. The LM26420 has over-temperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of about 15°C. Once the silicon temperature has decreased to approximately 150°C, the device will start to switch again. Knowing this, the $R_{\theta JA}$ for any application can be characterized during the early stages of the design one may calculate the $R_{\theta JA}$ by placing the PCB circuit into a thermal chamber. Raise the ambient temperature in the given working application until the circuit enters thermal shutdown. If the SW-pin is monitored, it will be obvious when the internal FETs stop switching, indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature, and the ambient temperature $R_{\theta JA}$ can be determined.

$$R_{\theta JA} = \frac{165° - T_A}{P_{INTERNAL}} \tag{41}$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

An example of calculating $R_{\theta JA}$ for an application using the LM26420 WQFN demonstration board is shown below.

The four layer PCB is constructed using FR4 with 1 oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by eight vias. The board measures 3.0cm x 3.0cm. It was placed in an oven with no forced airflow. The ambient temperature was raised to 152°C, and at that temperature, the device went into thermal shutdown.

From the previous example:

$$P_{INTERNAL} = 304mW \quad (42)$$

$$R_{\theta JA} = \frac{165^{o}C - 152^{o}C}{304\ mW} = 42.8^{o}\ C/W \quad (43)$$

If the junction temperature was to be kept below 125°C, then the ambient temperature could not go above 112°C.

$$T_j - (R_{\theta JA} \times P_{INTERNAL}) = T_A \quad (44)$$

$$125°C - (42.8°C/W \times 304mW) = 112.0°C \quad (45)$$

Layout Considerations

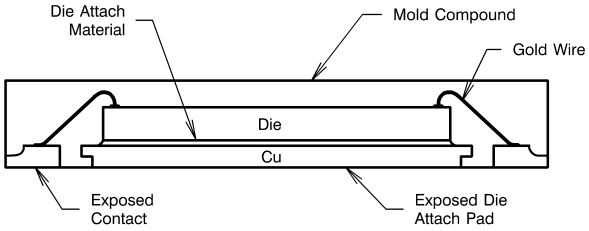


Figure 43. Internal Connection

For certain high power applications, the PCB land may be modified to a *dog bone* shape (see Figure 44). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

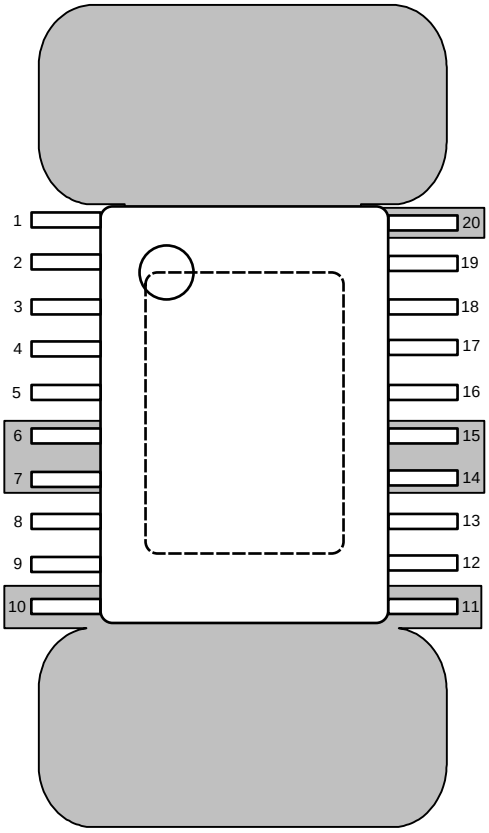


Figure 44. PCB Dog Bone Layout

LM26420X Design Example 1

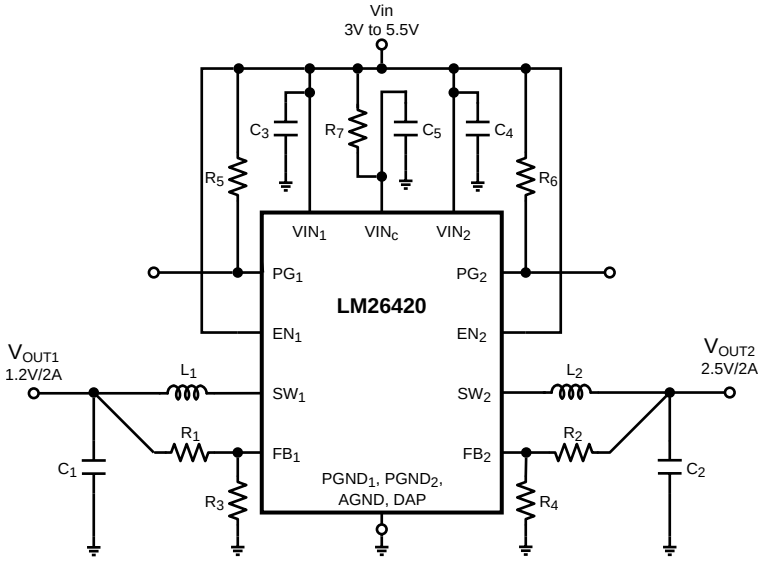


Figure 45. LM26420X (2.2MHz): V_{IN} = 5V, V_{OUT1} = 1.2V @ 2.0A and V_{OUT2} = 2.5V @ 2.0A

Table 2. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	TI	LM26420X
C3, C4	15µF, 6.3V, 1206, X5R	TDK	C3216X5R0J156M
C1	33µF, 6.3V, 1206, X5R	TDK	C3216X5R0J336M
C2	22µF, 6.3V, 1206, X5R	TDK	C3216X5R0J226M
C5	0.47µF, 10V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1	1.0µH, 7.9A	TDK	RLF7030T-1R0M6R4
L2	1.5µH, 6.5A	TDK	RLF7030T-1R5M6R1
R3, R4	10.0kΩ, 0603, 1%	Vishay	CRCW060310K0F
R1	4.99kΩ, 0603, 1%	Vishay	CRCW06034K99F
R5, R6	49.9kΩ, 0603, 1%	Vishay	CRCW060649K9F
R2	21.5kΩ, 0603, 1%	Vishay	CRCW060321K5F
R7	4.99Ω, 0603, 1%	Vishay	CRCW06034R99F

LM26420X Design Example 2

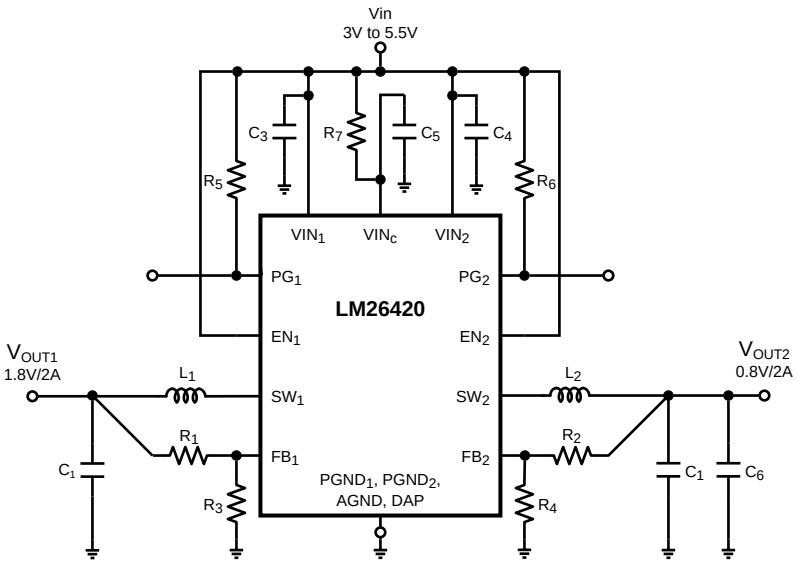


Figure 46. LM26420X (2.2MHz): V_{IN} = 5V, V_{OUT1} = 1.8V @ 2.0A and V_{OUT2} = 0.8V @ 2.0A

Table 3. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	TI	LM26420X
C3, C4	15µF, 6.3V, 1206, X5R	TDK	C3216X5R0J156M
C1	33µF, 6.3V, 1206, X5R	TDK	C3216X5R0J336M
C2, C6	22µF, 6.3V, 1206, X5R	TDK	C3216X5R0J226M
C5	0.47µF, 10V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1	1.0µH, 7.9A	TDK	RLF7030T-1R0M6R4
L2	0.7µH, 3.7A	Coilcraft	LPS4414-701ML
R3, R4	10.0kΩ, 0603, 1%	Vishay	CRCW060310K0F
R5, R6	49.9kΩ, 0603, 1%	Vishay	CRCW060649K9F
R1	12.7kΩ, 0603, 1%	Vishay	CRCW060312K7F
R7, R2	4.99Ω, 0603, 1%	Vishay	CRCW06034R99F

LM26420X Design Example 3

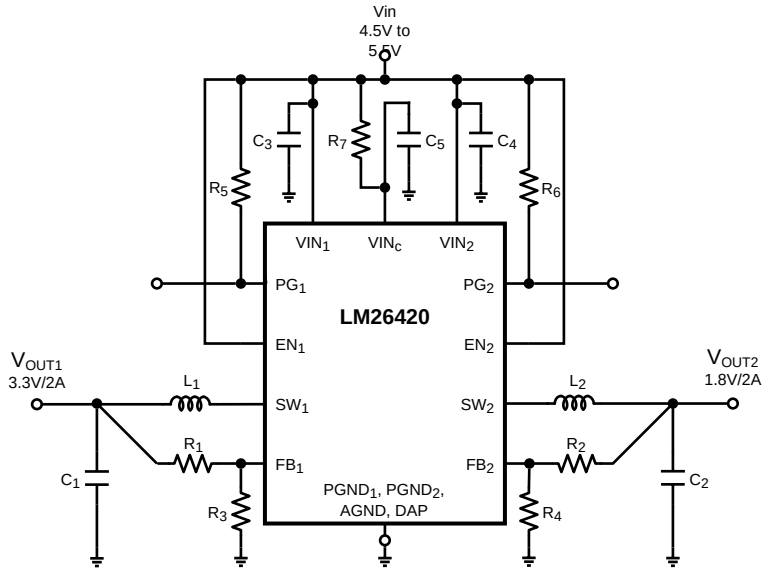


Figure 47. LM26420X (2.2MHz): V_{IN} = 5V, V_{OUT1} = 3.3V @ 2.0A and V_{OUT2} = 1.8V @ 2.0A

Table 4. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	TI	LM26420X
C3, C4	15µF, 6.3V, 1206, X5R	TDK	C3216X5R0J156M
C1	22µF, 6.3V, 1206, X5R	TDK	C3216X5R0J226M
C2	33µF, 6.3V, 1206, X5R	TDK	C3216X5R0J336M
C5	0.47µF, 10V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1, L2	1.0µH, 7.9A	TDK	RLF7030T-1R0M6R4
R3, R4	10.0kΩ, 0603, 1%	Vishay	CRCW060310K0F
R2	12.7kΩ, 0603, 1%	Vishay	CRCW060312K7F
R5, R6	49.9kΩ, 0603, 1%	Vishay	CRCW060649K9F
R1	31.6kΩ, 0603, 1%	Vishay	CRCW060331K6F
R7	4.99Ω, 0603, 1%	Vishay	CRCW06034R99F

LM26420Y Design Example 4

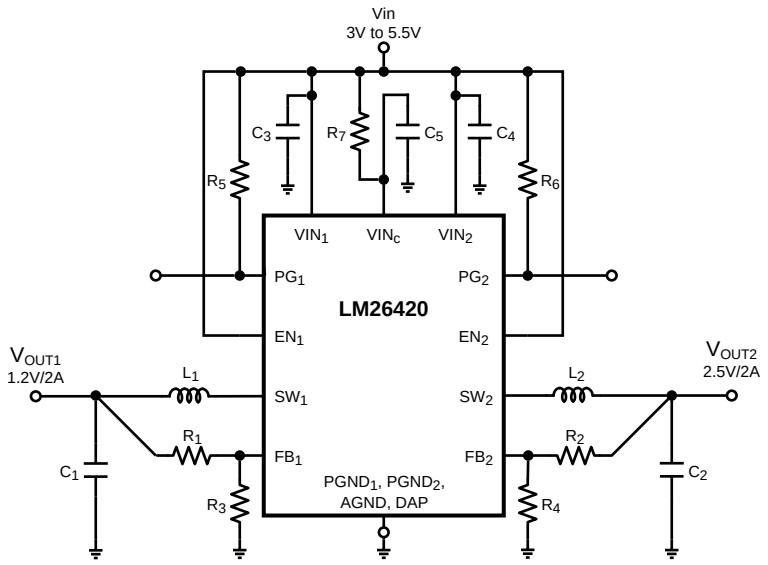


Figure 48. LM26420Y (550kHz): V_{IN} = 5V, V_{OUT1} = 1.2V @ 2.0A and V_{OUT2} = 2.5V @ 2.0A

Table 5. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	TI	LM26420Y
C3, C4	22µF, 6.3V, 1206, X5R	TDK	C3216X5R0J226M
C1, C6, C7	33µF, 6.3V, 1206, X5R	TDK	C3216X5R0J336M
C2	47µF, 6.3V, 1206, X5R	TDK	C3216X5R0J476M
C5	0.47µF, 10V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1	3.3µH, 3.28A	Coilcraft	MSS7341-332NL
L2	5.0µH, 2.82A	Coilcraft	MSS7341-502NL
R3, R4	10.0kΩ, 0603, 1%	Vishay	CRCW060310K0F
R1	4.99kΩ, 0603, 1%	Vishay	CRCW06034K99F
R5, R6	49.9kΩ, 0603, 1%	Vishay	CRCW060649K9F
R2	21.5kΩ, 0603, 1%	Vishay	CRCW060321K5F
R7	4.99Ω, 0603, 1%	Vishay	CRCW06034R99F

LM26420Y Design Example 5

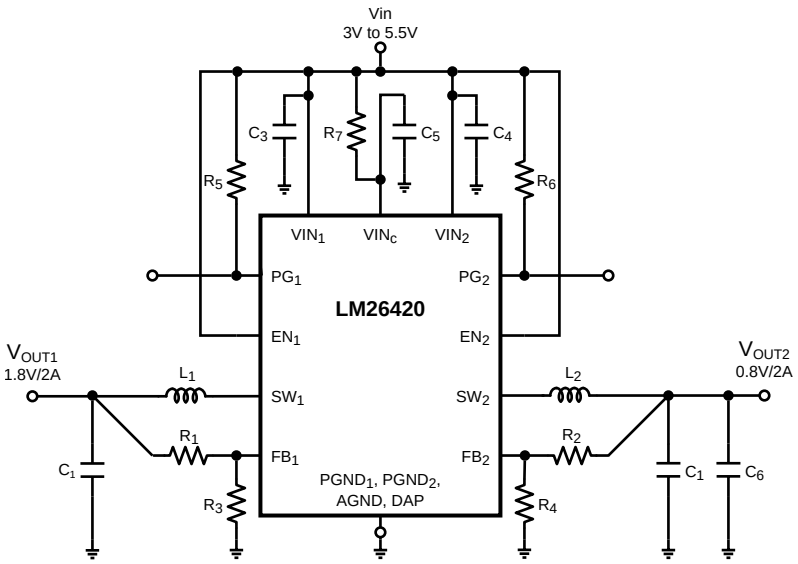


Figure 49. LM26420Y (550kHz): V_{IN} = 5V, V_{OUT1} = 1.8V @ 2.0A and V_{OUT2} = 0.8V @ 2.0A

Table 6. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	TI	LM26420Y
C3, C4	22µF, 6.3V, 1206, X5R	TDK	C3216X5R0J226M
C1, C2, C6, C7, C8	47µF, 6.3V, 1206, X5R	TDK	C3216X5R0J476M
C5	0.47µF, 10V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1	5.0µH, 2.82A	Coilcraft	MSS7341-502NL
L2	3.3µH, 3.28A	Coilcraft	MSS7341-332NL
R3, R4	10.0kΩ, 0603, 1%	Vishay	CRCW060310K0F
R5, R6	49.9kΩ, 0603, 1%	Vishay	CRCW060649K9F
R1	12.7kΩ, 0603, 1%	Vishay	CRCW060312K7F
R7, R2	4.99Ω, 0603, 1%	Vishay	CRCW06034R99F

LM26420Y Design Example 6

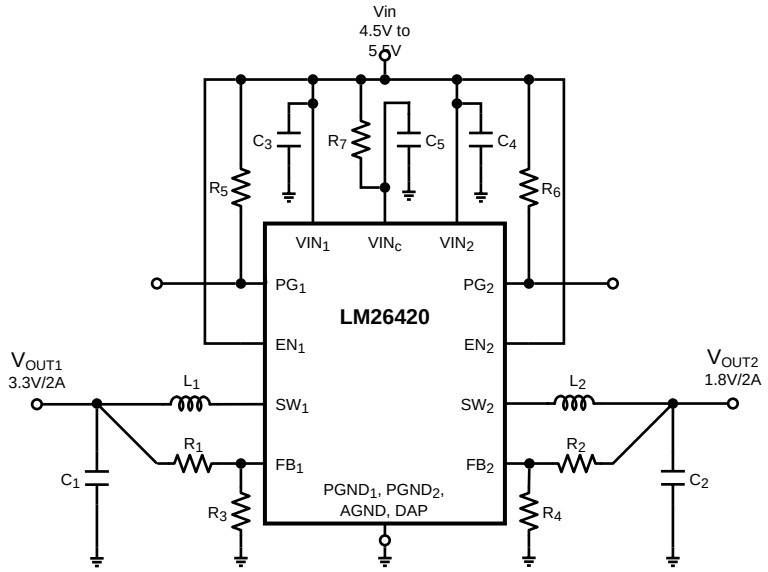


Figure 50. LM26420Y (550kHz): V_{IN} = 5V, V_{OUT1} = 3.3V @ 2.0A and V_{OUT2} = 1.8V @ 2.0A

Table 7. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2A Buck Regulator	TI	LM26420Y
C3, C4	22µF, 6.3V, 1206, X5R	TDK	C3216X5R0J226M
C1, C2, C6	47µF, 6.3V, 1206, X5R	TDK	C3216X5R0J476M
C5	0.47µF, 10V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1, L2	5.0µH, 2.82A	Coilcraft	MSS7341-502NL
R3, R4	10.0kΩ, 0603, 1%	Vishay	CRCW060310K0F
R2	12.7kΩ, 0603, 1%	Vishay	CRCW060312K7F
R5, R6	49.9kΩ, 0603, 1%	Vishay	CRCW060649K9F
R1	31.6kΩ, 0603, 1%	Vishay	CRCW060331K6F
R7	4.99Ω, 0603, 1%	Vishay	CRCW06034R99F

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM26420Q1XSQ/NOPB	ACTIVE	WQFN	RUM	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L26420Q	Samples
LM26420Q1XSQX/NOPB	ACTIVE	WQFN	RUM	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L26420Q	Samples
LM26420XMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM26420 XMH	Samples
LM26420XMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM26420 XMH	Samples
LM26420XSQ/NOPB	ACTIVE	WQFN	RUM	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L26420X	Samples
LM26420XSQX/NOPB	ACTIVE	WQFN	RUM	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L26420X	Samples
LM26420YMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM26420 YMH	Samples
LM26420YMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM26420 YMH	Samples
LM26420YSQ/NOPB	ACTIVE	WQFN	RUM	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L26420Y	Samples
LM26420YSQX/NOPB	ACTIVE	WQFN	RUM	16	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L26420Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF LM26420, LM26420-Q1 :

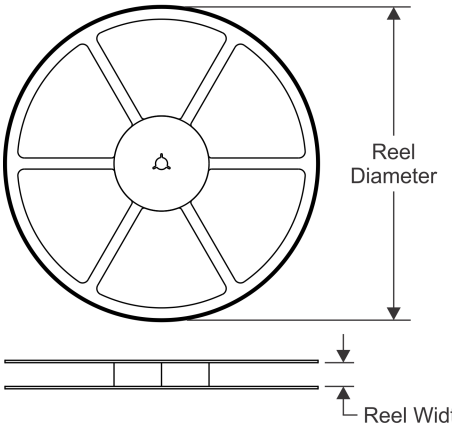
- Catalog: LM26420
- Automotive: LM26420-Q1

NOTE: Qualified Version Definitions:

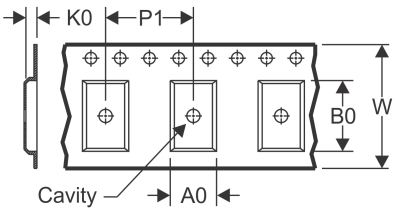
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

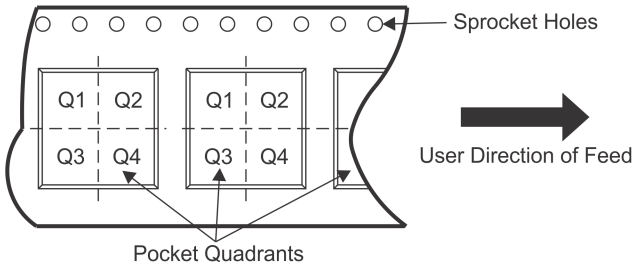


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

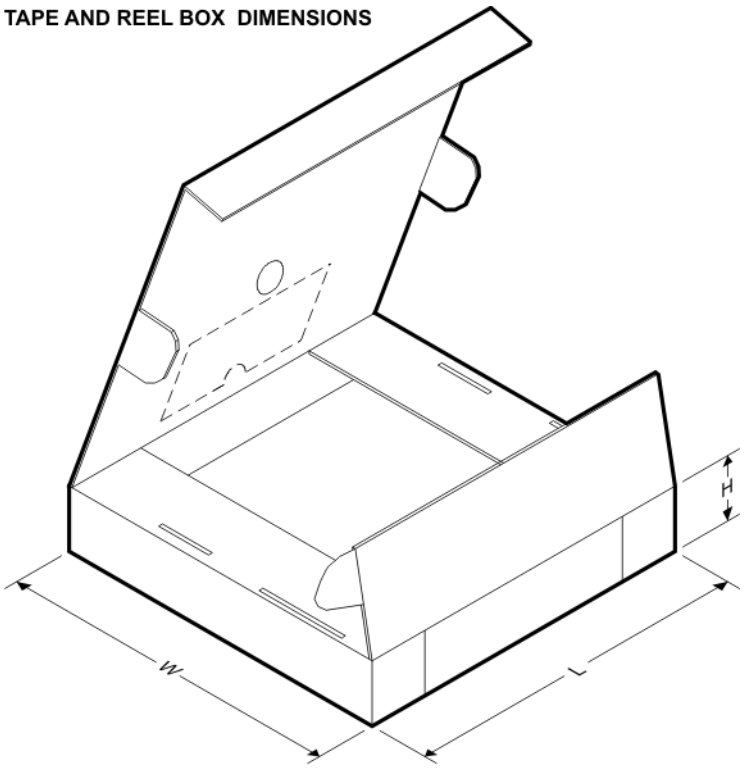
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26420Q1XSQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26420Q1XSQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26420XMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM26420XSQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26420XSQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26420YMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM26420YSQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26420YSQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

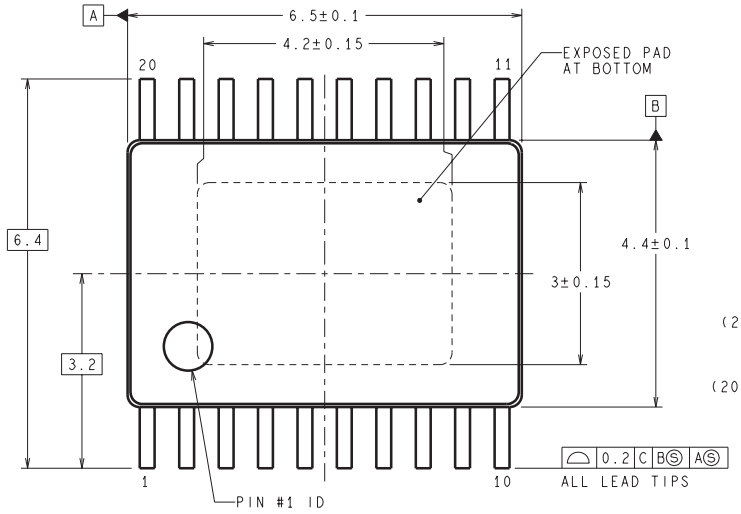
TAPE AND REEL BOX DIMENSIONS

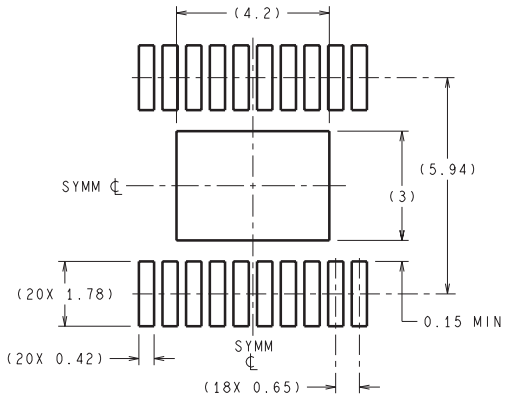


*All dimensions are nominal

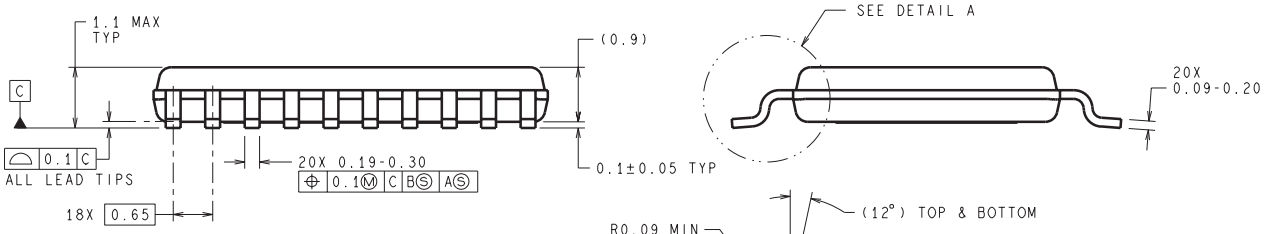
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26420Q1XSQ/NOPB	WQFN	RUM	16	1000	213.0	191.0	55.0
LM26420Q1XSQX/NOPB	WQFN	RUM	16	4500	367.0	367.0	35.0
LM26420XMHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM26420XSQ/NOPB	WQFN	RUM	16	1000	213.0	191.0	55.0
LM26420XSQX/NOPB	WQFN	RUM	16	4500	367.0	367.0	35.0
LM26420YMHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM26420YSQ/NOPB	WQFN	RUM	16	1000	213.0	191.0	55.0
LM26420YSQX/NOPB	WQFN	RUM	16	4500	367.0	367.0	35.0

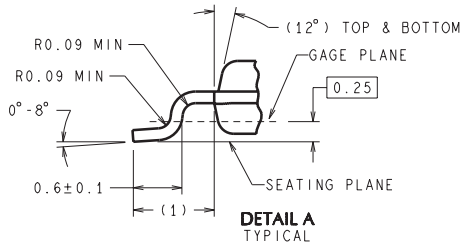
PWP0020A





RECOMMENDED LAND PATTERN



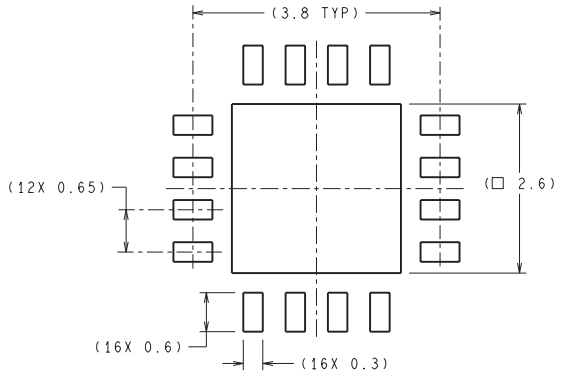


DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

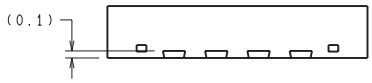
MXA20A (Rev C)

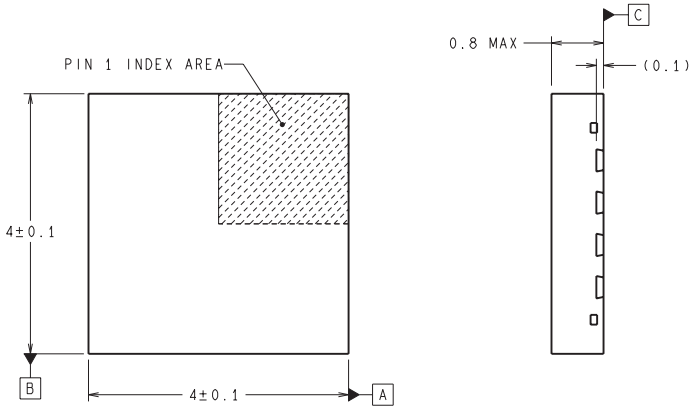
RUM0016A

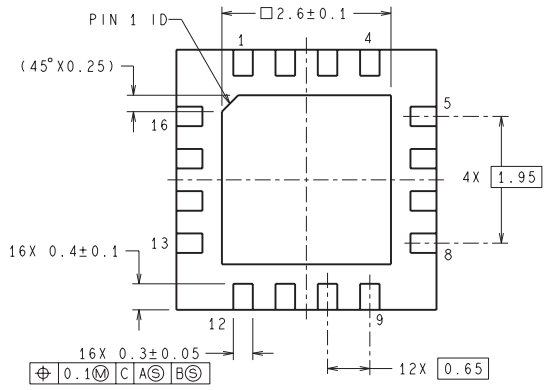


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY







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