LM22673/LM22673-Q1 42V, 3A SIMPLE SWITCHER®, Step-Down Voltage Regulator with Features

Check for Samples: LM22673

FEATURES

- **Wide Input Voltage Range: 4.5V to 42V**
- **Internally Compensated Voltage Mode Control**
- **Stable with Low ESR Ceramic Capacitors**
- **120 mΩ N-Channel MOSFET PFM Package**
- **100 mΩ N-Channel MOSFET SO PowerPAD Package**
- **Output Voltage Options:**
  - **ADJ (Outputs as Low as 1.285V)**
  - **5.0 (Output Fixed to 5V)**
- **±1.5% Feedback Reference Accuracy**
- **Switching Frequency of 500 kHz**
- **-40°C to 125°C Operating Junction Temperature Range**
- **Adjustable Soft-Start**
- **Adjustable Current Limit**
- **Integrated Boot-Strap Diode**
- **Fully Webench® Enabled**
- **LM22673-Q1 is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (-40°C to +125°C Junction Temperature)**

PACKAGE

- **SO PowerPAD (Exposed Pad)**
- **PFM (Exposed Pad)**

APPLICATIONS

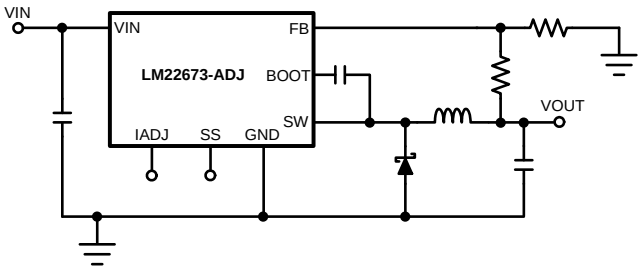
- **Industrial Control**
- **Telecom and Datacom Systems**
- **Embedded Systems**
- **Conversions from Standard 24V, 12V and 5V Input Rails**

DESCRIPTION

The LM22673 switching regulator provides all of the functions necessary to implement an efficient high voltage step-down (buck) regulator using a minimum of external components. This easy to use regulator incorporates a 42V N-channel MOSFET switch capable of providing up to 3A of load current. Excellent line and load regulation along with high efficiency (>90%) are featured. Voltage mode control offers short minimum on-time, allowing the widest ratio between input and output voltages. Internal loop compensation means that the user is free from the tedious task of calculating the loop compensation components. Fixed 5V output and adjustable output voltage options are available. A switching frequency of 500 kHz allows for small external components and good transient response. An adjustable soft-start feature is provided through the selection of a single external capacitor. In addition, the switch current limit can be programmed with a single external resistor, allowing solution optimization. The LM22673 also has built in thermal shutdown, and current limiting to protect against accidental overloads.

The LM22673 is a member of Texas Instruments' SIMPLE SWITCHER® family. The SIMPLE SWITCHER® concept provides for an easy to use complete design using a minimum number of external components and the TI WEBENCH® design tool. TI's WEBENCH® tool includes features such as external component calculation, electrical simulation, thermal simulation, and Build-It boards for easy design-in.

Simplified Application Schematic



Connection Diagram

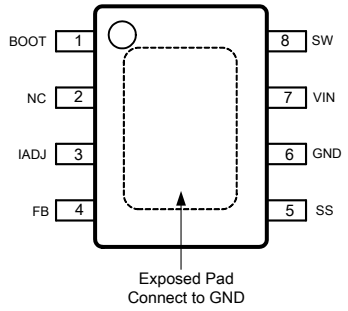


Figure 1. 8-Lead Plastic SO PowerPAD Package
Package Number DDA0008B

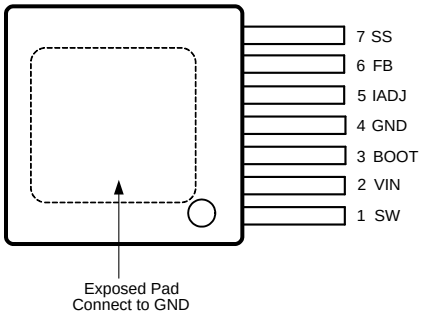


Figure 2. 7-Lead Plastic PFM Package
Package Number NDR0007A

PIN DESCRIPTIONS

Pin Numbers SO PowerPAD Package	Pin Numbers PFM Package	Name	Description	Application Information
1	3	BOOT	Bootstrap input	Provides the gate voltage for the high side NFET.
2	-	NC	Not Connected	Pin is not electrically connected inside the chip. Pin does function as thermal conductor.
3	5	IADJ	Current limit adjust input pin	A resistor attached between this pin and GND can be used to set the current limit threshold. Pin can be left floating and internal setting will be default.
4	6	FB	Feedback input	Feedback input to regulator.
5	7	SS	Soft-Start pin	Used to increase soft-start time. See Soft-Start section of data sheet.
6	4	GND	Ground input to regulator; system common	System ground pin.
7	2	VIN	Input voltage	Supply input to the regulator.
8	1	SW	Switch output	Switching output of regulator.
EP	EP	EP	Exposed Pad	Connect to ground. Provides thermal connection to PCB. See Application Information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VIN to GND		43V
SS, IADJ Pin Voltage		-0.5V to 7V
SW to GND[3]		-5V to V_{IN}
Boot Pin Voltage		V_{SW} + 7V
FB Pin Voltage		-0.5V to 7V
Power Dissipation		Internally Limited
Junction Temperature		150°C
For soldering specifications, refer to the following document: www.ti.com/lit/snoa549		
ESD Rating[4]	Human Body Model	±2 kV
Storage Temperature Range		-65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The absolute maximum specification of the 'SW to GND' applies to DC voltage. An extended negative voltage limit of -10V applies to a pulse of up to 50 ns.
(4) ESD was applied using the human body model, a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings[1]

Supply Voltage (V_{IN})	4.5V to 42V
Junction Temperature Range	-40°C to +125°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the recommended Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and should not be operated beyond such conditions.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_A = T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise specified: V_{IN} = 12V.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
LM22673-5.0						
V_{FB}	Feedback Voltage	V_{IN} = 8V to 42V	4.925/**4.9**	5.0	5.075/**5.1**	V
LM22673-ADJ						
V_{FB}	Feedback Voltage	V_{IN} = 4.7V to 42V	1.266/**1.259**	1.285	1.304/**1.311**	V
All Output Voltage Versions						
I_Q	Quiescent Current	V_{FB} = 5V		3.4	**6**	mA
V_{ADJ}	Current Limit Adjust Voltage		**0.65**	0.8	**0.9**	V
I_{CL}	Current Limit		3.4/**3.35**	4.2	5.3/**5.5**	A
$R_{DS(ON)}$	Switch On-Resistance	PFM Package		0.12	0.16/**0.22**	Ω
		SO PowerPAD Package		0.10	0.16/**0.20**	
f_O	Oscillator Frequency		**400**	500	**600**	kHz
T_{OFFMIN}	Minimum Off-time		**100**	200	**300**	ns
T_{ONMIN}	Minimum On-time			100		ns
I_{BIAS}	Feedback Bias Current	V_{FB} = 1.3V (ADJ Version Only)		230		nA
I_{SS}	Soft-start Current	EN Input = 0V	**30**	50	**70**	µA
T_{SD}	Thermal Shutdown Threshold			150		°C
θ_{JA}	Thermal Resistance	TJ package, junction to ambient thermal resistance(3)		22		°C/W
θ_{JA}	Thermal Resistance	MR Package, junction to ambient thermal resistance(4)		60		°C/W

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) Typical values represent most likely parametric norms at the conditions specified and are not ensured.
(3) The value of θ_{JA} for the PFM (TJ) package of 22°C/W is valid if package is mounted to 1 square inch of copper. The θ_{JA} value can range from 20 to 30°C/W depending on the amount of PCB copper dedicated to heat transfer. See application note AN-1797 (SNVA328) for more information.
(4) The value of θ_{JA} for the SO PowerPAD exposed pad (MR) package of 60°C/W is valid if package is mounted to 1 square inch of copper. The θ_{JA} value can range from 42 to 115°C/W depending on the amount of PCB copper dedicated to heat transfer.

Typical Performance Characteristics

Unless otherwise specified the following conditions apply: Vin = 12V, T_J = 25°C.

Efficiency vs I_{OUT} and V_{IN}
V_{OUT} = 3.3V

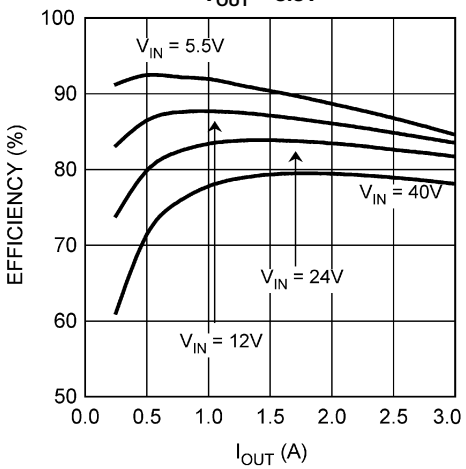


Figure 3.

Current Limit vs Temperature

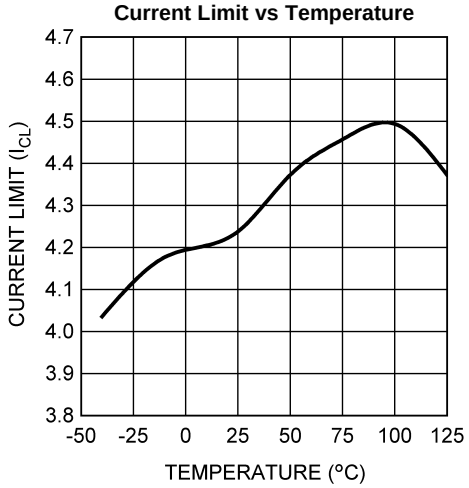


Figure 4.

Normalized Switching Frequency vs Temperature

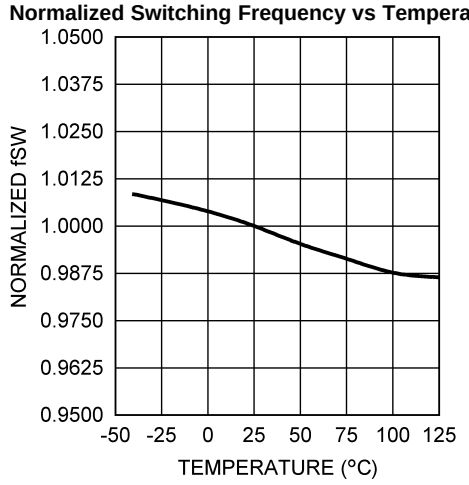


Figure 5.

Feedback Bias Current vs Temperature

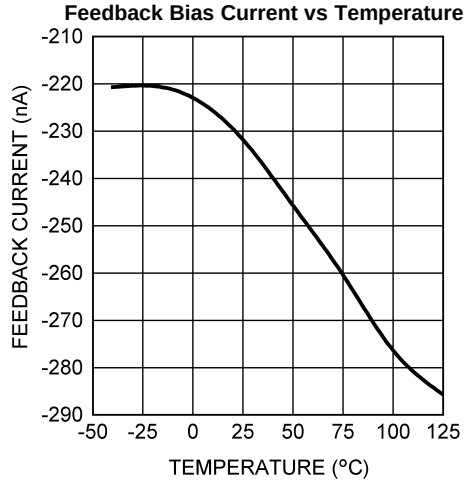


Figure 6.

Normalized Feedback Voltage vs Temperature

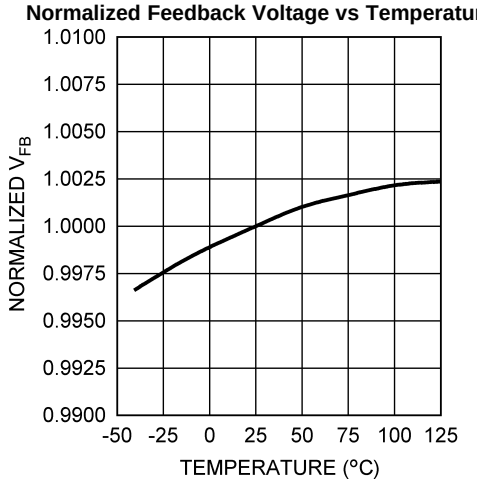


Figure 7.

Normalized $R_{DS(ON)}$ vs Temperature

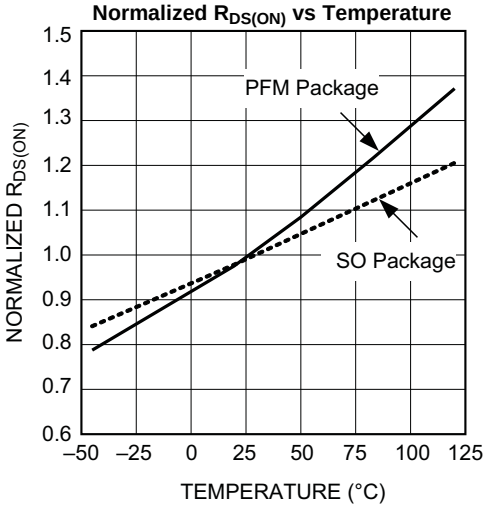


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply: Vin = 12V, T_J = 25°C.

Normalized Feedback Voltage vs Input Voltage

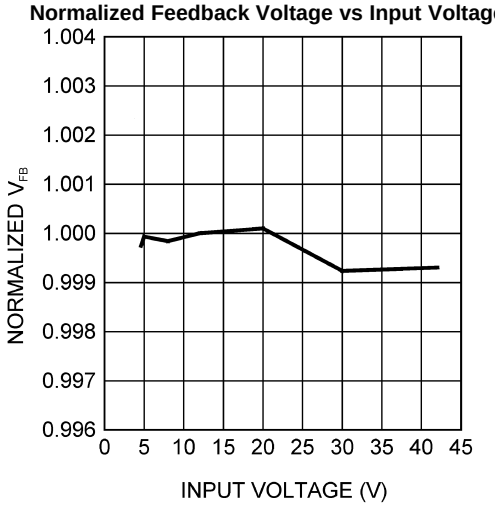


Figure 9.

Soft-start Current vs Temperature

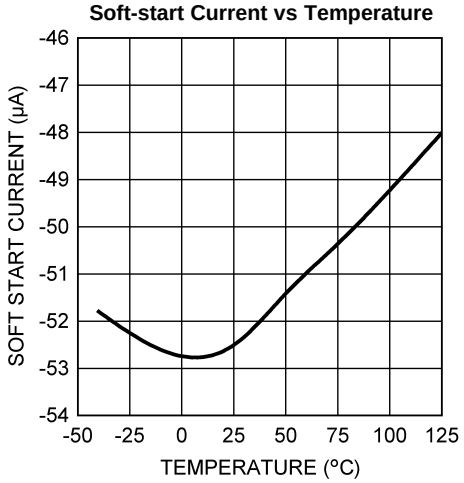


Figure 10.

Current Limit vs IADJ Resistor

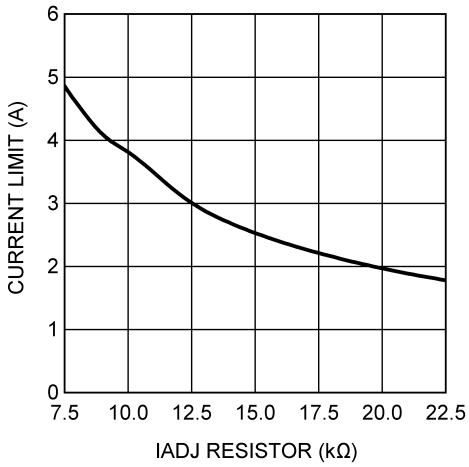


Figure 11.

SIMPLIFIED BLOCK DIAGRAM

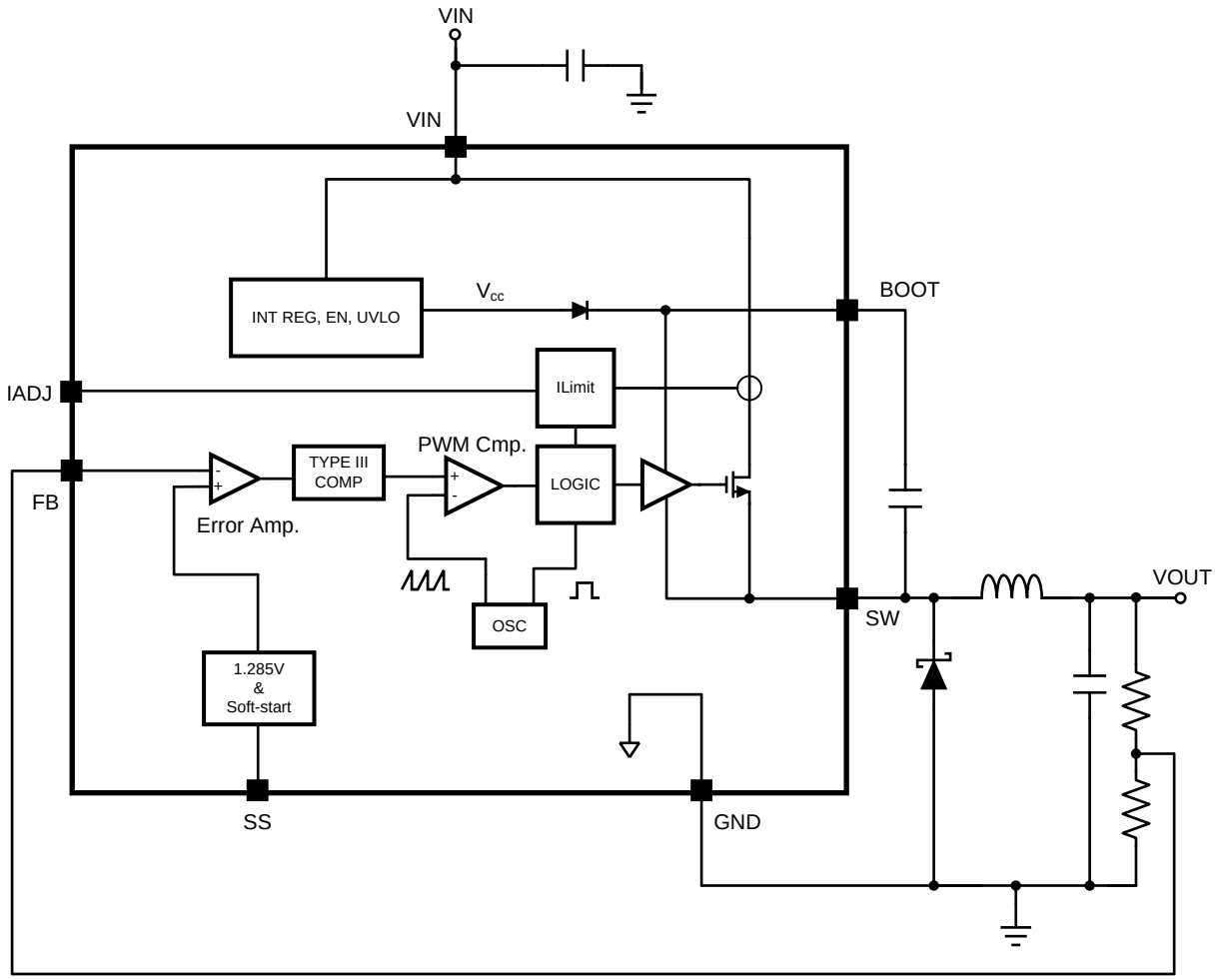


Figure 12. Simplified Block Diagram

Detailed Operating Description

The LM22673 incorporates a voltage mode constant frequency PWM architecture. In addition, input voltage feed-forward is used to stabilize the loop gain against variations in input voltage. This allows the loop compensation to be optimized for transient performance. The power MOSFET, in conjunction with the diode, produce a rectangular waveform at the switch pin, that swings from about zero volts to VIN. The inductor and output capacitor average this waveform to become the regulator output voltage. By adjusting the duty cycle of this waveform, the output voltage can be controlled. The error amplifier compares the output voltage with the internal reference and adjusts the duty cycle to regulate the output at the desired value.

The internal loop compensation of the -ADJ option is optimized for outputs of 5V and below. If an output voltage of 5V or greater is required, the -5.0 option can be used with an external voltage divider. The minimum output voltage is equal to the reference voltage; 1.285V (typ.).

The functional block diagram of the LM22673 is shown in Figure 12 .

UVLO

The LM22673 also incorporates an input under voltage lock-out (UVLO) feature. This prevents the regulator from turning on when the input voltage is not great enough to properly bias the internal circuitry. The rising threshold is 4.3V (typ.) while the falling threshold is 3.9V (typ.).

Duty-Cycle Limits

Ideally the regulator would control the duty cycle over the full range of zero to one. However due to inherent delays in the circuitry, there are limits on both the maximum and minimum duty cycles that can be reliably controlled. This in turn places limits on the maximum and minimum input and output voltages that can be converted by the LM22673. A minimum on-time is imposed by the regulator in order to correctly measure the switch current during a current limit event. A minimum off-time is imposed in order the re-charge the bootstrap capacitor. The following equation can be used to determine the approximate maximum input voltage for a given output voltage:

$$V_{in}|_{max} \approx \frac{V_{out} + 0.4}{T_{on} \cdot F_{sw} \cdot 1.8} \quad (1)$$

Where F_{sw} is the switching frequency and T_{ON} is the minimum on-time; both found in the Electrical Characteristics table. Nominal values should be used. The worst case is lowest output voltage. If this input voltage is exceeded, the regulator will skip cycles, effectively lowering the switching frequency. The consequences of this are higher output voltage ripple and a degradation of the output voltage accuracy.

The second limitation is the maximum duty cycle before the output voltage will "dropout" of regulation. The following equation can be used to approximate the minimum input voltage before dropout occurs:

$$V_{in}|_{min} \approx \frac{V_{out} + 0.4 + I_{out} \cdot R_L}{1 - T_{off} \cdot F_{sw} \cdot 1.8} + I_{out} \cdot R_{dson} \quad (2)$$

The values of T_{OFF} and $R_{DS(ON)}$ are found in the Electrical Characteristics table. The worst case here is largest load. In this equation, R_L is the D.C. inductor resistance. Of course, the lowest input voltage to the regulator must not be less than 4.5V (typ.).

Current Limit

The LM22673 has current limiting to prevent the switch current from exceeding safe values during an accidental overload on the output. This peak current limit is found in the Electrical Characteristics table under the heading of I_{CL}. The maximum load current that can be provided, before current limit is reached, is determined from the following equation:

$$I_{out}|_{max} \approx I_{CL} - \frac{(V_{in} - V_{out})}{2 \cdot L \cdot F_{sw}} \cdot \frac{V_{out}}{V_{in}} \quad (3)$$

Where L is the value of the power inductor.

When the LM22673 enters current limit, the output voltage will drop and the peak inductor current will be fixed at I_{CL} at the end of each cycle. The switching frequency will remain constant while the duty cycle drops. The load current will not remain constant, but will depend on the severity of the overload and the output voltage.

For very severe overloads ("short-circuit"), the regulator changes to a low frequency current foldback mode of operation. The frequency foldback is about 1/5 of the nominal switching frequency. This will occur when the current limit trips before the minimum on-time has elapsed. This mode of operation is used to prevent inductor current "run-away", and is associated with very low output voltages when in overload. The following equation can be used to determine what level of output voltage will cause the part to change to low frequency current foldback:

$$V_x \leq V_{in} \cdot F_{sw} \cdot T_{on} \cdot 1.8 \quad (4)$$

Where F_{sw} is the normal switching frequency and V_{in} is the maximum for the application. If the overload drives the output voltage to less than or equal to V_x, the part will enter current foldback mode. If a given application can drive the output voltage to $\leq V_x$, during an overload, then a second criterion must be checked. The next equation gives the maximum input voltage, when in this mode, before damage occurs:

$$V_{in} \leq \frac{V_{sc} + 0.4}{T_{on} \cdot F_{sw} \cdot 0.36} \quad (5)$$

Where V_{sc} is the value of output voltage during the overload and F_{sw} is the normal switching frequency. **If the input voltage should exceed this value, while in foldback mode, the regulator and/or the diode may be damaged.** It is important to note that the voltages in these equations are measured at the inductor. Normal trace and wiring resistance will cause the voltage at the inductor to be higher than that at a remote load. Therefore, even if the load is shorted with zero volts across its terminals, the inductor will still see a finite voltage. It is this value that should be used for V_x and V_{sc} in the calculations. In order to return from foldback mode, the load must be reduced to a value much lower than that required to initiate foldback. This load "hysteresis" is a normal aspect of any type of current limit foldback associated with voltage regulators.

The safe operating area, when in short circuit mode, is shown in Figure 13. Operating points below and to the right of the curve represent safe operation.

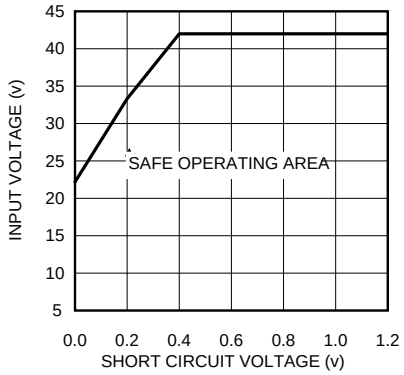


Figure 13. SOA

Current Limit Adjustment

A key feature of the LM22673 is the ability to adjust the peak switch current limit. This can be useful when the full current capability of the regulator is not required for a given application. A smaller current limit may allow the use of power components with lower current ratings, thus saving space and reducing cost. A single resistor between the IADJ pin and ground controls the current limit in accordance with Figure 14. The current limit mode is set during start-up of the regulator. When V_{IN} is applied, a weak pull-up is connected to the IADJ pin and, after approximately 100 µs, the voltage on the pin is checked against a threshold of about 0.8V. With the IADJ pin open, the voltage floats above this threshold, and the current limit is set to the default value of 4.2A (typ). With a resistor present, an internal reference holds the pin voltage at 0.8V; the resulting current sets the current limit. The accuracy of the adjusted current limit will be slightly worse than that of the default value; +35%/ -25% is to be expected. Resistor values should not exceed the limits shown in Figure 14

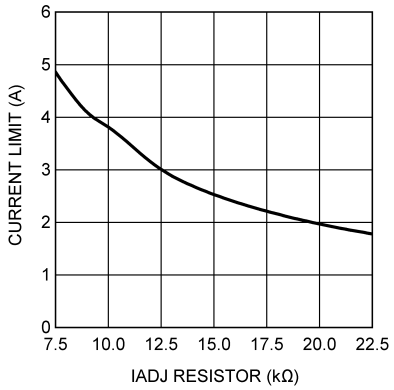


Figure 14. Current Limit vs IADJ Resistor

Soft-Start

The soft-start feature allows the regulator to gradually reach steady-state operation, thus reducing start-up stresses. The internal soft-start feature brings the output voltage up in about 500 µs. This time can be extended by using an external capacitor connected to the SS pin. Values in the range of 100 nF to 1 µF are recommended. The approximate soft-start time can be estimated from the following equation:

$$T_{ss} \approx 26 \times 10^{3} \cdot C_{ss} \quad (6)$$

Soft-start is reset any time the part is shut down or a thermal overload event occurs.

Boot-Strap Supply

The LM22673 incorporates a floating high-side gate driver to control the power MOSFET. The supply for this driver is the external boot-strap capacitor connected between the BOOT pin and SW. A good quality 10 nF ceramic capacitor must be connected to these pins with short, wide PCB traces. One reason the regulator imposes a minimum off-time is to ensure that this capacitor recharges every switching cycle. A minimum load of about 5 mA is required to fully recharge the boot-strap capacitor in the minimum off-time. Some of this load can be provided by the output voltage divider, if used.

Thermal Protection

Internal thermal shutdown circuitry protects the LM22673 should the maximum junction temperature be exceeded. This protection is activated at about 150°C, with the result that the regulator will shutdown until the temperature drops below about 135°C.

Internal Compensation

The LM22673 has internal loop compensation designed to provide a stable regulator over a wide range of external power stage components. The internal compensation of the -ADJ option is optimized for output voltages below 5V. If an output voltage of 5V or greater is needed, the -5.0 option with an external resistor divider can be used.

Ensuring stability of a design with a specific power stage (inductor and output capacitor) can be tricky. The LM22673 stability can be verified using the WEBENCH® Designer online circuit simulation tool at www.ti.com. A quick start spreadsheet can also be downloaded from the online product folder.

The complete transfer function for the regulator loop is found by combining the compensation and power stage transfer functions. The LM22673 has internal type III loop compensation, as detailed in Figure 15 . This is the approximate "straight line" function from the FB pin to the input of the PWM modulator. The power stage transfer function consists of a D.C. gain and a second order pole created by the inductor and output capacitor(s). Due to the input voltage feedforward employed in the LM22673, the power stage D.C. gain is fixed at 20dB. The second order pole is characterized by its resonant frequency and its quality factor (Q). For a first pass design, the product of inductance and output capacitance should conform to the following equation:

$$L \cdot C_{out} \approx 1.1 \times 10^{-9} \quad (7)$$

Alternatively, this pole should be placed between 1.5kHz and 15kHz and is given by the equation shown below:

$$F_o = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{out}}} \quad (8)$$

The Q factor depends on the parasitic resistance of the power stage components and is not typically in the control of the designer. Of course, loop compensation is only one consideration when selecting power stage components; see the Application Information section for more details.

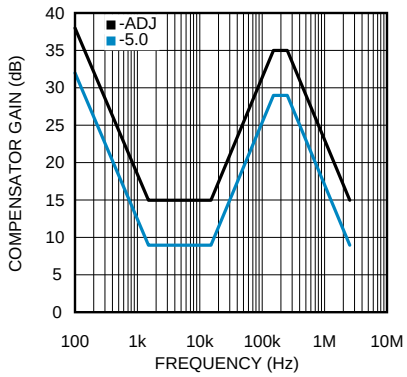


Figure 15. Compensator Gain

In general, hand calculations or simulations can only aid in selecting good power stage components. Good design practice dictates that load and line transient testing should be done to verify the stability of the application. Also, Bode plot measurements should be made to determine stability margins. Application note AN-1889 SNVA364 shows how to perform a loop transfer function measurement with only an oscilloscope and function generator.

Application Information

TYPICAL BUCK REGULATOR APPLICATION

Figure 16 shows an example of converting an input voltage range of 5.5V to 42V, to an output of 3.3v at 3A. See AN-1894 (SNVA367) for more information.

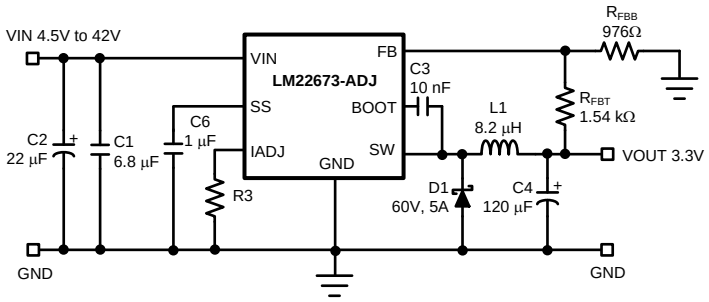


Figure 16. Typical Buck Regulator Application

EXTERNAL COMPONENTS

The following guidelines should be used when designing a step-down (buck) converter with the LM22673.

INDUCTOR

The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltages. To keep the application in continuous conduction mode (CCM), the maximum ripple current, I_{RIPPLE} , should be less than twice the minimum load current.

The general rule of keeping the inductor current peak-to-peak ripple around 30% of the nominal output current is a good compromise between excessive output voltage ripple and excessive component size and cost. Using this value of ripple current, the value of inductor, L, is calculated using the following formula:

$$L = \frac{(V_{in} - V_{out}) \cdot V_{out}}{0.3 \cdot I_{out} \cdot F_{sw} \cdot V_{in}} \quad (9)$$

where F_{sw} is the switching frequency and V_{in} should be taken at its maximum value, for the given application. The above formula provides a guide to select the value of the inductor L; the nearest standard value will then be used in the circuit.

Once the inductor is selected, the actual ripple current can be found from the equation shown below:

$$\Delta I = \frac{(V_{in} - V_{out}) \cdot V_{out}}{L \cdot F_{sw} \cdot V_{in}} \quad (10)$$

Increasing the inductance will generally slow down the transient response but reduce the output voltage ripple. Reducing the inductance will generally improve the transient response but increase the output voltage ripple.

The inductor must be rated for the peak current, I_{PK}, in a given application, to prevent saturation. During normal loading conditions, the peak current is equal to the load current plus 1/2 of the inductor ripple current.

During an overload condition, as well as during certain load transients, the controller may trip current limit. In this case the peak inductor current is given by I_{CL}, found in the Electrical Characteristics table. Good design practice requires that the inductor rating be adequate for this overload condition. **If the inductor is not rated for the maximum expected current, it can saturate resulting in damage to the LM22673 and/or the power diode.** This consideration highlights the value of the current limit adjust feature of the LM22673.

INPUT CAPACITOR

The input capacitor selection is based on both input voltage ripple and RMS current. Good quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the regulator current during switch on-time. Low ESR ceramic capacitors are preferred. Larger values of input capacitance are desirable to reduce voltage ripple and noise on the input supply. This noise may find its way into other circuitry, sharing the same input supply, unless adequate bypassing is provided. A very approximate formula for determining the input voltage ripple is shown below:

$$V_{ri} \approx \frac{I_{out}}{4 \cdot F_{sw} \cdot C_{in}} \quad (11)$$

Where V_{ri} is the peak-to-peak ripple voltage at the switching frequency. Another concern is the RMS current passing through this capacitor. The following equation gives an approximation to this current:

$$I_{rms} \approx \frac{I_{out}}{2} \quad (12)$$

The capacitor must be rated for at least this level of RMS current at the switching frequency.

All ceramic capacitors have large voltage coefficients, in addition to normal tolerances and temperature coefficients. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum capacitance up to the desired value. This may also help with RMS current constraints by sharing the current among several capacitors. Many times it is desirable to use an electrolytic capacitor on the input, in parallel with the ceramics. The moderate ESR of this capacitor can help to damp any ringing on the input supply caused by long power leads. This method can also help to reduce voltage spikes that may exceed the maximum input voltage rating of the LM22673.

It is good practice to include a high frequency bypass capacitor as close as possible to the LM22673. This small case size, low ESR, ceramic capacitor should be connected directly to the VIN and GND pins with the shortest possible PCB traces. Values in the range of 0.47 µF to 1 µF are appropriate. This capacitor helps to provide a low impedance supply to sensitive internal circuitry. It also helps to suppress any fast noise spikes on the input supply that may lead to increased EMI.

OUTPUT CAPACITOR

The output capacitor is responsible for filtering the output voltage and supplying load current during transients. Capacitor selection depends on application conditions as well as ripple and transient requirements. Best performance is achieved with a parallel combination of ceramic capacitors and a low ESR SP™ or POSCAP™ type. Very low ESR capacitors such as ceramics reduce the output ripple and noise spikes, while higher value electrolytics or polymers provide large bulk capacitance to supply transients. Assuming very low ESR, the following equation gives an approximation to the output voltage ripple:

$$V_{ro} \approx \frac{(V_{in}-V_{out})\cdot V_{out}}{8\cdot V_{in}} \cdot \frac{1}{F_{sw}^2 \cdot L \cdot C_{out}} \quad (13)$$

Typically, a total value of 100 µF, or greater, is recommended for output capacitance.

In applications with V_{out} less than 3.3V, it is critical that low ESR output capacitors are selected. This will limit potential output voltage overshoots as the input voltage falls below the device normal operating range.

BOOT-STRAP CAPACITOR

The bootstrap capacitor between the BOOT pin and the SW pin supplies the gate current to turn on the N-channel MOSFET. The recommended value of this capacitor is 10 nF and should be a good quality, low ESR ceramic capacitor. In some cases it may be desirable to slow down the turn-on of the internal power MOSFET, in order to reduce EMI. This can be done by placing a small resistor in series with the C_{boot} capacitor. Resistors in the range of 10Ω to 50Ω can be used. This technique should only be used when absolutely necessary, since it will increase switching losses and thereby reduce efficiency.

OUTPUT VOLTAGE DIVIDER SELECTION

For output voltages between about 1.285V and 5V, the -ADJ option should be used, with an appropriate voltage divider as shown in Figure 17. The following equation can be used to calculate the resistor values of this divider:

$$R_{FBT} = \left[\frac{V_{out}}{1.285} - 1\right] \cdot R_{FBB} \quad (14)$$

A good value for R_{FBB} is 1k Ω. This will help to provide some of the minimum load current requirement and reduce susceptibility to noise pick-up. The top of R_{FBT} should be connected directly to the output capacitor or to the load for remote sensing. If the divider is connected to the load, a local high-frequency bypass should be provided at that location.

For output voltages of 5V, the -5.0 option should be used. In this case no divider is needed and the FB pin is connected to the output. The approximate values of the internal voltage divider are as follows: 7.38kΩ from the FB pin to the input of the error amplifier and 2.55kΩ from there to ground.

Both the -ADJ and -5.0 options can be used for output voltages greater than 5V, by using the correct output divider. As mentioned in the Internal Compensation section, the -5.0 option is optimized for output voltages of 5V. However, for output voltages greater than 5V, this option may provide better loop bandwidth than the -ADJ option, in some applications. If the -5.0 option is to be used at output voltages greater than 5V, the following equation should be used to determine the resistor values in the output divider:

$$R_{FBT} = \frac{R_{FBB}\cdot(V_{out}-5)}{5+ R_{FBB}\cdot 5\times 10^{-4}} \quad (15)$$

Again a value of R_{FBB} of about 1k Ω is a good first choice.

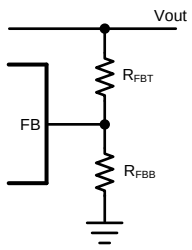


Figure 17. Resistive Feedback Divider

A maximum value of 10 kΩ is recommended for the sum of R_{FBB} and R_{FBT} to maintain good output voltage accuracy for the -ADJ option. A maximum of 2 kΩ is recommended for the -5.0 option. For the -5.0 option, the total internal divider resistance is typically 9.93 kΩ.

In all cases the output voltage divider should be placed as close as possible to the FB pin of the LM22673; since this is a high impedance input and is susceptible to noise pick-up.

POWER DIODE

A Schottky type power diode is required for all LM22673 applications. Ultra-fast diodes are not recommended and may result in damage to the IC due to reverse recovery current transients. The near ideal reverse recovery characteristics and low forward voltage drop of Schottky diodes are particularly important for high input voltage and low output voltage applications common to the LM22673. The reverse breakdown rating of the diode should be selected for the maximum V_{IN}, plus some safety margin. A good rule of thumb is to select a diode with a reverse voltage rating of 1.3 times the maximum input voltage.

Select a diode with an average current rating at least equal to the maximum load current that will be seen in the application.

Circuit Board Layout

Board layout is critical for the proper operation of switching power supplies. First, the ground plane area must be sufficient for thermal dissipation purposes. Second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such cases, the rapid increase of input current combined with the parasitic trace inductance generates unwanted L di/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This noise may turn into electromagnetic interference (EMI) and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

The most important layout rule is to keep the AC current loops as small as possible. Figure 18 shows the current flow in a buck converter. The top schematic shows a dotted line which represents the current flow during the FET switch on-state. The middle schematic shows the current flow during the FET switch off-state.

The bottom schematic shows the currents referred to as AC currents. These AC currents are the most critical since they are changing in a very short time period. The dotted lines of the bottom schematic are the traces to keep as short and wide as possible. This will also yield a small loop area reducing the loop inductance. To avoid functional problems due to layout, review the PCB layout example. Best results are achieved if the placement of the LM22673, the bypass capacitor, R_{FFB}, R_{FBT}, the Schottky diode and the inductor are placed as shown in the example. Note that, in the layout shown, R1 = R_{FBB} and R2 = R_{FBT}. It is also recommended to use 2oz copper boards or heavier to help thermal dissipation and to reduce the parasitic inductances of board traces. See application note AN-1229 (SNVA054) for more information.

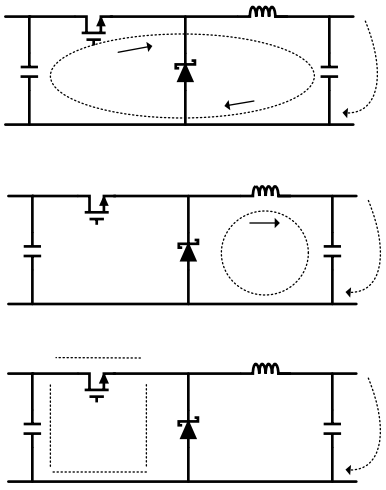


Figure 18. Current Flow in a Buck Application

Thermal Considerations

The components with the highest power dissipation are the power diode and the power MOSFET internal to the LM22673 regulator. The easiest method to determine the power dissipation within the LM22673 is to measure the total conversion losses then subtract the power losses in the diode and inductor. The total conversion loss is the difference between the input power and the output power. An approximation for the power diode loss is:

$$P_D = I_{out} \cdot V_D \cdot \left[1 - \frac{V_{out}}{V_{in}}\right] \quad (16)$$

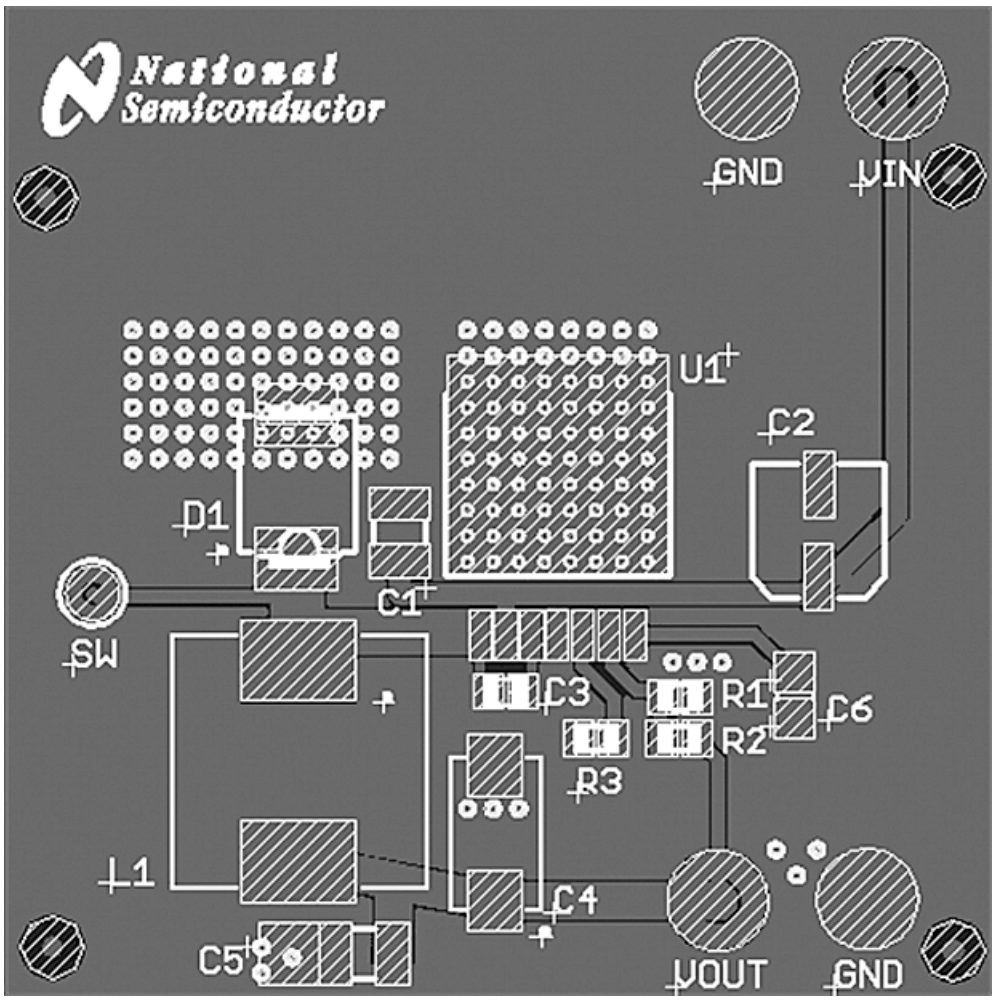
Where V_D is the diode voltage drop. An approximation for the inductor power is:

$$P_L = I_{out}^2 \cdot R_L \cdot 1.1 \quad (17)$$

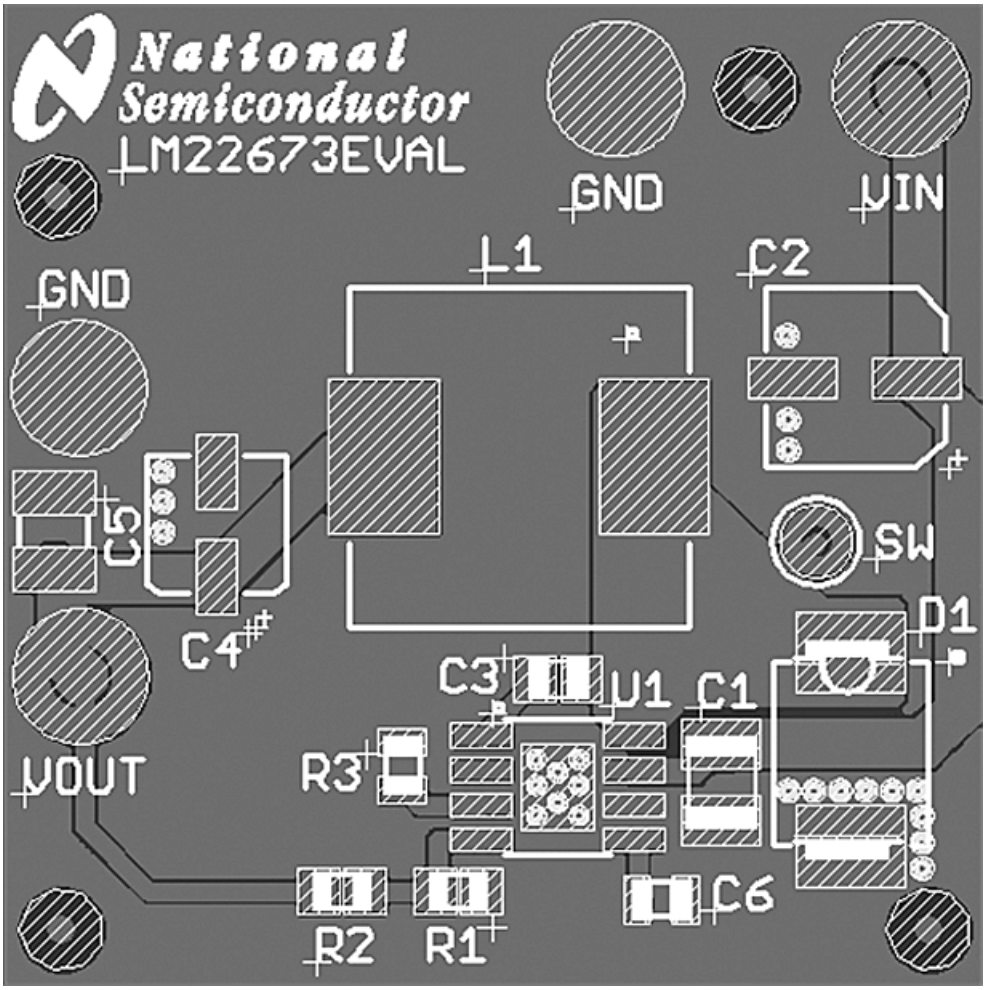
where R_L is the DC resistance of the inductor and the 1.1 factor is an approximation for the AC losses.

The regulator has an exposed thermal pad to aid power dissipation. Adding multiple vias under the device to the ground plane will greatly reduce the regulator junction temperature. Selecting a diode with an exposed pad will also aid the power dissipation of the diode. The most significant variables that affect the power dissipation of the regulator are output current, input voltage and operating frequency. The power dissipated while operating near the maximum output current and maximum input voltage can be appreciable. The junction-to-ambient thermal resistance of the LM22673 will vary with the application. The most significant variables are the area of copper in the PC board, the number of vias under the IC exposed pad and the amount of forced air cooling provided. A large continuos ground plane on the top or bottom PCB layer will provide the most effective heat dissipation. The integrity of the solder connection from the IC exposed pad to the PC board is critical. Excessive voids will greatly diminish the thermal dissipation capacity. The junction-to-ambient thermal resistance of the LM22673 SO PowerPAD package, and the PFM package, are specified in the Electrical Characteristics table. See application note AN-2020 (SNVA419) for more information.

PCB Layout Example for PFM Package



PCB Layout Example for SO PowerPAD Package



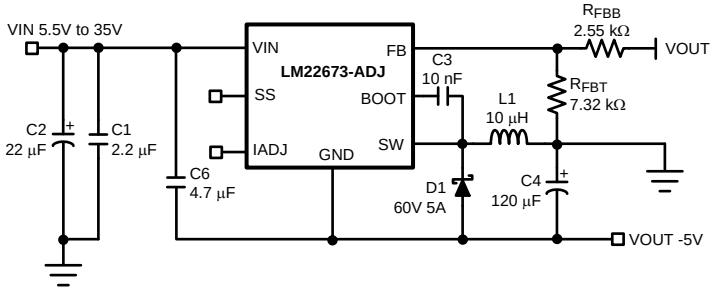


Figure 19. Inverting Regulator Application

REVISION HISTORY

Changes from Revision M (April 2013) to Revision N	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM22673MR-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L22673 5.0	Samples
LM22673MR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L22673 ADJ	Samples
LM22673MRE-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L22673 5.0	Samples
LM22673MRE-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L22673 ADJ	Samples
LM22673MRX-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L22673 5.0	Samples
LM22673MRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L22673 ADJ	Samples
LM22673QMR-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L22673 Q-5.0	Samples
LM22673QMR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L22673 QADJ	Samples
LM22673QMRE-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L22673 Q-5.0	Samples
LM22673QMRE-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L22673 QADJ	Samples
LM22673QMRX-5.0/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L22673 Q-5.0	Samples
LM22673QMRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L22673 QADJ	Samples
LM22673QTJ-5.0/NOPB	ACTIVE	TO-263	NDR	7	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM22673 QTJ-5.0	Samples
LM22673QTJ-ADJ/NOPB	ACTIVE	TO-263	NDR	7	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM22673 QTJ-ADJ	Samples
LM22673QTJE-5.0/NOPB	ACTIVE	TO-263	NDR	7	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM22673 QTJ-5.0	Samples
LM22673QTJE-ADJ/NOPB	ACTIVE	TO-263	NDR	7	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM22673 QTJ-ADJ	Samples
LM22673TJ-5.0/NOPB	ACTIVE	TO-263	NDR	7	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-5.0	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM22673TJ-ADJ/NOPB	ACTIVE	TO-263	NDR	7	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-ADJ	Samples
LM22673TJE-5.0/NOPB	ACTIVE	TO-263	NDR	7	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-5.0	Samples
LM22673TJE-ADJ/NOPB	ACTIVE	TO-263	NDR	7	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM22673 TJ-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

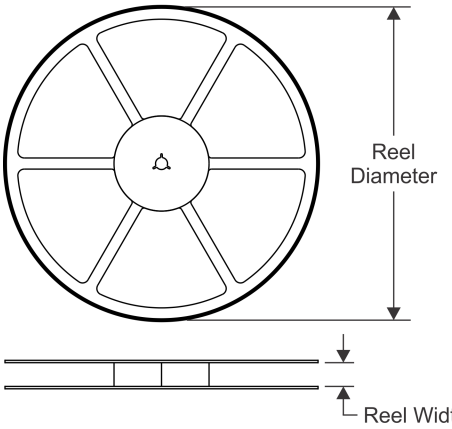
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

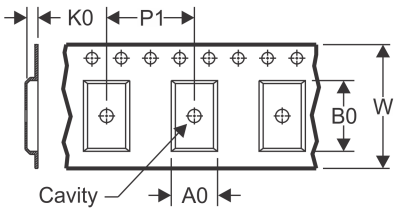
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

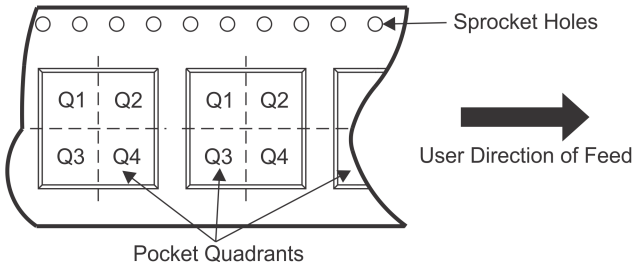


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

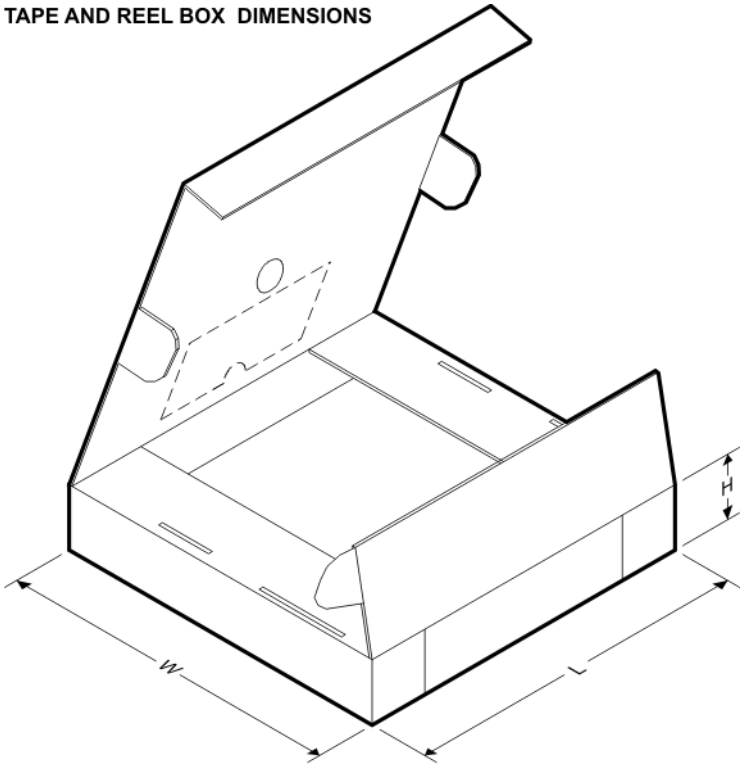


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM22673MRE-5.0/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673MRE-ADJ/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673MRX-5.0/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673MRX-ADJ/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRE-5.0/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRE-ADJ/NOPB	SO Power PAD	DDA	8	250	178.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRX-5.0/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM22673QMRX-ADJ/NOP	SO	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
B	Power PAD											
LM22673QTJ-5.0/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673QTJ-ADJ/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673QTJE-5.0/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673QTJE-ADJ/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJ-5.0/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJ-ADJ/NOPB	TO-263	NDR	7	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJE-5.0/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LM22673TJE-ADJ/NOPB	TO-263	NDR	7	250	178.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

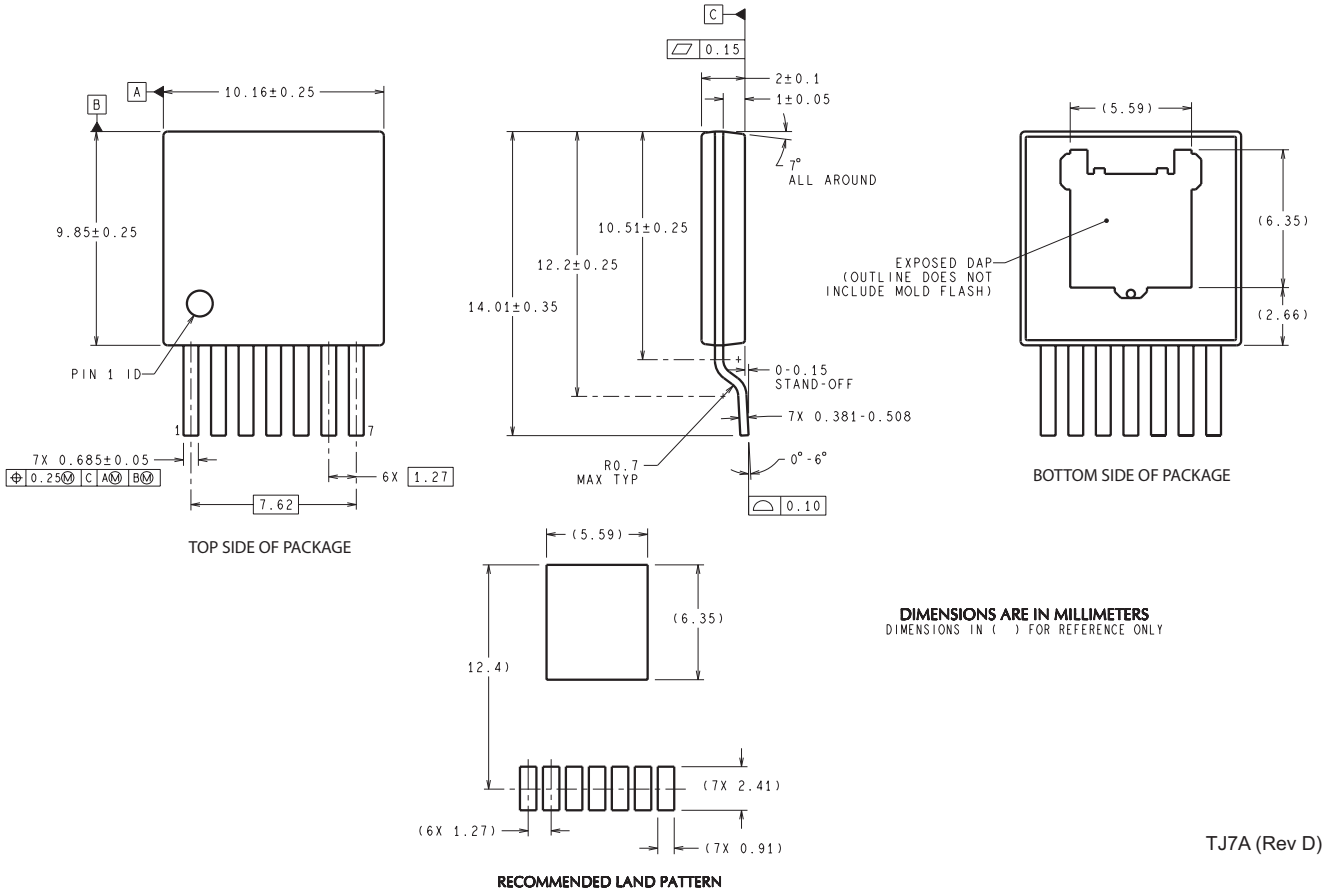


*All dimensions are nominal

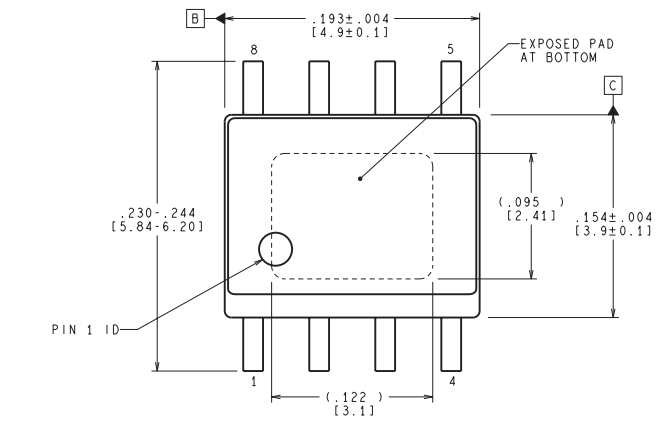
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM22673MRE-5.0/NOPB	SO PowerPAD	DDA	8	250	213.0	191.0	55.0
LM22673MRE-ADJ/NOPB	SO PowerPAD	DDA	8	250	213.0	191.0	55.0
LM22673MRX-5.0/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM22673MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM22673QMRE-5.0/NOPB	SO PowerPAD	DDA	8	250	213.0	191.0	55.0
LM22673QMRE-ADJ/NOPB	SO PowerPAD	DDA	8	250	213.0	191.0	55.0

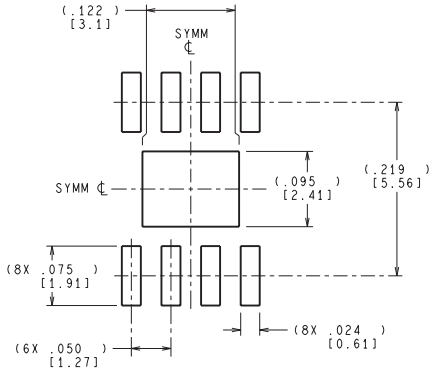
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM22673QMRX-5.0/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM22673QMRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM22673QTJ-5.0/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673QTJ-ADJ/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673QTJE-5.0/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22673QTJE-ADJ/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22673TJ-5.0/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673TJ-ADJ/NOPB	TO-263	NDR	7	1000	367.0	367.0	35.0
LM22673TJE-5.0/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0
LM22673TJE-ADJ/NOPB	TO-263	NDR	7	250	210.0	185.0	35.0

NDR0007A


C
0.15
2±0.1
1±0.05
7°
ALL AROUND
A
B
10.16±0.25
9.85±0.25
10.51±0.25
12.2±0.25
14.01±0.35
PIN 1 ID
1
7
0-0.15
STAND-OFF
7X 0.381-0.508
R0.7
MAX TYP
0°-6°
0.10
7X 0.685±0.05
0.25 M C A M B M
6X 1.27
7.62
TOP SIDE OF PACKAGE
(5.59)
(6.35)
EXPOSED DAP
(OUTLINE DOES NOT
INCLUDE MOLD FLASH)
(2.66)
BOTTOM SIDE OF PACKAGE
(5.59)
(6.35)
12.4)
(7X 2.41)
(6X 1.27)
(7X 0.91)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
TJ7A (Rev D)

DDA0008B





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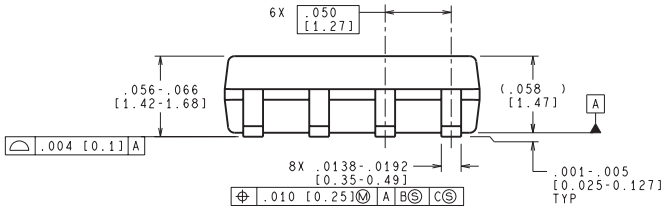

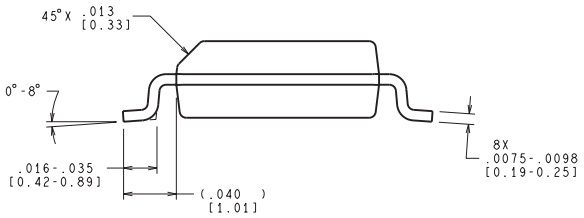

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