LM3424 Constant Current N-Channel Controller with Thermal Foldback for Driving LEDs

Check for Samples: LM3424

FEATURES

- **LM3424Q is an Automotive Grade Product that is AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)**
- **V_{IN} Range from 4.5V to 75V**
- **High-side Adjustable Current Sense**
- **2Ω, 1A Peak MosFET Gate Driver**
- **Input Under-voltage and Output Over-voltage Protection**
- **PWM and Analog Dimming**
- **Cycle-by-cycle Current Limit**
- **Programmable Slope Compensation**
- **Programmable, Synchronizable Switching Frequency**
- **Programmable Thermal Foldback**
- **Programmable Softstart**
- **Precision Voltage Reference**
- **Low Power Shutdown and Thermal Shutdown**

APPLICATIONS

- **LED Drivers - Buck, Boost, Buck-Boost, and SEPIC**
- **Indoor and Outdoor Area SSL**
- **Automotive**
- **General Illumination**
- **Constant-Current Regulators**

DESCRIPTION

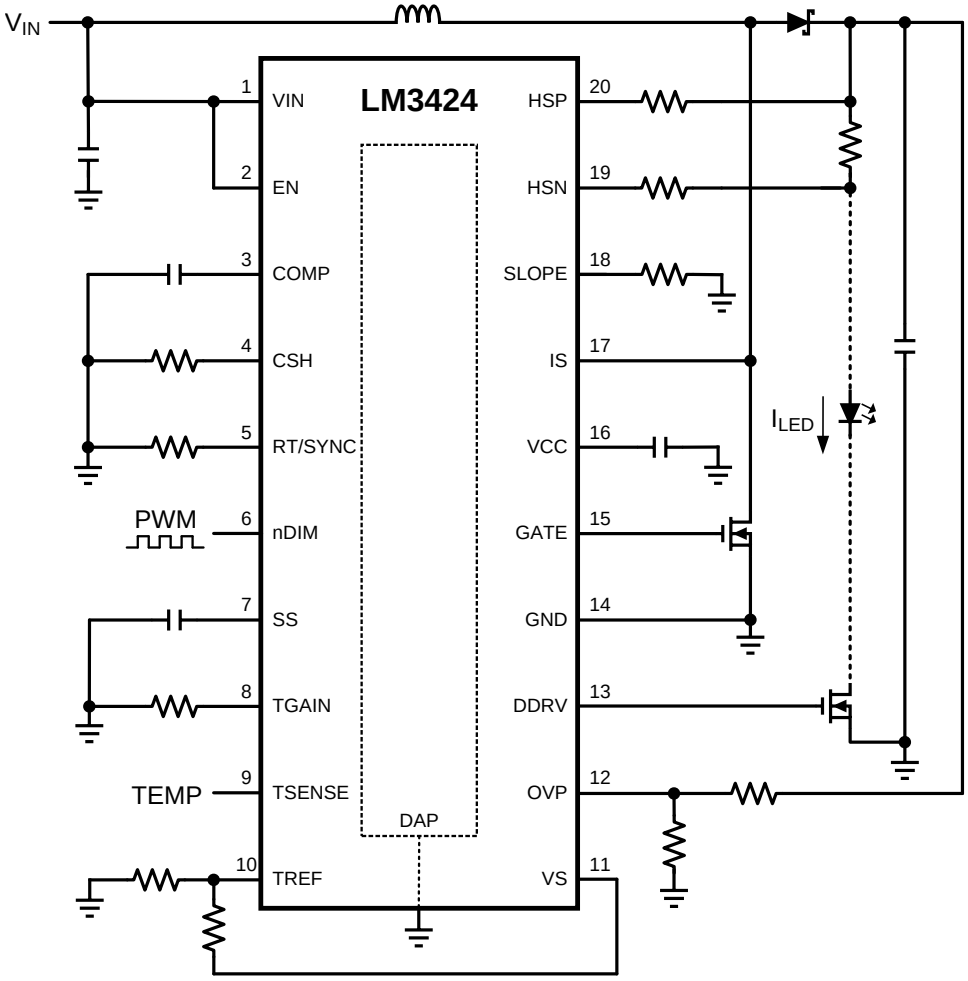
The LM3424 is a versatile high voltage N-channel MosFET controller for LED drivers . It can be easily configured in buck, boost, buck-boost and SEPIC topologies. In addition, the LM3424 includes a thermal foldback feature for temperature management of the LEDs. This flexibility, along with an input voltage rating of 75V, makes the LM3424 ideal for illuminating LEDs in a large family of applications.

Adjustable high-side current sense voltage allows for tight regulation of the LED current with the highest efficiency possible. The LM3424 uses standard peak current-mode control providing inherent input voltage feed-forward compensation for better noise immunity. It is designed to provide accurate thermal foldback with a programmable foldback breakpoint and slope. In addition, a 2.45V reference is provided.

The LM3424 includes a high-voltage startup regulator that operates over a wide input range of 4.5V to 75V. The internal PWM controller is designed for adjustable switching frequencies of up to 2.0 MHz and external synchronization is possible. The controller is capable of high speed PWM dimming and analog dimming. Additional features include slope compensation, softstart, over-voltage and under-voltage lock-out, cycle-by-cycle current limit, and thermal shutdown.

The LM3424Q is an Automotive Grade product that is AEC-Q100 grade 1 qualified.

Typical Boost Application Circuit



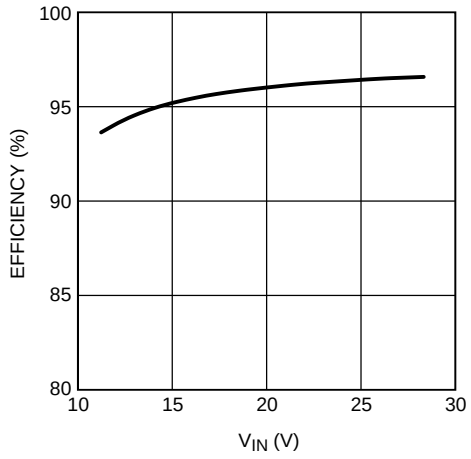


Figure 1. Boost Evaluation Board
9 Series LEDs at 1A

Connection Diagram

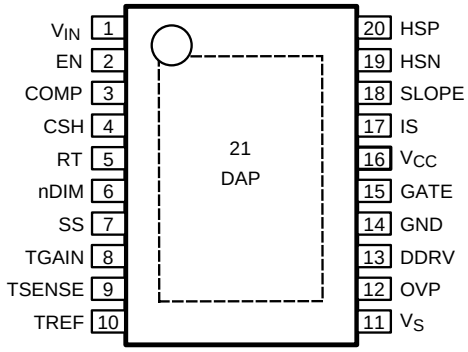


Figure 2. 20-Lead HTSSOP EP

PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	V_{IN}	Input Voltage	Bypass with 100 nF capacitor to GND as close to the device as possible.
2	EN	Enable	Connect to > 2.4V to enable the device or to < 0.8V for low power shutdown.
3	COMP	Compensation	Connect a capacitor to GND to compensate control loop.
4	CSH	Current Sense High	Connect a resistor to GND to set the signal current. Can also be used to analog dim as explained in the THERMAL FOLDBACK / ANALOG DIMMING section.
5	RT	Resistor Timing	Connect a resistor to GND to set the switching frequency. Can also be used to synchronize external clock as explained in the SWITCHING FREQUENCY section.
6	nDIM	Dimming Input / Under-Voltage Protection	Connect a PWM signal for dimming as detailed in the PWM DIMMING section and/or a resistor divider from V_{IN} to program input under-voltage lockout.
7	SS	Soft-start	Connect a capacitor to GND to extend start-up time.
8	TGAIN	Temp Foldback Gain	Connect a resistor to GND to set the foldback slope.
9	TSENSE	Temp Sense Input	Connect a resistor/ thermistor divider from V_S to sense the temperature as explained in the THERMAL FOLDBACK / ANALOG DIMMING section.
10	TREF	Temp Foldback Reference	Connect a resistor divider from V_S to set the foldback reference voltage.
11	V_S	Voltage Reference	2.45V reference for temperature foldback circuit and other external circuitry.
12	OVP	Over-Voltage Protection	Connect a resistor divider from V_O to program output over-voltage lockout.
13	DDRV	Dimming Gate Drive Output	Connect to gate of dimming MosFET.
14	GND	Ground	Connect to DAP to provide proper system GND

PIN DESCRIPTIONS (continued)

Pin	Name	Description	Application Information
15	GATE	Main Gate Drive Output	Connect to gate of main switching MosFET.
16	V_{CC}	Internal Regulator Output	Bypass with a 2.2 µF – 3.3 µF, ceramic capacitor to GND.
17	IS	Main Switch Current Sense	Connect to the drain of the main N-channel MosFET switch for R_{DS-ON} sensing or to a sense resistor installed in the source of the same device.
18	SLOPE	Slope Compensation	Connect a resistor to GND to set slope of additional ramp.
19	HSN	LED Current Sense Negative	Connect through a series resistor to LED current sense resistor (negative).
20	HSP	LED Current Sense Positive	Connect through a series resistor to LED current sense resistor (positive).
DAP	DAP	Thermal pad on bottom of IC	Connect to GND. Refer to (1) for thermal considerations.

(1) Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for a reference layout wherein the 20L HTSSOP EP package has its DAP pad populated with 9 vias. In applications where high maximum power dissipation exists, namely driving a large MosFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$. In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be 104 °C/W for the 20L HTSSOP EP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

V_{IN}, EN, nDIM		-0.3V to 76.0V -1 mA continuous
OVP, HSP, HSN		-0.3V to 76.0V -100 µA continuous
IS		-0.3V to 76.0V -2V for 100 ns -1 mA continuous
V_{CC}		-0.3V to 8.0V
V_S, TREF, TSENSE, TGAIN, COMP, CSH, RT, SLOPE, SS		-0.3V to 6.0V
SS		-30 µA to +30 µA continuous
GATE, DDRV		-0.3V to V_{CC} -2.5V for 100 ns V_{CC}+2.5V for 100 ns -1 mA to +1 mA continuous
GND		-0.3V to 0.3V -2.5V to 2.5V for 100 ns
Maximum Junction Temperature		Internally Limited
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Reflow and Solder) (3)		260°C
Continuous Power Dissipation		Internally Limited
ESD Susceptibility (4)	Human Body Model	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Refer to TI's packaging website for more detailed information and mounting techniques, http://www.ti.com/packaging.
(4) Human Body Model, applicable std. JESD22-A114-C.

OPERATING CONDITIONS(1)

Operating Junction Temperature Range	−40°C to +125°C
Input Voltage V_{IN}	4.5V to 75V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

ELECTRICAL CHARACTERISTICS(1)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25°C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: V_{IN} = +14V.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
STARTUP REGULATOR (V_{CC})						
V_{CC-REG}	V_{CC} Regulation	I_{CC} = 0 mA	**6.30**	6.90	**7.35**	V
I_{CC-LIM}	V_{CC} Current Limit	V_{CC} = 0V	**20**	25		mA
I_Q	Quiescent Current	EN = 3.0V, Static		2.0	**3.0**	mA
I_{SD}	Shutdown Current	EN = 0V		0.1	1.0	µA
$V_{CC-UVLO}$	V_{CC} UVLO Threshold	V_{CC} Increasing		4.17	**4.50**	V
		V_{CC} Decreasing	**3.70**	4.08		V
V_{CC-HYS}	V_{CC} UVLO Hysteresis			0.1		V
ENABLE (EN)						
V_{EN-ST}	EN Startup Threshold	EN Increasing		1.75	**2.40**	V
		EN decreasing	**0.80**	1.63		V
V_{EN-HYS}	EN Startup Hysteresis			0.1		V
R_{EN}	EN Pull-down Resistance		**0.45**	0.82	**1.30**	MΩ
OVER-VOLTAGE PROTECTION (OVP)						
V_{TH-OVP}	OVP OVLO Threshold	OVP Increasing	**1.185**	1.240	**1.285**	V
$I_{HYS-OVP}$	OVP Hysteresis Source Current	OVP Active (high)	**13**	20	**27**	µA
ERROR AMPLIFIER						
V_{CSH}	CSH Reference Voltage	With Respect to GND	**1.210**	1.235	**1.260**	V
	Error Amplifier Input Bias Current		-0.6	0	0.6	µA
	COMP Sink / Source Current		**17**	26	**35**	µA
	Transconductance			100		µA/V
	Linear Input Range	(4)		±125		mV
	Transconductance Bandwidth	-6dB Unloaded Response (4)		1.0		MHz
OSCILLATOR (RT)						
f_{SW}	Switching Frequency	R_T = 36 kΩ	**164**	207	**250**	kHz
		R_T = 12 kΩ	**525**	597	**669**	kHz
$V_{RT-SYNC}$	Sync Threshold			3.5		V
PWM COMPARATOR						
$V_{CP-BASE}$	COMP to PWM Offset - No Slope Compensation		**750**	900	**1050**	mV
SLOPE COMPENSATION (SLOPE)						
ΔV_{CP}	Slope Compensation Amplitude	Additional COMP to PWM Offset - SLOPE sinking 100 µA		85		mV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

(2) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(3) Typical numbers are at 25°C and represent the most likely norm.

(4) These electrical parameters are specified by design, and are not verified by test.

ELECTRICAL CHARACTERISTICS[1] (continued)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25°C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: V_{IN} = +14V.

Symbol	Parameter	Conditions		Min (2)	Typ (3)	Max (2)	Units
CURRENT LIMIT (IS)							
V_{LIM}	Current Limit Threshold			**215**	245	**275**	mV
	V_{LIM} Delay to Output				35	**75**	ns
t_{ON-MIN}	Leading Edge Blanking Time			**140**	240	**340**	ns
HIGH SIDE TRANSCONDUCTANCE AMPLIFIER							
	Input Bias Current				10		µA
	Transconductance			**20**			mA/V
	Input Offset Current			**-1.5**	0	**1.5**	µA
	Input Offset Voltage			**-5**	0	**5**	mV
	Transconductance Bandwidth	I_{CSH} = 100 µA [5]			500		kHz
GATE DRIVER (GATE)							
$R_{SRC-GATE}$	GATE Sourcing Resistance	GATE = High			2.0	**6.0**	Ω
$R_{SNK-GATE}$	GATE Sinking Resistance	GATE = Low			1.3	**4.5**	Ω
UNDER-VOLTAGE LOCKOUT and DIM INPUT (nDIM)							
$V_{TH-nDIM}$	nDIM / UVLO Threshold			**1.185**	1.240	**1.285**	V
$I_{HYS-nDIM}$	nDIM Hysteresis Current			**13**	20	**27**	µA
DIM DRIVER (DDRV)							
$R_{SRC-DDRV}$	DDRV Sourcing Resistance	DDRV = High			13.5	**30.0**	Ω
$R_{SNK-DDRV}$	DDRV Sinking Resistance	DDRV = Low			3.5	**10.0**	Ω
	nDIM rising to DDRV rising				700		ns
	nDIM rising to DDRV falling				360		ns
SOFT-START (SS)							
I_{SS}	Soft-start current				10		µA
THERMAL CONTROL							
V_S	V_S Voltage	I_{VS} = 0A		**2.40**	2.45	**2.50**	V
		I_{VS} = 1 mA					
	TREF input bias current	V_{TREF} = 1.5V V_{TSENSE} = 1.5V			0.1		µA
	TSENSE Input Bias Current	V_{TREF} = 1.5V V_{TSENSE} = 1.5V			0.1		µA
$I_{TGAIN-MAX}$	TGAIN Maximum Sourcing Current	V_{TGAIN} = 2V		**200**	600		µA
I_{TF}	CSH Current with High-side Amplifier Disabled	R_{TGAIN} = 10 kΩ	V_{TREF} = 1.5V V_{TSENSE} = 0.5V		100		µA
			V_{TREF} = 1.5V V_{TSENSE} = 1.4V		10		µA
			V_{TREF} = 1.5V V_{TSENSE} = 1.5V		2		µA

(5) These electrical parameters are specified by design, and are not verified by test.

ELECTRICAL CHARACTERISTICS[1] (continued)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25°C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: V_{IN} = +14V.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold	(6)		165		°C
T_{HYS}	Thermal Shutdown Hysteresis	(6)		25		
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	20L HTSSOP EP (7)		34		°C/W

(6) These electrical parameters are specified by design, and are not verified by test.

(7) Junction-to-ambient thermal resistance is highly board-layout dependent. The numbers listed in the table are given for a reference layout wherein the 20L HTSSOP EP package has its DAP pad populated with 9 vias. In applications where high maximum power dissipation exists, namely driving a large MosFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$. In most applications there is little need for the full power dissipation capability of this advanced package. Under these circumstances, no vias would be required and the thermal resistances would be 104 °C/W for the 20L HTSSOP EP. It is possible to conservatively interpolate between the full via count thermal resistance and the no via count thermal resistance with a straight line to get a thermal resistance for any number of vias in between these two limits.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A=+25°C and V_{IN} = 14V unless otherwise specified

Boost Efficiency vs. Input Voltage
V_O = 32V (9 LEDs) (1)

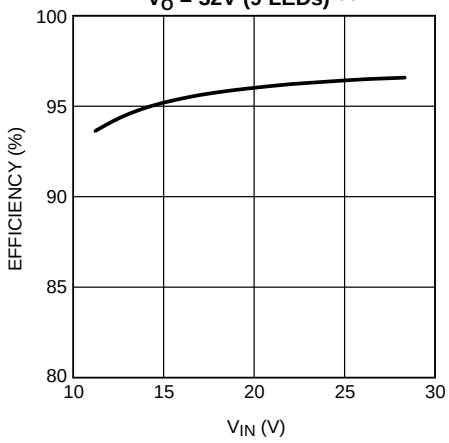


Figure 3.

Buck-Boost Efficiency vs. Input Voltage
V_O = 21V (6 LEDs) (2)

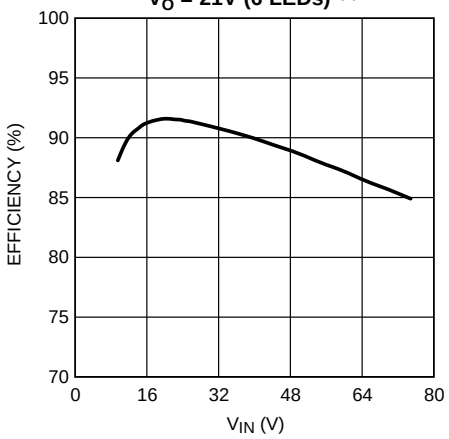


Figure 4.

Boost LED Current vs. Input Voltage
V_O = 32V (9 LEDs) (1)

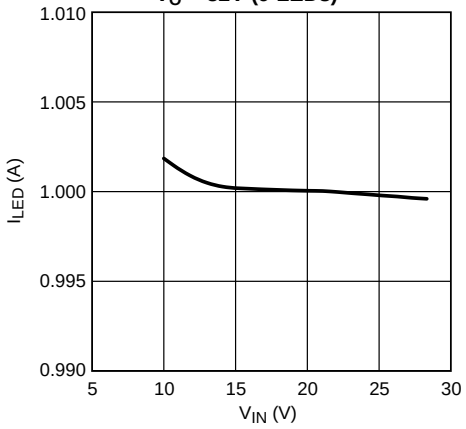


Figure 5.

Buck-Boost LED Current vs. Input Voltage
V_O = 21V (6 LEDs) (2)

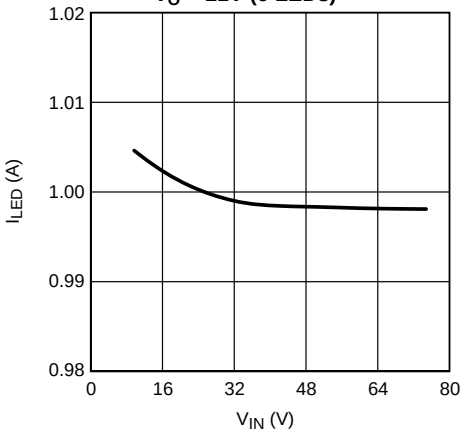


Figure 6.

Analog Dimming
V_O = 21V (6 LEDs); V_{IN} = 24V (2)

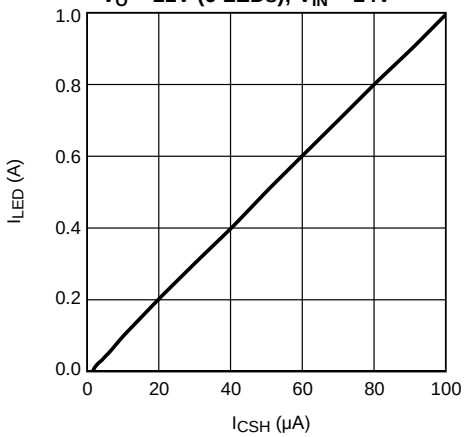


Figure 7.

PWM Dimming
V_O = 32V (9 LEDs); V_{IN} = 24V (1)

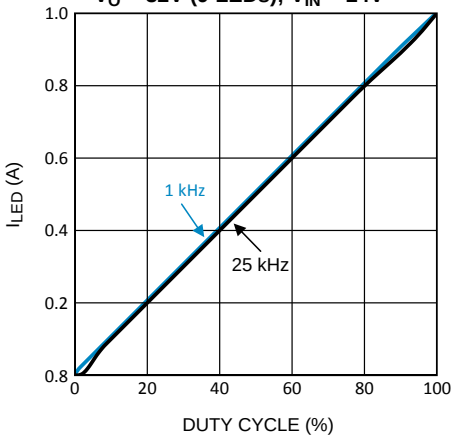


Figure 8.

(1) The measurements were made using the standard boost evaluation board from AN-1969 (literature number SNVA398).
(2) The measurements were made using the standard buck-boost evaluation board from AN-1967 (literature number SNVA397).

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A=+25°C and V_{IN} = 14V unless otherwise specified

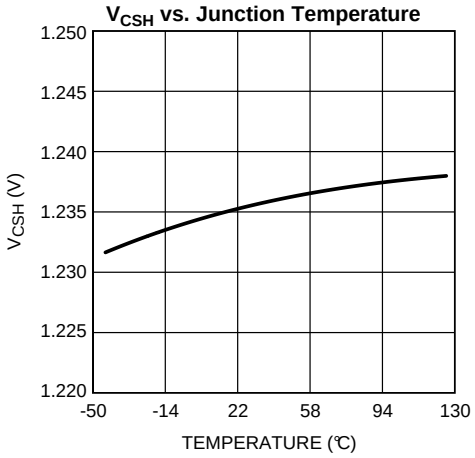


Figure 9.

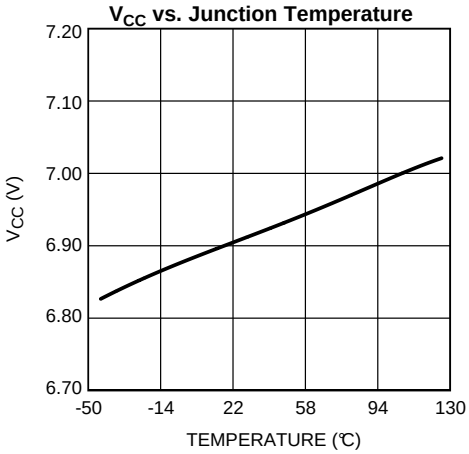


Figure 10.

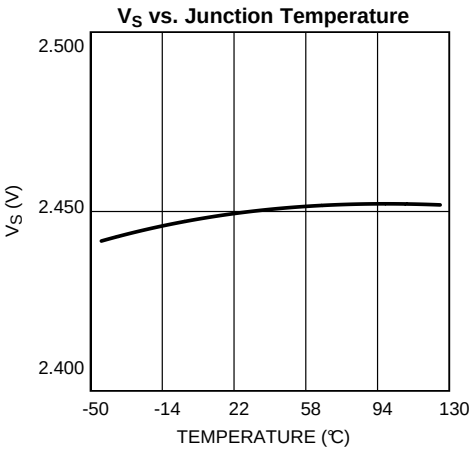


Figure 11.

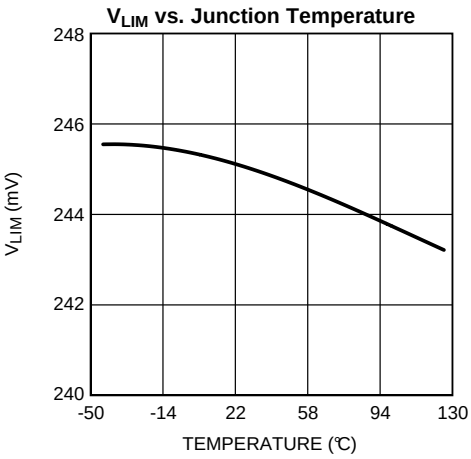


Figure 12.

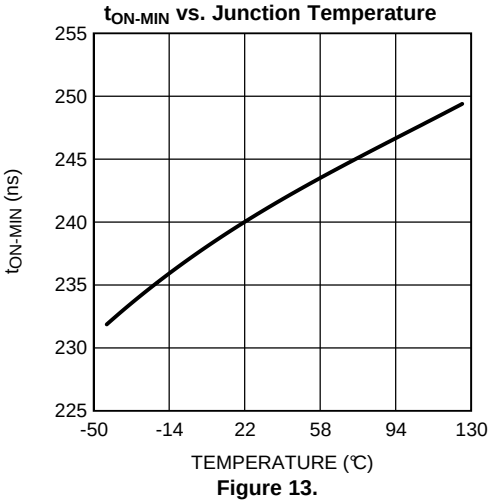


Figure 13.

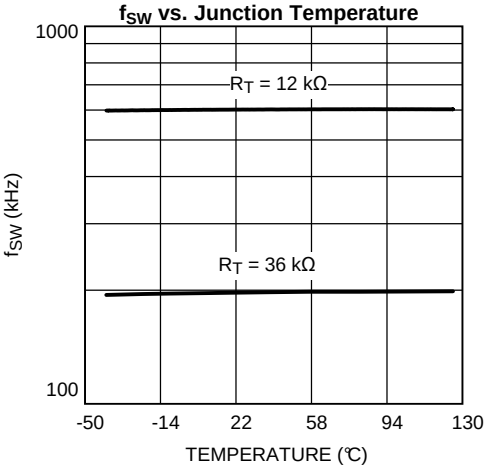


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A=+25°C and V_{IN} = 14V unless otherwise specified

I_{TF} vs. Junction Temperature
R_{GAIN} = 10 kΩ; V_{TSENSE} = 0.5V; V_{TREF} = 1.5V

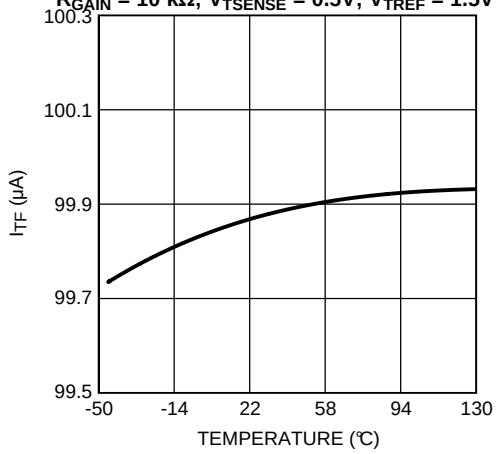


Figure 15.

f_{SW} vs. R_T

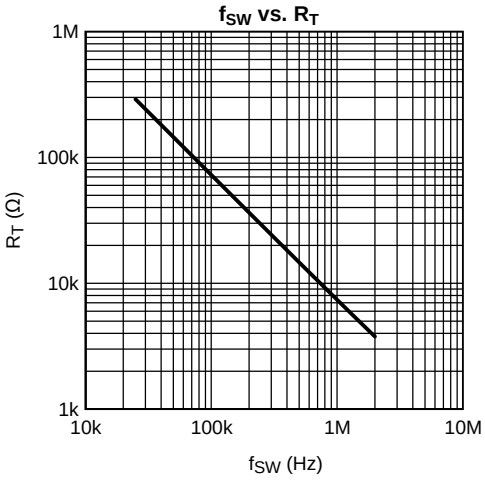


Figure 16.

Ideal Thermal Foldback - Varied Slope
R_{REF1} = R_{REF2} = 49.9 kΩ; R_{NTC-BK} = R_{BIAS} = 43.2 kΩ

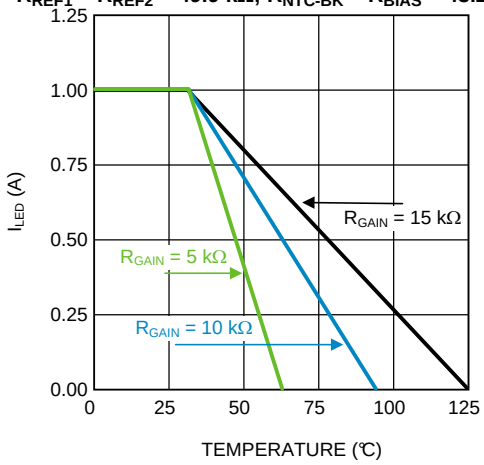


Figure 17.

Ideal Thermal Foldback - Varied Breakpoint
R_{REF1} = R_{REF2} = 49.9 kΩ; R_{GAIN} = 10 kΩ

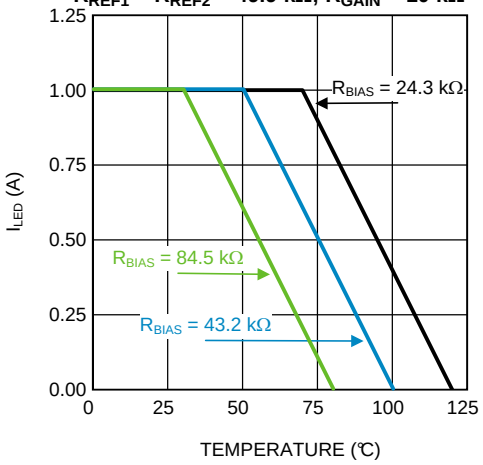
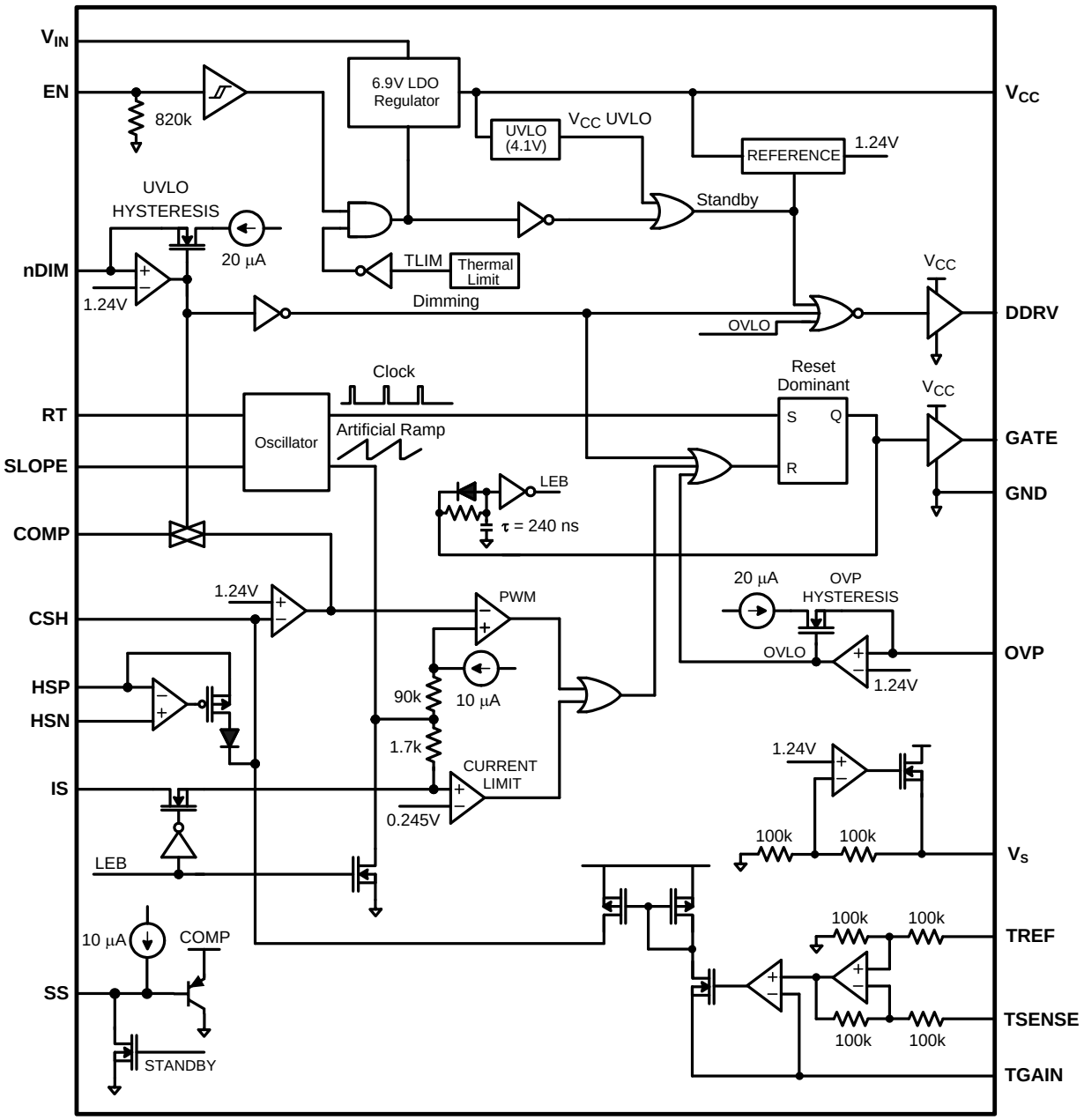


Figure 18.

BLOCK DIAGRAM



THEORY OF OPERATION

The LM3424 is an N-channel MosFET (NFET) controller for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency. The LM3424 uses peak current mode control providing good noise immunity and an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the thermal foldback circuitry allows for precise temperature management of the LEDs. Tthe output enable/disable function coupled with an internal dimming drive circuit provides high speed PWM dimming through the use of an external MosFET placed at the LED load. When designing, the maximum attainable LED current is not internally limited because the LM3424 is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM3424 to easily provide constant currents up to 5A. This simple controller contains all the features necessary to implement a high efficiency versatile LED driver.

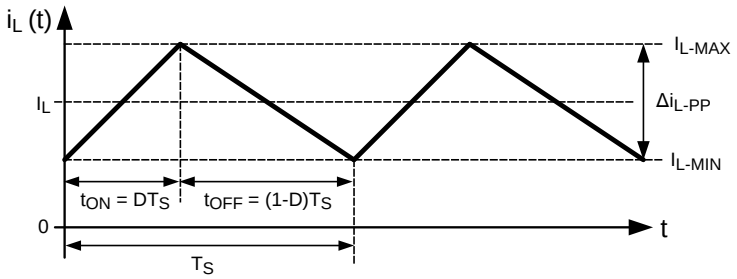


Figure 19. Ideal CCM Regulator Inductor Current $i_L(t)$

CURRENT REGULATORS

Current regulators can be designed to accomplish three basic functions: buck, boost, and buck-boost. All three topologies in their most basic form contain a main switching MosFET, a recirculating diode, an inductor and capacitors. The LM3424 is designed to drive a ground referenced NFET which is perfect for a standard boost regulator. Buck and buck-boost regulators, on the other hand, usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch can be used to drive a floating load instead. The LM3424 can then be used to drive all three basic topologies as shown in the Basic Topology Schematics section. Other topologies such as the SEPIC and flyback converter (both derivatives of the buck-boost) can be implemented as well.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the NFET (Q1) is turned on (t_{ON}), the input voltage source stores energy in the inductor (L1) while the output capacitor (C_O) provides energy to the LED load. When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both C_O and the LED load. Figure 19 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

The average output LED current (I_{LED}) is proportional to the average inductor current (I_L) , therefore if I_L is tightly controlled, I_{LED} will be well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate I_L and ultimately I_{LED}. For any current regulator, D is a function of the conversion ratio:

Buck

$$D = \frac{V_O}{V_{IN}} \quad (1)$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \quad (2)$$

Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \quad (3)$$

PEAK CURRENT MODE CONTROL

Peak current mode control is used by the LM3424 to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MosFET path or the MosFET R_{DS-ON} for both cycle-by-cycle current limit and input voltage feed forward. The controller has a fixed switching frequency set by an internal programmable oscillator which means current mode instability can occur at duty cycles higher than 50%. To mitigate this standard problem, an aritifical ramp is added to the control signal internally. The slope of this ramp is programmable to allow for a wider range of component choices for a given design. A detailed explanation of this control method is presented in the following sections.

SWITCHING FREQUENCY

The switching frequency of the LM3424 is programmed using an external resistor (R_T) connected from the RT pin to GND as shown in Figure 20.

Alternatively, an external PWM signal can be applied to the RT pin through a filter (R_{FLT} and C_{FLT}) and an AC coupling capacitor (C_{AC}) to synchronize the part to an external clock as shown in Figure 20. If the external PWM signal is applied at a frequency higher than the base frequency set by the R_T resistor, the internal oscillator is bypassed and the switching frequency becomes the synchronized frequency. The external synchronization signal should have a pulse width of 100ns, an amplitude between 3V and 6V, and be AC coupled to the RT pin with a ceramic capacitor (C_{AC} = 100pF). A 10MHz RC filter (R_{FLT} = 150Ω and C_{FLT} = 100 pF) should be placed between the PWM signal and C_{AC} to eliminate unwanted high frequency noise from coupling into the RT pin.

The switching frequency is defined:

$$f_{SW} = \frac{1}{1.40e^{-10} \times R_T - 1.95e^{-8}} \quad (4)$$

See the Typical Performance Characteristics section for a plot of R_T vs. f_{SW}.

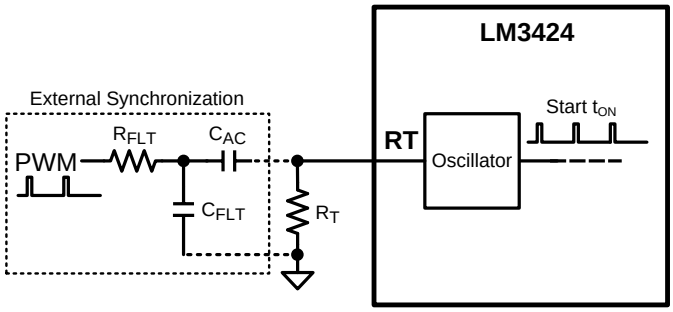


Figure 20. Timing Circuitry

AVERAGE LED CURRENT

To first understand how the LM3424 regulates LED current, the thermal foldback functionality will be ignored. Figure 21 shows the physical implementation of the LED current sense circuitry assuming the thermal foldback circuitry is a simple current source which, for now, will be set to zero (I_{TF} = 0A). The LM3424 uses an external current sense resistor (R_{SNS}) placed in series with the LED load to convert the LED current (I_{LED}) into a voltage (V_{SNS}). The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential (V_{HSP}=V_{HSN}) through negative feedback. Because of this, the V_{SNS} voltage is forced across R_{HSP} which generates a current that is summed with the thermal foldback current (I_{TF}) to generate the signal current (I_{CSH}) which flows out of the CSH pin and through the R_{CSH} resistor. The error amplifier will regulate the CSH pin to 1.24V and assuming I_{TF} = 0A, I_{CSH} can be calculated:

$$I_{CSH} = \frac{V_{SNS}}{R_{HSP}} \quad (5)$$

This means V_{SNS} will be regulated as follows:

$$V_{SNS} = 1.24V \times \frac{R_{HSP}}{R_{CSH}} \quad (6)$$

I_{LED} can then be calculated:

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{1.24V}{R_{SNS}} \times \frac{R_{HSP}}{R_{CSH}} \quad (7)$$

The selection of the three resistors (R_{SNS}, R_{CSH}, and R_{HSP}) is not arbitrary. For matching and noise performance, the suggested signal current I_{CSH} is approximately 100 µA. This current does not flow in the LEDs and will not affect either the off-state LED current or the regulated LED current. I_{CSH} can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum V_{SNS} is suggested to be 50 mV. Finally, a resistor (R_{HSN} = R_{HSP}) should be placed in series with the HSN pin to cancel out the effects of the input bias current (~10 µA) of both inputs of the high-side sense amplifier.

Note that he CSH pin can also be used as a low-side current sense input regulated to 1.24V. The high-side sense amplifier is disabled if HSP and HSN are tied to GND.

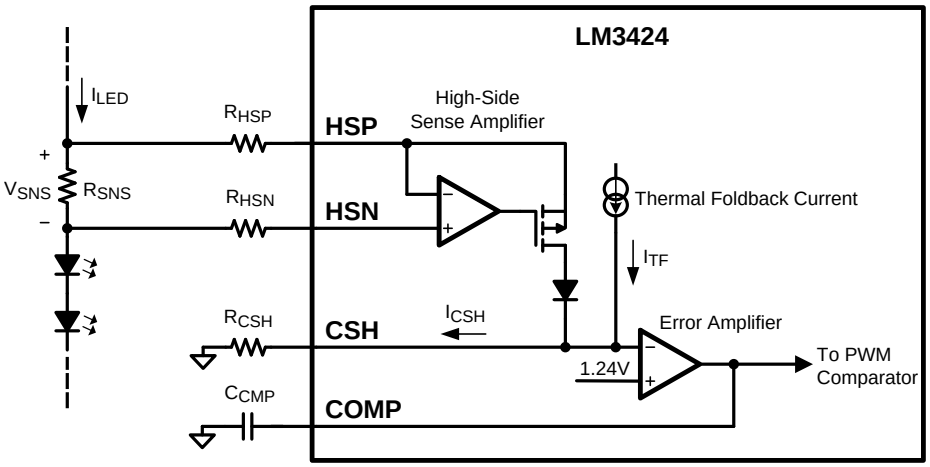


Figure 21. LED Current Sense Circuitry

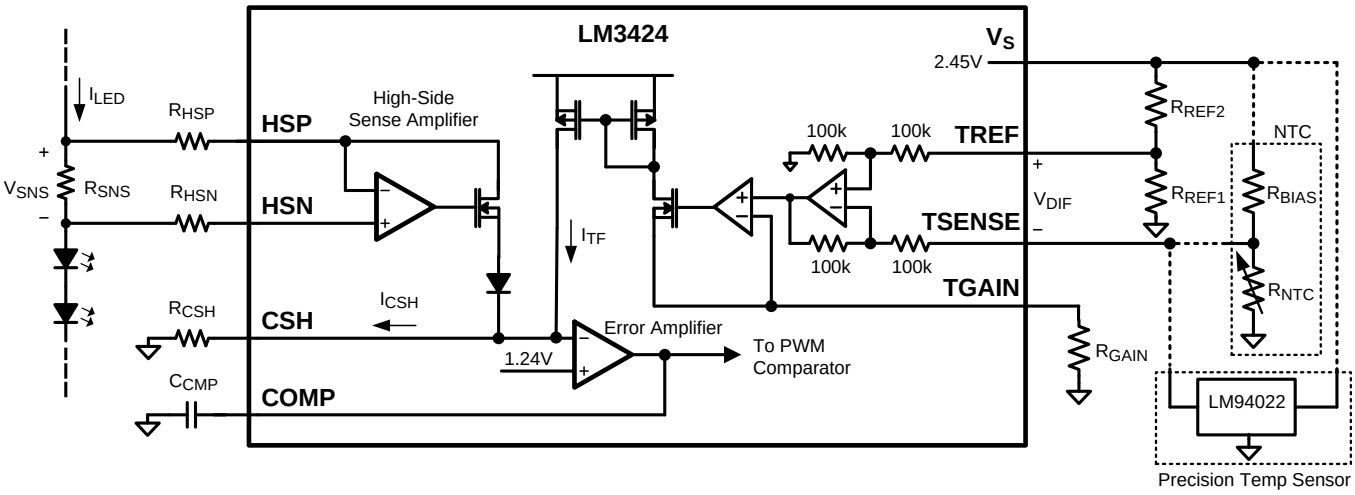


Figure 22. Thermal Foldback Circuitry

THERMAL FOLDBACK / ANALOG DIMMING

Thermal foldback is necessary in many applications due to the extreme temperatures created in LED environments. In general, two functions are necessary: a temperature breakpoint (T_{BK}) after which the nominal operating current needs to be reduced, and a slope corresponding to the amount of LED current decrease per temperature increase as shown in Figure 23. The LM3424 allows the user to program both the breakpoint and slope of the thermal foldback profile.

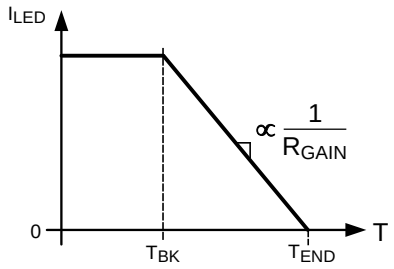


Figure 23. Ideal Thermal Foldback Profile

Foldback is accomplished by adding current (I_{TF}) to the CSH summing node. As more current is added, less current is needed from the high side amplifier and correspondingly, the LED current is regulated to a lower value. The final temperature (T_{END}) is reached when $I_{TF} = I_{CSH}$ causing no current to be needed from the high-side amplifier, yielding $I_{LED} = 0A$.

Figure 22 shows how the thermal foldback circuitry is physically implemented in the system. I_{TF} is set by placing a differential voltage ($V_{DIF} = V_{TREF} – V_{TSENSE}$) across TSENSE and TREF. V_{TREF} can be set with a simple resistor divider (R_{REF1} and R_{REF2}) supplied from the V_S voltage reference (typical 2.45V). V_{TSENSE} is set with a temperature dependant voltage (as temperature increases, voltage should decrease).

An NTC thermistor is the most cost effective device used to sense temperature. As the temperature of the thermistor increases, its resistance decreases (albeit non-linearly). Usually, the NTC manufacturer's datasheet will detail the resistance-temperature characteristic of the thermistor. The thermistor will have a different resistance (R_{NTC}) at each temperature. The nominal resistance of an NTC is the resistance when the temperature is 25°C (R_{25}) and in many datasheets this will be given a multiplier of 1. Then the resistance at a higher temperature will have a multiplier less than 1 (i.e. R_{85} multiplier is 0.161 therefore $R_{85} = 0.161 \times R_{25}$). Given a desired T_{BK} and T_{END}, the corresponding resistances at those temperatures (R_{NTC-BK} and $R_{NTC-END}$) can be found.

Using the NTC method, a resistor divider from V_S can be implemented with a resistor connected between V_S and TSENSE and the NTC thermistor placed at the desired location and connected from TSENSE to GND. This will ensure that the desired temperature-voltage characteristic occurs at TSENSE.

If a linear decrease over the foldback range is necessary, a precision temperature sensor such as the LM94022 can be used instead as shown in Figure 22. Either method can be used to set V_{TSENSE} according to the temperature. However, for the rest of this datasheet, the NTC method will be used for thermal foldback calculations.

During operation, if $V_{DIF} < 0V$, then the sensed temperature is less than T_{BK} and the differential sense amplifier will regulate its output to zero forcing $I_{TF} = 0$. This maintains the nominal LED current and no foldback is observed.

At T_{BK}, $V_{DIF} = 0V$ exactly and I_{TF} is still zero. Looking at the manufacturer's datasheet for the NTC thermistor, R_{NTC-BK} can be obtained for the desired T_{BK} and the voltage relationship at the breakpoint ($V_{TSENSE-BK} = V_{TREF}$) can be defined:

$$\frac{R_{REF1}}{R_{REF1} + R_{REF2}} = \frac{R_{NTC-BK}}{R_{NTC-BK} + R_{BIAS}} \tag{8}$$

A general rule of thumb is to set $R_{REF1} = R_{REF2}$ simplifying the breakpoint relationship to $R_{BIAS} = R_{NTC-BK}$.

If $V_{DIF} > 0V$ (temperature is above T_{BK}), then the amplifier will regulate its output equal to the input forcing V_{DIF} across the resistor (R_{GAIN}) connected from TGAIN to GND. R_{GAIN} ultimately sets the slope of the LED current decrease with respect to increasing temperature by changing I_{TF}:

$$I_{TF} = \frac{V_{TREF} - V_{TSENSE}}{R_{GAIN}} \tag{9}$$

If an analog temperature sensor such as the LM94022 is used, then R_{BIAS} and the NTC are not necessary and V_{TENSE} will be the direct voltage output of the sensor.

Since the NTC is not usually local to the controller, a bypass capacitor (C_{NTC}) is suggested from TSENSE to GND. If a capacitor is used at TSENSE, then a capacitor (C_{REF}) of equal or greater value should be placed from TREF to GND in order to ensure the controller does not start-up in foldback. Alternatively, a smaller C_{REF} can be used to create a fade-up function at start-up (see APPLICATIONS INFORMATION section).

Thermal foldback is simply analog dimming according to a specific profile, therefore any method of controlling the differential voltage between TREF and TSENSE can be use to analog dim the LED current. The corresponding LED current for any V_{DIF} > 0V is defined:

$$I_{LED} = (I_{CSH} - I_{TF}) \times \left(\frac{R_{HSP}}{R_{SNS}}\right) \quad (10)$$

The CSH pin can also be used to analog dim the LED current by adjusting the current sense voltage (V_{SNS}), similar to thermal foldback. There are several different methods to adjust V_{SNS} using the CSH pin:

1. External variable resistance : Adjust a potentiometer placed in series with R_{CSH} to vary V_{SNS}.
2. External variable current source: Source current (0 µA to I_{CSH}) into the CSH pin to adjust V_{SNS}.

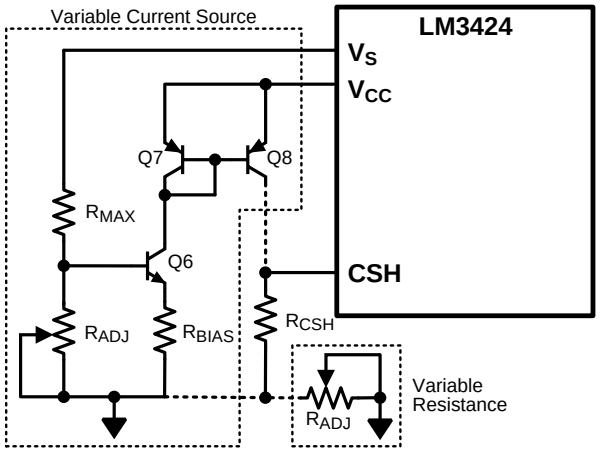


Figure 24. Analog Dimming Circuitry

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 24 shows how both CSH methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin since the potentiometer increases the size of the signal current loop.

Method 2 provides a complete dimming range and better noise performance, though it is more complex. Like thermal foldback, it simply sources current into the CSH pin, decreasing the amount of signal current that is necessary. This method consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer (R_{ADJ}), where R_{ADJ} controls the amount of current sourced into the CSH pin. A higher resistance value will source more current into the CSH pin causing less regulated signal current through R_{HSP}, effectively dimming the LEDs. Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current (I_{ADD}) sourced into the CSH pin can be calculated:

$$I_{ADD} = \frac{\left(\frac{R_{ADJ} \times V_{REF}}{R_{ADJ} + R_{MAX}}\right) - V_{BE\text{-}Q6}}{R_{BIAS}} \quad (11)$$

The corresponding I_{LED} for a specific I_{ADD} is:

$$I_{LED} = (I_{CSH} - I_{ADD}) \times \left(\frac{R_{HSP}}{R_{SNS}}\right) \quad (12)$$

THERMAL SHUTDOWN

The LM3424 includes thermal shutdown. If the die temperature reaches approximately 165°C the device will shut down (GATE pin low), until it reaches approximately 140°C where it turns on again.

CURRENT SENSE/CURRENT LIMIT

The LM3424 achieves peak current mode control using a comparator that monitors the main MosFET (Q1) transistor current, comparing it with the COMP pin voltage as shown in Figure 25. Further, it incorporates a cycle-by-cycle over-current protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MosFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 240 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time (t_{ON-MIN}).

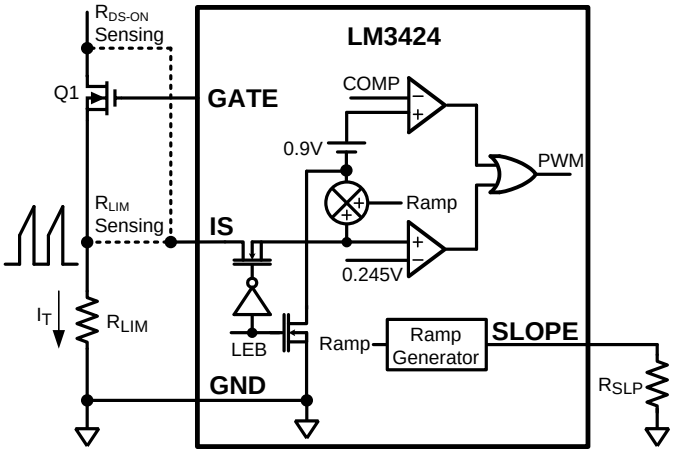


Figure 25. Current Sense / Current Limit Circuitry

There are two possible methods to sense the transistor current. The R_{DS-ON} of the main power MosFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MosFET is in the off state. Alternatively, a sense resistor located in the source of the MosFET may be used for current sensing, however a low inductance (ESL) type is suggested. The cycle-by-cycle current limit (I_{LIM}) can be calculated using either method as the limiting resistance (R_{LIM}):

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} \tag{13}$$

In general, the external series resistor allows for more design flexibility, however it is important to ensure all of the noise sensitive low power ground connections are connected together local to the controller and a single connection is made to GND.

SLOPE COMPENSATION

The LM3424 has programmable slope compensation in order to provide stability over a wide range of operating conditions. Without slope compensation, a well-known condition called current mode instability (or sub-harmonic oscillation) can result if there is a perturbation of the MosFET current sense voltage at the IS pin, due to noise or a some type of transient.

Through a mathematical / geometrical analysis of the inductor current (I_L) and the corresponding control current (I_C, it can be shown that if D < 0.5, the effect of the perturbation will decrease each switching cycle and the system will remain stable. However, if D > 0.5 then the perturbation will grow as shown in Figure 26, eventually causing a "period doubling" effect where the effect of the perturbation remains, yielding current mode instability.

Looking at Figure 25, the positive PWM comparator input is the IS voltage, a mirror of I_L during t_{ON}, plus a typical 900 mV offset. The negative input of the PWM comparator is the COMP pin which is proportional to I_C, the threshold at which the main MosFET (Q1) is turned off.

The LM3424 mitigates current mode instability by implementing an aritifical ramp (commonly called slope compensation) which is summed with the sensed MosFET current at the IS pin as shown in Figure 25. This combined signal is compared to the COMP pin to generate the PWM signal. An increase in the ramp that is added to the sense voltage will increase the maximum achievable duty cycle. It should be noted that as the artificial ramp is increased more and more, the control method approaches standard voltage mode control and the benefits of current mode control are reduced.

To program the slope compensation, an external resistor, R_{SLP}, is connected from SLOPE to GND. This sets the slope of the artificial ramp that is added to the MosFET current sense voltage. A smaller R_{SLP} value will increase the slope of the added ramp. A simple calculation is suggested to ensure any duty cycle is attainable while preventing the addition of excessive ramp. This method requires the artifical ramp slope (M_A) to be equal to half the inductor slope during t_{OFF}:

$$M_A = \frac{7.5e^{12}}{R_T \times R_{SLP} \times R_{SNS}} = \frac{V_O}{2 \times L1} \quad (14)$$

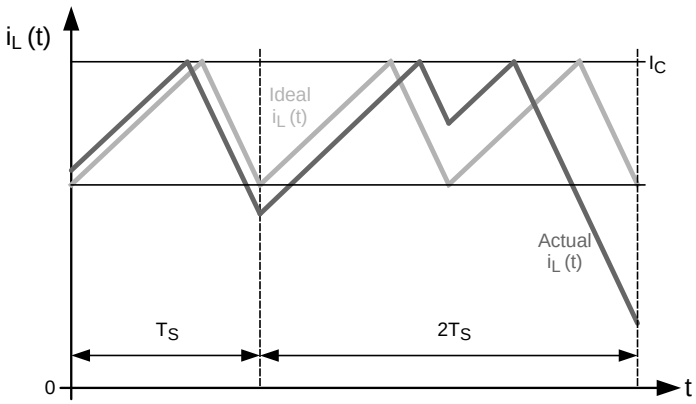


Figure 26. "Period Doubling" due to Current Mode Instability

CONTROL LOOP COMPENSATION

The LM3424 control loop is modeled like any current mode controller. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high frequency pole in the model, however it is near the switching frequency and plays no part in the compensation design process therefore it will be neglected. Since ceramic capacitance is recommended for use with LED drivers due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. Finally, there is a DC gain of the uncompensated loop which is dependent on internal controller gains and the external sensing network.

A buck-boost regulator will be used as an example case. See the Design Guide section for compensation of all topologies.

The uncompensated loop gain for a buck-boost regulator is given by the following equation:

$$T_U = T_{U0} \times \frac{\left(1 - \frac{S}{\omega_{Z1}}\right)}{\left(1 + \frac{S}{\omega_{P1}}\right)} \quad (15)$$

Where the uncompensated DC loop gain of the system is described as:

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \quad (16)$$

And the output pole (ω_{P1}) is approximated:

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \quad (17)$$

And the right half plane zero (ω_{Z1}) is:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \quad (18)$$

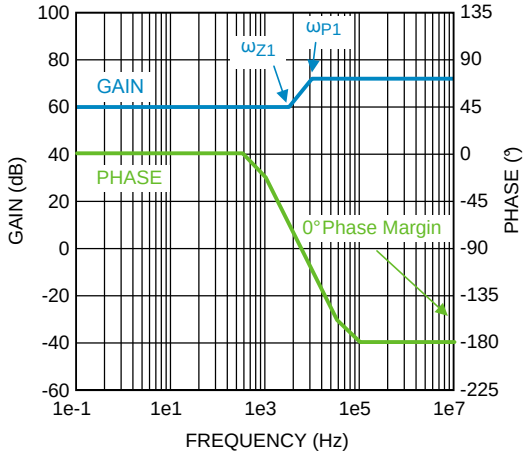


Figure 27. Uncompensated Loop Gain Frequency Response

Figure 27 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while loosing 45°/decade of phase which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high frequency pole (not modeled or shown in figure). The phase will be below -180° at the crossover frequency which means there is no phase margin (180° + phase at crossover frequency) causing system instability. Even if the output pole is below the RHP zero, the phase will still reach -180° before the crossover frequency in most cases yielding instability.

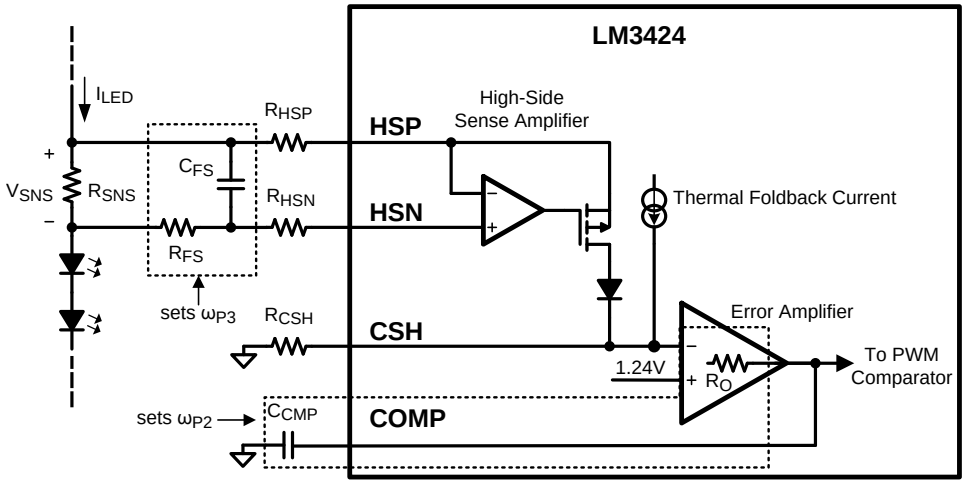


Figure 28. Compensation Circuitry

To mitigate this problem, a compensator should be designed to give adequate phase margin (above 45°) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin (C_{CMP}) will add a dominant pole to the system, which will ensure adequate phase margin if placed low enough. At high duty cycles (as shown in Figure 27), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach.

The dominant compensation pole (ω_{P2}) is determined by C_{CMP} and the output resistance (R_O) of the error amplifier (typically 5 MΩ):

$$\omega_{P2} = \frac{1}{5e^6 \Omega \times C_{CMP}} \quad (19)$$

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate switching noise and, in some cases, provide better gain margin. This pole can be placed across R_{SNS} to filter the ESL of the sense resistor at the same time. Figure 28 shows how the compensation is physically implemented in the system.

The high frequency pole (ω_{P3}) can be calculated:

$$\omega_{P3} = \frac{1}{R_{FS} \times C_{FS}} \quad (20)$$

The total system transfer function becomes:

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (21)$$

The resulting compensated loop gain frequency response shown in Figure 29 indicates that the system has adequate phase margin (above 45°) if the dominant compensation pole is placed low enough, ensuring stability:

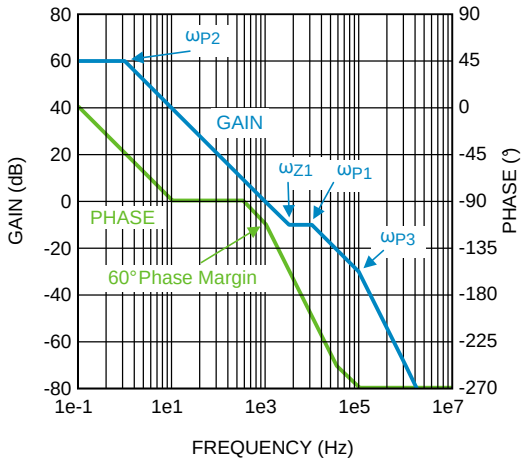


Figure 29. Compensated Loop Gain Frequency Response

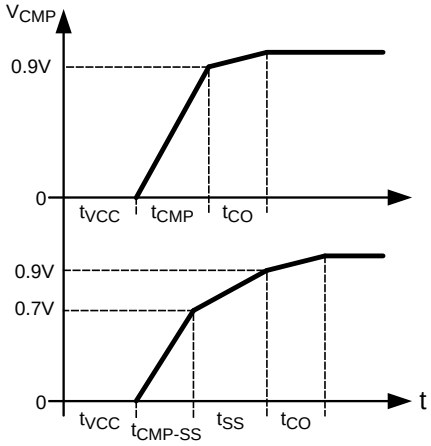


Figure 30. Start-up Waveforms

START-UP REGULATOR and SOFT-START

The LM3424 includes a high voltage, low dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor (C_{BYP}) connected to the V_{CC} pin. The recommended bypass capacitance for the V_{CC} regulator is 2.2 µF to 3.3 µF. The output of the V_{CC} regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited.

The LM3424 also has programmable soft-start, set by an external capacitor (C_{SS}), connected from SS to GND. For C_{SS} to affect start-up, $C_{REF} > C_{NTC}$ must be maintained so that the converter does not start in foldback mode. Figure 30 shows the typical start-up waveforms for the LM3424 assuming $C_{REF} > C_{NTC}$.

First, C_{BYP} is charged to be above V_{CC} UVLO threshold (~4.2V). The C_{VCC} charging time (t_{VCC}) can be estimated as:

$$t_{VCC} = \frac{4.2V}{25\ mA} \times C_{BYP} = 168\Omega \times C_{BYP} \quad (22)$$

Assuming there is no C_{SS} or if C_{SS} is less than 40% of C_{CMP} , C_{CMP} is then charged to 0.9V over the charging time (t_{CMP}) which can be estimated as:

$$t_{CMP} = \frac{0.9V}{25\ \mu A} \times C_{CMP} = 36\ k\Omega \times C_{CMP} \quad (23)$$

Once C_{CMP} = 0.9V, the part starts switching to charge C_O until the LED current is in regulation. The C_O charging time (t_{CO}) can be roughly estimated as:

$$t_{CO} = C_O \times \frac{V_O}{I_{LED}} \quad (24)$$

If C_{SS} is greater than 40% of C_{CMP}, the compensation capacitor will only charge to 0.7V over a smaller C_{CMP} charging time ($t_{CMP\text{-}SS}$) which can be estimated as:

$$t_{CMP\text{-}SS} = \frac{0.70V}{25\ \mu A} \times C_{CMP} = 28\ k\Omega \times C_{CMP} \quad (25)$$

Then COMP will clamp to SS, forcing COMP to rise (the last 200 mV before switching begins) according to the C_{SS} charging time (t_{SS}) which can be estimated as:

$$t_{SS} = \frac{0.2V}{10\ \mu A} \times C_{SS} = 20\ k\Omega \times C_{SS} \quad (26)$$

The system start-up time (t_{SU} or $t_{SU\text{-}SS}$) is defined as:

$C_{SS} < 0.4 \times C_{CMP}$

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \quad (27)$$

$C_{SS} > 0.4 \times C_{CMP}$

$$t_{SU\text{-}SS} = t_{VCC} + t_{CMP\text{-}SS} + t_{SS} + t_{CO} \quad (28)$$

As a general rule of thumb, standard smooth startup operation can be achieved with $C_{SS} = C_{CMP}$.

OVER-VOLTAGE LOCKOUT (OVLO)

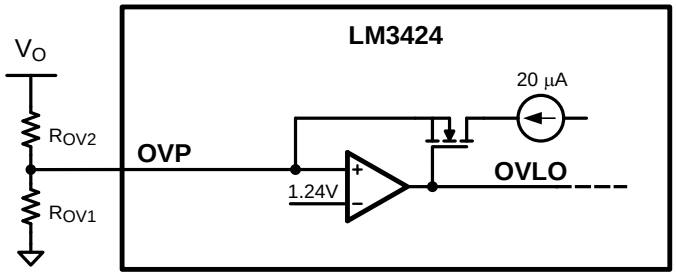


Figure 31. Over-Voltage Protection Circuitry

The LM3424 can be configured to detect an output (or input) over-voltage condition via the OVP pin. The pin features a precision 1.24V threshold with 20 µA (typical) of hysteresis current as shown in Figure 31. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 20 µA current source provides hysteresis to the lower threshold of the OVLO hysteretic band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage (V_O) should be sensed and translated to ground by using a single PNP as shown in Figure 32.

The over-voltage turn-off threshold ($V_{TURN-OFF}$) is defined:

Ground Referenced

$$V_{TURN-OFF} = 1.24V \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right) \quad (29)$$

Floating

$$V_{TURN-OFF} = 1.24V \times \left(\frac{0.5 \times R_{OV1} + R_{OV2}}{R_{OV1}} \right) \quad (30)$$

In the ground referenced configuration, the voltage across R_{OV2} is V_O - 1.24V whereas in the floating configuration it is V_O - 620 mV where 620 mV approximates V_{BE} of the PNP.

The over-voltage hysteresis (V_{HYSO}) is defined:

$$V_{HYSO} = 20\ \mu A \times R_{OV2} \quad (31)$$

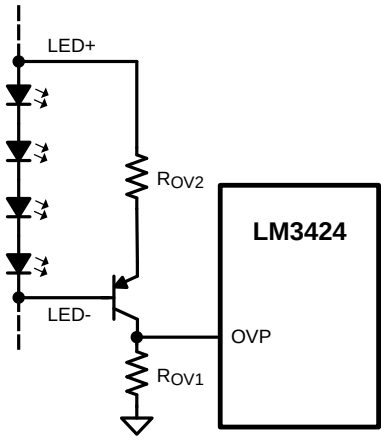


Figure 32. Floating Output OVP Circuitry

INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24V threshold with programmable hysteresis as shown in Figure 33. This pin functions as both the PWM dimming input for the LEDs and as a V_{IN} UVLO. When the pin voltage rises and exceeds the 1.24V threshold, 20 µA (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

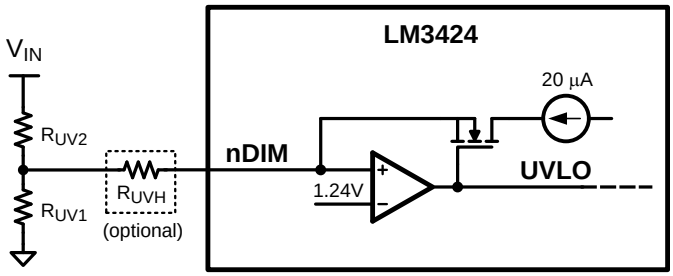


Figure 33. UVLO Circuit

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pull-down MosFET at the nDIM pin (see PWM DIMMING section). In general, at least 3V of hysteresis is preferable when PWM dimming, if operating near the UVLO threshold.

The turn-on threshold ($V_{TURN-ON}$) is defined as follows:

$$V_{TURN\ ON} = 1.24V \times \left(\frac{R_{UV1} + R_{UV2}}{R_{UV1}}\right) \quad (32)$$

The hysteresis (V_{HYS}) is defined as follows:

UVLO only

$$V_{HYS} = 20\,\mu A \times R_{UV2} \quad (33)$$

PWM dimming and UVLO

$$V_{HYS} = 20\,\mu A \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}}\right) \quad (34)$$

PWM DIMMING

The active low nDIM pin can be driven with a PWM signal which controls the main NFET and the dimming FET (dimFET). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, (i.e. 30% duty cycle ~ 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a V_{IN} UVLO input as described in the INPUT UNDER-VOLTAGE LOCKOUT (UVLO) section or by tying it directly to V_{CC} or V_{IN}.

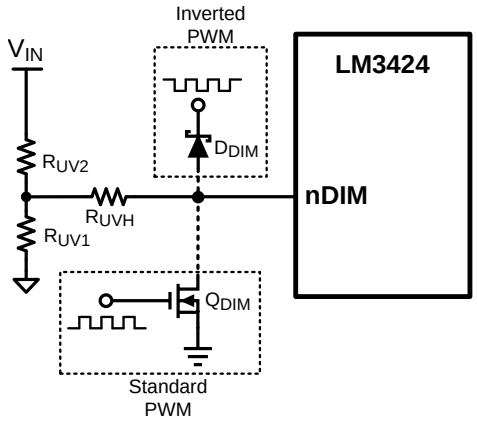


Figure 34. PWM Dimming Circuit

Figure 34 shows how the PWM signal is applied to nDIM:

1. Connect the dimming MosFET (Q_{DIM}) with the drain to the nDIM pin and the source to GND. Apply an external logic-level PWM signal to the gate of Q_{DIM}.
2. Connect the anode of a Schottky diode (D_{DIM}) to the nDIM pin. Apply an inverted external logic-level PWM signal to the cathode of the same diode.

The DDRV pin is a PWM output that follows the nDIM PWM input signal. When the nDIM pin rises, the DDRV pin rises and the PWM latch reset signal is removed allowing the main MosFET Q1 to turn on at the beginning of the next clock set pulse. In boost and buck-boost topologies, the DDRV pin is used to control a N-channel MosFET placed in series with the LED load, while it would control a P-channel MosFET in parallel with the load for a buck topology.

The series dimFET will open the LED load, when nDIM is low, effectively speeding up the rise and fall times of the LED current. Without any dimFET, the rise and fall times are limited by the inductor slew rate and dimming frequencies above 1 kHz are impractical. Using the series dimFET, dimming frequencies up to 30 kHz are achievable. With a parallel dimFET (buck topology), even higher dimming frequencies are achievable.

When using the PWM functionality in a boost regulator, the PWM signal drives a ground referenced FET. However, with buck-boost and buck topologies, level shifting circuitry is necessary to translate the PWM dim signal to the floating dimFET as shown in Figure 35 and Figure 36.

When using a series dimFET to PWM dim the LED current, more output capacitance is always better. A general rule of thumb is to use a minimum of 40 µF when PWM dimming. For most applications, this will provide adequate energy storage at the output when the dimFET turns off and opens the LED load. Then when the dimFET is turned back on, the capacitance helps source current into the load, improving the LED current rise time.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the minimum dimming pulse length in seconds (t_{PULSE}) is:

$$t_{PULSE} = \frac{2 \times I_{LED} \times V_O \times L1}{V_{IN}^2} \quad (35)$$

Even maintaining a dimming pulse greater than t_{PULSE}, preserving linearity at low dimming duty cycles is difficult. Several modifications are suggested for applications requiring low dimming duty cycles. Since nDIM rising releases the latch but does not trigger the on-time specifically, there will be an effective jitter on the rising edge of the LED current. This jitter can be easily removed by tying the PWM input signal through the synchronization network at the RT pin (shown in Figure 20), forcing the on-time to synchronize with the nDIM pulse.

The second helpful modification is to remove the C_{FS} capacitor and R_{FS} resistor, eliminating the high frequency compensation pole. This should not affect stability, but it will speed up the response of the CSH pin, specifically at the rising edge of the LED current when PWM dimming, thus improving the achievable linearity at low dimming duty cycles.

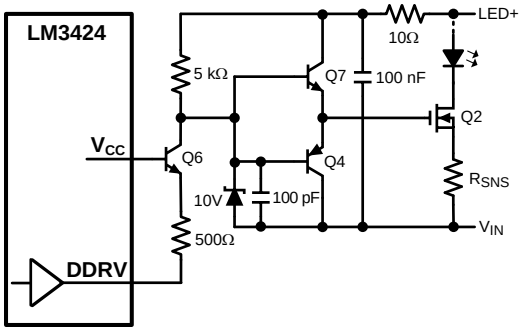


Figure 35. Buck-boost Level-Shifted PWM Circuit

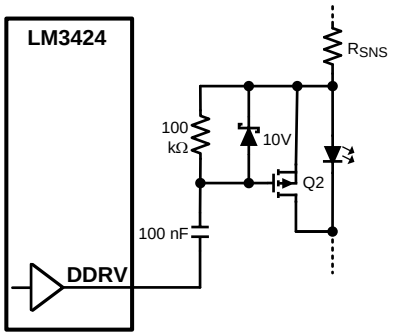


Figure 36. Buck Level-Shifted PWM Circuit

Design Considerations

This section describes the application level considerations when designing with the LM3424. For corresponding calculations, refer to the Design Guide section.

INDUCTOR

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transferred to the load in different ways (as an example, buck-boost operation is detailed in the CURRENT REGULATORS section). The size of the inductor, the voltage across it, and the length of the switching subinterval (t_{ON} or t_{OFF}) determines the inductor current ripple ($\Delta i_{L\text{-}PP}$). In the design process, L1 is chosen to provide a desired $\Delta i_{L\text{-}PP}$. For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore $\Delta i_{L\text{-}PP}$ is basically equal to the LED ripple current $\Delta i_{LED\text{-}PP}$. However, for boost and buck-boost regulators, there is always an output capacitor which reduces $\Delta i_{LED\text{-}PP}$, therefore the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.

In general, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current (I_{LED}). Therefore, for the buck regulator with no output capacitance, $\Delta i_{L\text{-}PP}$ should also be less than 40% of I_{LED}. For the boost and buck-boost topologies, $\Delta i_{L\text{-}PP}$ can be much higher depending on the output capacitance value. However, $\Delta i_{L\text{-}PP}$ is suggested to be less than 100% of the average inductor current (I_L) to limit the RMS inductor current.

L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ($I_{L\text{-}RMS}$).

LED DYNAMIC RESISTANCE

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus R_{SNS}. LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED (V_{LED}) by the forward current (I_{LED}) leads to an incorrect calculation of the dynamic resistance of a single LED (r_{LED}). The result can be 5 to 10 times higher than the true r_{LED} value.

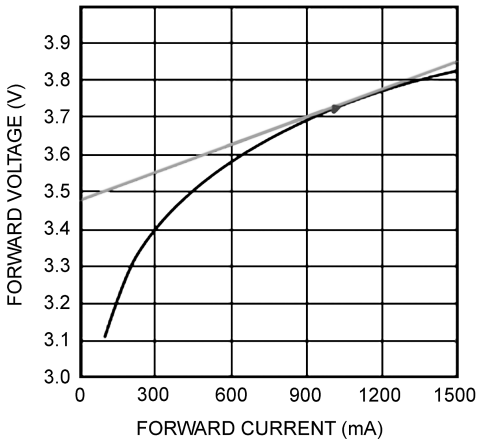


Figure 37. Dynamic Resistance

Obtaining r_{LED} is accomplished by referring to the manufacturer's LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 37. For any application with more than 2 series LEDs, R_{SNS} can be neglected allowing r_D to be approximated as the number of LEDs multiplied by r_{LED}.

OUTPUT CAPACITOR

For boost and buck-boost regulators, the output capacitor (C_O) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple ($\Delta i_{LED\text{-}PP}$) below the inductor current ripple ($\Delta i_{L\text{-}PP}$). In all cases, C_O is sized to provide a desired $\Delta i_{LED\text{-}PP}$. As mentioned in the INDUCTOR section, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current ($I_{LED\text{-}PP}$).

C_O should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

INPUT CAPACITORS

The input capacitance (C_{IN}) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators, C_{IN} provides energy during t_{ON} and during t_{OFF}, the input voltage source charges up C_{IN} with the average input current (I_{IN}). For boost regulators, C_{IN} only needs to provide the ripple current due to the direct connection to the inductor. C_{IN} is selected given the maximum input voltage ripple (Δv_{IN-PP}) which can be tolerated. Δv_{IN-PP} is suggested to be less than 10% of the input voltage (V_{IN}).

An input capacitance at least 100% greater than the calculated C_{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transistion of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

For most applications, it is recommended to bypass the V_{IN} pin will an 0.1 µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the LM3424 device, a 10 Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150 kHz filter to eliminate undesired high frequency noise.

MAIN MosFET / DIMMING MosFET

The LM3424 requires an external NFET (Q1) as the main power MosFET for the switching regulator. Q1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the NFET on-resistance (R_{DS-ON}).

When PWM dimming, the LM3424 requires another MosFET (Q2) placed in series (or parallel for a buck regulator) with the LED load. This MosFET should have a voltage rating equal to the output voltage (V_O) and a current rating at least 10% higher than the nominal LED current (I_{LED}) . The power rating is simply V_O multiplied by I_{LED}, assuming 100% dimming duty cycle (continuous operation) will occur.

In general, the NFETs should be chosen to minimize total gate charge (Q_g) when f_{SW} is high and minimize R_{DS-ON} otherwise. This will minimize the dominant power losses in the system. Frequently, higher current NFETs in larger packages are chosen for better thermal performance.

RE-CIRCULATING DIODE

A re-circulating diode (D1) is required to carry the inductor current during t_{OFF}. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product datasheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

CIRCUIT LAYOUT

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximimize noise rejection and minimize the generation of EMI within the circuit.

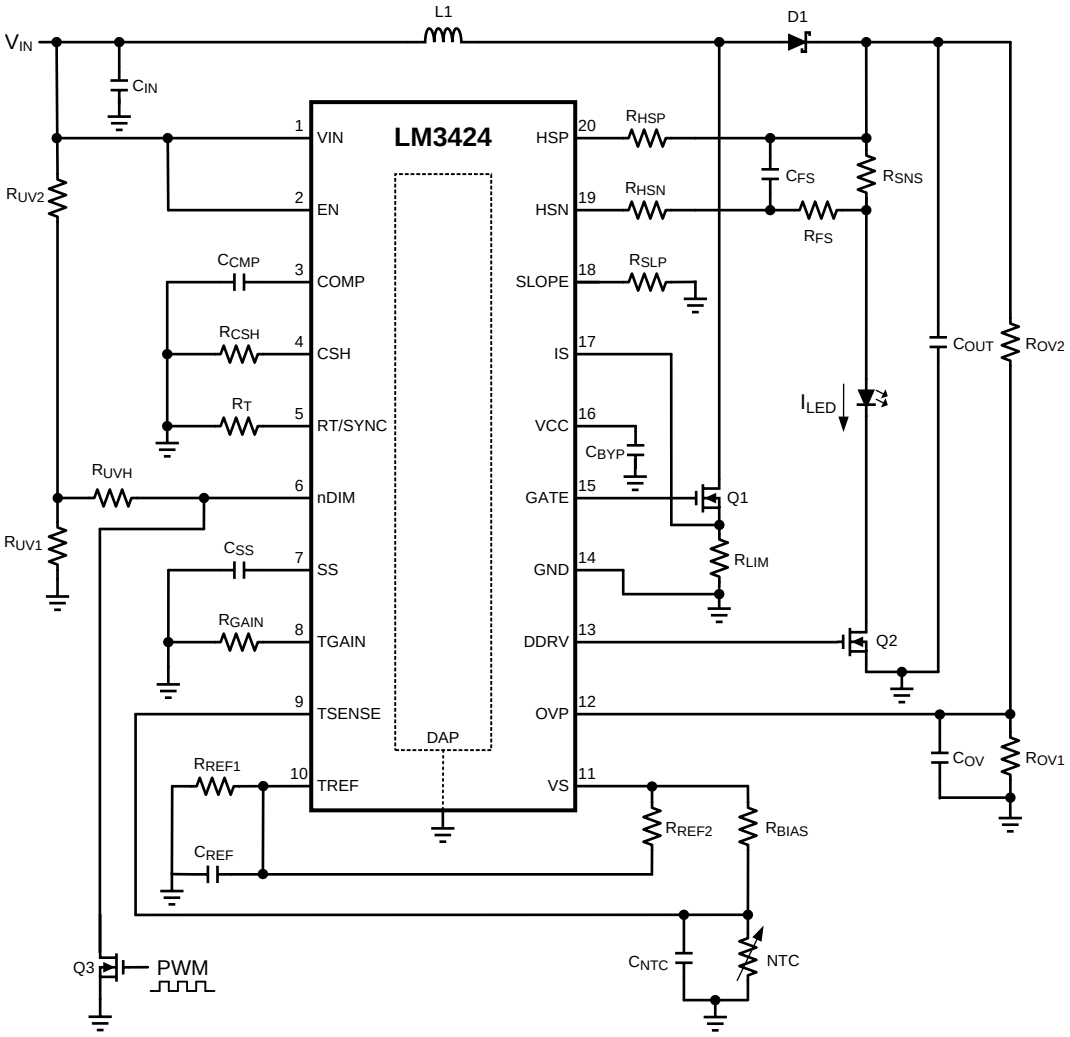
Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM3424 buck regulator contains the input capacitor (C_{IN}), the recirculating diode (D1), the N-channel MosFET (Q1), and the sense resistor (R_{LIM}). In the LM3424 boost regulator, the discontinuous current flows through the output capacitor (C_O), D1, Q1, and R_{LIM}. In the buck-boost regulator both loops are discontinuous and should be carefully layed out. These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RT, COMP, CSH, IS, TSENSE, TREF, HSP and HSN pins are all high-impedance inputs which couple external noise easily, therefore the loops containing these nodes should be minimized whenever possible.

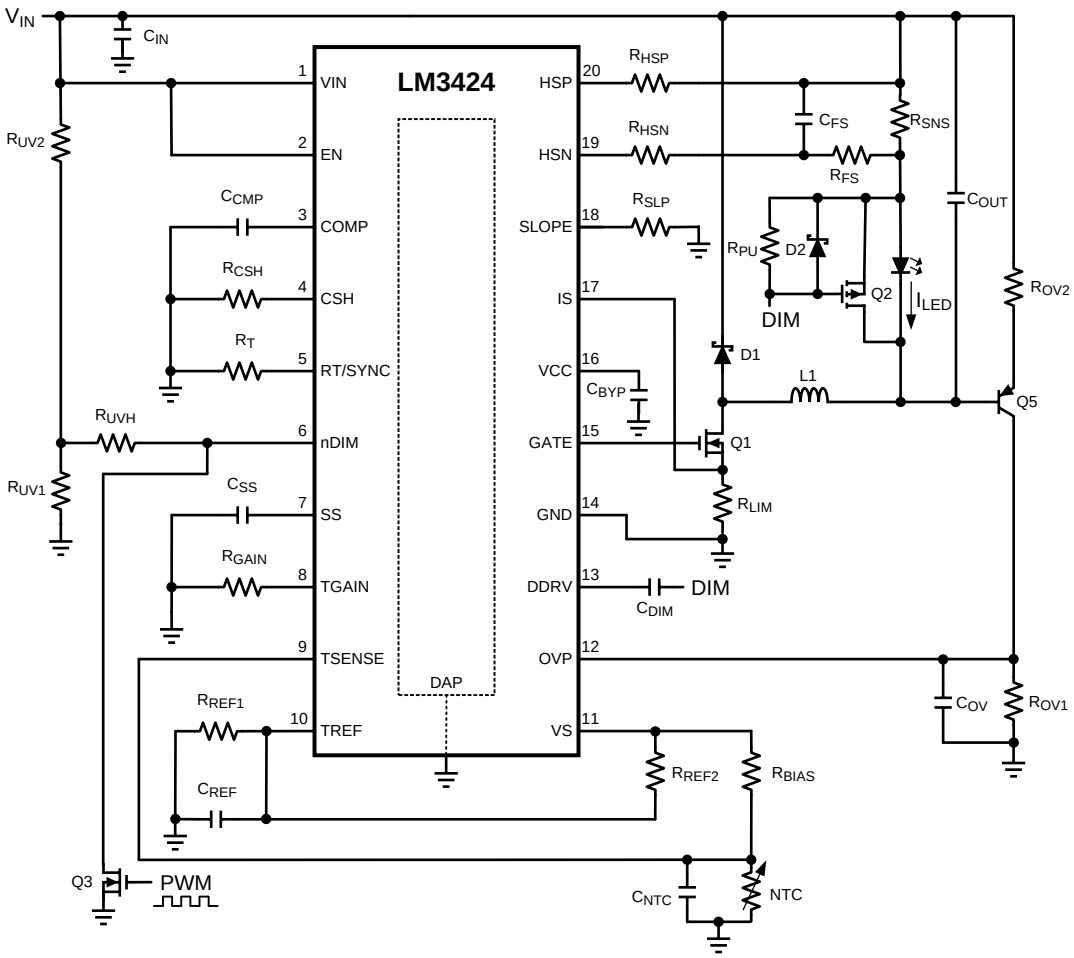
In some applications the LED or LED array can be far away (several inches or more) from the LM3424, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

Basic Topology Schematics

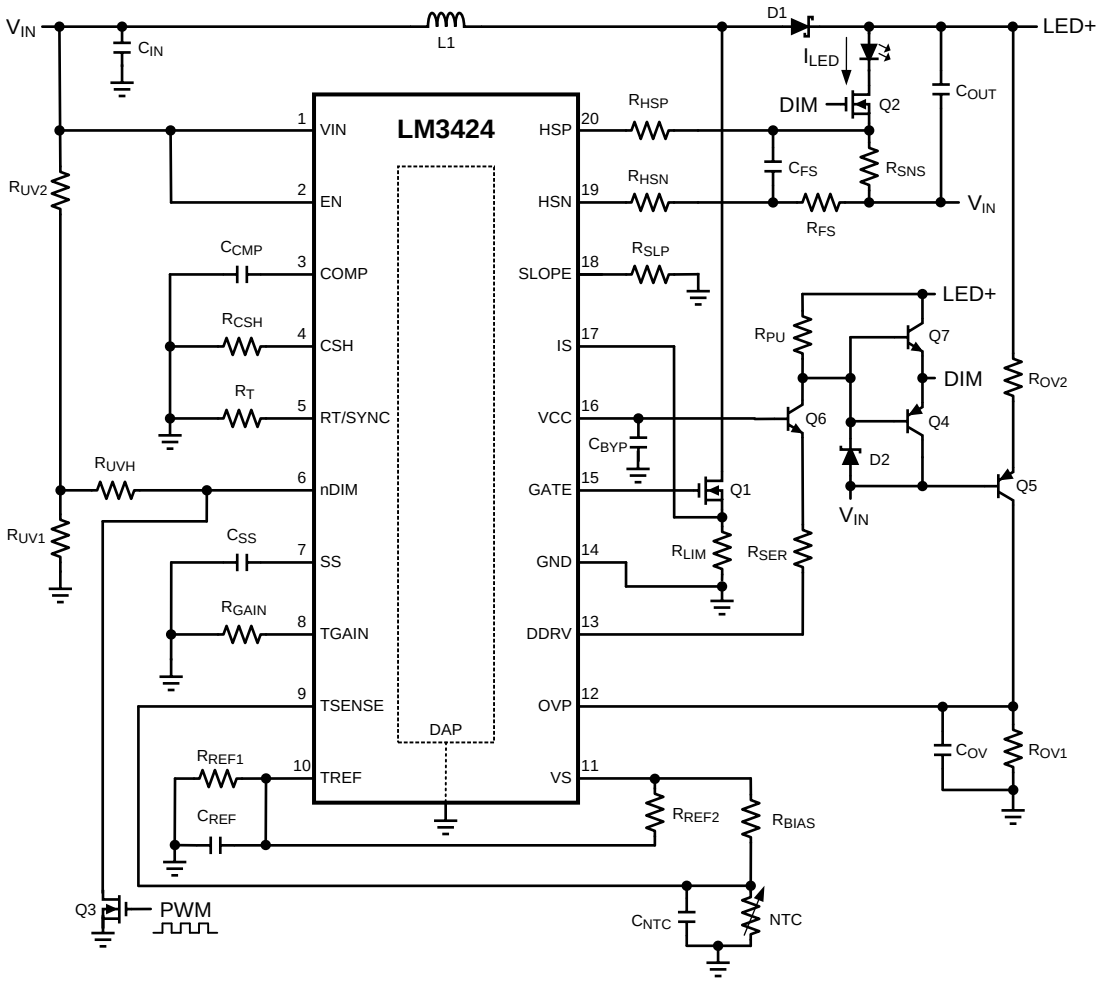
BOOST REGULATOR ($V_{IN} < V_O$)



BUCK REGULATOR (V_{IN} > V_O)



BUCK-BOOST REGULATOR



Design Guide

Refer to Basic Topology Schematics section.

SPECIFICATIONS

Number of series LEDs: N

Single LED forward voltage: V_{LED}

Single LED dynamic resistance: r_{LED}

Nominal input voltage: V_{IN}

Input voltage range: V_{IN-MAX}, V_{IN-MIN}

Switching frequency: f_{SW}

Current sense voltage: V_{SNS}

Average LED current: I_{LED}

Inductor current ripple: Δi_{L-PP}

LED current ripple: Δi_{LED-PP}

Peak current limit: I_{LIM}

Input voltage ripple: Δv_{IN-PP}

Output OVLO characteristics: $V_{TURN-OFF}$, V_{HYSO}

Input UVLO characteristics: $V_{TURN-ON}$, V_{HYS}

Thermal foldback characteristics: T_{BK}, T_{END}

Total start-up time: t_{TSU}

1. OPERATING POINT

Given the number of series LEDs (N), the forward voltage (V_{LED}) and dynamic resistance (r_{LED}) for a single LED, solve for the nominal output voltage (V_O) and the nominal LED string dynamic resistance (r_D):

$$V_O = N \times V_{LED} \tag{36}$$

$$r_D = N \times r_{LED} \tag{37}$$

Solve for the ideal nominal duty cycle (D):

Buck

$$D = \frac{V_O}{V_{IN}} \tag{38}$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \tag{39}$$

Buck-boost

$$D = \frac{V_O}{V_O + V_{IN}} \tag{40}$$

Using the same equations, find the minimum duty cycle (D_{MIN}) using maximum input voltage (V_{IN-MAX}) and the maximum duty cycle (D_{MAX}) using the minimum input voltage (V_{IN-MIN}). Also, remember that D' = 1 - D.

2. SWITCHING FREQUENCY

Set the switching frequency (f_{SW}) by solving for R_T:

$$R_T = \frac{1 + 1.95e^{-8} \times f_{SW}}{1.40e^{-10} \times f_{SW}} \tag{41}$$

3. AVERAGE LED CURRENT

For all topologies, set the average LED current (I_{LED}) knowing the desired current sense voltage (V_{SNS}) and solving for R_{SNS}:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} \tag{42}$$

If the calculated R_{SNS} is too far from a desired standard value, then V_{SNS} will have to be adjusted to obtain a standard value.

Setup the suggested signal current of 100 µA by assuming R_{CSH} = 12.4 kΩ and solving for R_{HSP}:

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} \tag{43}$$

If the calculated R_{HSP} is too far from a desired standard value, then R_{CSH} can be adjusted to obtain a standard value.

4. THERMAL FOLDBACK

For all topologies, set the thermal foldback breakpoint (T_{BK}) by finding corresponding R_{NTC-BK} from manufacturer's datasheet and solving for R_{BIAS}:

$$R_{BIAS} = R_{NTC-BK} \times \frac{R_{REF2}}{R_{REF1}} \tag{44}$$

The easiest approach is to set $R_{REF1} = R_{REF2}$, therefore setting $R_{BIAS} = R_{NTC-BK}$ will properly set T_{BK}. Remember, capacitance is recommended at the TSENSE and TREF pins, so ensure $C_{REF} > C_{NTC}$ to prevent start-up in foldback.

Then set the thermal foldback endpoint (T_{END}) by finding the corresponding $R_{NTC-END}$ from manufacturer's datasheet and solving for R_{GAIN}:

$$R_{GAIN} = \frac{\left(\frac{R_{REF1}}{R_{REF1}+R_{REF2}} - \frac{R_{NTC-END}}{R_{NTC-END}+R_{BIAS}}\right) \times 2.45V}{I_{CSH}} \tag{45}$$

5. INDUCTOR RIPPLE CURRENT

Set the nominal inductor ripple current (Δi_{L-PP}) by solving for the appropriate inductor (L1):

Buck

$$L1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L-PP} \times f_{SW}} \tag{46}$$

Boost and Buck-boost

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} \tag{47}$$

To set the worst case inductor ripple current, use V_{IN-MAX} and D_{MIN} when solving for L1.

The minimum allowable inductor RMS current rating (I_{L-RMS}) can be calculated as:

Buck

$$I_{L-RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L-PP}}{I_{LED}}\right)^2} \tag{48}$$

Boost and Buck-boost

$$I_{L-RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L-PP} \times D'}{I_{LED}}\right)^2} \tag{49}$$

6. LED RIPPLE CURRENT

Set the nominal LED ripple current (Δi_{LED-PP}), by solving for the output capacitance (C_O):

Buck

$$C_O = \frac{\Delta i_{L-PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED-PP}} \quad (50)$$

Boost and Buck-boost

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta\, i_{LED-PP} \times f_{SW}} \quad (51)$$

To set the worst case LED ripple current, use D_{MAX} when solving for C_O. Remember, when PWM dimming it is recommended to use a minimum of 40 µF of output capacitance to improve performance.

The minimum allowable RMS output capacitor current rating (I_{CO-RMS}) can be approximated:

Buck

$$I_{CO-RMS} = \frac{\Delta i_{LED-PP}}{\sqrt{12}} \quad (52)$$

Boost and Buck-boost

$$I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (53)$$

7. PEAK CURRENT LIMIT

Set the peak current limit (I_{LIM}) by solving for the transistor path sense resistor (R_{LIM}):

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} \quad (54)$$

8. SLOPE COMPENSATION

For all topologies, the preferred method to set slope compensation is to ensure any duty cycle is attainable for the nominal V_O and chosen L by solving for R_{SLP}:

$$R_{SLP} = \frac{1.5e^{13} \times L1}{V_O \times R_T \times R_{SNS}} \quad (55)$$

9. LOOP COMPENSATION

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain (T_U) of the regulator can be approximated:

Buck

$$T_U = T_{U0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad (56)$$

Boost and Buck-boost

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \quad (57)$$

Where the pole (ω_{P1}) is approximated:

Buck

$$\omega_{P1} = \frac{1}{r_D \times C_O} \quad (58)$$

Boost

$$\omega_{P1} = \frac{2}{r_D \times C_O} \quad (59)$$

Buck-boost

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \quad (60)$$

And the RHP zero (ω_{Z1}) is approximated:

Boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{L1} \quad (61)$$

Buck-boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \quad (62)$$

And the uncompensated DC loop gain (T_{U0}) is approximated:

Buck

$$T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \quad (63)$$

Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \quad (64)$$

Buck-boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \quad (65)$$

For all topologies, the primary method of compensation is to place a low frequency dominant pole (ω_{P2}) which will ensure that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor (C_{CMP}) from the COMP pin to GND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} \quad (66)$$

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5e^6} \quad (67)$$

If analog dimming is used, C_{CMP} should be approximately 4x larger to maintain stability as the LEDs are dimmed to zero.

A high frequency compensation pole (ω_{P3}) can be used to attenuate switching noise and provide better gain margin. Assuming R_{FS} = 10Ω, C_{FS} is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

$$\omega_{P3} = \max(\omega_{P1}, \omega_{Z1}) \times 10 \quad (68)$$

$$C_{FS} = \frac{1}{10 \times \omega_{P3}} \quad (69)$$

The total system loop gain (T) can then be written as:

Buck

$$T = T_{U0} \times \frac{1}{\left(1+\frac{s}{\omega_{P1}}\right) \times \left(1+\frac{s}{\omega_{P2}}\right) \times \left(1+\frac{s}{\omega_{P3}}\right)} \quad (70)$$

Boost and Buck-boost

$$T = T_{U0} \times \frac{\left(1-\frac{s}{\omega_{Z1}}\right)}{\left(1+\frac{s}{\omega_{P1}}\right) \times \left(1+\frac{s}{\omega_{P2}}\right) \times \left(1+\frac{s}{\omega_{P3}}\right)} \quad (71)$$

10. INPUT CAPACITANCE

Set the nominal input voltage ripple (Δv_{IN-PP}) by solving for the required capacitance (C_{IN}):

Buck

$$C_{IN} = \frac{I_{LED} \times (1 - D) \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (72)$$

Boost

$$C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} \quad (73)$$

Buck-boost

$$C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (74)$$

Use D_{MAX} to set the worst case input voltage ripple, when solving for C_{IN} in a buck-boost regulator and D_{MID} = 0.5 when solving for C_{IN} in a buck regulator.

The minimum allowable RMS input current rating ($I_{CIN-RMS}$) can be approximated:

Buck

$$I_{CIN-RMS} = I_{LED} \times \sqrt{D_{MID} \times (1-D_{MID})} \quad (75)$$

Boost

$$I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} \quad (76)$$

Buck-boost

$$I_{CIN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \quad (77)$$

11. NFET

The NFET voltage rating should be at least 15% higher than the maximum NFET drain-to-source voltage (V_{T-MAX}):

Buck

$$V_{T-MAX} = V_{IN-MAX} \quad (78)$$

Boost

$$V_{T-MAX} = V_O \quad (79)$$

Buck-boost

$$V_{T-MAX} = V_{IN-MAX} + V_O \quad (80)$$

The current rating should be at least 10% higher than the maximum average NFET current ($I_{T\text{-}MAX}$):

Buck

$$I_{T\text{-}MAX} = D_{MAX} \times I_{LED} \quad (81)$$

Boost and Buck-boost

$$I_{T\text{-}MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LED} \quad (82)$$

Approximate the nominal RMS transistor current ($I_{T\text{-}RMS}$) :

Buck

$$I_{T\text{-}RMS} = I_{LED} \times \sqrt{D} \quad (83)$$

Boost and Buck-boost

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} \quad (84)$$

Given an NFET with on-resistance ($R_{DS\text{-}ON}$), solve for the nominal power dissipation (P_T):

$$P_T = I_{T\text{-}RMS}^2 \times R_{DSON} \quad (85)$$

12. DIODE

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage ($V_{RD\text{-}MAX}$):

Buck

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} \quad (86)$$

Boost

$$V_{RD\text{-}MAX} = V_O \quad (87)$$

Buck-boost

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (88)$$

The current rating should be at least 10% higher than the maximum average diode current ($I_{D\text{-}MAX}$):

Buck

$$I_{D\text{-}MAX} = (1 - D_{MIN}) \times I_{LED} \quad (89)$$

Boost and Buck-boost

$$I_{D\text{-}MAX} = I_{LED} \quad (90)$$

Replace D_{MAX} with D in the $I_{D\text{-}MAX}$ equation to solve for the average diode current (I_D). Given a diode with forward voltage (V_{FD}), solve for the nominal power dissipation (P_D):

$$P_D = I_D \times V_{FD} \quad (91)$$

13. OUTPUT OVLO

For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage ($V_{TURN\text{-}OFF}$) and the desired hysteresis (V_{HYSO}). To set V_{HYSO}, solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} \quad (92)$$

To set $V_{TURN\text{-}OFF}$, solve for R_{OV1}:

Boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 1.24V} \quad (93)$$

Buck-boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 620\,mV} \quad (94)$$

A small filter capacitor (C_{OVP} = 47 pF) should be added from the OVP pin to ground to reduce coupled switching noise.

14. INPUT UVLO

For all topologies, input UVLO is programmed with the turn-on threshold voltage ($V_{TURN-ON}$) and the desired hysteresis (V_{HYS}).

Method #1: If no PWM dimming is required, a two resistor network can be used. To set V_{HYS}, solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} \tag{95}$$

To set $V_{TURN-ON}$, solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} \tag{96}$$

Method #2: If PWM dimming is required, a three resistor network is suggested. To set $V_{TURN-ON}$, assume R_{UV2} = 10 kΩ and solve for R_{UV1} as in Method #1. To set V_{HYS}, solve for R_{UVH}:

$$R_{UVH} = \frac{R_{UV1} \times (V_{HYS} - 20\,\mu A \times R_{UV2})}{20\,\mu A \times (R_{UV1} + R_{UV2})} \tag{97}$$

15. SOFT-START

For all topologies, if soft-start is desired, find the start-up time without C_{SS} (t_{SU}):

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \tag{98}$$

Then, if the desired total start-up time (t_{TSU}) is larger than t_{SU}, solve for the base start-up time ($t_{SU-SS-BASE}$), assuming that a C_{SS} greater than 40% of C_{CMP} will be used:

$$t_{SU-SS-BASE} = 168\Omega \times C_{BYP} + 28\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O \tag{99}$$

Then solve for C_{SS}:

$$C_{SS} = \frac{10\,\mu A}{0.2V} \times (t_{TSU} - t_{SU-SS-BASE}) \tag{100}$$

16. PWM DIMMING METHOD

PWM dimming can be performed several ways:

Method #1: Connect the dimming MosFET (Q_3) with the drain to the nDIM pin and the source to GND. Apply an external PWM signal to the gate of Q_{DIM}. A pull down resistor may be necessary to properly turn off Q_3.

Method #2: Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

The DDRV pin should be connected to the gate of the dimFET with or without level-shifting circuitry as described in the PWM DIMMING section. The dimFET should be rated to handle the average LED current and the nominal output voltage.

17. ANALOG DIMMING METHOD

Analog dimming can be performed several ways:

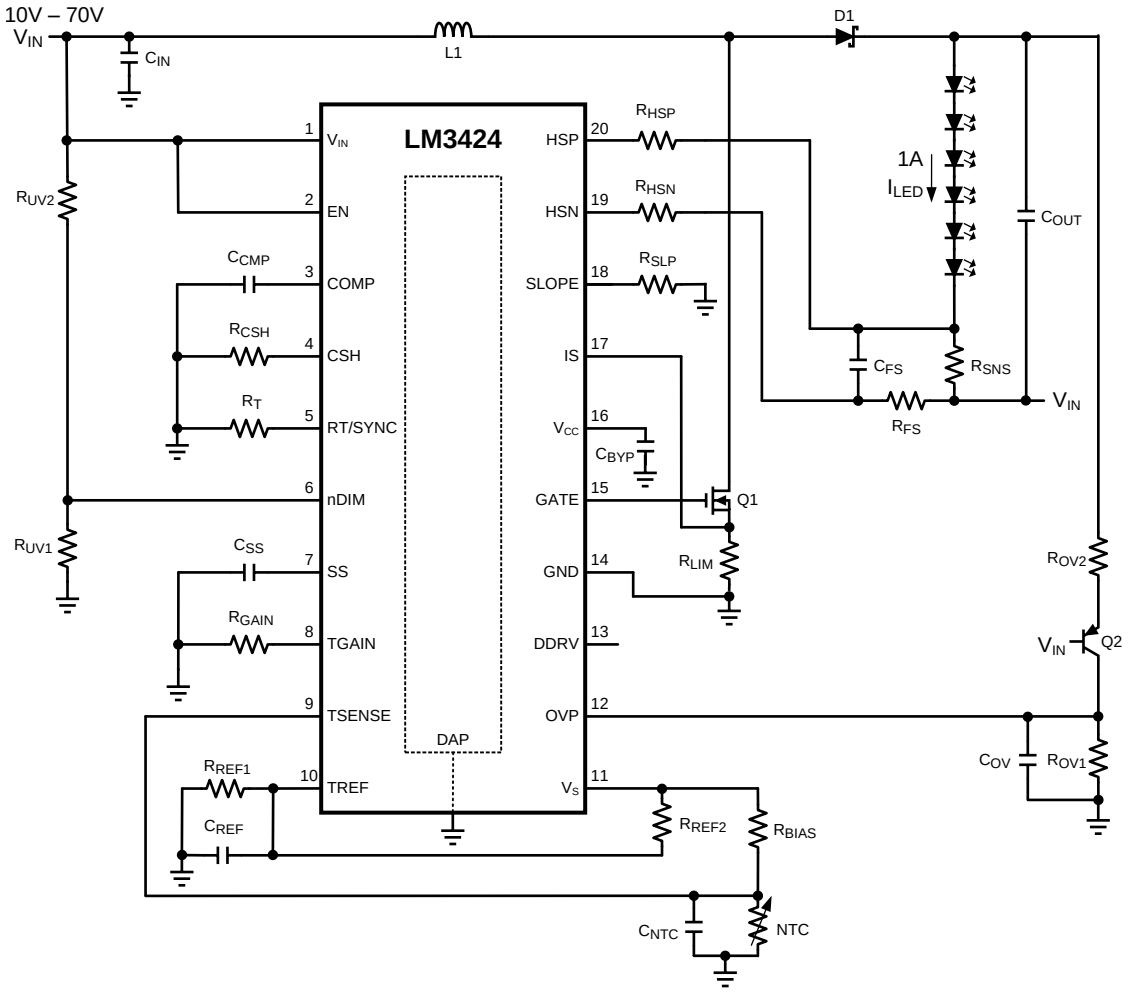
Method #1: Place a potentiometer in place of the thermistor in the thermal foldback circuit shown in the THERMAL FOLDBACK / ANALOG DIMMING section.

Method #2: Place a potentiometer in series with the R_{CSH} resistor to dim the LED current from the nominal I_{LED} to near zero.

Method #3: Connect a controlled current source as detailed in the THERMAL FOLDBACK / ANALOG DIMMING section to the CSH pin. Increasing the current sourced into the CSH node will decrease the LEDs from the nominal I_{LED} to zero current in the same manner as the thermal foldback circuit.

Design Example

DESIGN #1 - BUCK-BOOST Application



SPECIFICATIONS

N = 6

V_{LED} = 3.5V

r_{LED} = 325 mΩ

V_{IN} = 24V

V_{IN-MIN} = 10V

V_{IN-MAX} = 70V

f_{SW} = 500 kHz

V_{SNS} = 100 mV

I_{LED} = 1A

Δi_{L-PP} = 700 mA

Δi_{LED-PP} = 12 mA

Δv_{IN-PP} = 100 mV

I_{LIM} = 6A

$V_{TURN-ON}$ = 10V

V_{HYS} = 3V

$V_{TURN-OFF}$ = 40V

V_{HYSO} = 10V

T_{BK} = 70°C

T_{END}= 120°C

t_{TSU} = 30 ms

1. OPERATING POINT

Solve for V_O and r_D:

$$V_O = N \times V_{LED} = 6 \times 3.5V = 21V \quad (101)$$

$$r_D = N \times r_{LED} = 6 \times 325\,m\Omega = 1.95\Omega \quad (102)$$

Solve for D, D', D_{MAX}, and D_{MIN}:

$$D = \frac{V_O}{V_O + V_{IN}} = \frac{21V}{21V + 24V} = 0.467 \quad (103)$$

$$D' = 1 - D = 1 - 0.467 = 0.533 \quad (104)$$

$$D_{MIN} = \frac{V_O}{V_O + V_{IN-MAX}} = \frac{21V}{21V + 70V} = 0.231 \quad (105)$$

$$D_{MAX} = \frac{V_O}{V_O + V_{IN-MIN}} = \frac{21V}{21V + 10V} = 0.677 \quad (106)$$

2. SWITCHING FREQUENCY

Solve for R_T:

$$R_T = \frac{1+1.95e^{-8} \times f_{SW}}{1.40e^{-10} \times f_{SW}} = \frac{1+1.95e^{-8} \times 500\,kHz}{1.40e^{-10} \times 500\,kHz} = 14.4\,k\Omega \quad (107)$$

The closest standard resistor is 14.3 kΩ therefore f_{SW} is:

$$f_{SW} = \frac{1}{1.40e^{-10} \times R_T - 1.95e^{-8}}$$

$$f_{SW} = \frac{1}{1.40e^{-10} \times 14.3\,k\Omega - 1.95e^{-8}} = 504\,kHz \quad (108)$$

The chosen component from step 2 is:

$$\boxed{R_T = 14.3\,k\Omega} \quad (109)$$

3. AVERAGE LED CURRENT

Solve for R_{SNS}:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} = \frac{100\,mV}{1A} = 0.1\Omega \quad (110)$$

Assume R_{CSH} = 12.4 kΩ and solve for R_{HSP}:

$$R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} = \frac{1A \times 12.4\,k\Omega \times 0.1\Omega}{1.24V} = 1.0\,k\Omega \quad (111)$$

The closest standard resistor for R_{SNS} is actually 0.1Ω and for R_{HSP} is actually 1 kΩ therefore I_{LED} is:

$$I_{LED} = \frac{1.24V \times R_{HSP}}{R_{SNS} \times R_{CSH}} = \frac{1.24V \times 1.0\,k\Omega}{0.1\Omega \times 12.4\,k\Omega} = 1.0A \quad (112)$$

The chosen components from step 3 are:

$$\boxed{\begin{aligned} R_{SNS} &= 0.1\Omega \\ R_{CSH} &= 12.4\,k\Omega \\ R_{HSP} &= R_{HSN} = 1k\Omega \end{aligned}} \quad (113)$$

4. THERMAL FOLDBACK

Find the resistances corresponding to T_{BK} and T_{END} ($R_{NTC\text{-}BK}$ = 24.3 kΩ and $R_{NTC\text{-}END}$ = 7.15 kΩ) from the manufacturer's datasheet. Assuming $R_{REF1} = R_{REF2}$ = 49.9 kΩ, then $R_{BIAS} = R_{NTC\text{-}BK}$= 24.3 kΩ.

Solve for R_{GAIN}:

$$R_{GAIN} = \frac{\left(\frac{R_{REF1}}{R_{REF1}+R_{REF2}} - \frac{R_{NTC-END}}{R_{NTC-END}+R_{BIAS}}\right) \times 2.45V}{I_{CSH}}$$

$$R_{GAIN} = \frac{\left(\frac{1}{2} - \frac{7.15\,k\Omega}{7.15\,k\Omega+24.3k\Omega}\right) \times 2.45V}{100\,\mu A} = 6.68\,k\Omega \quad (114)$$

The chosen components from step 4 are:

$$\boxed{\begin{aligned} R_{GAIN} &= 6.81k\Omega \\ R_{BIAS} &= 243\,k\Omega \\ R_{REF1} &= R_{REF2} = 49.9\,k\Omega \end{aligned}} \quad (115)$$

5. INDUCTOR RIPPLE CURRENT

Solve for L1:

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} = \frac{24V \times 0.467}{700\ mA \times 504\ kHz} = 32\ \mu H \tag{116}$$

The closest standard inductor is 33 µH therefore $\Delta i_{L\text{-}PP}$ is:

$$\Delta i_{L\text{-}PP} = \frac{V_{IN} \times D}{L1 \times f_{SW}} = \frac{24V \times 0.467}{33\ \mu H \times 504\ kHz} = 674\ mA \tag{117}$$

Determine minimum allowable RMS current rating:

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta i_{L\text{-}PP} \times D'}{I_{LED}}\right)^2}$$

$$I_{L\text{-}RMS} = \frac{1A}{0.533} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{674\ mA \times 0.533}{1A}\right)^2} = 1.89A \tag{118}$$

The chosen component from step 5 is:

$$\boxed{L1 = 33\ \mu H} \tag{119}$$

6. OUTPUT CAPACITANCE

Solve for C_O:

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}}$$

$$C_O = \frac{1A \times 0.467}{1.95\Omega \times 12\ mA \times 504\ kHz} = 39.6\ \mu F \tag{120}$$

The closest capacitance totals 40 µF therefore $\Delta i_{LED\text{-}PP}$ is:

$$\Delta i_{LED\text{-}PP} = \frac{I_{LED} \times D}{r_D \times C_O \times f_{SW}}$$

$$\Delta i_{LED\text{-}PP} = \frac{1A \times 0.467}{1.95\Omega \times 40\ \mu F \times 504\ kHz} = 12\ mA \tag{121}$$

Determine minimum allowable RMS current rating:

$$I_{CO\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \tag{122}$$

The chosen components from step 6 are:

$$\boxed{C_O = 4 \times 10\ \mu F} \tag{123}$$

7. PEAK CURRENT LIMIT

Solve for R_{LIM}:

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} = \frac{245\ mV}{6A} = 0.041\Omega \tag{124}$$

The closest standard resistor is 0.04 Ω therefore I_{LIM} is:

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} = \frac{245\ mV}{0.04\Omega} = 6.13A \tag{125}$$

The chosen component from step 7 is:

$$\boxed{R_{LIM} = 0.04\Omega} \tag{126}$$

8. SLOPE COMPENSATION

Solve for R_{SLP}:

$$R_{SLP} = \frac{1.5e^{13} \times L1}{V_O \times R_T \times R_{SNS}}$$

$$R_{SLP} = \frac{1.5e^{13} \times 33\,\mu H}{21V \times 14.3\,k\Omega \times 0.1\Omega} = 16.5\,k\Omega \quad (127)$$

The chosen component from step 8 is:

$$\boxed{R_{SLP} = 16.5\,k\Omega} \quad (128)$$

9. LOOP COMPENSATION

ω_{P1} is approximated:

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 40\,\mu F} = 19k\frac{rad}{sec} \quad (129)$$

ω_{Z1} is approximated:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33\,\mu H} = 36k\frac{rad}{sec} \quad (130)$$

T_{U0} is approximated:

$$T_{U0} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \quad (131)$$

To ensure stability, calculate ω_{P2}:

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{P1}}{5 \times 5630} = \frac{19k\frac{rad}{sec}}{5 \times 5630} = 0.675\frac{rad}{sec} \quad (132)$$

Solve for C_{CMP}:

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5e^6\Omega} = \frac{1}{0.675\frac{rad}{sec} \times 5e^6\Omega} = 0.30\,\mu F \quad (133)$$

To attenuate switching noise, calculate ω_{P3}:

$$\omega_{P3} = (\max \omega_{P1}, \omega_{Z1}) \times 10 = \omega_{Z1} \times 10$$

$$\omega_{P3} = 36k\frac{rad}{sec} \times 10 = 360k\frac{rad}{sec} \quad (134)$$

Assume R_{FS} = 10Ω and solve for C_{FS}:

$$C_{FS} = \frac{1}{10\Omega \times \omega_{P3}} = \frac{1}{10\Omega \times 360k\frac{rad}{sec}} = 0.28\,\mu F \quad (135)$$

The chosen components from step 9 are:

$$\boxed{\begin{array}{l} C_{CMP} = 0.33\,\mu F \\ R_{FS} = 10\Omega \\ C_{FS} = 0.27\mu F \end{array}} \quad (136)$$

10. INPUT CAPACITANCE

Solve for the minimum C_{IN}:

$$C_{IN} = \frac{I_{LED} \times D}{\Delta v_{IN-PP} \times f_{SW}} = \frac{1A \times 0.467}{100\,mV \times 504\,kHz} = 9.27\,\mu F \quad (137)$$

To minimize power supply interaction a 200% larger capacitance of approximately 20 µF is used, therefore the actual Δv_{IN-PP} is much lower. Since high voltage ceramic capacitor selection is limited, four 4.7 µF X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

$$I_{IN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \quad (138)$$

The chosen components from step 10 are:

$$\boxed{C_{IN} = 4 \times 4.7\ \mu F} \quad (139)$$

11. NFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \quad (140)$$

$$I_{T-MAX} = \frac{0.677}{1 - 0.677} \times 1A = 2.1A \quad (141)$$

A 100V NFET is chosen with a current rating of 32A due to the low R_{DS-ON} = 50 mΩ. Determine I_{T-RMS} and P_T:

$$I_{T-RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \quad (142)$$

$$P_T = I_{T-RMS}^2 \times R_{DSON} = 1.28A^2 \times 50\,m\Omega = 82\,mW \quad (143)$$

The chosen component from step 11 is:

$$\boxed{Q1 \rightarrow 32A,\ 100V,\ DPAK} \quad (144)$$

12. DIODE

Determine minimum D1 voltage rating and current rating:

$$V_{RD-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \quad (145)$$

$$I_{D-MAX} = I_{LED} = 1A \quad (146)$$

A 100V diode is chosen with a current rating of 12A and V_D = 600 mV. Determine P_D:

$$P_D = I_D \times V_{FD} = 1A \times 600\,mV = 600\,mW \quad (147)$$

The chosen component from step 12 is:

$$\boxed{D1 \rightarrow 12A,\ 100V,\ DPAK} \quad (148)$$

13. INPUT UVLO

Solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} = \frac{3V}{20\,\mu A} = 150\,k\Omega \quad (149)$$

The closest standard resistor is 150 kΩ therefore V_{HYS} is:

$$V_{HYS} = R_{UV2} \times 20\,\mu A = 150\,k\Omega \times 20\,\mu A = 3V \quad (150)$$

Solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} = \frac{1.24V \times 150\,k\Omega}{10V - 1.24V} = 21.2\,k\Omega \quad (151)$$

The closest standard resistor is 21 kΩ making $V_{TURN-ON}$:

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN-ON} = \frac{1.24V \times (21\,k\Omega + 150\,k\Omega)}{21\,k\Omega} = 10.1V \quad (152)$$

The chosen components from step 13 are:

$$\boxed{\begin{array}{l} R_{UV1} = 21\,k\Omega \\ R_{UV2} = 150\,k\Omega \end{array}} \quad (153)$$

14. OUTPUT OVLO

Solve for R_{OV2}:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} = \frac{10V}{20\,\mu A} = 500\,k\Omega \quad (154)$$

The closest standard resistor is 499 kΩ therefore V_{HYSO} is:

$$V_{HYSO} = R_{OV2} \times 20\,\mu A = 499\,k\Omega \times 20\,\mu A = 9.98V \quad (155)$$

Solve for R_{OV1}:

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 0.62V} = \frac{1.24V \times 499\,k\Omega}{40V - 0.62V} = 15.7\,k\Omega \quad (156)$$

The closest standard resistor is 15.8 kΩ making $V_{TURN-OFF}$:

$$V_{TURN-OFF} = \frac{1.24V \times (0.5 \times R_{OV1} + R_{OV2})}{R_{OV1}}$$

$$V_{TURN-OFF} = \frac{1.24V \times (0.5 \times 15.8\,k\Omega + 499\,k\Omega)}{15.8\,k\Omega} = 39.8V \quad (157)$$

The chosen components from step 14 are:

$$\boxed{\begin{array}{l} R_{OV1} = 15.8\,k\Omega \\ R_{OV2} = 499\,k\Omega \end{array}} \quad (158)$$

15. SOFT-START

Solve for t_{SU}:

$$t_{SU} = 168\Omega \times C_{BYP} + 36\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O$$

$$t_{SU} = 168\Omega \times 2.2\,\mu F + 36\,k\Omega \times 0.33\,\mu F + \frac{21V}{1A} \times 40\,\mu F$$

$$t_{SU} = 13.1\ ms \quad (159)$$

If t_{SU} is less than t_{TSU}, solve for $t_{SU\text{-}SS\text{-}BASE}$:

$$t_{SU\text{-}SS\text{-}BASE} = 168\Omega \times C_{BYP} + 28\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O$$

$$t_{SU\text{-}SS\text{-}BASE} = 168\Omega \times 2.2\,\mu F + 28\,k\Omega \times 0.33\,\mu F + \frac{21V}{1A} \times 40\,\mu F$$

$$t_{SU\text{-}SS\text{-}BASE} = 10.5\ ms \quad (160)$$

Solve for C_{SS}:

$$C_{SS} = \frac{(t_{TSU} - t_{SU\text{-}SS\text{-}BASE})}{20\,k\Omega} = \frac{(30\ ms - 10.5\ ms)}{20\,k\Omega} = 975\,nF \quad (161)$$

The chosen component from step 15 is:

$$\boxed{C_{SS} = 1\,\mu F} \quad (162)$$

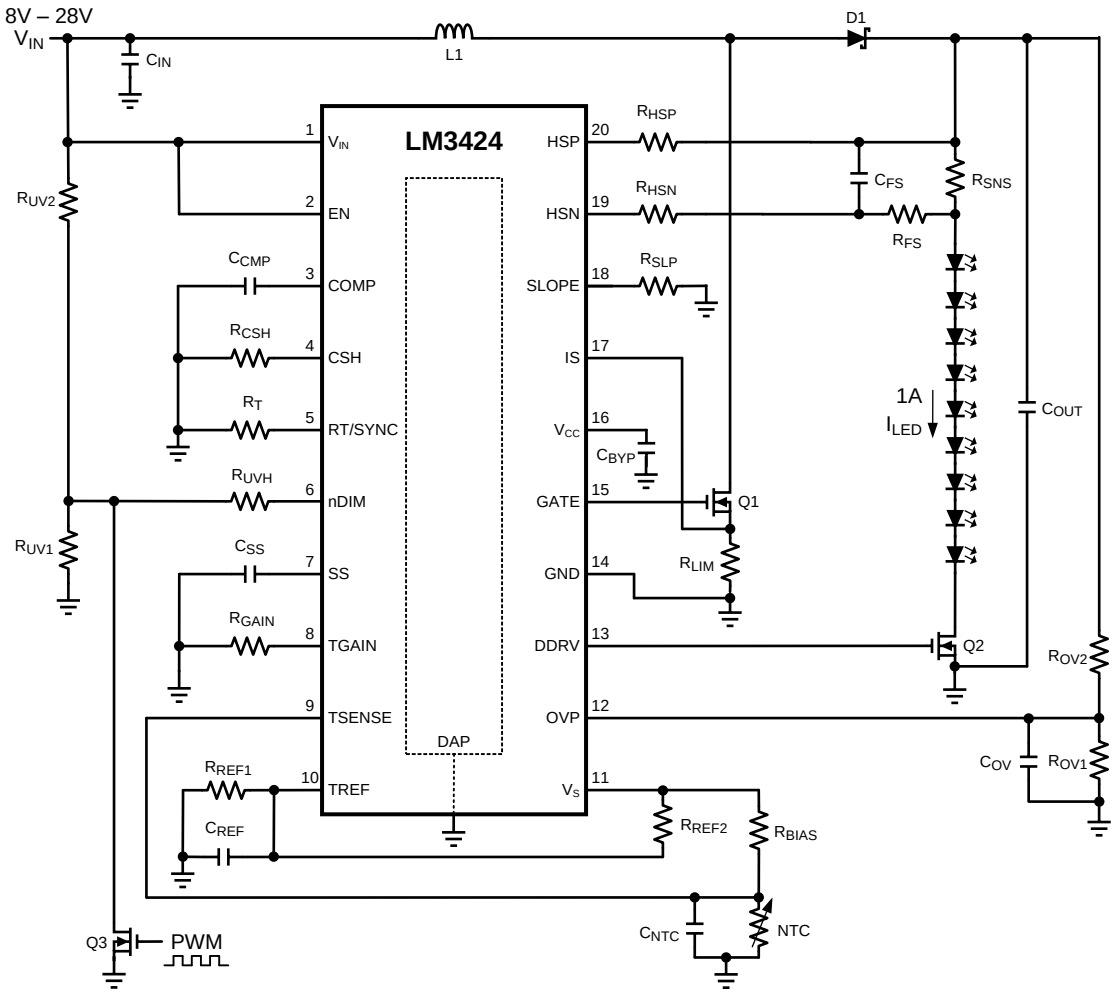
DESIGN #1 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
2	C_{CMP}, C_{NTC}	0.33 µF X7R 10% 25V	MURATA	GRM21BR71E334KA01L
1	C_{FS}	0.27 µF X7R 10% 25V	MURATA	GRM21BR71E274KA01L
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
4	C_O	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_{REF}, C_{SS}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	L1	33 µH 20% 6.3A	COILCRAFT	MSS1278-333MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R_{BIAS}	24.3 kΩ 1%	VISHAY	CRCW080524K3FKEA
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
1	R_{GAIN}	6.81 kΩ 1%	VISHAY	CRCW08056K81FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
2	R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{SLP}	16.5 kΩ 1%	VISHAY	CRCW080516K5FKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA
1	R_T	14.3 kΩ 1%	VISHAY	CRCW080514K3FKEA
1	R_{UV1}	21 kΩ 1%	VISHAY	CRCW080521K0FKEA
1	R_{UV2}	150 kΩ 1%	VISHAY	CRCW0805150KFKEA
1	NTC	Thermistor 100 kΩ 5%	TDK	NTCG204H154J

APPLICATIONS INFORMATION

The following designs are provided as reference circuits. For a specific design, the steps in the Design Guide section should be performed. In all designs, an RC filter (0.1 µF, 10Ω) is recommended at VIN placed as close as possible to the LM3424 device. This filter is not shown in the following designs.

DESIGN #2 - BOOST Application



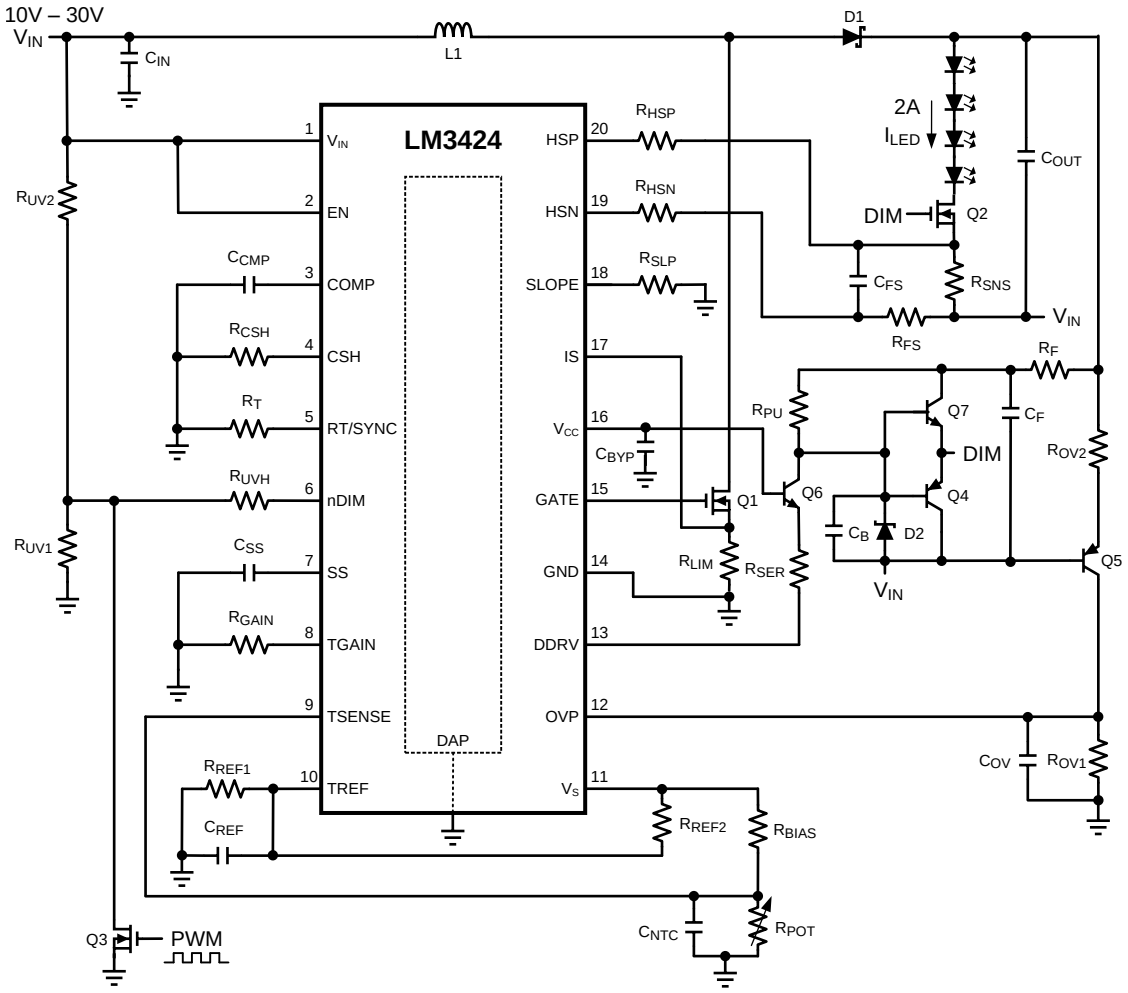
Features

- Input: 8V to 28V
- Output: 9 LEDs at 1A
- 65°C - 100°C Thermal Foldback
- PWM Dimming up to 30kHz
- 700 kHz Switching Frequency

DESIGN #2 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
1	C_{CMP}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
4	C_{OUT}	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
2	C_{NTC}, C_{SS}	0.27 µF X7R 10% 25V	MURATA	GRM21BR71E274KA01L
1	C_{REF}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1	33 µH 20% 6.3A	COILCRAFT	MSS1278-333MLB
2	Q1, Q2	NMOS 60V 8A	VISHAY	SI4436DY
1	Q3	NMOS 60V 115mA	ON-SEMI	2N7002ET1G
1	R_{BIAS}	19.6 kΩ 1%	VISHAY	CRCW080519K6FKEA
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0Ω 1%	VISHAY	CRCW08050000Z0EA
1	R_{GAIN}	6.49 kΩ 1%	VISHAY	CRCW08056K49FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.06Ω 1% 1W	VISHAY	WSL2512R0600FEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
2	R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA
2	R_{SLP}, R_{UV2}	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_T	14.3 kΩ 1%	VISHAY	CRCW080514K3FKEA
1	R_{UV1}	1.82 kΩ 1%	VISHAY	CRCW08051K82FKEA
1	R_{UVH}	17.8 kΩ 1%	VISHAY	CRCW080517K8FKEA
1	NTC	Thermistor 100 kΩ 5%	TDK	NTCG204H154J

DESIGN #3 - BUCK-BOOST Application



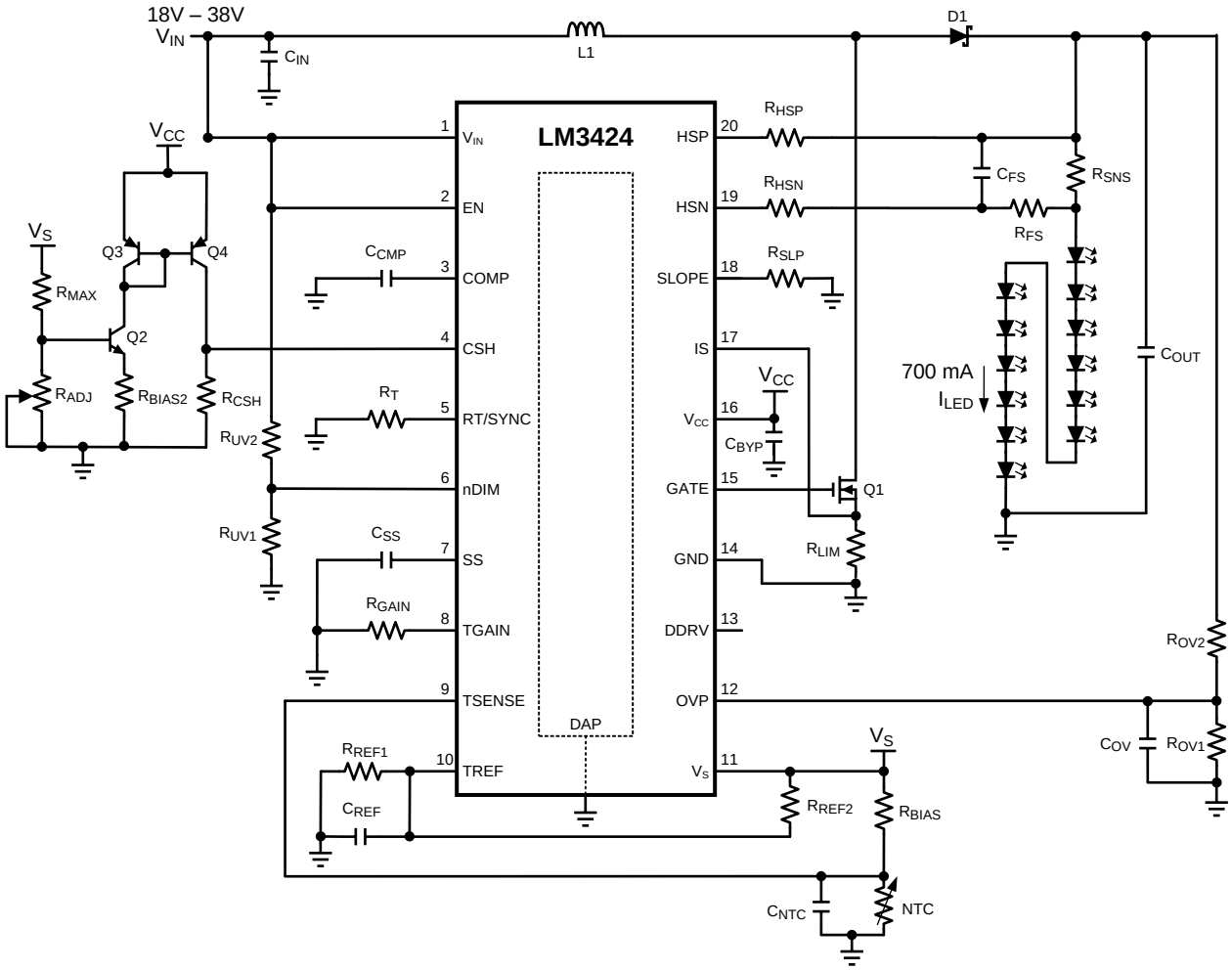
Features

- Input: 10V to 30V
- Output: 4 LEDs at 2A
- PWM Dimming up to 10kHz
- Analog Dimming
- 600 kHz Switching Frequency

DESIGN #3 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_B	100 pF COG/NPO 5% 50V	MURATA	GRM2165C1H101JA01D
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
3	C_{CMP}, C_{REF}, C_{SS}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	C_F	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	6.8 µF X7R 10% 50V	TDK	C5750X7R1H685K
1	C_{NTC}	0.47 µF X7R 10% 25V	MURATA	GRM21BR71E474KA01L
4	C_{OUT}	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	22 µH 20% 7.2A	COILCRAFT	MSS1278-223MLB
2	Q1, Q2	NMOS 60V 8A	VISHAY	SI4436DY
1	Q3	NMOS 60V 260mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 40V 200 mA	FAIRCHILD	MMBT5087
1	Q5	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	Q6	NPN 300V 600 mA	FAIRCHILD	MMBTA42
1	Q7	NPN 40V 200 mA	FAIRCHILD	MMBT6428
3	R_{BIAS}, R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
2	R_{CSH}, R_T	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_F	10Ω 1%	VISHAY	CRCW080510R0FKEA
1	R_{FS}	0Ω 1%	VISHAY	CRCW08050000Z0EA
2	R_{GAIN}, R_{UV2}	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	18.2 kΩ 1%	VISHAY	CRCW080518K2FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{POT}	50 kΩ potentiometer	BOURNS	3352P-1-503
1	R_{PU}	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R_{SER}	499Ω 1%	VISHAY	CRCW0805499RFKEA
1	R_{SLP}	34.0 kΩ 1%	VISHAY	CRCW080534K0FKEA
1	R_{SNS}	0.05Ω 1% 1W	VISHAY	WSL2512R0500FEA
1	R_{UV1}	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R_{UVH}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

DESIGN #4 - BOOST Application



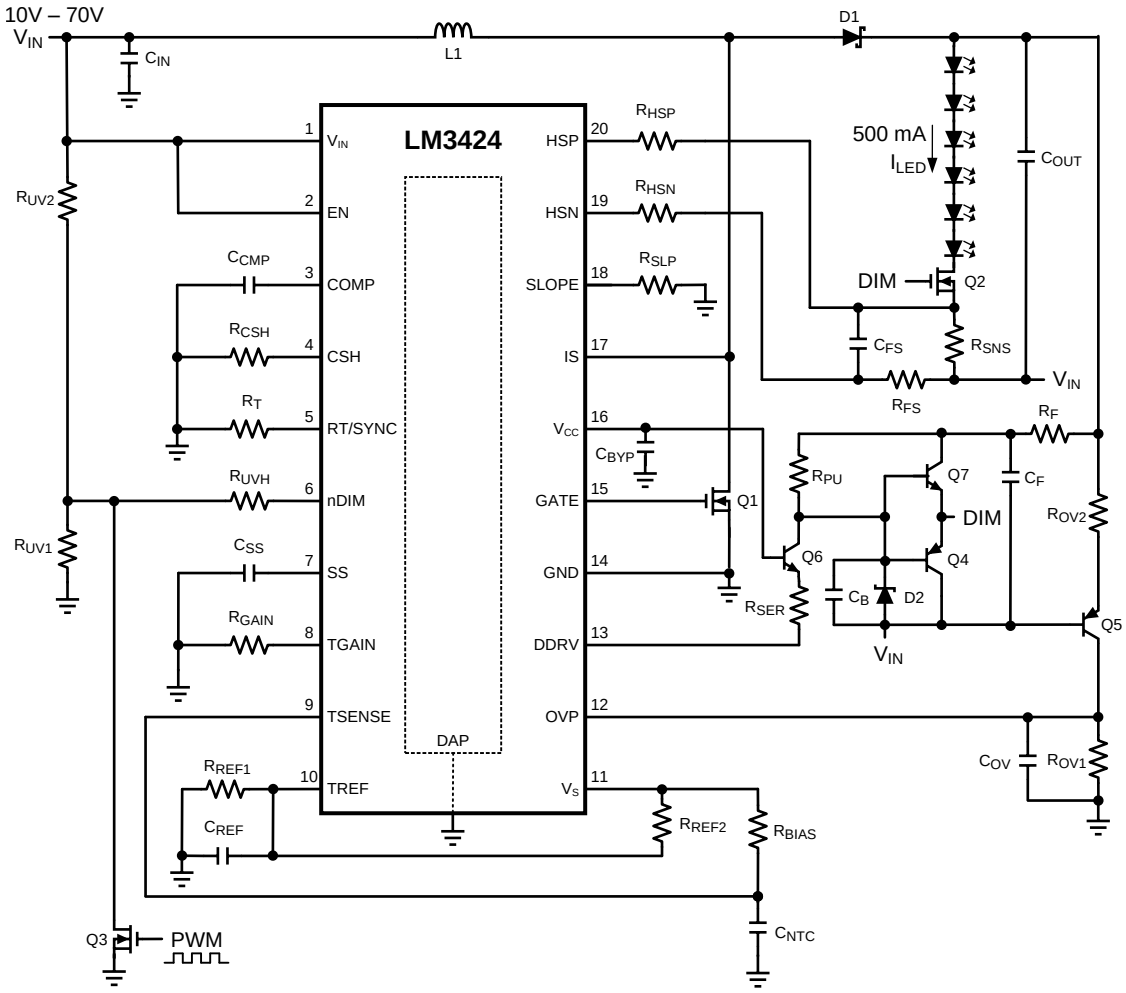
Features

- Input: 18V to 38V
- Output: 12 LEDs at 700mA
- 85°C - 125°C Thermal Foldback
- Analog Dimming
- 700 kHz Switching Frequency

DESIGN #4 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
3	C_{CMP}, C_{REF}, C_{SS}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	C_{NTC}	0.33 µF X7R 10% 25V	MURATA	GRM21BR71E334KA01L
1	C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
4	C_{OUT}	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1	47 µH 20% 5.3A	COILCRAFT	MSS1278-473MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	NPN 40V 200 mA	FAIRCHILD	MMBT3904
1	Q3, Q4 (dual pack)	Dual PNP 40V 200mA	FAIRCHILD	FFB3906
1	R_{ADJ}	100 kΩ potentiometer	BOURNS	3352P-1-104
1	R_{BIAS}	9.76 kΩ 1%	VISHAY	CRCW08059K76FKEA
1	R_{BIAS2}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA
3	R_{CSH}, R_{OV1}, R_{UV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
1	R_{GAIN}	6.55 kΩ 1%	VISHAY	CRCW08056K55FKEA
3	R_{HSP}, R_{HSN}, R_{MAX}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.06Ω 1% 1W	VISHAY	WSL2512R0600FEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
2	R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
2	R_{SLP}, R_T	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_{SNS}	0.15Ω 1% 1W	VISHAY	WSL2512R1500FEA
1	R_{UV2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA
1	NTC	Thermistor 100 kΩ 5%	TDK	NTCG204H154J

DESIGN #5 - BUCK-BOOST Application



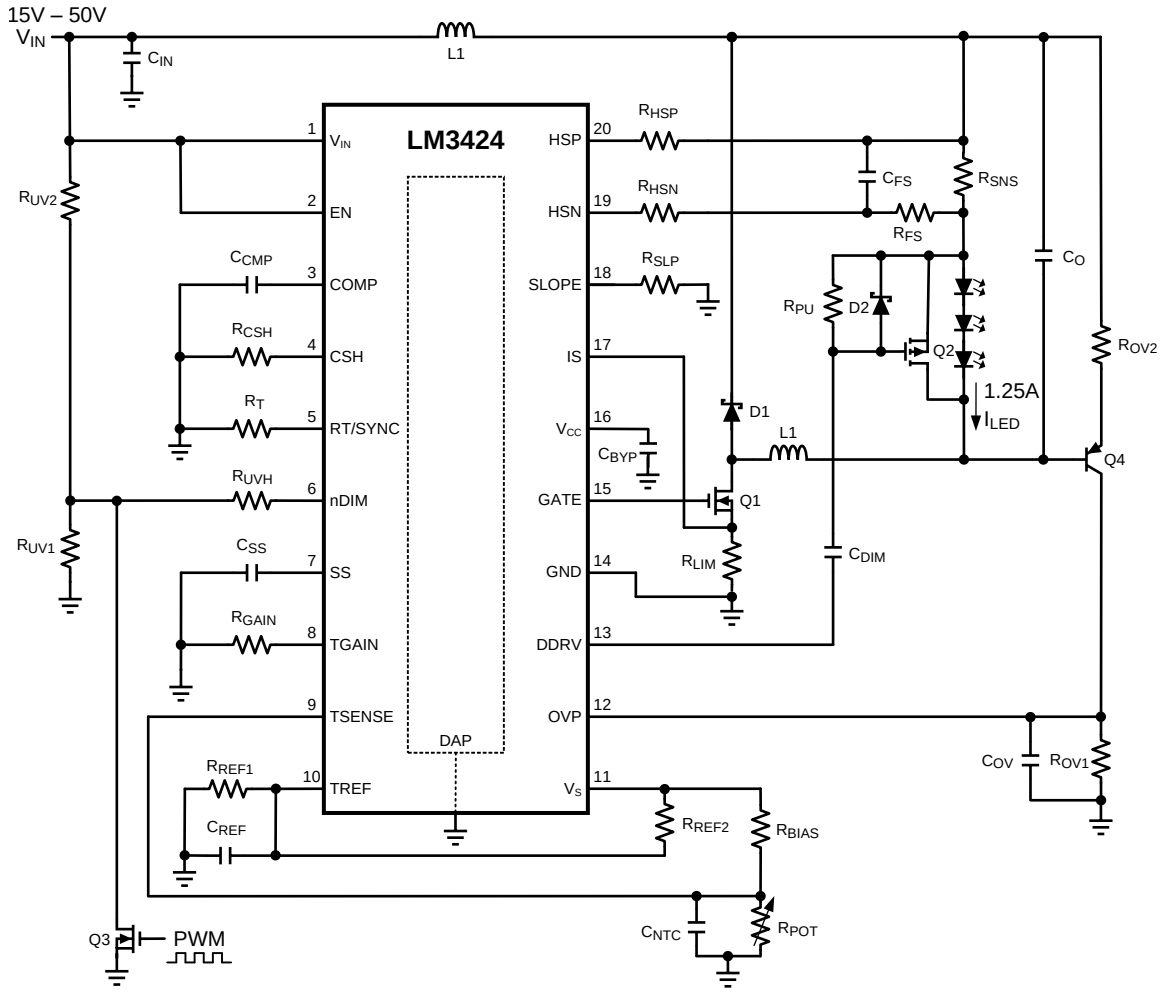
Features

- Input: 10V to 70V
- Output: 6 LEDs at 500mA
- PWM Dimming up to 10 kHz
- 5 sec Fade-up
- MosFET R_{DS-ON} Sensing
- 700 kHz Switching Frequency

DESIGN #5 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_B	100 pF COG/NPO 5% 50V	MURATA	GRM2165C1H101JA01D
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
2	C_{CMP}, C_{SS}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	C_{REF}	0.01 µF X7R 10% 25V	MURATA	GRM21BR71E103KA01L
1	C_F	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
1	C_{NTC}	10 µF X7R 10% 10V	MURATA	GRM21BR71A106KE51L
4	C_{OUT}	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	68 µH 20% 4.3A	COILCRAFT	MSS1278-683MLB
2	Q1, Q2	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q3	NMOS 60V 260mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 40V 200mA	FAIRCHILD	MMBT5087
1	Q5	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	Q6	NPN 300V 600mA	FAIRCHILD	MMBTA42
1	Q7	NPN 40V 200mA	FAIRCHILD	MMBT6428
3	R_{BIAS}, R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0Ω 1%	VISHAY	CRCW08050000Z0EA
3	R_{GAIN}, R_T, R_{UV2}	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{PU}	4.99 kΩ 1%	VISHAY	CRCW08054K99FKEA
1	R_{SER}	499Ω 1%	VISHAY	CRCW0805499RFKEA
1	R_{SNS}	0.2Ω 1% 1W	VISHAY	WSL2512R2000FEA
1	R_{SLP}	24.3 kΩ 1%	VISHAY	CRCW080524K3FKEA
1	R_{UV1}	1.43 kΩ 1%	VISHAY	CRCW08051K43FKEA
1	R_{UVH}	17.4 kΩ 1%	VISHAY	CRCW080517K4FKEA

DESIGN #6 - BUCK Application



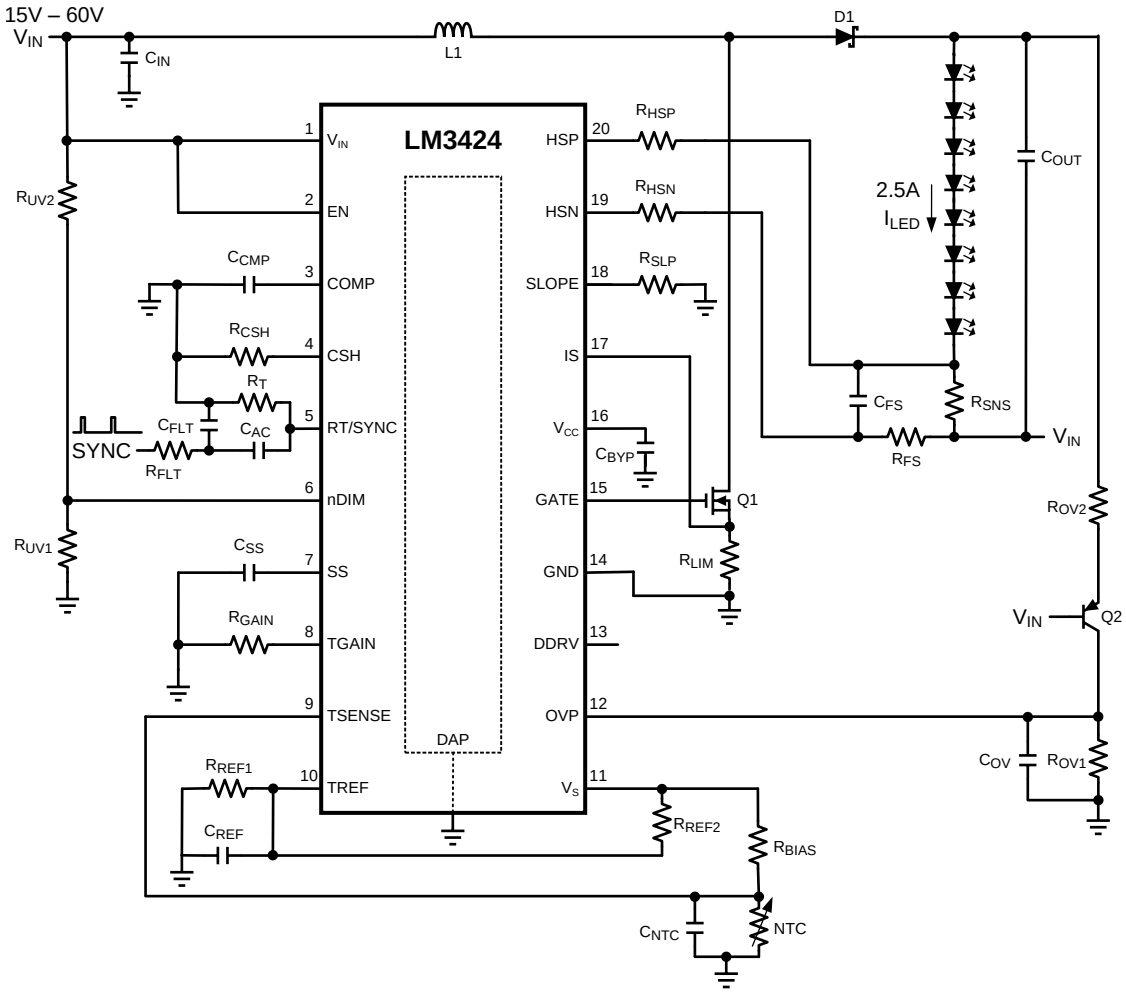
Features

- Input: 15V to 50V
- Output: 3 LEDS AT 1.25A
- PWM Dimming up to 50 kHz
- Analog Dimming
- 700 kHz Switching Frequency

DESIGN #6 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
2	C_{CMP}, C_{DIM}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
0	C_{FS}	DNP		
1	C_{NTC}	0.33 µF X7R 10% 25V	MURATA	GRM21BR71E334KA01L
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
0	C_{OUT}	DNP		
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_{REF}, C_{SS}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	D2	Zener 10V 500mA	ON-SEMI	BZX84C10LT1G
1	L1	22 µH 20% 7.3A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 60V 8A	VISHAY	SI4436DY
1	Q2	PMOS 30V 6.2A	VISHAY	SI3483DV
1	Q3	NMOS 60V 115mA	ON-SEMI	2N7002ET1G
1	Q4	PNP 150V 600 mA	FAIRCHILD	MMBT5401
3	R_{BIAS}, R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0Ω 1%	VISHAY	CRCW08050000OZEA
1	R_{GAIN}, R_T	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	21.5 kΩ 1%	VISHAY	CRCW080521K5FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
1	R_{POT}	50 kΩ potentiometer	BOURNS	3352P-1-503
2	R_{PU}, R_{UV2}	100 kΩ 1%	VISHAY	CRCW0805100KFKEA
1	R_{SLP}	36.5 kΩ 1%	VISHAY	CRCW080536K5FKEA
1	R_{SNS}	0.08Ω 1% 1W	VISHAY	WSL2512R0800FEA
1	R_{UV1}	11.5 kΩ 1%	VISHAY	CRCW080511K5FKEA

DESIGN #7 - BUCK-BOOST Application



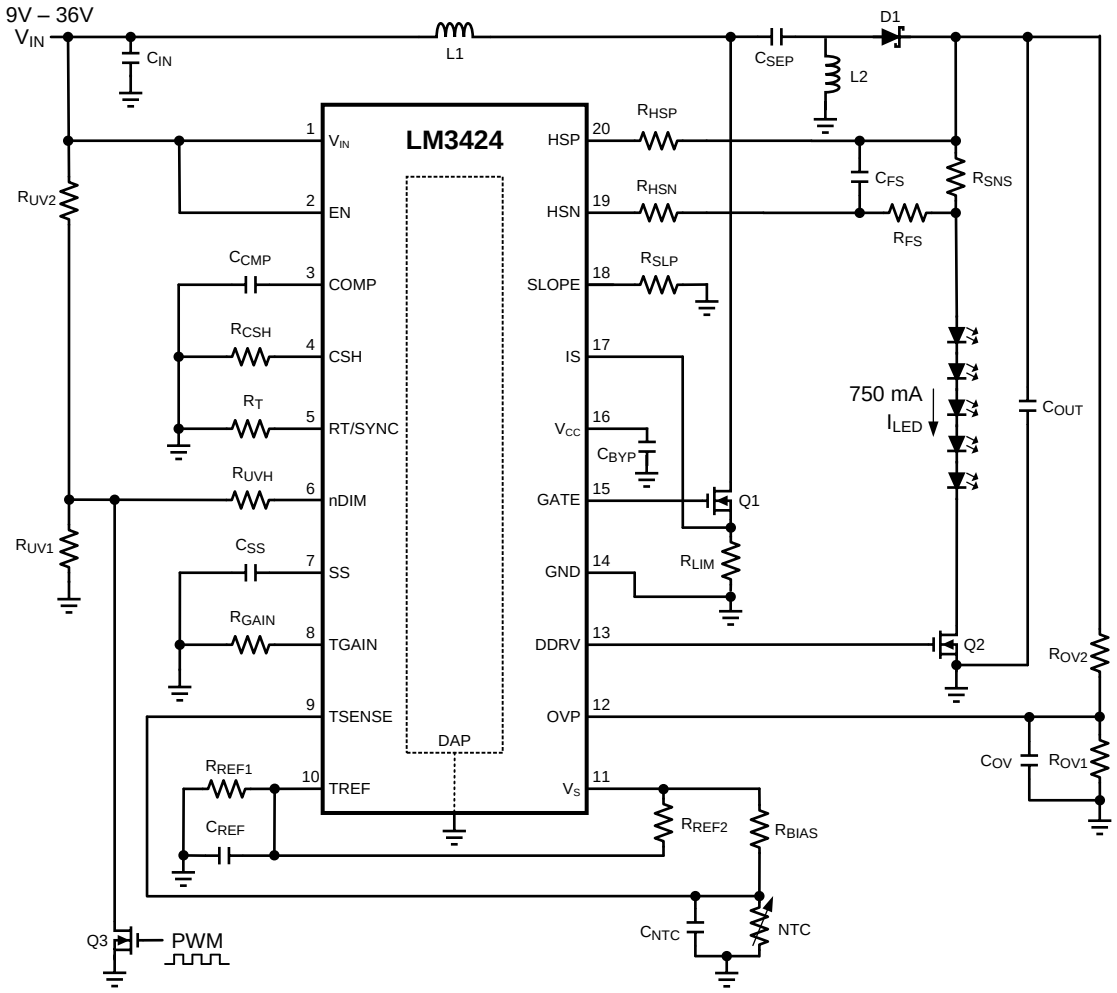
Features

- Input: 15V to 60V
- Output: 8 LEDs at 2.5A
- 80°C - 110°C Thermal Foldback
- 500 kHz Switching Frequency
- External Synchronization > 500 kHz

DESIGN #7 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
2	C_{AC}, C_{FLT}	100 pF COG/NPO 5% 50V	MURATA	GRM2165C1H101JA01D
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
3	C_{CMP}, C_{NTC}, C_{SS}	0.33 µF X7R 10% 25V	MURATA	GRM21BR71E334KA01L
1	C_{FS}	0.1 µF X7R 10% 25V	MURATA	GRM21BR71E104KA01L
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
4	C_{OUT}	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_{REF}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	D1	Schottky 100V 12A	VISHAY	12CWQ10FNPBF
1	L1	22 µH 20% 7.2A	COILCRAFT	MSS1278-223MLB
1	Q1	NMOS 100V 32A	FAIRCHILD	FDD3682
1	Q2	PNP 150V 600 mA	FAIRCHILD	MMBT5401
1	R_{BIAS}	11.5 kΩ 1%	VISHAY	CRCW080511K5FKEA
2	R_{CSH}, R_{OV1}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	10Ω 1%	VISHAY	CRCW080510R0FKEA
1	R_{FLT}	150Ω 1%	VISHAY	CRCW0805150RFKEA
1	R_{GAIN}	5.49 kΩ 1%	VISHAY	CRCW08055K49FKEA
2	R_{HSP}, R_{HSN}	1.0 kΩ 1%	VISHAY	CRCW08051K00FKEA
2	R_{LIM}, R_{SNS}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
2	R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{SLP}	20.5 kΩ 1%	VISHAY	CRCW080520K5FKEA
1	R_T	14.3 kΩ 1%	VISHAY	CRCW080514K3FKEA
1	R_{UV1}	13.7 kΩ 1%	VISHAY	CRCW080513K7FKEA
1	R_{UV2}	150 kΩ 1%	VISHAY	CRCW0805150KFKEA
1	NTC	Thermistor 100 kΩ 5%	TDK	NTCG204H154J

DESIGN #8 - SEPIC Application



Features

- Input: 9V to 36V
- Output: 5 LEDs at 750mA
- 60°C - 120°C Thermal Foldback
- PWM Dimming up to 30 kHz
- 500 kHz Switching Frequency

DESIGN #8 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3424	Boost controller	TI	LM3424MH
1	C_{BYP}	2.2 µF X7R 10% 16V	MURATA	GRM21BR71C225KA12L
3	C_{CMP}, C_{NTC}, C_{SS}	0.47 µF X7R 10% 25V	MURATA	GRM21BR71E474KA01L
0	C_{FS}	DNP		
4	C_{IN}	4.7 µF X7R 10% 100V	TDK	C5750X7R2A475K
4	C_{OUT}	10 µF X7R 10% 50V	TDK	C4532X7R1H106K
1	C_{SEP}	1.0 µF X7R 10% 100V	TDK	C4532X7R2A105K
1	C_{OV}	47 pF COG/NPO 5% 50V	AVX	08055A470JAT2A
1	C_{REF}	1 µF X7R 10% 25V	MURATA	GRM21BR71E105KA01L
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
2	L1, L2	68 µH 20% 4.3A	COILCRAFT	DO3340P-683
2	Q1, Q2	NMOS 60V 8A	VISHAY	SI4436DY
1	Q3	NMOS 60V 115 mA	ON-SEMI	2N7002ET1G
1	R_{BIAS}	23.7 kΩ 1%	VISHAY	CRCW080523K7FKEA
1	R_{CSH}	12.4 kΩ 1%	VISHAY	CRCW080512K4FKEA
1	R_{FS}	0Ω 1%	VISHAY	CRCW08050000OZEA
1	R_{GAIN}	9.31 kΩ 1%	VISHAY	CRCW08059K31FKEA
2	R_{HSP}, R_{HSN}	750Ω 1%	VISHAY	CRCW0805750RFKEA
1	R_{LIM}	0.04Ω 1% 1W	VISHAY	WSL2512R0400FEA
1	R_{OV1}	15.8 kΩ 1%	VISHAY	CRCW080515K8FKEA
1	R_{OV2}	499 kΩ 1%	VISHAY	CRCW0805499KFKEA
2	R_{REF1}, R_{REF2}	49.9 kΩ 1%	VISHAY	CRCW080549K9FKEA
1	R_{SLP}	20.0 kΩ 1%	VISHAY	CRCW080520K0FKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA
1	R_T	14.3 kΩ 1%	VISHAY	CRCW080514K3FKEA
1	R_{UV1}	1.62 kΩ 1%	VISHAY	CRCW08051K62FKEA
1	R_{UV2}	10.0 kΩ 1%	VISHAY	CRCW080510K0FKEA
1	R_{UVH}	16.9 kΩ 1%	VISHAY	CRCW080516K9FKEA
1	NTC	Thermistor 100 kΩ 5%	TDK	NTCG204H154J

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3424MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3424 MH	Samples
LM3424MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3424 MH	Samples
LM3424QMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3424 QMH	Samples
LM3424QMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM3424 QMH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF LM3424, LM3424-Q1 :

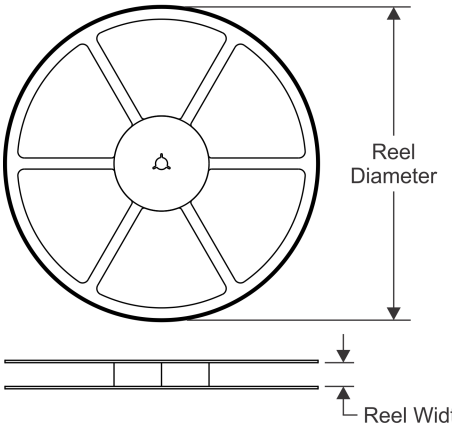
- Catalog: LM3424
- Automotive: LM3424-Q1

NOTE: Qualified Version Definitions:

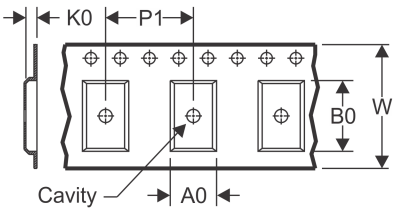
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

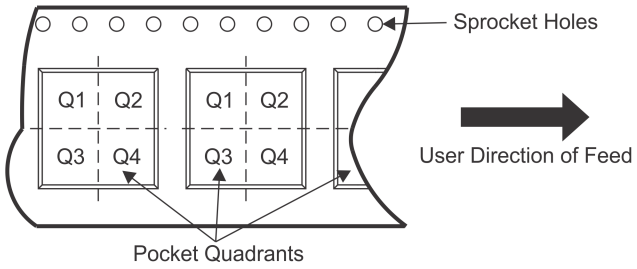


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

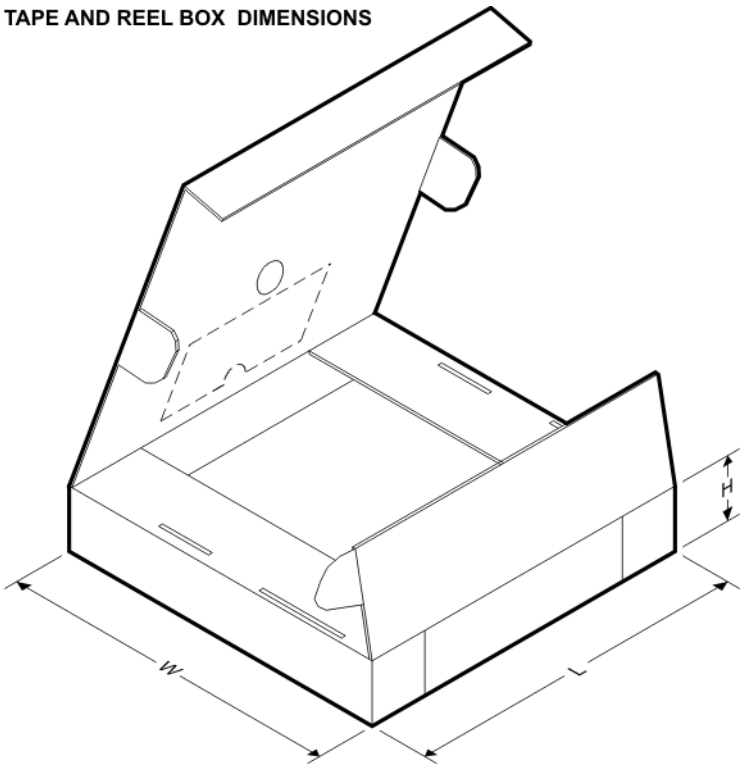
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3424MHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM3424QMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

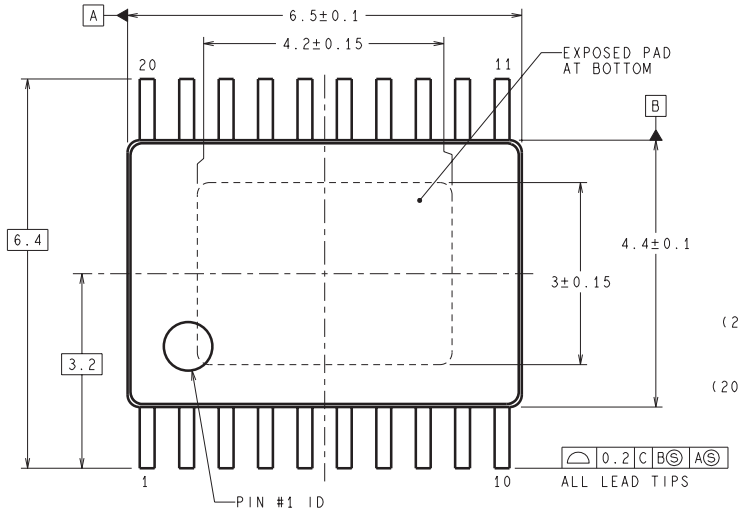
TAPE AND REEL BOX DIMENSIONS

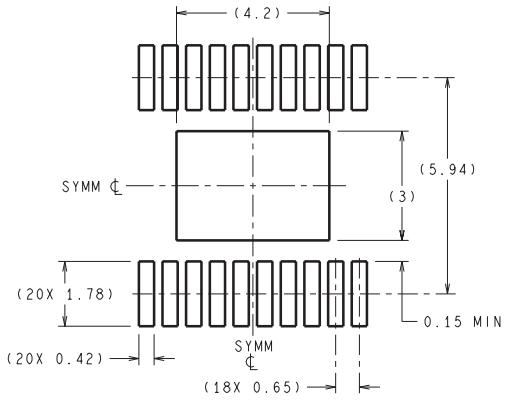


*All dimensions are nominal

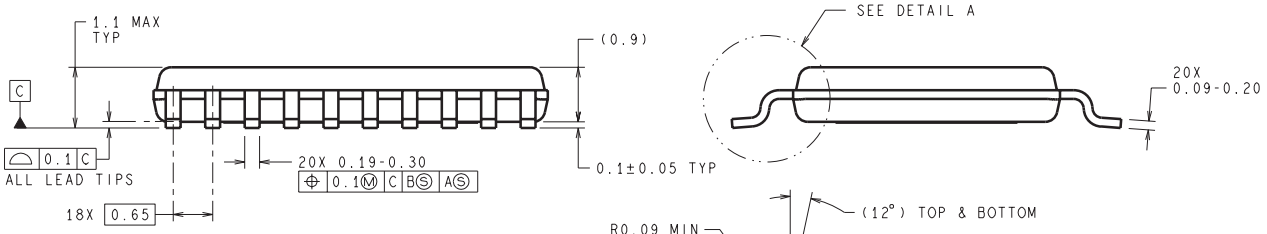
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3424MHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM3424QMHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

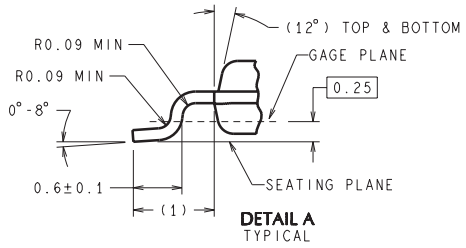
PWP0020A





RECOMMENDED LAND PATTERN





DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MXA20A (Rev C)

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