Voltage Mode Active Clamp Controller

Check for Samples: LM5027A

FEATURES

- **Voltage-Mode Control**
- **Line Feed-Forward PWM Ramp**
- **Internal 105V Rated Start-Up Bias Regulator**
- **Programmable Line Under-Voltage Lockout (UVLO) with Adjustable Hysteresis**
- **Versatile Dual Mode Over-Current Protection**
- **Programmable Volt-Second Limiter and Soft-Start**
- **Programmable Synchronous Rectifier Soft-Start and Stop**
- **Precise 500mV Over-Current Comparator**
- **Current Sense Leading Edge Blanking**
- **Programmable Oscillator With 1 MHz Maximum Frequency and Synchronization Capability**
- **Precision 5V Reference**
- **Programmable Time Delays Between Outputs**
- **A 70% Maximum Duty Cycle**

DESCRIPTION

The LM5027A is a functional variant of the LM5027 active clamp PWM controller. The functional difference of the LM5027A is that the maximum duty cycle of the LM5027A is decreased from 91% to 71%. In addition, the oscillator timing equation has been modified.

The LM5027A pulse-width modulation (PWM) controller contains all of the features necessary to implement power converters utilizing the Active Clamp / Reset technique. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Three control outputs are provided: the main power switch control (OUTA), the active clamp switch control (OUTB), and secondary side synchronous rectifier control (OUTSR). The timing between the control outputs is adjustable with external resistors that program internal precision timers. This controller is designed for high-speed operation including an oscillator frequency range up to 1 MHz and total PWM propagation delays less than 50 ns. The LM5027A includes a high-voltage startup regulator with a maximum input voltage rating of 105V. Additional features include Line Under Voltage Lockout (UVLO), separate soft-start of main and synchronous rectifier outputs, a timer for hiccup mode current limiting, a precision reference, and thermal shutdown.

Packages

- HTSSOP-20
- WQFN-24

Typical Application Circuit

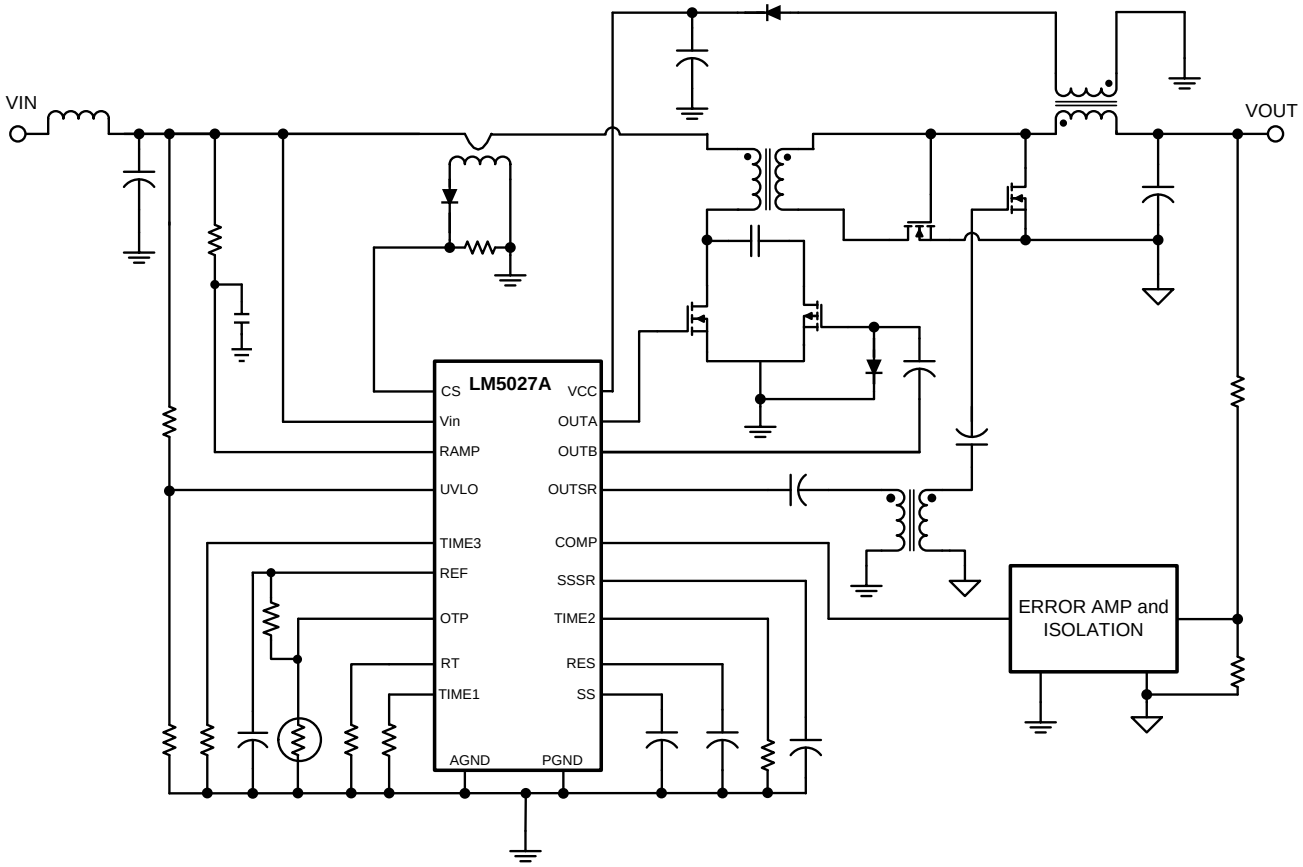


Figure 1. Simplified Active Clamp Converter

Connection Diagram

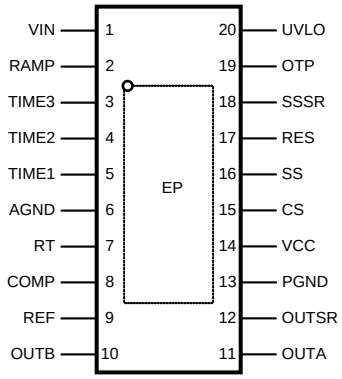


Figure 2. 20-Lead HTSSOP

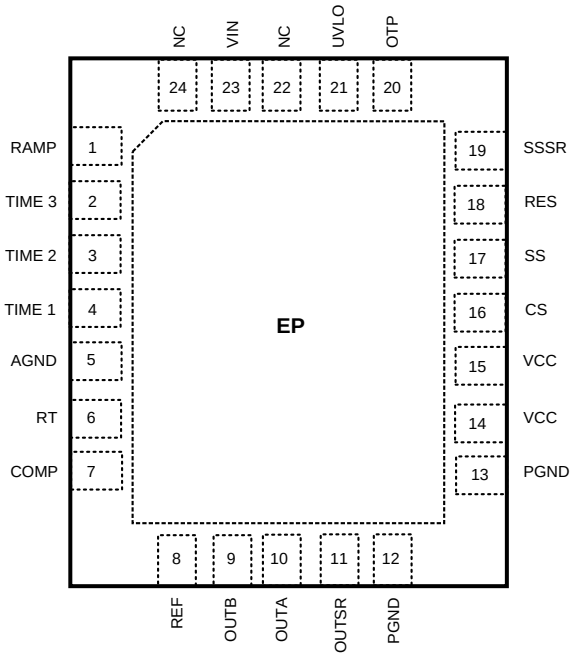


Figure 3. 24-Lead WQFN

Table 1. Pin Descriptions

Pin(1)	Name	Description	Application Information
1	VIN	Input voltage source	Input to the Start-up Regulator. Operating input range is 13V to 90V. The Absolute Maximum Rating is 105V. For power sources outside of this range, the LM5027A can be biased directly at VCC by an external regulator.
2	RAMP	Feed-forward modulation ramp	An external RC circuit from VIN sets the PWM ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET. An internal comparator terminates the PWM pulse if the RAMP pin exceeds 2.5V thus limiting the maximum volt-second product to the transformer primary.
3	TIME3	Overlap delay 3	An external resistor sets the overlap delay for the active clamp output. The R_{TIME3} resistor connected between TIME3 and AGND sets the OUTA turn-off (falling edge) to OUTB turn-on (falling edge) pulse delay. See Figure 26.
4	TIME2	Overlap delay 2	An external resistor sets the overlap delay for the OUTSR output. The R_{TIME2} resistor connected between TIME2 and AGND sets the OUTA turn-off (falling edge) to OUTSR turn-on (rising edge) pulse delay. See Figure 26.
5	TIME1	Overlap delay 1	An external resistor sets the overlap delay for the active clamp output. The R_{TIME1} resistor connected between TIME1 and AGND sets the OUTB and OUTSR turn-off to OUTA turn-on pulse delay. See Figure 26.
6	AGND	Analog ground	Connect directly to Power Ground.
7	RT	Oscillator frequency control and sync clock input	Normally biased at 2V by an internal amplifier. An external resistor connected between RT and AGND sets the internal oscillator frequency. The internal oscillator can be synchronized to an external clock with a frequency higher than the free running frequency set by the RT resistor.
8	COMP	Input to the pulse width modulator	An external opto-coupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is at its maximum value with zero input current, while 1mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the ac voltage across the opto-coupler detector transistor.
9	REF	Reference Output	Output of a 5V reference. Maximum output current is 10 mA. Locally decouple with a 0.1 µF capacitor.

(1) Note: The pin numbers shown are only for the HTSSOP package.

Table 1. Pin Descriptions (continued)

Pin(1)	Name	Description	Application Information
10	OUTB	Output driver	Control output of the active clamp PFET gate. Capable of 1A peak source and sink current.
11	OUTA	Output driver	Control output of the main PWM NFET gate. Capable of 2A peak source and sink current.
12	OUTSR	Output driver	Control output of the secondary side synchronous rectifier FET gates. Capable of 3A peak source and sink current.
13	PGND	Power ground	Connect directly to Analog Ground
14	VCC	Start-up regulator output	Output of the internal high voltage start-up regulator. Regulated at 9.5V during start-up and 7.5V during run mode. If the auxiliary winding raises the voltage on this pin above the regulation set point, the internal start-up regulator will shutdown, thus reducing the IC power dissipation.
15	CS	Current sense input	Current sense input for cycle-by-cycle current limiting. If the CS pin exceeds 500mV the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 100 ns after OUTA switches high to blank leading edge transients.
16	SS	Soft-start Input	An internal 22 µA current source charges an external capacitor to set the soft-start rate.
17	RES	Restart timer	If cycle-by-cycle current limit is reached during any cycle, a 22 µA current is sourced into the RES capacitor. If the RES capacitor voltage charges to 1.0V, a hiccup sequence is initiated. The SS and SSSR capacitors are discharged and the control outputs are disabled. The voltage on the RES capacitor is ramped between 4V and 2V eight times. After the eighth cycle, the SS capacitor is released and the normal start-up sequence begins.
18	SSSR	Soft-start for synchronous rectifier output.	An external capacitor and an internal 25 µA current source sets the soft-start and soft-stop ramps for the synchronous rectifier output (OUTSR).
19	OTP	Over-Temperature Protection	The OTP comparator can be used for over-temperature shutdown protection with an external NTC thermistor voltage divider setting the shutdown temperature. The OTP comparator threshold is 1.25V. Hysteresis is set by an internal current source that sources 20 µA into the external resistor divider when the OTP pin voltage is above the threshold.
20	UVLO	Line under-voltage lockout	An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4V threshold, the VCC and REF regulators are enabled. When UVLO reaches the 2.0V threshold, the SS pin is released and the device enters the active mode. Hysteresis is set by an internal current source that pulls 20 µA from the external resistor divider when the UVLO pin is below the 2.0V threshold.
	EP	Exposed pad, underside of package	No electrical contact to the LM5027A integrated circuit. Connect to system ground plane for reduced thermal resistance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN to GND	-0.3V to 105V
VCC to GND	-0.3V to 16V
UVLO to GND	-0.3 to 8V
All other inputs to GND	-0.3 to 7V
COMP Input Current	10 mA
COMP, REF (3)	
ESD Rating, Human Body Model(4)	2kV
Storage Temperature Range	-55°C to 150°C
Junction Temperature	150°C

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(3) It is not recommended that external power sources be connected to these pins.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings(1)

VIN	13 to 90V
VCC	8 to 15V
Operating Junction Temperature	-40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 48V, VCC = 10V, RT= 38.4K , No Load on OUTA, OUTB and OUTSR unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN SUPPLY						
Ibias	VIN Operating Current	COMP and VCC Open, UVLO and OTP = 3V			**6.8**	mA
	VIN Shutdown Current	UVLO = 0V, Vin = 100 V		310	**650**	µA
VCC REGULATOR						
	VCC Regulation	No Load (SS<4V)	**9.1**	9.5	**9.9**	V
	VCC Current Limit	VCC=9.5V	**55**	65		mA
	VCC Regulator load regulation	IVCCREG 0 to 15 mA		75		mV
	VCC Under-voltage Lockout Voltage	Positive going VCC	**VccReg –180mV**	VccReg – 100mV		V
VccReg	VCC Regulation	No Load	**7.3**	7.5	**7.7**	V
	VCC Under-voltage Lockout Voltage	Negative going Vcc	**5.7**	6.0	**6.3**	V
	VCC Supply Current (Icc)	Supply current into VCC form an external source, CGATE = OPEN, VCC 10V			**6**	mA
REFERENCE SUPPLY						
	Reference Voltage	IREF = 0mA	**4.85**	5.0	**5.15**	V
	Reference Voltage Regulation	IREF= 0 to 10mA		10	**20**	mV
	Reference Current Limit		**10**	17.5		mA
	REF Under-voltage Threshold	UVLO >0.4V, VCC >9.5V	**3.8**			V

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 48V, VCC = 10V, RT= 38.4K , No Load on OUTA, OUTB and OUTSR unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
UVLO/OTP THRESHOLDS						
	UVLO Threshold		**1.9**	2	**2.1**	V
	UVLO Hysteresis Current	UVLO	**16**	20	**25**	µA
	UVLO Shutdown Threshold	ULVLO voltage falling		0.3		V
	UVLO Standby Enable Threshold	UVLO voltage rising		0.4		V
	OTP Shutdown Threshold	OTP rising	**1.21**	1.25	**1.29**	V
	OTP Hysteresis Current	OTP	**15**	20	**24**	µA
SOFT-START						
	SS Charging Current Source	SS = 0V	**17**	22	**26**	µA
	SS Rising Threshold for SSSR charge current enable		**3.85**	4.05	**4.25**	V
	SSSR Charging Current Source	SSSR = 0V, SS>4V	**18**	25	**30**	µA
	SSSR Discharge Current Source in Soft Stop		**14**	20	**26**	µA
	SSSR Falling Threshold for SS Soft Stop		**1.5**	2.2	**3.0**	V
	SS output low voltage	Sinking 100 µA UVLO = 0		120		mV
	SSSR output low voltage			100		mV
OSCILLATOR						
	Frequency1	RT = 38.4 kΩ	**275**	310	**345**	kHz
	Sync Threshold			2.85		V
	Sync Pulse Width		**15**		**150**	ns
PWM COMPARATORS						
	Delay to Output			50		ns
	COMP to PWM Offset			1.0		V
	Duty Cycle Maximum	OUTA, OUT_A = Tdelay_min	**70**	72.5	75	%
CURRENT LIMIT RESTART (RES Pin)						
	RES Threshold			1.1		V
	Charge Source Current Level 1	V_{RES} < 1.0V		22	**26**	µA
	Charge Source Current Level 2	4.0V < VRES > 1.0V	**4**	5.0	**6.5**	µA
	Discharge Current Source	V_{RES} ramping down	**4**	5	**7**	µA
	Ratio of RES Threshold to SS Low	V_{RES} > 1V, Hiccup counter		125		
CURRENT LIMIT						
	Cycle by cycle sense voltage threshold	RAMP = 0	**450**	500	**550**	mV
CS prop	Current limit propagation delay	CS step from 0 to 0.6V time to onset of OUTA transition (90%) Cgate = 0pen		30		ns
VOLTAGE FEED-FORWARD (RAMP Pin)						
	RAMP Discharge Device	$R_{DS(ON)}$		5		Ω
VOLT-SECOND CLAMP						
	Ramp Clamp Level	Delta RAMP measured from onset of OUTA to Ramp peak. Comp = 5V	**2.3**	2.5	**2.6**	V

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature range of –40°C to +125°C. Unless otherwise specified, the following conditions apply: VIN = 48V, VCC = 10V, RT= 38.4K , No Load on OUTA, OUTB and OUTSR unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTA GATE DRIVER						
VOL	OUTA Low-state Output Voltage	I_{OUTA} = 100 mA		0.15	**0.5**	V
VOH	OUTA High-state Output Voltage	I_{OUTA} = -100 mA, VOHL = VCC -VLO	**0.35**	0.21		V
	OUTA Rise Time	C-load = 1000 pF		10		ns
	OUTA Fall Time	C-load = 1000 pF		13		ns
IOHL	Peak OUTA Source Current	V_{OUTA} = 0V (VCC = 10V)		2		A
IOLL	Peak OUTA Sink Current	V_{OUTA} = VCC= 10V		2		A
OUTB GATE DRIVER						
VOL	OUTB Low-state Output Voltage	I_{OUTB} = 100 mA		0.2	**0.4**	V
VOH	OUTB High-state Output Voltage	I_{OUTB} = -100 mA, VOHL = VCC -VLO	**0.5**	0.31		V
	OUTB Rise Time	C-load = 1000 pF		15		ns
	OUTB High Side Fall Time	C-load = 1000 pF		13		ns
IOHL	Peak OUTB Source Current	V_{OUTB} = 0V (VCC = 10V)		1		A
IOLL	Peak OUTB Sink Current	V_{OUTB} = VCC= 10V		1		A
OUTSR GATE DRIVER						
VOL	OUTSR Low-state Output Voltage	I_{OUTSR} = 100 mA		0.1	**0.2**	V
VOH	OUTSR High-state Output Voltage	I_{OUTSR} = -100 mA, VOHL = VCC -VLO	**0.25**	0.11		V
	OUTSR Rise Time	C-load = 1000 pF		12		ns
	OUTSR High Side Fall Time	C-load = 1000 pF		10		ns
IOHH	Peak OUTSR Source Current	V_{OUTSR} = 0V (VCC = 10V)		3		A
IOLH	Peak OUTSR Sink Current	V_{OUTSR} = VCC= 10V		3		A
OUTPUT TIMING CONTROL						
T1	Delay Leading Range	R_{TIME1}=10 kΩ – 100 kΩ	**30**		**300**	ns
T1	Delay Leading Accuracy	R_{TIME1} = 33.2 kΩ	**75**	100	**125**	ns
T2	Delay Trailing Range	R_{TIME2} = 10 kΩ – 100 kΩ	**30**		**300**	ns
T2	Delay Trailing Accuracy	R_{TIME2} = 28.7 kΩ	**75**	100	**125**	ns
T3	Delay Leading Range	R_{TIME3} = 10 kΩ – 100 kΩ	**30**		**300**	ns
T3	Delay Leading Accuracy	R_{TIME3} = 29.4 kΩ	**75**	100	**125**	ns
THERMAL						
t_{sd}	Thermal Shutdown Temp.		**150**	165		°C
	Thermal Shutdown Hysteresis			25		°C
RJA	Junction to Ambient			40		°C/W
RJC	Junction to Exposed Pad			4		°C/W

Typical Performance Characteristics

Efficiency

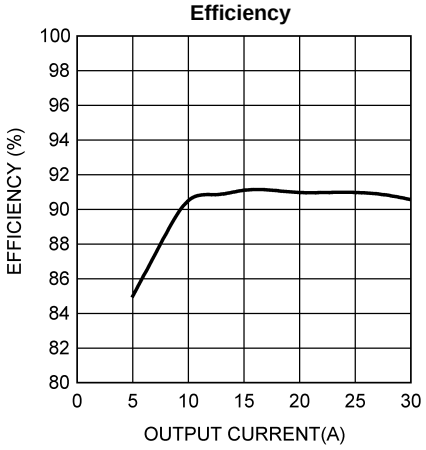


Figure 4.

VCC and V_{REF} vs. VIN

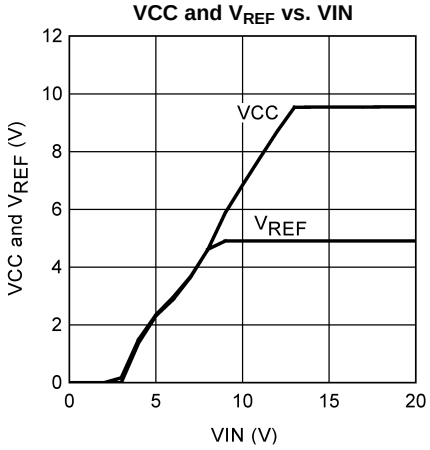


Figure .

VCC vs. I_{CC}

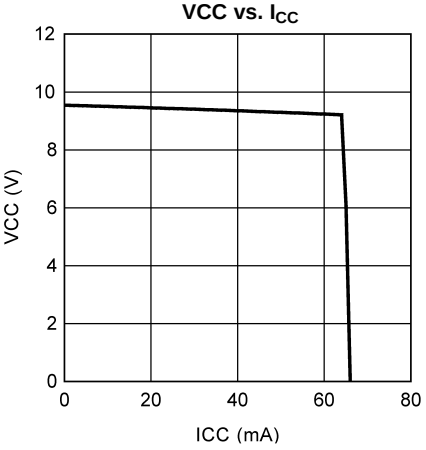


Figure 5.

V_{REF} vs. I_{REF}

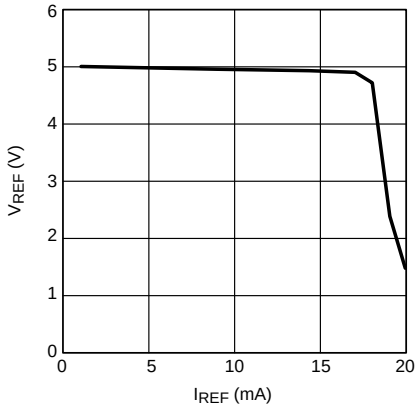


Figure 6.

Oscillator Frequency vs R_T Resistor

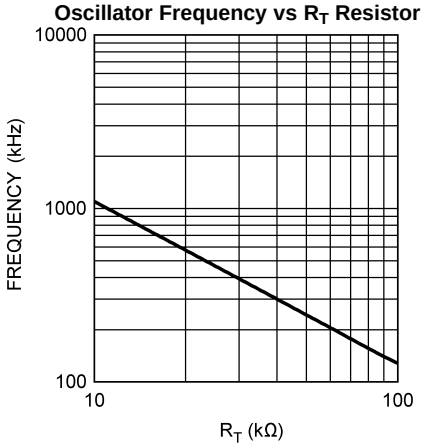


Figure 7.

Oscillator Frequency vs Temperature

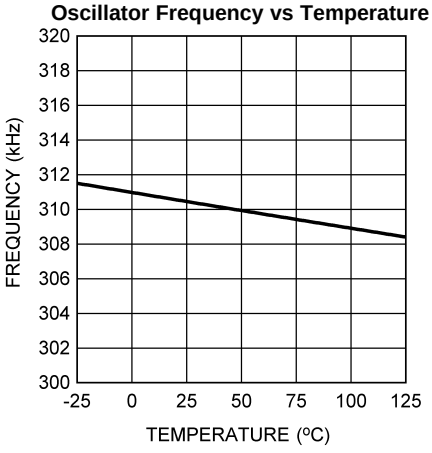


Figure 8.

Typical Performance Characteristics (continued)

Time1 Delay vs R_{TIME1} (kΩ)

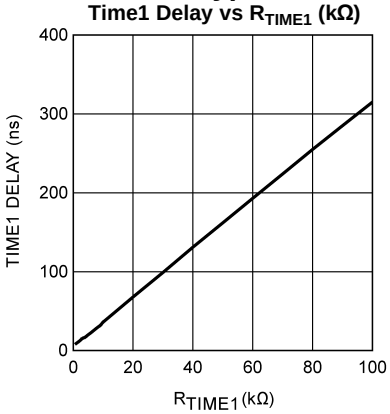


Figure 9.

Time2 Delay vs R_{TIME2} (kΩ)

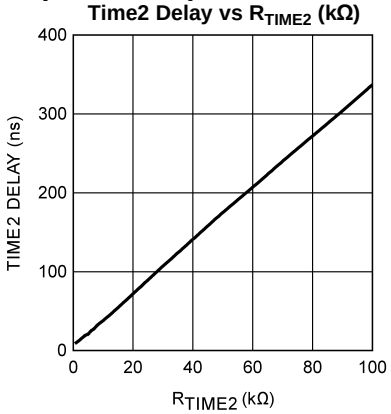


Figure 10.

Time3 Delay vs R_{TIME3} (kΩ)

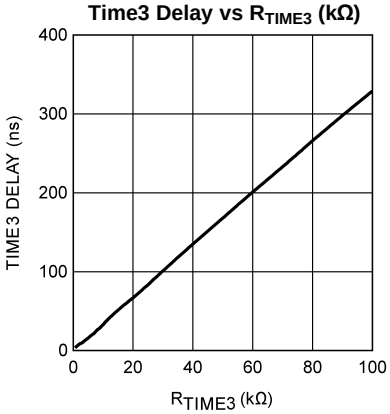


Figure 11.

Time1 Delay vs Temperature
R_{TIME1} = 33.2 kΩ

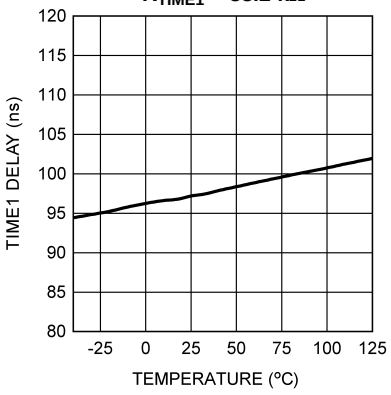


Figure 12.

Time2 Delay vs Temperature
R_{TIME2} = 28.7 kΩ

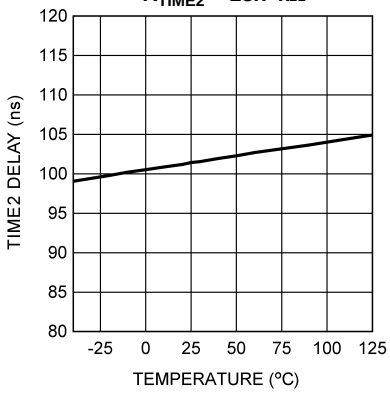


Figure 13.

Time3 Delay vs Temperature
R_{TIME3} = 29.4 kΩ

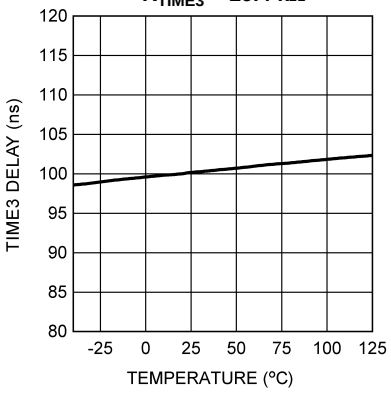


Figure 14.

Typical Performance Characteristics (continued)

SS Pin Current vs Temperature

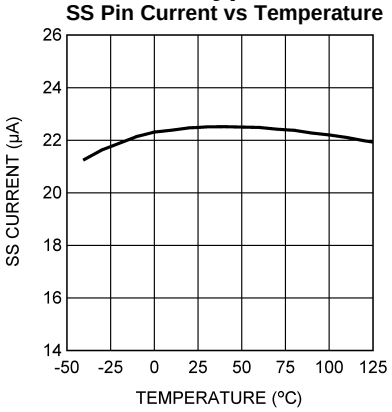


Figure 15.

SSSR Pin Charging Current vs Temperature

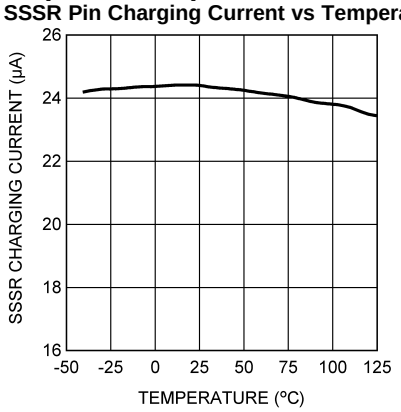


Figure 16.

RES Pin Charging Current Level 1 vs Temperature

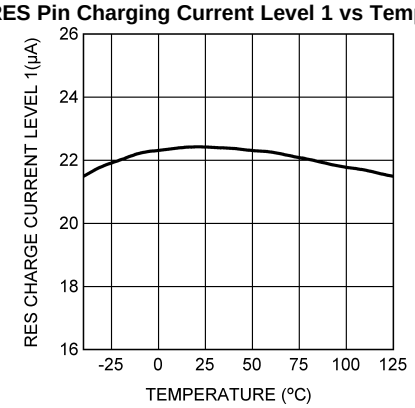


Figure 17.

BLOCK DIAGRAM

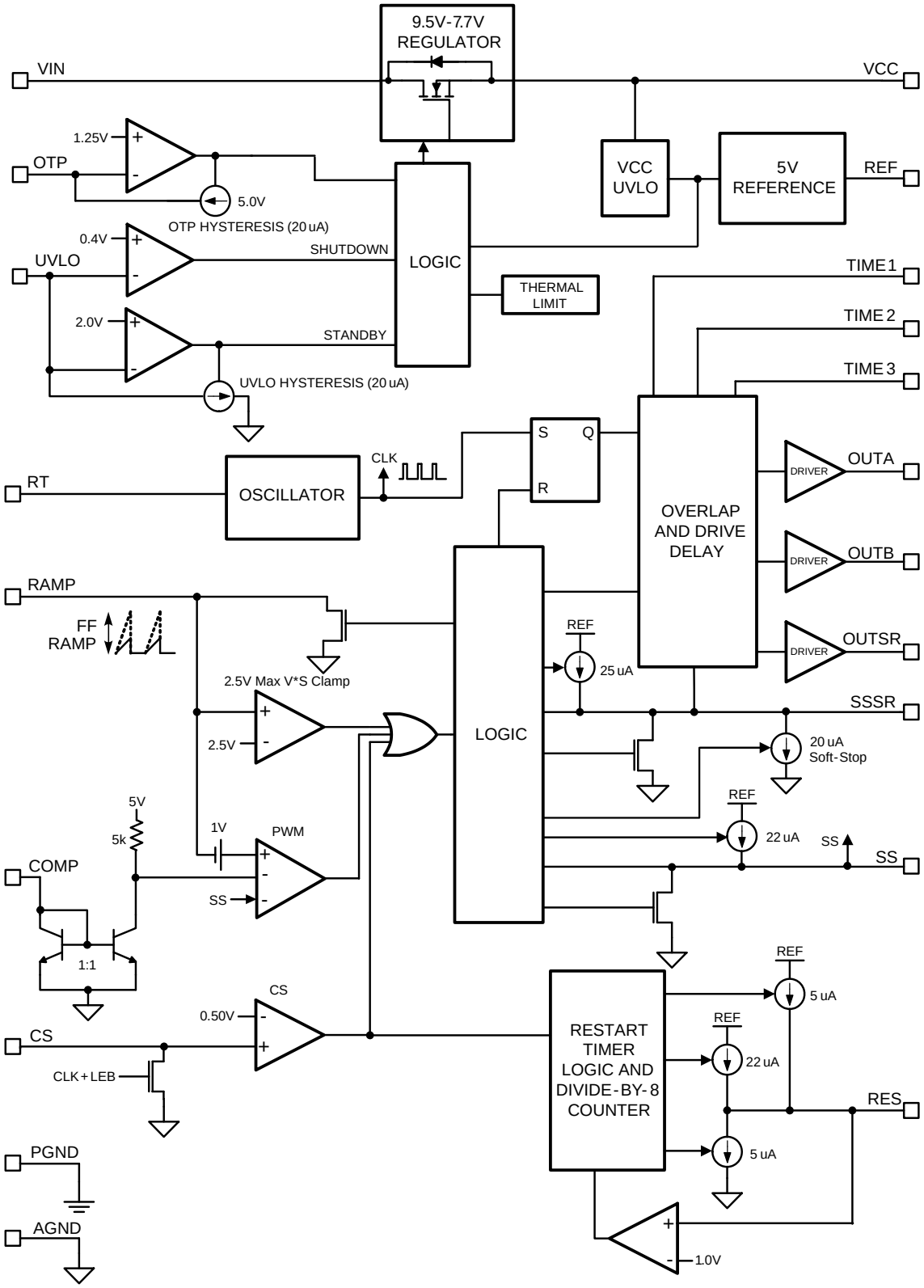


Figure 18. Simplified Block Diagram

DETAILED OPERATING DESCRIPTION

The LM5027A PWM controller contains all the features necessary to implement power converters utilizing the Active Clamp Reset technique with synchronous rectification. The device is configured to control a P-Channel clamp switch. With the active clamp technique higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. The LM5027A provides three gate driver outputs: one to drive the primary side MOSFET (OUTA), one for the active clamp P-Channel MOSFET (OUTB), and one output to drive the synchronous rectifier through an isolation interface (OUTSR). This controller is designed for high-speed operation including an oscillator frequency range up to 1 MHz and total PWM and current sense propagation delay less than 50 ns. The LM5027A includes a high-voltage start-up regulator that operates over a wide input range of 13V to 90V. Additional features include: Line Under-Voltage lockout (UVLO), soft-start/soft-stop, oscillator with synchronization capability, cycle-by-cycle current limit, hiccup mode fault protection with adjustable delay, precision reference, and thermal shutdown.

High Voltage Start-Up Regulator

The LM5027A contains an internal high voltage start-up regulator that allows the input pin (VIN) to be connected directly to the line voltage. The regulator output is internally current limited to 55mA. When the UVLO pin potential is greater than 0.4V, the VCC regulator is enabled to charge an external capacitor connected to the VCC pin. The VCC regulator provides power to the voltage reference (REF) and the gate drivers (OUTA, OUTB, and OUTSR). The controller outputs are enabled when the voltage on the VCC pin reaches the regulation point of 9.5V, the internal voltage reference (REF) reaches its regulation point of 5V, the UVLO pin voltage is greater than 2V, and the OTP pin voltage is greater than 1.25V. The outputs will remain enabled unless one of the following conditions occurs, VCC falls below 6.0V, UVLO is below 2.0 V, or the OTP pin falls below 1.25V. The value selected for the VCC capacitor depends on the total system design and the start-up characteristics. The recommended capacitance range for the VCC regulator is 0.1 µF to 100 µF. In a typical application, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above the VCC regulation set point to shut off the internal start-up regulator. The LM5027A lowers the VCC regulation set point from 9.5V to 7.5V after the output of the first OUTSR drive pulse. Powering VCC from an auxiliary winding improves efficiency while reducing the controller power dissipation. When the converter auxiliary winding is inactive, external current draw on the VCC line should be limited so the power dissipation in the start-up regulator does not exceed the maximum power dissipation of the LM5027A package. An external start-up regulator or other bias rail can be used instead of the internal start-up regulator by connecting the VCC and the VIN pins together and feeding the external bias into the two pins.

Line Under-Voltage Detector

The LM5027A contains a dual level line Under Voltage Lock Out (UVLO) circuit. When the UVLO pin voltage is greater than 0.4V but less than 2.0V, the controller is in a standby mode. In the standby mode the VCC and REF bias regulators are active while the controller outputs are disabled. This feature allows the UVLO pin to be used as a remote enable/disable function. Pulling the UVLO pin below the 2.0V threshold initiates a soft-stop sequence described later in this document. There is 100mV of hysteresis provided in the 0.4V shutdown comparator. When the VCC and REF outputs exceed their respective under-voltage thresholds and the UVLO pin voltage is greater than 2.0V and the OTP pin voltage is greater than 1.25V, the outputs are enabled and normal operation begins. An external set-point voltage divider from the VIN to GND can be used to set the minimum operating voltage of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 2.0V when Vin is in the desired operating range. If the under-voltage threshold is not met, all three outputs are disabled. UVLO hysteresis is accomplished with an internal 20 µA current sink that is switched on or off into the impedance of the set-point divider. When the UVLO pin voltage exceeds 2.0V threshold, the current sink is deactivated to quickly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.0V threshold, the current sink is turned on causing the voltage at the UVLO pin to quickly fall .

Reference

The REF pin is the output of a 5V linear regulator that can be used to bias an opto-coupler transistor and external house-keeping circuits. The regulator output is internally current limited to 10 mA.

Cycle-by-Cycle Current Limit

The CS pin is to be driven by a signal representative of the transformer primary current. If the voltage on the CS pin exceeds 0.5V, the current sense comparator terminates the output driver pulse, with the duty cycle determined by the current sense comparator instead of the PWM comparator. A small R-C filter connected to the CS pin and located near the controller is recommended to suppress noise. An internal 5Ω MOSFET discharges the external current sense filter capacitor at the conclusion of every cycle. The discharge MOSFET remains on for an additional 30 ns after either OUTA driver switches high to blank leading edge transients in the current sensing circuit. Discharging the CS pin filter each cycle and blanking leading edge spikes reduces the filtering requirements and improves the current sense response time. The current sense comparator is very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the CS and AGND pins. If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network, which should be located close to the IC. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the AGND pin, and a single connection should be made to the power ground (sense resistor ground point).

Restart Time Delay (Hiccup Mode)

The LM5027A provides a current limit restart timer to disable the outputs and force a delayed restart (hiccup mode) if a current limit condition is repeatedly sensed. The number of cycle-by-cycle current limit events required to trigger the restart is programmable by the external capacitor at the RES pin. During each PWM cycle, the LM5027A either sources or sinks current from the RES pin capacitor. If no current limit is detected during a cycle, a 5 µA current sink is enabled to pull the RES pin to ground. If a current limit is detected, the 5 µA current sink is disabled and a 22 µA current source causes the voltage at the RES pin to gradually increase. If the RES voltage reaches the 1.0V threshold, the following restart sequence occurs (also see Figure 19).

- The SS and SSSR capacitors are fully discharged.
- The RES 20 µA current source is turned-off and the 5 µA current source is turned-on.
- The voltage on the RES pin is allowed to charge up to 4.0V.
- When voltage on the RES pin reaches 4.0V the 5 µA current source is turned-off and a 5 µA current sink is turned-on, ramping the voltage on the RES capacitor down to 2.0V.
- The RES capacitor voltage is ramped between 4.0V and 2.0V eight times.
- When the counter reaches eight, the RES pin voltage is pulled low and the Soft-Start capacitor is released to begin a soft-start sequence. The SS capacitor voltage slowly increases. When the SS voltage reaches 1.0V, the PWM comparator will produce the first narrow output pulse at OUTA.
- When the SS voltage reaches 4.0V the capacitor on the SSSR pin is released and is charged with a 25 µA current source, soft-starting the free-wheeling synchronous rectifier.
- If the overload condition persists after restart, cycle-by-cycle current limiting will begin to increase the voltage on the RES capacitor again, repeating the hiccup mode sequence.
- If the overload condition no longer exists after restart, the RES pin will be held at ground by the 5 µA current sink and normal operation resumes.

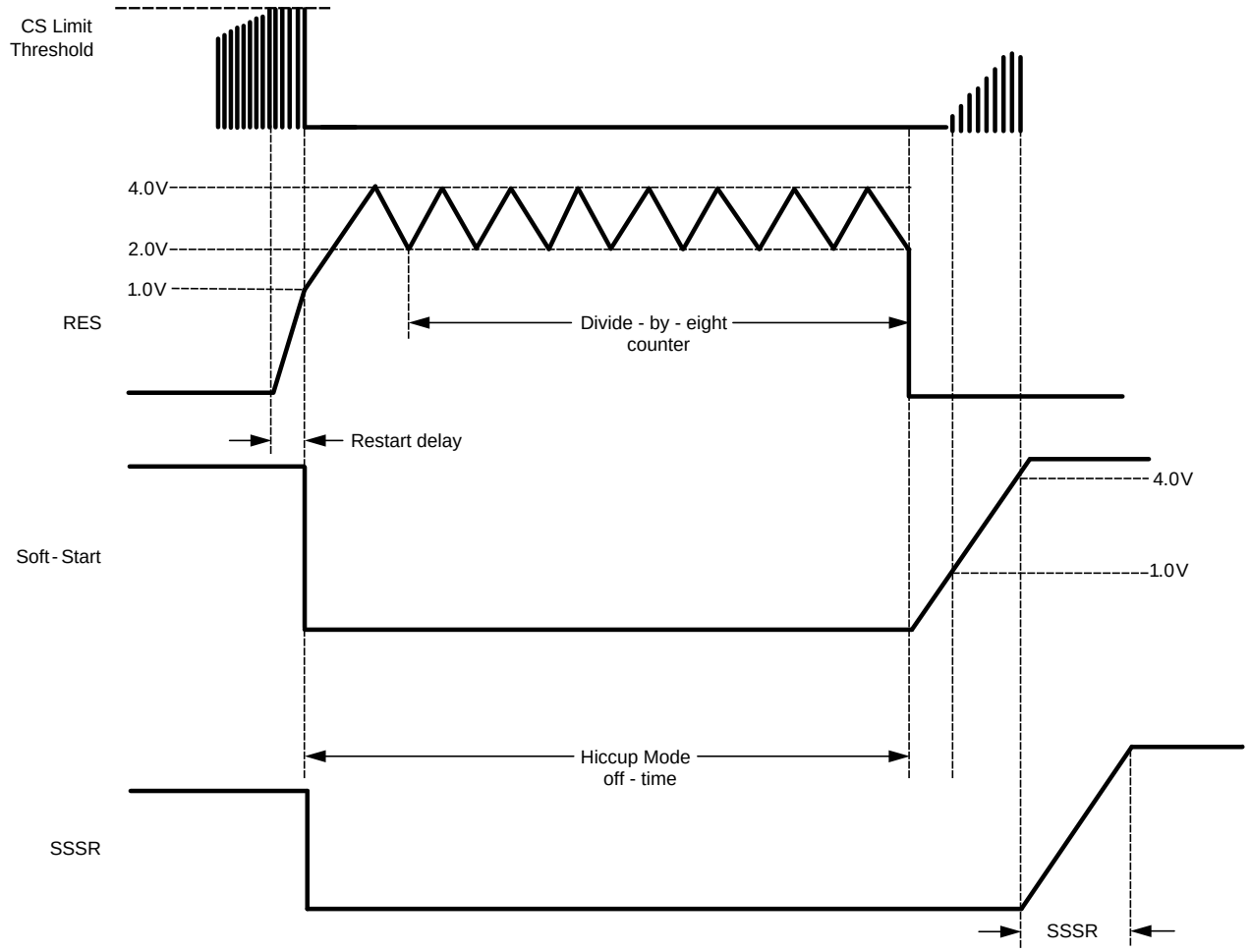


Figure 19. Restart and Soft-Start Delay Timing

Soft-Start

The soft-start circuit allows the regulator to gradually increase its output voltage until the steady state operating point is reached; thereby reducing start-up stresses and surge currents. When bias power is supplied to the LM5027A, the SS pin capacitor is discharged by an internal MOSFET. When the voltages on the UVLO, OTP, VCC, and REF pins reach the operating thresholds, the soft-start capacitor is released and is charged with a 22 µA current source. When the SS pin voltage reaches 1V, output pulses commence with a slowly increasing duty cycle (refer to Figure 20, Figure 21 and Figure 22). The voltage on the SS pin eventually increases to 5V, while the voltage at the PWM comparator is limited to the level required for regulation as determined by the voltage feedback loop via the COMP pin. When the soft-start voltage reaches 4.0V, the capacitor on the SSSR pin is released and charged with a 25 µA current source (refer to Figure 20, Figure 21 and Figure 22) . When the SSSR pin voltage reaches approximately 2.5V (refer to Figure 23), the internal synchronous rectifier PWM circuit gradually increases the synchronous rectifier drive duty cycle (OUTSR) in proportion the rising SSSR pin voltage. Delaying the start of the SSSR gate drive pulses until after the main soft-start is completed allows the output voltage to reach regulation before the synchronous rectifiers begins operation. This delay prevents the synchronous rectifier from sinking current from the output in applications where the output voltage may be pre-biased.

Soft-Stop

If the UVLO pin voltage falls below the 2.0V standby threshold, but above the 0.4V shutdown threshold, the synchronous rectification soft-start capacitor is discharged with a 20 µA current source which gradually disables the synchronous rectifiers (refer to Figure 21). After the SSSR capacitor has been discharged to 2.0V the soft-start and synchronous rectification soft-start capacitors are quickly discharged to ground to terminate PWM pulses at OUTA ,OUTB, and OUTSR. The PWM pulses may cease before the SSSR voltage reduces the synchronous rectifier duty cycle if the VCC or REF voltage drops below the respective under-voltage thresholds during the soft-stop process. This soft-stop method of turning off the converter prevents oscillations in the synchronous rectifiers during a shutdown sequence.

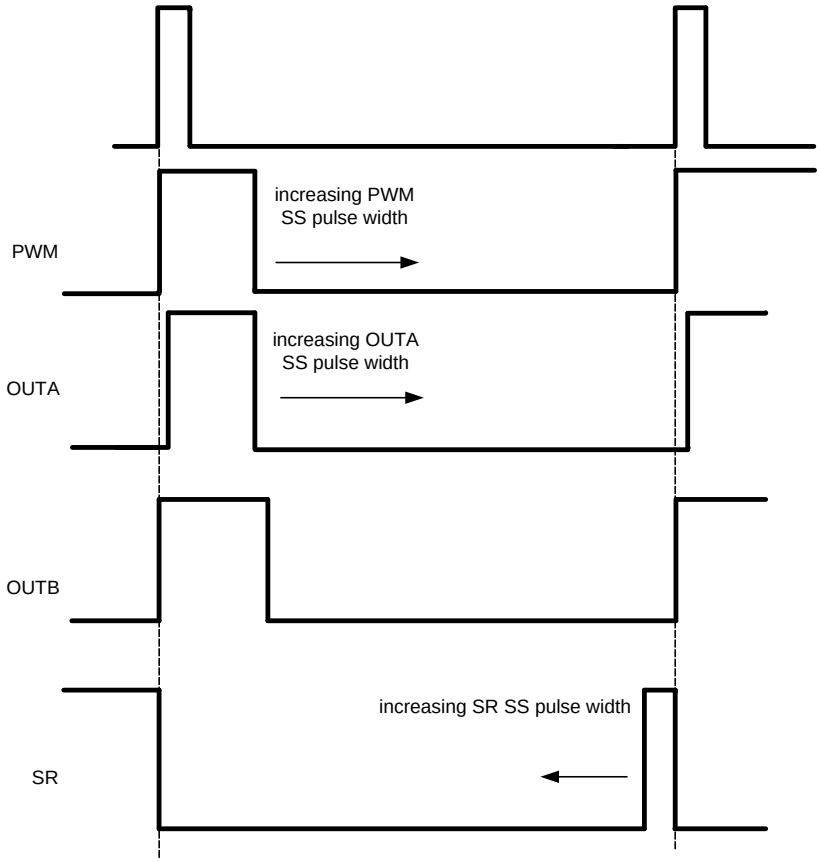


Figure 20. Soft-Start Timing

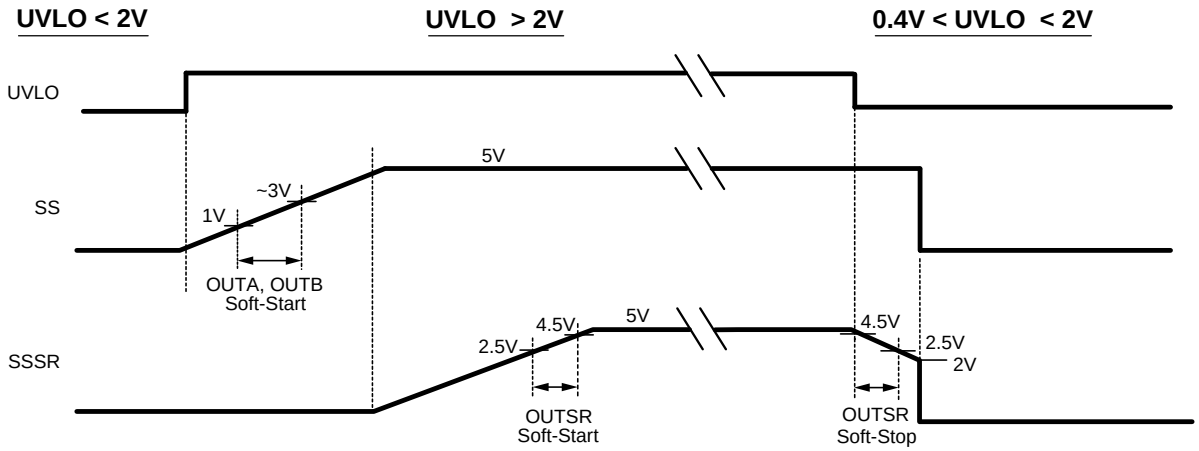


Figure 21. Soft-Start/Soft-Stop Timing

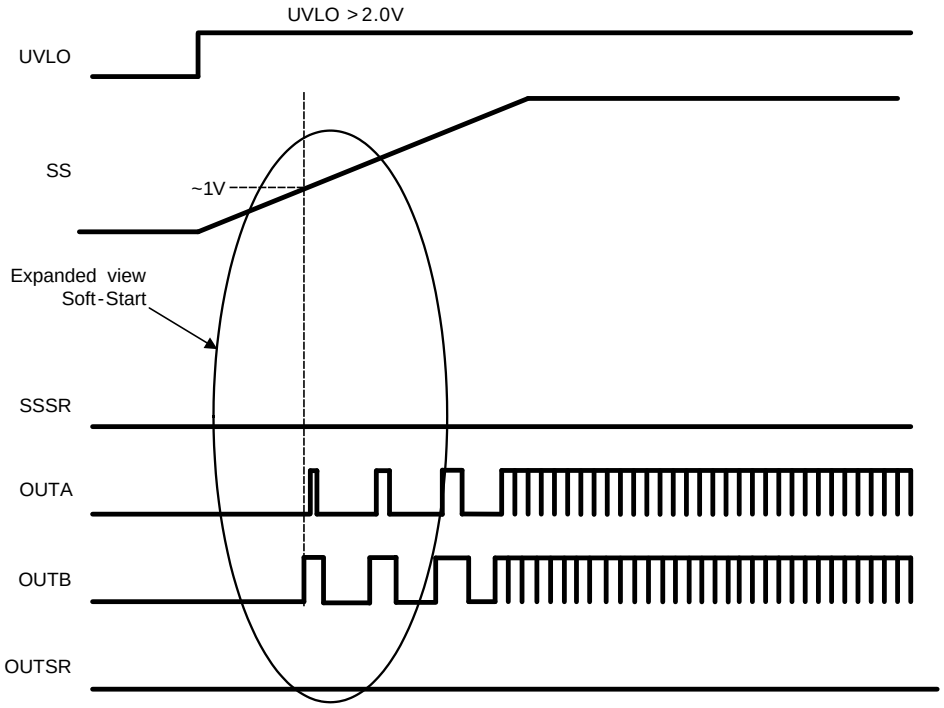


Figure 22. Soft-Start and Drive Enable

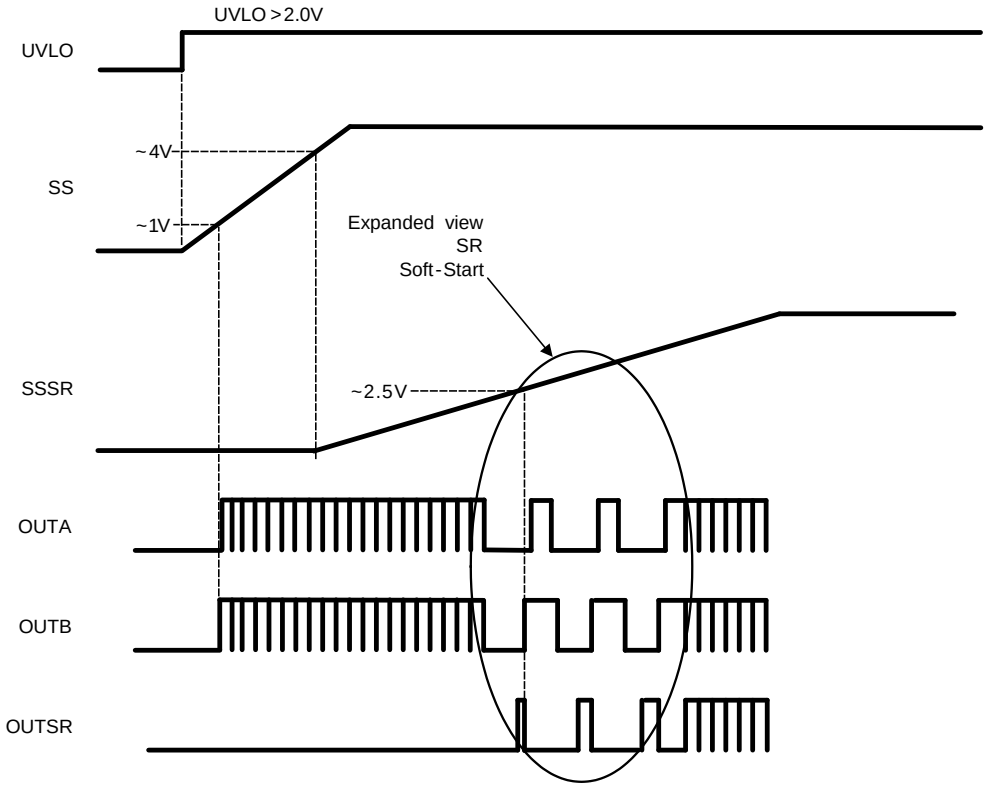


Figure 23. Soft-Start Synchronous Rectifier Timing

External Over-Temperature Protection

An external set-point voltage divider between the REF, OTP, and AGND pins, as shown in Figure 24, is one method to implement over-temperature protection shutdown. Typically a NTC thermistor is installed as the lower device of the voltage divider. The divider must be designed such that the voltage at the OTP pin will be greater than 1.25V when there is not an over-temperature condition, and the OTP pin must drop below 1.25V during an over-temperature event. OTP hysteresis is accomplished with an internal 20 µA current source that is switched on or off into the impedance of the external set-point divider. When the OTP pin voltage exceeds 1.25V threshold, the current source is activated to quickly raise the voltage at the OTP pin. When the OTP pin voltage falls below the 1.25V threshold, the current source is turned off causing the voltage at the OTP pin to quickly fall. When OTP falls below 1.25V the LM5027A will go through a soft-stop turn-off sequence.

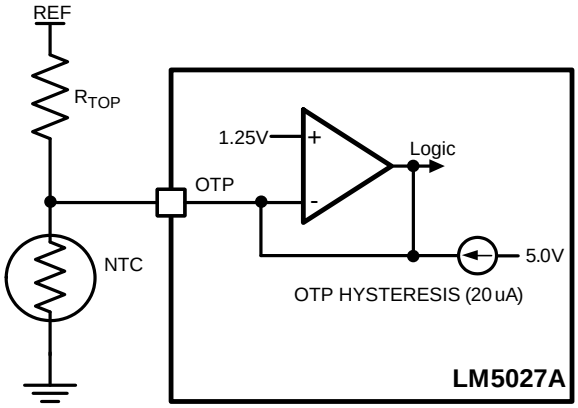


Figure 24. External OTP Protection

Fault/Events Summary

Table 2 is a Truth Table which describes the faults and events that control the LM5027A drive outputs. For example the first event is with UVLO being pulled below 0.4V, a possible remote shutdown condition. When this occurs the SS, and SSSR capacitors are discharged, and the three drive outputs will stop switching (outputs low). The last fault is if the OTP pin is pulled low <1.25V, this would occur if an OTP protection circuit is used, see Figure 24. In an OTP event, the LM5027A goes into a soft-stop shutdown.

Table 2. Fault/Event Summary

Fault/Event	Vcc	UVLO	OTP	SS	SSSR	OUTA	OUTB	OUTSR
UVLO<0.4V	>6.2V	-	>1.25V	Fast discharge	Fast discharge	Low	Low	Low
2.0V<UVLO>0.4V	>6.2V	-	>1.25V	Fast discharge after SSSR<2V	Slow discharge	Low	Low	Low
SS<1V	>6.2V	>2.0V	>1.25V	-	Fast discharge	Low	Low	Low
SSSR<2.0V	>6.2V	>2.0V	>1.25V	>4.0V	-	Switching	Switching	Low
OTP<1.25V	>6.2V	>2.0V	-	Fast discharge after SSSR<2V	Slow discharge	Low	Low	Low

PWM Comparators

The pulse width modulator (PWM) comparator compares the voltage ramp signal at the RAMP pin to the loop error signal. The loop error signal is received from the external feedback and isolation circuit in the form of a control current into the matched pair of NPN transistors which sink current through a 5 kΩ resistor connected to the 5V reference. The resulting control voltage is compared at the PWM input to a 1V level shifted ramp signal. An opto-coupler detector can be connected directly between the REF pin and the COMP pin. Since the COMP pin is a current mirror input, the potential difference across the opto-coupler detector is nearly constant. The bandwidth limiting phase delay which is normally introduced by the significant capacitance of the opto-coupler is thereby greatly reduced. Higher loop bandwidths can be realized since the bandwidth-limiting pole associated with the opto-coupler is now at a much higher frequency. The PWM comparator polarity is configured such that with no current into the COMP pin, the controller produces maximum duty cycle at the main gate drive output (OUTA).

Feed-Forward Ramp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to VIN, AGND, and the RAMP pins is required to create the PWM ramp signal as shown in Figure 25. The slope of the signal at the RAMP pin will vary in proportion to the input line voltage. This varying slope provides line feed-forward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal by the pulse width modulator comparator to control the duty cycle of the outputs. With a constant error signal, the on-time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the volt-second product of the transformer primary. The power path gain of the conventional voltage-mode pulse with modulator (oscillator generated ramp) varies directly with input voltage. The use of a line generated ramp (input voltage feed-forward) nearly eliminates the gain variation. As a result, the feedback loop is only required to make very small corrections for large changes in input voltage. At the end of each clock period, an internal MOSFET with an $R_{DS(ON)}$ of 10Ω (typical) is enabled to reset the C_{FF} capacitor voltage to ground.

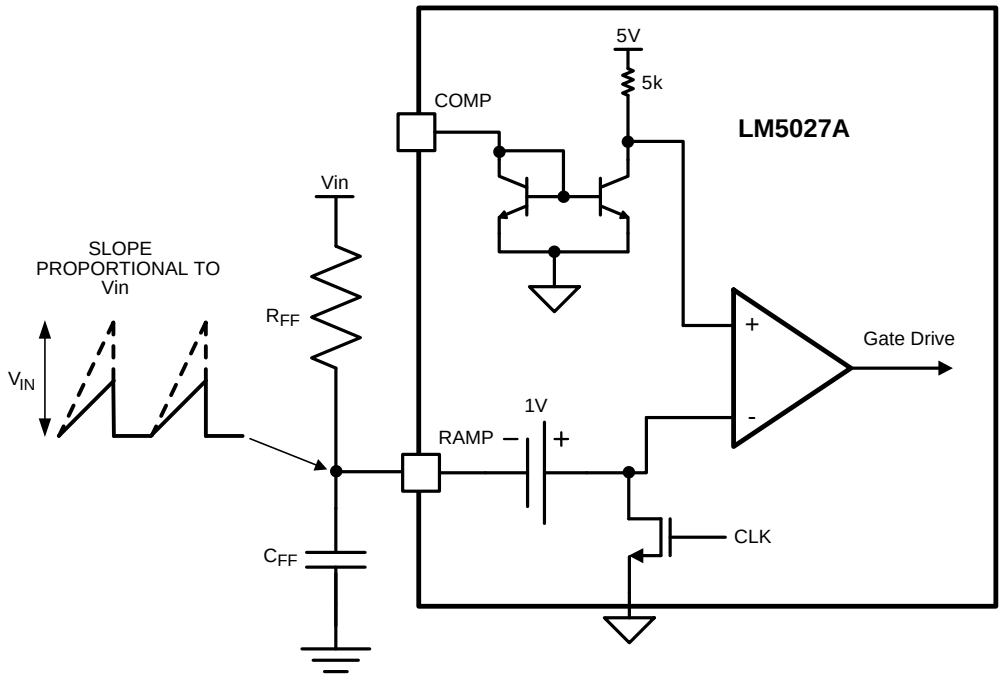


Figure 25. Feed-Forward Voltage Mode Configuration

Volt-Second Clamp

An external resistor (R_{FF}) and a capacitor (C_{FF}) connected between the VIN, RAMP and AGND pins is required to create a saw-tooth modulation ramp signal as shown in Figure 25. The slope of the RAMP will vary in proportion to the input line voltage. Varying the PWM ramp slope inversely with the input voltage provides line feed-forward information necessary to improve line transient response with voltage mode control. With a constant error signal, the on time (t_{ON}) varies inversely with the input voltage (VIN) to stabilize the volt-second product of the transformer primary.

The volt-second clamp compares the ramp signal (RAMP) to a fixed 2.5V reference. By proper selection of R_{FF} and C_{FF}, the maximum on-time of the main switch can be set to the desired duration. An example will illustrate the use of the volt-second clamp comparator to achieve a 70% duty cycle limit at 200 kHz and 18V line input: A 70% duty cycle at 200 kHz requires a 3.5 µs on-time. At 18V input the volt-second product is 63µs (18V x 3.5 µs). To achieve this clamp level:

$$R_{FF} \times C_{FF} = VIN \times t_{ON} / 2.5V \quad (1)$$

$$18V \times 3.5\ \mu s / 2.5V = 25.2\mu \quad (2)$$

Select C_{FF} = 470 pF

R_{FF} = 53.6 kΩ

The recommended capacitor value range for CFF is 100 pF to 1000 pF. The C_{FF} ramp capacitor is discharged at the conclusion of every cycle by an internal discharge switch controlled by either the PWM comparator, the CS comparator or by the volt-second clamp comparator, which ever occurs first.

Oscillator and Sync Capability

The LM5027A oscillator frequency is set by the external resistor connected between the RT pin and the ground (AGND). To set a desired oscillator frequency, the necessary R_T resistor is calculated from:

$$R_T = \frac{1}{Freq \times 8.3567 \times 10^{-11}} \quad (3)$$

For example, if the desired oscillator frequency is 200 kHz, a 59.7K resistor would be the nearest standard one percent value. The R_T resistor should be located as close as possible to the IC and connected directly to the pins (RT and AGND). The tolerance of the external resistor and the frequency tolerance indicated in the Electrical Characteristics must be taken into account when determining the worst case operating frequency. The LM5027A can be synchronized to an external clock by applying a narrow pulse to the RT pin. The external clock must be at least 10% higher than the free-running oscillator frequency set by the R_T resistor. If the external clock frequency is less than the R_T resistor programming frequency, the LM5027A will ignore the synchronizing pulses. The synchronization pulse should be coupled to the RT pin through a 100 pF capacitor with a pulse width of 15 ns to 150 ns. When a synchronizing pulse transitions from low-to-high (rising edge), the voltage at the RT pin must be driven to exceed 3.2V from its nominal 2.85V level. During the clock signal low time, the voltage at the RT pin will be clamped at 2V by an internal regulator. The output impedance of the RT regulator is approximately 100Ω. The RT resistor is always required, whether the oscillator is free running or externally synchronized.

Gate Drive Outputs

The LM5027A contains three unique gate drivers. OUTA, the primary switch driver, is designed to drive the gate of an N-Channel MOSFET and is capable of sourcing and sinking a peak current of 2A. The active clamp drive, OUTB, is designed to drive a P-Channel MOSFET and is capable of sourcing and sinking peak currents of 1A. The third driver, OUTSR, is designed to drive the gate of a synchronous rectification MOSFET through a gate drive transformer. OUTSR gate driver has a source and sink capability of 3A.

Driver Delay Timing

The three independent time delay adjustments allow a great deal of flexibility for the user to optimize the efficiency of the system. The active clamp output (OUTB) is in phase with the main output (OUTA), with the active clamp output overlapping the main output. The overlap time provides dead-time between the operation of the main switch and the P-Channel active clamp switch at both the rising and falling edges. The rising edge control is set by a resistor from the TIME1 pin to the AGND pin. The falling edge control is set with a resistor from the TIME3 pin to the AGND pin.

The rising edge of the PWM comparator output coincides with the rising edge of OUTB and the falling edge of the OUTSR output without delay, as shown in Figure 26. The rising edge control for turning on the OUTSR output after the main output (OUTA) has turned off is set with a resistor from the TIME2 pin to the AGND pin. The PWM output goes high (see Figure 26) at the beginning of the oscillator cycle. The rising edge of OUTA is delayed by time delay T1. The T1 delay directly affects the maximum PWM duty cycle. The maximum duty cycle is calculated using the following equation:

$$\text{Maximum Duty Cycle} = \frac{(72\% \ (1/\text{Freq}) - \text{T1})}{1/\text{Freq}} \tag{4}$$

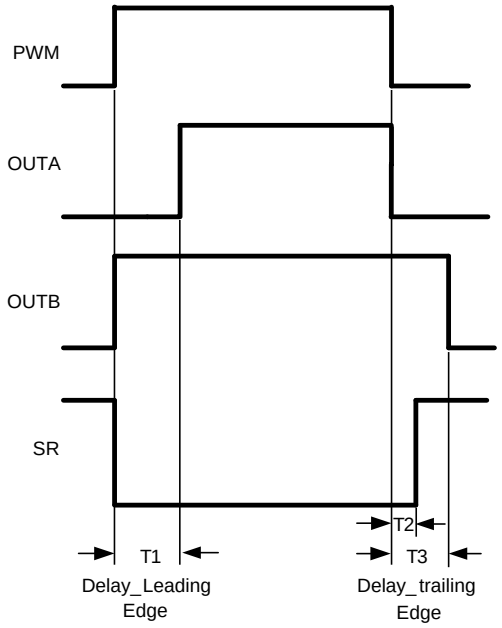


Figure 26. LM5027A Driver Output Timing

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum rated junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state with the output drivers (OUTA, OUTB, and OUTSR), the bias regulators (VCC and REF) disabled. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating. During a restart, after thermal shutdown, the soft-start capacitors (SS and SSSR) are fully discharged and the controller follows a normal start-up sequence after the junction temperature falls below the Thermal Shutdown hysteresis threshold (typically 145°C).

VIN

The voltage applied to the VIN pin, normally the same as the system voltage applied to the power transformer's primary (V_{PWR}), can vary in the range of the 13 to 90V with transient capability of 105V. The current into VIN depends primarily on the output driver capacitive loads, the switching frequency, and any external loads on the VCC pin. If the power dissipation associated with the VIN current exceeds the package capability, an external voltage should be applied to the VCC pin (see Figure 27) to disable the internal start-up regulator. The VCC regulation set point voltage is initially internally regulated to 9.5V. After the first OUTSR pulse, the VCC set point voltage is reduced to 7.5V. If an external voltage is applied to the VCC pin the required range is 8V to 15V . The VIN to VCC series pass regulator includes a parasitic diode between VIN and VCC. This diode should not be forward biased in normal operation. The VCC voltage should never exceed the VIN voltage. It is recommended the circuit of Figure 27 be used to suppress transients which may occur at the input supply, in particular where VIN is operated close to the maximum operating rating of the LM5027A.

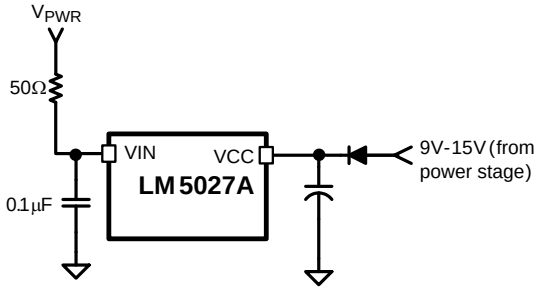


Figure 27. Start-up Regulator Power Reduction

For Applications > 100V

For applications where the system input voltage (V_{PWR}) exceeds 100V, VIN can be powered from an external start-up regulator as shown in Figure 28. Connecting the VIN and VCC pins together allows the LM5027A to be operated with VIN below 13V. To turn-off the internal start-up regulator the VCC voltage must be raised above 9.9V. The voltage at the VCC pin must not exceed 15V. The voltage source at the right side of Figure 28 is typically derived from the power stage, and becomes active when the LM5027A outputs are active.

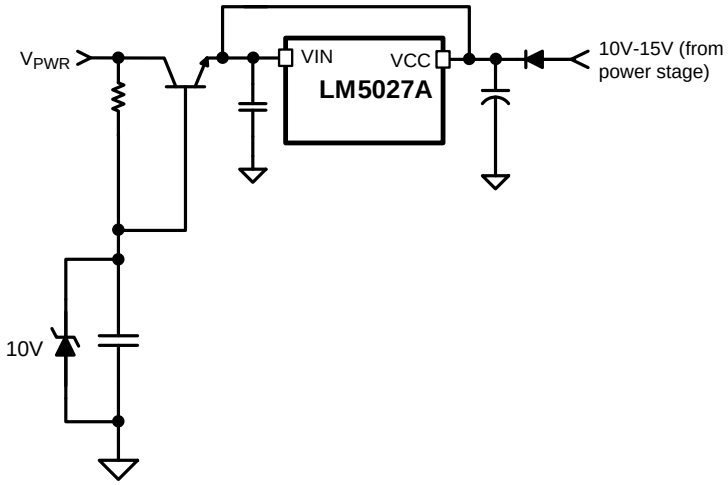


Figure 28. Start-up Regulator for V_{PWR} > 100V

UVLO

The under-voltage lockout threshold (UVLO) is internally set to 2.0V at the UVLO pin. With two external resistors as shown in Figure 29, the LM5027A is enabled when V_{PWR} causes the UVLO pin to exceed threshold voltage of 2V. When V_{PWR} is below the threshold, the internal 20 µA current sink is enabled to reduce the voltage at the UVLO pin. When the UVLO pin voltage exceeds the 2V threshold, the 20 µA current sink is turned off causing the UVLO voltage to increase and providing hysteresis. The values of R1 and R2 can be determined from the following equation:

$$R1 = V_{HYS}/20\ \mu A \quad (5)$$

$$R2 = \frac{2.0 \times R1}{V_{PWR} - 2.0 - 20\ \mu A \times R1} \quad (6)$$

Where V_{HYS} is the desired UVLO hysteresis at V_{PWR}, and V_{PWR} in the second equation is the turn-on voltage. For example, if the LM5027A is to be enabled when V_{PWR} reaches 34V, and the hysteresis is 1.8V, then R1 is 90 kΩ and 5.6 kΩ. For this application R1 was selected to be 90.0 kΩ, R2 was selected to be 6.19 kΩ. The LM5027A can be remotely shutdown by taking the UVLO pin below 0.4V with an external open collector or open drain device, as shown in Figure 29. The outputs and the VCC regulator are disabled in shutdown mode.

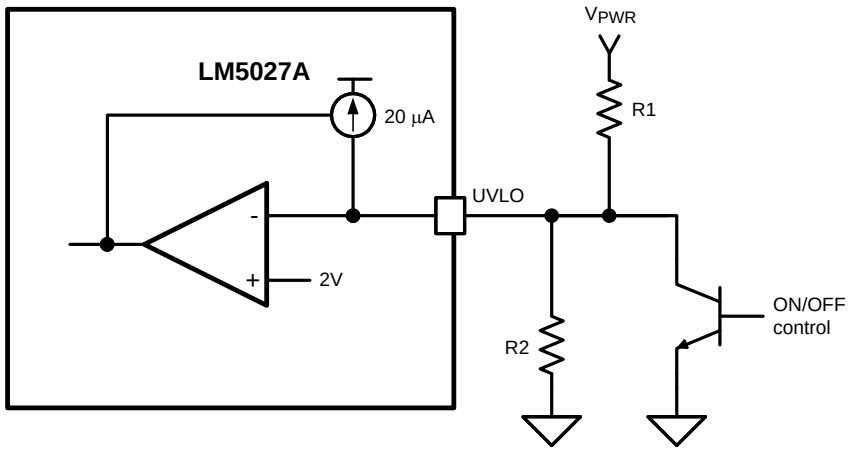


Figure 29. UVLO Circuit with Shutdown Control

Oscillator

The oscillator frequency is generally selected in conjunction with the system magnetic components and any other aspects of the system which may be affected by the frequency. The R_T resistor selection equation is specified in the Oscillator and Sync Capability section. If the required frequency tolerance is critical in particular application, the tolerance of the external resistor and the frequency tolerance specified in the Electrical Characteristics table must be considered when selecting the R_T resistor.

Voltage Feedback

The COMP pin is designed to accept a current input typically from an opto-coupler. A typical configuration is shown in Figure 30, where the emitter of the opto-coupler transistor is connected to the COMP pin and the collector is connected to the REF pin of the LM5027A. When the output voltage is below regulation, no current flows into the COMP pin and the LM5027A operates at maximum duty cycle. At the secondary side, VOUT is compared to a reference by the error amplifier which has an appropriate frequency compensation network. The amplifier output drives the opto-coupler, which in turn drives the LM5027A COMP pin current mirror.

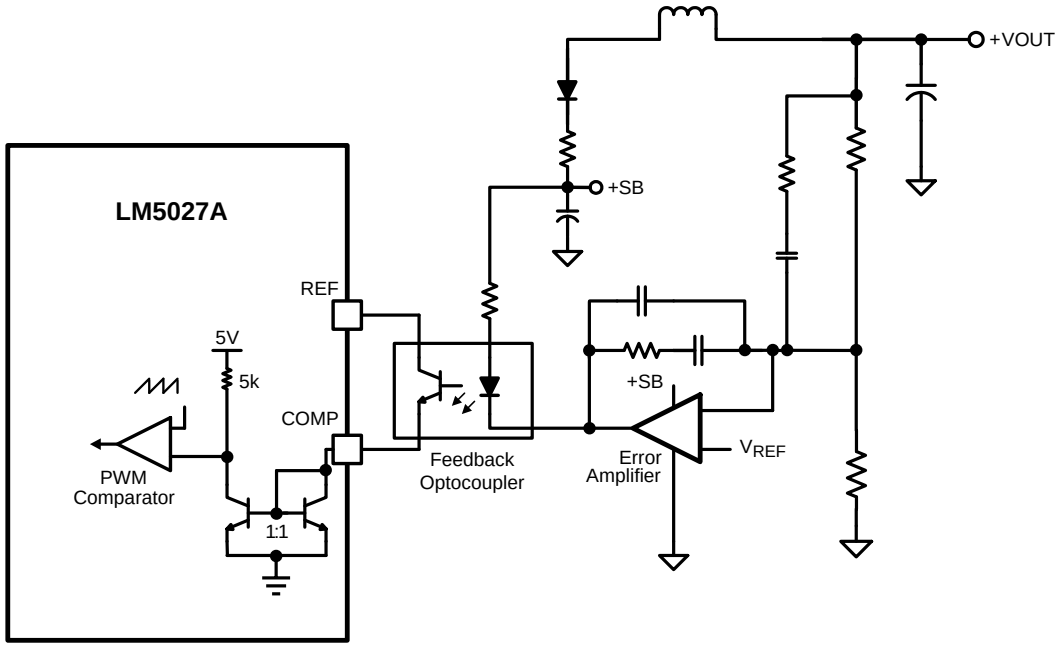


Figure 30. Typical COMP Configuration

Current Sense

The CS pin receives an input signal representative of the transformer primary current, either from a current sense transformer or from a resistor in series with the source of the primary switch, as shown in Figure 31 and Figure 32. In both cases the sensed current creates a ramping voltage across R_{SENSE}, and the RF/CF filter suppresses noise and leading edge transients. The filtering components RSENSE, RF and CF should be physically as close to the LM5027A as possible. The current sense components must be scaled for 0.5V at the CS pin when an over-current condition exists.

If the voltage on the CS pin reaches 0.5V, the present cycle will be immediately terminated. If the over-load event continues and the RES pin reaches 1V, the soft-start capacitor is discharged and the LM5027A will go through an auto re-start (Hiccup Mode). The Hiccup Mode time is set by the capacitor on the RES pin.

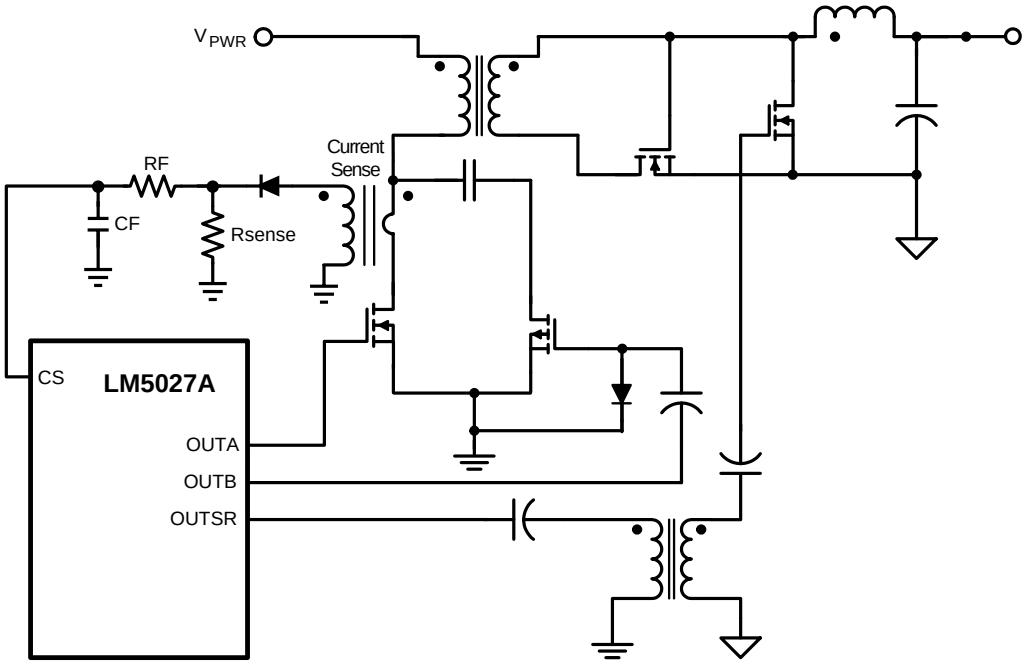


Figure 31. Transformer Current Sense

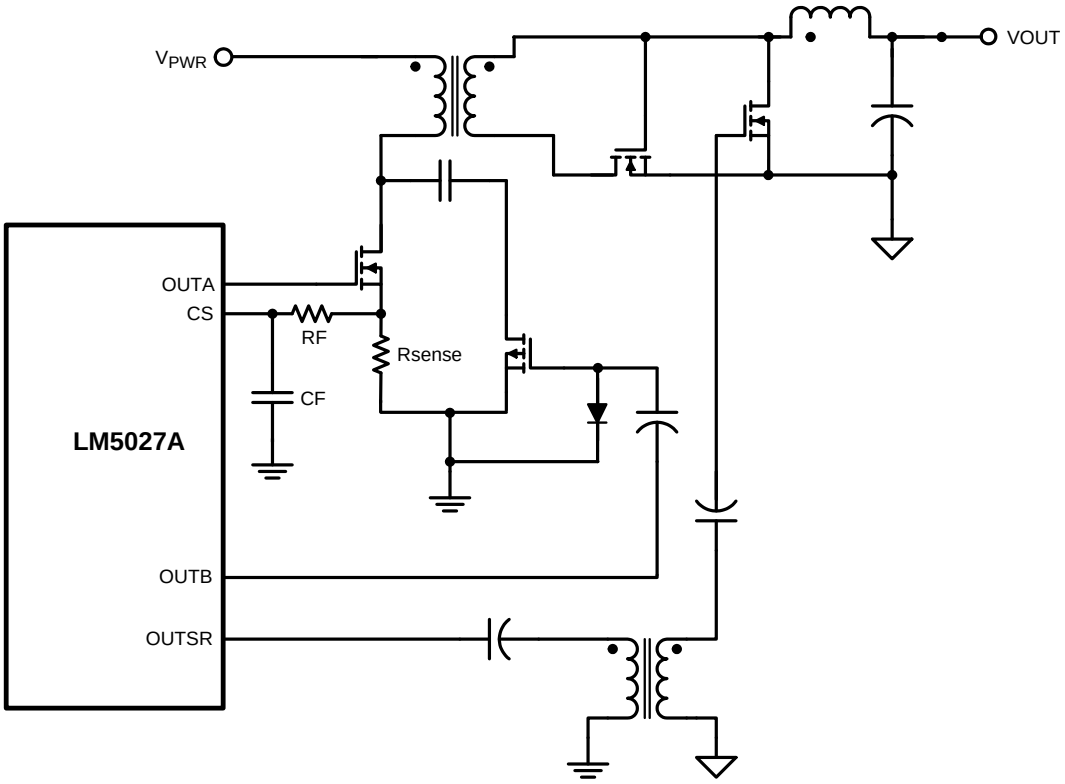


Figure 32. Resistor Current Sense

Soft-Start

The capacitor on the SS pin determines the time required for the output duty cycle to increase from zero to its final value for regulation. The minimum acceptable time is dependent on the output capacitance and the response of the feedback loop that controls the COMP pin. If the soft-start time is too quick, the output could significantly overshoot its intended voltage before the feedback loop has a chance to regulate the PWM controller. After power is applied and VCC has passed its upper UV threshold (9.5V), the voltage at the SS pin ramps up as the external capacitor is charged with an internal 20 µA current source. The voltage at the internal PWM comparator input node follows the voltage at the SS pin. When the voltage on the SS pin has reached 1.0V, PWM pulses appear at the drive output with a very low duty cycle. The voltage at the SS pin eventually increases to approximately 5.0V. The voltage at the input to the PWM comparator and the PWM duty cycle increase to the value required for regulation as determined by the voltage regulation loop.

Hiccup Mode Current Limit Restart

Hiccup mode operation is described in the Restart Time Delay (Hiccup Mode) section. In the case of continuous current limit detection at the CS pin, the time required to reach the 1.0V RES pin threshold is:

$$t_{CS} = \frac{C_{RES} \times 1.0V}{22\ \mu A} \tag{7}$$

For example, if C_{RES} = 0.047 µF the time t_{CS} in Figure 33 is approximately 2.14 ms. After the voltage on the RES pin reaches 1.0V, the 22 µA current source is turned-off and a 5 µA current source is turned-on. The Hiccup Mode time is:

$$t_{hiccup} = \frac{(4.0 - 1.0)C_{RES}}{5\ \mu A} + \left(\frac{\Delta V \times C_{RES}}{5\ \mu A} \times 8\right) \tag{8}$$

where ΔV is 2.0V. With a C_{RES} = 0.047 µF, the Hiccup Mode time is 179 ms. After the Hiccup Mode off time is complete, the RES pin voltage is pulled low and soft-start capacitor is released allowing a soft-start sequence to commence.

The soft-start time $t_{restart}$ is set by the internal 22 µA current source, and is equal to:

$$t_{restart} = \frac{C_{SS} \times 3.0V}{22\ \mu A} \quad (9)$$

If C_{SS} = 0.1 µF, $t_{restart}$ is = 6.41 ms

The hiccup mode provides the periodic cool-down time for the power converter in the event of a sustained overload or short circuit. This off time results in lower average input current and lower power dissipation within the power components.

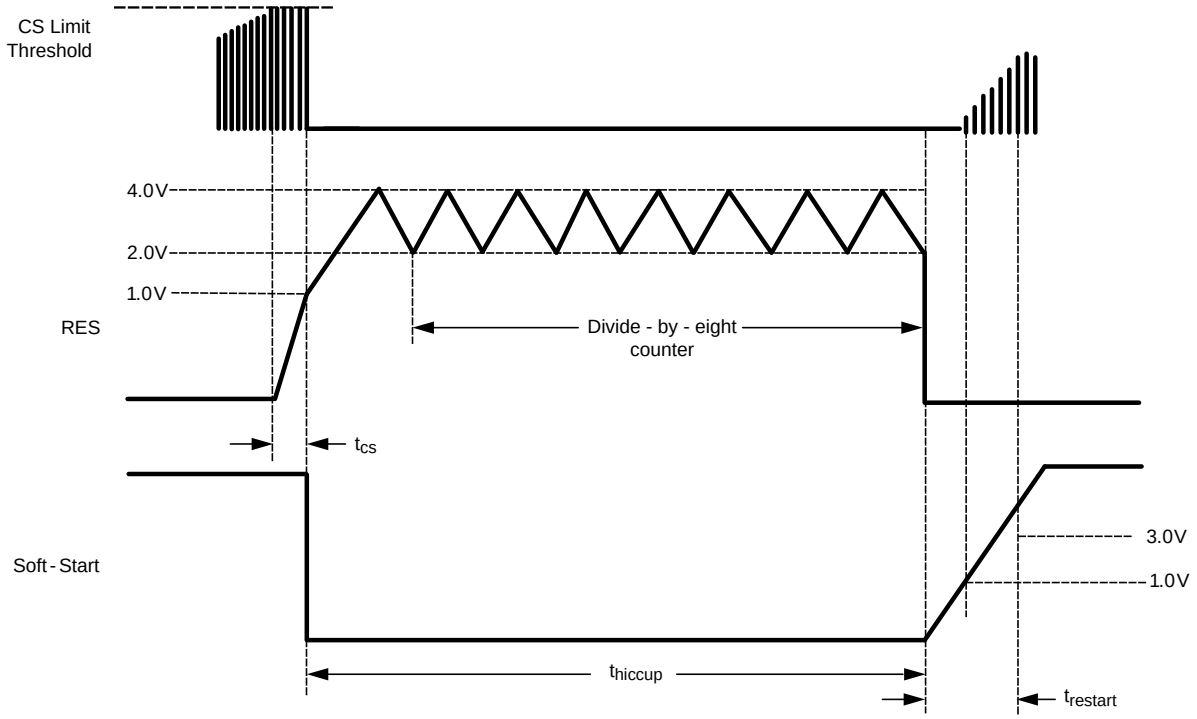


Figure 33. Hiccup Mode Timing

Printed Circuit Board Layout

The LM5027A Current Sense and PWM comparators are very fast and respond to short duration noise pulses. The components at the CS, COMP, SS, UVLO, TIME1, TIME2, and TIME3 pins should be physically close as possible to the IC, thereby minimizing noise pickup on the PC board trace inductance. Layout consideration is critical for the current sense filter. If a current sense transformer is used, both leads of the transformer secondary should be routed to the sense filter components and to the IC pins. The ground side of the transformer should be connected via a dedicated PC board trace to the AGND pin, rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor source, low inductance resistors should be used. In this case, all the noise sensitive, low-current ground trace should be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point). The gate drive outputs of the LM5027A should have short, direct paths to the power MOSFETs in order to minimize inductance in the PC board. The two ground pins (AGND, PGND) must be connected together with a short, direct connection, to avoid jitter due to relative ground bounce.

Application Circuit Example

The following schematic shows an example of the LM5027A controlling a 100W active clamp forward power converter. The input voltage range (V_{PWR}) is 36V to 76V, and the output voltage is 3.3V. The output current capability is 30 Amps. Current sense transformer T3 provides information to the CS pin for current limit protection. The error amplifier and reference U3 and U5 provide voltage feedback via opto-coupler U2. Synchronous rectifiers Q3-Q6 minimize rectification losses in the secondary. An auxiliary winding on the power transformer T1 provides power to the LM5027A VCC pin when the output is in regulation. The input UVLO levels are 34V for increasing V_{PWR}, and approximately 32V for decreasing V_{PWR}. The circuit can be shutdown by forcing the ON/OFF input J2 below 0.4V. An external synchronizing frequency can be applied to the Oscillator input. The converter output current limit is limited at 32A.

Special care was taken in this design such that the converter will turn on with the output pre-biased without sinking current from the output. More information is available in TBD.

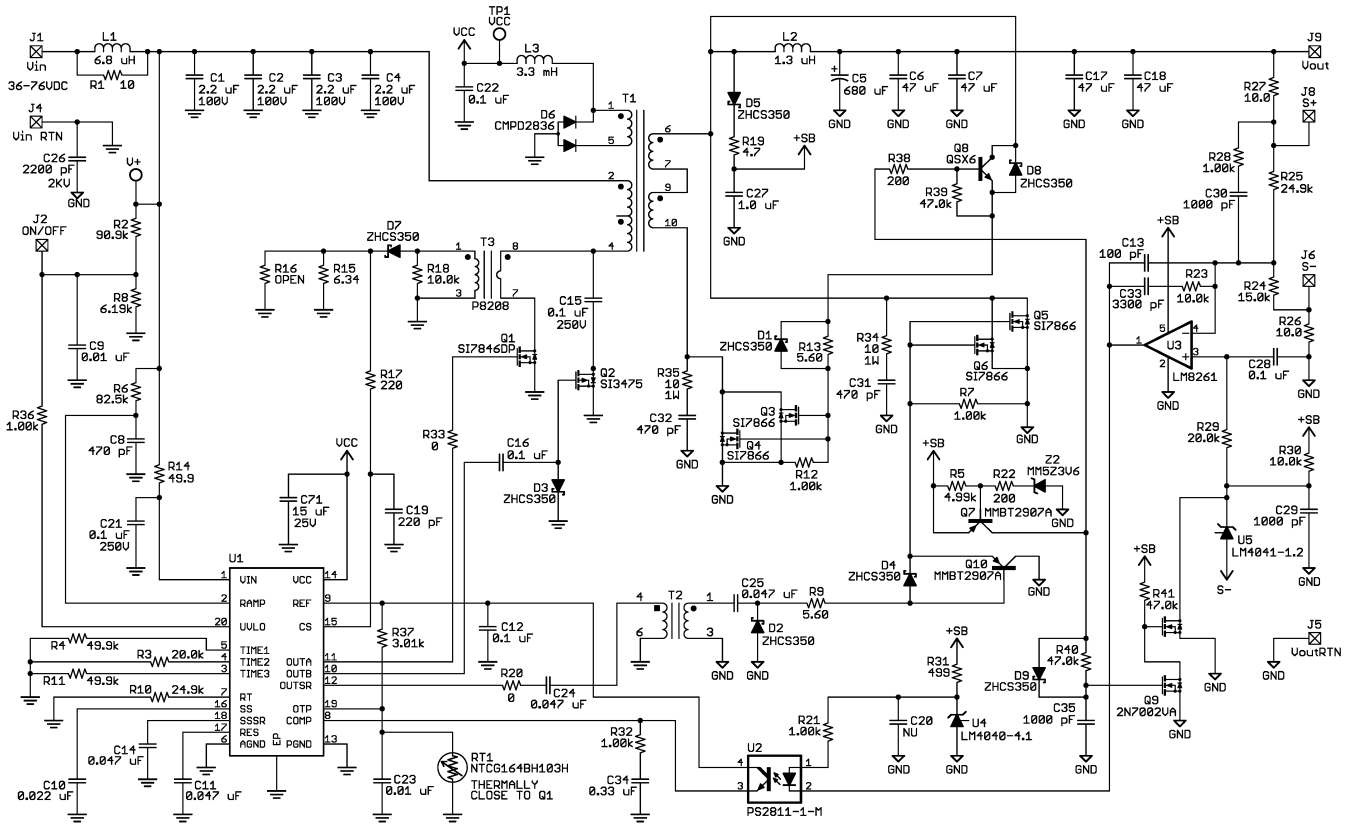


Figure 34. Application Circuit

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5027AMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5027A MH	Samples
LM5027AMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5027A MH	Samples
LM5027ASQ/NOPB	ACTIVE	WQFN	NHZ	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5027A	Samples
LM5027ASQX/NOPB	ACTIVE	WQFN	NHZ	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5027A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

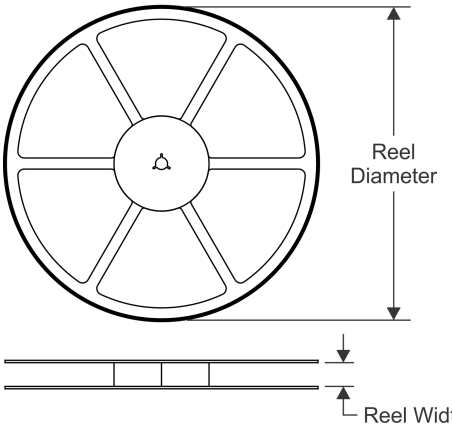
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

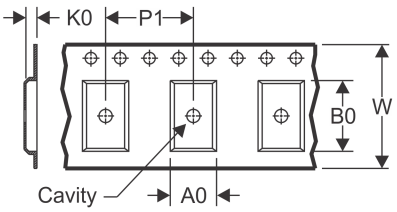
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

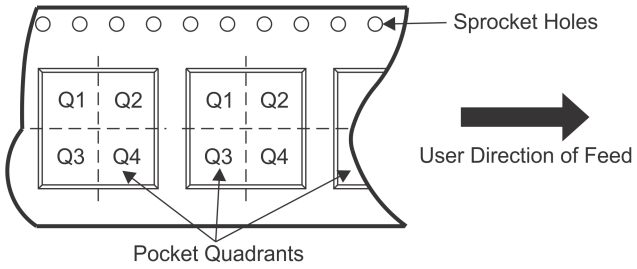


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

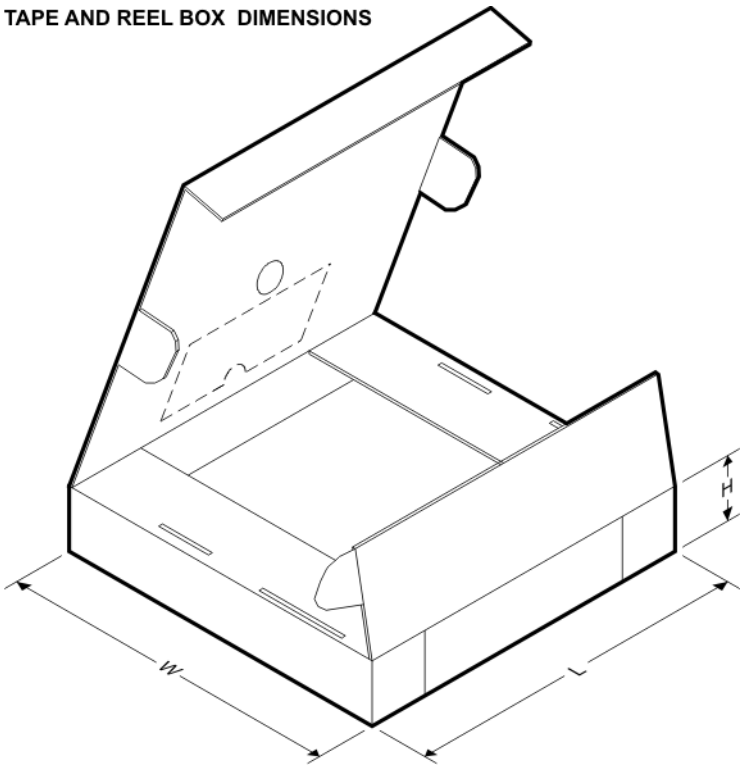
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5027AMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM5027ASQ/NOPB	WQFN	NHZ	24	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM5027ASQX/NOPB	WQFN	NHZ	24	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

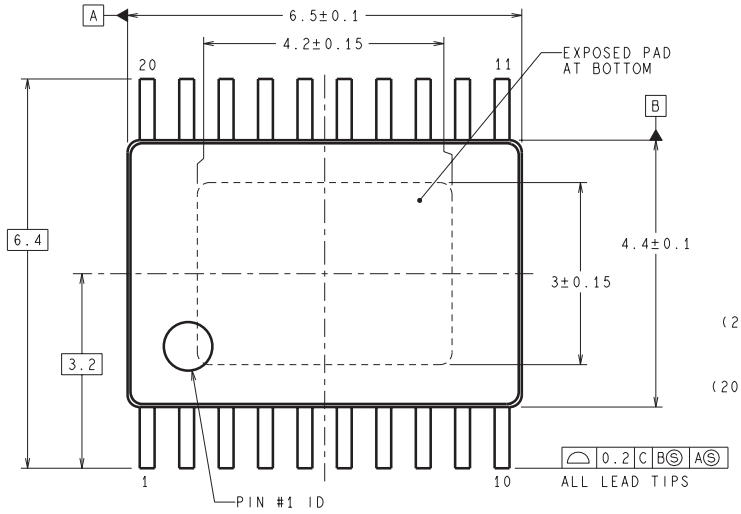
TAPE AND REEL BOX DIMENSIONS

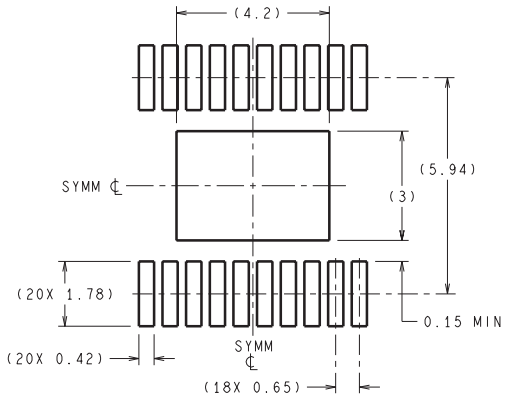


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5027AMHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM5027ASQ/NOPB	WQFN	NHZ	24	1000	203.0	190.0	41.0
LM5027ASQX/NOPB	WQFN	NHZ	24	4500	367.0	367.0	35.0

PWP0020A





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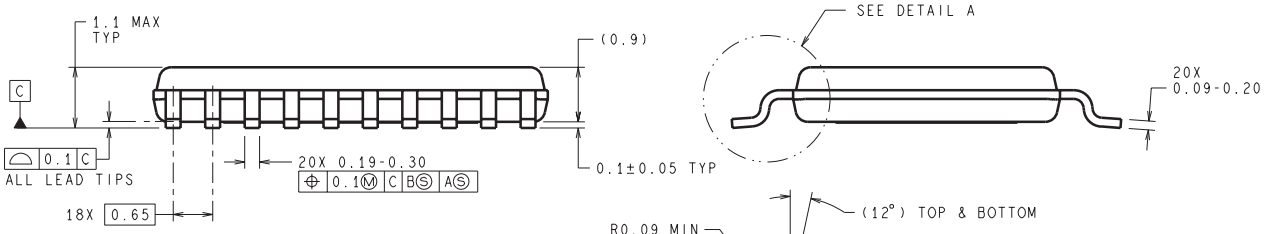

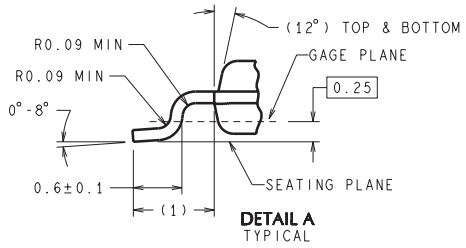

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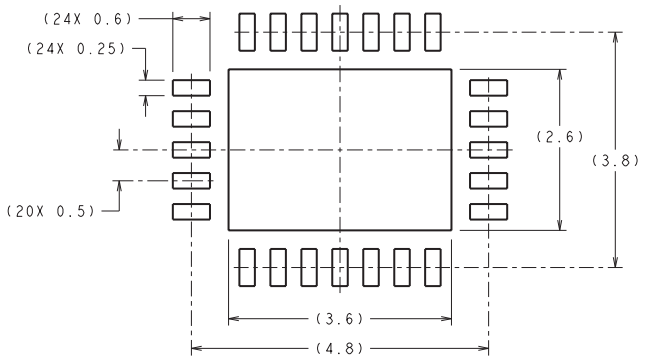

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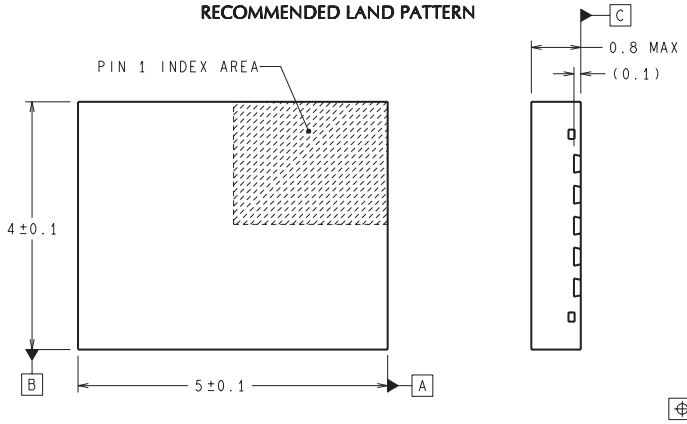

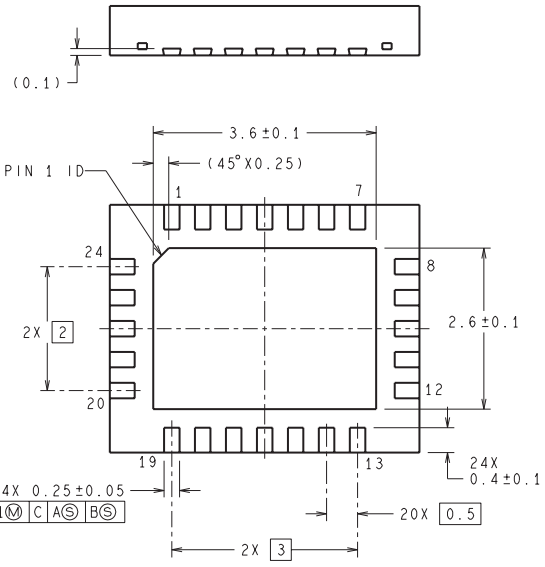

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