

## LM5066 High Voltage System Power Management and Protection IC with PMBus

Check for Samples: [LM5066](#)

### FEATURES

- Input Voltage Range: 10V to 80V
- Programmable 26 mV or 50 mV Current Limit Threshold with Power Limiting (MOSFET Power Dissipation Limiting)
- Real Time Monitoring of  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{IN}$ ,  $P_{IN}$ ,  $V_{AUX}$  with 12-Bit Resolution and 1 kHz Sampling Rate
- Configurable Circuit Breaker Protection for Hard Shorts
- Configurable Under-Voltage and Over-Voltage Protection
- Remote Temperature Sensing with Programmable Warning and Shutdown Thresholds
- Detection and Notification of Damaged MOSFET Condition
- Power Measurement Accuracy:  $\pm 4.5\%$  Over Temperature
- True Input Power Averages Dynamic Power Readings
- Averaging of  $V_{IN}$ ,  $I_{IN}$ ,  $P_{IN}$ , and  $V_{OUT}$  Over Programmable Interval Ranging from 0.001 to 4 Seconds
- Programmable WARN and FAULT Thresholds with SMBA Notification
- Black Box Capture of Telemetry Measurements and Device Status Triggered by WARN or FAULT Condition
- I<sup>2</sup>C/SMBus Interface and PMBus Compliant Command Structure
- Full Featured Application Development Software
- HTSSOP-28 Package

### APPLICATIONS

- Server Backplane Systems
- Base Station Power Distribution Systems
- Solid State Circuit Breaker

### DESCRIPTION

The LM5066 combines a high performance hot swap controller with a PMBus™ compliant SMBus/I<sup>2</sup>C interface to accurately measure, protect and control the electrical operating conditions of systems connected to a backplane power bus. The LM5066 continuously supplies real-time power, voltage, current, temperature and fault data to the system management host via the SMBus interface.

The LM5066 control block includes a unique hot swap architecture that provides current and power limiting to protect sensitive circuitry during insertion of boards into a live system backplane, or any other "hot" power source. A fast acting circuit breaker prevents damage in the event of a short circuit on the output. The input under-voltage and over-voltage levels and hysteresis are configurable, as well as the insertion delay time and fault detection time. A temperature monitoring block on the LM5066 interfaces with a low-cost external diode for monitoring the temperature of the external MOSFET or other thermally sensitive components. The PGD output provides a fast indicator when the input and/or output voltages are outside their programmed ranges. LM5066 current measurement accuracy is  $\pm 4.5\%$  over the operating temperature range.

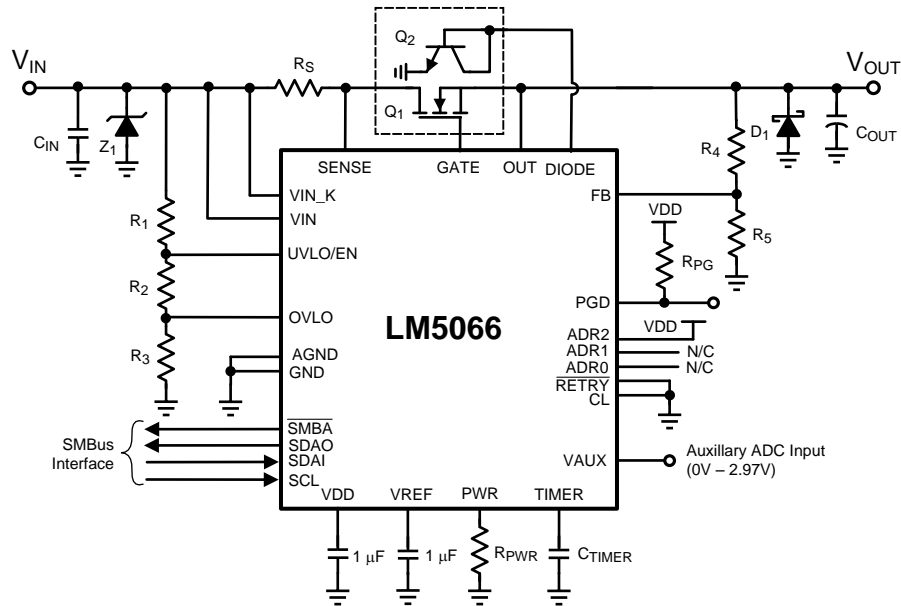
The LM5066 monitoring block computes both the real-time and average values of subsystem operating parameters ( $V_{IN}$ ,  $I_{IN}$ ,  $P_{IN}$ ,  $V_{OUT}$ ) as well as the peak power. Accurate power averaging is accomplished by averaging the product of the input voltage and current. A black box (Telemetry/Fault Snapshot) function captures and stores telemetry data and device status in the event of a warning or a fault.



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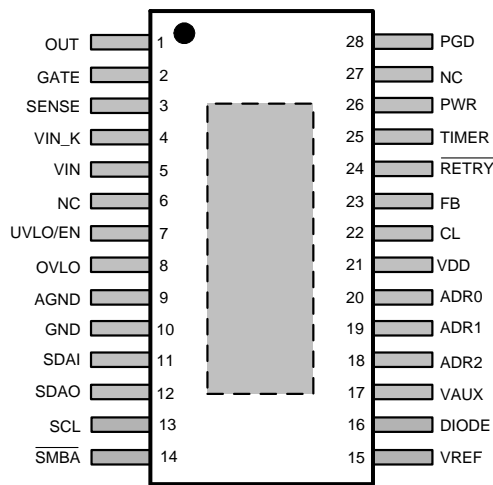
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### Typical Application Schematic



### Connection Diagram

Solder exposed pad to ground.



**Top View  
28-Lead HTSSOP with  
Exposed Pad**

### PIN DESCRIPTIONS

Pin No.	Name	Description	Applications Information
Pad	Exposed Pad	Exposed pad of HTSSOP package	Solder to the ground plane to reduce thermal resistance
1	OUT	Output feedback	Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET $V_{DS}$ voltage for power limiting, and to monitor the output voltage.
2	GATE	Gate drive output	Connect to the external MOSFET's gate.

**PIN DESCRIPTIONS (continued)**

Pin No.	Name	Description	Applications Information
3	SENSE	Current sense input	The voltage across the current sense resistor ( $R_S$ ) is measured from VIN_K to this pin. If the voltage across $R_S$ reaches over-current threshold the load current is limited and the fault timer activates.
4	VIN_K	Positive supply kelvin pin	The input voltage is measured on this pin.
5	VIN	Positive supply input	This pin is the input supply connection for the device.
6	N/C	No connection	
7	UVLO/EN	Under-voltage lockout	An external resistor divider from the system input voltage sets the under-voltage turn-on threshold. An internal 20 $\mu$ A current source provides hysteresis. The enable threshold at the pin is nominally 2.48V. This pin can also be used for remote shutdown control.
8	OVLO	Over-voltage lockout	An external resistor divider from the system input voltage sets the over-voltage turn-off threshold. An internal 21 $\mu$ A current source provides hysteresis. The disable threshold at the pin is 2.46V.
9	AGND	Circuit ground	Analog device ground. Connect to GND at the pin.
10	GND	Circuit ground	
11	SDAI	SMBus data input pin	Data input pin for SMBus. Connect to SDAO if the application does not require unidirectional isolation devices.
12	SDAO	SMBus data output pin	Data output pin for SMBus. Connect to SDAI if the application does not require unidirectional isolation devices.
13	SCL	SMBus clock	Clock pin for SMBus.
14	$\overline{\text{SMBA}}$	SMBus alert line	Alert pin for SMBus, active low.
15	VREF	Internal Reference	Internally generated precision reference used for analog to digital conversion. Connect a 1 $\mu$ F capacitor on this pin to ground for bypassing.
16	DIODE	External diode	Connect this to a diode-configured MMBT3904 NPN transistor for temperature monitoring.
17	VAUX	Auxiliary voltage input	Auxiliary pin allows voltage telemetry from an external source. Full scale input of 2.97V.
18	ADR2	SMBUS address line 2	Tri-state address line. Should be connected to GND, VDD, or left floating.
19	ADR1	SMBUS address line 1	Tri-state address line. Should be connected to GND, VDD, or left floating.
20	ADR0	SMBUS address line 0	Tri-state address line. Should be connected to GND, VDD, or left floating.
21	VDD	Internal sub-regulator output	Internally sub-regulated 4.85V bias supply. Connect a 1 $\mu$ F capacitor on this pin to ground for bypassing.
22	CL	Current limit range	Connect this pin to GND or leave floating to set the nominal over-current threshold at 50mV. Connecting CL to VDD will set the over-current threshold to be 26mV.
23	FB	Power Good feedback	An external resistor divider from the output sets the output voltage at which the PGD pin switches. The threshold at the pin is nominally 2.46V. An internal 20 $\mu$ A current source provides hysteresis.
24	$\overline{\text{RETRY}}$	Fault retry input	This pin configures the power up fault retry behavior. When this pin is connected to GND or left floating, the device will continually try to engage power during a fault. If the pin is connected to VDD, the device will latch off during a fault.
25	TIMER	Timing capacitor	An external capacitor connected to this pin sets the insertion time delay, fault timeout period and restart timing.
26	PWR	Power limit set	An external resistor connected to this pin, in conjunction with the current sense resistor ( $R_S$ ), sets the maximum power dissipation allowed in the external series pass MOSFET.
27	N/C	No Connection	
28	PGD	Power Good indicator	An open drain output. This output is high when the voltage at the FB pin is above $V_{FBTH}$ (nominally 2.46V) and the input supply is within its under-voltage and over-voltage thresholds. Connect to the output rail (external MOSFET source) or any other voltage to be monitored.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)</sup>

VIN, VIN_K, GATE, UVLO/EN, OUT, SENSE, PGD to GND <sup>(2)</sup>	-0.3V to 100V
OVLO, FB, TIMER, PWR to GND	-0.3V to 7.0V
SCL, SDAI, SDAO, CL, ADR0, ADR1, ADR2, VDD, VAUX, DIODE, RETRY to GND	-0.3V to 6.0V
SENSE to VIN_K, VIN to VIN_K, AGND to GND	-0.3V to +0.3V
ESD Rating <sup>(3)</sup> Human Body Model	2kV
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For specifications and conditions see the [Electrical Characteristics](#).
- (2) The GATE pin voltage is typically 13.6V above VIN when the LM5066 is enabled. Therefore, the Absolute Maximum Rating for VIN applies only when the LM5066 is disabled, or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is also 100V.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2 kV rating for all pins except GATE which is rated for 1 kV.

### Operating Ratings

VIN, SENSE, OUT voltage	10V to 80V
Junction Temperature	-40°C to +125°C

## Electrical Characteristics

Limits in standard type are for  $T_J = 25^\circ\text{C}$  only; limits in boldface type apply over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  unless otherwise stated. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise stated the following conditions apply:  $V_{IN} = 48\text{V}$ . See <sup>(1)</sup> and <sup>(2)</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Input (VIN Pin)</b>						
$I_{IN-EN}$	Input Current, enabled	$V_{UVLO} = 3\text{V}$ and $V_{OVLO} = 2\text{V}$		7.2	<b>9.5</b>	mA
$POR_{IT}$	Power On Reset threshold at VIN to trigger insertion timer	VIN Increasing		7.8	<b>9.0</b>	V
$POR_{EN}$	Power On Reset threshold at VIN to enable all functions	VIN Increasing		8.6	<b>9.9</b>	V
$POR_{HYS}$	$POR_{EN}$ Hysteresis	VIN Decreasing		120		mV
<b>V<sub>DD</sub> Regulator (VDD pin)</b>						
$V_{DD}$		$I_{VDD} = 0\text{ mA}$	<b>4.60</b>	4.90	<b>5.15</b>	V
		$I_{VDD} = 10\text{ mA}$		4.85		V
$V_{DDLIM}$	VDD Current Limit		<b>-25</b>	-30	<b>-42</b>	mA
$V_{DDPOR}$	VDD Voltage Reset threshold	$V_{DD}$ Rising		4.1		V
<b>UVLO/EN, OVLO Pins</b>						
$UVLO_{TH}$	UVLO threshold	$V_{UVLO}$ Falling	<b>2.41</b>	2.48	<b>2.55</b>	V
$UVLO_{HYS}$	UVLO hysteresis current	$UVLO = 1\text{V}$	<b>13</b>	20	<b>26</b>	$\mu\text{A}$
$UVLO_{DEL}$	UVLO delay	Delay to GATE high		9		$\mu\text{s}$
		Delay to GATE low		13		$\mu\text{s}$
$UVLO_{BIAS}$	UVLO bias current	$UVLO = 3\text{V}$			<b>1</b>	$\mu\text{A}$
$OVLO_{TH}$	OVLO threshold	$V_{OVLO}$ Rising	<b>2.39</b>	2.46	<b>2.53</b>	V
$OVLO_{HYS}$	OVLO hysteresis current	$OVLO = 1\text{V}$	<b>-26</b>	-21	<b>-13</b>	$\mu\text{A}$
$OVLO_{DEL}$	OVLO delay	Delay to GATE high		13		$\mu\text{s}$
		Delay to GATE low		10		$\mu\text{s}$
$OVLO_{BIAS}$	OVLO bias current	$OVLO = 1\text{V}$			<b>1</b>	$\mu\text{A}$
<b>Power Good (PGD pin)</b>						
$PGD_{VOL}$	Output low voltage	$I_{SINK} = 2\text{ mA}$		60	<b>110</b>	mV
$PGD_{IOH}$	Off leakage current	$V_{PGD} = 80\text{V}$			<b>1</b>	$\mu\text{A}$
<b>FB Pin</b>						
$FB_{TH}$	FB Threshold	$V_{UVLO} = 3\text{V}$ and $V_{OVLO} = 2\text{V}$	<b>2.41</b>	2.46	<b>2.52</b>	V
$FB_{HYS}$	FB Hysteresis Current		<b>-25</b>	-20	<b>-15</b>	$\mu\text{A}$
$FB_{DEL}$	FB Delay	Delay to PGD high		7.6		$\mu\text{s}$
		Delay to PGD low		9.2		$\mu\text{s}$
$FB_{LEAK}$	Off Leakage Current	$V_{FB} = 2.3\text{V}$			<b>1</b>	$\mu\text{A}$
<b>Power Limit (PWR Pin)</b>						
$PWR_{LIM}$	Power limit sense voltage (VIN-SENSE)	SENSE-OUT = 48V, $R_{PWR} = 121\text{ k}\Omega$	<b>16.5</b>	19.5	<b>22.5</b>	mV
		SENSE-OUT = 24V, $R_{PWR} = 75\text{ k}\Omega$		23		mV
$I_{PWR}$	PWR pin current	$V_{PWR} = 2.5\text{V}$		-20		$\mu\text{A}$
$R_{SAT(PWR)}$	PWR pin impedance when disabled	$UVLO = 2\text{V}$		135		$\Omega$
<b>Gate Control (GATE Pin)</b>						
$I_{GATE}$	Source current	Normal Operation	<b>-26</b>	-20	<b>-10</b>	$\mu\text{A}$
	Fault Sink current	$UVLO = 2\text{V}$	<b>3.4</b>	4.2	<b>5.3</b>	mA
	POR Circuit Breaker sink current	$V_{IN} - \text{SENSE} = 150\text{ mV}$ or $V_{IN} < POR_{IT}$ , $V_{GATE} = 5\text{V}$	<b>50</b>	115	<b>180</b>	mA

(1) Current out of a pin is indicated as a negative value.

(2) All electrical characteristics having room temperature limits are tested during production at  $T_A = 25^\circ\text{C}$ . All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

## Electrical Characteristics (continued)

Limits in standard type are for  $T_J = 25^\circ\text{C}$  only; limits in boldface type apply over the junction temperature ( $T_J$ ) range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  unless otherwise stated. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at  $T_J = 25^\circ\text{C}$ , and are provided for reference purposes only. Unless otherwise stated the following conditions apply:  $V_{IN} = 48\text{V}$ . See <sup>(1)</sup> and <sup>(2)</sup>.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{\text{GATEZ}}$	Reverse-bias voltage of GATE to OUT zener diode	GATE - OUT	<b>15</b>	16.5	<b>18</b>	V
$V_{\text{GATECP}}$	Peak charge pump voltage in normal operation ( $V_{IN} = V_{OUT}$ )	GATE - OUT		13.6		V
<b>OUT Pin</b>						
$I_{\text{OUT-EN}}$	OUT bias current, enabled	OUT = $V_{IN}$ , Normal operation		78		$\mu\text{A}$
$I_{\text{OUT-DIS}}$	OUT bias current, disabled <sup>(3)</sup>	Disabled, OUT = 0V, SENSE = $V_{IN}$		-50		$\mu\text{A}$
<b>Current Limit</b>						
$V_{\text{CL}}$	Current limit threshold voltage ( $V_{IN} - V_{\text{SENSE}}$ )	CL = VDD	<b>23</b>	26	<b>29</b>	mV
		CL = GND	<b>47</b>	50	<b>53</b>	
$t_{\text{CL}}$	Response time	$V_{IN}$ -SENSE stepped from 0 mV to 80 mV		45		$\mu\text{s}$
$I_{\text{SENSE}}$	SENSE input current	Enabled, SENSE = OUT		25		$\mu\text{A}$
		Disabled, OUT = 0V		66		
		Enabled, OUT = 0V		220		
<b>Circuit Breaker</b>						
$RT_{\text{CB}}$	Circuit Breaker to Current Limit Ratio: ( $V_{IN} - V_{\text{SENSE}}\text{CB}/V_{\text{CL}}$ )	CB/CL ratio bit = 0, ILim = 50 mV	<b>1.64</b>	1.94	<b>2.23</b>	V/V
		CB/CL ratio bit = 1, ILim = 50 mV	<b>3.28</b>	3.87	<b>4.45</b>	
		CB/CL ratio bit = 0, ILim = 26 mV		1.88		
		CB/CL ratio bit = 1, ILim = 26 mV		3.75		
$V_{\text{CB}}$	Circuit Breaker Threshold Voltage: ( $V_{IN} - V_{\text{SENSE}}$ )	CB/CL ratio bit = 0, ILim = 50 mV	<b>80</b>	96	<b>110</b>	mV
		CB/CL ratio bit = 1, ILim = 50 mV	<b>164</b>	193	<b>222</b>	
		CB/CL ratio bit = 0, ILim = 26 mV	<b>39</b>	48	<b>57</b>	
		CB/CL ratio bit = 1, ILim = 26 mV	<b>79</b>	96	<b>113</b>	
$t_{\text{CB}}$	Response time	$V_{IN} - \text{SENSE}$ stepped from 0 mV to 150 mV, time to GATE low, no load		0.42	<b>0.83</b>	$\mu\text{s}$
<b>Timer (TIMER pin)</b>						
$V_{\text{TMRH}}$	Upper threshold		<b>3.74</b>	3.9	<b>4.07</b>	V
$V_{\text{TMRL}}$	Lower threshold	Restart cycles	<b>0.98</b>	1.1	<b>1.24</b>	V
		End of 8 <sup>th</sup> cycle		0.3		V
		Re-enable Threshold		0.3		V
$I_{\text{TIMER}}$	Insertion time current	TIMER pin = 2V	<b>-5.9</b>	-4.8	<b>-3.3</b>	$\mu\text{A}$
		Sink current, end of insertion time	<b>1.0</b>	1.5	<b>2.0</b>	mA
		Fault detection current	<b>-95</b>	-75	<b>-50</b>	$\mu\text{A}$
		Fault sink current	<b>1.7</b>	2.5	<b>3.2</b>	$\mu\text{A}$
$DC_{\text{FAULT}}$	Fault Restart Duty Cycle			0.5		%
$t_{\text{FAULT\_DELAY}}$	Fault to GATE low delay	TIMER pin reaches the upper threshold		12		$\mu\text{s}$
<b>Internal Reference</b>						
$V_{\text{REF}}$	Reference Voltage		<b>2.93</b>	2.97	<b>3.02</b>	V
<b>ADC and MUX</b>						
	Resolution			12		Bits
INL	Integral Non-Linearity	ADC only		$\pm 4$		LSB
$t_{\text{ACQUIRE}}$	Acquisition + Conversion Time	Any Channel		100		$\mu\text{s}$
$t_{\text{RR}}$	Acquisition Round Robin Time	Cycle all channels		1		ms

(3) OUT bias current (disabled) due to leakage current through an internal 1 M $\Omega$  resistance from SENSE to VOUT.

## Electrical Characteristics (continued)

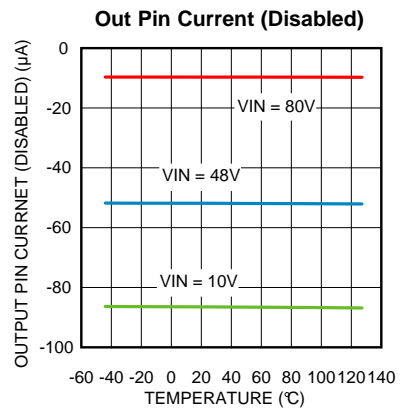
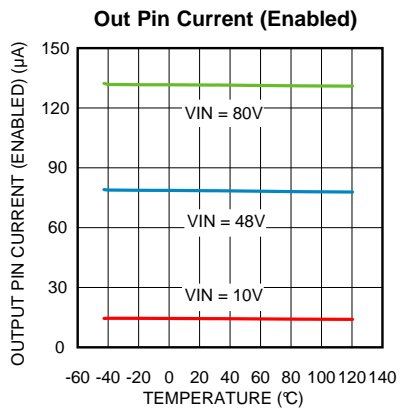
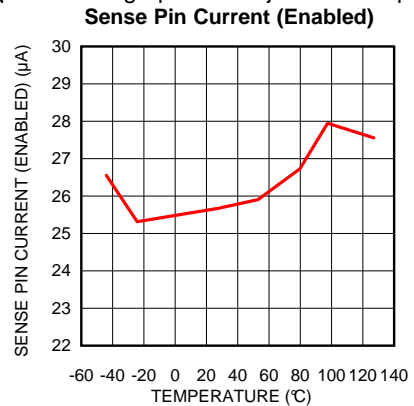
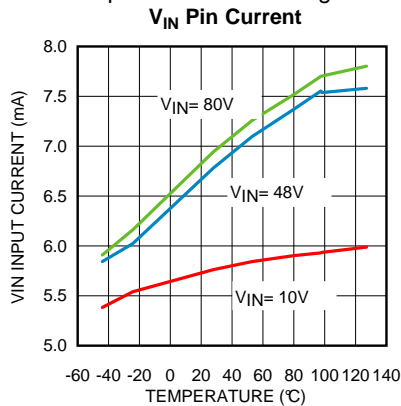
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Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Telemetry Accuracy</b>						
$I_{INFSR}$	Current input full scale range	CL = GND		75.8		mV
		CL = VDD		38.2		mV
$I_{INLSB}$	Current input LSB	CL = GND		18.5		$\mu\text{V}$
		CL = VDD		9.3		$\mu\text{V}$
$V_{AUXFSR}$	VAUX input full scale range			2.97		V
$V_{AUXLSB}$	VAUX input LSB			725		$\mu\text{V}$
$V_{INFSR}$	Input voltage full scale range			89.3		V
$V_{INLSB}$	Input voltage LSB			21.8		mV
$I_{INACC}$	Input Current Accuracy	$V_{IN} - \text{SENSE} = 50\text{mV}$ , CL = GND	<b>-3.0</b>		<b>+3.0</b>	%
$V_{ACC}$	VAUX, $V_{IN}$ , $V_{OUT}$	$V_{IN}$ , $V_{OUT} = 48\text{V}$ $V_{AUX} = 2.8\text{V}$	<b>-2.7</b>		<b>+2.7</b>	%
$P_{INACC}$	Input Power Accuracy	$V_{IN} = 48\text{V}$ , $V_{IN} - \text{SENSE} = 50\text{mV}$ , CL = VDD	<b>-4.5</b>		<b>+4.5</b>	%
<b>Remote Diode Temperature Sensor</b>						
$T_{ACC}$	Temperature Accuracy Using Local Diode	$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$		2	<b>10</b>	$^\circ\text{C}$
	Remote Diode Resolution			9		bits
$I_{DIODE}$	External Diode Current Source	High Level		250	<b>325</b>	$\mu\text{A}$
		Low Level		9.4		$\mu\text{A}$
	Diode Current Ratio			25.9		
<b>PMBus Pin Thresholds (SMBA, SDA, SCL)</b>						
$V_{IL}$	Data, Clock Input Low Voltage				<b>0.9</b>	V
$V_{IH}$	Data, Clock Input High Voltage		<b>2.1</b>		<b>5.5</b>	V
$V_{OL}$	Data Output Low Voltage	$I_{SINK} = 3\text{mA}$	<b>0</b>		<b>0.4</b>	V
$I_{LEAK}$	Input Leakage Current	SDA, SMBA, SCL = 5V			<b>1</b>	$\mu\text{A}$
<b>Configuration Pin Thresholds (CL, RETRY)</b>						
$V_{IH}$	Threshold Voltage		<b>3</b>			V
$I_{LEAK}$	Input Leakage Current	CL, RETRY = 5V		5		$\mu\text{A}$
<b>Thermal <sup>(4)</sup></b>						
$\theta_{JA}$	Junction to Ambient			29		$^\circ\text{C/W}$
$\theta_{JC}$	Junction to Case			4		$^\circ\text{C/W}$

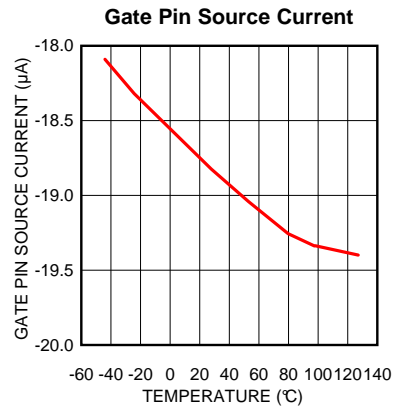
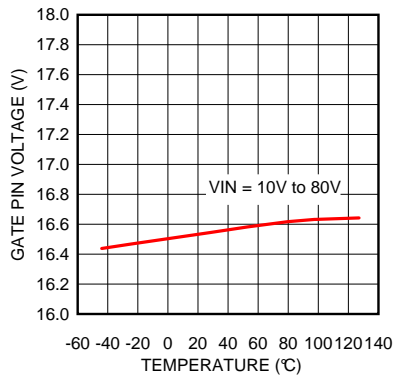
(4) Junction to ambient thermal resistance is highly application and board layout dependent. Specified thermal resistance values for the package specified is based on a 4-layer, 4"x3", 2/1/1/2 oz. Cu board with 15 vias with 8 mil. diameter under the DAP.

### Typical Performance Characteristics

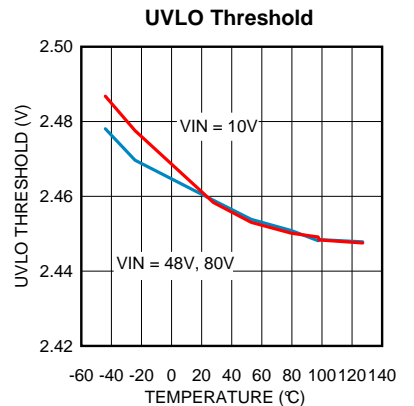
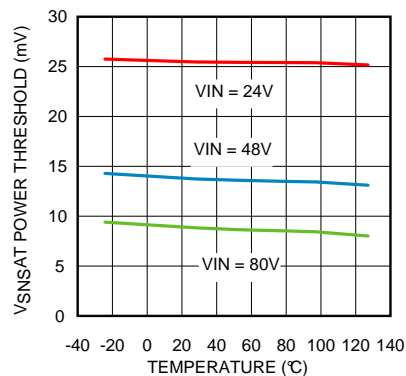
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#### Gate Zener Reverse Bias Voltage (V<sub>GATE</sub> - V<sub>OUT</sub>)



#### V<sub>SNS</sub> at Power Limit Threshold R<sub>PWR</sub> = 75 kΩ

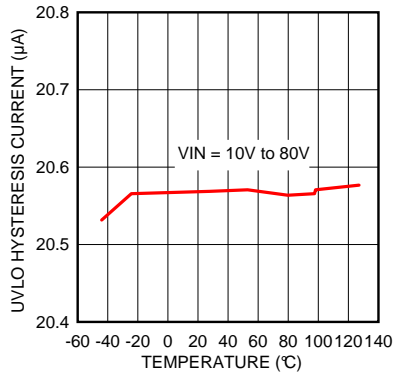




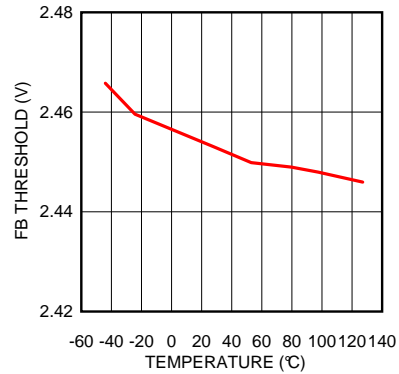
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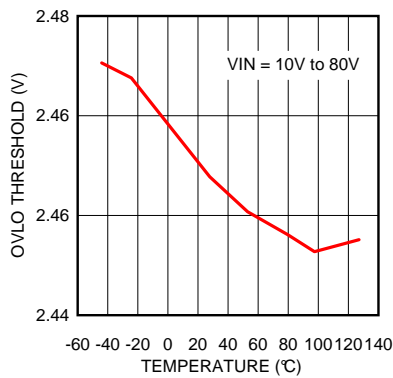
**UVLO Hysteresis Current**



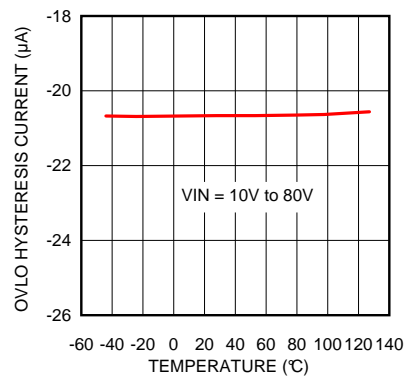
**FB Threshold**



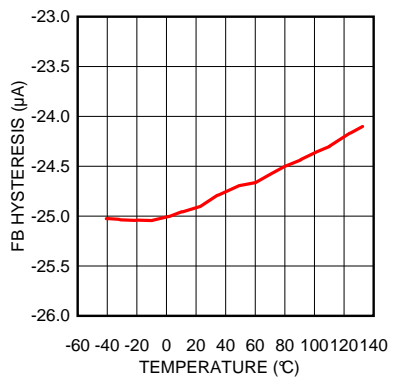
**OVLO Threshold**



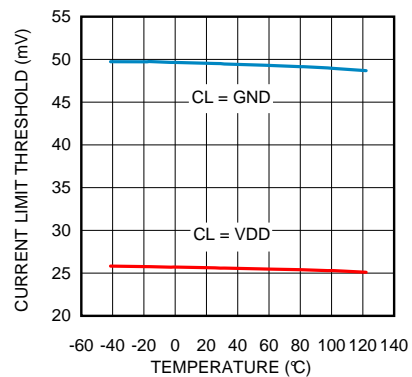
**OVLO Hysteresis**



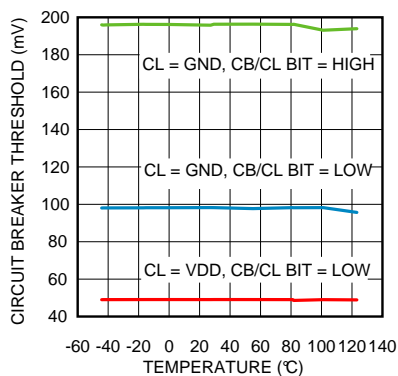
**FB Pin Hysteresis**



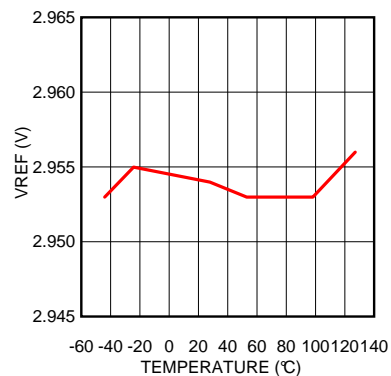
**Current Limit Threshold**



**Circuit Breaker Threshold**



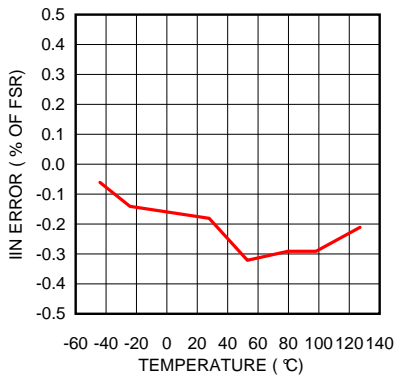
**Reference Voltage**



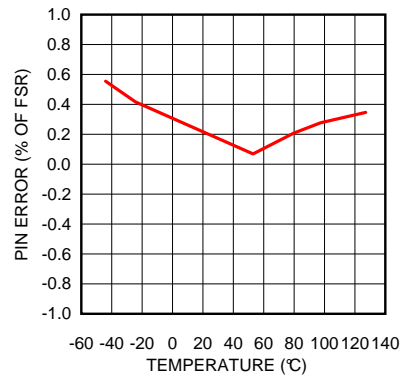
### Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 48\text{V}$ . All graphs show junction temperature.

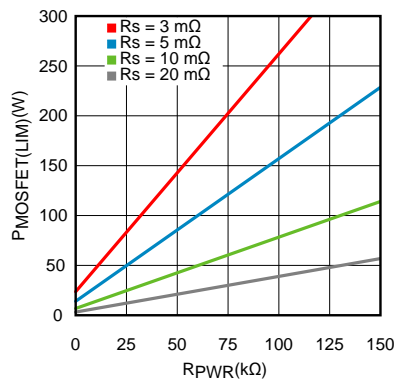
**IIN Measurement Accuracy**  
( $V_{IN} - \text{SENSE} = 50\text{ mV}$ )



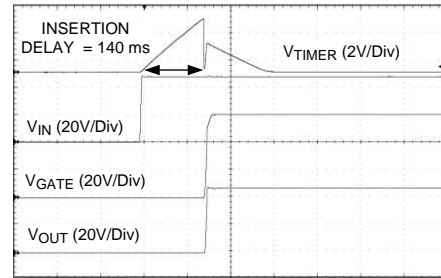
**PIN Measurement Accuracy**  
( $V_{IN} - \text{SENSE} = 50\text{ mV}$ )



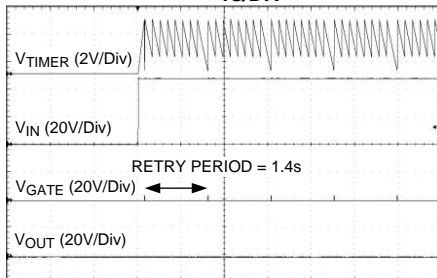
**MOSFET Power Dissipation Limit vs.  $R_{PWR}$  and  $R_s$**   
( $V_{IN} = 48\text{V}$ )



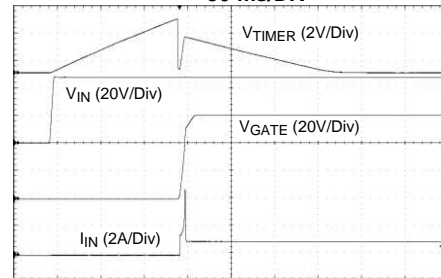
**Startup (Insertion Delay)**  
100 ms/DIV



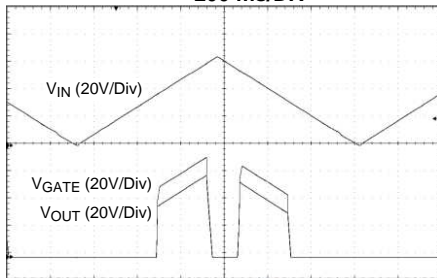
**Startup (Short circuit  $V_{OUT}$ )**  
1s/DIV



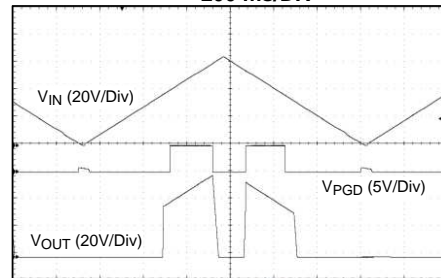
**Startup (1A Load)**  
50 ms/DIV



**Startup (UVLO/EN, OVLO)**  
200 ms/DIV



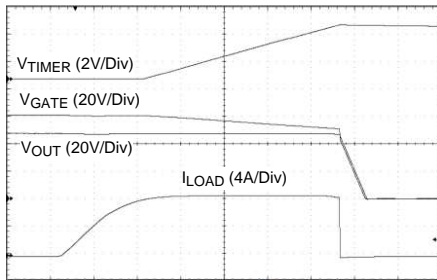
**Startup (PGD)**  
200 ms/DIV



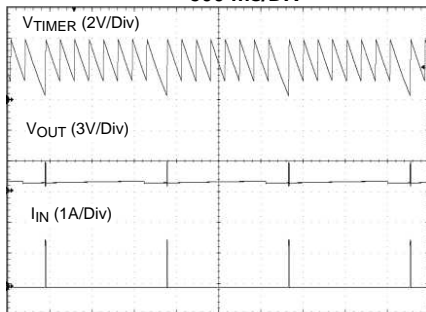
### Typical Performance Characteristics (continued)

Unless otherwise specified the following conditions apply:  $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 48\text{V}$ . All graphs show junction temperature.

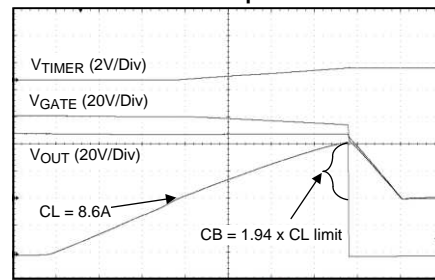
**Current Limit Event (CL = VDD)**  
2 ms/DIV



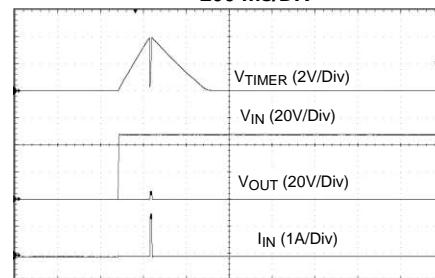
**Retry Event (RETRY = GND)**  
500 ms/DIV



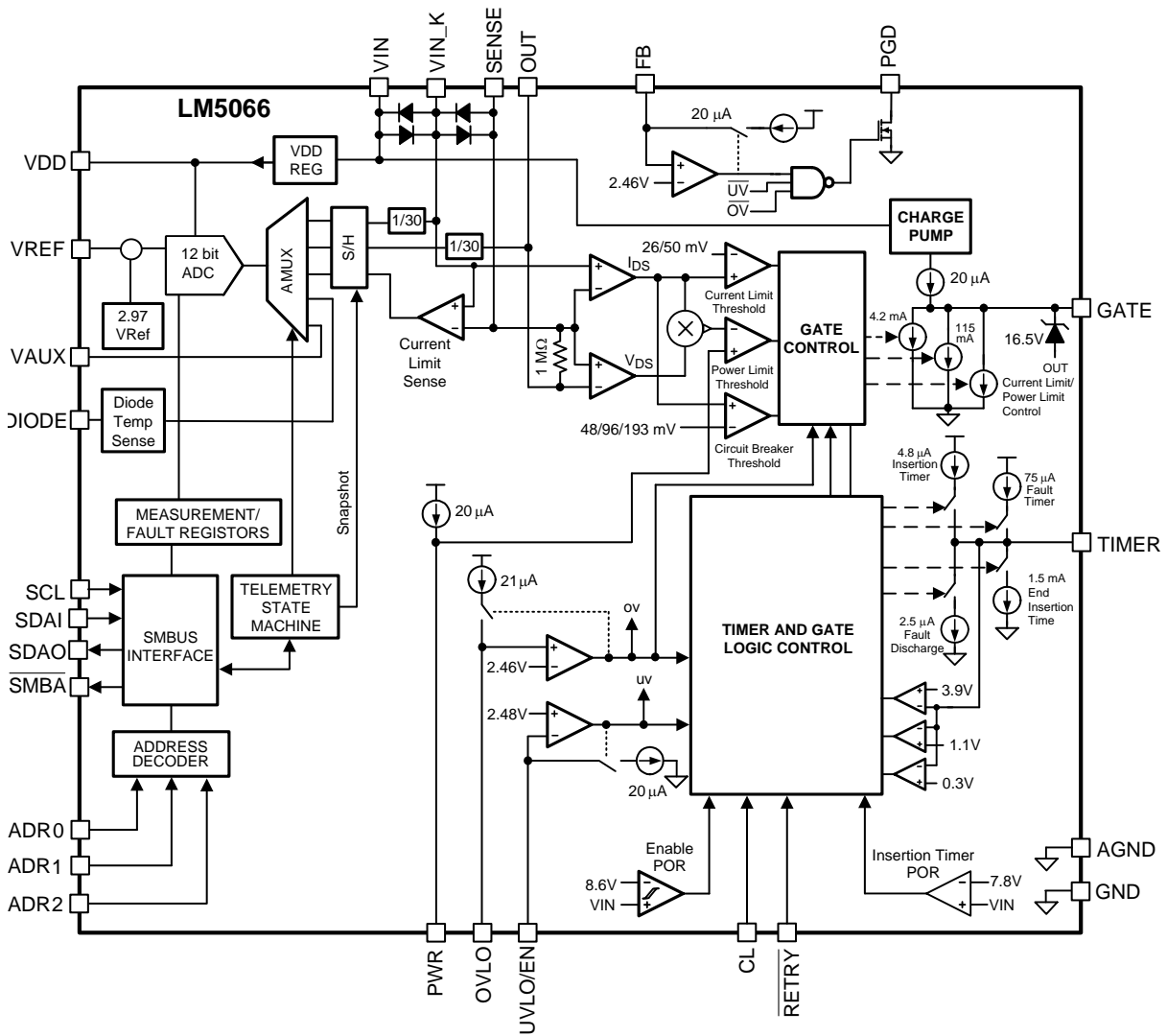
**Circuit Breaker Event (CL = VDD)**  
500  $\mu\text{s}$ /DIV



**Latch Off (RETRY = VDD)**  
200  $\mu\text{s}$ /DIV



**BLOCK DIAGRAM**



## FUNCTIONAL DESCRIPTION

The inline protection functionality of the LM5066 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other “hot” power source, thereby limiting the voltage sag on the backplane’s supply voltage, and the  $dV/dt$  of the voltage applied to the load. The effects on other circuits in the system are minimized by preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the LM5066.

In addition to a programmable current limit, the LM5066 monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LM5066 can latch off or repetitively retry based on the hardware setting of the  $\overline{\text{RETRY}}$  pin. Once started, the number of retries can be set to none, 1, 2, 4, 8, 16, or infinite. The circuit breaker function quickly switches off the series pass device upon detection of a severe over-current condition. Programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) circuits shut down the LM5066 when the system input voltage is outside the desired operating range.

The telemetry capability of the LM5066 provides intelligent monitoring of the input voltage, output voltage, input current, input power, temperature, and an auxiliary input. The LM5066 also provides a peak capture of the input power and programmable hardware averaging of the input voltage, current, power, and output voltage. Warning thresholds which trigger the  $\overline{\text{SMBA}}$  pin may be programmed for input and output voltage, current, power and temperature via the PMBus interface. Additionally, the LM5066 is capable of detecting damage to the external MOSFET,  $Q_1$ .

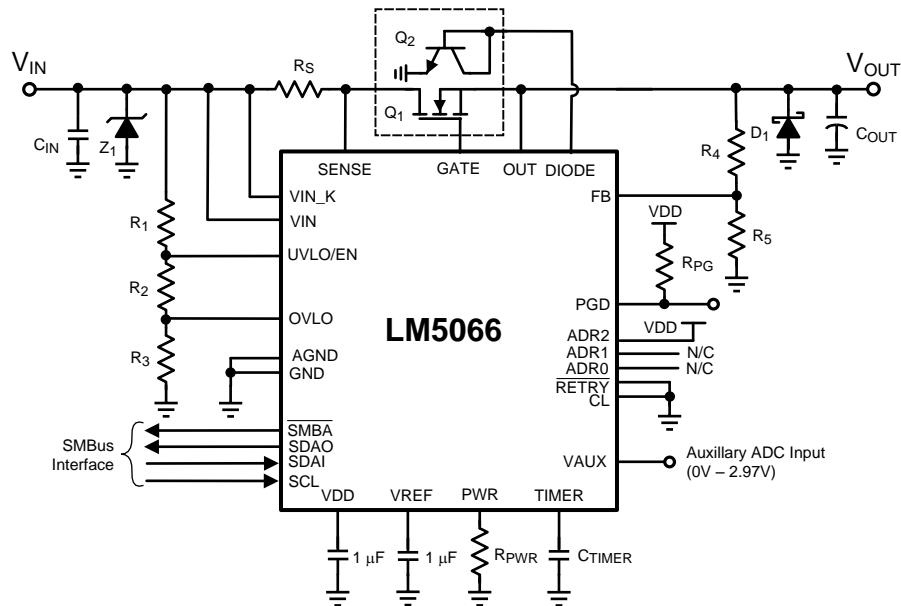


Figure 1. Typical Application Circuit

### Power Up Sequence

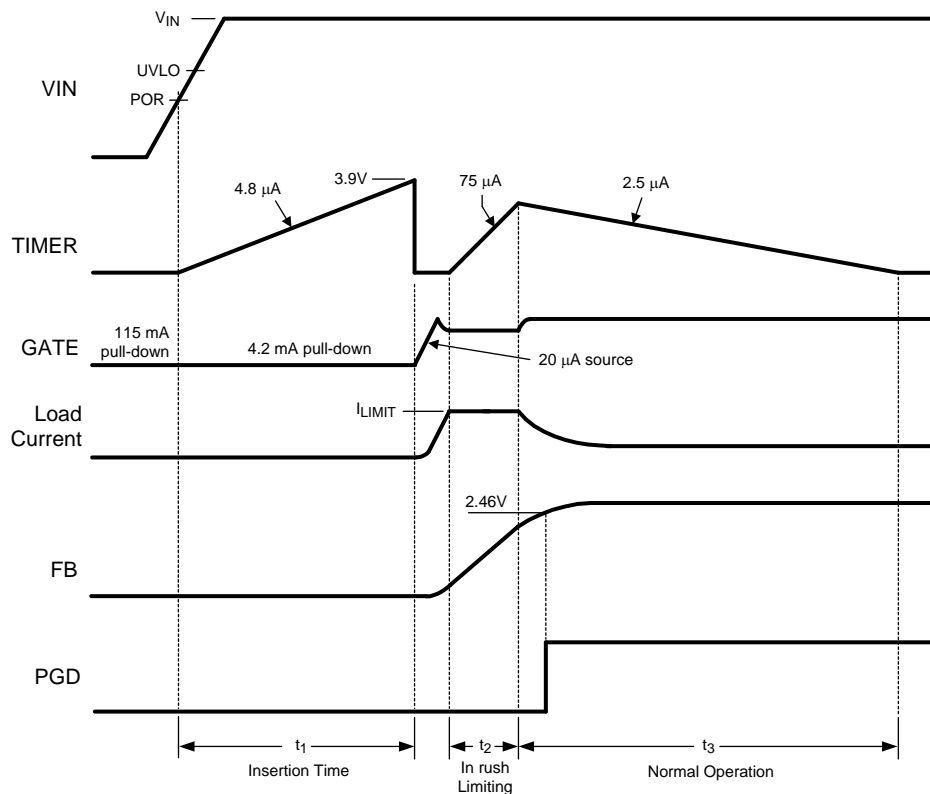
The  $V_{IN}$  operating range of the LM5066 is 10V to 80V, with a transient capability to 100V. Referring to [Figure 1](#) and [Figure 2](#), as the voltage at  $V_{IN}$  initially increases, the external N-channel MOSFET ( $Q_1$ ) is held off by an internal 115 mA pull-down current at the GATE pin. The strong pull-down current at the GATE pin prevents an inadvertent turn-on as the MOSFET’s gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at ground. When the  $V_{IN}$  voltage reaches the POR threshold the insertion time begins. During the insertion time, the capacitor at the TIMER pin ( $C_T$ ) is charged by a 4.8  $\mu\text{A}$  current source, and  $Q_1$  is held off by a 4.2 mA pull-down current at the GATE pin regardless of the input voltage. The insertion time delay allows ringing

and transients at  $V_{IN}$  to settle before  $Q_1$  is enabled. The insertion time ends when the TIMER pin voltage reaches 3.9V.  $C_T$  is then quickly discharged by an internal 1.5 mA pull-down current. The GATE pin then switches on  $Q_1$  when  $V_{IN}$  exceeds the UVLO threshold. If  $V_{IN}$  is above the UVLO threshold at the end of the insertion time,  $Q_1$  the GATE pin charge pump sources 20  $\mu$ A to charge the gate capacitance of  $Q_1$ . The maximum voltage from the gate to source of the  $Q_1$  is limited by an internal 16.5V zener diode.

As the voltage at the OUT pin increases, the LM5066 monitors the drain current and power dissipation of MOSFET  $Q_1$ . In-rush current limiting and/or power limiting circuits actively control the current delivered to the load. During the in-rush limiting interval ( $t_2$  in Figure 2) an internal 75  $\mu$ A fault timer current source charges  $C_T$ . If  $Q_1$ 's power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 3.9V, the 75  $\mu$ A current source is switched off, and  $C_T$  is discharged by the internal 2.5  $\mu$ A current sink ( $t_3$  in Figure 2). The in-rush limiting will no longer engage unless a current-limit condition occurs.

If the TIMER pin voltage reaches 3.9V before in-rush current limiting or power limiting ceases during  $t_2$ , a fault is declared and  $Q_1$  is turned off. See the [Fault Timer & Restart](#) section for a complete description of the fault mode.

The LM5066 will assert the  $\overline{SMBA}$  pin after the input voltage has exceeded its POR threshold to indicate that the volatile memory and device settings are in their default state. The CONFIG\_PRESET bit within the STATUS\_MFR\_SPECIFIC register (80h) indicates default configuration of warning thresholds and device operation and will remain high until a CLEAR\_FAULTS command is received.



**Figure 2. Power Up Sequence (Current Limit Only)**

## Gate Control

A charge pump provides the voltage at the GATE pin to enhance the N-Channel MOSFET's gate ( $Q_1$ ). During normal operating conditions ( $t_3$  in Figure 2) the gate of  $Q_1$  is held charged by an internal 20  $\mu$ A current source. The charge pump peak voltage is roughly 13.5V, which will force a  $V_{GS}$  across  $Q_1$  of 13.5V under normal operation. When the system voltage is initially applied, the GATE pin is held low by a 115 mA pull-down current. This helps prevent an inadvertent turn-on of  $Q_1$  through its drain-gate capacitance as the applied system voltage increases.

During the insertion time ( $t_1$  in [Figure 2](#)) the GATE pin is held low by a 4.2 mA pull-down current. This maintains  $Q_1$  in the off-state until the end of  $t_1$ , regardless of the voltage at VIN or UVLO. Following the insertion time, during  $t_2$  in [Figure 2](#) the gate voltage of  $Q_1$  is modulated to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode, the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 3.9V the TIMER pin capacitor then discharges, and the circuit begins normal operation. If the in-rush limiting condition persists such that the TIMER pin reached 3.9V during  $t_2$ , the GATE pin is then pulled low by the 4.2 mA pull-down current. The GATE pin is then held low until either a power up sequence is initiated (RETRY pin to VDD), or an automatic retry is attempted (RETRY pin to GROUND or floating). See the [Fault Timer & Restart](#) section. If the system input voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 4.2 mA pull-down current to switch off  $Q_1$ .

## Current Limit

The current limit threshold is reached when the voltage across the sense resistor  $R_S$  (VIN to SENSE) exceeds the internal voltage limit of 26 mV or 50 mV depending on whether the CL pin is connected to VDD or GND, respectively. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET  $Q_1$ . While the current limit circuit is active, the fault timer is active as described in the [Fault Timer & Restart](#) section. If the load current falls below the current limit threshold before the end of the Fault Timeout Period, the LM5066 resumes normal operation. If the current limit condition persists for longer than the Fault Timeout Period set by  $C_T$ , the IIN OC Fault bit in the STATUS\_INPUT (7Ch) register, the INPUT bit in the STATUS\_WORD (79h) register, and IIN\_OC/PFET\_OP\_FAULT bit in the DIAGNOSTIC\_WORD (E1h) register will be toggled high and SMBA pin will be asserted. SMBA toggling can be disabled using the ALERT\_MASK (D8h) register. For proper operation, the  $R_S$  resistor value should be no higher than 200 m $\Omega$ . Higher values may create instability in the current limit control loop. The current limit threshold pin value may be overridden by setting appropriate bits in the DEVICE\_SETUP register (D9h).

## Circuit Breaker

If the load current increases rapidly (for example, the load is short circuited) the current in the sense resistor ( $R_S$ ) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds 1.94x or 3.87x (CL = GND) the current limit threshold,  $Q_1$  is quickly switched off by the 115 mA pull-down current at the GATE pin, and a Fault Timeout Period begins. When the voltage across  $R_S$  falls below the circuit breaker (CB) threshold, the 115 mA pull-down current at the GATE pin is switched off, and the gate voltage of  $Q_1$  is then determined by the current limit or the power limit functions. If the TIMER pin reaches 3.9V before the current limiting or power limiting condition ceases,  $Q_1$  is switched off by the 4.2 mA pull-down current at the GATE pin as described in the [Fault Timer & Restart](#) section. A circuit breaker event will cause the CIRCUIT\_BREAKER\_FAULT bit in the STATUS\_MFR\_SPECIFIC (80h) and DIAGNOSTIC\_WORD (E1h) registers to be toggled high and SMBA pin will be asserted unless this feature is disabled using the ALERT\_MASK (D8h) register. The circuit breaker pin configuration may be overridden by setting appropriate bits in the DEVICE\_SETUP (D9h) register.

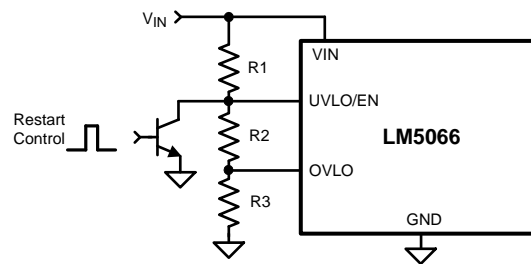
## Power Limit

An important feature of the LM5066 is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET  $Q_1$  within the device SOA rating. The LM5066 determines the power dissipation in  $Q_1$  by monitoring its drain-source voltage (SENSE to OUT), and the drain current through the  $R_S$  (VIN to SENSE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is modulated to regulate the current in  $Q_1$ . While the power limiting circuit is active, the fault timer is active as described in the [Fault Timer & Restart](#) section. If the power limit condition persists for longer than the Fault Timeout Period set by the timer capacitor,  $C_T$ , the IIN OC Fault bit in the STATUS\_INPUT (7Ch) register, the INPUT bit in the STATUS\_WORD (79h) register, and the IIN\_OC/PFET\_OP\_FAULT bit in the DIAGNOSTIC\_WORD (E1h) register will be toggled high and SMBA pin will be asserted unless this feature is disabled using the ALERT\_MASK (D8h) register.

## Fault Timer & Restart

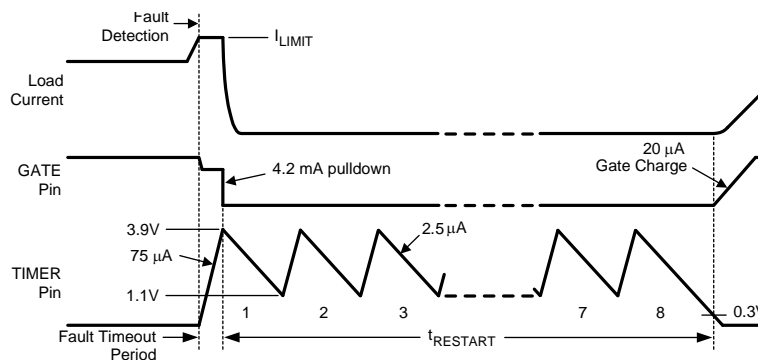
When the current limit or power limit threshold is reached during turn-on, or as a result of a fault condition, the gate-to-source voltage of  $Q_1$  is modulated to regulate the load current and power dissipation in  $Q_1$ . When either limiting function is active, a  $75\ \mu\text{A}$  fault timer current source charges the external capacitor ( $C_T$ ) at the TIMER pin as shown in Figure 2 (Fault Timeout Period). If the fault condition subsides during the Fault Timeout Period before the TIMER pin reaches  $3.9\text{V}$ , the LM5066 returns to the normal operating mode and  $C_T$  is discharged by the  $1.5\ \text{mA}$  current sink. If the TIMER pin reaches  $3.9\text{V}$  during the Fault Timeout Period,  $Q_1$  is switched off by a  $4.2\ \text{mA}$  pull-down current at the GATE pin. The subsequent restart procedure then depends on the selected retry configuration.

If the  $\overline{\text{RETRY}}$  pin is high, the LM5066 latches the GATE pin low at the end of the Fault Timeout Period.  $C_T$  is then discharged to ground by the  $2.5\ \mu\text{A}$  fault current sink. The GATE pin is held low by the  $4.2\ \text{mA}$  pull-down current until a power up sequence is externally initiated by cycling the input voltage ( $V_{\text{IN}}$ ), or momentarily pulling the UVLO/EN pin below its threshold with an open-collector or open-drain device as shown in Figure 3. The voltage at the TIMER pin must be  $<0.3\text{V}$  for the restart procedure to be effective. The  $\text{TIMER\_LATCHED\_OFF}$  bit in the  $\text{DIAGNOSTIC\_WORD}$  (E1h) register will remain high while the latched off condition persists.



**Figure 3. Latched Fault Restart Control**

The LM5066 provides an automatic restart sequence which consists of the TIMER pin cycling between  $3.9\text{V}$  and  $1.1\text{V}$  seven times after the Fault Timeout Period, as shown in Figure 4. The period of each cycle is determined by the  $75\ \mu\text{A}$  charging current, and the  $2.5\ \mu\text{A}$  discharge current, and the value of the capacitor  $C_T$ . When the TIMER pin reaches  $0.3\text{V}$  during the eighth high-to-low ramp, the  $20\ \mu\text{A}$  current source at the GATE pin turns on  $Q_1$ . If the fault condition is still present, the Fault Timeout Period and the restart sequence repeat. The  $\text{RETRY}$  pin allows selecting no retries or infinite retries. Finer control of the retry behavior can be achieved through the  $\text{DEVICE\_SETUP}$  (D9h) register. Retry counts of 0, 1, 2, 4, 8, 16 or infinite may be selected by setting the appropriate bits in the  $\text{DEVICE\_SETUP}$  (D9h) register.



**Figure 4. Restart Sequence**



## Under-Voltage Lockout (UVLO)

The series pass MOSFET ( $Q_1$ ) is enabled when the input supply voltage ( $V_{IN}$ ) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) levels. Typically the UVLO level at  $V_{IN}$  is set with a resistor divider (R1-R3) as shown in Figure 5. Referring to the Block Diagram when  $V_{IN}$  is below the UVLO level, the internal 20  $\mu$ A current source at UVLO is enabled, the current source at OVLO is off, and  $Q_1$  is held off by the 4.2 mA pull-down current at the GATE pin. As  $V_{IN}$  is increased, raising the voltage at UVLO above its threshold the 20  $\mu$ A current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO/EN pin above its threshold,  $Q_1$  is switched on by the 20  $\mu$ A current source at the GATE pin if the insertion time delay has expired.

See the [Application Information](#) section for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level at  $V_{IN}$  can be set by connecting the UVLO/EN pin to  $V_{IN}$ . In this case  $Q_1$  is enabled after the insertion time when the voltage at  $V_{IN}$  reaches the POR threshold. After power up an UVLO condition will cause the INPUT bit in the STATUS\_WORD (79h) register, the VIN\_UV\_FAULT bit in the STATUS\_INPUT (7Ch) register, and the VIN\_UNDERVOLTAGE\_FAULT bit in the DIAGNOSTIC\_WORD (E1h) registers to be toggled high and SMBA pin will be pulled low unless this feature is disabled using the ALERT\_MASK (D8h) register.

## Over-Voltage Lockout (OVLO)

The series pass MOSFET ( $Q_1$ ) is enabled when the input supply voltage ( $V_{IN}$ ) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lockout (OVLO) levels. If  $V_{IN}$  raises the OVLO pin voltage above its threshold,  $Q_1$  is switched off by the 4.2 mA pull-down current at the GATE pin, denying power to the load. When the OVLO pin is above its threshold, the internal 21  $\mu$ A current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When  $V_{IN}$  is reduced below the OVLO level  $Q_1$  is re-enabled. An OVLO condition will toggle the VIN\_OV\_FAULT bit in the STATUS\_INPUT (7Ch) register, the INPUT bit in the STATUS\_WORD (79h) register and the VIN\_OVERVOLTAGE\_FAULT bit in the DIAGNOSTIC\_WORD (E1h) register. The SMBA pin will be pulled low unless this feature is disabled using the ALERT\_MASK (D8h) register.

See the [Application Information](#) section for a procedure to calculate the threshold setting resistor values.

## Shutdown Control

The load current can be remotely switched off by taking the UVLO/EN pin below its threshold with an open collector or open drain device, as shown in Figure 5. Upon releasing the UVLO/EN pin the LM5066 switches on the load current with in-rush current and power limiting.

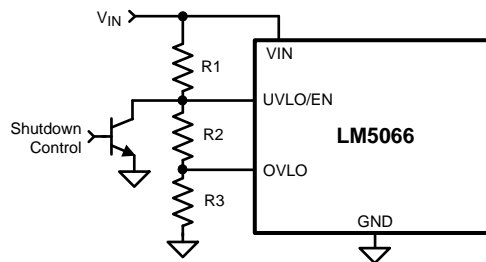


Figure 5. Shutdown Control

## Power Good Pin

The Power Good indicator pin (PGD) is connected to the drain of an internal N-channel MOSFET capable of sustaining 80V in the off-state, and transients up to 100V. An external pull-up resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin can be higher or lower than the voltages at  $V_{IN}$  and  $OUT$ . PGD is switched high when the voltage at the FB pin exceeds the PGD threshold voltage. Typically the output voltage threshold is set with a resistor divider from output to feedback, although the monitored voltage need not be the output voltage. Any other voltage can be monitored as long as the voltage at the FB pin does not exceed its maximum rating. Referring to the Block Diagram, when the

voltage at the FB pin is below its threshold, the 20  $\mu\text{A}$  current source at FB is disabled. As the output voltage increases, taking FB above its threshold, the current source is enabled, sourcing current out of the pin, raising the voltage at FB to provide threshold hysteresis. The PGD output is forced low when either the UVLO/EN pin is below its threshold or the OVLO pin is above its threshold. The status of the PGD pin can be read via the PMBus interface in either the STATUS\_WORD (79h) or DIAGNOSTIC\_WORD (E1h) registers.

## VDD Sub-Regulator

The LM5066 contains an internal linear sub-regulator which steps down the input voltage to generate a 4.9V rail used for powering low voltage circuitry. The VDD sub-regulator should be used as the pull-up supply for the CL, RETRY, ADR2, ADR1, ADR0 pins if they are to be tied high. It may also be used as the pull-up supply for the PGD and the SMBus signals (SDA, SCL, SMBA). The VDD sub-regulator is not designed to drive high currents and should not be loaded with other integrated circuits. The VDD pin is current limited to 30mA in order to protect the LM5066 in the event of a short. The sub-regulator requires a ceramic bypass capacitance having a value of 1  $\mu\text{F}$  or greater to be placed as close to the VDD pin as the PCB layout allows.

## Remote Temperature Sensing

The LM5066 is designed to measure temperature remotely using an MMBT3904 NPN transistor. The base and collector of the MMBT3904 should be connected to the DIODE pin and the emitter to the LM5066 ground. Place the MMBT3904 near the device that requires temperature sensing. If the temperature of the hot swap pass MOSFET,  $Q_1$ , is to be measured, the MMBT3904 should be placed as close to  $Q_1$  as the layout allows. The temperature is measured by means of a change in the diode voltage in response to a step in current supplied by the DIODE pin. The DIODE pin sources a constant 9.4  $\mu\text{A}$  but pulses 250  $\mu\text{A}$  once every millisecond in order to measure the diode temperature. Care must be taken in the PCB layout to keep the parasitic resistance between the DIODE pin and the MMBT3904 low so as not to degrade the measurement. Additionally, a small 1000 pF bypass capacitor should be placed in parallel with the MMBT3904 to reduce the effects of noise. The temperature can be read using the READ\_TEMPERATURE\_1 PMBus command (8Dh). The default limits of the LM5066 will cause SMBA pin to be pulled low if the measured temperature exceeds 125°C and will disable  $Q_1$  if the temperature exceeds 150°C. These thresholds can be reprogrammed via the PMBus interface using the OT\_WARN\_LIMIT (51h) and OT\_FAULT\_LIMIT (4Fh) commands. If the temperature measurement and protection capability of the LM5066 are not used, the DIODE pin should be grounded.

Erroneous temperature measurements may result when the device input voltage is below the minimum operating voltage (10V), due to VREF dropping out below the nominal voltage (2.97V). At higher ambient temperatures, this measurement could read a value higher than the OT\_FAULT\_LIMIT, and will trigger a fault, disabling  $Q_1$ . In this case, the faults should be removed and the device reset by writing a 0h, followed by an 80h to the OPERATION (03h) register.

## Damaged MOSFET Detection

The LM5066 is able to detect whether the external MOSFET,  $Q_1$ , is damaged under certain conditions. If the voltage across the sense resistor exceeds 4mV while the GATE voltage is low or the internal logic indicates that the GATE should be low, the EXT\_MOSFET\_SHORTED bit in the STATUS\_MFR\_SPECIFIC (80h) and DIAGNOSTIC\_WORD (E1h) registers will be toggled high and the SMBA pin will be asserted unless this feature is disabled using the ALERT\_MASK register (D8h). This method effectively determines whether  $Q_1$  is shorted because of damage present between the drain and gate and/or drain and source.

## Enabling/Disabling and Resetting

The output can be disabled at any time during normal operation by either pulling the UVLO/EN pin to below its threshold or the OVLO pin above its threshold, causing the GATE voltage to be forced low with a pulldown strength of 4.2mA. Toggling the UVLO/EN pin will also reset the LM5066 from a latched-off state due to an over-current or over-power limit condition which has caused the maximum allowed number of retries to be exceeded. While the UVLO/EN or OVLO pins can be used to disable the output they have no effect on the volatile memory or address location of the LM5066. User stored values for address, device operation, and warning and fault levels programmed via the SMBus are preserved while the LM5066 is powered regardless of the state of the UVLO/EN and OVLO pins. The output may also be enabled or disabled by writing 80h or 0h to the OPERATION (03h) register. To re-enable after a fault, the fault condition should be cleared and the OPERATION (03h) register with 0h and then 80h.

The SMBus address of the LM5066 is captured based on the states of the ADR0, ADR1, and ADR2 pins (GND, NC, VDD) during turn on and is latched into a volatile register once VDD has exceeded its POR threshold of 4.1V. Reassigning or postponing the address capture is accomplished by holding the VREF pin to ground. Pulling the VREF pin low will also reset the logic and erase the volatile memory of the LM5066. Once released, the VREF pin will charge up to its final value and the address will be latched into a volatile register once the voltage at the VREF exceeds 2.55V.

## APPLICATION INFORMATION

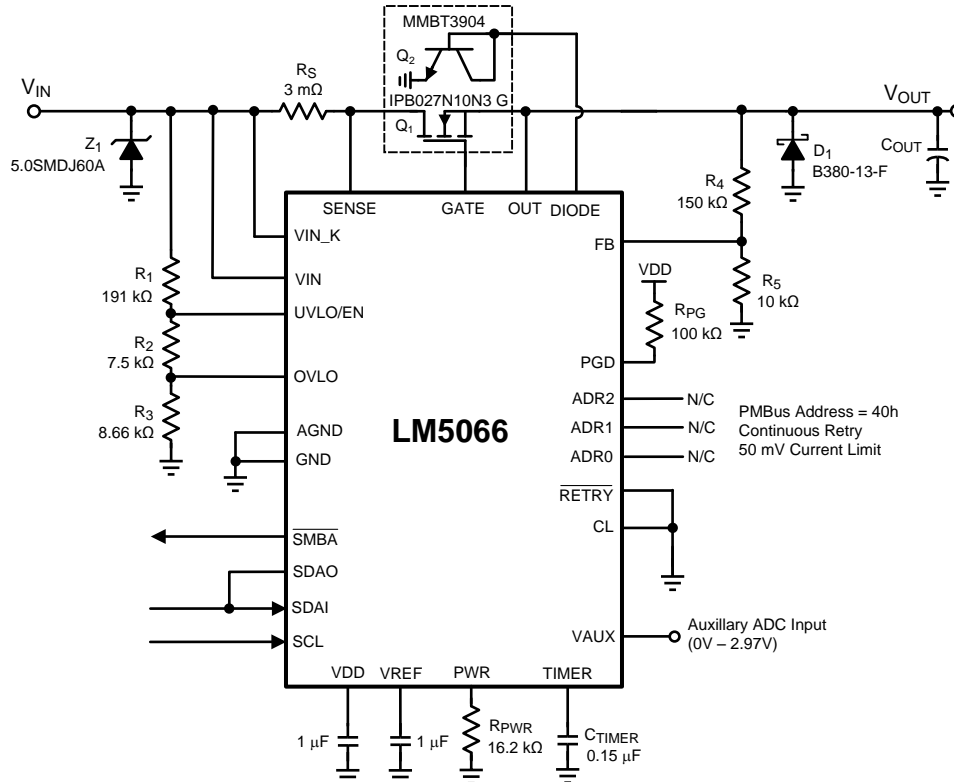


Figure 6. Typical Application Circuit

### DESIGN-IN PROCEDURE

Refer to [Figure 6](#) for Typical Application Circuit. The following is the step-by-step procedure for hardware design of the LM5066. This procedure refers to section numbers that provide detailed information on the following design steps. The recommended design-in procedure is as follows:

**MOSFET Selection:** Determine MOSFET based on breakdown voltage, current and power ratings.

**Current Limit,  $R_S$ :** Determine the current limit threshold ( $I_{LIM}$ ). This threshold must be higher than the normal maximum load current, allowing for tolerances in the current sense resistor value and the LM5066 Current Limit threshold voltage. Use [Equation 1](#) to determine the value for  $R_S$ .

**Power Limit Threshold:** Determine the maximum allowable power dissipation for the series pass MOSFET ( $Q_1$ ), using the device's SOA information. Use [Equation 2](#) to determine the value for  $R_{PWR}$ . Note that many MOSFET manufacturers do not accurately specify the device SOA so it is usually beneficial to choose a conservative value when selecting  $R_{PWR}$ .

**Turn-on Time and TIMER Capacitor,  $C_T$ :** Determine the value for the timing capacitor at the TIMER pin ( $C_T$ ) using [Equation 7](#) and [Equation 8](#). The fault timeout period ( $t_{FAULT}$ ) **MUST** be longer than the circuit's turn-on time. The turn-on time can be estimated using the equations in the [TURN-ON TIME](#) section, but should be verified experimentally. Review the resulting insertion time and the restart timing if retry is enabled.

**UVLO, OVLO:** Choose option A, B, C, or D from the [UVLO, OVLO](#) section to set the UVLO and OVLO thresholds and hysteresis. Use the procedure for the appropriate option to determine the resistor values at the UVLO/EN and OVLO pins.

**Power Good:** Choose the appropriate output voltage and calculate the required resistor divider from the output voltage to the FB pin. Choose either VDD or OUT to connect a properly sized pull-up resistor for the Power Good output (PGD).

**Refer to Programming Guide section:** After all hardware design is complete, refer to the programming guide for a step by step procedure regarding software.

## MOSFET SELECTION

It is recommended that the external MOSFET ( $Q_1$ ) selection is based on the following criteria:

- The  $BV_{DSS}$  rating should be greater than the maximum system voltage ( $V_{IN}$ ), plus ringing and transients which can occur at  $V_{IN}$  when the circuit card, or adjacent cards, are inserted or removed.
- The maximum continuous current rating should be based on the current limit threshold (for example,  $26\text{ mV}/R_S$  for  $CL = VDD$ ), not the maximum load current, since the circuit can operate near the current limit threshold continuously.
- The Pulsed Drain Current spec ( $I_{DM}$ ) must be greater than the current threshold for the circuit breaker function ( $48/96/193\text{ mV}/R_S$ , depending on CL and CB configuration).
- The SOA (Safe Operating Area) chart of the device, and the thermal properties, should be used to determine the maximum power dissipation threshold set by the  $R_{PWR}$  resistor. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the MOSFET's SOA curve. If the device is set to infinitely retry, the MOSFET will be repeatedly stressed during fault restart cycles. The MOSFET manufacturer should be consulted for guidelines.
- $R_{DS(on)}$  should be sufficiently low such that the power dissipation at maximum load current ( $I_{LIM}^2 \times R_{DS(on)}$ ) does not raise its junction temperature above the manufacturer's recommendation.
- The gate-to-source voltage provided by the LM5066 can be as high as 16.5V, limited by the internal zener diode from GATE to OUT.  $Q_1$  must be able to tolerate this voltage for its  $V_{GS}$  rating. An additional zener diode can be added from GATE to OUT to lower this voltage and limit the peak  $V_{GS}$ . The zener diode's forward current rating must be at least 110 mA to conduct the GATE pull-down current when a circuit breaker condition is detected.

## CURRENT LIMIT ( $R_S$ )

The LM5066 monitors the current in the external MOSFET  $Q_1$  by measuring the voltage across the sense resistor ( $R_S$ ), connected from  $V_{IN}$  to SENSE. The required resistor value is calculated from:

$$R_S = \frac{V_{CL}}{I_{LIM}} \quad (1)$$

where  $I_{LIM}$  is the desired current limit threshold. If the voltage across  $R_S$  reaches  $V_{CL}$ , the current limit circuit modulates the gate of  $Q_1$  to regulate the current at  $I_{LIM}$ . While the current limiting circuit is active, the fault timer is active as described in the [Fault Timer & Restart](#) section. For proper operation,  $R_S$  must be less than 200 m $\Omega$ .

$V_{CL}$  can be set to either 26 mV or 50 mV via hardware and/or software. This setting defaults to use of CL pin which, when connected to VDD is 26 mV, or grounded is 50 mV. The value, when powered, can be set via the PMBus with the MFR\_SPECIFIC\_DEVICE\_SETUP command, which defaults to the 26 mV setting.

Once the desired setting is known, calculate the shunt based on that input voltage and maximum current. While the maximum load current in normal operation can be used to determine the required power rating for resistor  $R_S$ , basing it on the current limit value provides a more reliable design since the circuit can operate near the current limit threshold continuously. The resistor's surge capability must also be considered since the circuit breaker threshold is 1.94 or 3.87 times the current limit threshold.

Connections from  $R_S$  to the LM5066 should be made using Kelvin techniques. In the suggested layout of [Figure 7](#) the small pads at the lower corners of the sense resistor connect only to the sense resistor terminals, and not to the traces carrying the high current. With this technique, only the voltage across the sense resistor is applied to  $V_{IN\_K}$  and SENSE, eliminating the voltage drop across the high current solder connections.



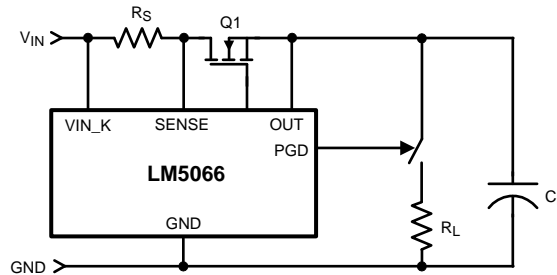
$$t_{ON} = \frac{V_{SYS} \times C_L}{I_{LIM}} \quad (4)$$

where  $C_L$  is the load capacitance. For example, if  $V_{IN} = 48V$ ,  $C_L = 200 \mu F$ , and  $I_{LIM} = 5A$ ,  $t_{ON}$  calculates to 12 ms. The maximum instantaneous power dissipated in the MOSFET is 12W. This calculation assumes the time from  $t_1$  to  $t_2$  in Figure 9(a) is small compared to  $t_{ON}$ , the load does not draw any current until after the output voltage has reached its final value, and PGD switches high (Figure 8A). The Fault Timeout Period must be set longer than  $t_{ON}$  to prevent a fault shutdown before the turn-on sequence is complete.

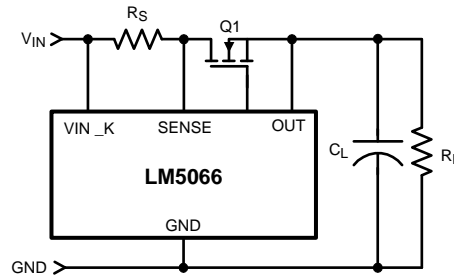
If the load draws current during the turn-on sequence (Figure 8B), the turn-on time is longer than the above calculation, and is approximately equal to:

$$t_{ON} = -(R_L \times C_L) \times \ln \left[ \frac{(I_{LIM} \times R_L) - V_{SYS}}{(I_{LIM} \times R_L)} \right] \quad (5)$$

where  $R_L$  is the load resistance. The Fault Timeout Period must be set longer than  $t_{ON}$  to prevent a fault shutdown before the turn-on sequence is complete.



A. No Load Current During Turn-On



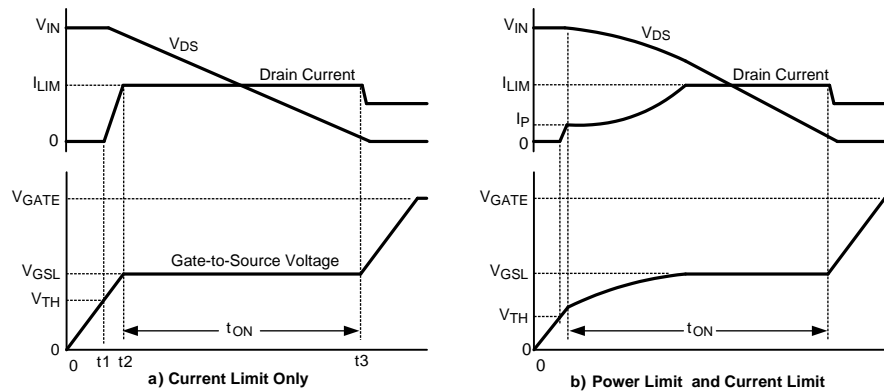
B. Load Draws Current During Turn-On

Figure 8. Current During Turn-On

**B) Turn-On with Power Limit and Current Limit:** The maximum allowed power dissipation in  $Q_1$  ( $P_{MOSFET(LIM)}$ ) is defined by the resistor at the PWR pin, and the current sense resistor  $R_S$ . See the **POWER LIMIT THRESHOLD** section. If the current limit threshold ( $I_{LIM}$ ) is higher than the current defined by the power limit threshold at maximum  $V_{DS}$  ( $P_{MOSFET(LIM)}/V_{IN}$ ) the circuit operates initially in the power limit mode when the  $V_{DS}$  of  $Q_1$  is high, and then transitions to current limit mode as the current increases to  $I_{LIM}$  and  $V_{DS}$  decreases. Assuming the load ( $R_L$ ) is not connected during turn-on, the time for the output voltage to reach its final value is approximately equal to:

$$t_{ON} = \frac{C_L \times V_{IN}^2}{2 \times P_{MOSFET(LIM)}} + \frac{C_L \times P_{MOSFET(LIM)}}{2 \times I_{LIM}^2} \quad (6)$$

For example, if  $V_{IN} = 48V$ ,  $C_L = 200 \mu F$ ,  $I_{LIM} = 1A$ , and  $P_{MOSFET(LIM)} = 10W$ ,  $t_{ON}$  calculates to  $\approx 24$  ms, and the initial current level ( $I_p$ ) is approximately 0.208A. The Fault Timeout Period must be set longer than  $t_{ON}$ .



**Figure 9. MOSFET Power Up Waveforms**

### TIMER CAPACITOR, $C_T$

The TIMER pin capacitor ( $C_T$ ) sets the timing for the insertion time delay, fault timeout period, and the restart timing of the LM5066.

**A) Insertion Delay** -Upon applying the system voltage ( $V_{IN}$ ) to the circuit, the external MOSFET ( $Q_1$ ) is held off during the insertion time ( $t_1$  in Figure 2) to allow ringing and transients at  $V_{IN}$  to settle. Since each backplane's response to a circuit card plug-in is unique, the worst case settling time must be determined for each application. The insertion time starts when  $V_{IN}$  reaches the POR threshold, at which time the internal 4.8  $\mu A$  current source charges  $C_T$  from 0V to 3.9V. The required capacitor value is calculated from:

$$C_T = \frac{t_1 \times 4.8 \mu A}{3.9V} = t_1 \times 1.2 \times 10^{-6} \quad (7)$$

For example, if the desired insertion delay is 250 ms,  $C_T$  calculates to 0.3  $\mu F$ . At the end of the insertion delay,  $C_T$  is quickly discharged by a 1.5 mA current sink.

**B) Fault Timeout Period** -During in-rush current limiting or upon detection of a fault condition where the current limit and/or power limit circuits regulate the current through  $Q_1$ , the fault timer current source (75  $\mu A$ ) is switched on to charge  $C_T$ . The Fault Timeout Period is the time required for the TIMER pin voltage to reach 3.9V, at which time  $Q_1$  is switched off. The required capacitor value for the desired Fault Timeout Period  $t_{FAULT}$  is calculated from:

$$C_T = \frac{t_{FAULT} \times 75 \mu A}{3.9V} = t_{FAULT} \times 1.9 \times 10^{-5} \quad (8)$$

For example, if the desired Fault Timeout Period is 15 ms,  $C_T$  calculates to 0.3  $\mu F$ .  $C_T$  is discharged by the 2.5  $\mu A$  current sink at the end of the Fault Timeout Period. After the Fault Timeout Period, if retry is disabled, the LM5066 latches the GATE pin low until a power up sequence is initiated by external circuitry. When the Fault Timeout Period of the LM5066 expires, a restart sequence starts as described below (Restart Timing). During consecutive cycles of the restart sequence, the fault timeout period is shorter than the initial fault time out period described above by approximately 8% since the voltage at the TIMER pin starts ramping up from 0.3V rather than ground.

Since the LM5066 normally operates in power limit and/or current limit during a power up sequence, the Fault Timeout Period **MUST** be longer than the time required for the output voltage to reach its final value. See the **TURN-ON TIME** section.

**C) Restart Timing** For the LM5066, after the Fault Timeout Period described above,  $C_T$  is discharged by the 2.5  $\mu A$  current sink to 1.1V. The TIMER pin then cycles through seven additional charge/discharge cycles between 1.1V and 3.9V as shown in Figure 4. The restart time ends when the TIMER pin voltage reaches 0.3V during the final high-to-low ramp. The restart time, after the Fault Timeout Period, is equal to:

$$t_{RESTART} = C_T \times \left[ \frac{7 \times 2.8V}{2.5\mu A} + \frac{7 \times 2.8V}{75\mu A} + \frac{3.6V}{2.5\mu A} \right] \quad (9)$$

$$= C_T \times 9.5 \times 10^6 \quad (10)$$



For example, if  $C_T = 0.8 \mu\text{F}$ ,  $t_{\text{RESTART}} = 7.9$  seconds. At the end of the restart time,  $Q_1$  is switched on. If the fault is still present, the fault timeout and restart sequence repeats. The on-time duty cycle of  $Q_1$  is approximately 0.5% in this mode.

### UVLO, OVLO

By programming the UVLO and OVLO thresholds the LM5066 enables the series pass device ( $Q_1$ ) when the input supply voltage ( $V_{\text{IN}}$ ) is within the desired operational range. If  $V_{\text{IN}}$  is below the UVLO threshold, or above the OVLO threshold,  $Q_1$  is switched off, denying power to the load. Hysteresis is provided for each threshold.

**Option A:** The configuration shown in Figure 10 requires three resistors (R1-R3) to set the thresholds.

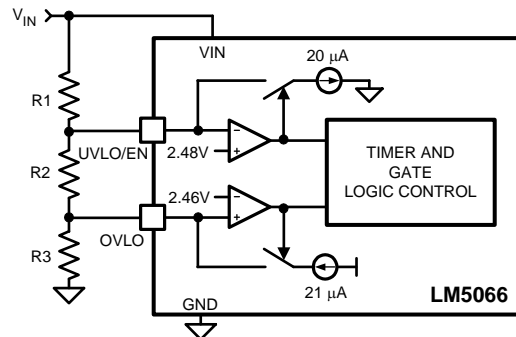


Figure 10. UVLO and OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

- Choose the upper UVLO threshold ( $V_{\text{UVH}}$ ), and the lower UVLO threshold ( $V_{\text{UVL}}$ ).
- Choose the upper OVLO threshold ( $V_{\text{OVH}}$ ).
- The lower OVLO threshold ( $V_{\text{OVL}}$ ) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If  $V_{\text{OVL}}$  must be accurately defined in addition to the other three thresholds, see **Option B** below. The resistors are calculated as follows:

$$R1 = \frac{V_{\text{UVH}} - V_{\text{UVL}}}{20 \mu\text{A}} = \frac{V_{\text{UV(HYS)}}}{20 \mu\text{A}} \quad (11)$$

$$R3 = \frac{R1 \times V_{\text{UVL}} \times 2.46\text{V}}{V_{\text{OVH}} \times (V_{\text{UVL}} - 2.48\text{V})} \quad (12)$$

$$R2 = \frac{2.48\text{V} \times R1}{V_{\text{UVL}} - 2.48\text{V}} - R3 \quad (13)$$

The lower OVLO threshold is calculated from:

$$V_{\text{OVL}} = \left[ (R1 + R2) \times \left( \frac{2.46\text{V}}{R3} \right) - 21 \mu\text{A} \right] + 2.46\text{V} \quad (14)$$

As an example, assume the application requires the following thresholds:  $V_{\text{UVH}} = 36\text{V}$ ,  $V_{\text{UVL}} = 32\text{V}$ ,  $V_{\text{OVH}} = 60\text{V}$ .

$$R1 = \frac{36\text{V} - 32\text{V}}{20 \mu\text{A}} = \frac{4\text{V}}{20 \mu\text{A}} = 200\text{k} \quad (15)$$

$$R3 = \frac{R1 \times 32\text{V} \times 2.46\text{V}}{60\text{V} \times (32\text{V} - 2.48\text{V})} = 8.89 \text{ k}\Omega \quad (16)$$

$$R2 = \frac{2.48\text{V} \times R1}{32\text{V} - 2.48\text{V}} - R3 = 7.91 \text{ k}\Omega \quad (17)$$

The lower OVLO threshold calculates to 55.6V, and the OVLO hysteresis is 4.4V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration. When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.48V + R1 \times \left( \frac{2.48V}{R2 + R3} + 20 \mu A \right) \quad (18)$$

$$V_{UVL} = \frac{2.48V \times (R1 + R2 + R3)}{R2 + R3} \quad (19)$$

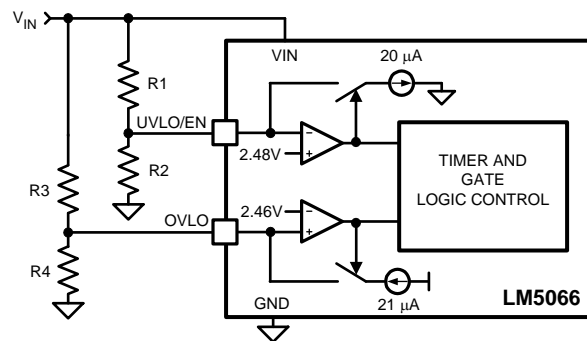
$$V_{UV(HYS)} = R1 \times 20\mu A \quad (20)$$

$$V_{OVH} = \frac{2.46V \times (R1 + R2 + R3)}{R3} \quad (21)$$

$$V_{OVL} = \left( \frac{2.46V}{R3} - 21 \mu A \right) \times (R1 + R2) + 2.46V \quad (22)$$

$$V_{OV(HYS)} = (R1 + R2) \times 21\mu A \quad (23)$$

**Option B:** If all four thresholds must be accurately defined, the configuration in [Figure 11](#) can be used.



**Figure 11. Programming the Four Thresholds**

The four resistor values are calculated as follows: - Choose the upper and lower UVLO thresholds ( $V_{UVH}$ ) and ( $V_{UVL}$ ).

$$R1 = \frac{V_{UVH} - V_{UVL}}{20 \mu A} = \frac{V_{UV(HYS)}}{20 \mu A} \quad (24)$$

$$R2 = \frac{2.48V \times R1}{(V_{UVL} - 2.48V)} \quad (25)$$

- Choose the upper and lower OVLO threshold ( $V_{OVH}$ ) and ( $V_{OVL}$ ).

$$R3 = \frac{V_{OVH} - V_{OVL}}{21 \mu A} \quad (26)$$

$$R4 = \frac{2.46V \times R3}{(V_{OVH} - 2.46V)} \quad (27)$$

As an example, assume the application requires the following thresholds:  $V_{UVH} = 36V$ ,  $V_{UVL} = 32V$ ,  $V_{OVH} = 60V$ , and  $V_{OVL} = 56V$ . Therefore  $V_{UV(HYS)} = 4V$ , and  $V_{OV(HYS)} = 4V$ . The resistor values are:

$$R1 = 200 \text{ k}\Omega, R2 = 16.8 \text{ k}\Omega$$

$$R3 = 190 \text{ k}\Omega, R4 = 8.1 \text{ k}\Omega$$

When the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.48V + \left[ R1 \times \left( \frac{2.48V}{R2} + 20 \mu A \right) \right] \quad (28)$$

$$V_{UVL} = \frac{2.48V \times (R1 + R2)}{R2} \quad (29)$$

$$V_{UV(HYS)} = R1 \times 20 \mu A \quad (30)$$

$$V_{OVH} = \frac{2.46V \times (R3 + R4)}{R4} \quad (31)$$

$$V_{OVL} = 2.46V + \left[ R3 \times \left( \frac{2.46V}{R4} - 21 \mu A \right) \right] \quad (32)$$

**Option C:** The minimum UVLO level is obtained by connecting the UVLO/EN pin to VIN as shown in Figure 12. Q1 is switched on when the VIN voltage reaches the POR<sub>EN</sub> threshold (≈8.6V). The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in **Option B**.

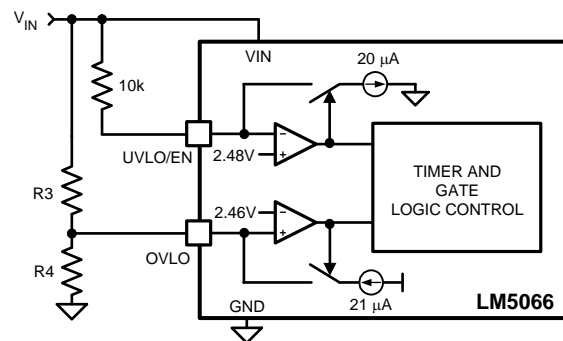


Figure 12. UVLO = POR<sub>EN</sub>

**Option D:** The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in **Option B** or **Option C**.

### POWER GOOD PIN

When the voltage at the FB pin increases above its threshold the internal pulldown acting on the PGD pin is disabled allowing PGD to rise to V<sub>PGD</sub> through the pull-up resistor, R<sub>PG</sub>, as shown in Figure 14. The pull-up voltage (V<sub>PGD</sub>) can be as high as 80V, and can be higher or lower than the voltages at VIN and OUT. VDD is a convenient choice for V<sub>PGD</sub> as it allows interface to low voltage logic and avoids glitching on PGD during power-up. If a delay is required at PGD, suggested circuits are shown in Figure 15. In Figure 15A, capacitor C<sub>PG</sub> adds delay to the rising edge, but not to the falling edge. In Figure 15B, the rising edge is delayed by R<sub>PG1</sub> + R<sub>PG2</sub> and C<sub>PG</sub>, while the falling edge is delayed a lesser amount by R<sub>PG2</sub> and C<sub>PG</sub>. Adding a diode across R<sub>PG2</sub> (Figure 15C) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

Setting the output threshold for the PGD pin requires two resistors (R4, R5) as shown in Figure 13. While monitoring the output voltage is shown in Figure 13, R4 can be connected to any other voltage which requires monitoring.

The resistor values are calculated as follows:

Choose the upper and lower threshold (V<sub>PGDH</sub>) and (V<sub>PGDL</sub>) at V<sub>OUT</sub>.

$$R4 = \frac{V_{PGDH} - V_{PGDL}}{20 \mu A} = \frac{V_{PGD(HYS)}}{20 \mu A} \quad (33)$$

$$R5 = \frac{2.46V \times R4}{(V_{PGDH} - 2.46V)} \quad (34)$$

As an example, assume the application requires the following thresholds:  $V_{PGDH} = 40V$ , and  $V_{PGDL} = 38V$ . Therefore  $V_{PGD(HYS)} = 2V$ . The resistor values are:

$$R4 = 100\text{ k}\Omega, R5 = 6.55\text{ k}\Omega$$

When the R4 and R5 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{PGDH} = \frac{2.46V \times (R4 + R5)}{R5}$$

$$V_{PGDL} = 2.46V + \left[ R4 \times \frac{(2.46V - 20\ \mu A)}{R5} \right]$$

$$V_{PGD(HYS)} = R4 \times 20\ \mu A$$

(35)

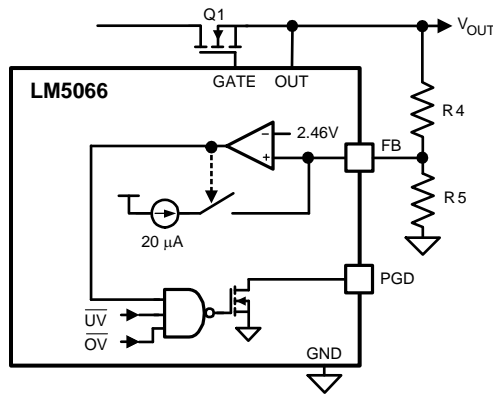


Figure 13. Programming the PGD Threshold

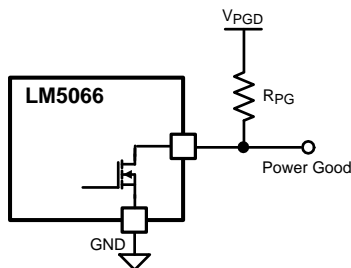


Figure 14. Power Good Output

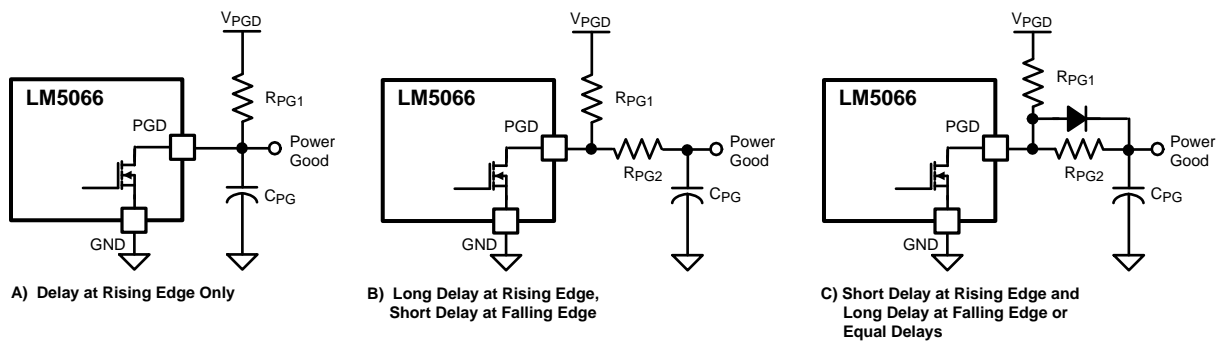


Figure 15. Adding Delay to the Power Good Output Pin

## SYSTEM CONSIDERATIONS

A) Continued proper operation of the LM5066 hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Figure 16. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. If the TVS is not present, inductance in the supply lines will generate a voltage transient at shut-off which can exceed the absolute maximum rating of the LM5066, resulting in its destruction. For low current solutions (<2A), a capacitor may be sufficient to limit the voltage surge, however this comes at the expense of input surge current on card insertion.

If the load powered by the LM5066 hot swap circuit has inductive characteristics, a Schottky diode is required across the LM5066's output, along with some load capacitance. The capacitance and the diode are necessary to limit the negative excursion at the OUT pin when the load current is shut off. If the OUT pin transitions more than 0.3V negative the LM5066 can be permanently damaged. See Figure 16.

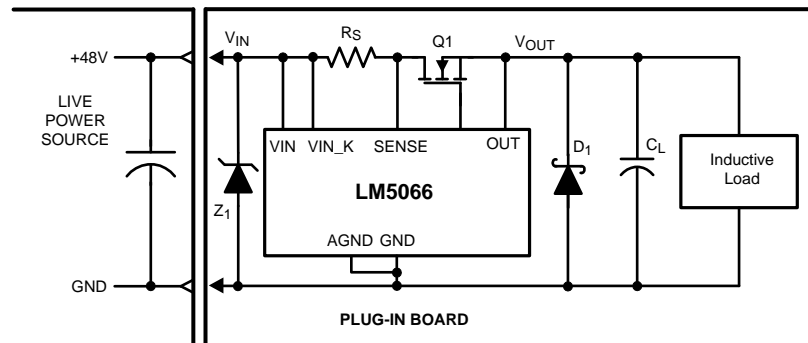


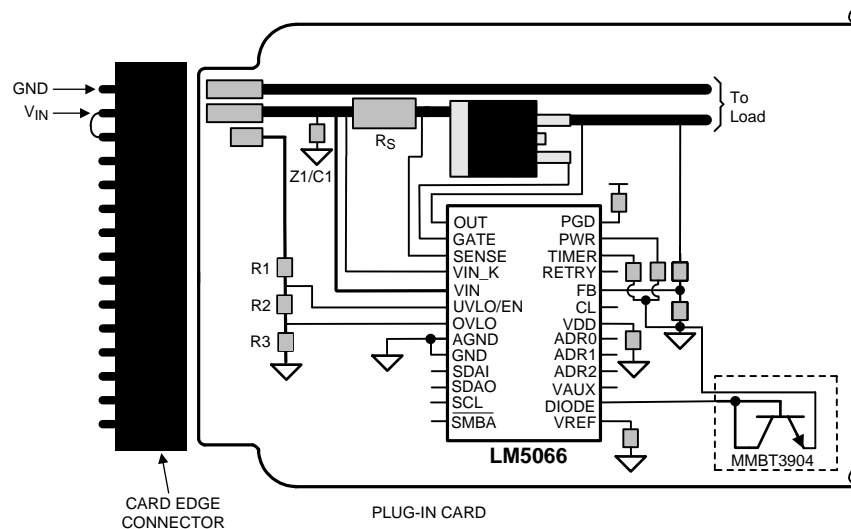
Figure 16. Output Diode Required for Inductive Loads

## PC BOARD GUIDELINES

The following guidelines should be followed when designing the PC board for the LM5066:

- Place the LM5066 close to the board's input connector to minimize trace inductance from the connector to the MOSFET.
- Place a TVS,  $Z_1$ , directly adjacent to the VIN and GND pins of the LM5066 to help minimize voltage transients which may occur on the input supply line. The TVS should be chosen such that the peak  $V_{IN}$  is just lower the TVS reverse-bias voltage. Transients of 20 volts or greater over the nominal input voltage can easily occur when the load current is shut off. A small capacitor may be sufficient for low current sense applications ( $I < 2A$ ). It is recommended to test the VIN input voltage transient performance of the circuit by current limiting or shorting the load and measuring the peak input voltage transient.
- Place a 1  $\mu F$  ceramic capacitor as close as possible to VREF pin.
- Place a 1  $\mu F$  ceramic capacitor as close as possible to VDD pin.
- Minimize the inductance between the VIN and VIN\_K pins. There are anti-parallel diodes between these pins so any voltage greater than 0.3V in either polarity will cause significant current flow through the diodes, which can result in device failure. Do not place any resistors between these two nodes.
- Minimize the impedance between the VIN\_K and SENSE pins. There are anti-parallel diodes between these pins so any voltage greater than 0.3V in either polarity will cause significant current flow through the diodes, which can result in device failure.
- The sense resistor ( $R_S$ ) should be placed close to the LM5066. A trace should connect the VIN pad and  $Q_1$  pad of the sense resistor to VIN\_K and SENSE pins, respectively. Connect  $R_S$  using the Kelvin techniques shown in Figure 7.
- The high current path from the board's input to the load (via  $Q_1$ ), and the return path, should be parallel and close to each other to minimize loop inductance.

- The AGND and GND connections should be connected at the pins of the device. The ground connections for the various components around the LM5066 should be connected directly to each other, and to the LM5066's GND and AGND pin connection, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- Provide adequate thermal sinking for the series pass device ( $Q_1$ ) to help reduce stresses during turn-on and turn-off.
- The board's edge connector can be designed such that the LM5066 detects via the UVLO/EN pin that the board is being removed, and responds by turning off the load before the supply voltage is disconnected. For example, in Figure 17, the voltage at the UVLO/EN pin goes to ground before  $V_{IN}$  is removed from the LM5066 as a result of the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5066's VIN pin before the UVLO voltage is taken high, thereby allowing the LM5066 to turn on the output in a controlled fashion.



**Figure 17. Recommended Board Connector Design**

## PMBUS™ COMMAND SUPPORT

The device features an SMBus interface that allows the use of PMBus commands to set warn levels, error masks, and get telemetry on  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{IN}$ ,  $V_{AUX}$ , and  $P_{IN}$ . The supported PMBus commands are shown in [Table 1](#).

**Table 1. Supported PMBus Commands**

Code	Name	Function	R/W	Number Of Data Bytes	Default Value
01h	OPERATION	Retrieves or stores the operation status.	R/W	1	80h
03h	CLEAR_FAULTS	Clears the status registers and re-arms the Black Box registers for updating.	Send Byte	0	
19h	CAPABILITY	Retrieves the device capability.	R	1	B0h
43h	VOUT_UV_WARN_LIMIT	Retrieves or stores output under-voltage warn limit threshold.	R/W	2	0000h
4Fh	OT_FAULT_LIMIT	Retrieves or stores over temperature fault limit threshold.	R/W	2	0960h (150°C)
51h	OT_WARN_LIMIT	Retrieves or stores over temperature warn limit threshold.	R/W	2	07D0h (125°C)
57h	VIN_OV_WARN_LIMIT	Retrieves or stores input over-voltage warn limit threshold.	R/W	2	0FFFh
58h	VIN_UV_WARN_LIMIT	Retrieves or stores input under-voltage warn limit threshold.	R/W	2	0000h
78h	STATUS_BYTE	Retrieves information about the parts operating status.	R	1	49h
79h	STATUS_WORD	Retrieves information about the parts operating status.	R	2	3849h
7Ah	STATUS_VOUT	Retrieves information about output voltage status.	R	1	00h
7Ch	STATUS_INPUT	Retrieves information about input status.	R	1	10h
7Dh	STATUS_TEMPERATURE	Retrieves information about temperature status.	R	1	00h
7Eh	STATUS_CML	Retrieves information about communications status.	R	1	00h
80h	STATUS_MFR_SPECIFIC	Retrieves information about circuit breaker and MOSFET shorted status.	R	1	10h
88h	READ_VIN	Retrieves input voltage measurement.	R	2	0000h
8Bh	READ_VOUT	Retrieves output voltage measurement.	R	2	0000h
8Dh	READ_TEMPERATURE_1	Retrieves temperature measurement.	R	2	0190h
99h	MFR_ID	Retrieves manufacturer ID in ASCII characters (NSC).	R	3	4Eh 53h 43h
9Ah	MFR_MODEL	Retrieves Part number in ASCII characters. (LM5066\0\0).	R	8	4Ch 4Dh 35h 30h 36h 36h 0h 0h
9Bh	MFR_REVISION	Retrieves part revision letter/number in ASCII (for example, AA).	R	2	41h 41h
D0h	MFR_SPECIFIC_00 READ_VAUX	Retrieves auxiliary voltage measurement.	R	2	0000h
D1h	MFR_SPECIFIC_01 MFR_READ_IIN	Retrieves input current measurement.	R	2	0000h
D2h	MFR_SPECIFIC_02 MFR_READ_PIN	Retrieves input power measurement.	R	2	0000h
D3h	MFR_SPECIFIC_03 MFR_IIN_OC_WARN_LIMIT	Retrieves or stores input current limit warn threshold.	R/W	2	0FFFh
D4h	MFR_SPECIFIC_04 MFR_PIN_OP_WARN_LIMIT	Retrieves or stores input power limit warn threshold.	R/W	2	0FFFh
D5h	MFR_SPECIFIC_05 READ_PIN_PEAK	Retrieves measured peak input power measurement.	R	2	0000h

**Table 1. Supported PMBus Commands (continued)**

Code	Name	Function	R/W	Number Of Data Bytes	Default Value
D6h	MFR_SPECIFIC_06 CLEAR_PIN_PEAK	Resets the contents of the peak input power register to zero.	Send Byte	0	
D7h	MFR_SPECIFIC_07 GATE_MASK	Allows the user to disable MOSFET gate shutdown for various fault conditions.	R/W	1	0000h
D8h	MFR_SPECIFIC_08 ALERT_MASK	Retrieves or stores user $\overline{\text{SMBA}}$ fault mask.	R/W	2	0820h
D9h	MFR_SPECIFIC_09 DEVICE_SETUP	Retrieves or stores information about number of retry attempts.	R/W	1	0000h
DAh	MFR_SPECIFIC_10 BLOCK_READ	Retrieves most recent diagnostic and telemetry information in a single transaction.	R	12	0190h 0000h 0000h 0000h 0000h 0000h
DBh	MFR_SPECIFIC_11 SAMPLES_FOR_AVG	Exponent value AVGN for number of samples to be averaged ( $N = 2^{\text{AVGN}}$ ), range = 00h to 0Ch .	R/W	1	00h
DCh	MFR_SPECIFIC_12 READ_AVG_VIN	Retrieves averaged input voltage measurement.	R	2	0000h
DDh	MFR_SPECIFIC_13 READ_AVG_VOUT	Retrieves averaged output voltage measurement.	R	2	0000h
DEh	MFR_SPECIFIC_14 READ_AVG_IIN	Retrieves averaged input current measurement.	R	2	0000h
DFh	MFR_SPECIFIC_15 READ_AVG_PIN	Retrieves averaged input power measurement.	R	2	0000h
E0h	MFR_SPECIFIC_16 BLACK_BOX_READ	Captures diagnostic and telemetry information which are latched when the first $\overline{\text{SMBA}}$ event after faults are cleared.	R	12	0000h 0000h 0000h 0000h 0000h 0000h
E1h	MFR_SPECIFIC_17 DIAGNOSTIC_WORD_READ	Manufacturer-specific parallel of the STATUS_WORD to convey all FAULT/WARN data in a single transaction.	R	2	08E0h
E2h	MFR_SPECIFIC_18 AVG_BLOCK_READ	Retrieves most recent average telemetry and diagnostic information in a single transaction.	R	12	0000h 0000h 0000h 0000h 0000h 0000h



## STANDARD PMBUS COMMANDS

### OPERATION (01h)

The OPERATION command is a standard PMBus command that controls the MOSFET switch. This command may be used to switch the MOSFET ON and OFF under host control. It is also used to re-enable the MOSFET after a fault triggered shutdown. Writing an OFF command, followed by an ON command, will clear all faults and re-enable the device. Writing only an ON after a fault-triggered shutdown will not clear the fault registers or re-enable the device. The OPERATION command is issued with the write byte protocol.

**Table 2. Recognized OPERATION Command Values**

Value	Meaning	Default
80h	Switch ON	80h
00h	Switch OFF	n/a

### CLEAR FAULTS (03h)

The CLEAR\_FAULTS command is a standard PMBus command that resets all stored warning and fault flags and the SMBA signal. If a fault or warning condition still exists when the CLEAR\_FAULTS command is issued, the SMBA signal may not clear or will re-assert almost immediately. Issuing a CLEAR\_FAULTS command will not cause the MOSFET to switch back on in the event of a fault turnoff - that must be done by issuing an OPERATION command after the fault condition is cleared. This command uses the PMBus send byte protocol.

### CAPABILITY (19h)

The CAPABILITY command is a standard PMBus command that returns information about the PMBus functions supported by the LM5066. This command is read with the PMBus read byte protocol.

**Table 3. CAPABILITY Register**

Value	Meaning	Default
B0h	Supports Packet Error Check, 400Kbits/sec, Supports SMBus Alert	B0h

### VOUT\_UV\_WARN\_LIMIT (58h)

The VOUT\_UV\_WARN\_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VOUT Under-voltage Warning detection. Reading and writing to this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read or write word protocol. If the measured value of VOUT falls below the value in this register, VOUT UV Warn flags are set and the SMBA signal is asserted.

**Table 4. VOUT\_UV\_WARN\_LIMIT Register**

Value	Meaning	Default
1h – 0FFFh	VOUT Under-voltage Warning detection threshold	0000h (disabled)
0000h	VOUT Under-voltage Warning disabled	n/a

### OT\_FAULT\_LIMIT (4Fh)

The OT\_FAULT\_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the overtemperature fault detection. Reading and writing to this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read or write word protocol. If the measured temperature exceeds this value, an overtemperature fault is triggered and the MOSFET is switched off, OT FAULT flags set, and the SMBA signal asserted. After the measured temperature falls below the value in this register, the MOSFET may be switched back on with the OPERATION command. A single temperature measurement is an average of 16 round-robin cycles; therefore, the minimum temperature fault detection time is 16 ms.

**Table 5. OT\_FAULT\_LIMIT Register**

Value	Meaning	Default
0h – 0FFEh	Overtemperature Fault threshold value	0960h (150°C)
0FFFh	Overtemperature Fault detection disabled	n/a

**OT\_WARN\_LIMIT (51h)**

The OT\_WARN\_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the overtemperature warning detection. Reading and writing to this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read or write word protocol. If the measured temperature exceeds this value, an Overtemperature warning is triggered and the OT WARN flags set in the respective registers and the SMBA signal asserted. A single temperature measurement is an average of 16 round-robin cycles; therefore, the minimum temperature warn detection time is 16 ms.

**Table 6. OT\_WARN\_LIMIT Register**

Value	Meaning	Default
0h – 0FFEh	Overtemperature Warn Threshold Value	07D0h (125°C)
0FFFh	Overtemperature Warn detection disabled	n/a

**VIN\_OV\_WARN\_LIMIT (57h)**

The VIN\_OV\_WARN\_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VIN over-voltage warning detection. Reading and writing to this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read or write word protocol. If the measured value of VIN rises above the value in this register, VIN OV Warn flags are set in the respective registers and the SMBA signal is asserted.

**Table 7. VIN\_OV\_WARN\_LIMIT Register**

Value	Meaning	Default
0h – 0FFEh	VIN Over-voltage Warning detection threshold	0FFFh (disabled)
0FFFh	VIN Over-voltage Warning disabled	n/a

**VIN\_UV\_WARN\_LIMIT (58h)**

The VIN\_UV\_WARN\_LIMIT command is a standard PMBus command that allows configuring or reading the threshold for the VIN under-voltage warning detection. Reading and writing to this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read or write word protocol. If the measured value of VIN falls below the value in this register, VIN UV Warn flags are set in the respective register, and the SMBA signal is asserted.

**Table 8. VIN\_UV\_WARN\_LIMIT Register**

Value	Meaning	Default
1h – 0FFFh	VIN Under-voltage Warning detection threshold	0000h (disabled)
0000h	VIN Under-voltage Warning disabled	n/a

### STATUS\_BYTE (78h)

The STATUS\_BYTE is a standard PMBus command that returns the value of a number of flags indicating the state of the LM5066. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be removed on the system and a CLEAR\_FAULTS command issued.

**Table 9. STATUS\_BYTE Definitions**

Bit	NAME	Meaning	Default
7	BUSY	Not Supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason.	1
5	VOUT OV	Not Supported, always 0	0
4	IOUT OC	Not Supported, always 0	0
3	VIN UV Fault	A VIN Under-voltage Fault has occurred	1
2	TEMPERATURE	A Temperature Fault or Warning has occurred	0
1	CML	A Communication Fault has occurred	0
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred	1

### STATUS\_WORD (79h)

The STATUS\_WORD command is a standard PMBus command that returns the value of a number of flags indicating the state of the LM5066. Accesses to this command should use the PMBus read word protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR\_FAULTS command issued. The INPUT and VIN UV flags will default to 1 on startup, however, they will be cleared to 0 after the first time the input voltage exceeds the resistor-programmed UVLO threshold.

**Table 10. STATUS\_WORD Definitions**

Bit	NAME	Meaning	Default
15	VOUT	An output voltage fault or warning has occurred	0
14	IOUT/POUT	Not Supported, always 0	0
13	INPUT	An input voltage or current fault has occurred	1
12	MFR	A Manufacturer Specific Fault or Warning has occurred	1
11	POWER GOOD	The Power Good signal has been negated	1
10	FANS	Not Supported, always 0	0
9	OTHER	Not Supported, always 0	0
8	UNKNOWN	Not Supported, always 0	0
7	BUSY	Not Supported, always 0	0
6	OFF	This bit is asserted if the MOSFET is not switched on for any reason.	1
5	VOUT OV	Not Supported, always 0	0
4	IOUT OC	Not Supported, always 0	0
3	VIN UV	A VIN Under-voltage Fault has occurred	1
2	TEMPERATURE	A Temperature Fault or Warning has occurred	0
1	CML	A Communication Fault has occurred	0
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred	1

### STATUS\_VOUT (7Ah)

The STATUS\_VOUT command is a standard PMBus command that returns the value of the VOUT UV Warn flag. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR\_FAULTS command issued.

**Table 11. STATUS\_VOUT Definitions**

Bit	NAME	Meaning	Default
7	VOUT OV Fault	Not Supported, always 0	0
6	VOUT OV Warn	Not Supported, always 0	0
5	VOUT UV Warn	A VOUT Under-voltage Warning has occurred	0
4	VOUT UV Fault	Not Supported, always 0	0
3	VOUT Max	Not Supported, always 0	0
2	TON Max Fault	Not Supported, always 0	0
1	TOFF Max Fault	Not Supported, always 0	0
0	VOUT Tracking Error	Not Supported, always 0	0

### STATUS\_INPUT (7Ch)

The STATUS\_INPUT command is a standard PMBus command that returns the value of a number of flags related to input voltage, current, and power. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR\_FAULTS command issued. The VIN UV Warn flag will default to 1 on startup, however, it will be cleared to 0 after the first time the input voltage increases above the resistor-programmed UVLO threshold.

**Table 12. STATUS\_INPUT Definitions**

Bit	NAME	Meaning	Default
7	VIN OV Fault	A VIN Over-voltage Fault has occurred	0
6	VIN OV Warn	A VIN Over-voltage Warning has occurred	0
5	VIN UV Warn	A VIN Under-voltage Warning has occurred	1
4	VIN UV Fault	A VIN Under-voltage Fault has occurred	0
3	Insufficient Voltage	Not Supported, always 0	0
2	IIN OC Fault	An IIN Over-current Fault has occurred	0
1	IIN OC Warn	An IIN Over-current Warning has occurred	0
0	PIN OP Warn	A PIN Over-power Warning has occurred	0

### STATUS\_TEMPERATURE (7dh)

The STATUS\_TEMPERATURE is a standard PMBus command that returns the value of the of a number of flags related to the temperature telemetry value. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be cleared and a CLEAR\_FAULTS command issued.

**Table 13. STATUS\_TEMPERATURE Definitions**

Bit	NAME	Meaning	Default
7	Overtemp Fault	An Overtemperature Fault has occurred	0
6	Overtemp Warn	An Overtemperature Warning has occurred	0
5	Undertemp Warn	Not Supported, always 0	0
4	Undertemp Fault	Not Supported, always 0	0
3	reserved	Not Supported, always 0	0
2	reserved	Not Supported, always 0	0
1	reserved	Not Supported, always 0	0
0	reserved	Not Supported, always 0	0

### STATUS\_CML (7Eh)

The STATUS\_CML is a standard PMBus command that returns the value of a number of flags related to communication faults. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, a CLEAR\_FAULTS command should be issued.

**Table 14. STATUS\_CML Definitions**

Bit	NAME	Default
7	Invalid or unsupported command received	0
6	Invalid or unsupported data received	0
5	Packet Error Check failed	0
4	Not supported, always 0	0
3	Not supported, always 0	0
2	Not supported, always 0	0
1	Miscellaneous communications fault has occurred	0
0	Not supported, always 0	0

### STATUS\_MFR\_SPECIFIC (80h)

The STATUS\_MFR\_SPECIFIC command is a standard PMBus command that contains manufacturer specific status information. Accesses to this command should use the PMBus read byte protocol. To clear bits in this register, the underlying fault should be removed and a CLEAR\_FAULTS command should be issued.

**Table 15. STATUS\_MFR\_SPECIFIC Definitions**

Bit	Meaning	Default
7	Circuit breaker fault	0
6	Ext. MOSFET shorted fault	0
5	Not Supported, Always 0	0
4	Defaults loaded	1
3	Not supported: Always 0	0
2	Not supported: Always 0	0
1	Not supported: Always 0	0
0	Not supported: Always 0	0

### READ\_VIN (88h)

The READ\_VIN command is a standard PMBus command that returns the 12-bit measured value of the input voltage. Reading this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read word protocol. This value is also used internally for the VIN Over and Under Voltage Warning detection.

**Table 16. READ\_VIN Register**

Value	Meaning	Default
0h – 0FFFh	Measured value for VIN	0000h

### READ\_VOUT (8Bh)

The READ\_VOUT command is a standard PMBus command that returns the 12-bit measured value of the output voltage. Reading this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read word protocol. This value is also used internally for the VOUT Under Voltage Warning detection.

**Table 17. READ\_VOUT Register**

Value	Meaning	Default
0h – 0FFFh	Measured value for VOUT	0000h

### READ\_TEMPERATURE\_1 (8Dh)

The READ\_TEMPERATURE\_1 command is a standard PMBus command that returns the signed value of the temperature measured by the external temperature sense diode. Reading this register should use the coefficients shown in [Table 41](#). Accesses to this command should use the PMBus read word protocol. This value is also used internally for the Over Temperature Fault and Warning detection. This data has a range of -256°C to +255°C after the coefficients are applied.

**Table 18. READ\_TEMPERATURE\_1 Register**

Value	Meaning	Default
0h – 0FFFh	Measured value for TEMPERATURE	0000h

### MFR\_ID (99h)

The MFR\_ID command is a standard PMBus command that returns the identification of the manufacturer. To read the MFR\_ID, use the PMBus block read protocol.

**Table 19. MFR\_ID Register**

Byte	Name	Value
0	Number of bytes	03h
1	MFR ID-1	4Eh 'N'
2	MFR ID-2	53h 'S'
3	MFR ID-3	43h 'C'

### MFR\_MODEL (9Ah)

The MFR\_MODEL command is a standard PMBus command that returns the part number of the chip. To read the MFR\_MODEL, use the PMBus block read protocol.

**Table 20. MFR\_MODEL Register**

Byte	Name	Value
0	Number of bytes	08h
1	MFR ID-1	4Ch 'L'
2	MFR ID-2	4Dh 'M'
3	MFR ID-3	35h '5'
4	MFR ID-4	30h '0'
5	MFR ID-5	36h '6'
6	MFR ID-6	36h '6'
7	MFR ID-7	00h
8	MFR ID-8	00h

**MFR\_REVISION (9Bh)**

The MFR\_REVISION command is a standard PMBus command that returns the revision level of the part. To read the MFR\_REVISION, use the PMBus block read protocol.

**Table 21. MFR\_REVISION Register**

Byte	Name	Value
0	Number of bytes	02h
1	MFR ID-1	41h 'A'
2	MFR ID-2	41h 'A'

## MANUFACTURER SPECIFIC PMBUS™ COMMANDS

### MFR\_SPECIFIC\_00: READ\_VAUX (D0h)

The READ\_VAUX command will report the 12-bit ADC measured auxiliary voltage. Voltages greater than or equal to 2.97V to ground will be reported at plus full scale (0FFFh). Voltages less than or equal to 0V referenced to ground will be reported as 0 (0000h). To read data from the READ\_VAUX command, use the PMBus Read Word protocol.

**Table 22. READ\_VAUX Register**

Value	Meaning	Default
0h – 0FFFh	Measured value for VAUX input	0000h

### MFR\_SPECIFIC\_01: MFR\_READ\_IIN (D1h)

The MFR\_READ\_IIN command will report the 12-bit ADC measured current sense voltage. To read data from the MFR\_READ\_IIN command, use the PMBus Read Word protocol. Reading this register should use the coefficients shown in [Table 41](#). Please see the section on coefficient calculations to calculate the values to use.

**Table 23. MFR\_READ\_IIN Register**

Value	Meaning	Default
0h – 0FFFh	Measured value for input current sense voltage	0000h

### MFR\_SPECIFIC\_02: MFR\_READ\_PIN (D2h)

The MFR\_READ\_PIN command will report the upper 12 bits of the VIN x IIN product as measured by the 12-bit ADC. To read data from the MFR\_READ\_PIN command, use the PMBus Read Word protocol. Reading this register should use the coefficients shown in [Table 41](#). Please see the section on coefficient calculations to calculate the values to use.

**Table 24. MFR\_READ\_PIN Register**

Value	Meaning	Default
0h – 0FFFh	Value for input current x input voltage	0000h

### MFR\_SPECIFIC\_03: MFR\_IN\_OC\_WARN\_LIMIT (D3h)

The MFR\_IIN\_OC\_WARN\_LIMIT PMBus command sets the input over-current warning threshold. In the event that the input current rises above the value set in this register, the IIN Over-current flags are set in the respective registers and the  $\overline{SMBA}$  is asserted. To access the MFR\_IIN\_OC\_WARN\_LIMIT register, use the PMBus Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in [Table 41](#).

**Table 25. MFR\_IIN\_OC\_WARN\_LIMIT Register**

Value	Meaning	Default
0h – 0FFEh	Value for input over-current warn limit	0FFFh
0FFFh	Input over-current warning disabled	n/a



**MFR\_SPECIFIC\_04: MFR\_PIN\_OP\_WARN\_LIMIT (D4h)**

The MFR\_PIN\_OP\_WARN\_LIMIT PMBus command sets the input over-power warning threshold. In the event that the input power rises above the value set in this register, the PIN Over-power flags are set in the respective registers and the SMBA is asserted. To access the MFR\_PIN\_OP\_WARN\_LIMIT register, use the PMBus Read/Write Word protocol. Reading/writing to this register should use the coefficients shown in [Table 41](#).

**Table 26. MFR\_PIN\_OPWARN\_LIMIT Register**

Value	Meaning	Default
0h – 0FFEh	Value for input over power warn limit	0FFFh
0FFFh	Input over power warning disabled	n/a

**MFR\_SPECIFIC\_05: READ\_PIN\_PEAK (D5h)**

The READ\_PIN\_PEAK command will report the maximum input power measured since a Power On reset or the last CLEAR\_PIN\_PEAK command. To access the READ\_PIN\_PEAK command, use the PMBus Read Word protocol. Use the coefficients shown in [Table 41](#).

**Table 27. READ\_PIN\_PEAK Register**

Value	Meaning	Default
0h – 0FFEh	Maximum Value for input current x input voltage since reset or last clear	0h

**MFR\_SPECIFIC\_06: CLEAR\_PIN\_PEAK (D6h)**

The CLEAR\_PIN\_PEAK command will clear the PIN PEAK register. This command uses the PMBus Send Byte protocol.

**MFR\_SPECIFIC\_07: GATE\_MASK (D7h)**

The GATE\_MASK register allows the hardware to prevent fault conditions from switching off the MOSFET. When the bit is high, the corresponding FAULT has no control over the MOSFET gate. All status registers will still be updated (STATUS, DIAGNOSTIC) and an SMBA will still be asserted. This register is accessed with the PMBus Read / Write Byte protocol.

The IIN/PFET Fault refers to the input current fault and the MOSFET power dissipation fault. There is no input power fault detection; only input power warning detection.

**WARNING**

**Inhibiting the MOSFET switch off in response to over-current or circuit breaker fault conditions will likely result in the destruction of the MOSFET! This functionality should be used with great care and supervision!**

**Table 28. MFR\_SPECIFIC\_07 GATE MASK Definitions**

Bit	NAME	Default
7	Not used, always 0	0
6	Not used, always 0	0
5	VIN UV FAULT	0
4	VIN OV FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMP FAULT	0
1	Not used, always 0	0
0	CIRCUIT BREAKER FAULT	0

**MFR\_SPECIFIC\_08: ALERT\_MASK (D8h)**

The ALERT\_MASK command is used to mask the  $\overline{\text{SMBA}}$  when a specific fault or warning has occurred. Each bit corresponds to one of the 14 different analog and digital faults or warnings that would normally result in an SMBA being asserted. When the corresponding bit is high, that condition will not cause the SMBA to be asserted. If that condition occurs, the registers where that condition is captured will still be updated (STATUS registers, DIAGNOSTIC\_WORD) and the external MOSFET gate control will still be active (VIN\_OV\_FAULT, VIN\_UV\_FAULT, IIN/PFET\_FAULT, CB\_FAULT, OT\_FAULT). This register is accessed with the PMBus Read / Write Word protocol. The VIN UNDERVOLTAGE FAULT flag will default to 1 on startup, however, it will be cleared to 0 after the first time the input voltage increases above the resistor-programmed UVLO threshold.

**Table 29. ALERT\_MASK Definitions**

BIT	NAME	DEFAULT
15	VOUT UNDERVOLTAGE WARN	0
14	IIN LIMIT Warn	0
13	VIN UNDERVOLTAGE WARN	0
12	VIN OVERVOLTAGE WARN	0
11	$\overline{\text{POWER GOOD}}$	1
10	OVERTEMP WARN	0
9	Not Used	0
8	OVERPOWER LIMIT WARN	0
7	Not Used	0
6	EXT_MOSFET_SHORTED	0
5	VIN UNDERVOLTAGE FAULT	1
4	VIN OVERVOLTAGE FAULT	0
3	IIN/PFET FAULT	0
2	OVERTEMPERATURE FAULT	0
1	CML FAULT (Communications Fault)	0
0	CIRCUIT BREAKER FAULT	0

**MFR\_SPECIFIC\_09: DEVICE\_SETUP (D9h)**

The DEVICE\_SETUP command may be used to override pin settings to define operation of the LM5066 under host control. This command is accessed with the PMBus read / write byte protocol.

**Table 30. DEVICE\_SETUP Byte Format**

Bit	Name	Meaning
7:5	Retry setting	111 = Unlimited retries
		110 = Retry 16 times
		101 = Retry 8 times
		100 = Retry 4 times
		011 = Retry 2 times
		010 = Retry 1 time
		001 = No retries
		000 = Pin configured retries
4	Current limit setting	0 = High setting (50mV)
		1 = Low setting (26mV)
3	CB/CL Ratio	0 = Low setting (1.9x)
		1 = High setting (3.9x)
2	Current Limit Configuration	0 = Use pin settings
		1 = Use SMBus settings
1	Unused	

**Table 30. DEVICE\_SETUP Byte Format (continued)**

Bit	Name	Meaning
0	Unused	

In order to configure the Current Limit Setting via this register, it is necessary to set the Current Limit Configuration bit (2) to 1 to enable the register to control the current limit function and the Current Limit Setting bit (4) to select the desired setting. If the Current Limit Configuration bit is not set, the pin setting will be used. The Circuit Breaker to Current Limit ratio value is set by the CB / CL Ratio bit (3). Note that if the Current Limit Configuration is changed, the samples for the telemetry averaging function will not be reset. It is recommended to allow a full averaging update period with the new Current Limit Configuration before processing the averaged data.

Note that the Current Limit Configuration affects the coefficients used for the Current and Power measurements and warning registers.

**MFR\_SPECIFIC\_10: BLOCK\_READ (DAh)**

The BLOCK\_READ command concatenates the DIAGNOSTIC\_WORD with input and output telemetry information (IIN, VOUT, VIN, PIN) as well as TEMPERATURE to capture all of the operating information of the LM5066 in a single SMBus transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ\_XXX command had been issued (shown below). The contents of the block read register are updated every clock cycle (85ns) as long as the SMBus interface is idle. BLOCK\_READ also specifies that the VIN, VOUT, IIN and PIN measurements are all time-aligned. If separate commands are used, individual samples may not be time-aligned, because of the delay necessary for the communication protocol.

The Block Read command is read via the PMBus block read protocol.

**Table 31. BLOCK\_READ Register Format**

Byte Count (always 12)	(1 byte)
DIAGNOSTIC_WORD	(1 Word)
IIN_BLOCK	(1 Word)
VOUT_BLOCK	(1 Word)
VIN_BLOCK	(1 Word)
PIN_BLOCK	(1 Word)
TEMP_BLOCK	(1 Word)

**MFR\_SPECIFIC\_11: SAMPLES\_FOR\_AVG (DBh)**

The SAMPLES\_FOR\_AVG command is a manufacturer specific command for setting the number of samples used in computing the average values for IIN, VIN, VOUT, PIN. The decimal equivalent of the AVGN nibble is the power of 2 samples, (for example, AVGN=12 equates to N=4096 samples used in computing the average). The LM5066 supports average numbers of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096. The SAMPLES\_FOR\_AVG number applies to average values of IIN, VIN, VOUT, PIN simultaneously. The LM5066 uses simple averaging. This is accomplished by summing consecutive results up to the number programmed, then dividing by the number of samples. Averaging is calculated according to the following sequence:

$$Y = (X_{(N)} + X_{(N-1)} + \dots + X_{(0)}) / N \quad (36)$$

When the averaging has reached the end of a sequence (for example, 4096 samples are averaged), then a whole new sequence begins that will require the same number of samples (in this example, 4096) to be taken before the new average is ready.

**Table 32. SAMPLES\_FOR\_AVG Register**

AVGN	N = 2 <sup>AVGN</sup>	Averaging/Register Update Period (ms)
0000	1	1
0001	2	2
0010	4	4

**Table 32. SAMPLES\_FOR\_AVG Register (continued)**

AVGN	$N = 2^{AVGN}$	Averaging/Register Update Period (ms)
0011	8	8
0100	16	16
0101	32	32
0110	64	64
0111	128	128
1000	256	256
1001	512	512
1010	1024	1024
1011	2048	2048
1100	4096	4096

Note that a change in the SAMPLES\_FOR\_AVG register will not be reflected in the average telemetry measurements until the present averaging interval has completed. The default setting for AVGN is 0000, therefore, the average telemetry will mirror the instantaneous telemetry until a value higher than zero is programmed.

The SAMPLES\_FOR\_AVG register is accessed via the PMBus read / write byte protocol.

**Table 33. SAMPLES\_FOR\_AVG Register**

Value	Meaning	Default
0h – 0Ch	Exponent (AVGN) for number of samples to average over	00h

**MFR\_SPECIFIC\_12: READ\_AVG\_VIN (DCh)**

The READ\_AVG\_VIN command will report the 12-bit ADC measured input average voltage. If the data is not ready, the returned value will be the previous averaged data. However, if there is no previously averaged data, the default value (0000h) will be returned. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in [Table 41](#).

**Table 34. READ\_AVG\_VIN Register**

Value	Meaning	Default
0h – 0FFFh	Average of measured values for input voltage	0000h

**MFR\_SPECIFIC\_13: READ\_AVG\_VOUT (DDh)**

The READ\_AVG\_VOUT command will report the 12-bit ADC measured current sense average voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in [Table 41](#).

**Table 35. READ\_AVG\_VOUT Register**

Value	Meaning	Default
0h – 0FFFh	Average of measured values for output voltage	0000h

**MFR\_SPECIFIC\_14: READ\_AVG\_IIN (DEh)**

The READ\_AVG\_IIN command will report the 12-bit ADC measured current sense average voltage. The returned value will be the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in [Table 41](#).

**Table 36. READ\_AVG\_IIN Register**

Value	Meaning	Default
0h – 0FFFh	Average of measured values for current sense voltage	0000h

**MFR\_SPECIFIC\_15: READ\_AVG\_PIN**

The READ\_AVG\_PIN command will report the upper 12-bits of the average VIN x IIN product as measured by the 12-bit ADC. You will read the default value (0000h) or previous data when the average data is not ready. This data is read with the PMBus Read Word protocol. This register should use the coefficients shown in [Table 41](#).

**Table 37. READ\_AVG\_PIN Register**

Value	Meaning	Default
0h – 0FFFh	Average of measured value for input voltage x input current sense voltage	0000h

**MFR\_SPECIFIC\_16: BLACK\_BOX\_READ (E0h)**

The BLACK BOX READ command retrieves the BLOCK READ data which was latched in at the first assertion of SMBA by the LM5066. It is re-armed with the CLEAR\_FAULTS command. It is the same format as the BLOCK\_READ registers, the only difference being that its contents are updated with the SMBA edge rather than the internal clock edge. This command is read with the PMBus Block Read protocol.

**MFR\_SPECIFIC\_17: READ\_DIAGNOSTIC\_WORD (E1h)**

The READ\_DIAGNOSTIC\_WORD PMBus command will report all of the LM5066 faults and warnings in a single read operation. The standard response to the assertion of the SMBA signal of issuing multiple read requests to various status registers can be replaced by a single word read to the DIAGNOSTIC\_WORD register. The READ\_DIAGNOSTIC\_WORD command should be read with the PMBus Read Word protocol. The READ\_DIAGNOSTIC\_WORD is also returned in the BLOCK\_READ, BLACK\_BOX\_READ, and AVG\_BLOCK\_READ operations.

**Table 38. DIAGNOSTIC\_WORD Format**

Bit	Meaning	Default
15	VOUT_UNDERVOLTAGE_WARN	0
14	IIN_OP_WARN	0
13	VIN_UNDERVOLTAGE_WARN	0
12	VIN_OVERVOLTAGE_WARN	0
11	POWER_GOOD	1
10	OVER_TEMPERATURE_WARN	0
9	TIMER_LATCHED_OFF	0
8	EXT_MOSFET_SHORTED	0
7	CONFIG_PRESET	1
6	DEVICE_OFF	1
5	VIN_UNDERVOLTAGE_FAULT	1
4	VIN_OVERVOLTAGE_FAULT	0
3	IIN_OC/PFET_OP_FAULT	0
2	OVER_TEMPERATURE_FAULT	0
1	CML_FAULT	0
0	CIRCUIT_BREAKER_FAULT	0

### MFR\_SPECIFIC\_18: AVG\_BLOCK\_READ (E2h)

The AVG\_BLOCK\_READ command concatenates the DIAGNOSTIC\_WORD with input and output average telemetry information (IIN, VOUT, VIN, PIN) as well as temperature to capture all of the operating information of the part in a single PMBus transaction. The block is 12 bytes long with telemetry information being sent out in the same manner as if an individual READ\_AVG\_XXX command had been issued (shown below). AVG\_BLOCK\_READ also specifies that the VIN, VOUT, and IIN measurements are all time-aligned whereas there is a chance they may not be if read with individual PMBus commands. To read data from the AVG\_BLOCK\_READ command, use the SMBus Block Read protocol.

**Table 39. AVG\_BLOCK\_READ Register Format**

Byte Count (always 12)	(1 byte)
DIAGNOSTIC_WORD	(1 word)
AVG_IIN	(1 word)
AVG_VOUT	(1 word)
AVG_VIN	(1 word)
AVG_PIN	(1 word)
TEMPERATURE	(1 word)

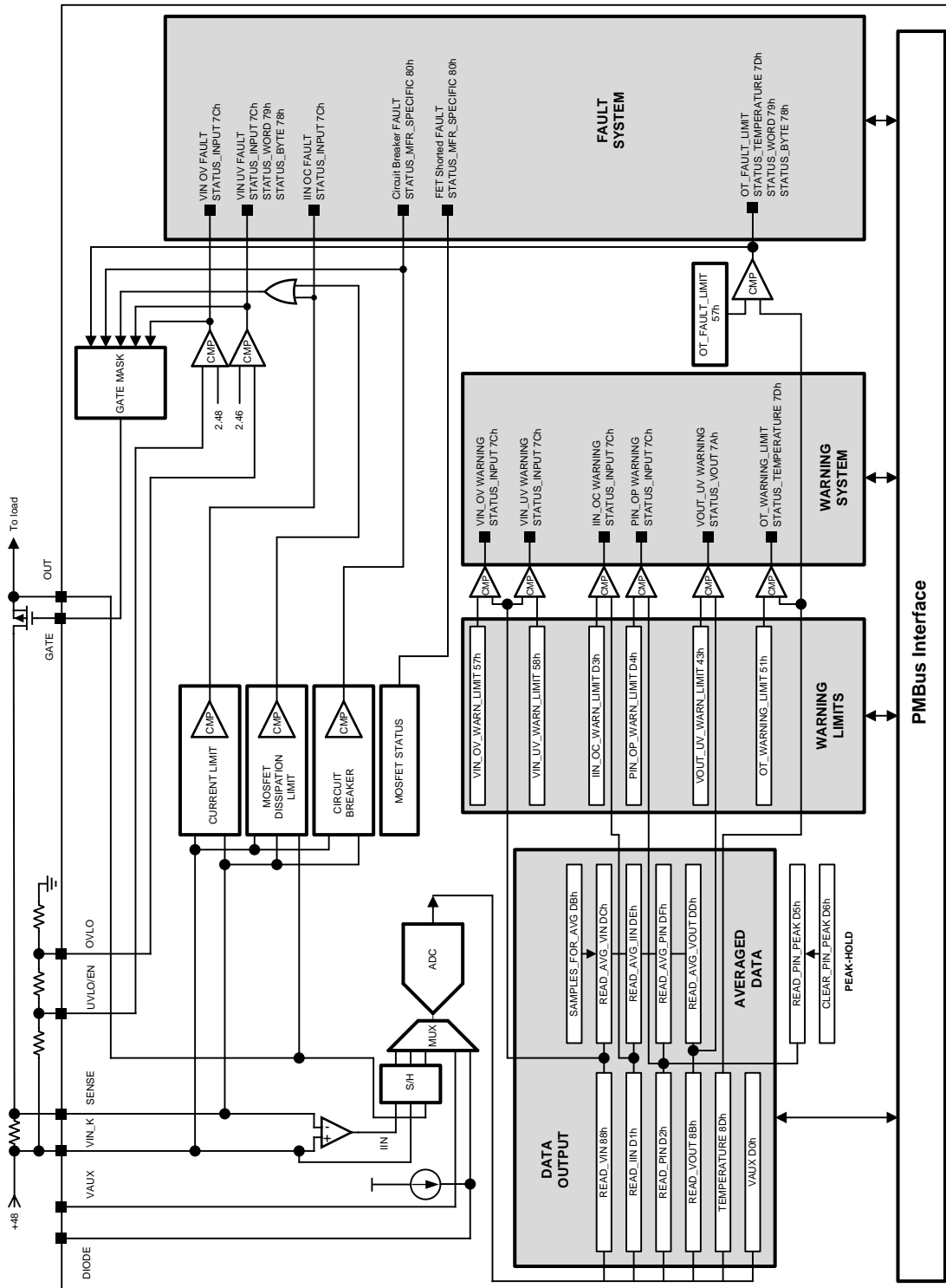


Figure 18. Command/Register and Alert Flow Diagram

## READING AND WRITING TELEMETRY DATA AND WARNING THRESHOLDS

All measured telemetry data and user programmed warning thresholds are communicated in 12-bit two's complement binary numbers read/written in 2 byte increments conforming to the Direct format as described in section 8.3.3 of the PMBus Power System Management Protocol Specification 1.1 (Part II). The organization of the bits in the telemetry or warning word is shown in [Table 40](#), where Bit\_11 is the most significant bit (MSB) and Bit\_0 is the least significant bit (LSB). The decimal equivalent of all warning and telemetry words are constrained to be within the range of 0 to 4095, with the exception of temperature. The decimal equivalent value of the temperature word ranges from 0 to 65535.

**Table 40. Telemetry and Warning Word Format**

Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Bit_7	Bit_6	Bit_5	Bit_4	Bit_3	Bit_2	Bit_1	Bit_0
2	0	0	0	0	Bit_11	Bit_10	Bit_9	Bit_8

Conversion from direct format to real-world dimensions of current, voltage, power, and temperature is accomplished by determining appropriate coefficients as described in section 7.2.1 of the PMBus Power System Management Protocol Specification 1.1 (Part II). According to this specification, the host system converts the values received into a reading of volts, amperes, watts, or other units using the following relationship:

$$X = \frac{1}{m} (Y \times 10^R - b) \quad (37)$$

Where:

**X:** the calculated "real-world" value (volts, amps, watt, etc.)

**m:** the slope coefficient

**Y:** a two byte two's complement integer received from device

**b:** the offset, a two byte, two's complement integer

**R:** the exponent, a one byte two's complement integer

R is only necessary in systems where m is required to be an integer (for example, where m may be stored in a register in an integrated circuit). In those cases, R only needs to be large enough to yield the desired accuracy.

**Table 41. Telemetry and Warning Conversion Coefficients**

Commands	Condition	Format	Number of Data Bytes	m	b	R	Units
READ_VIN, READ_AVG_VIN VIN_OV_WARN_LIMIT VIN_UV_WARN_LIMIT		DIRECT	2	4587	-1200	-2	V
READ_VOUT, READ_AVG_VOUT VOUT_UV_WARN_LIMIT		DIRECT	2	4587	-2400	-2	V
READ_VAUX		DIRECT	2	13793	0	-1	V
<sup>(1)</sup> READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	10753	-1200	-2	A
<sup>(1)</sup> READ_IN, READ_AVG_IN MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	5405	-600	-2	A
<sup>(1)</sup> READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	1204	-6000	-3	W
<sup>(1)</sup> READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	605	-8000	-3	W
READ_TEMPERATURE_1 OT_WARN_LIMIT OT_FAULT_LIMIT		DIRECT	2	16000	0	-3	°C

(1) The coefficients relating to current/power measurements and warning thresholds shown are normalized to a sense resistor ( $R_S$ ) value of 1mΩ. In general, the current/power coefficients can be calculated using the relationships shown in [Table 42](#).



**Table 42. Current and Power Telemetry and Warning Conversion Coefficients ( $R_S$  in  $m\Omega$ )**

Commands	Condition	Format	Number of Data Bytes	m	b	R	Units
<sup>(1)</sup> READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = VDD	DIRECT	2	$10753 \times R_S$	-1200	-2	A
<sup>(1)</sup> READ_IIN, READ_AVG_IIN MFR_IIN_OC_WARN_LIMIT	CL = GND	DIRECT	2	$5405 \times R_S$	-600	-2	A
<sup>(1)</sup> READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = VDD	DIRECT	2	$1204 \times R_S$	-6000	-3	W
<sup>(1)</sup> READ_PIN, READ_AVG_PIN, READ_PIN_PEAK MFR_PIN_OP_WARN_LIMIT	CL = GND	DIRECT	2	$605 \times R_S$	-8000	-3	W

(1) The coefficients relating to current/power measurements and warning thresholds shown in [Table 41](#) are normalized to a sense resistor ( $R_S$ ) value of  $1m\Omega$ . In general, the current/power coefficients can be calculated using the relationships shown.

Care must be taken to adjust the exponent coefficient, R, such that the value of m remains within the range of -32768 to +32767. For example, if a  $5m\Omega$  sense resistor is used, the correct coefficients for the READ\_IIN command with CL = VDD would be  $m = 5359$ ,  $b = -120$ ,  $R = -1$ .

#### A Note on the "b" Coefficient

Since b coefficients represent offset, for simplification b is set to zero in the following discussions.

## READING CURRENT

The current register actually displays a value equivalent to a voltage across the user specified sense resistor,  $R_S$ . The coefficients enable the data output to be converted to amps. The values shown in the example are based on having the device programmed for a 26 mV current limit threshold ( $CL = VDD$ ). In the 26mV range, the LSB value is 9.3  $\mu$ V and the full scale range is 38.0 mV. In the 50mV range ( $CL = GND$ ), the LSB value is 18.5  $\mu$ V and the full scale range in 76.0 mV.

Step	Example
1. Determine full scale current and shunt value based on 38.0 mV across shunt at full scale: $I_{IN\_MAX} = \frac{38.0 \text{ mV}}{R_S} \quad (38)$ or:	Example: 8.6A application with 3 m $\Omega$ shunt. $I_{IN\_MAX} = \frac{38.0 \text{ mV}}{3 \text{ m}\Omega} = 12.667 \quad (39)$
2. Determine m': $m' = \frac{4095}{I_{IN\_MAX}} \quad (40)$	$m' = \frac{4095}{12.667} = 323.3 \quad (41)$
3. Determine exponent R necessary to set m' to integer value m: $10^R = \frac{m'}{m} \quad (42)$	Select R to provide 16 bit accuracy for the integer value of m: $R = \log_{10}\left(\frac{323.3}{3233}\right) \quad (43)$ R = -1
4. Final values	m = 3233 R = -1 b = 0

## READING INPUT AND OUTPUT VOLTAGE

Coefficients for VIN and VOUT are fixed and are consistent between read telemetry measurements (for example, READ\_VIN, READ\_AVG\_VIN) and warning thresholds (for example, VIN\_UV\_WARN\_LIMIT). Input and output voltage values are read/written in Direct format with 12-bit resolution and a 21.8 mV LSB. An example of calculating the PMBus coefficients for input voltage is shown below.

Step	Example
1. Determine m' based on full scale analog input and full scale digital range: $m' = \frac{4095}{V_{IN\_MAX}} = \frac{4095}{89.3V} \quad (44)$	$m' = \frac{4095}{89.3V} = 45.86 \quad (45)$
2. Determine exponent R necessary to set m' to integer value m with desired accuracy: $10^R = \frac{m'}{m} \quad (46)$	Select R to provide 16 bit accuracy for the integer value of m: (4585 in this example): $R = \log_{10}\left(\frac{45.86}{4586}\right) \quad (47)$ R = -2
3. Final values	m = 4586 R = -2 b = 0

## READING POWER

The power calculation of the LM5066 is a relative power calculation meaning that full scale of the power register corresponds to simultaneous full scale values in the current register and voltage register such that the power register has the following relationship based on decimal equivalents of the register contents:

$$PIN = \frac{IIN \times VIN}{4096} \quad (48)$$

For this reason power coefficients will also vary depending on the shunt value and must be calculated for each application. The power LSB will vary depending on shunt value according to 828  $\mu$ W/Rsense for the 26mV range or 1.65 mW/Rsense for the 50mV range.

Step	Example
1. Determine full scale power from known full scale of input current and input voltage: $P_{IN\_MAX} = V_{IN\_MAX} \times I_{IN\_MAX}$	Example: 8.6A application with 3 m $\Omega$ shunt. $P_{IN\_MAX} = (89.3V) \times (76 \text{ mV} / 3 \text{ m}\Omega) = 2262W$
2. Determine m': $m' = \frac{4095}{P_{MAX}} \quad (49)$	$m' = \frac{4095}{2262W} = 1.8103 \quad (50)$
3. Optional: Determine exponent R necessary to set m' to integer value m with desired accuracy: $10^R = \frac{m'}{m} \quad (51)$	Select R to provide 16 bit accuracy for the integer value of m : $R = \log_{10} \frac{1.8103}{18103} \quad (52)$ R = -4
4. Final values	m = 18103 R = -4 b = 0

## DETERMINING TELEMETRY COEFFICIENTS EMPIRICALLY WITH LINEAR FIT

The coefficients for telemetry measurements and warning thresholds presented in [Table 41](#) are adequate for the majority of applications. Current and power coefficients must be calculated per application as they are dependent on the value of the sense resistor,  $R_S$ , used. [Table 42](#) provides the equations necessary for calculating the current and power coefficients for the general case. The small signal nature of the current measurement make it and the power measurement more susceptible to PCB parasitics than other telemetry channels. This may cause slight variations in the optimum coefficients ( $m$ ,  $b$ ,  $R$ ) for converting from Direct format digital values to real-world values (for example, Amps and Watts). The optimum coefficients can be determined empirically for a specific application and PCB layout using two or more measurements of the telemetry channel of interest. The current coefficients can be determined using the following method:

1. While the LM5066 is in normal operation measure the voltage across the sense resistor using kelvin test points and a high accuracy DVM while controlling the load current. Record the integer value returned by the READ\_AVG\_IIN command (with the SAMPLES\_FOR\_AVG set to a value greater than 0) for two or more voltages across the sense resistor. For best results, the individual READ\_AVG\_IIN measurements should span nearly the full scale range of the current (For example, voltage across  $R_S$  of 5mV and 20mV).
2. Convert the measured voltages to currents by dividing them by the value of  $R_S$ . For best accuracy the value of  $R_S$  should be measured. [Table 43](#) assumes a sense resistor value of 5m $\Omega$ .

**Table 43. Measurements for linear fit determination of current coefficients:**

Measured voltage across $R_S$ (V)	Measured Current (A)	READ_AVG_IIN (integer value)
0.005	1	568
0.01	2	1108
0.02	4	2185

1. Using the spreadsheet or math program of your choice determine the slope and the y-intercept of the data returned by the READ\_AVG\_IIN command versus the measured current. For the data shown in [Table 42](#):
  - READ\_AVG\_IN value = slope x (Measured Current) + (y-intercept)
  - slope = 538.9
  - y-intercept = 29.5
2. To determine the 'm' coefficient, simply shift the decimal point of the calculated slope to arrive at an integer with a suitable number of significant digits for accuracy (typically 4) while staying with the range of -32768 to +32767. This shift in the decimal point equates to the 'R' coefficient. For the slope value shown above, the decimal point would be shifted to the right once hence  $R = -1$ .
3. Once the 'R' coefficient has been determined, the 'b' coefficient is found by multiplying the y-intercept by  $10^{-R}$ . In this case the value of  $b = 295$ .
  - Calculated Current Coefficients:
  - $m = 5389$
  - $b = 295$
  - $R = -1$

$$X = \frac{1}{m} (Y \times 10^{-R} - b)$$

(53)

Where:

**X:** the calculated "real-world" value (volts, amps, watts, temperature)

**m:** the slope coefficient, is the two byte, two's complement integer

**Y:** a two byte two's complement integer received from device

**b:** the offset, a two byte, two's complement integer

**R:** the exponent, a one byte two's complement integer

The above procedure can be repeated to determine the coefficients of any telemetry channel simply by substituting measured current for some other parameter (for example, power, voltage, etc.).

## WRITING TELEMETRY DATA

There are several locations that will require writing data if their optional usage is desired. Use the same coefficients previously calculated for your application, and apply them using this method as prescribed by the PMBus revision section 7.2.2 "Sending a Value"

$$Y = (mX + b) \times 10^R \quad (54)$$

Where:

**X**: the calculated "real-world" value (volts, amps, watts, temperature)

**m**: the slope coefficient, is the two byte, two's complement integer

**Y**: a two byte two's complement integer received from device

**b**: the offset, a two byte, two's complement integer

**R**: the exponent, a one byte two's complement integer

### PMBUS™ ADDRESS LINES (ADR0, ADR1, ADR2)

The three address lines are to be set high (connect to VDD), low (connect to GND), or open to select one of 27 addresses for communicating with the LM5066. [Table 44](#) depicts 7-bit addresses (eighth bit is read/write bit):

**Table 44. Device Addressing**

ADR2	ADR1	ADR0	Decoded Address
Z	Z	Z	40h
Z	Z	0	41h
Z	Z	1	42h
Z	0	Z	43h
Z	0	0	44h
Z	0	1	45h
Z	1	Z	46h
Z	1	0	47h
Z	1	1	10h
0	Z	Z	11h
0	Z	0	12h
0	Z	1	13h
0	0	Z	14h
0	0	0	15h
0	0	1	16h
0	1	Z	17h
0	1	0	50h
0	1	1	51h
1	Z	Z	52h
1	Z	0	53h
1	Z	1	54h
1	0	Z	55h
1	0	0	56h
1	0	1	57h
1	1	Z	58h
1	1	0	59h
1	1	1	5Ah

SMBUS COMMUNICATIONS TIMING REQUIREMENTS

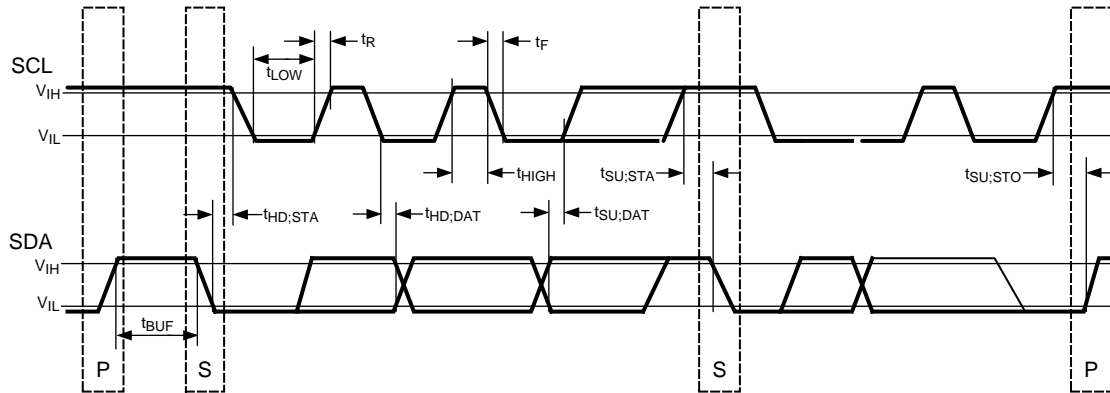


Figure 19. SMBus Timing Diagram

Table 45. SMBus Timing Definition

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
$F_{SMB}$	SMBus Operating Frequency	10	400	kHz	
$T_{BUF}$	Bus free time between Stop and Start Condition	1.3		$\mu s$	
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		$\mu s$	
$T_{SU:STA}$	Repeated Start Condition setup time	0.6		$\mu s$	
$T_{SU:STO}$	Stop Condition setup time	0.6		$\mu s$	
$T_{HD:DAT}$	Data hold time	85		ns	
$T_{SU:DAT}$	Data setup time	100		ns	
$T_{TIMEOUT}$	Clock low time-out	25	35	ms	(1)
$T_{LOW}$	Clock low period	1.5		$\mu s$	
$T_{HIGH}$	Clock high period	0.6		$\mu s$	(2)
$T_{LOW:SEXT}$	Cumulative clock low extend time (slave device)		25	ms	(3)
$T_{LOW:MEXT}$	Cumulative low extend time (master device)		10	ms	(4)
$T_F$	Clock or Data Fall Time	20	300	ns	(5)
$T_R$	Clock or Data Rise Time	20	300	ns	(5)

- (1) Devices participating in a transfer will timeout when any clock low exceeds the value of  $T_{TIMEOUT,MIN}$  of 25 ms. Devices that have detected a timeout condition must reset the communication no later than  $T_{TIMEOUT,MAX}$  of 35 ms. The maximum value must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master (10ms) and a slave (25ms).
- (2)  $T_{HIGH,MAX}$  provides a simple method for devices to detect bus idle conditions.
- (3)  $T_{LOW:SEXT}$  is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave exceeds this time, it is expected to release both its clock and data lines and reset itself.
- (4)  $T_{LOW:MEXT}$  is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
- (5) Rise and fall time is defined as follows: •  $T_R = (V_{ILMAX} - 0.15) \text{ to } (V_{IHMIN} + 0.15)$  •  $T_F = 0.9 VDD \text{ to } (V_{ILMAX} - 0.15)$

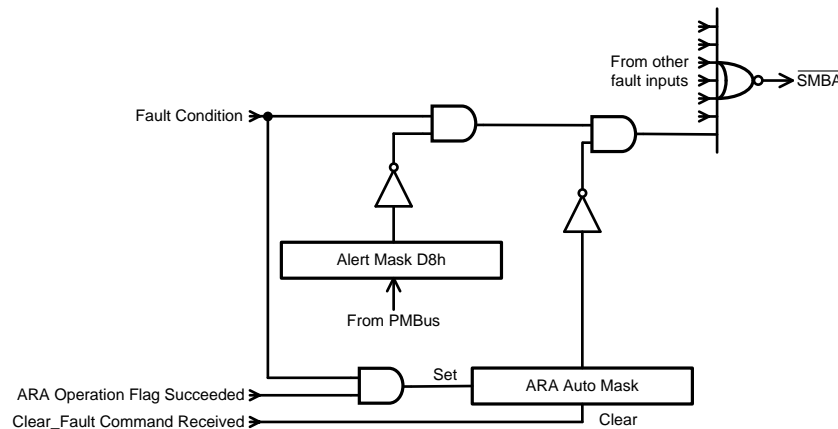
## SMBA RESPONSE

The  $\overline{\text{SMBA}}$  effectively has two masks:

1. The Alert Mask Register at D8h, and
2. The ARA Automatic Mask.

The ARA Automatic Mask is a mask that is set in response to a successful ARA read. An ARA read operation returns the PMBus address of the lowest addressed part on the bus that has its  $\overline{\text{SMBA}}$  asserted. A successful ARA read means that THIS part was the one that returned its address. When a part responds to the ARA read, it releases the  $\overline{\text{SMBA}}$  signal. When the last part on the bus that has an  $\overline{\text{SMBA}}$  set has successfully reported its address, the  $\overline{\text{SMBA}}$  signal will de-assert.

The way that the LM5066 releases the  $\overline{\text{SMBA}}$  signal is by setting the ARA Automatic mask bit for all fault conditions present at the time of the ARA read. All status registers will still show the fault condition, but it will not generate and  $\overline{\text{SMBA}}$  on that fault again until the ARA Automatic mask is cleared by the host issuing a CLEAR\_FAULTS command to this part. This should be done as a routine part of servicing an  $\overline{\text{SMBA}}$  condition on a part, even if the ARA read is not done. Figure 20 depicts a schematic version of this flow.



**Figure 20. Typical Flow Schematic for  $\overline{\text{SMBA}}$  Fault**



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**REVISION HISTORY**

<b>Changes from Revision F (February 2013) to Revision G</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">56</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5066PMH/NOPB	ACTIVE	HTSSOP	PWP	28	48	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM5066PMH	<a href="#">Samples</a>
LM5066PMHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM5066PMH	<a href="#">Samples</a>
LM5066PMHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	LM5066PMH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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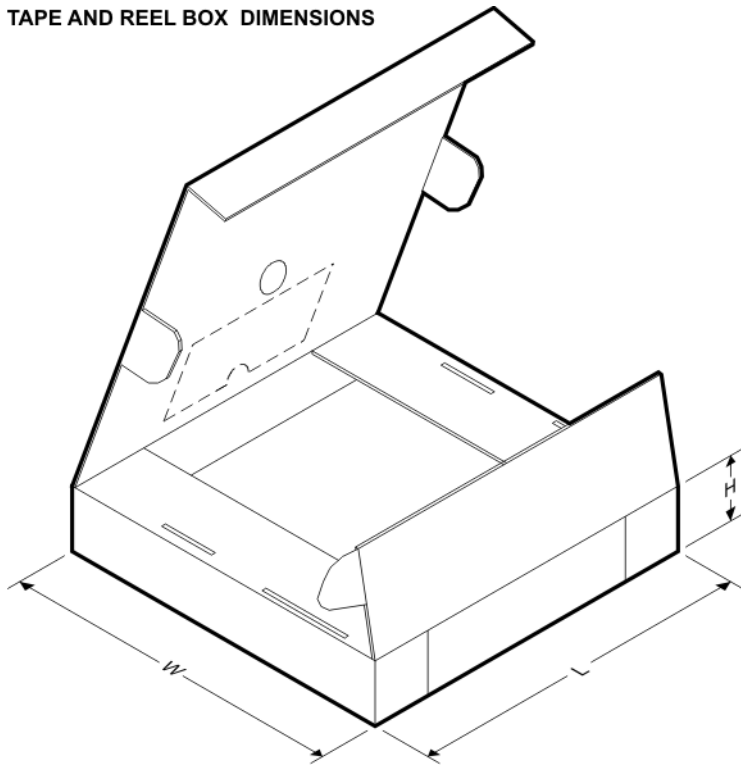
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5066PMHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LM5066PMHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

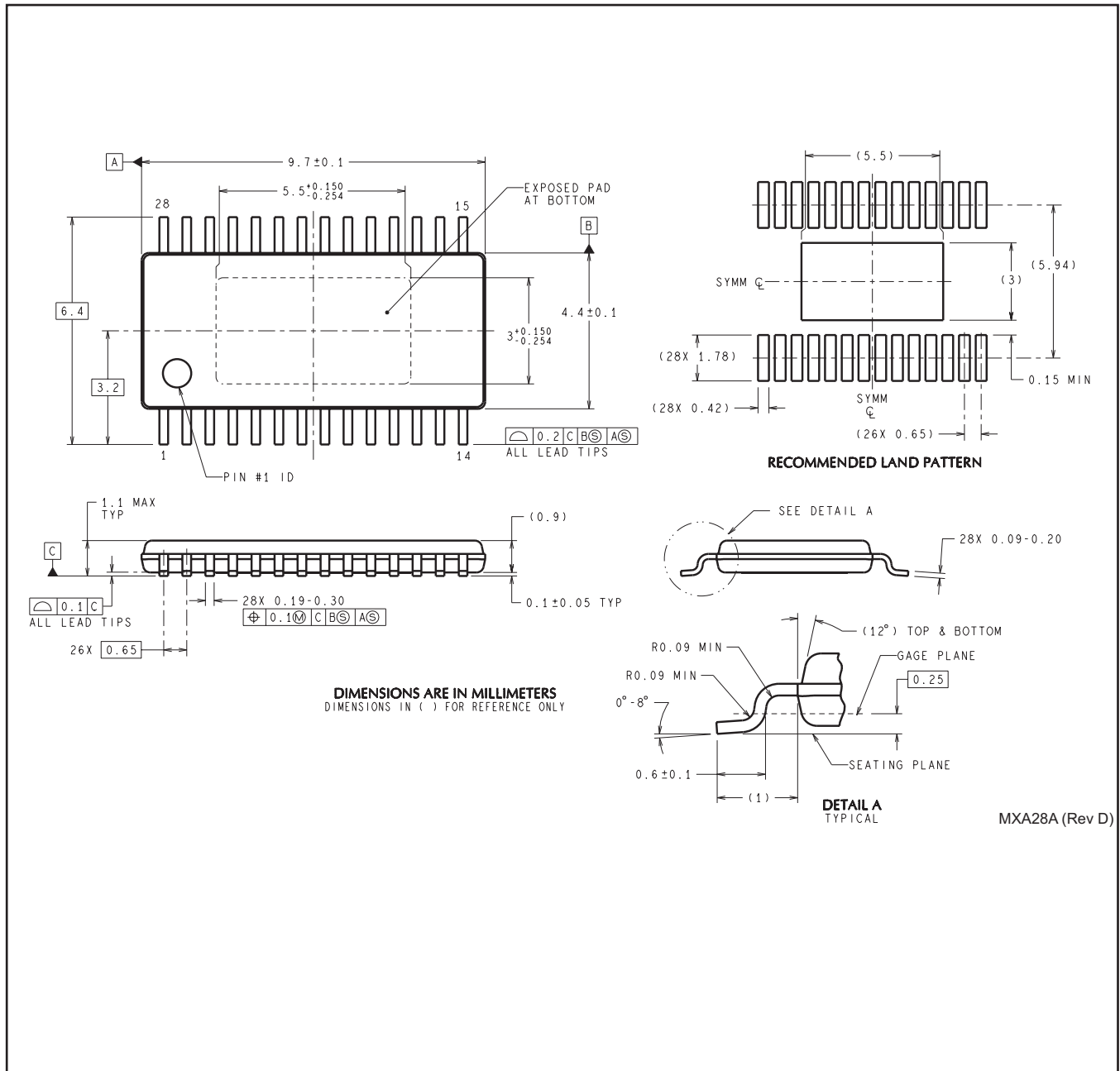
**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5066PMHE/NOPB	HTSSOP	PWP	28	250	213.0	191.0	55.0
LM5066PMHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0

PWP0028A



MXA28A (Rev D)

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