12A High Efficiency Synchronous Point of Load Buck Regulator with Frequency Synchronization

Check for Samples: LM21212-1

FEATURES

- **Integrated 7.0 mΩ High Side and 4.3 mΩ Low Side FET Switches**
- **300 kHz to 1.5 MHz Frequency SYNC pin**
- **Adjustable Output Voltage From 0.6V to V_{IN} (100% duty cycle capable), ±1% Reference**
- **Input Voltage Range 2.95V to 5.5V**
- **Startup Into Pre-Biased Loads**
- **Output Voltage Tracking Capability**
- **Wide Bandwidth Voltage Loop Error Amplifier**
- **Adjustable Soft-Start With External Capacitor**
- **Precision Enable Pin With Hysteresis**
- **Integrated OVP, OCP, OTP, UVLO and Power-Good**
- **Thermally Enhanced HTSSOP-20 Exposed Pad Package**

APPLICATIONS

- **Broadband, Networking and Wireless Communications**
- **High-Performance FPGAs, ASICs and Microprocessors**
- **Simple to Design, High Efficiency Point of Load Regulation From a 5V or 3.3V Bus**

DESCRIPTION

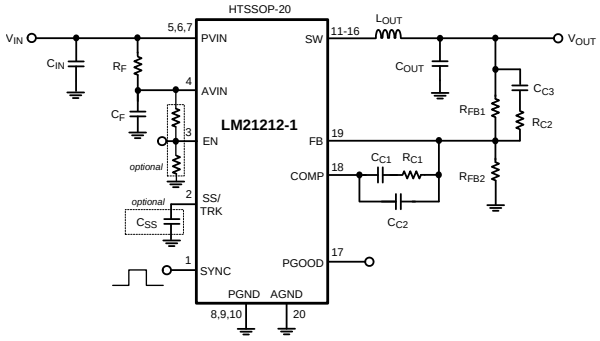
The LM21212-1 is a monolithic synchronous point of load buck regulator that is capable of delivering up to 12A of continuous output current while producing an output voltage down to 0.6V with outstanding efficiency. The device is optimized to work over an input voltage range of 2.95V to 5.5V, making it suited for a wide variety of low voltage systems. The voltage mode control loop provides high noise immunity, narrow duty cycle capability and can be compensated to be stable with any type of output capacitance, providing maximum flexibility and ease of use.

The LM21212-1 features internal over voltage protection (OVP) and over-current protection (OCP) for increased system reliability. A precision enable pin and integrated UVLO allow turn-on of the device to be tightly controlled and sequenced. Startup inrush currents are limited by both an internally fixed and externally adjustable soft-start circuit. Fault detection and supply sequencing are possible with the integrated power good circuit.

The LM21212-1 is designed to work well in multi-rail power supply architectures. The output voltage of the device can be configured to track an external voltage rail using the SS/TRK pin. The switching frequency can be synchronized to the falling edge of a clock between frequencies of 300kHz to 1.5MHz.

If the output is pre-biased at startup, it will not sink current, allowing the output to smoothly rise past the pre-biased voltage. The regulator is offered in a 20-pin HTSSOP package with an exposed pad that can be soldered to the PCB, eliminating the need for bulky heatsinks.

SIMPLIFIED APPLICATION CIRCUIT



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CONNECTION DIAGRAM

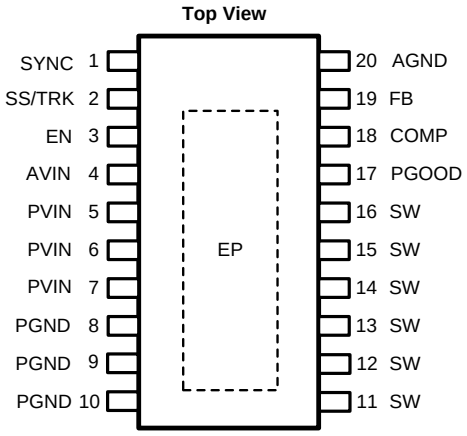


Figure 1. Top View
HTSSOP-20 Package

PIN DESCRIPTIONS

Pins	Name	Description
1	SYNC	Frequency Synchronization input pin. Applying a clock signal to this pin will force the device to switch at the clock frequency. If left unconnected, the frequency will default to 1 MHz.
2	SS/TRK	Soft-start control pin. An internal 2 µA current source charges an external capacitor connected between this pin and AGND to set the output voltage ramp rate during startup. This pin can also be used to configure the tracking feature.
3	EN	Active high enable input for the device. If not used, the EN pin can be left open, which will go high due to an internal current source.
4	AVIN	Analog input voltage supply that generates the internal bias. It is recommended to connect PVIN to AVIN through a low pass RC filter to minimize the influence of input rail ripple and noise on the analog control circuitry.
5,6,7	PVIN	Input voltage to the power switches inside the device. These pins should be connected together at the device. A low ESR input capacitance should be located as close as possible to these pins.
8,9,10	PGND	Power ground pins for the internal power switches.
11-16	SW	Switch node pins. These pins should be tied together locally and connected to the filter inductor.
17	PGOOD	Open-drain power good indicator.
18	COMP	Compensation pin is connected to the output of the voltage loop error amplifier.
19	FB	Feedback pin is connected to the inverting input of the voltage loop error amplifier.
20	AGND	Quiet analog ground for the internal reference and bias circuitry.
EP	Exposed Pad	Exposed metal pad on the underside of the package with an electrical and thermal connection to PGND. It is recommended to connect this pad to the PC board ground plane in order to improve thermal dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

PVIN(3), AVIN to GND	−0.3V to +6V
SW(4), EN, FB, COMP, PGOOD, SS/TRK to GND	−0.3V to PVIN + 0.3V
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating, Human Body Model (5)	2kV

(1) Absolute Maximum Ratings indicate limits beyond witch damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The PVIN pin can tolerate transient voltages up to 6.5 V for a period of up to 6ns. These transients can occur during the normal operation of the device.
(4) The SW pin can tolerate transient voltages up to 9.0 V for a period of up to 6ns, and -1.0V for a duration of 4ns. These transients can occur during the normal operation of the device.
(5) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor to each pin.

OPERATING RATINGS(1)

PVIN, AVIN to GND	+2.95V to +5.5V
Junction Temperature	−40°C to +125°C
θ_{JA}(2)	24°C/W

(1) Absolute Maximum Ratings indicate limits beyond witch damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) Thermal measurements were performed on a 2x2 inch, 4 layer, 2 oz. copper outer layer, 1 oz.copper inner layer board with twelve 8 mil. vias underneith the EP of the device and an additional sixteen 8 mil. vias under the unexposed package.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the following conditions apply: $V_{PVIN,\ AVIN}$ = 5V. Limits in standard type are for T_J = 25°C only, limits in **bold face type** apply over the junction temperature (T_J) range of −40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
V_{FB}	Feedback pin voltage	V_{IN} = 2.95V to 5.5V	**-1%**	0.6	**1%**	V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation			0.02		$\%V_{OUT}$/A
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		$\%V_{OUT}$/V
$R_{DSON\ HS}$	High Side Switch On Resistance	I_{SW} = 12A		7.0	**9.0**	mΩ
$R_{DSON\ LS}$	Low Side Switch On Resistance	I_{SW} = 12A		4.3	**6.0**	mΩ
I_{CLR}	HS Rising Switch Current Limit		**15**	17	**19**	A
I_{CLF}	LS Falling Switch Current Limit			12		A
V_{ZX}	Zero Cross Voltage		-8	3	12	mV
I_Q	Operating Quiescent Current			1.5	**3.0**	mA
I_{SD}	Shutdown Quiescent Current	V_{EN} = 0V		50	**70**	µA
V_{UVLO}	AVIN Under Voltage Lockout	AVIN Rising	**2.45**	2.70	**2.95**	V
$V_{UVLOHYS}$	AVIN Under Voltage Lockout Hysteresis		**140**	200	**280**	mV
$V_{TRACKOS}$	SS/TRACK PIN accuracy (V_{SS} - V_{FB})	0 < V_{TRACK} < 0.55V	**-10**	6	**20**	mV
I_{SS}	Soft-Start Pin Source Current		**1.3**	1.9	**2.5**	µA
t_{INTSS}	Internal Soft-Start Ramp to Vref	C_{SS} = 0	**350**	500	**675**	µs

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, the following conditions apply: $V_{PVIN,\ AVIN}$ = 5V. Limits in standard type are for T_J = 25°C only, limits in **bold face type** apply over the junction temperature (T_J) range of −40°C to +125°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SYSTEM						
$t_{RESETSS}$	DeviceReset to Soft-Start Ramp		**50**	110	**200**	µs
OSCILLATOR						
f_{SYNCR}	SYNC Frequency Range		**300**		**1500**	kHz
$f_{DEFAULT}$	Default (no SYNC signal) Frequency		**950**	1000	**1050**	kHz
t_{SY_SW}	Time from SYNC falling to V_{SW} Rising			200		ns
t_{SY_MIN}	Minimum SYNC pin pulse width, high or low			100		ns
$t_{HSBLANK}$	HS OCP Blanking Time	Rising edge of SW to I_{CLR} comparison		55		ns
$t_{LSBLANK}$	LS OCP Blanking Time	Falling edge of SW to I_{CLF} comparison		400		ns
$t_{ZXBLANK}$	Zero Cross Blanking Time	Falling edge of SW to V_{ZX} comparison		120		ns
t_{MINON}	Minimum HS on-time			140		ns
ΔVramp	PWM Ramp p-p Voltage			0.8		V
ERROR AMPLIFIER						
V_{OL}	Error Amplifier Open Loop Voltage Gain	ICOMP = -65µA to 1mA		95		dBV/V
GBW	Error Amplifier Gain-Bandwidth Product			11		MHz
I_{FB}	Feedback Pin Bias Current	V_{FB} = 0.6V		1		nA
$I_{COMPSRC}$	COMP Output Source Current			1		mA
$I_{COMPSINK}$	COMP Output Sink Current			65		µA
POWERGOOD						
V_{OVP}	Over Voltage Protection Rising Threshold	V_{FB} Rising	**105**	112.5	**120**	$\%V_{FB}$
V_{OVPHYS}	Over Voltage Protection Hysteresis	V_{FB} Falling		2		$\%V_{FB}$
V_{UVP}	Under Voltage Protection Rising Threshold	V_{FB} Rising	**82**	90	**97**	$\%V_{FB}$
V_{UVPHYS}	Under Voltage Protection Hysteresis	V_{FB} Falling		2.5		$\%V_{FB}$
t_{PGDGL}	PGOOD Deglitch Low (OVP/UVP Condition Duration to PGOOD Falling)			15		µs
t_{PGDGH}	PGOOD Deglitch High (minimum low pulse)			12		µs
R_{PGOOD}	PGOOD Pull-down Resistance		**10**	20	**40**	Ω
$I_{PGOODLEAK}$	PGOOD Leakage Current	V_{PGOOD} = 5V		1		nA
LOGIC						
V_{IHSYNC}	SYNC Pin Logic High		2.0			V
V_{ILSYNC}	SYNC Pin Logic Low				0.8	V
V_{IHENR}	EN Pin Rising Threshold	V_{EN} Rising	**1.20**	1.35	**1.45**	V
V_{ENHYS}	EN Pin Hysteresis		**50**	110	**180**	mV
I_{EN}	EN Pin Pullup Current	V_{EN} = 0V		2		µA
THERMAL SHUTDOWN						
$T_{THERMSD}$	Thermal Shutdown			165		°C
$T_{THERMSDHYS}$	Thermal Shutdown Hysteresis			10		°C

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: V_{VIN} = 5V, V_{OUT} = 1.2V, L= 0.56µH (1.8mΩ R_{DCR}), C_{SS} = 33nF, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Efficiency

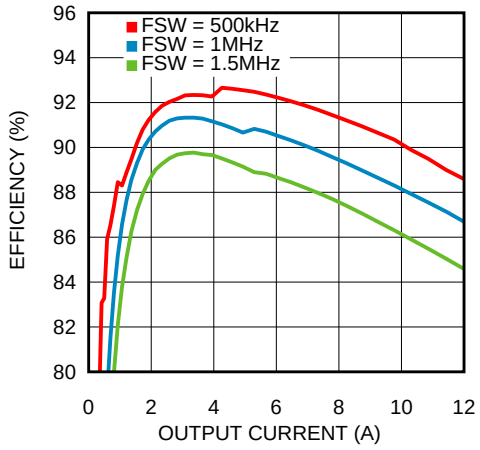


Figure 2.

Efficiency

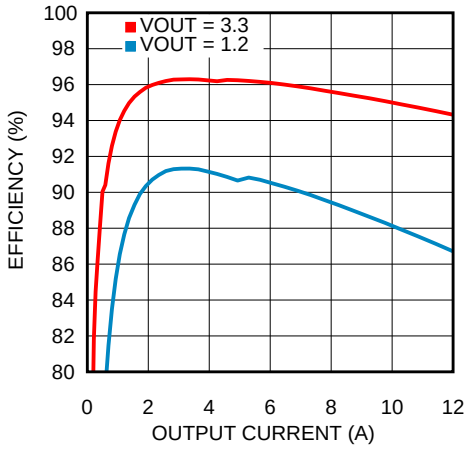


Figure 3.

Efficiency
(VOUT = 2.5 V, f_{SW}= 300 kHz , Inductor P/N SER2010-102MLD)

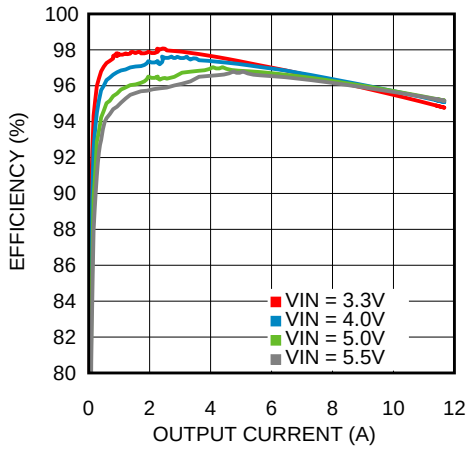


Figure 4.

Load Regulation

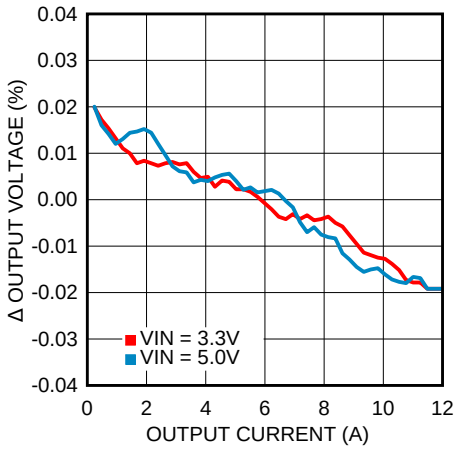


Figure 5.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{VIN} = 5V, V_{OUT} = 1.2V, L= 0.56µH (1.8mΩ R_{DCR}), C_{SS} = 33nF, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Line Regulation

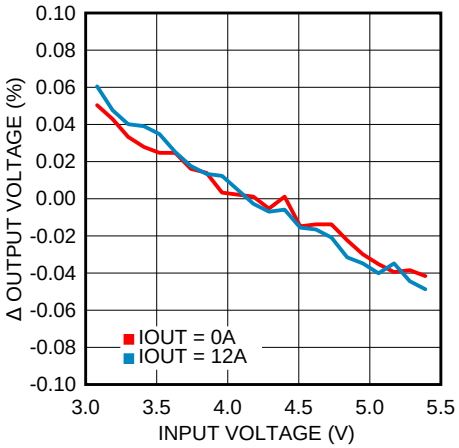


Figure 6.

Non-Switching I_{QTOTAL} vs. V_{IN}

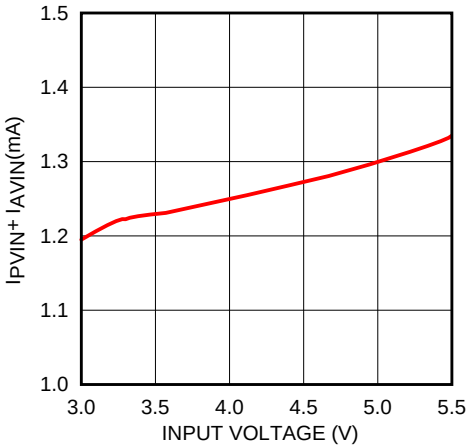


Figure 7.

Non-Switching I_{AVIN} and I_{PVIN} vs. Temperature

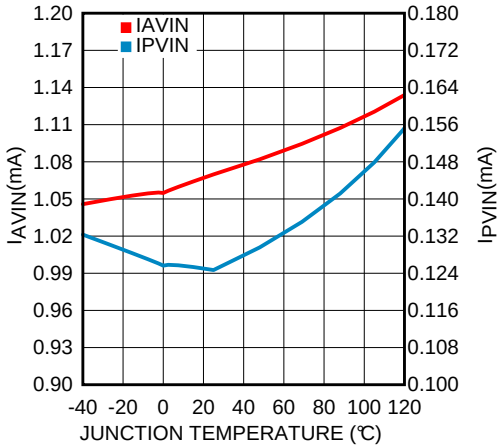


Figure 8.

V_{FB} vs. Temperature

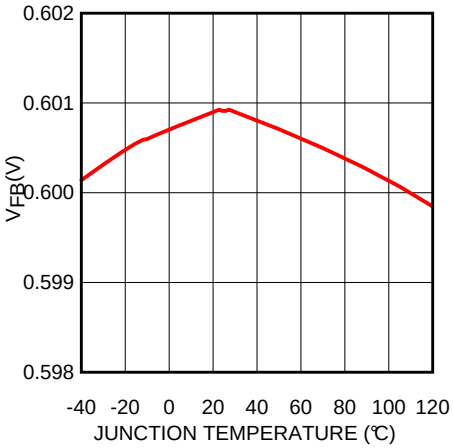


Figure 9.

Enable Threshold and Hysteresis vs. Temperature

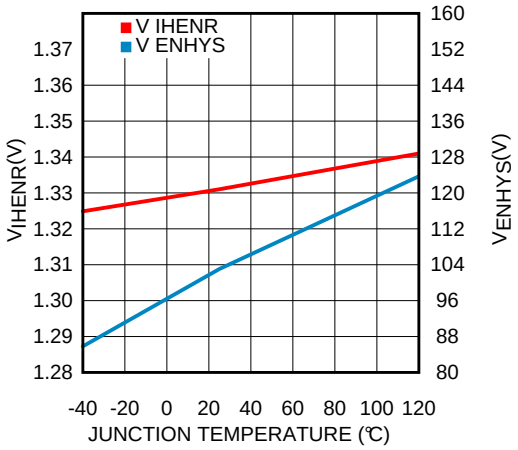


Figure 10.

UVLO Threshold and Hysteresis vs. Temperature

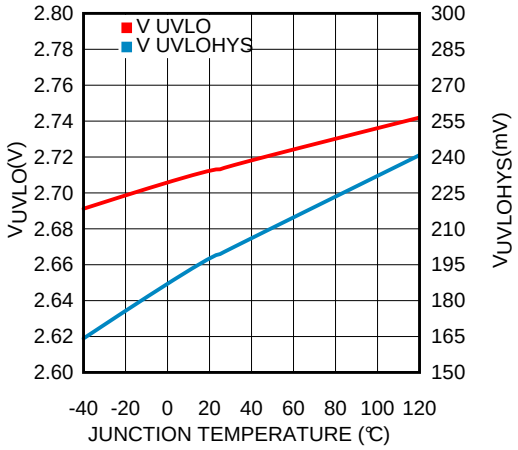


Figure 11.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{VIN} = 5V, V_{OUT} = 1.2V, L= 0.56µH (1.8mΩ R_{DCR}), C_{SS} = 33nF, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Enable Low Current vs. Temperature

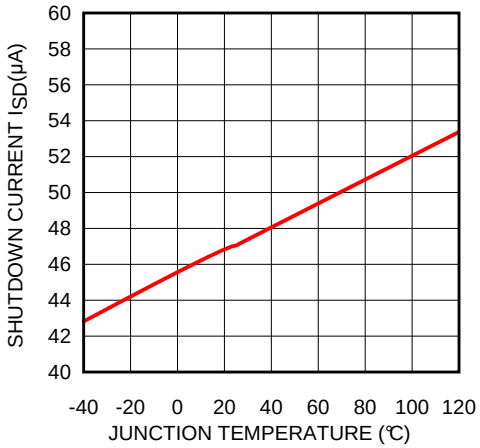


Figure 12.

OVP/UVP Threshold vs. Temperature

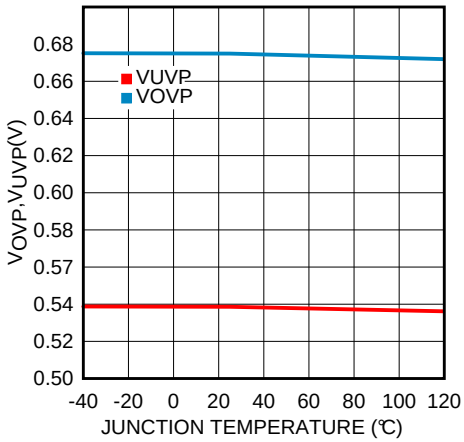


Figure 13.

Minimum On-Time vs. Temperature

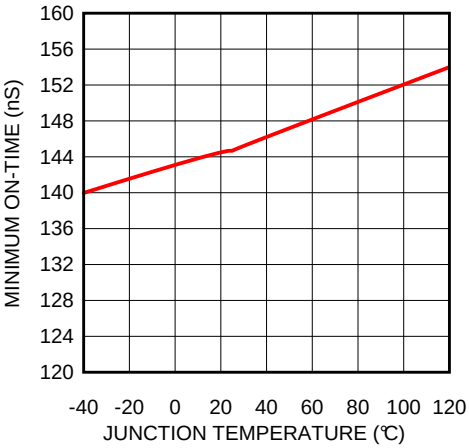


Figure 14.

FET Resistance vs. Temperature

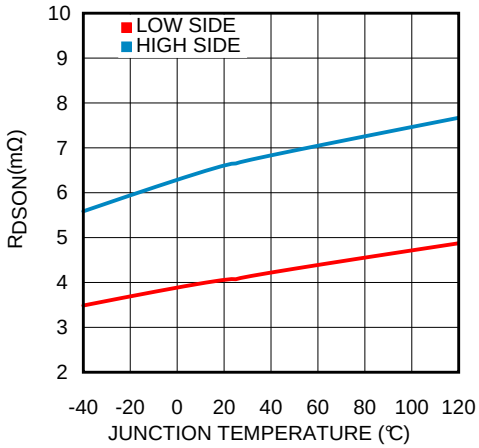


Figure 15.

Peak Current Limit vs. Temperature

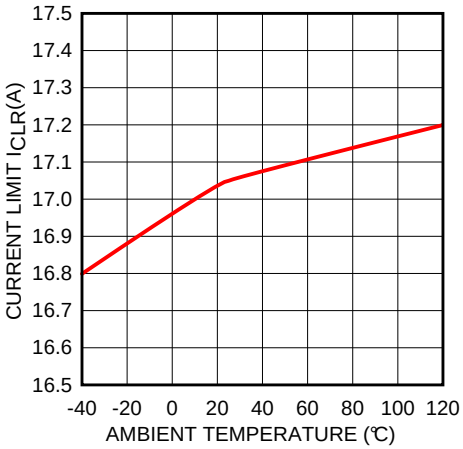
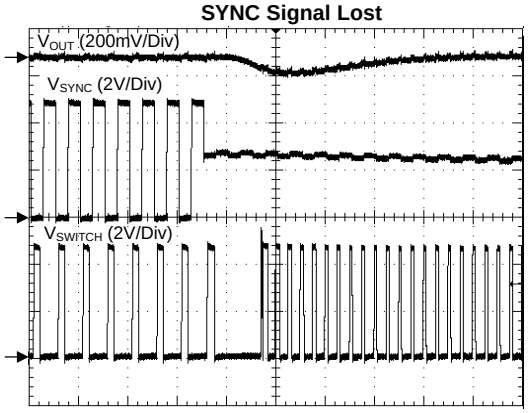


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{VIN} = 5V, V_{OUT} = 1.2V, L= 0.56µH (1.8mΩ R_{DCR}), C_{SS} = 33nF, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

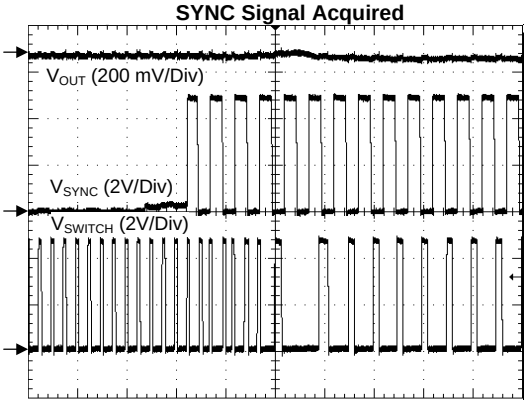
SYNC Signal Lost



4 µs/DIV

Figure 17.

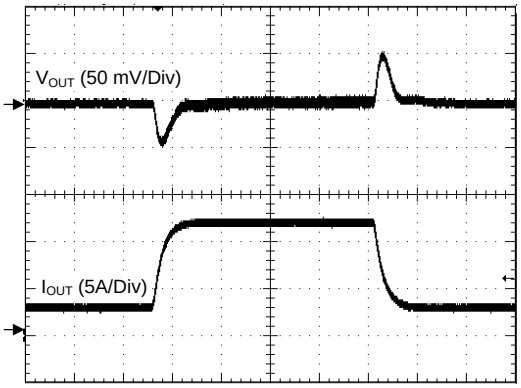
SYNC Signal Acquired



4 µs/DIV

Figure 18.

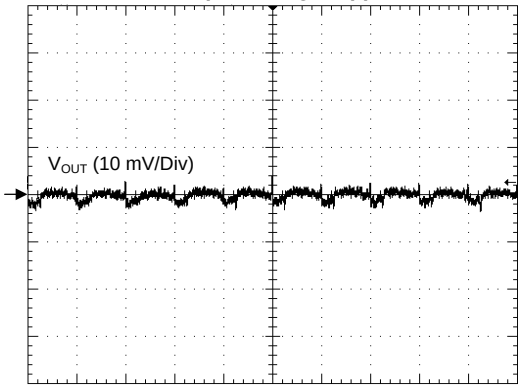
Load Transient Response



100 µs/DIV

Figure 19.

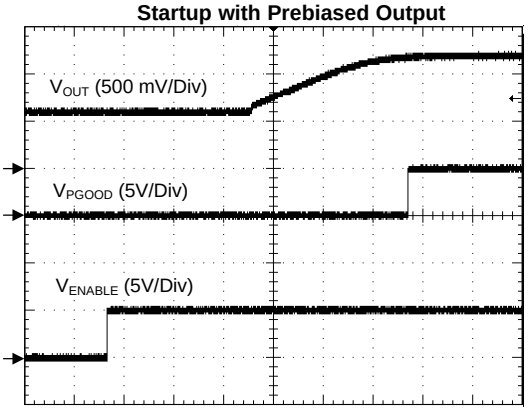
Output Voltage Ripple



1 µs/DIV

Figure 20.

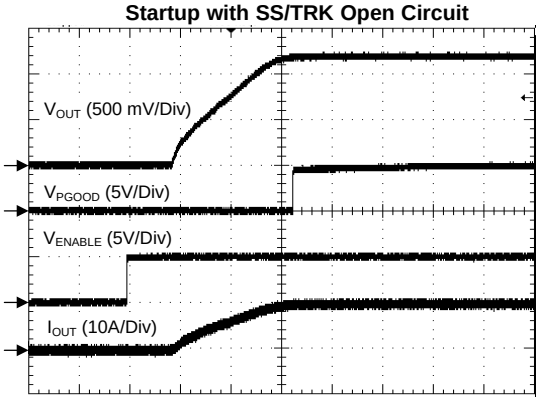
Startup with Prebiased Output



2 ms/DIV

Figure 21.

Startup with SS/TRK Open Circuit



200 µs/DIV

Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: V_{VIN} = 5V, V_{OUT} = 1.2V, L= 0.56µH (1.8mΩ R_{DCR}), C_{SS} = 33nF, f_{SW} = 1 MHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

Startup with applied Track Signal

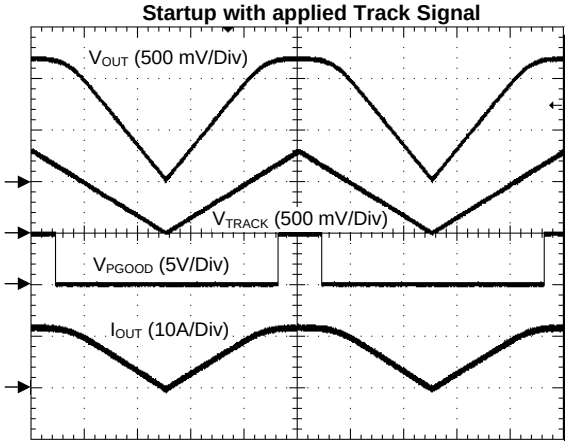


Figure 23.

Output Over-Current Condition

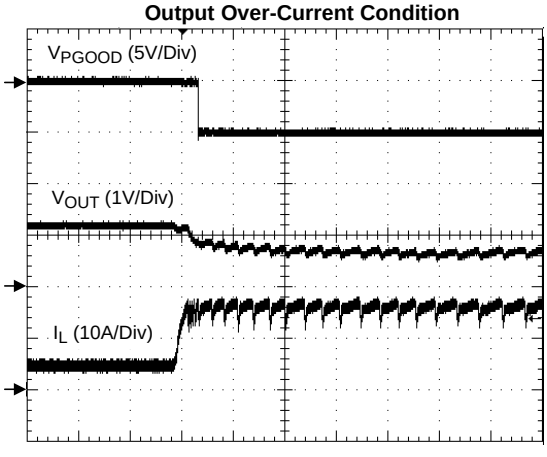
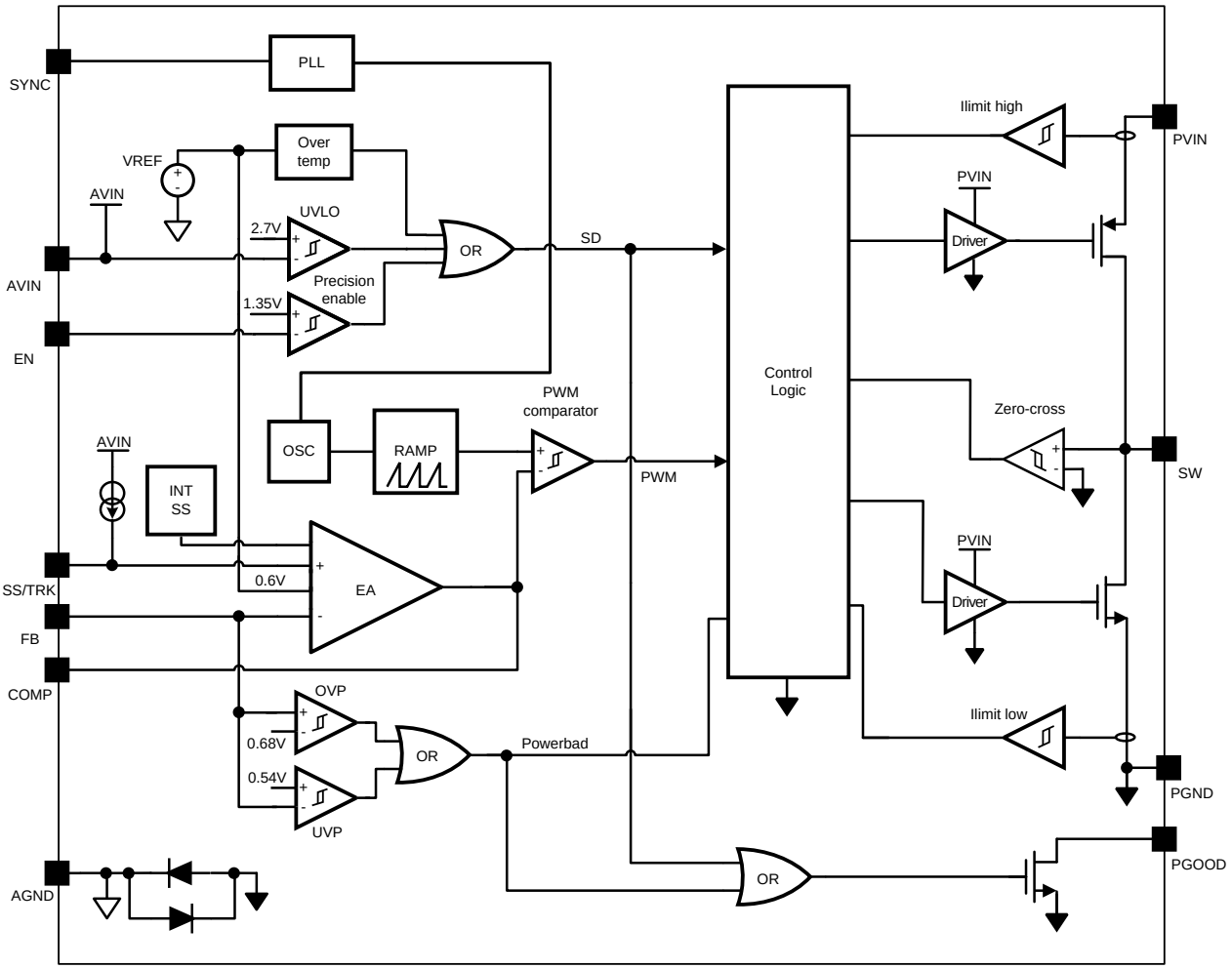


Figure 24.

BLOCK DIAGRAM



OPERATION DESCRIPTION

GENERAL

The LM21212-1 switching regulator features all of the functions necessary to implement an efficient low voltage buck regulator using a minimum number of external components. This easy to use regulator features two integrated switches and is capable of supplying up to 12A of continuous output current. The regulator utilizes voltage mode control with trailing edge modulation to optimize stability and transient response over the entire output voltage range. The device can operate at high switching frequency allowing use of a small inductor while still achieving high efficiency. The precision internal voltage reference allows the output to be set as low as 0.6V. Fault protection features include: current limiting, thermal shutdown, over voltage protection, and shutdown capability. The device is available in the HTSSOP-20 package featuring an exposed pad to aid thermal dissipation. The LM21212-1 can be used in numerous applications to efficiently step-down from a 5V or 3.3V bus.

FREQUENCY SYNCHRONIZATION

The sync (SYNC) pin allows the LM21212-1 to be switched at an external clock frequency. When a clock signal is present on the SYNC pin within the allowable frequency range, 300 kHz to 1.5 MHz, the device will synchronize the turn-on of the high side FET (switch rising) to the negative edge of the clock signal, as seen in Figure 25 . If no clock signal is present, the LM21212-1 will default to a switching frequency of 1 MHz. The clock signal can be present on the SYNC pin before the device is powered on with no loading on the clock signal. Alternatively, if no clock is present while the device is powered up, it will begin switching at the default frequency of 1 MHz. Once the clock signal is present, the device will begin synchronizing to the clock frequency. The length of time necessary for the synchronization depends on the clock frequency.

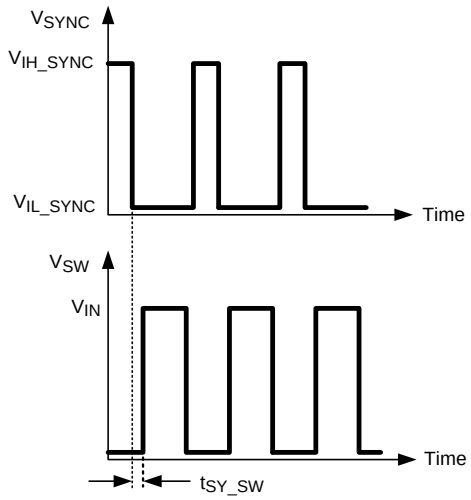


Figure 25. Frequency synchronization

PRECISION ENABLE

The enable (EN) pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.35V (typical). The EN pin has 110 mV of hysteresis and will disable the output when the enable voltage falls below 1.24V (typical). If the EN pin is not used, it can be left open, and will be pulled high by an internal 2 µA current source. Since the enable pin has a precise turn-on threshold it can be used along with an external resistor divider network from VIN to configure the device to turn-on at a precise input voltage.

UVLO

The LM21212-1 has a built-in under-voltage lockout protection circuit that keeps the device from switching until the input voltage reaches 2.7V (typical). The UVLO threshold has 200 mV of hysteresis that keeps the device from responding to power-on glitches during start up. If desired the turn-on point of the supply can be changed by using the precision enable pin and a resistor divider network connected to VIN as shown in Figure 30 in the design guide.

CURRENT LIMIT

The LM21212-1 has current limit protection to avoid dangerous current levels on the power FETs and inductor. A current limit condition is met when the current through the high side FET exceeds the rising current limit level (I_{CLR}). The control circuitry will respond to this event by turning off the high side FET and turning on the low side FET. This forces a negative voltage on the inductor, thereby causing the inductor current to decrease. The high side FET will not conduct again until the lower current limit level (I_{CLF}) is sensed on the low side FET. At this point, the device will resume normal switching.

A current limit condition will cause the internal soft-start voltage to ramp downward. After the internal soft-start ramps below the Feedback (FB) pin voltage, (nominally 0.6 V), FB will begin to ramp downward, as well. This voltage foldback will limit the power consumption in the device, thereby protecting the device from continuously supplying power to the load under a condition that does not fall within the device SOA. After the current limit condition is cleared, the internal soft-start voltage will ramp up again. Figure 26 shows current limit behavior with V_{SS}, V_{FB}, V_{OUT} and V_{SW}.

SHORT-CIRCUIT PROTECTION

In the unfortunate event that the output is shorted with a low impedance to ground, the LM21212-1 will limit the current into the short by resetting the device. A short-circuit condition is sensed by a current-limit condition coinciding with a voltage on the FB pin that is lower than 100 mV. When this condition occurs, the device will begin its reset sequence, turning off both power FETs and discharging the soft-start capacitor after $t_{RESETSS}$ (nominally 110 µs). The device will then attempt to restart. If the short-circuit condition still exists, it will reset again, and repeat until the short-circuit is cleared. The reset prevents excess current flowing through the FETs in a highly inefficient manner, potentially causing thermal damage to the device or the bus supply.

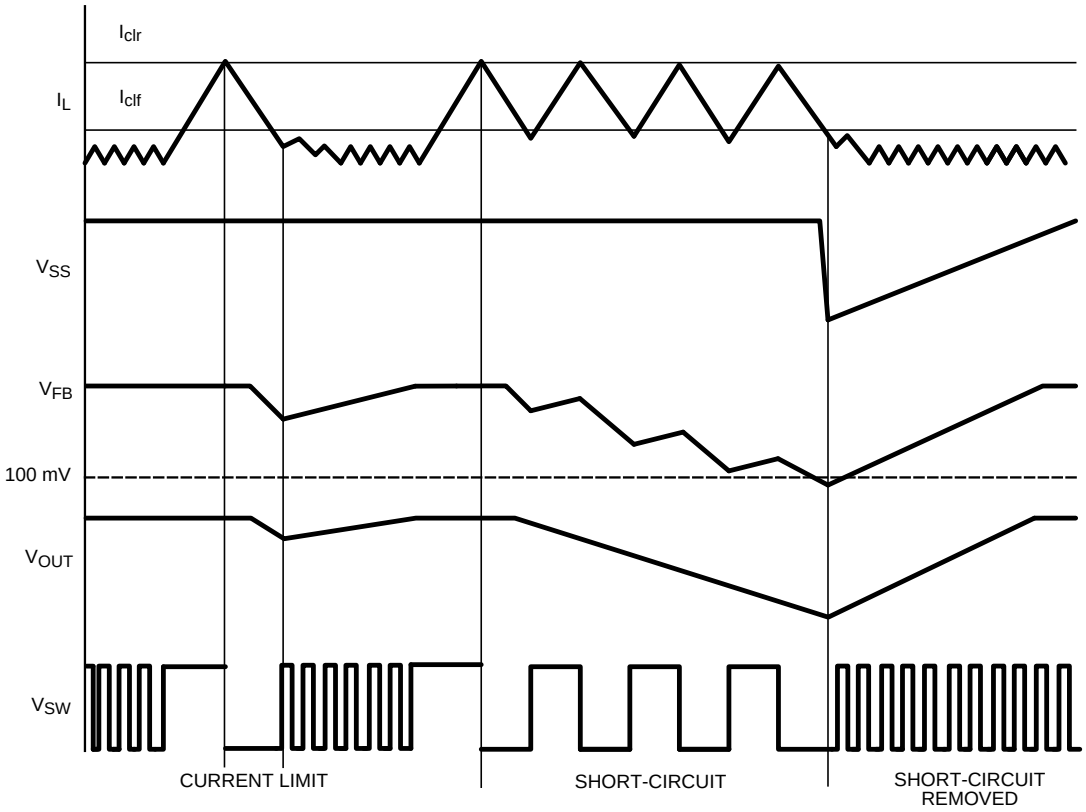


Figure 26. Current Limit Conditions

THERMAL PROTECTION

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the LM21212-1 tri-states the power FETs and resets soft start. After the junction cools to approximately 155°C, the device starts up using the normal start up routine. This feature is provided to prevent catastrophic failures from accidental device overheating. Note that thermal limit will not stop the die from operating above the specified maximum operating temperature,125°C. The die should be kept under 125°C to ensure correct operation.

POWERGOOD FLAG

The PGOOD pin provides the user with a way to monitor the status of the LM21212-1. In order to use the PGOOD pin, the application must provide a pull-up resistor to a desired DC voltage (i.e. Vin). PGOOD will respond to a fault condition by pulling the PGOOD pin low with the open-drain output. PGOOD will pull low on the following conditions – 1) V_{FB} moves above or below the V_{OVP} or V_{UVP}, respectively 2) The enable pin is brought below the enable threshold 3) The device enters a pre-biased output condition (V_{FB}>V_{SS}).

Figure 27 shows the conditions that will cause PGOOD to fall.

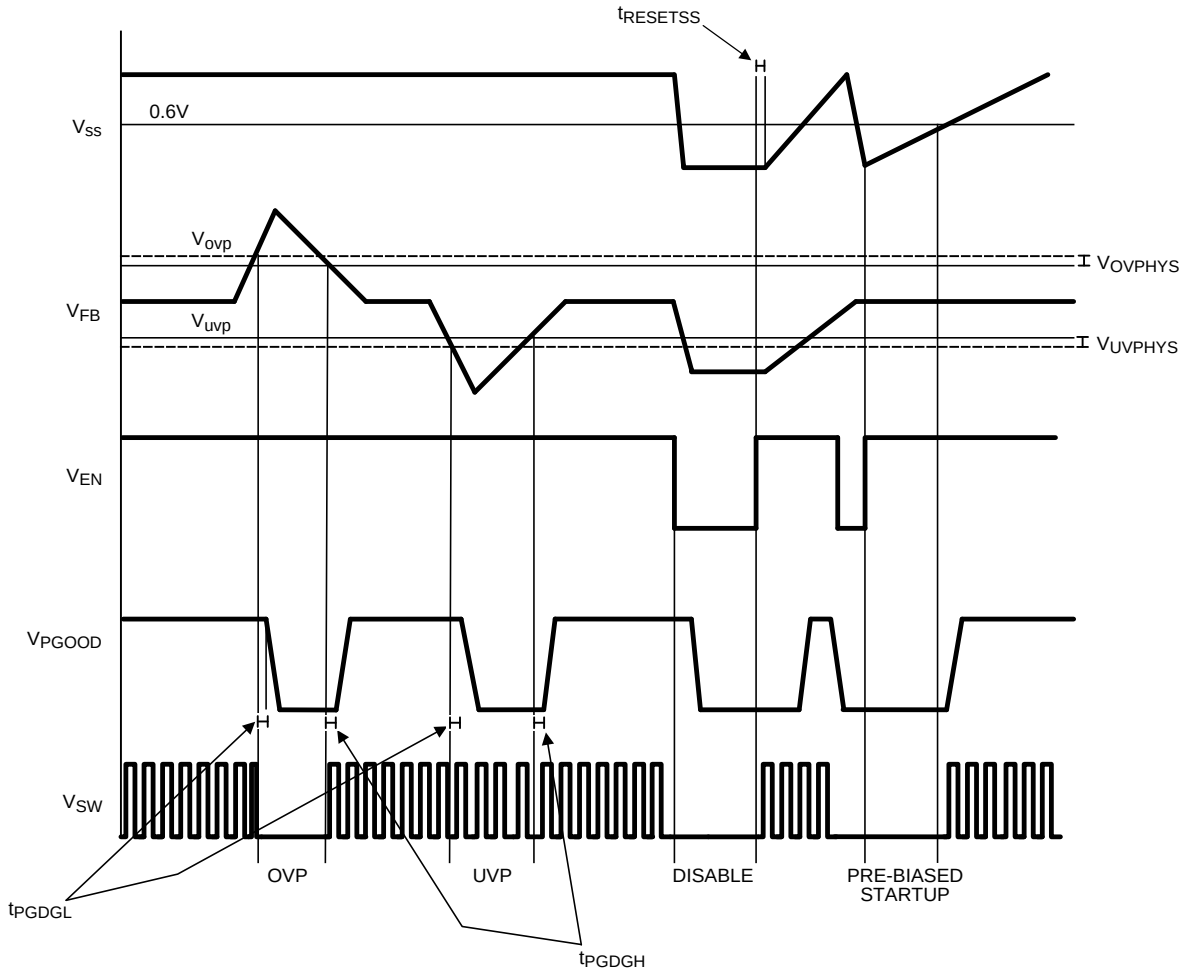


Figure 27. PGOOD Conditions

LIGHT LOAD OPERATION

The LM21212-1 offers increased efficiency when operating at light loads. Whenever the load current is reduced to a point where the peak to peak inductor ripple current is greater than two times the load current, the device will enter the diode emulation mode preventing significant negative inductor current. The point at which this occurs is the critical conduction boundary and can be calculated by the following equation:

$$I_{BOUNDARY} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times f_{SW}} \quad (1)$$

Several diagrams are shown in Figure 28 illustrating continuous conduction mode (CCM), discontinuous conduction mode (DCM), and the boundary condition.

It can be seen that in diode emulation mode, whenever the inductor current reaches zero the SW node will become high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the parasitic capacitance at the node. If this ringing is of concern an additional RC snubber circuit can be added from the switch node to ground.

At very light loads, usually below 100mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

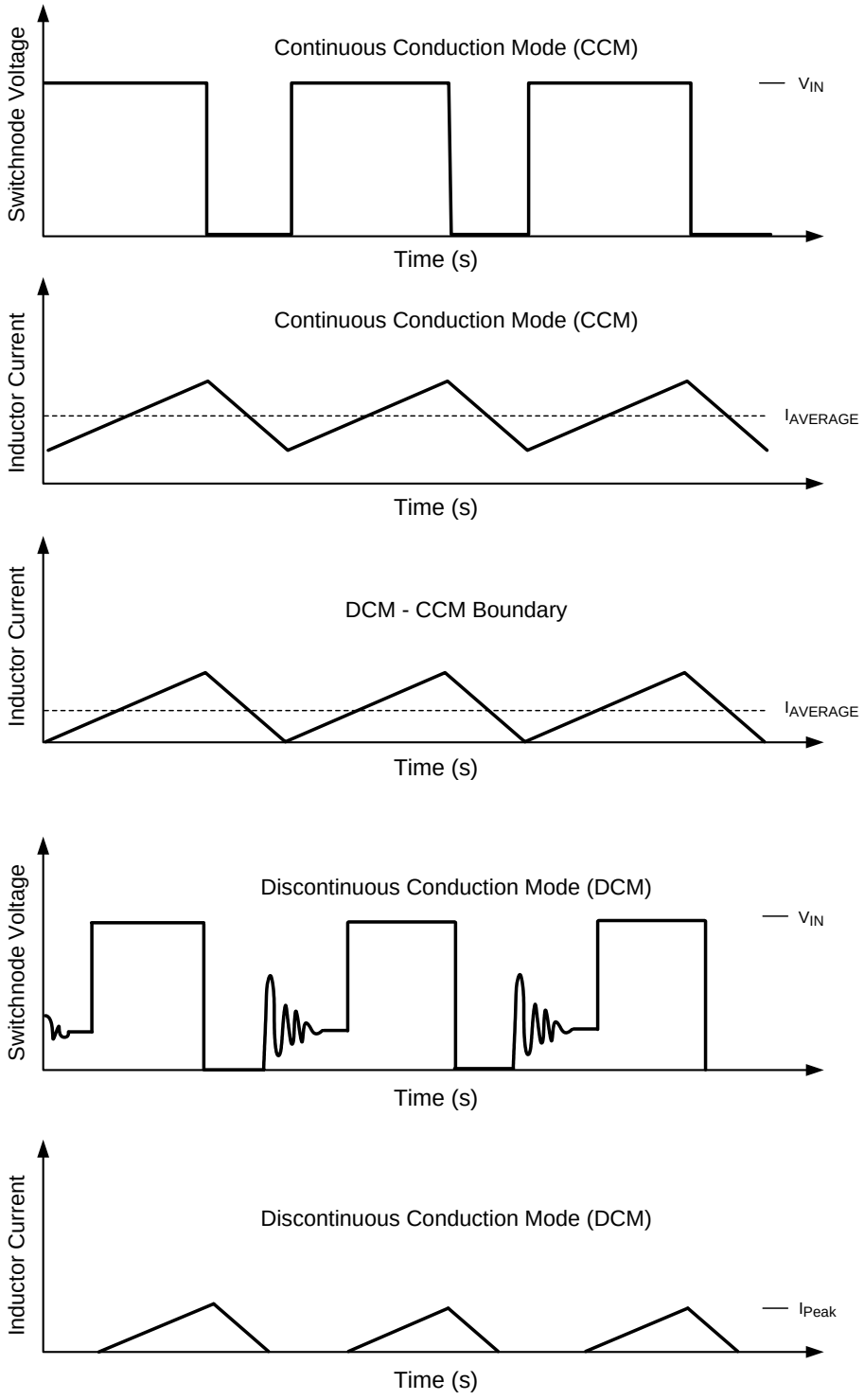


Figure 28. Modes of Operation for LM21212-1

DESIGN GUIDE

OUTPUT VOLTAGE

The first step in designing the LM21212-1 application is setting the output voltage. This is done by using a voltage divider between V_{OUT} and AGND, with the middle node connected to V_{FB}. When operating under steady-state conditions, the LM21212-1 will force V_{OUT} such that V_{FB} is driven to 0.6 V.

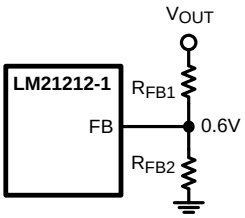


Figure 29. Setting V_{OUT}

A good starting point for the lower feedback resistor, R_{FB2}, is 10kΩ. R_{FB1} can then be calculated the following equation:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} 0.6V \quad (2)$$

PRECISION ENABLE

The enable (EN) pin of the LM21212-1 allows the output to be toggled on and off. This pin is a precision analog input. When the voltage exceeds 1.35V, the controller will try to regulate the output voltage as long as the input voltage has exceeded the UVLO voltage of 2.70V. There is an internal current source connected to EN so if enable is not used, the device will turn on automatically. If EN is not toggled directly the device can be preprogrammed to turn on at a certain input voltage higher than the UVLO voltage. This can be done with an external resistor divider from AVIN to EN and EN to AGND as shown below in Figure 30.

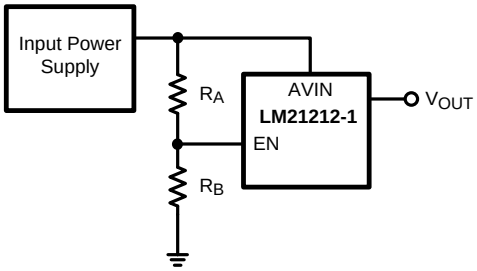


Figure 30. Enable Startup Through Vin

The resistor values of R_A and R_B can be relatively sized to allow EN to reach the enable threshold voltage depending on the input supply voltage. With the enable current source accounted for, the equation solving for R_A is shown below:

$$R_A = \frac{R_B(V_{PVIN} - 1.35V)}{1.35V - I_{EN}R_B} \quad (3)$$

In the above equation, R_A is the resistor from V_{IN} to enable, R_B is the resistor from enable to ground, I_{EN} is the internal enable pull-up current (2µA) and 1.35V is the fixed precision enable threshold voltage. Typical values for R_B range from 10kΩ to 100kΩ.

SOFT START

When EN has exceeded 1.35V, and both PVIN and AVIN have exceeded the UVLO threshold, the LM21212-1 will begin charging the output linearly to the voltage level dictated by the feedback resistor network. The LM21212-1 employs a user adjustable soft start circuit to lengthen the charging time of the output set by a capacitor from the soft start pin to ground. After enable exceeds 1.35V, an internal 2 µA current source begins to charge the soft start capacitor. This allows the user to limit inrush currents due to a high output capacitance and not cause an over current condition. Adding a soft-start capacitor can also reduce the stress on the input rail. Larger capacitor values will result in longer start up times. Use the equation below to approximate the size of the soft-start capacitor:

$$\frac{t_{SS} \times I_{SS}}{0.6V} = C_{SS} \quad (4)$$

where $I_{SS}$is nominally 2 µA and t_{SS} is the desired startup time. If V_{IN} is higher than the UVLO level and enable is toggled high the soft start sequence will begin. There is a small delay between enable transitioning high and the beginning of the soft start sequence. This delay allows the LM21212-1 to initialize its internal circuitry. Once the output has charged to 90% of the nominal output voltage the power good flag will transition high. This behavior is illustrated in Figure 31.

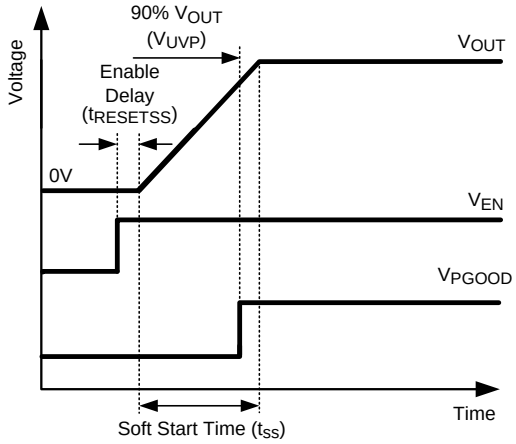


Figure 31. Soft Start Timing

As shown above, the size of the capacitor is influenced by the nominal feedback voltage level 0.6V, the soft-start charging current I_{SS} (2 µA), and the desired soft start time. If no soft-start capacitor is used then the LM21212-1 defaults to a minimum startup time of 500 µs. The LM21212-1 will not startup faster than 500 µs. When enable is cycled or the device enters UVLO, the charge developed on the soft-start capacitor is discharged to reset the startup process. This also happens when the device enters short circuit mode from an over-current event.

INDUCTOR SELECTION

The inductor (L) used in the application will influence the ripple current and the efficiency of the system. The first selection criteria is to define a ripple current, ΔI_L. In a buck converter, it is typically selected to run between 20% to 30% of the maximum output current. Figure 32 shows the ripple current in a standard buck converter operating in continuous conduction mode. Larger ripple current will result in a smaller inductance value, which will lead to a lower series resistance in the inductor, and improved efficiency. However, larger ripple current will also cause the device to operate in discontinuous conduction mode at a higher average output current.

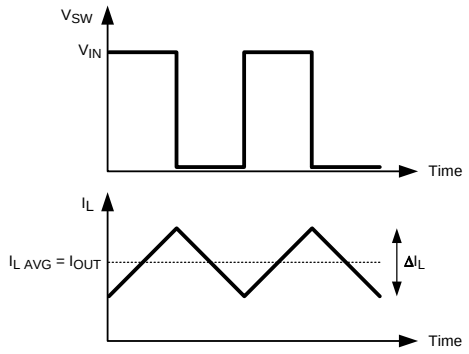


Figure 32. Switch and Inductor Current Waveforms

Once the ripple current has been determined, the appropriate inductor size can be calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \cdot D}{\Delta I_L \cdot f_{SW}} \tag{5}$$

OUTPUT CAPACITOR SELECTION

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM21212-1 that provide various advantages. The best performance is typically obtained using ceramic, SP or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting the value for the output capacitor, the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by using the following formula:

$$\Delta V_{OUT} \approx \Delta I_L \times \left[R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right] \tag{6}$$

where ΔV_{OUT} (V) is the amount of peak to peak voltage ripple at the power supply output, R_{ESR} (Ω) is the series resistance of the output capacitor, f_{SW} (Hz) is the switching frequency, and C_{OUT} (F) is the output capacitance used in the design. The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor the value of the capacitance can drop significantly with applied voltage. The output capacitor selection will also affect the output voltage droop during a load transient. The peak droop on the output voltage during a load transient is dependent on many factors; however, an approximation of the transient droop ignoring loop bandwidth can be obtained using the following equation:

$$V_{DROOP} = \Delta I_{OUTSTEP} \times R_{ESR} + \frac{L \times \Delta I_{OUTSTEP}^2}{C_{OUT} \times (V_{IN} - V_{OUT})} \tag{7}$$

where, C_{OUT} (F) is the minimum required output capacitance, L (H) is the value of the inductor, V_{DROOP} (V) is the output voltage drop ignoring loop bandwidth considerations, $\Delta I_{OUTSTEP}$ (A) is the load step change, R_{ESR} (Ω) is the output capacitor ESR, V_{IN} (V) is the input voltage, and V_{OUT} (V) is the set regulator output voltage. Both the tolerance and voltage coefficient of the capacitor should be examined when designing for a specific output ripple or transient droop target.

INPUT CAPACITOR SELECTION

Quality input capacitors are necessary to limit the ripple voltage at the PVIN pin while supplying most of the switch current during the on-time. Additionally, they help minimize input voltage droop in an output current transient condition. In general, it is recommended to use a ceramic capacitor for the input as it provides both a low impedance and small footprint. Use of a high grade dielectric for the ceramic capacitor, such as X5R or X7R, will provide improved over-temperature performance and also minimize the DC voltage derating that occurs with Y5V capacitors. The input capacitors C_{IN1} and C_{IN2} should be placed as close as possible to the PVIN and PGND pins.

Non-ceramic input capacitors should be selected for RMS current rating and minimum ripple voltage. A good approximation for the required ripple current rating is given by the relationship:

$$I_{IN\text{-}RMS} = I_{OUT} \sqrt{D(1 - D)} \quad (8)$$

As indicated by the RMS ripple current equation, highest requirement for RMS current rating occurs at 50% duty cycle. For this case, the RMS ripple current rating of the input capacitor should be greater than half the output current. For best performance, low ESR ceramic capacitors should be placed in parallel with higher capacitance capacitors to provide the best input filtering for the device.

When operating at low input voltages (3.3V or lower), additional capacitance may be necessary to protect from triggering an under-voltage condition on an output current transient. This will depend on the impedance between the input voltage supply and the LM21212-1, as well as the magnitude and slew rate of the output transient.

The AVIN pin requires a 1 µF ceramic capacitor to AGND and a 1Ω resistor to PVIN. This RC network will filter inherent noise on PVIN from the sensitive analog circuitry connected to AVIN.

CONTROL LOOP COMPENSATION

The LM21212-1 incorporates a high bandwidth amplifier between the FB and COMP pins to allow the user to design a compensation network that matches the application. This section will walk through the various steps in obtaining the open loop transfer function.

There are three main blocks of a voltage mode buck switcher that the power supply designer must consider when designing the control system; the power train, modulator, and the compensated error amplifier. A closed loop diagram is shown in Figure 33.

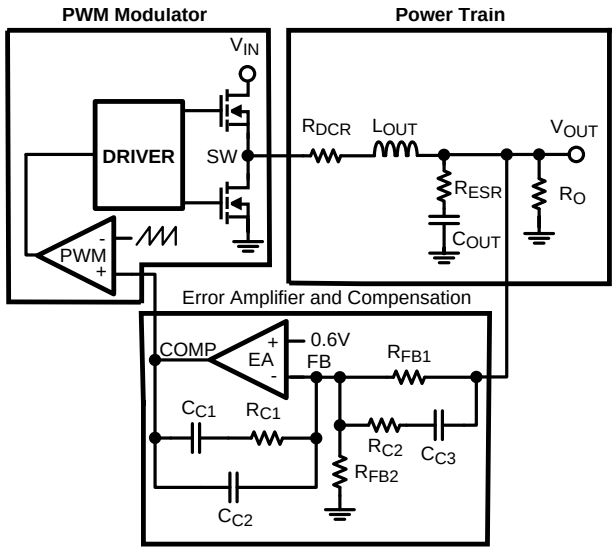


Figure 33. Loop Diagram

The power train consists of the output inductor (L) with DCR (DC resistance R_{DCR}), output capacitor (C_0) with ESR (effective series resistance R_{ESR}), and load resistance (R_0). The error amplifier (EA) constantly forces FB to 0.6V. The passive compensation components around the error amplifier help maintain system stability. The modulator creates the duty cycle by comparing the error amplifier signal with an internally generated ramp set at the switching frequency.

There are three transfer functions that must be taken into consideration when obtaining the total open loop transfer function; COMP to SW (Modulator) , SW to V_{OUT} (Power Train), and V_{OUT} to COMP (Error Amplifier). The COMP to SW transfer function is simply the gain of the PWM modulator.

$$G_{PWM} = \frac{V_{in}}{\Delta V_{ramp}} \tag{9}$$

where ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8 V). The SW to COMP transfer function includes the output inductor, output capacitor, and output load resistance. The inductor and capacitor create two complex poles at a frequency described by:

$$f_{LC} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_{DCR}}{L_{OUT}C_{OUT}(R_O + R_{ESR})}} \tag{10}$$

In addition to two complex poles, a left half plane zero is created by the output capacitor ESR located at a frequency described by:

$$f_{esr} = \frac{1}{2\pi C_o R_{esr}} \tag{11}$$

A Bode plot showing the power train response can be seen below.

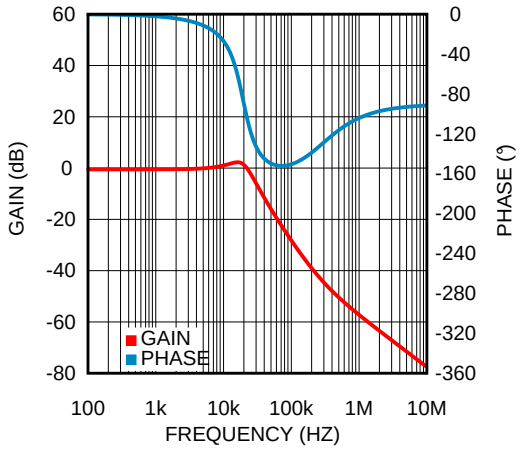


Figure 34. Power Train Bode Plot

The complex poles created by the output inductor and capacitor cause a 180° phase shift at the resonant frequency as seen in Figure 34. The phase is boosted back up to -90° due to the output capacitor ESR zero. The 180° phase shift must be compensated out and phase boosted through the error amplifier to stabilize the closed loop response. The compensation network shown around the error amplifier in Figure 33 creates two poles, two zeros and a pole at the origin. Placing these poles and zeros at the correct frequencies will stabilize the closed loop response. The Compensated Error Amplifier transfer function is:

$$G_{EA} = K_m \frac{\left(\frac{s}{2\pi f_{Z1}} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)} \tag{12}$$

The pole located at the origin gives high open loop gain at DC, translating into improved load regulation accuracy. This pole occurs at a very low frequency due to the limited gain of the error amplifier, however, it can be approximated at DC for the purposes of compensation. The other two poles and two zeros can be located accordingly to stabilize the voltage mode loop depending on the power stage complex poles and Q. Figure 35 is an illustration of what the Error Amplifier Compensation transfer function will look like.

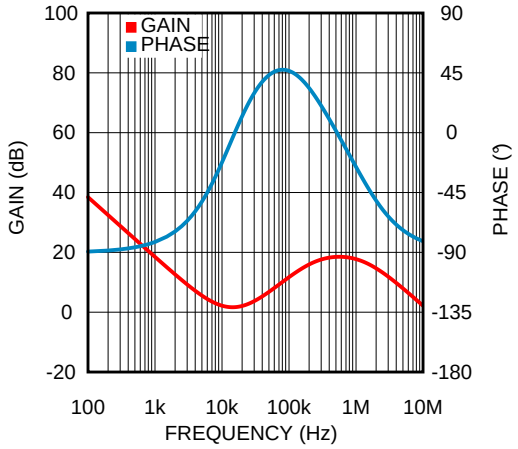


Figure 35. Type 3 Compensation Network Bode Plot

As seen in Figure 35, the two zeros ($f_{LC}/2$, f_{LC}) in the comensation network give a phase boost. This will cancel out the effects of the phase loss from the output filter. The compensation network also adds two poles to the system. One pole should be located at the zero caused by the output capacitor ESR (f_{ESR}) and the other pole should be at half the switching frequency ($f_{SW}/2$) to roll off the high frequency response. The dependancy of the pole and zero locations on the compensation components is described below.

$$f_{Z1} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_{C1} C_{C1}}$$

$$f_{Z2} = f_{LC} = \frac{1}{2\pi (R_{C1} + R_{FB1}) C_{C3}}$$

$$f_{P1} = f_{ESR} = \frac{1}{2\pi R_{C2} C_{C3}}$$

$$f_{P2} = \frac{f_{sw}}{2} = \frac{C_{C1} + C_{C2}}{2\pi R_{C1} C_{C1} C_{C2}} \quad (13)$$

An example of the step-by-step procedure to generate compensation component values using the typical application setup (see Figure 40) is given. The parameters needed for the compensation values are given in the table below.

Parameter	Value
V_{IN}	5.0V
V_{OUT}	1.2V
I_{OUT}	12A
$f_{CROSSOVER}$	100 kHz
L	0.56 µH
R_{DCR}	1.8 mΩ
C_O	150 µF
R_{ESR}	1.0 mΩ
ΔV_{RAMP}	0.8V
f_{SW}	500 kHz

where ΔV_{RAMP} is the oscillator peak-to-peak ramp voltage (nominally 0.8V), and $f_{CROSSOVER}$ is the frequency at which the open-loop gain is a magnitude of 1. It is recommended that the $f_{crossover}$ not exceed one-fifth of the switching frequency. The output capacitance, C_O, depends on capacitor chemistry and bias voltage. For Multi-Layer Ceramic Capacitors (MLCC), the total capacitance will degrade as the DC bias voltage is increased. Measuring the actual capacitance value for the output capacitors at the output voltage is recommended to accurately calculate the compensation network. The example given here is the total output capacitance using the three MLCC output capacitors biased at 1.2V, as seen in the typical application schematic, Figure 40. Note that it is more conservative, from a stability standpoint, to err on the side of a smaller output capacitance value in the compensation calculations rather than a larger, as this will result in a lower bandwidth but increased phase margin.

First, a the value of R_{FB1} should be chosen. A typical value is 10kΩ. From this, the value of R_{C1} can be calculated to set the mid-band gain so that the desired crossover frequency is achieved:

$$R_{C1} = \frac{f_{crossover}}{f_{LC}} \bullet \frac{\Delta V_{RAMP}}{V_{IN}} \bullet R_{FB1}$$
$$= \frac{100\ kHz}{17.4\ kHz} \frac{0.8\ V}{5.0\ V} 10\ k\Omega$$
$$= 9.2\ k\Omega \quad (14)$$

Next, the value of C_{C1} can be calculated by placing a zero at half of the LC double pole frequency (f_{LC}):

$$C_{C1} = \frac{1}{\pi f_{LC} R_{C1}}$$
$$= 1.99\ nF \quad (15)$$

Now the value of C_{C2} can be calculated to place a pole at half of the switching frequency (f_{SW}):

$$C_{C2} = \frac{C_{C1}}{\pi f_{SW} R_{C1} C_{C1} - 1}$$
$$= 71\ pF \quad (16)$$

R_{C2} can then be calculated to set the second zero at the LC double pole frequency:

$$R_{C2} = \frac{R_{FB1} f_{LC}}{f_{ESR} - f_{LC}}$$
$$= 166\Omega \quad (17)$$

Last, C_{C3} can be calculated to place a pole at the same frequency as the zero created by the output capacitor ESR:

$$C_{C3} = \frac{1}{2\pi f_{ESR} R_{C2}}$$
$$= 898\ pF \quad (18)$$

An illustration of the total loop response can be seen in Figure 36.

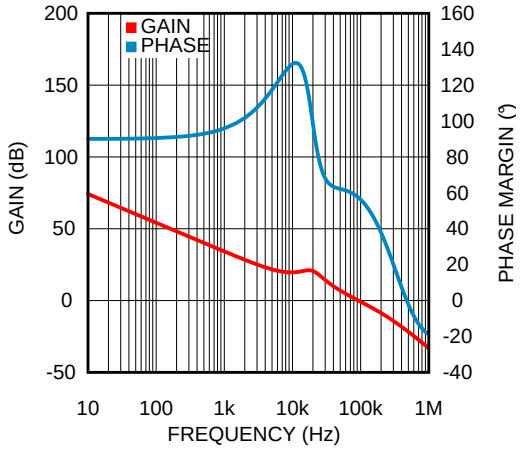


Figure 36. Loop Response

It is important to verify the stability by either observing the load transient response or by using a network analyzer. A phase margin between 45° and 70° is usually desired for voltage mode systems. Excessive phase margin can cause slow system response to load transients and low phase margin may cause an oscillatory load transient response. If the load step response peak deviation is larger than desired, increasing $f_{CROSSOVER}$ and recalculating the compensation components may help but usually at the expense of phase margin.

THERMAL CONSIDERATIONS

The thermal characteristics of the LM21212-1 are specified using the parameter θ_{JA}, which relates the junction temperature to the ambient temperature. Although the value of θ_{JA} is dependant on many variables, it still can be used to approximate the operating junction temperature of the device.

To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \bullet \theta_{JA} + T_A \tag{19}$$

and

$$P_D = P_{IN} \bullet (1 - \text{Efficiency}) - I_{OUT}^2 \bullet R_{DCR} \tag{20}$$

Where:

T_J is the junction temperature in °C, P_{IN} is the input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$), θ_{JA} is the junction to ambient thermal resistance for the LM21212-1, T_A is the ambient temperature in °C, and I_{OUT} is the output load current.

It is important to always keep the operating junction temperature (T_J) below 125°C for reliable operation. If the junction temperature exceeds 165°C the device will cycle in and out of thermal shutdown. If thermal shutdown occurs it is a sign of inadequate heatsinking or excessive power dissipation in the device.

Figure 37, shown below, provides a better approximation of the θ_{JA} for a given PCB copper area. The PCB used in this test consisted of 4 layers: 1oz. copper was used for the internal layers while the external layers were plated to 2oz. copper weight. To provide an optimal thermal connection, a 3 x 4 array of 8 mil. vias under the thermal pad were used, and an additional sixteen 8 mil. vias under the rest of the device were used to connect the 4 layers.

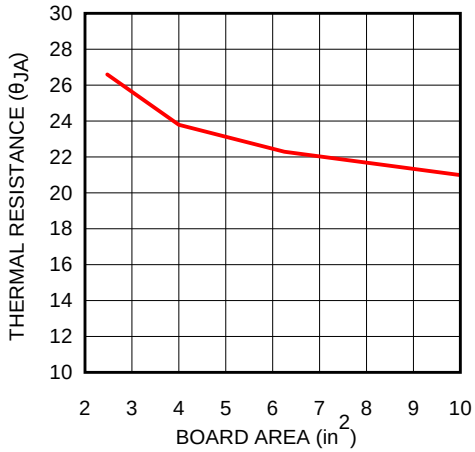


Figure 37. Thermal Resistance vs PCB Area (4 Layer Board)

Figure 38 shows a plot of the maximum ambient temperature vs. output current for the typical application circuit shown in Figure 40, assuming a θ_{JA} value of 24 °C/W.

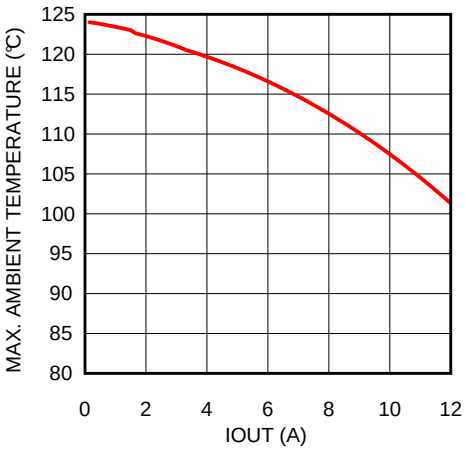


Figure 38. Maximum Ambient Temperature vs. Output Current (0 LFM)

PCB LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability.

Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched at high slew rates. The first loop starts from the input capacitor, to the regulator PVIN pin, to the regulator SW pin, to the inductor then out to the output capacitor and load. The second loop starts from the output capacitor ground, to the regulator GND pins, to the inductor and then out to the load (see Figure 39). To minimize both loop areas, the input capacitor should be placed as close as possible to the VIN pin. Grounding for both the input and output capacitor should be close. Ideally, a ground plane should be placed on the top layer that connects the PGND pins, the exposed pad (EP) of the device, and the ground connections of the input and output capacitors in a small area near pin 10 and 11 of the device. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The six SW pins should be routed on a single top plane to the pad of the inductor. The inductor should be placed as close as possible to the switch pins of the device with

a wide trace to minimize conductive losses. The inductor can be placed on the bottom side of the PCB relative to the LM21212-1, but care must be taken to not allow any coupling of the magnetic field of the inductor into the sensitive feedback or compensation traces.

3. Have a solid ground plane between PGND, the EP and the input and output cap. ground connections. The ground connections for the AGND, compensation, feedback, and soft-start components should be physically isolated (located near pin 1 and 20) from the power ground plane but a separate ground connection is not necessary. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Carefully route the connection from the VOUT signal to the compensation network. This node is high impedance and can be susceptible to noise coupling. The trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Voltage accuracy at the load is important so make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.
6. Provide adequate device heatsinking. For most 12A designs a four layer board is recommended. Use as many vias as is possible to connect the EP to the power plane heatsink. The vias located underneith the EP will wick solder into them if they are not filled. Complete solder coverage of the EP to the board is required to achieve the θ_{JA} values described in the previous section. Either an adequate amount of solder must be applied to the EP pad to fill the vias, or the vias must be filled during manufacturing. See the THERMAL CONSIDERATIONS section to ensure enough copper heatsinking area is used to keep the junction temperature below 125°C.

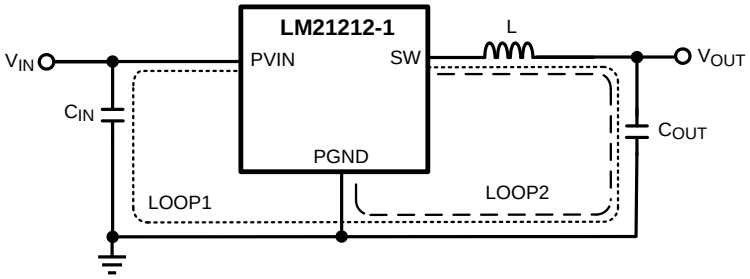


Figure 39. Schematic of LM21212-1 Highlighting Layout Sensitive Nodes

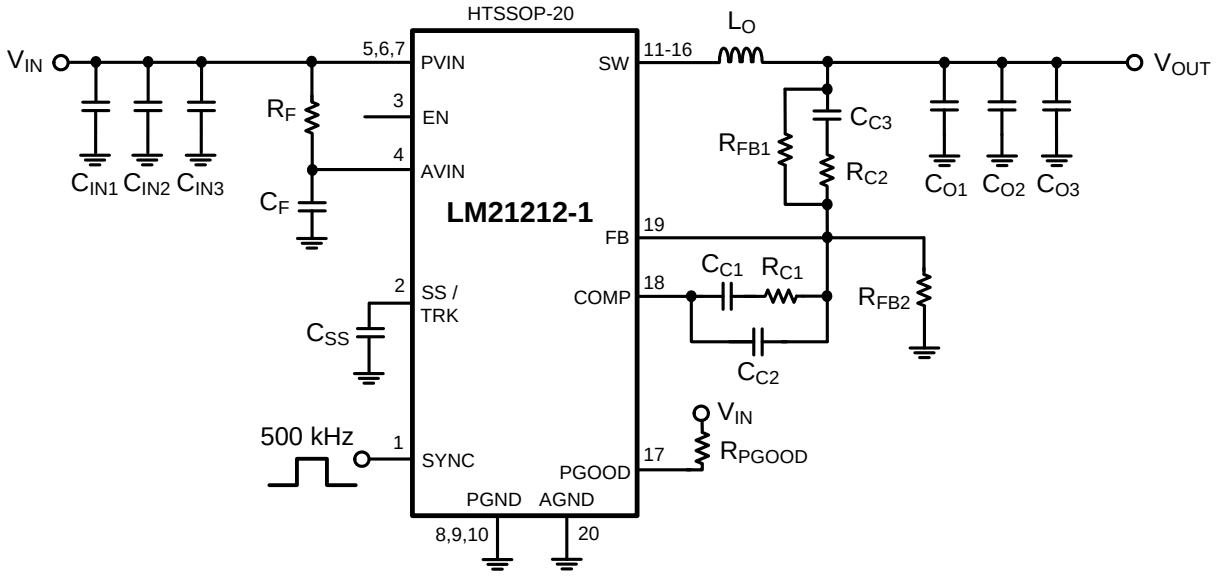


Figure 40. Typical Application Schematic 1

Table 1. Bill of Materials (V_{IN} = 3.3 - 5.5V, V_{OUT} = 1.2V, I_{OUT} = 12A, f_{SW} = 500kHz)

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1}, C_{IN2}, C_{IN3}, C_{O1}, C_{O2}, C_{O3}	CAP, CERM, 100uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	6
C_{C1}	CAP, CERM, 1800pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H182J	1
C_{C2}	CAP, CERM, 68pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 820pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H821J	1
C_{SS}	CAP, CERM, 0.033uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_O	Inductor, Shielded Drum Core, Powdered Iron, 560nH, 27.5A, 0.0018 ohm, SMD	Vishay-Dale	IHLP4040DZERR56M01	1
R_F	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 9.31k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06039K31FKEA	1
R_{C2}	RES, 165 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603165RFKEA	1
R_{FB1}, R_{FB2}, R_{PGOOD}	RES, 10k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3

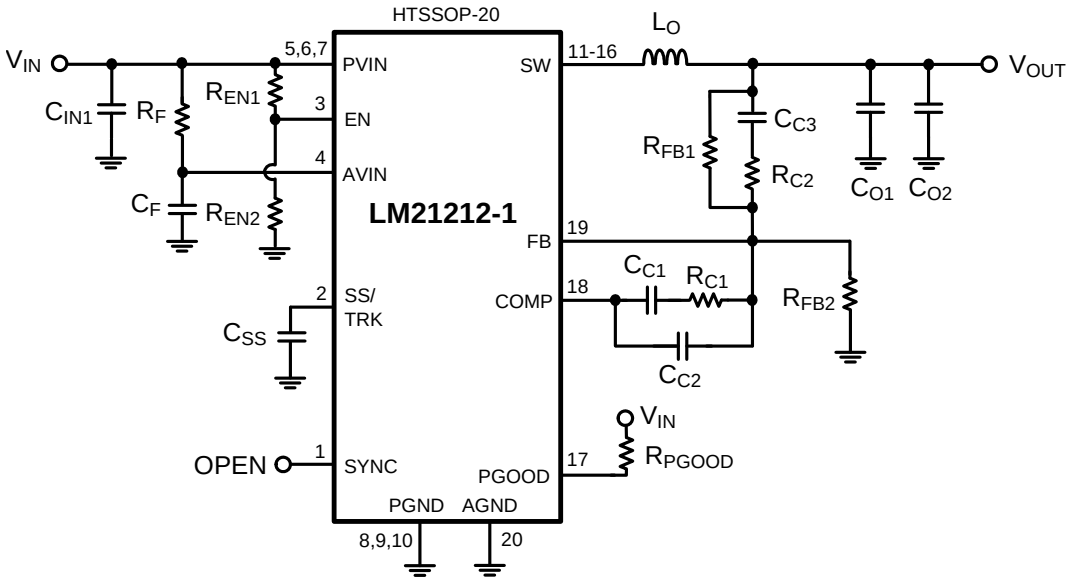


Figure 41. Typical Application Schematic 2

Table 2. Bill of Materials (V_{IN} = 4.0 - 5.5V, V_{OUT} = 0.9V, I_{OUT} = 8A, f_{SW} = 1MHz)

ID	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1}, C_{O1}, C_{O2}	CAP, CERM, 100uF, 6.3V, +/-20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	3
C_{C1}	CAP, CERM, 1800pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H182JA01D	1
C_{C2}	CAP, CERM, 68pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 470pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H471J	1
C_{SS}	CAP, CERM, 0.033uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_O	Inductor, Shielded Drum Core, Superflux, 240nH, 20A, 0.001 ohm, SMD	Wurth Elektronik eiSos	744314024	1
R_F	RES, 1.0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 4.87k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K87FKEA	1
R_{C2}	RES, 210 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603210RFKEA	1
R_{EN1}, R_{FB1}, R_{PGOOD}	RES, 10k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R_{EN2}	RES, 19.6k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060319K6FKEA	1
R_{FB2}	RES, 20.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K0FKEA	1

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	27

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM21212MH-1/NOPB	ACTIVE	HTSSOP	PWP	20	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-1	Samples
LM21212MHE-1/NOPB	ACTIVE	HTSSOP	PWP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		LM21212 MH-1	Samples
LM21212MHX-1/NOPB	ACTIVE	HTSSOP	PWP	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21212 MH-1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

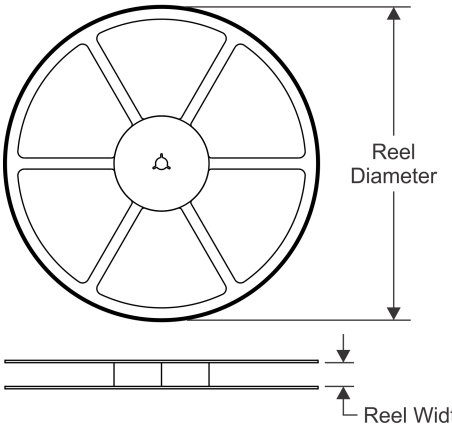
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

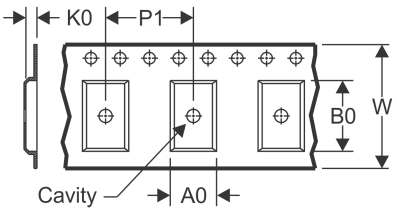
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

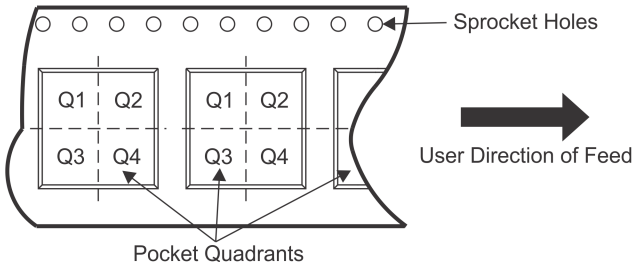


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

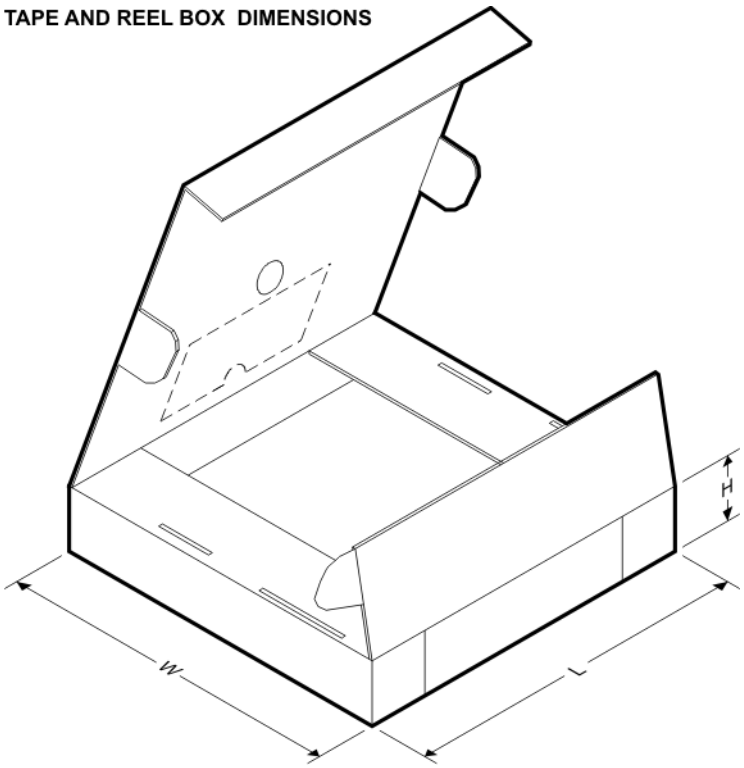
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM21212MHE-1/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
LM21212MHX-1/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

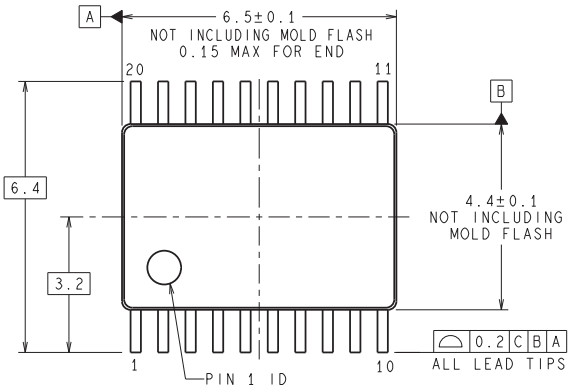
TAPE AND REEL BOX DIMENSIONS



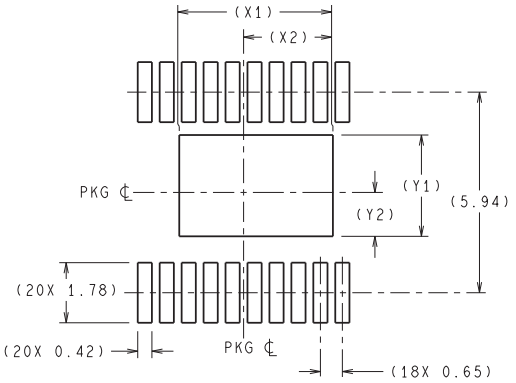
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM21212MHE-1/NOPB	HTSSOP	PWP	20	250	203.0	190.0	41.0
LM21212MHX-1/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

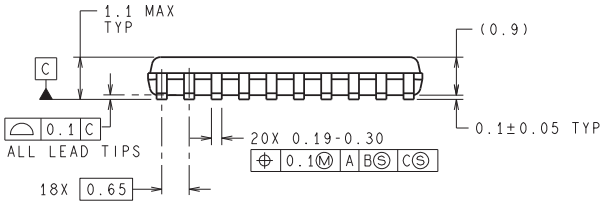
PWP0020AA

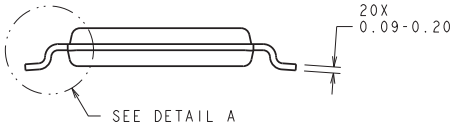


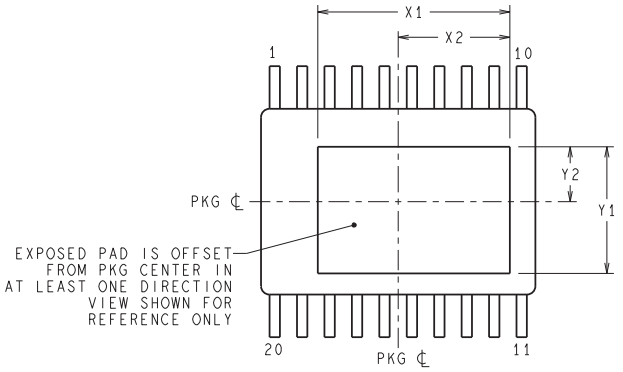
TOP VIEW



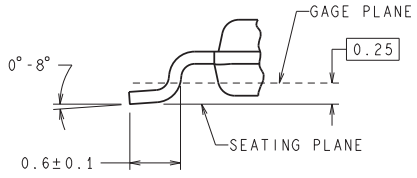
LAND PATTERN RECOMENDATION







BOTTOM VIEW



DETAIL A
TYPICAL

PAD SIZE CODE IN DWG No. (XX)	PAD SIZE		X2	Y2
	X1	Y1		
AA	4.55	3.32	2.645±0.1	1.66±0.1

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MYB20XX (REV E)

4214875/A 02/2013

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Reference JEDEC Registration MO-153, Variation ACT.

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