High Performance Power Management Unit for Handset Applications

Check for Samples: LP3925

FEATURES

- **Linear Charger With Single Input**
  - **USB or AC Adapter Input**
  - **Power Routing Switch**
  - **28-V OVP on the Charger Input**
- **Three High-Efficiency Synchronous Magnetic Buck Regulators, I_{OUT} 800 mA Each:**
  - **Two Regulators Have DVS Support**
  - **High-Efficiency ECO Mode at Low I_{OUT}**
  - **Auto Mode ECO/PWM Switch**
  - **28-V OVP on the Charger Input**
- **15 LDOs**
  - **10 General-Type Low-Noise LDOs: 8 x 300 mA, 2 x 80 mA**
  - **Three Wide-Input Low-Output (WILO) LDOs, All Capable of Supplying up to 300 mA**
  - **One Micro-Power LDO With I_{OUT} 30 mA**
  - **One High-Voltage USB LDO**
  - **S/W Controllable Outputs**
  - **Outputs Configurable for Pulldown**
- **Two Comparators and Two TCXO Buffers**
- **USB 2.0-Compatible Transceiver (12 Mbps)**
- **12-Bit A/D Converter for Battery Management and External Monitoring**
- **Two Over-Voltage Protected Outputs for USB Transceivers**
- **Real-Time Clock With Two Alarms**
- **SIM Card Level Translator**
- **Three Controllable Current Sinks for Keypad LEDs**
- **Backup Battery Charger**
- **Thermal Shutdown With Early Warning Alarm**
- **Momentary Power Loss detection**
- **Interrupt Request to Reduce S/W Polling**
- **81-Bump DSBGA Package**

KEY SPECIFICATIONS

- **Low PMU I_Q in Sleep Mode**
- **50-mA to 1200-mA Charging Current From AC Adapter**
- **3.0-V to 4.5-V Battery Voltage**
- **150-mV (Typ) Dropout Voltage on LDOs at 300 mA**
- **2% (Typ) Output Voltage Accuracy on LDOs**
- **Ultra Low Noise (10 µV Typ), Ultra Low I_Q, Remote Capacitor General-Type "Perfect" LDOs**
- **3% Accurate Buck Regulators up to 90% Efficient**

APPLICATIONS

- **GSM, GPRS, EDGE, CDMA, and 3G Handsets**

DESCRIPTION

The LP3925 is designed to meet the power management requirements of the latest 3G/GSM/GPRS/EDGE cellular phones. The LP3925 PMU contains a single-input Li-Ion battery charger, 14 low-dropout voltage regulators including 3 wide-input, low-output, regulators, 3 buck regulators, a USB Transceiver, two comparators, two TCXO buffers, SIM level shifter, 12-bit ADC, real time clock, and backup battery charger. Programming is handled via an I^2C-compatible high-speed Serial Interface allowing control of program on/off conditions and the output voltages of individual regulators, and to read status information of the PMU.

It can charge and maintain a single cell Li-Ion battery operating from an AC adapter or USB power source.

The Li-Ion charger requires few external components and integrates the power FET. Charging is thermally regulated to obtain the most efficient charging rate for a given ambient temperature.

A built-in Over-Voltage Protection (OVP) circuit at the charger input protects the PMU from input voltages up to +28V eliminating the need for any external protection circuitry.

Buck regulators have an automatic switch to ECO mode at low load conditions providing very good efficiency at low output currents.

DESCRIPTION (CONTINUED)

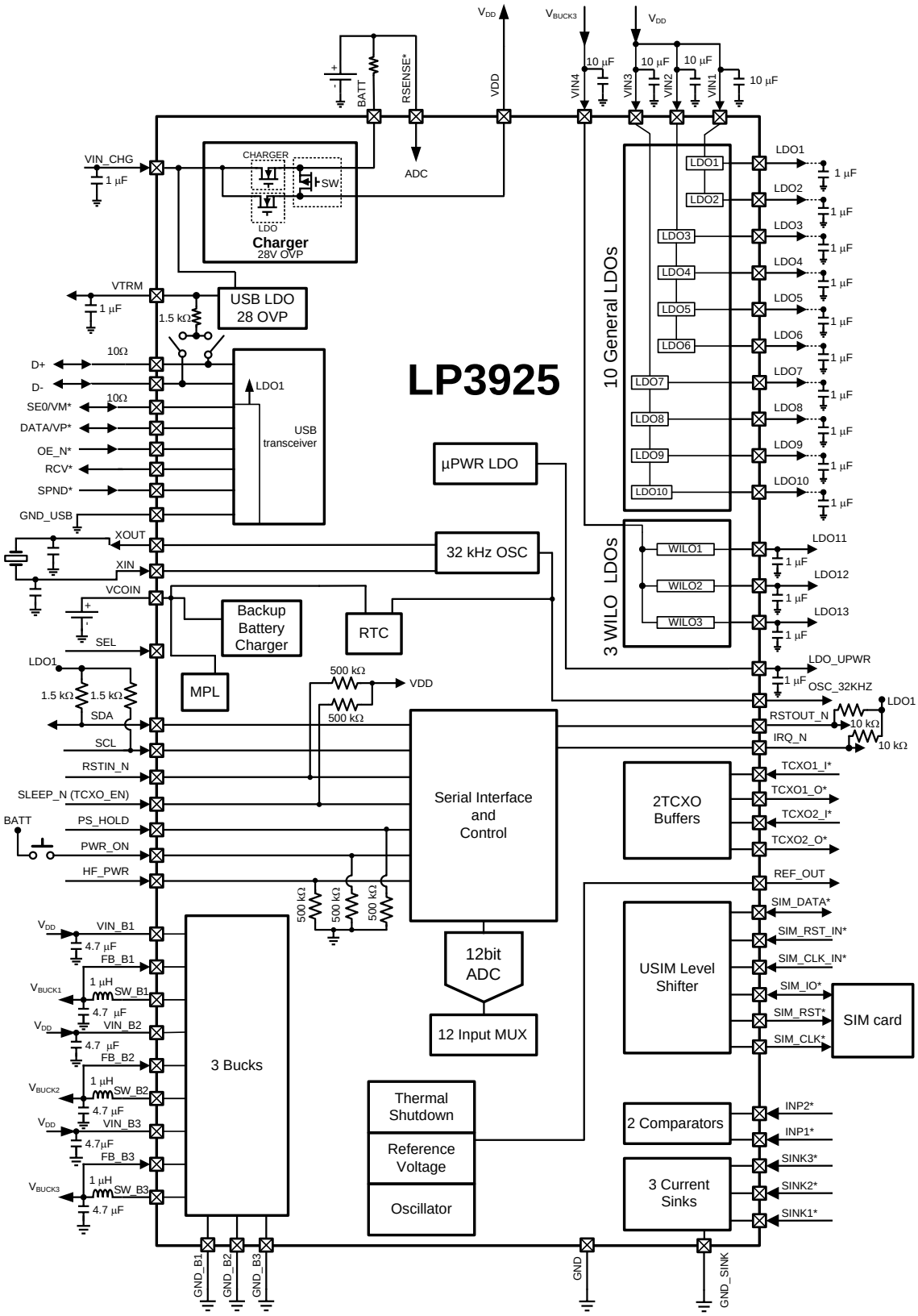
Buck regulators have an automatic switch to ECO mode at low load conditions providing very good efficiency at low output currents.

General-type “PERFECT” LDO regulators provide excellent PSRR and ULTRA LOW NOISE, 10 µV typ., ideally suited for supplying voltage to RF section.

The real-time clock/calendar provides time interval information as well as two programmable alarms.

To accommodate different baseband requirements, the LP3925 PMU has different default voltage settings and startup sequences. Two general-purpose comparators can be used for detecting external accessories like ear-phones etc. Power conversion and signal level shifting circuits are provided to allow SIM interfacing.

Typical Application Diagram



Pin Configuration

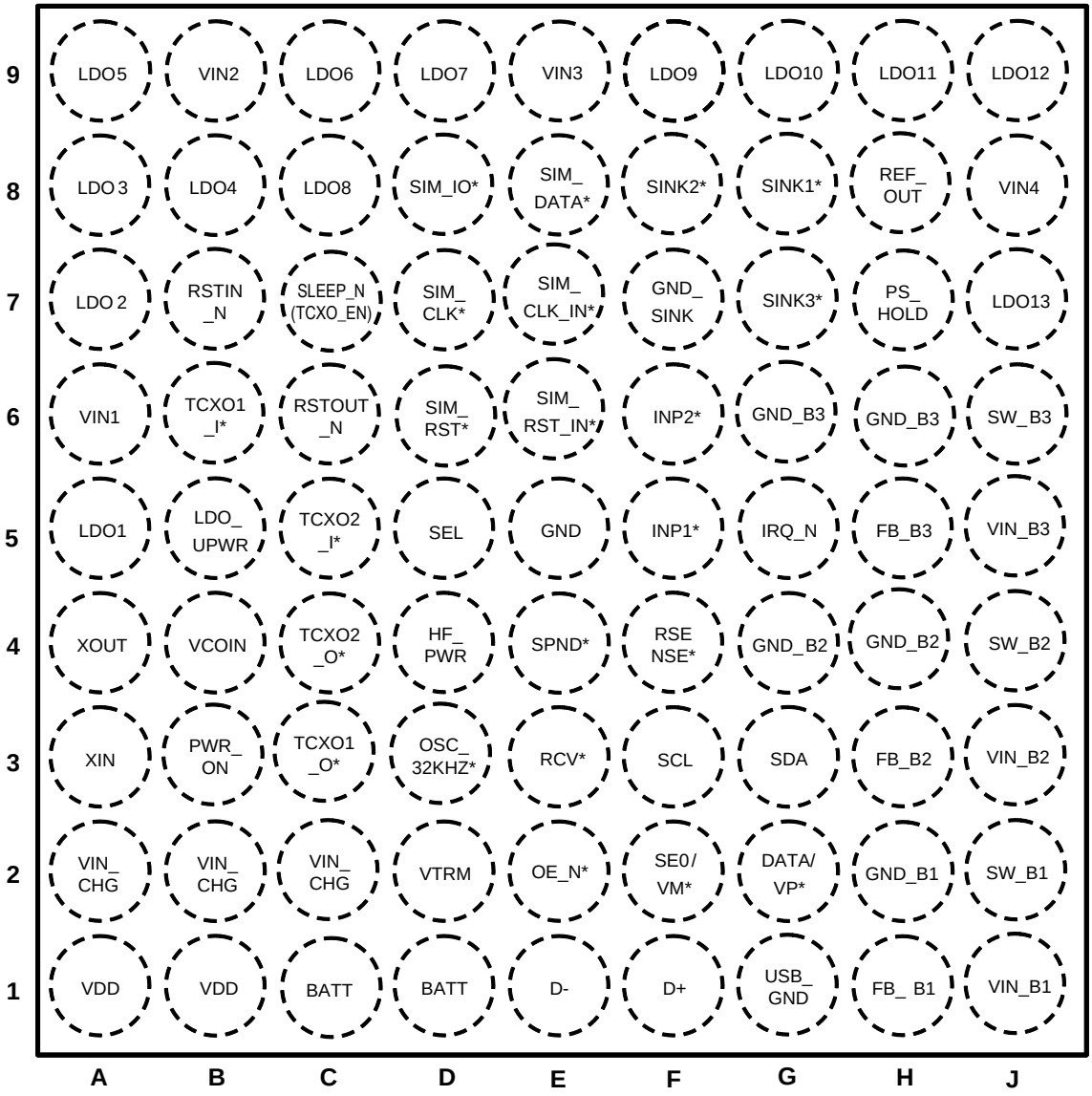
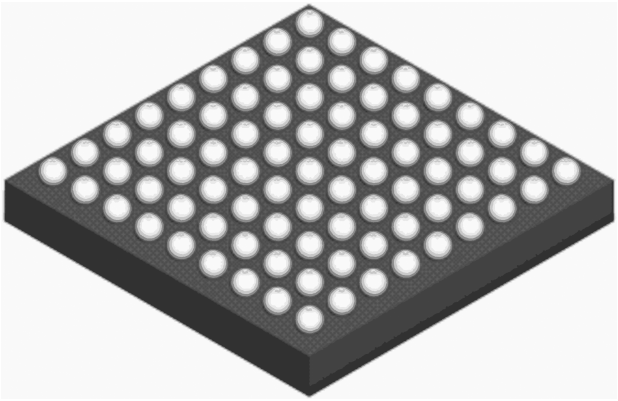


Figure 1. LP3925 (Top View)

* Pins that can be programmed as analog pins (default as stated in pin configuration) or digital input/output pins. Pins that are used for USB transceiver interfacing are chosen in accordance of the interface used, either 3-wire or 5-wire. All these pins except SINK1, 2, 3 and INP1, 2 can be used as ADC inputs.



Pin Functions

Table 1. Pin Descriptions

Name	Pin No.	Type(1)	Description
BATT	C1, D1	P	Main battery connection.
D-	E1	A	USB Differential Data Line (-) Input/Output.
D+	F1	A	USB Differential Data Line (+) Input/Output.
DATA/VP(2)	G2	DI/O	Data input/output for 3 wire USB transceiver/ USB Interface Plus Input/Output for 5 wire USB. If OE_N = HIGH, VP is a receiver output (+), If OE_N = LOW, VP is a driver input (+).
FB_B1	H1	A	Buck1 Feedback.
FB_B2	H3	A	Buck2 Feedback.
FB_B3	H5	A	Buck3 Feedback.
GND	E5	G	Ground
GND_B1	H2	G	Power Ground for Buck1.
GND_B2	G4, H4	G	Power Ground for Buck2.
GND_B3	G6, H6	G	Power Ground for Buck3.
GND_SINK	F7	G	Ground of GPIO current sink.
HF_PWR	D4	DI	Input for triggering startup. Power up sequence starts when this pin is set HIGH. Internal 500 kΩ pulldown resistor.
INP1(3)	F5	A	Comparator 1 input
INP2(3)	F6	A	Comparator 2 input
IRQ_N	G5	DO	Interrupt output, active LOW. Open Drain output, external pull up resistor is needed, typ. 10 kΩ.
LDO_UPWR	B5	A	Internal supply output, fixed to 1.8V. Can be loaded externally, max 30 mA.
LDO1	A5	A	LDO1 Output
LDO10	G9	A	LDO10 Output
LDO11	H9	A	LDO11 Output
LDO12	J9	A	LDO12 Output
LDO13	J7	A	LDO13 Output
LDO2	A7	A	LDO2 Output
LDO3	A8	A	LDO3 Output
LDO4	B8	A	LDO4 Output

(1) A = Analog Pin, D = Digital Pin, I = Input Pin, DI/O = Digital Input/Output Pin, G = Ground, O = Output Pin, P = Power Connection
(2) Pins that can be programmed as analog pins (default as stated in pin configuration) or digital input/output pins. Pins that are used for USB transceiver interfacing are chosen in accordance of the interface used, either 3-wire or 5-wire. All these pins except SINK1, 2, 3 and INP1, 2 can be used as ADC inputs.
(3) Pins that can be programmed as analog pins (default as stated in pin configuration) or digital input/output pins. Pins that are used for USB transceiver interfacing are chosen in accordance of the interface used, either 3-wire or 5-wire. All these pins except SINK1, 2, 3 and INP1, 2 can be used as ADC inputs.

Table 1. Pin Descriptions (continued)

Name	Pin No.	Type(1)	Description
LDO5	A9	A	LDO5 Output
LDO6	C9	A	LDO6 Output
LDO7	D9	A	LDO7 Output
LDO8	C8	A	LDO8 Output
LDO9	F9	A	LDO9 Output
OE_N(3)	E2	DI	USB Output Enable input. Active LOW enables the transceiver to transmit data onto the bus. A HIGH input enables receive mode.
OSC_32KHZ(3)	D3	DO	Buffered 32 kHz clock signal output.
PS_HOLD	H7	DI	Control input for Power Up/Power Down sequences of PMU. Internal 500 kΩ pulldown resistor by EEPROM default. Can be configured as pullup as well.
PWR_ON	B3	DI	Power button input. Power up sequence starts when this pin is set HIGH. Internal 500 kΩ pulldown resistor.
RCV(3)	E3	DO	Receive Data: Single ended output from USB differential data lines for 5 wire USB.
REF_OUT	H8	A	2.5V Reference output
RSENSE(3)	F4	A	Sense resistor input pin for charge/discharge current measurement
RSTIN_N	B7	DI	Reset button input, active low. Internal 500 kΩ pullup resistor.
RSTOUT_N	C6	DO	Reset output, active low. Pin stays LOW during power up sequence.
SCL	F3	DI	Serial interface clock input; requires external pullup, 1.5 kΩ typ.
SDA	G3	DI/O	Serial interface bi-directional data; requires external pullup, 1.5 kΩ typ.
SEO/M(4)	F2	DI/O	Data input/output for 3 wire USB transceiver/ USB Interface Minus Input/Output for 5 wire USB. If OE_N = HIGH, VM is a receiver output (-), If OE_N = LOW, VM is a driver input (-).
SEL	D5	DI	Select input for default option at power up
SIM_CLK(4)	D7	DO	SIM card connection. Level shifted clock signal to SIM
SIM_CLK_IN(4)	E7	DI	SIM clock input from Baseband Processor
SIM_DATA(4)	E8	D	SIM data input/output from Baseband Processor
SIM_IO(4)	D8	D	SIM card connection. SIM Card Data input/output
SIM_RST(4)	D6	DO	SIM card connection. Level shifted reset signal to SIM
SIM_RST_IN(4)	E6	DI	SIM reset input from Baseband Processor
SINK1(4)	G8	A	Current sink input 3.
SINK2(4)	F8	A	Current sink input 2.
SINK3(4)	G7	A	Current sink input 3.
SLEEP_N (TCXO_EN)	C7	DI	Sleep mode input, active low. Internal 500 kΩ pullup resistor by EEPROM default. Can be configured as pulldown as well.
SPND(4)	E4	DI	USB Suspend mode control input for 5 wire USB. A logical high at SUSPEND will power down the differential receiver and VP and VM will remain active with reduced current consumption.
SW_B1	J2	A	Buck1 Output.
SW_B2	J4	A	Buck2 Output.
SW_B3	J6	A	Buck3 Output.
TCXO1_I(4)	B6	A	TCXO1 buffer input.
TCXO1_O(4)	C3	DO	Buffered and validated TCXO1 output clock signal.
TCXO2_I(4)	C5	A	TCXO2 buffer input.
TCXO2_O(4)	C4	DO	Buffered and validated TCXO2 output clock signal.
USB_GND	G1	G	USB Ground
VCOIN	B4	A	Back up battery Charger Output. Connection of external coin cell (2.5 or 3.0V).
VDD	A1, B1	P	Output for system power.
VIN_B1	J1	P	Input for Buck1

(4) Pins that can be programmed as analog pins (default as stated in pin configuration) or digital input/output pins. Pins that are used for USB transceiver interfacing are chosen in accordance of the interface used, either 3-wire or 5-wire. All these pins except SINK1, 2, 3 and INP1, 2 can be used as ADC inputs.

Table 1. Pin Descriptions (continued)

Name	Pin No.	Type(1)	Description
VIN_B2	J3	P	Input for Buck2
VIN_B3	J5	P	Input for Buck3
VIN_CHG	A2, B2, C2	P	DC power input to charger block from wall, car power adapter or USB. Requires 1µF capacitor to ground.
VIN1	A6	P	Input for LDOs
VIN2	B9	P	Input for LDOs
VIN3	E9	P	Input for LDOs
VIN4	J8	P	Input for LDOs
VTRM	D2	A	USB Reference supply output (3.3 V). Requires 1µF capacitor to GND for stability. LDO14
XIN	A3	A	External Crystal Oscillator In
XOUT	A4	A	External Crystal Oscillator Out

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1) (2)(3)

VINCHG to GND	−0.3V to +28V
BATT, VIN_B1, VIN_B2, VIN_B3, VCOIN, VIN1, VIN2, VIN3, VIN4	−0.3V to +6V
SEL	−0.3V to +2V
Other input-only pins	0.3V to +6V
Junction Temperature (4)	150°C
Storage Temperature	−65°C to +150°C
Maximum continuous power dissipation	See (4)
VIN_CHG, BATT, HF_PWR, PWR_ON, RSTIN_N, D+, D-, RSENSE, SIM_IO, SIM_CLK, SIM_RST, GND_USB (5)	8kV HBM
All other (5)	2kV HBM

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J=130°C (typ).
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1) (2)

VIN_CHG	4.5V to 6.5V
BATT, PRSW, VIN_B1, VIN_B2, BIN_B3	3.0V to 4.5V
VCOIN	1.9V to 4.5V
VIN1, VIN2, VIN3	2.5V to 4.5V
VIN4	1.0V to 4.5V
Junction Temperature Range	−40°C to +125°C
Maximum Ambient Temperature (3)	−40°C to +85°C
Maximum power dissipation (3)	1.72W
Package Thermal Resistance θ_{JA}	32°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) The Maximum power dissipation depends on the ambient temperature and can be calculated using the formula $P = (T_J - T_A)/\theta_{JA}$ where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 1.72W rating appearing under Maximum Ratings results from substituting the Maximum junction temperature, 125°C, for T_J, 70°C for T_A, and 32°C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70°C. Less power can be dissipated safely at ambient temperatures above 70°C. The Maximum power dissipation can be increased by 31 mW for each degree below 70°C, and it must be de-rated by 31 mW for each degree above 70°C.

General Electrical Characteristics

Typical values and limits appearing in normal typeface are for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation T_J = −40°C to +125°C). Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
UNDER VOLTAGE LOCK-OUT						
UVLO	Range-to-range accuracy	V_{IN} Rising; UVLO LEVEL programmed to 3.10V		3.0	3.25	V
LOGIC AND CONTROL INPUTS						
V_{IL}	Input low level	SDA (2), SCL (2), OE_N, DATA/VP, SEO/VM, SPND			**0.25 × V_{LDO1}**	V
		PWR_ON, RS_HOLD, SLEEP_N, HF_PWR, RSTIN_N			**1.08**	
V_{IH}	Input high level	SDA (2), SCL (2), OE_N, DATA/VP, SEO/VM, SPND		**0.75 × V_{LDO1}**		V
		PWR_ON, RS_HOLD, SLEEP_N, HF_PWR, RSTIN_N		**1.32**		
V_{IL}	Multifunctional pins low level	When configured as logic inputs.			0.6	V
V_{IH}	Multifunctional pins high level			1.6	3.0	
I_{LEAK}	Input current	SEL input between 0V and 1.8V.		**−5**	**+5**	µA
		Other logic inputs without internal pullup or pulldown resistors between 0V and V_{DD} at 3.6V.				
R_{IN}	Input resistance	PWR_ON, HF_PWR, PS_HOLD, RSTIN_N, SLEEP_N (TXCO_EN) pullup or pulldown resistors (if configured)	500			kΩ

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Specified by design.

General Electrical Characteristics (continued)

Typical values and limits appearing in normal typeface are for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation T_J = −40°C to +125°C). Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
LOGIC AND CONTROL OUTPUTS						
V_{OL}	Output low level	RSTOUT_N, RCV, DATA/VP, SEO/VM, IRQ_N I_{OUT} = 2mA			**0.25 × V_{LDO1}**	V
		SDA (3)			**0.25 × V_{LDO1}**	
V_{OH}	Output high level	RCV, DATA/VP, SEO/VM I_{OUT} = 2mA		**0.75 × V_{LDO1}**		V
I_{OH}	Output high leakage	SDA (3), RSTOUT_N, IRQ_N V_{OH} = V_{LDO1}			**10**	µA

(3) Specified by design.

Current Consumption

Current consumption of the LP3925 PMU has been one of the main features this device is famous for. It is mainly because of ultra low I_Qs in sleep and standby modes the LP3925 can ensure dramatic power savings and prolong battery life for enormous amount of time. Due to such a significant advantage in these critical factors, an LP3925 is very convenient to use in innovative and environmentally friendly designs, giving the end user the possibility of increased consumer device working time and thus a crucial advantage of the rapidly developing mobile market.

The quiescent currents in standby and sleep modes are stated in the Current Consumption Electrical Characteristics.

Current Consumption Electrical Characteristics

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
CURRENT CONSUMPTION						
$I_{Q(STANDBY)}$	Battery Standby Current	V_{IN} = 3.6V I_{COIN} = 0µA	3.5			µA
$I_{Q(SLEEP)}$	Battery Current in SLEEP mode at 0 load	LDO1 ON	60			

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

DEVICE OPERATING MODES

POWER-ON-RESET: All internal registers are reset to default values. This is the default state after applying power to the PMU, duration 1ms.

STANDBY: All functions disabled (except RTC power management); PMU is in low power mode.

START UP: Startup sequence is triggered by setting PWR_ON input high for 100 ms or by setting HF_PWR input high for 100 ms or by connecting a suitable voltage to charger input. For MPL or RTC ALARM events the startup sequence begins after 2ms delay from the MPL or RTC ALARM events. During the sequence the regulators on PMU are enabled according to a pre-programmed timing pattern. If the regulators are enabled, RSTOUT_N is released, allowing the application processor to start up. PS_HOLD must be set high in 1.5 seconds from the start of STARTUP. The input signal witch activates startup must stay on until PS_HOLD asserted. If PS_HOLD is not asserted in 1.5 seconds then SHUTDOWN is initiated. For PWR_ON startup there is no 1.5 seconds limit.

IDLE: PMU goes to normal working mode, if PS_HOLD is pulled HIGH after releasing RSTOUT_N. In this mode all features and control interfaces are available to the user. Chip temperature over TSDH, VDD voltage below UVLO, PS_HOLD going low for 10 ms or a flag failure in a monitored regulator for 10 ms will cause the PMU to go to SHUTDOWN state.

SLEEP: PMU goes to SLEEP state from IDLE state, if SLEEP_N input is pulled low. In this mode PMU current consumption is minimized to extend device's standby time. Load on regulators and bucks should stay below 5mA each. Conditions of going to SHUTDOWN state are the same as in IDLE state.. SLEEP Mode is controlled by the Serial Interface.

SHUTDOWN: In this state RSTOUT_N is pulled LOW and all regulators are disabled according to pre-programmed timing pattern. After this, all registers are reset to default values, and PMU goes to STANDBY state.

SYSTEM RESET: PMU goes to SYSTEM RESET mode if RSTIN_N input has been pulled low for 33 ms. In this mode RSTOUT_N output is pulled low and user registers are reset. After a pre-programmed time delay RSTOUT_N is released, allowing the application processor to start up. During SYSTEM RESET, the LP3925's always-on power rail will not drop to zero. If for some reason PS_HOLD is pulled down during reset, it must come back up within 1.5s of the beginning of system reset. If EN RSTIN SHUTDOWN bit is high then the reset sequence is similar to shutdown and will startup again only if EN RSTIN STARTUP bit is high.

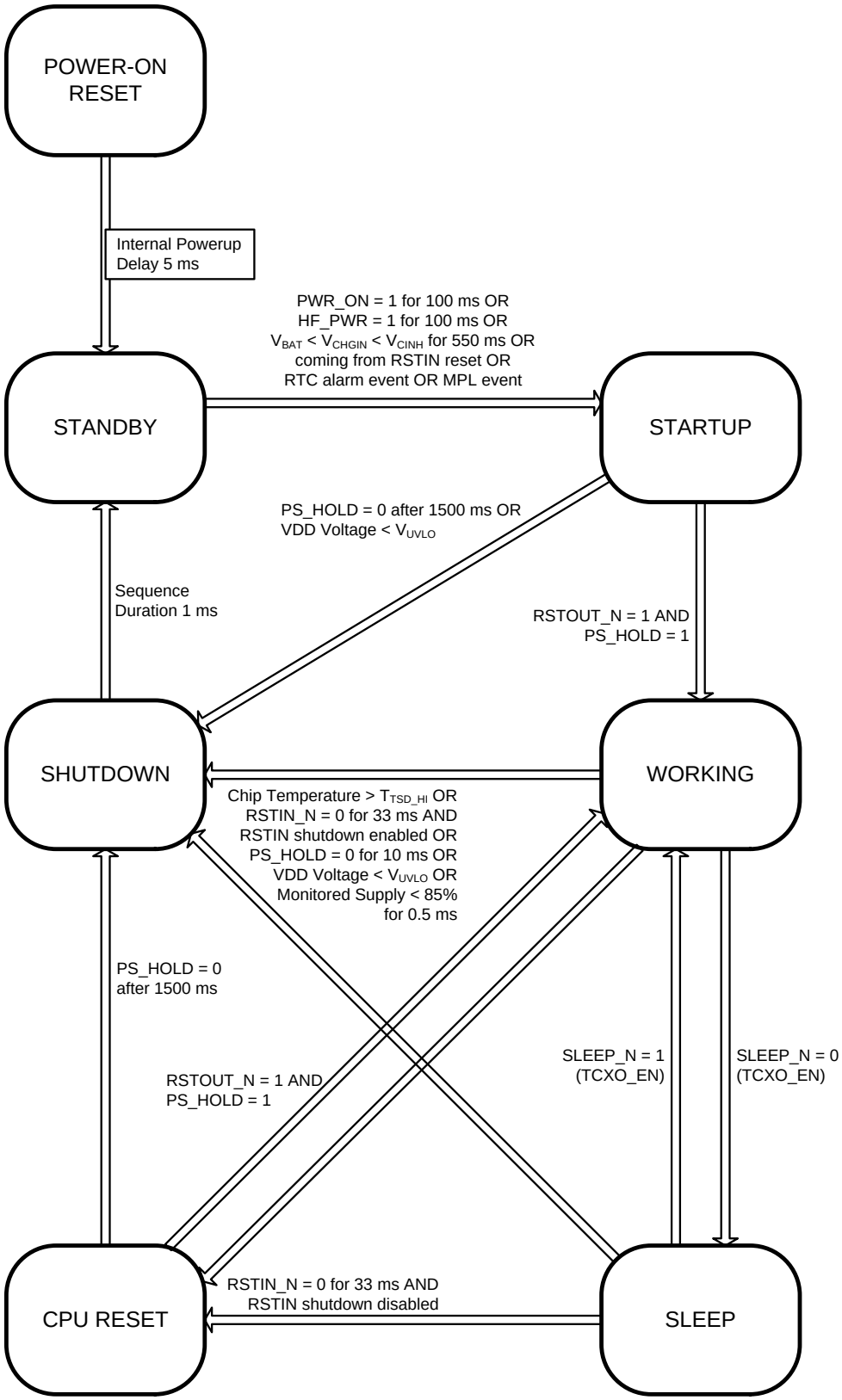


Figure 2. Device Operating Modes

STARTUP AND SHUTDOWN SEQUENCES

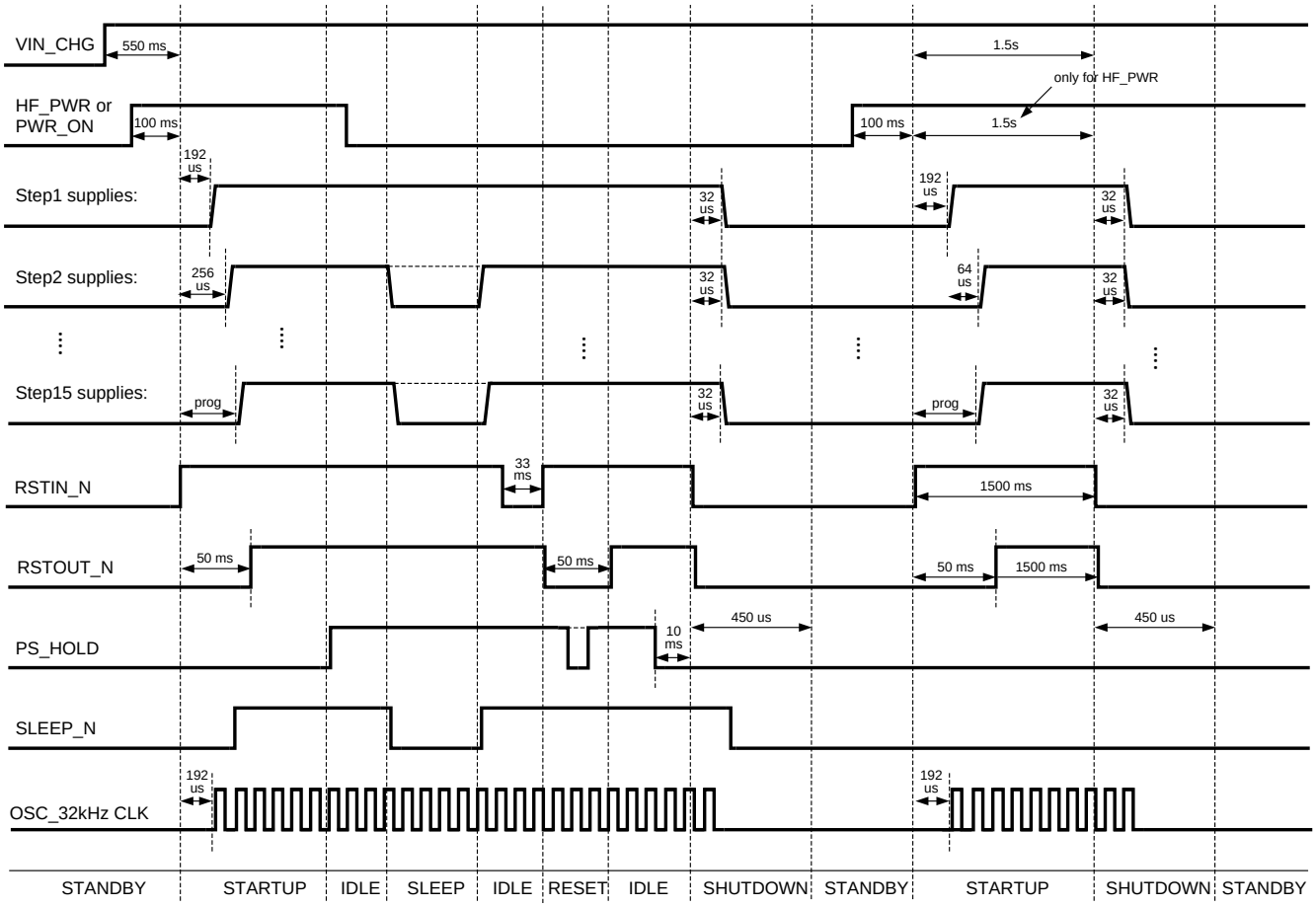


Figure 3. Startup and Shutdown Sequences

The default, factory-programmed power-up sequence of the PMU can be seen in Figure 3. Startup sequence is triggered by setting PWR_ON or HF_PWR input high for 100 ms or after 500 ms is passed from the connection of a suitable voltage to the charger input. Once this time has expired, the start-up time slots begin. The programmable values of the startup and shutdown time slots are available in the Default Operating Settings section at the end of the datasheet. If the Idle state has been reached from the Startup state, all regulators that are enabled are on, and their outputs are defined by their programmed register values. 450 µs in startup/shutdown diagram is the time needed for system to perform a shutdown event.

NOTE

All the timings are limited by an internal oscillator's accuracy. Please contact TI sales for default EEPROM setting details.

ENABLE CONTROL

LP3925 provides much flexibility in enabling/disabling on-chip features. The blocks that have advanced enable controls include: LDOs, buck regulators, USB transceiver, TCXO buffers, SIM level shifter. Each block has a 4-bit code in registers, which selects the enable signal for that block. These codes are in register addresses 0x37...0x41, with bit names ending with CONTROL. The enable signal translation table is stated below.

In order to make the control more flexible, there is a possibility for the blocks to be enabled through registers 0x00…0x02 or through multifunctional pins. One control signal can enable any number of features. This allows to group signals so, that any end-system function can be switched on with only one input or register write.

There are additional enable controls for sleep mode operation with ALLOW IN SLEEP bits in register addresses 0x34...0x36. If a block is not allowed in sleep mode, then this block is always off during sleep. If a block is allowed in sleep mode, then it is controlled by its selected enable signal, and does not depend on sleep mode.

Example 1:

Goal: Buck2 is always disabled in sleep mode and enabled in idle mode.

Best solution: write BUCK2 CONTROL to '0001' and ALLOW BUCK2 IN SLEEP to '0'; now Buck2 is enabled in working mode and disabled in sleep mode, with no separate enable bit/input.

Example 2:

Goal - Enable LDO9, LDO10 and TCXO buffer1 together with one register write.

One possible solution: write LDO9 CONTROL, LDO10 CONTROL and TCXO1 CONTROL to 0010; now writing '11' to address 0x00 bits [1:0] enables all three blocks.

MULTIFUNCTIONAL PINS

Some pins corresponding to 32 kHz oscillator, USB transceiver, SIM interface, TCXO buffer, current sink and comparator blocks along with RSENSE pin are multifunctional pins, which means that they can be programmed as analog function pins, ADC inputs or digital input/output pins. These pins can be configured from registers 0x19..0x23.

If one block uses more than one pin, then all the pins must be configured for the block to work. For example, all 6 SIM level shifter pins must have level shifter function selected, before the block is connected to the pins. To use USB with 4- or 5-wire interface, the used pins must all be configured as 5-wire USB pins. For 3-wire interface the 3 pins must all be configured as 3-wire USB pins.

Some GPIO functions have separate enable controls. These enables will take the blocks to a shutdown state, but will not disconnect them from the pins. The GPIO configuration options are described in Table 2.

Table 2.

Pin/Code	1000	1001	1010	1011	1100	1101	1110	1111
OSC_32 KHZ	32 kHz OSC							
RSENSE	N/A	Maximum measurable voltage drop on sense resistor						
		12 mV	26.4 mV	39.6 mV	56.4 mV	81.6 mV	98.4 mV	120 mV
SIM_RST_IN	SIM RST, baseband side							
SIM_CLK _IN	SIM CLK, baseband side							
SIM_DATA	SIM I/O, baseband side							
SIM_RST	SIM RST, SIM side							
SIM_CLK	SIM CLK, SIM side							
SIM_IO	SIM I/O, SIM side							
TCXO1_I	TCXO1 warmup time before output enable							
	1µs		21 µs		41 µs		61 µs	
TCXO1_O	TCXO1 output driver strength							
	x8		x4		x2		x1	
TCXO2_I	TCXO2_I warmup time before output enable							
	TCXO2in wait=1µs		TCXO2in wait=21 µs		TCXO2in wait=41 µs		TCXO2in wait=61 µs	
TCXO2_O	TCXO2 output driver strength							
	TCXO2out strength=1		TCXO2out strength=2		TCXO2out strength=4		TCXO2out strength=8	
OE_N	OE_N: 3-pin USB interface				OE_N: 5-pin USB interface			
DATA/VP	DATA: 3-pin USB interface				VP: 5-pin USB interface			
SEO/VM	SEO: 3-pin USB interface				VM: 5-pin USB interface			
RCV	N/A				RCV: 5-pin USB interface			
SPND	N/A				SUSP: 5-pin USB interface			
INP1	Comparator1 input comparison threshold							
	0.4V	0.6V	0.8V	1.0V	1.2V	1.5V	1.8V	2.4V
INP2	Comparator2 input comparison threshold							
	0.4V	0.6V	0.8V	1.0V	1.2V	1.5V	1.8V	2.4V
SINK1	Current sink1 max current output							
	31mA	63 mA	94 mA	125 mA	156 mA	188 mA	219 mA	250 mA
SINK2	Current sink2 max current output							
	13 mA	25 mA	38 mA	50 mA	63 mA	75 mA	88 mA	100 mA
SINK3	Current sink3 max current output							
	13 mA	25 mA	38 mA	50 mA	63 mA	75 mA	88 mA	100 mA

SINGLE-INPUT LINEAR CHARGER WITH PMOS ROUTING SWITCH

LP3925 has a built-in Li-Ion/Li-Poly battery management system. Its main features are:

- One input with many current limit options to accommodate different USB and adapter types
- Separate supply branches for battery and system
- Integrated power routing switch
- Charging cycle with precharge, constant current and constant voltage modes
- Selectable battery regulation voltage to accommodate different batteries
- Selectable system regulation voltage
- Wide array of battery charging current options
- Flexible charging cycle control
- Temperature monitoring to avoid overheating
- Selectable safety timer

GENERAL CHARGER CONTROL

The charger control is divided into two separate parts: battery charging and system supply.

Battery charging part of the charger measures battery voltage and current. Based on this data, it makes the decisions about starting or ending battery charging and choosing the right current.

System supply part monitors the power consumption by the external system, ensures that the system supply is stable and that the charger input is not overloaded. These systems work independently from each other.

If the power routing switch is OFF (non-conducting), then they can be viewed as two separate systems. The only dependence between the two is, that battery charging current can be reduced, if the system requires more current from the input. If the power routing switch is turned ON, then the two algorithms still work independently, but the system supply part is in control of the whole charger. The battery charging part is in the situation, that it still does make battery charging cycle decisions, but these do not affect the actual charging.

If the switch is turned OFF again, then the two systems keep on working separately.

CHARGER INPUT DETECTION AND LIMITS

Input detection is implemented with 2 comparators. One compares the input voltage to the lower limit of the working range, the other to the higher limit of the working range. If the input voltage is between these two levels, then the charger is allowed to work.

The lower limit of input's working range is V_{BATT}+200 mV, with an option to add a 4.2V minimum requirement. The higher limit of input's working range can be one of the following values: 6.15V, 6.64V, 7.18V, 7.71V, 10.28V, 15.38V, 18.45V or disabled. To get the exact information about your product, please refer to the Datasheet Addendum document.

The charger is capable of limiting input current, allowing to accommodate different voltage sources (wall adapters, USB, etc). IDCIN bits set the maximum input current. The sum of system supply and battery charging currents will not go over this limit during normal operation. For correct operation, IDCIN should be set to 235mA or more above IBATT (though this margin can be reduced for IDCIN below 500 mA; e.g. down to 85 mA at IDCIN = 135 mA). High current mode ignores the input current limit.

Some of the GPIO pins can be configured as a dedicated charger input status signal output. This signal is low, if charger input is in working range. The 'Inverted VDCIN' configuration details are in the GPIO chapter of the datasheet.

SYSTEM SUPPLY FUNCTION

system supply regulator starts to regulate voltage on VDD pin. The voltage is selectable with VDD control bits. System voltage regulator will work as long as charger input is in working range. The only exception is the case, where PMU is in standby mode and system supply is configured off in standby.

Because system and battery are supplied from separate branches, the VDD and BATT voltage levels can be different. This means, that the selected voltage can be supplied to VDD and the PMU can fully operate, while the battery is deeply discharged and the charger is in pre-charge mode. In that case the system should not use modes, which will require more current, than the input can provide.

System supply is with higher priority than battery charging. This means that if the sum of system and battery currents starts to go over the input limit, then battery charging current will be reduced to stay within the input loading limit.

If the system supply reaches the selected input current limit, then the power routing switch will be turned ON. This will connect the battery to the system, which will provide the extra power needed. Also, the system supply current limit will change from input current limit (IDCIN bits) to battery current limit (I_{BATT} bits). This ensures, that if the system load drops, then the battery will not be charged with too large current.

In some systems it may be practical to disable the input current limit, so the system can draw more than 1.2A without turning the switch ON. The SYSTEM SUPPLY CURLIM OFF bit can be used for this purpose. Warning: continuous high current draw from the input may cause the PMU to shut down because of high temperature. There is a configuration option for the system supply during PMU's standby mode. The selection for a specific product is shown in Datasheet Addendum document.

This option has following behavior:

a) supply on during PMU standby: VDD is supplied from BATT via switch (if charger is not working) or from system supply branch (if charger is working).

b) supply off during PMU standby: VDD is isolated from BATT pin during PMU standby and system supply branch is disabled.

BATTERY CHARGING FUNCTION

LP3925 has a safe and smart Li-Ion/Li-Poly battery charge management system, keeping the number of battery charging cycles to a minimum and thus increasing battery lifetime.

Following the correct detection of a voltage at the charger input, the charger enters precharge mode. In this mode the battery is charged with a small constant current. Precharge settings are available in register 0x82 and these values are remembered as long as the PMU has power. CHARGER IPRECHARGE bits select the battery current in precharge mode. It should be noted, that value '00' disables precharge current completely.

CHARGER VFULLRATE bits select the level, from which the battery can be charged with full charging current. If battery voltage reaches that level, then the charger will move on to full charging mode. CHARGER TPRECHARGE sets the maximum precharge time, after which the battery will be isolated, protecting it from further charging.

In full charging mode full rate constant current is applied to the battery, to raise the voltage to the termination level (selected by VTERM bits). The maximum charging current is selectable via IBATT bits, but the actual current can be lower than this limit, depending on the load of system branch. When termination voltage is reached, the charger enters constant voltage mode and a constant voltage is maintained. Now charging current is monitored to detect the end-of-charge condition. After reaching this condition, charger disables the battery charging branch and enters standby mode. FULL TIMEOUT sets the maximum full charge duration, after which the charging will be ended automatically. Then the charger enters standby mode, where the battery is isolated and the charger monitors battery voltage. If restart conditions have been met, then the charging cycle is re-initiated to re-establish the termination voltage level.

In standby mode the battery is isolated and the charger monitors battery voltage.

CC TO CV MODE TRANSITION

CC to CV mode transition is shown on Figure 9. The voltage level of charging mode change (CC to CV) is dependent on both V_{TERM} (0x47, bit3-0) and I_{BATT} (real charging current) settings, equation shows below:

$$V_{CCtoCV} = V_{TERM} - (I_{BATT}*0.05) \quad (1)$$

where 0.05 stands for charger's internal resistance. This equation is valid only when the power routing switch is in non conducting state and the charging is done through charger's branch. When the switch is ON, the charging is done through the supply branch, and the internal resistance in the equation is replaced by the power routing switch's ON resistance. Note that the I_{BATT} current in equation is the real battery charging current which may differ from the programmed one.

USER can use ADC to measure charging current and BATT pin voltage.

END-OF-CHARGE AND RESTART

Ending and re-starting the charging cycle can be accomplished in multiple ways.

Automatic control can be enabled with AUTOMATIC START/STOP bit. If this bit is '0', then the charging cycle can only be controlled manually. Writing this bit to '1' enables fully automatic cycle control.

Manual control is always available via STOP CHARGING and START CHARGING bits. These control bits are write-only and not tied to any internal monitoring, allowing to start and stop charging at any time. Only one of these bits must be written to '1' at once.

Automatic control utilizes internal battery monitoring, which can be configured trough control registers.

Automatic end-of-charge requires that the battery has reached termination level. Then the charger starts monitoring battery charging current and comparing it to end-of-charge current (set by ABS EOC and EOC LEVEL bits). If the charging current is below this level for the duration of EOC TIME, then the automatic end-of-charge condition has been reached.

Automatic restart requires that one charging cycle has already been completed and the charger is in standby mode. Then the charger monitors battery voltage and compares it to restart level (set by RESTART LEVEL). If the battery voltage is below this level for the duration of RESTART TIME, then the automatic restart condition has been reached.

In manual-only mode it is possible to get automatic cycle control information via interrupts. CHARGE STOP INT is generated, if end-of-charge condition has been reached, and CHARGE START INT is generated, if restart condition has been reached).

POWER ROUTING SWITCH

This switch separates the battery from the system. This helps to conserve charge and reduce the count of charge-discharge cycles.

If charger input is not connected, then the switch is in ON (conducting) state.

In normal conditions the switch is OFF during charger operation. The switch will be turned ON, if the system load is greater than the charger can supply. This event also generates a SWITCH AUTO ON interrupt. If the switch is turned ON during charger operation, then it does not turn back OFF automatically. The only exception to that rule is, if the PMU enters standby mode. If the charger is operating and the switch is turned ON, then only system supply branch is working. Maximum output current is then set by I_{BATT} code, to avoid too high current into the battery.

If the charger is working, then power routing switch state can be controlled manually with SWITCH ON and SWITCH OFF command bits. It is advisable to use the SWITCH ON command before the system enters a mode, which draws more current than the input can provide. This will help to avoid voltage drop on VDD, before the internal overload detection reacts. If the system returns to low consumption mode, the SWITCH OFF command bit should be used to restore normal charger operation.

OPERATION WITHOUT BATTERY

The charger is not aware of battery presence, it always behaves by the same configuration. If the battery is not connected, then it is recommended to keep the battery charging part disabled. This can be done by disabling the restart timer and ending the charging with STOP CHARGING bit. Otherwise the charger will keep trying to regulate the voltage on BATT pin, causing frequent charging cycles.

HIGH-CURRENT MODE

If HIGH-CURRENT MODE bit is set, then the charger enters special high load mode. In this mode the power routing switch is set ON, input current limit is disabled, and the charger branches are working together. All charging cycle controls do not have any effect in high current mode.

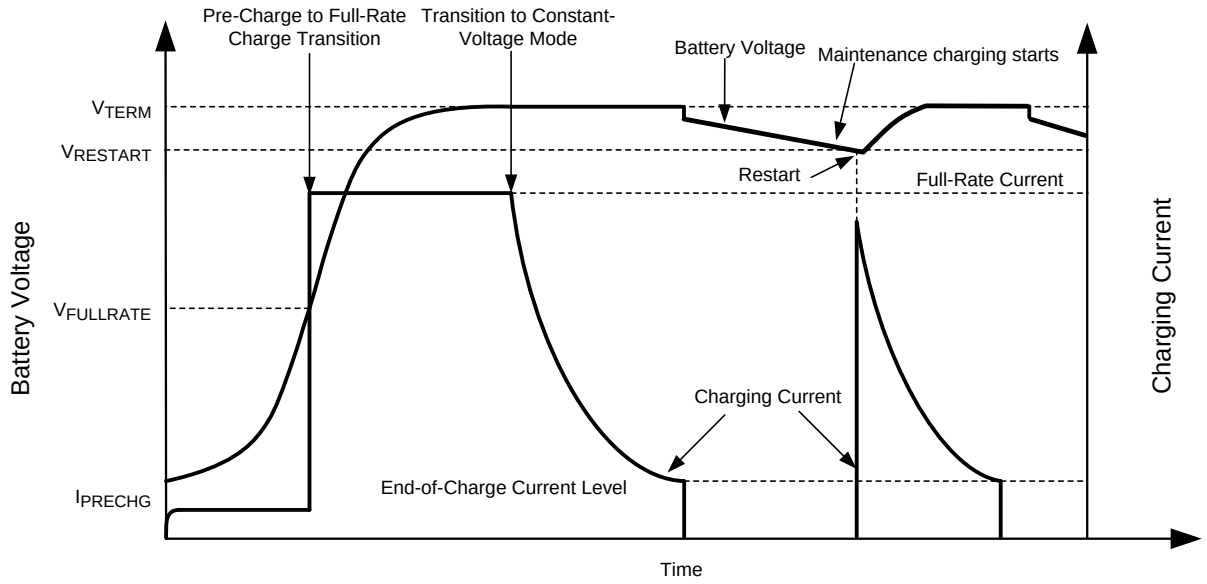


Figure 4. Charging Cycle Voltage and Current Plots

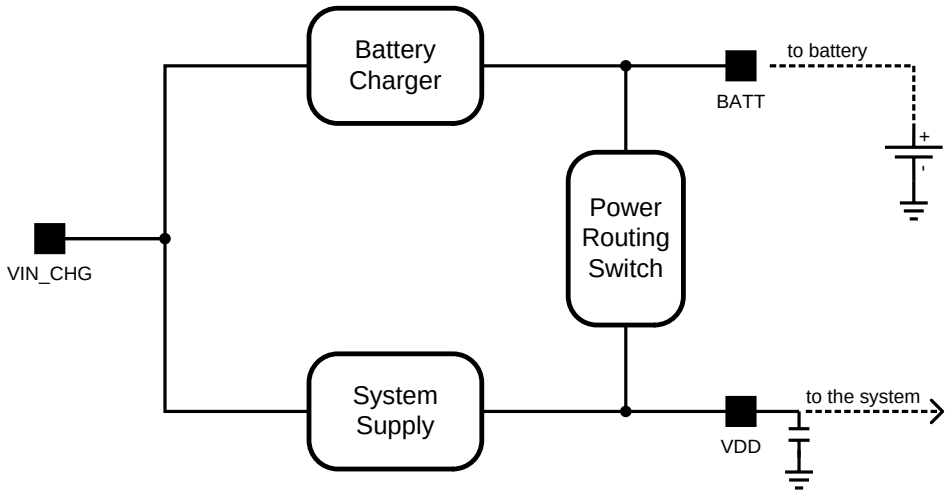
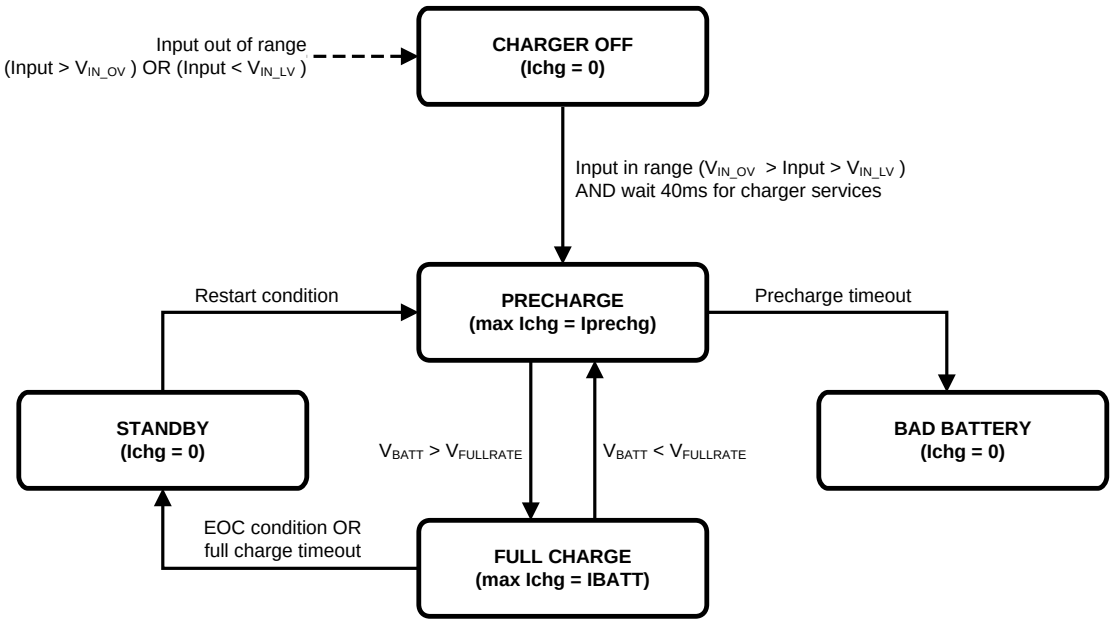


Figure 5. Charger Power Structure



Deglitching times:
- Charger input in range, rising edge: 50 ms
- Charger input in range, falling edge: 2 us
- Vfullrate, Vrestart, Ieoc: 400 ms

Figure 6. Charger Charging Cycle Operation Description

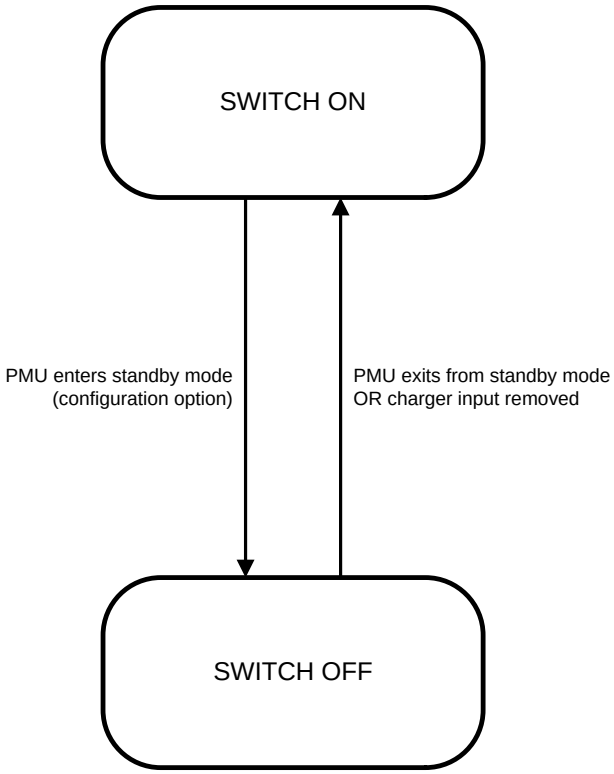


Figure 7. Charger Internal Power Switch Operation Description When Charger is Off

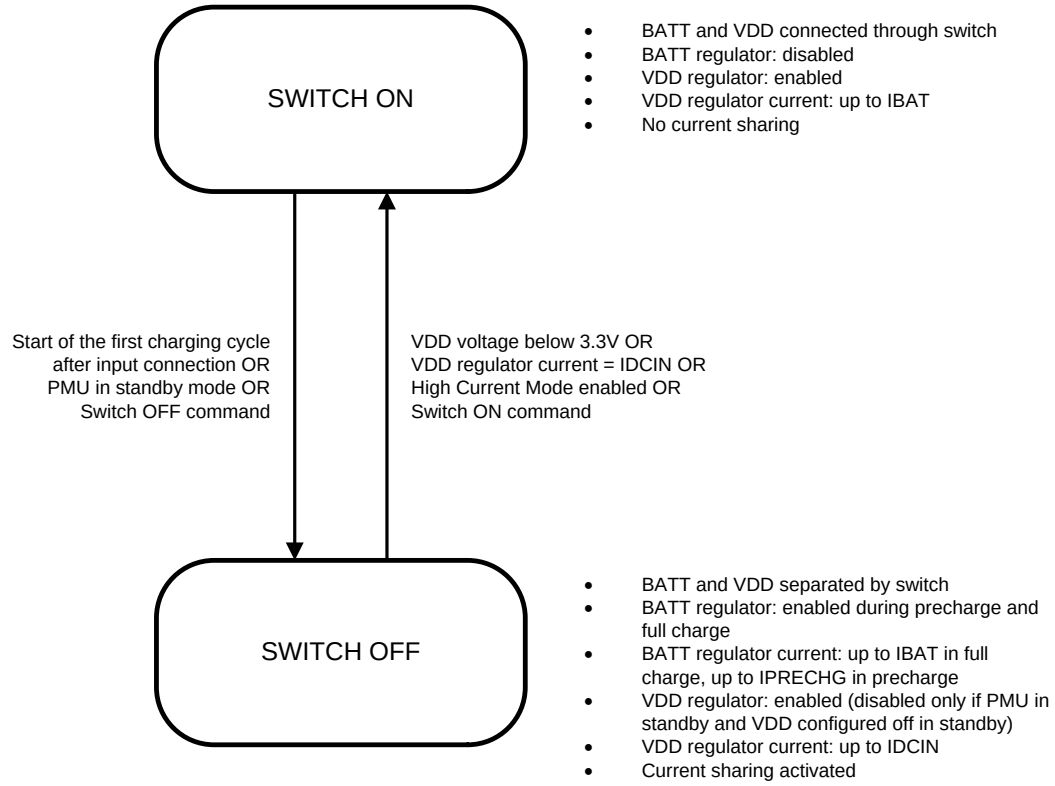


Figure 8. Charger Internal Power Switch Operation Description When Charger is On

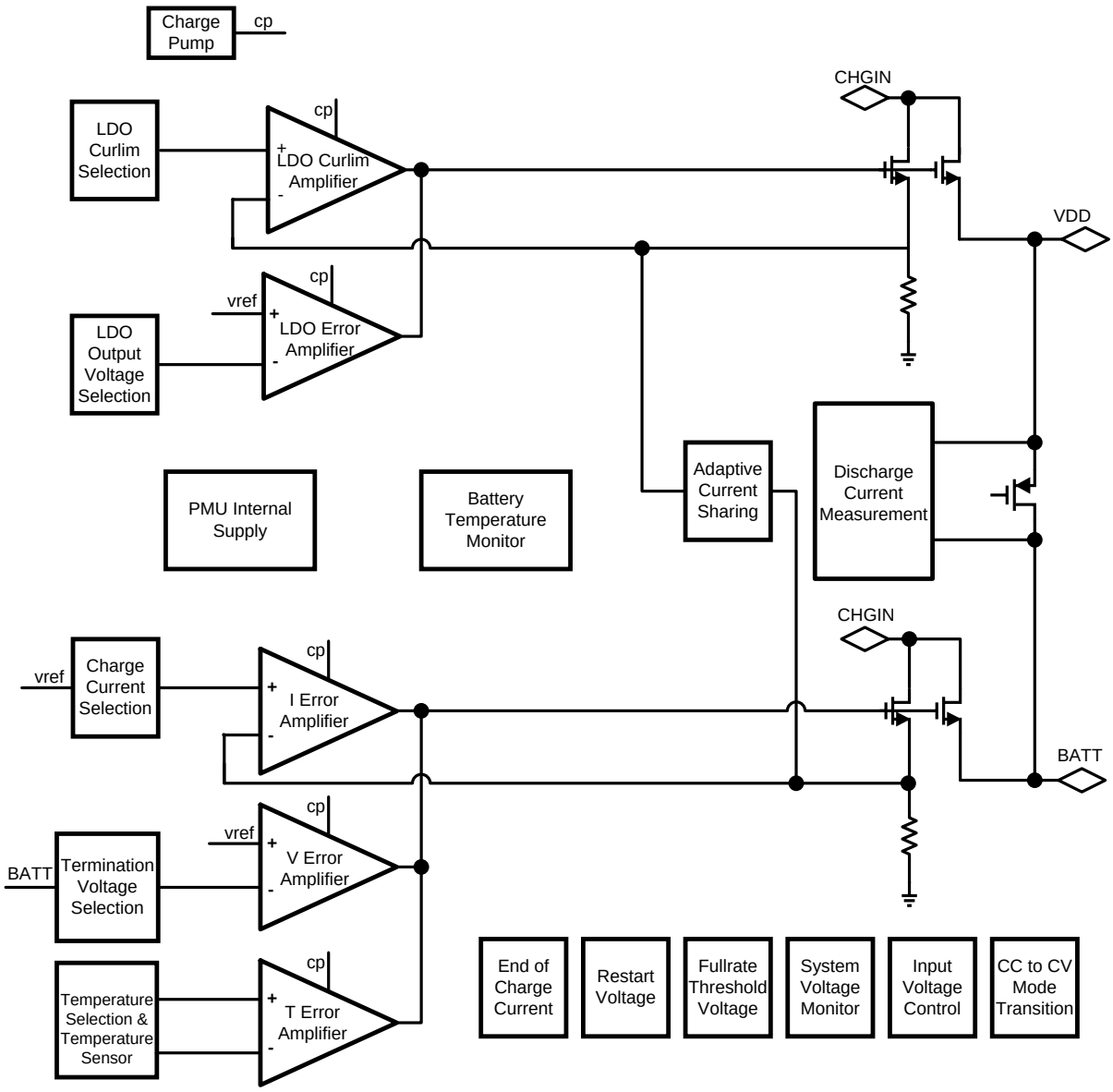


Figure 9. Charger Block Diagram

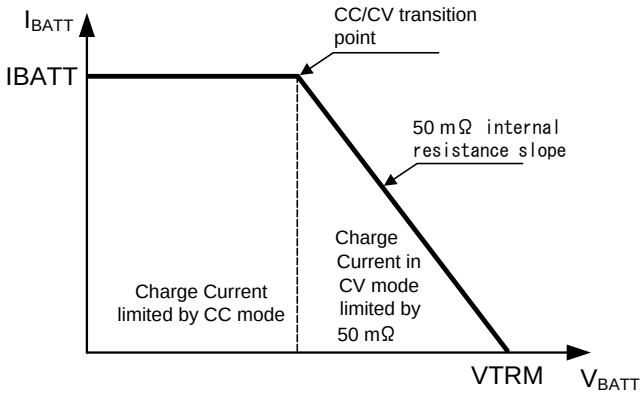


Figure 10. Charger CC to CV Mode Transition Diagram

CHARGER ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J =−25°C to +85°C. Unless otherwise specified, the following applies for V_{VIN_CHG} = 5.0V.(1) (2)

Symbol	Parameter	Test Conditions	Typ	Limit		Unit
				Min	Max	
V_{OV}	Over-Voltage Protection threshold	Charger input is turned off if voltage is above this threshold.	6.95	**6.55**	**7.4**	V
V_{VIN_CHG}	AC input voltage operating range			**4.5**	**6.5**	V
V_{OK_CHG}	VIN_CHG OK trip-point	V_{VIN_CHG} - V_{BATT} (Rising)	300			mV
		V_{VIN_CHG} - V_{BATT} (Falling)	90			
V_{TERM}	V_{TERM} voltage tolerance default	V_{TERM} = 4.2V, I_{CHG} = 50 mA		−0.35	+0.35	%
		V_{TERM} is measured at 10% of the programmed I_{CHG} current		**−1**	**+1**	
I_{CHG}	Programmable full-rate charge current	6.5V ≥ V_{VIN_CHG} ≥ 4.5V V_{BATT} < V_{VIN_CHG} − $V_{OK\_VIN\_CHG}$ V_{FULL_RATE} < V_{BATT} < V_{TERM}(1)		**50**	**1200**	mA
	Full-rate charge current tolerance	I_{CHG} = 100 mA (2)	100	**75**	**125**	mA
		I_{CHG} = 400 mA (2)	400	**350**	**450**	
		I_{CHG} = 600 mA	600	**540**	**660**	
		I_{CHG} = 1100 mA (2)	1100	**1040**	**1160**	
I_{PRECHG}	Pre-charge current	2.2V < V_{BATT} < V_{FULL_RATE}	50	**35**	**65**	mA
I_{DCIN}	Input current limit	IDCIN = 435 mA; IBATT = 200 mA		**−9**	**5**	%
$I_{VIN\_CHG\_MAX}$	Maximum input current in high-current mode	V_{VIN_CHG} - V_{DD} ≤ 0.8V (2)			2.3	A
V_{FULL_RATE}	Full-rate qualification threshold	V_{BATT} rising, transition from pre-charge to full-rate charging (2.8V option selected)	2.8	**2.7**	**2.9**	V
$V_{RESTART}$	Restart threshold voltage	From V_{TERM} voltage (4.2V, −150 mV options selected)	−150	**−180**	**−120**	mV

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.
(1) Specified for output voltages no less than 1.0V
(2) Specified by design.

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −25°C to +85°C. Unless otherwise specified, the following applies for V_{VIN_CHG} = 5.0V.(1) (1)

Symbol	Parameter	Test Conditions	Typ	Limit		Unit
				Min	Max	
T_{REG}	Regulated junction temperature	115°C option selected (2)	115			°C
DETECTION AND TIMING (2)						
T_{POK}	Power OK deglitch time	$V_{CHG} > V_{BATT} + V_{OK\_CHG}$	30			ms
T_{PQ_FULL}	Deglitch time	Pre-charge to full-rate charge transition	210			ms
T_{CHG}	Charge timer	Pre-charge mode (default setting)	45			mins
		CC mode/CV mode (default setting).	5			Hrs
T_{EOC}	Deglitch time for end-of-charge transition		210			ms

BUCK INFORMATION

The LP3925 has integrated three high efficiency step-down DC-DC switching buck converters that deliver a constant voltage from a single cell battery to portable devices. Using voltage mode architecture with synchronous rectification, the buck has the ability to deliver up to 800 mA depending on the input voltage and output voltage, ambient temperature, and the inductor chosen.

There are two modes of operation depending on the current required - PWM (Pulse Width Modulation), ECO (ECOnomy) mode. The device operates in PWM mode at load currents of approximately 50 mA (typ.) or higher. Lighter output current loads cause the device to automatically switch into ECO mode for reduced current consumption and a longer battery life. 2 buck regulators are capable of DVS control. Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection. Only three external power components are required for implementation.

BUCK CIRCUIT OPERATION

The switching buck converter operates as follows. During the first portion of each switching cycle, the control block in the LP3925 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of (VIN-VOUT)/L, by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $-V_{OUT}/L$.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. While in PWM mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

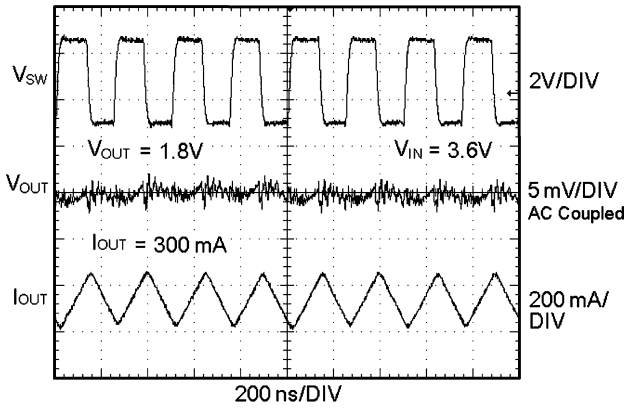


Figure 11. Typical PWM Operation

INTERNAL SYNCHRONOUS RECTIFICATION

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

CURRENT LIMITING

A current limit feature allows to protect itself and external components during overload conditions. PWM mode implements current limit using an internal comparator that trips at 1100 mA (typ.). If the output is shorted to ground and output voltage becomes lower than 0.3V (typ.), the device enters a timed current limit mode where the switching frequency will be one fourth, and NFET synchronous rectifier is disabled, thereby preventing excess current and thermal runaway.

ECO MODE OPERATION

The buck switches from ECO state to PWM state based on output load current. At light loads (less than 50mA), the converter enters ECO mode. In this mode the part operates with low Iq. During ECO operation, the converter positions the output voltage slightly higher (+30mV typ.) than the nominal output voltage in PWM operation. The more complete understanding of an ECO mode operation can be derived from diagram in Figure 12.

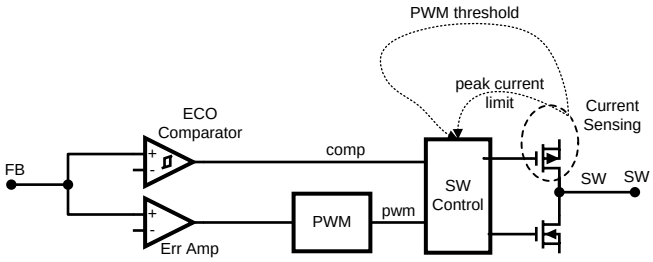


Figure 12. Typical ECO Operation

Power FETs are controlled by “SW Control” which is a combination of ‘comp’ and ‘pwm’ signals, dependent on ‘PWM threshold’ level. “ECO Comparator” is a simple comparator with hysteresis. “Err Amp” and “PWM” are error amplifier with a ramp generator. ‘PWM threshold’ is current sensing at PFET, that lets control logic know which input has to be used. In low load condition ‘comp’ is used and in high load condition ‘pwm’ is used. Once Vout voltage level gets too small, then in low load condition (ECO mode) the “ECO Comparator” triggers and “SW Control” opens PFET (wide pulse at SW pin; see Figure 3). The wideness of that pulse is determined by “ECO comparator” which has a built in hysteresis. Normal in ECO mode after that wide pulse has passed no action should be taken, until next “ECO Comparator” triggering. If some other condition (PWM threshold/Current limit) is fulfilled, then buck enters PWM mode.

If ‘peak current limit’ which is a current sensing signal for PFET’s switch peak currents triggers, then buck enters PWM mode from the next clock pulse. Peak current sensing is reset at the beginning of every clock pulse. Once in PWM mode, buck will stay there at least 32 clock pulses and if ‘PWM threshold’ indicates that buck should be operating in ECO mode, it will return into ECO mode. This is what actually happens on Figure 3 during wide ECO mode pulse. (The reason behind that is in high peak current during the time PFET is opened. Rough example:

$$I = \frac{c * v}{t} = \frac{10^{-5} * 5 * 10^{-2}}{0.35 * 10^{-6}} = 1.4A$$

Figure 13. Buck's Switches Controlling Diagram

where C_{OUT} = 10 µF, ripple V = 50 mV and PFET open time = 350 ns).

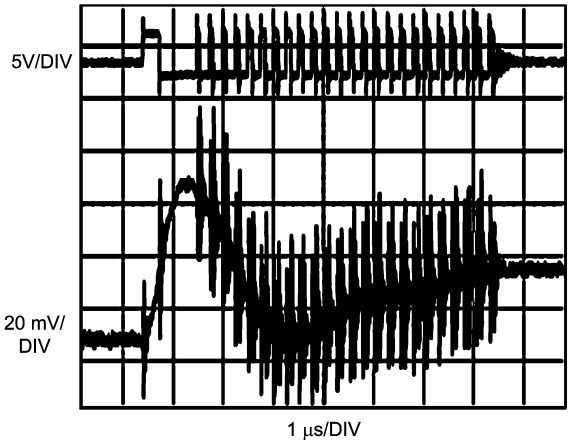


Figure 14. Typical ECO Operation

The output voltage ripple is slightly higher in ECO mode (30 mV peak-peak ripple typ.)

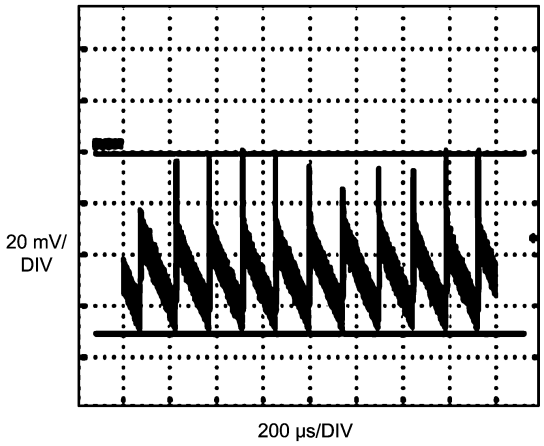


Figure 15. Typical Ripple in ECO Mode

BUCK OUTPUT VOLTAGE SELECTION

The selection of the bucks’ output voltages can be done by writing a specific code into the control registers (addr. 0x10 … 0x18). The required voltage can be calculated from the following equation:

BUCK (X)_VOUT(Y*)(mV) =
600 mV + code(dec)/127 * 2200 mV (2)

Where Y* denotes a number, which corresponds to the DVS control code. If DVS is not in use, then VOUT0 is used. 1-bit DVS uses VOUT0 and VOUT1 and 2-bit DVS uses V_{OUT}s 0 to 3.

EXTERNAL COMPONENT SELECTION

Default values for external components of LP3925 bucks are input and output capacitances $C_{IN} = C_{OUT} = 4.7\ \mu F$ and inductor L=1µH whit the lowest possible DCR (less than 50 mΩ). Below is the table with the selection of suitable inductors for the application. With the careful selection of the output components the performance of the buck will not degrade in stability, ripple, load regulation and transient aspects. The inductor current (IL) and output voltage (V_{OUT}) ripples are directly dependent on the external components. Current ripple is mainly dependent on the inductance L

$$\Delta I_L = \frac{(V_{IN} - I_L * R_{Pdson} - V_{OUT} - I_L * DCR) * V_{OUT}}{L * V_{IN} * f_{SW}} \quad (3)$$

where f_{SW} is the buck's switching frequency and R_{Pdson} is the drain to source resistance of the PMOS power switch. Voltage ripple on the other hand has 2 main components.

One dependent on output capacitance:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{8 * C_{OUT} * f_{SW}} \quad (4)$$

The other is due to capacitor's ESR

$$\Delta V_{OUT\_ESR} = ESR * \Delta i_L \quad (5)$$

The resulting RMS ripple is

$$\Delta V_{OUT} = \sqrt{\Delta V^2_{OUT\_C}{}^2 + \Delta V^2_{OUT\_ESR}} \quad (6)$$

For example if use the combination L = 0.47 µH (DCR = 50 mΩ) and C_{OUT} = 30 µF (ESR = 10 mΩ), when V_{IN} = 3V and V_{OUT} = 1.8V with load current of 600 mA, the theoretical peak to peak current ripple should be:

$$\Delta I_L = \frac{(3 - 0.6 * 0.16 - 1.8 - 0.6 * 0.05) * 1.8}{0.47 * 3 * 4} = 342\ mA \quad (7)$$

while the RMS peak-to-peak voltage ripple should be in the region of:

$$\Delta V_{OUT} = \sqrt{\left(\frac{342}{8 * 30 * 4}\right)^2 + (0.01 * 342)^2} = 4\ mV \quad (8)$$

DVS CONTROL

DVS allows a buck regulator to step between pre-programmed voltage values, using multifunctional pins as selectors. DVS is supported for Buck1 and Buck2. They can have up to 4 pre-programmed values, which are set in registers BUCKn VOUTn.

Multifunctional pins can be set as single DVS selectors (1 selecting signal) or dual DVS selectors (2 selecting signals). DVS-controlling pins must be set as Buck1 DVS (code 0101) or Buck2 DVS (code 0110) pins in their control registers (named GPIOnn).

Any multifunctional pin can be used as a single DVS signal. The signal selects between VOUT0 (input low) and VOUT1 (input high).

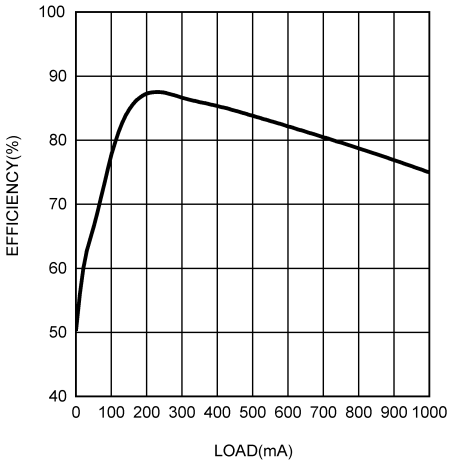
Dual DVS signals can only be predetermined pairs, the function description can be seen in Table 3.

Table 3. Dual DVS Control Table for Bucks 1 and 2

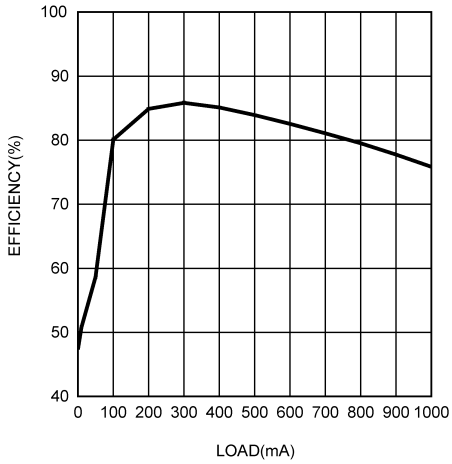
OSC_32KHZ	RSENSE	BUCK1,2 VOUT
SIM_RST_IN	SIM_CLK _IN	
SIM_DATA	SIM_RST	
SIM_CLK	SIM_IO	
TCXO1_I	TCXO1_O	
TCXO2_I	TCXO2_O	
OE_N	DATA/VP	
SE0/VM	RCV	
SPND	INP1	
INP2	SINK1	
SINK2	SINK3	
0	0	VOUT0
0	1	VOUT1
1	0	VOUT2
1	1	VOUT3

BUCK TYPICAL PERFORMANCE PLOTS

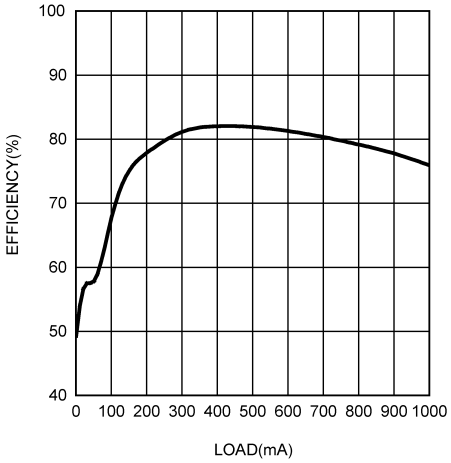
Efficiency (VIN = 3.0V, VOUT = 1.2V)



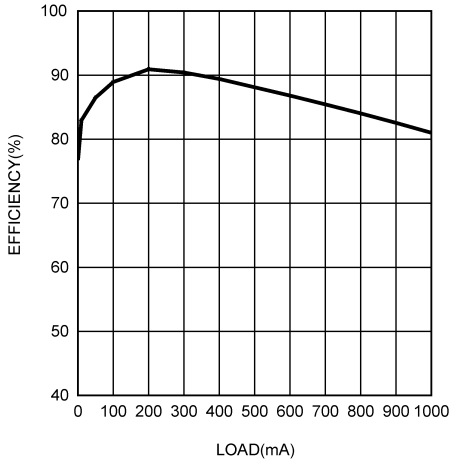
Efficiency (VIN = 3.6V, VOUT = 1.2V)



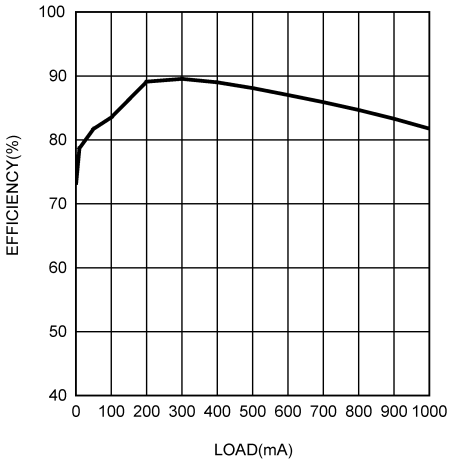
Efficiency (VIN = 4.2V, VOUT = 1.2V)



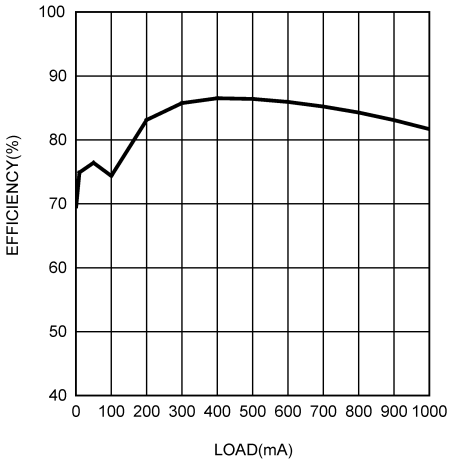
Efficiency (VIN = 3.0V, VOUT = 1.76V)



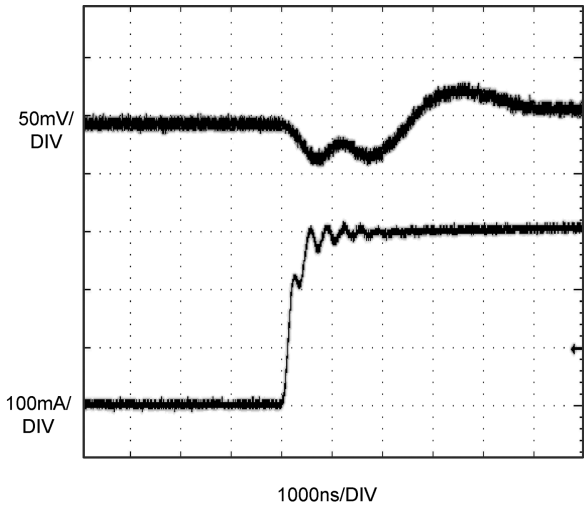
Efficiency
(VIN = 3.6V, VOUT = 1.76V)



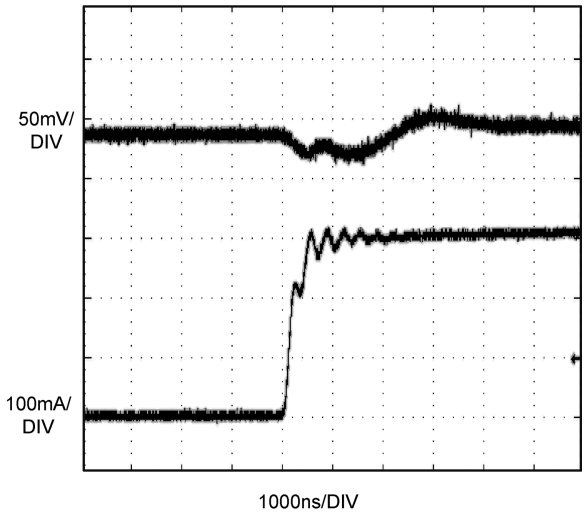
Efficiency
(VIN = 4.2V, VOUT = 1.76V)



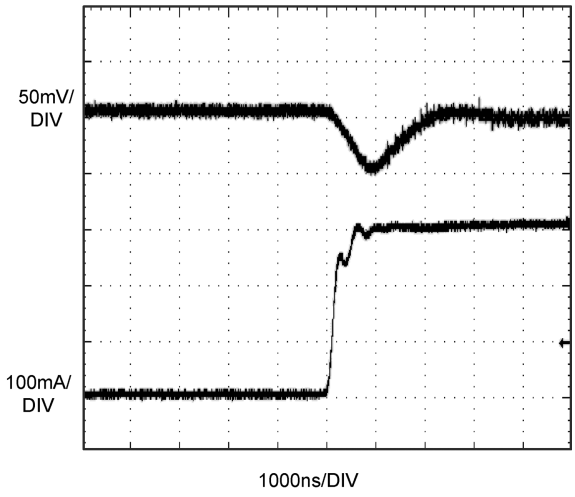
Buck1 Fast Rise (1µs)



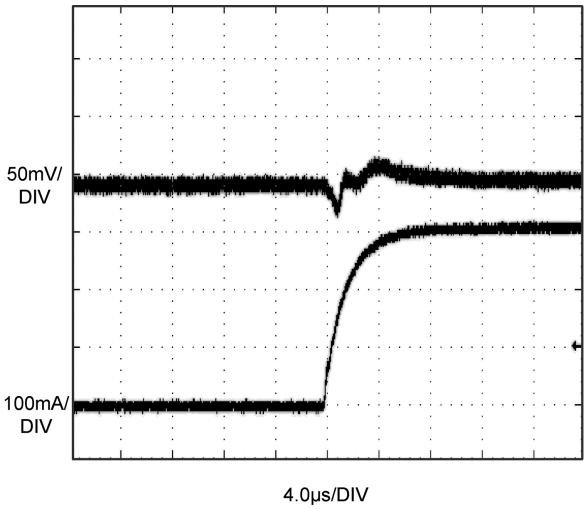
Buck2 Fast Rise (1µs)



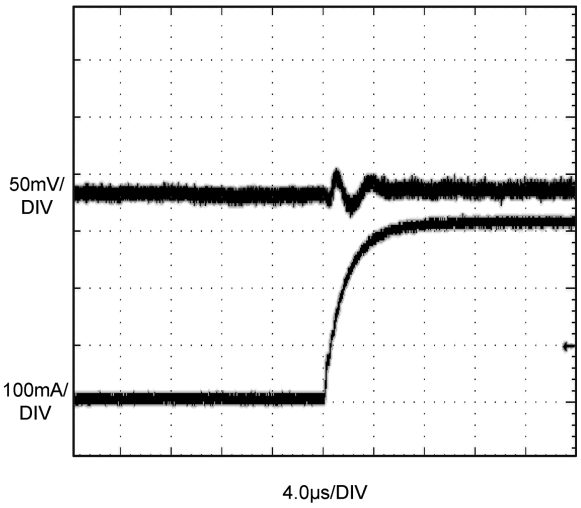
Buck3 Fast Rise (1µs)



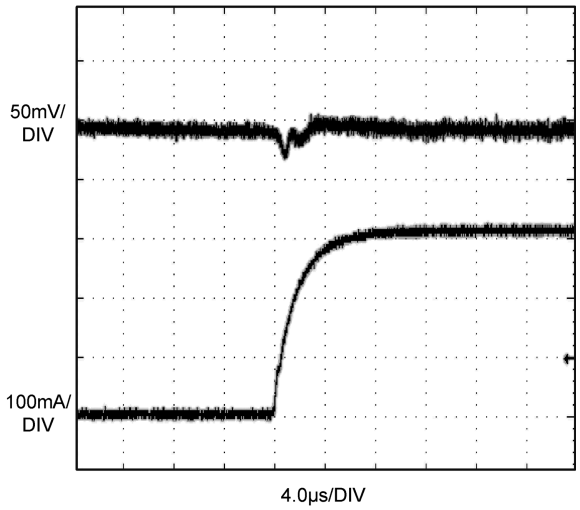
Buck1 Slow Rise (5µs)



Buck2 Slow Rise (5µs)



Buck1 Slow Rise (5µs)



BUCK ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −25°C to +85°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{FB}	Feedback voltage	PWM Mode, No load V_{OUT} = 1.1V to 1.8V		**-3**	**3**	%
		PWM Mode, No load V_{OUT} = 0.75V to 1.0V		**-10**	**10**	mV
I_{Q_ECO}	ECO mode I_Q	ECO Mode, FB = VIN No switching, sleep mode	25			µA
$R_{DSON\ (P)}$	Pin-pin resistance for PFET	VIN = VGS = 3.6V I_{OUT} = 200 mA	160		**250**	mΩ
$R_{DSON\ (N)}$	Pin-pin resistance for NFET	VIN = VGS = 3.6V I_{OUT} = -200 mA	115		**180**	mΩ
I_{LIM}	Switch peak current limit	Open loop; BuckX = 11	1475			mA
$t_{STARTUP}$	Startup time from shutdown	I_{OUT}= 0 V_{OUT} ≥ 0 to 97%(1)	65			µs
F_{SW}	Switching frequency	PWM Mode	4	**3.6**	**4.4**	MHz

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.

LDO INFORMATION

There are altogether 15 LDOs in LP3925 grouped as:

- General-type “PERFECT” LDOs;
- WILO-type LDOs;
- MICRO-PWR LDO; and
- USB LDO.

All LDOs can be programmed through serial interface for different output voltage values which are summarized in the “Control Register Bit Description” tables.

At the PMU power on, LDOs start up according to the selected startup sequence and the default voltages. See section **Power-on and Power-On Sequences** for details.

For stability all LDOs need to have external capacitors COUT connected to the output with recommended value of 1µF . It is important to select the type of capacitor which capacitance will in no case (voltage, temperature, etc) be outside of limits specified in the LDO Electrical Characteristics.

The description of different LDO types follow, except for the RTC description in the following section.

GENERAL-TYPE “PERFECT” LDOs

The general “PERFECT” LDOs are optimized to supply both analog and digital loads having ULTRA LOW NOISE (10 μV_{RMS} for I_{OUT} > 5mA) and excellent PSRR (75 dB at 10 kHz) performance. They can be programmed through the serial interface for different output voltage values.

For fast discharging of the output capacitors in shutdown, an internal 300Ω pulldown resistor to ground can be set via program control.

In sleep mode quiescent current is lowered to 5µA for energy saving; in this mode these LDOs should not be loaded by more than 3-5mA of output current.

The innovative design of these general type LDOs reduces the sensitivity to the placement of the output capacitor. These general purpose LDOs do not need the output capacitor to be placed as close to the PMU as is the case for normal LDOs. If a (1µF or more) capacitor is attached to a circuit load there is no need to place an output capacitor at the PMU.

WILO-TYPE LDOs

Wide Input Low Output (WILO) LDOs. The WILO-type LDO is optimized for wide range supply and low output voltage. It has good dynamic performance to supply different fast changing (digital) loads.

For proper operation, an input voltage of more than 2V is necessary. Hence, voltage drop on pass transistor (dropout voltage) will always exceed 0.45V and is independent of output current (in specified current range).

For fast discharge of the output capacitors in shut down, an internal 300Ω pulldown resistor to ground can be set via program control

MICRO-PWR LDO

This LDO is primarily used for internal supply purposes and fixed to 1.8V, but may deliver up to 30 mA of current also externally. This LDO is ON even in Standby mode (with total PMU current consumption about 2µA) and user may use it to supply some backup/always on system(s).

USB LDO

USB LDO is a high voltage LDO that uses VIN_CHG as a supply. It is used as a supply for D+ and D- buses as well as the VTRM output. It has a 28V over voltage protection capability. Regulator provides 45 dB PSRR at 10 kHz on entire voltage selection range except 4.85V option. Here it is 30 dB and is due to small distance to supply.

GENERAL LDO ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (2)

Symbol	Parameter	Test Conditions	LDO No.	Typ	Limits		Unit
					Min	Max	
V_{OUT}	Output voltage accuracy	I_{OUT} = 1mA, V_{OUT} = 2.0V	1-10		-2	2	%
					-3	**3**	
I_{MAX}	Output current rating		4,8			**80**	mA
			1-3, 5-7, 9, 10			**300**	
I_{SC}	Output current limit	V_{OUT} +0.5V ≤ V_{IN} ≤ 4.5V (1)	4,8	300	**80**		mA
		V_{OUT} +0.5V ≤ V_{IN} ≤ 4.5V (1)	1-3, 5-7, 9, 10	650	**300**		mA
I_{SLEEP}	Output current in sleep mode	V_{OUT} +0.5V ≤ V_{IN} ≤ 4.5V	1-10			**3**	mA
I_Q	Quiescent current in sleep mode			5			µA
V_{DO}	Dropout voltage	V_{OUT} = 3V; I_{OUT} = I_{MAX} (2)	4, 8	60		**150**	mV
			1-3, 4-7, 9, 10	100		**200**	
ΔV_{OUT}	Line regulation	V_{OUT} +0.5V ≤ V_{IN} ≤ 4.5V I_{OUT} = I_{MAX}	1-10	3			mV
	Load regulation	1mA ≤ I_{OUT} ≤ I_{MAX}	4, 8	0.5			mV
			1-3, 5-7, 9, 10	3.5			
e_N	Output noise voltage	10 Hz ≤ f ≤ 100 kHz C_{OUT} = 1µF (1)	1-10	15			µVRMS
PSRR	Power supply ripple rejection ratio	f = 10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA (1)	1-10	70			dB
$t_{START-UP}$	Startup time from shutdown	I_{OUT}= 0 V_{OUT} ≥ 0 - 90% V_{OUT} ≥ 0 - 97% (1)	1-10	45 50			µs
$V_{LOADTRANS}$	Load transient overshoot	I_{OUT} = 0 ≥ 200 mA I_{OUT} = 0 ≥ 200 mA (1)	1-10	-30 35			mV
$V_{LINETRANS}$	Line transient, peak-to-peak	V_{IN} = 3.6 ≥ 4.2 ≥ 3.6; tr = tf = 30 µs I_{OUT} = 50 mA (1)	1-10	90			µV
$V_{TRANSIENT}$	Start-up transient overshoot	C_{OUT} = 1µF, I_{OUT} = I_{MAX} (1)	1-10	1		30	mV
C_{OUT}	External output capacitance for stability		1-10	1	**0.6**	**20**	µF

(2) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.
(2) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.

WILO-TYPE LDO ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (3) (4)

Symbol	Parameter	Test Conditions	LDO No.	Typ	Limits		Unit
					Min	Max	
V_{OUT}	Output voltage accuracy	I_{OUT} = 1mA, V_{OUT} = 2.0V	11-13		-2	2	%
					-3	**3**	
I_{SC}	Output current limit	V_{OUT} = 0V	11-13	600	**300**		mA
I_{MAX}	Output current rating					**300**	mA
V_{DO}	Dropout voltage	V_{OUT} = 3V; I_{OUT} = I_{MAX} (1)	11-13	150		**250**	mV
ΔV_{OUT}	Line regulation	V_{OUT} +0.5V ≤ V_{IN} ≤ 4.5V I_{OUT} = I_{MAX}	11-13	2.5			mV
	Load regulation	1mA ≤ I_{OUT} ≤ I_{MAX}	11-13	3			
$I_{Qnormal}$	Quiescent current in normal mode	(2)	11-13	17			µA
I_{Qsleep}	Quiescent current in sleep mode	(2)		4			
e_N	Output noise voltage	10 Hz ≤ f ≤ 100 kHz C_{OUT} = 1µF, I_{OUT} = 20 mA V_{OUT} = 1.8V (2)	11-13	85			µVRMS
PSRR	Power supply ripple rejection ratio	f = 10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA (2)	11-13	60			dB
$t_{STARTUP}$	Startup time from shutdown	C_{OUT} = 1µF, I_{OUT} = I_{MAX}	11-13	35			µs
$V_{TRANSIENT}$	Startup transient overshoot	C_{OUT} = 1µF, I_{OUT} = I_{MAX}	11-13			**30**	mV
C_{OUT}	External output capacitance for stability		11-13	1.0	**0.5**	**20**	µF

(3) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(4) Specified for output voltages no less than 1.0V
(1) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.
(2) Specified by design.

MICRO-PWR LDO ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (3)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{OUT}	Output voltage accuracy	I_{OUT} = 1mA, V_{OUT} = 1.80V	1.8			V
I_{MAX}	Maximum output current	V_{OUT} = 1.8V	30			mA
I_{SC}	Output current limit	V_{OUT} = 0V	220			mA
ΔV_{OUT}	Line regulation	V_{OUT} +0.5V ≤ V_{IN} ≤ 4.5V I_{OUT} = I_{MAX}	2			mV
	Load regulation	1mA ≤ I_{OUT} ≤ I_{MAX}	1			
PSRR	Power supply ripple rejection ratio	f = 10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA (1)	45			dB
$t_{STARTUP}$	Startup time from shutdown	C_{OUT} = 1µF, I_{OUT} = I_{MAX} (1)	200			µs
$V_{TRANSIENT}$	Startup transient overshoot	C_{OUT} = 1µF, I_{OUT} = I_{MAX} (1)			75	mV
C_{OUT}	External output capacitance for stability		1.0	**0.6**	**20**	µF

(3) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.

USB LDO ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{VIN_CHG} = 5.0V. (2)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{OUT}	Output voltage accuracy	I_{OUT} = 1mA, V_{OUT} = 3.30V		**3.15**	**3.45**	V
I_{MAX}	Maximum output current	V_{OUT} = 3.30V	50			mA
I_{SC}	Output current limit	V_{OUT} = 0V	300			mA
V_{DO}	Dropout voltage	I_{OUT} = I_{MAX} USB LDO VOUT = 4.85V (1)	330			mV
ΔV_{OUT}	Line regulation	V_{OUT} +0.5V ≤ V_{IN_CHG} ≤ 6.5V I_{OUT} = 10 mA, V_{OUT} = 4.85V	5			mV
	Load regulation	1mA ≤ I_{OUT} ≤ I_{MAX} V_{OUT} = 3.3V	6			
PSRR	Power supply ripple rejection ratio	f = 10 kHz, C_{OUT} = 1µF I_{OUT} = 20 mA (2)	45			dB
$t_{STARTUP}$	Startup time from shutdown	C_{OUT} = 1µF, I_{OUT} = I_{MAX} (2)	15			µs
$V_{TRANSIENT}$	Startup transient overshoot	C_{OUT} = 1µF, I_{OUT} = I_{MAX}	250			mV
C_{OUT}	External output capacitance for stability		1.0	**0.6**	**20**	µF

(2) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply in cases it implies operation with an input voltage below the minimum appearing under Operating Ratings. For example, this specification does not apply for devices having 1.5V outputs because the specification would imply operation with an input voltage at or about 1.5V.
(2) Specified by design.

USB TRANSCEIVER

USB TRANSCEIVER

USB transceiver complies with USB 2.0 specification for full-speed (12Mb/s) device and low-speed (1.5Mb/s) device operation. The transceiver also supports USB Charger Detection by “Battery Charging Specification Revision 1.0 Mar 8, 2007”. The transceiver includes internal 1.5 kΩ pullup resistor and it is supplied from USB LDO.

USB transceiver can be configured to 3-pin, 4-pin or 5-pin interface.

If “USB transceiver not used” is configured, then USB transceiver is disabled in all circumstances, D+ and D- pins are Hi-Z and also 1.5 kΩ pullup resistor is disconnected. USB LDO has separate enable control and can be used also if “USB transceiver is not used”.

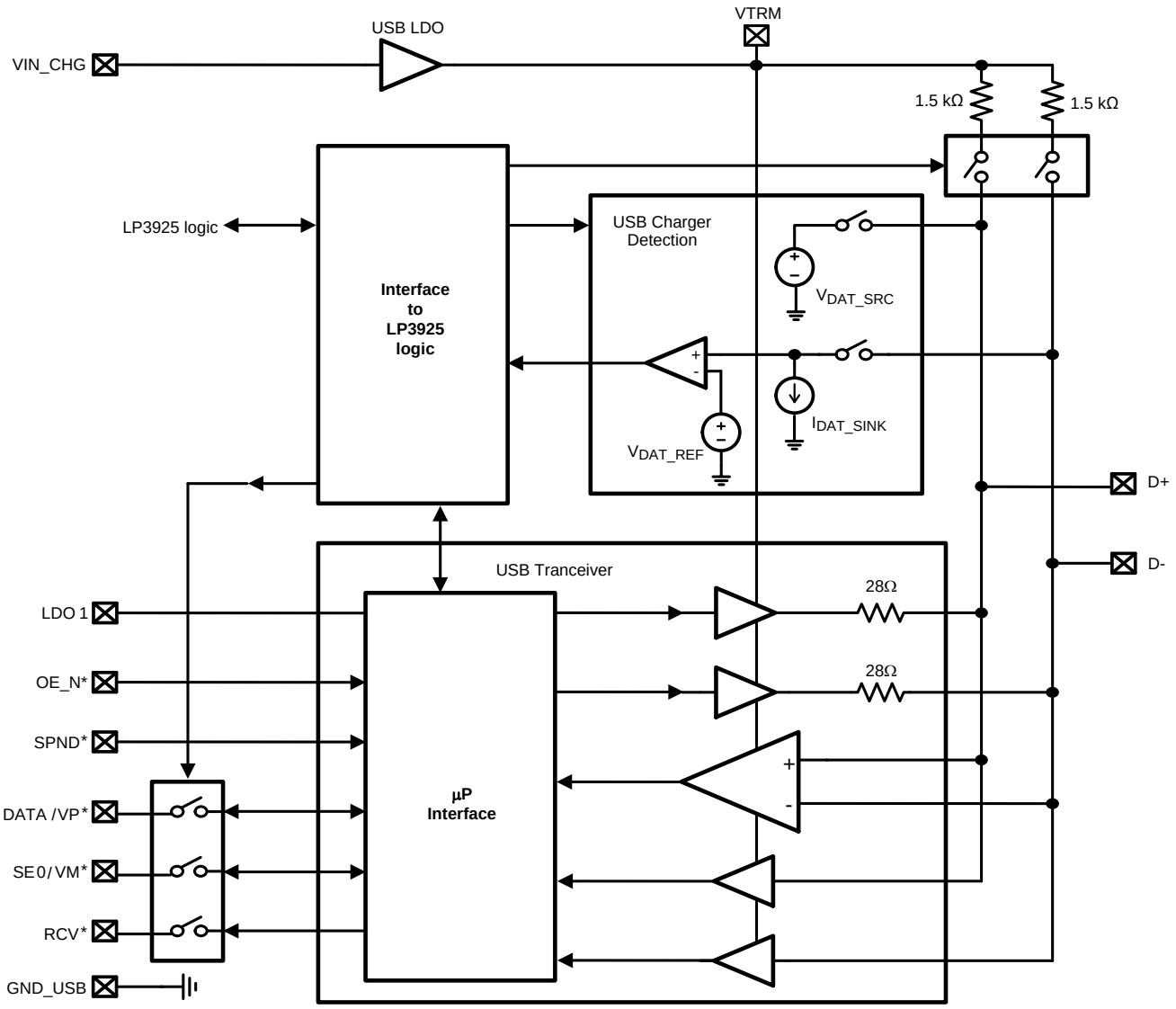


Figure 16. USB Transceiver Block Diagram

USB Transceiver enable is controlled by register 0x41 (USB XCVR CONTROL bits) and 0x36 (bit ALLOW USB XCVR IN SLEEP).

If AUTOMATIC USB DETECTION bit is set 1 then in any circumstances the USB transceiver stays disabled until USB Charger Detection is completed. USB Speed is determined by bit USB SPEED in register 0x4D:

USB SPEED	1 - Full Speed (12 Mb/s) 0 - Low Speed (1.5 Mb/s)

USB CHARGER DETECTION

USB Charger Detection works according to “Battery Charging Specification Revision 1.0 Mar 8, 2007” published by USB-IF.

To enable USB Charger detection:

(1) bit AUTOMATIC USB DETECTION in register 0x4D should be set 1; and

(2) Charger should be enabled.

After VIN_CHG voltage was detected to be high enough to start charging USB Charger Detection waits 900 ms and then checks D+ and D- for 100 ms. The detection result can be read form register 0x8D:

USB DETECTION DONE	1- USB Charger Detection completed 0 - USB Charger Detection is in progress or charger is disabled or there is no enough voltage on VIN_CHG.
USB DETECTION RESULT	1 - USB Charger detected 0 - USB host detected

If AUTOMATIC USB DETECTION is enabled (bit is set 1) then USB Transceiver stays disabled in all circumstances until USB Charger detection is completed. USB Charger Detection block gets supply from VTRM. To have detection result correct then USB_LDO should be enabled

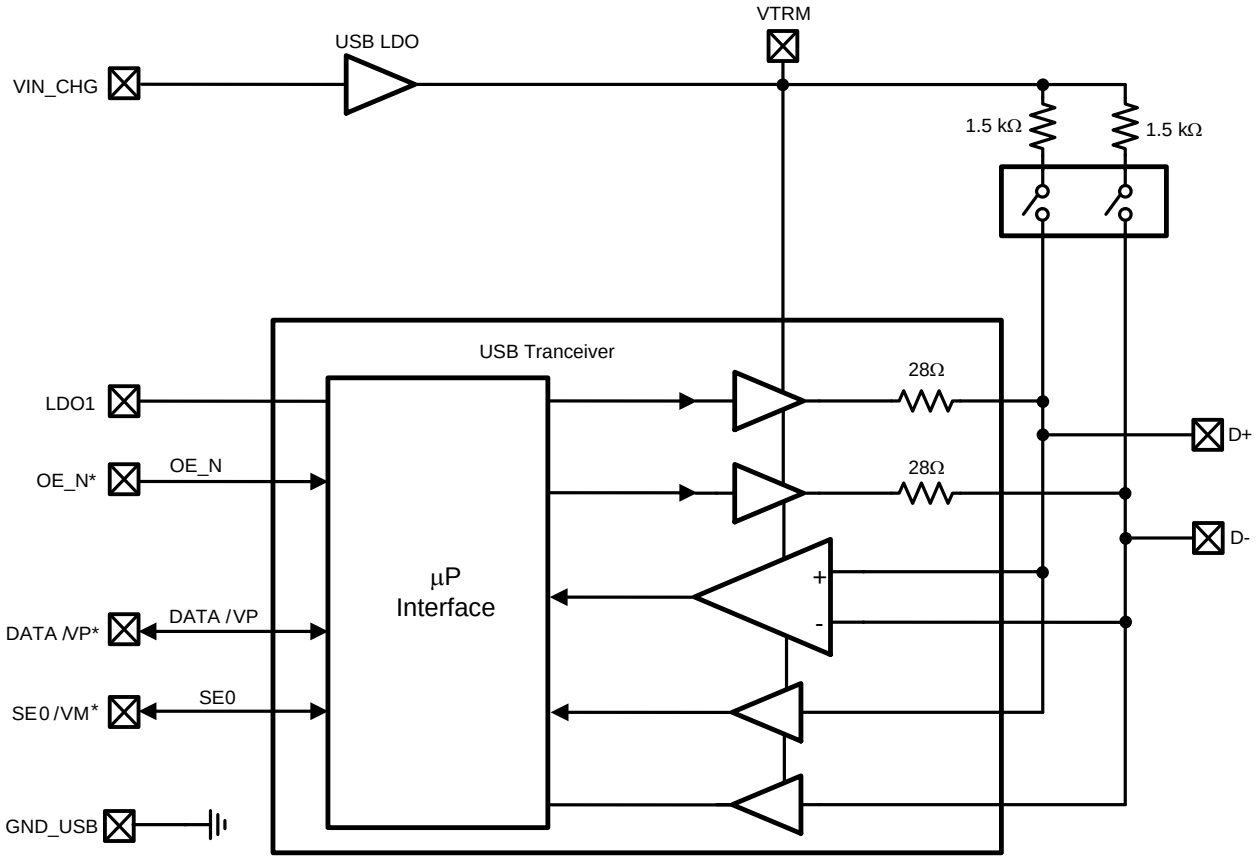


Figure 17. USB Transceiver Configured to 3-Pin Interface

Table 4. INTERFACE PINS

DATA	USB Interface data input/output
SE0	USB interface single ended 0 input/output
OE_N	USB Output Enable, active low

Table 5. TRUTH TABLE FOR 3-PIN INTERFACE

Transmitting OE_N=0				Receiving OE_N=1			
Inputs		Outputs		Inputs		Outputs	
DATA/VP*	SE0/VM*	D+	D-	D+	D-	DATA/VP*	SE0/VM*
0	0	0	1	0	0	previous state	1
0	1	0	0	0	1	0	0
1	0	1	0	1	0	1	0
1	1	0	0	1	1	undefined	0

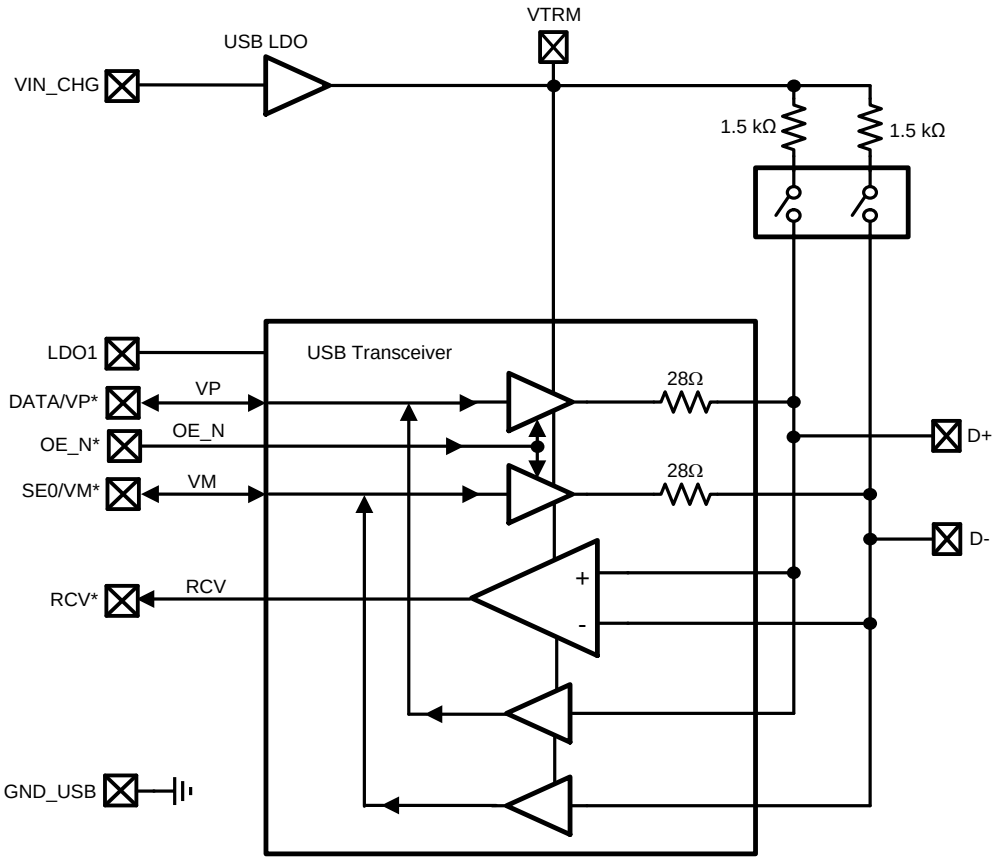


Figure 18. USB Transceiver Configured to 4-Pin Interface

Table 6. INTERFACE PINS

VM	USB interface minus input/output
VP	USB interface plus input/output
RCV	Receiver data - single ended output from USB differential lines.
OE_N	USB Output Enable, active low.

Table 7. Controlling the Transceiver

OE_N	VP	VM	FUNCTION
0	Input D+ = VP	Input D− = VM	Transmitting
1	Output D+ = VP	Output D− = VM	Receiving

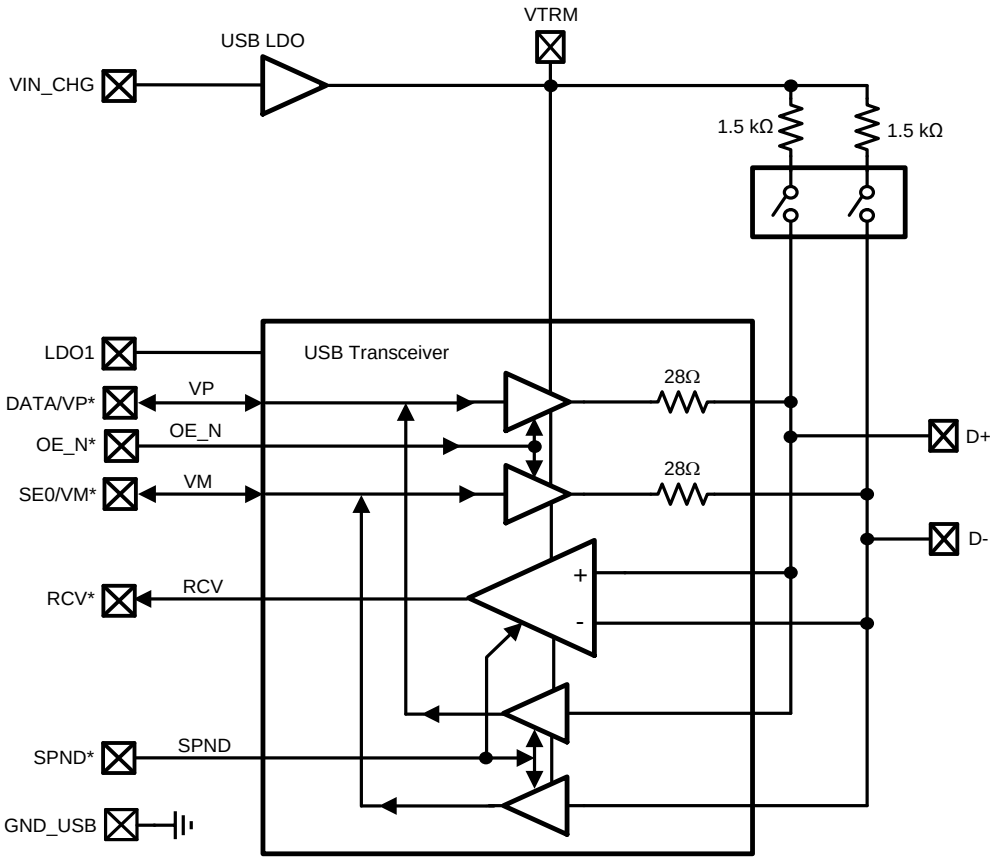


Figure 19. USB Transceiver Configured to 5-Pin Interface

Table 8. Interface Pins

VM	USB interface minus input/output
VP	USB interface plus input/output
RCV	Receiver data - single ended output from USB differential lines.
OE_N	USB Output Enable, active low.
SPND	USB suspend mode control input. A logical high will power down the differential receiver; VM and VP will remain active with reduced power consumption.

Table 9. Controlling the Transceiver in 5-Pin Configuration

SPND	OE_N	D+/D−	RCV	VP/VM	Function
0	0	Driving	Active	Input	Normal Transmitting
0	1	Receiving	Active	Output	Normal Receiving
1	0	Driving	USB_RCV_OFF in 0x6B	Input	Low-Power Transmitting
1	1	Receiving	USB_RCV_OFF in 0x6B	Output	Low-Power Receiving

USB CHARGER DETECTION ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{VIN_CHG} = 5V. (1)

Symbol	Parameter	Test Conditions	Typ.	Limits		Unit
				Min	Max	
V_{DAT_SRC}	Data source voltage	Load Current = 200 µA	0.6	**0.5**	**0.7**	V
V_{DAT_REF}	Data detect voltage		0.325	**0.25**	**0.4**	
I_{DAT_SINK}	Data sink current	0.15V < V_{D-} < 3.6V	100	**50**	**150**	µA

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

USB TRANSCEIVER ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V, V_{TRM} = 3.3V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{BUS}	VIN_CHG supply voltage	VIN_CHG pin works as USB VBUS pin		**4.2**	**5.5**	V
I_{BUS}	VIN_CHG pin quiescent current	Low-speed VIN_CHG pin works as USB VBUS pin USB Transmitter Receiving USB_LDO enabled, charger OFF	1.1		**2.5**	mA
Transceiver DC Characteristics						
I_{LO}	Hi-Z state data line leakage	0V < V < VTRM D+ if Low Speed; D- if High Speed, OE_N = 1.		−10	10	µA
V_{DI}	Differential input sensitivity	|(D+)−(D−)|, V_{IN} = 0.8V - 2.5V		**200**		mV
V_{CM}	Differential common-mode range	Includes V_{DI} Range (1)		**0.8**	**2.5**	V
V_{SE}	Single-ended receiver threshold high			**2.0**		V
	Single-ended receiver threshold low				**0.8**	
	Receiver hysteresis		100			mV
V_{OL}	Static output low	OE_N = 0, R_{LOAD} = 1.5 kΩ to 3.6V			**0.3**	V
V_{OH}	Static output high	OE_N = 0, R_{LOAD} = 15 kΩ to GND		**2.8**	**3.6**	
V_{TRM}	Termination voltage	I_{OUT} = 0, USB_LDO programmed to 3.3V		**3.15**	**3.45**	
R_{TRM}	Pullup resistance		1.5			kΩ
C_{IN}	Transceiver capacitance	Pin to GND (1)			**20**	pF
Z_{DRV}	Drive output resistance	D+, D− steady-state drive, I_{OUT} = 15 mA from regulator (1)		28	44	Ω
Low-Speed Driver Characteristics						
t_R	Transition rise time	C_{LOAD} = 50-600 pF (1)		**75**	**300**	ns
t_F	Transition fall time	C_{LOAD} = 50-600 pF (1)		**75**	**300**	
t_R/t_F	Rise/fall time matching	$_R/t_F$ (1)		**80**	**125**	%
Full-Speed Driver Characteristics						
t_R	Transition rise time	C_{LOAD} = 50 pF (1)		**4**	**20**	ns
t_F	Transition fall time	C_{LOAD} = 50 pF (1)		**4**	**20**	

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V, V_{TRM} = 3.3V. ()

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
t_R/t_F	Rise/fall time matching	$_R/t_F$ (1)		**90**	**110**	%

TCXO BUFFERS

The TCXO Buffer amplifies the 20 MHz sine wave from an external TCXO and shapes it into a buffered square wave clock signal with controlled rise and fall times.

The buffer input connected to an internal decoupling capacitor. The output clock signal has a default slew rate of 325 V/µs with an external load capacitance of 12.5 pF. The slew rate can be adjusted by changing the two-bit control data in the control register. This may be necessary if the actual load capacitance is considerably higher or the clock slew rate needs to be slower for EMC reasons.

If TCXO buffers are enabled, then they need some time to reach a working point. During this time the output signal can have an undesirable shape. To avoid unwanted signals, “TCXO in wait” control signals allow to set the time delay before enabling TCXO buffer output. “TCXO out strength” signals modify buffer output drive strength.

Possible values of “TCXO in wait” and “TCXO out strength” are stated in the GPIO section. Buffers are supplied from LDO1.

TCXO BUFFER ELECTRICAL CHARACTERISTICS (2)

Unless otherwise noted V_{BATT} = V_{DD} = 3.6V, C_{BYP_CHG} = 1µF, C_{FB_CHG} = 10 µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in boldface type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (3)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{IN}	Input voltage level	(1)		750		mV_{P-P}
V_{OH}	High-level output voltage	DC at 1µA	2.5	2.4		V
V_{OL}	Low-level output voltage	DC at 1µA	0.1		0.2	
T_P	Propagation delay	C_L = 13 pF (1)	12			ns
T_{TT}	Output transition time	C_L = 13 pF (10% and 90% level) (1)	7			
V_{SR}	Output slew rate	C_L = 13 pF (1)	325	200	450	V/µs
C_{IN}	Input capacitance	(1)	2		10	pF

(2) For warm-up time and driving strength, refer to multifunctional pins section.
(3) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.

BACKUP BATTERY CHARGER

Backup battery charger (BBC) is intended for charging an external coin battery. Its output is connected to VCOIN-pin. It consists of Voltage Limited Current Source with 1kΩ output resistor. By default it is always on. It is possible to turn backup battery charger off via registers. VCOIN - voltage limit and ICOIN - current source values are also programmable via registers (the possible values are stated in Backup battery charger selection table). BBC has a reverse current protection. VCOIN-pin voltage can be measured by an internal ADC.

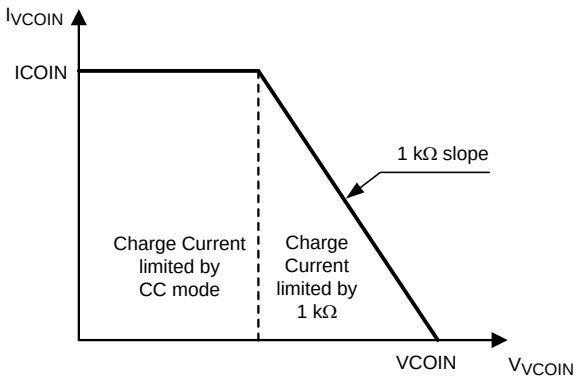


Figure 20. BBC IU Characteristics

MOMENTARY POWER LOSS

When power is removed from the LP3925 PMU and MPL function is enabled (register 0x81) then Momentary Power Loss (MPL) timer starts as unexpected power down has occurred. This timer is set to the maximum duration allowed for a momentary power loss (register 0x81). If power is restored before the timer expires, then MPL block informs LP3925 control logic about MPL-event.

The MPL circuit is powered from VCOIN-pin. MPL timer uses 32.786 kHz RTC crystal oscillator for time base. Host processor needs to enable the MPL function every time the device is powered up.

32.768 kHz CRYSTAL OSCILLATOR

There are two options for implementing the 32.768 kHz oscillator:

1. 1. An external crystal that is connected between XIN and XOUT. The external crystal ESR must not exceed 100 kΩ; if this value is exceeded the circuit may never start oscillating.
2. 2. An external oscillator module could be used by connecting the module output directly into XIN. When using an external oscillator module, the XOUT pin should be unconnected.

Pins XIN and XOUT are not able to drive external load. Oscillator output is buffered to pin OSC_32KHZx Note. Oscillator is powered by LDO1, thus before it is up, the oscillator will not start.

BACKUP BATTERY CHARGER ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (2)

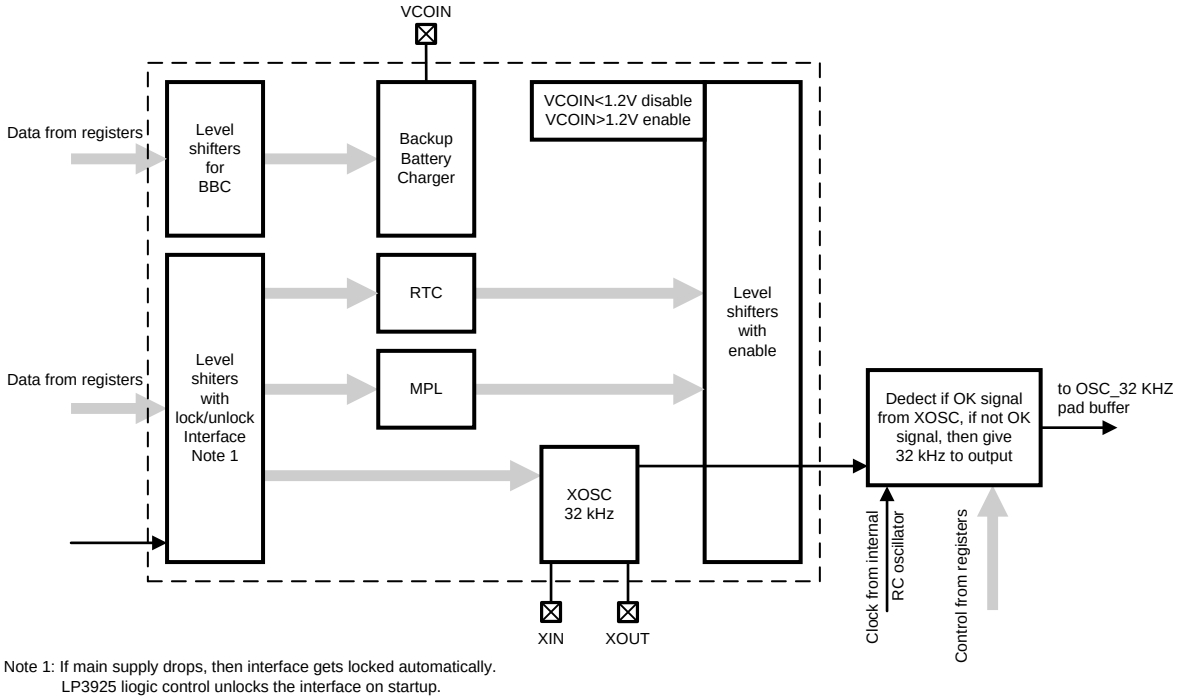
Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{COIN}	Voltage Limit	I_{LOAD} = 1µA; V_{COIN} programmed to 3.00V		**−3**	**+3**	%
I_{COIN}	Charging Current	V_{COIN} pin shorted to GND I_{COIN} programmed to 200 µA		**−20**	**+20**	%
R_{VCOIN}	Internal Series Resistor		1.0	0.5	1.6	kΩ
I_{LEAK}	Reverse leakage current	VRTC pin current = 0			10	µA
I_{GND}	Charger Ground Current	I_{LOAD} = 0.	2.5			
	Load Regulation	I_{LOAD} = 0.	0.5			

(2) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

REAL TIME CLOCK

The Real Time Clock (RTC) block is used for time tracking in any chip condition. It uses 32 kHz crystal oscillator for accurate timekeeping and is supplied either from system supply in normal condition or from coin battery when the PMU has no main power. The RTC gets power from V_{COIN}, with minimum operation above 1.9V. This RTC has following features:

- Accurate time counting with fine-grained correction for long-term accuracies;
- Calendar for years 2000 - 2099 with leap year compensation and automatic weekday calculation;
- Two highly customizable alarms; and
- Data in software-friendly binary format.



Note 1: If main supply drops, then interface gets locked automatically. LP3925 liogic control unlocks the interface on startup.

Figure 21. RTC Functional Block Diagram

Calendar and alarm data is presented in following format:

Table 10. Calendar and Alarm Data

Time Unit	Register Data	Represented Values
Seconds	000000 - 111011	0 - 59
Minutes	000000 - 111011	0 - 59
Hours	00000 - 10111	0 - 23
Day of Month	00001 - 11111	1 - 31
Month	0001 - 1100	January - December
Year	0000000 - 1100011	2000 - 2099
Weekday	0000001 - 1000000 (1-hot code)	Monday - Sunday

RTC calendar and alarm registers are user-writable, except for calendar weekday registers, which are calculated automatically and are read-only. All RTC registers are in RTC power domain. The registers are zeroed, if RTC is powered up. As long as RTC is supplied, the alarm registers will hold the written data and the calendar will keep track of time.

Writing data to a calendar register will initiate a calendar write sequence, which will last 3ms. During this time the register's data should not be read, because it may not be accurate.

Alarms allow creating periodical or one-time events. The result of an alarm event depends on the PMU state. If PMU is in standby, then alarm can cause PMU to start up. If PMU is in working mode, then alarm can create an interrupt.

Alarm event happens if the alarm is activated (ALARM ACTIVATED bit is 1) and current RTC time matches the time in all alarm configuration registers. To exclude a time unit value from matching check, write the unit's IGNORE bit to 1. If alarm's weekday is not important or not known, then all weekday bits should be set to 1.

Interrupt or PMU startup is triggered at the start of an alarm event.

The RTC also has a time counting correction register. This can slightly change time counting speed to compensate for oscillator inaccuracies. Correction events happen 7 times in an hour. The maximum correction range is 241 ppm (corresponds to code 127) and one step size is approximately 1.9 ppm.

USIM INTERFACE

LP3925 includes a SIM/RUIM card interface level-shifter function. This can be used, if the processor I/O voltage and SIM card I/O voltage have different values. The interface includes pins for 3 signals: reset, clock and data. Reset and clock are unidirectional control signals, going from the processor to the SIM card. Data signal is bidirectional.

The SIM card side of the level shifter is always supplied by LDO8. The processor side supply is user-selectable between Buck2, LDO1 and LDO11. If the level shifter is enabled, then the supplies on both sides must be 1.5V or higher to ensure proper operation.

USIM LEVEL TRANSLATOR ELECTRICAL CHARACTERISTICS

Unless otherwise noted, $C_{LDOx} = C_{VIN\_CHG}+C_{VBUS}+C_{VTRM}$ = 1µF. Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{ILS}	Input low threshold	RST_IN, CLK_IN logic inputs, LDO1 supply selected			**0.25* V_{LDO1}**	V
V_{IHS}	Input high threshold			**0.75* V_{LDO1}**		
V_{OLS}	Output low level	SIM_RST, SIM_CLK logic outputs			**0.25* V_{LDO8}**	V
V_{OHS}	Output high level			**0.75* V_{LDO8}**		
R_{INPU}	SIM_IO pullup resistor	SIM_IO	10			KΩ
$V_{IL\_SIM\_IO}$	Input low				0.3	V
$V_{IH\_SIM\_IO}$	Input high			V_{DD}-0.6V		
$V_{OL\_SIM\_IO}$	Output low level when SIM_DATA=GND				**0.25* V_{LDO8}**	
$V_{OH\_SIM\_IO}$	Output high level			**0.75* V_{LDO8}**		
R_{SPU}	SIM_DATA pullup resistor	SIM_DATA, LDO1 supply selected	20	13		KΩ
$V_{IL\_SIM\_DATA}$	Input low				0.3	V
$V_{IH\_SIM\_DATA}$	Input high			**0.75* V_{LDO1}**		
$V_{OL\_SIM\_DATA}$	Output low level when SIM_IO=GND				**0.25* V_{LDO1}**	
$V_{OH\_SIM\_DATA}$	Output high level			**0.75* V_{LDO1}**		
Timing						
	Clock frequency(1)		20	**5**		MHz

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.

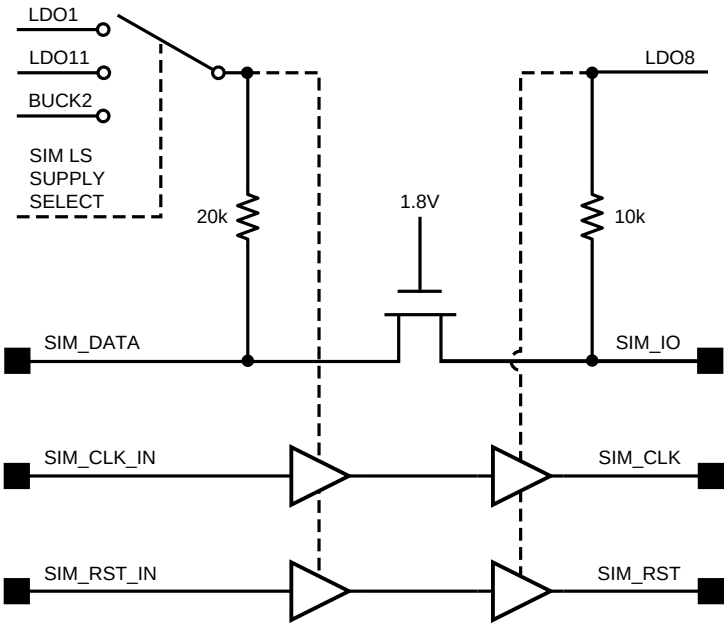


Figure 22. SIM Interface Level Shifters

COMPARATORS

Two general purpose comparators are available, which can be used for detecting the plugging of external accessories or other events. Voltage comparators are available on multifunctional pins INP1 and INP2. 8 comparison thresholds are available between 400 mV and 2400 mV, the values can be found in the multifunction pins section. Comparator state is available from registers as a read-only bit, or from multifunctional pins as a direct data output. It is also possible to generate an interrupt every time the comparator state changes.

COMPARATOR ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (2)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{TH}	Input threshold voltage	Default setting	0.6			V
V_{TH2}	Input threshold voltage 2	Default setting	1			
I_{IL}	Input leakage current	INP1, INP2 $0 \le V_{INPUT} \le V_{VIN1}$.		−1	1	µA

(2) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

ADC

LP3925 is equipped with a 12-bit ADC that has 8 inputs for measuring charging current, discharge current, battery voltage (measuring at BATT pin), backup battery voltage, charger input voltage, VDD, temperature and external signal through GPIO.

The inputs are scaled linearly to adapt the voltage/current range of the source to the input voltage range of the A/D core.

The ADC is clocked by the internal 4MHz system clock. The conversion result is available in the registers 0x88 and 0x89 in 3ms after the setting of the ADC CONV START bit in the 0x87 Register. The ADC will automatically enter power save mode if conversions are not performed.

A/D CONVERTER DATA AND CONTROL REGISTERS

Two read only registers 0x88 and 0x89 provide access to the a/d conversion result. 8 most significant bits of the data can be accessed in one read cycle. The Read/Write 0x87 register allows starting the conversion, source selection and output format selection. Setting the ADC CONV START bit in the control register starts a new A/D conversion. Setting ADC_FORMAT bit to 1 allows throwing out the MSB and shifting the result 1 bit left. This can be used if result's MSB is known, to get more data with one register read.

BATTERY DISCHARGE CURRENT MEASUREMENT

The discharge current is measured indirectly by measuring the voltage drop produced by discharge current on the Rsense. The calculation of the current value is done by equation below:

$$I_{BATT}\ (A) = code(dec) * \frac{V_{SNS}}{4095 * R_{SENSE}} \quad (9)$$

The value of the appropriate V_{SNS} (so that the maximum code would correspond to 1.2A) can be chosen in reg.0x19. That is if R_{SENSE} = 100 mΩ, the V_{SNS} should equal 120 mV.

JUNCTION TEMPERATURE MEASUREMENT

Temperature measurement is performed in the rage of +390°C...−275°C which means that the following equation is valid for calculating the chip's junction temperature:

$$TEMP(℃) = 390℃ - (code(dec) * 0.16℃) \quad (10)$$

OTHER ITEM CURRENT VOLTAGE MEASUREMENT

$$V(or\ I) = code(dec) * \frac{Full\_Scale\_Value}{4095} \quad (11)$$

For example: If ADC input SEL is set as 0011, it will measure the BATT voltage. Full_Scale_Value = 4.80V; so V_{BATT} = *code(dec) * 4.8/4095.*

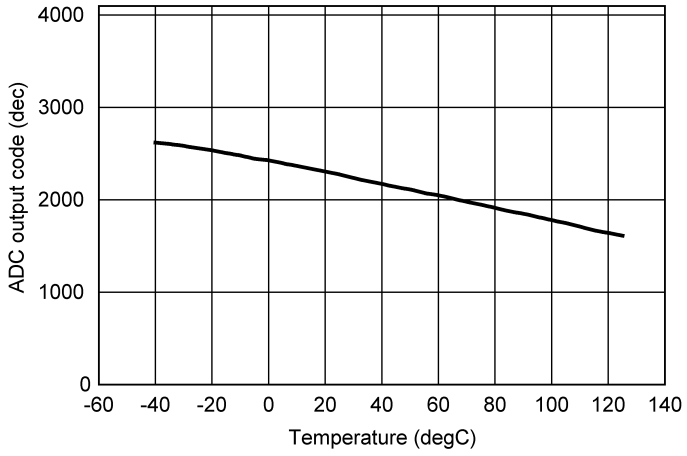


Figure 23. LP3925 ADC Temperature Range

ADC ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (1)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
	Resolution		12			bits
INL	Integral Nonlinearity	(1)		−4	+4	LSB
DNL	Differential Nonlinearity	No missing code (1)		−2	+2	
	Conversion Time	(1)			**3**	ms

(1) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(1) Specified by design.

REFERENCE OUTPUT

Reference Output Reference output voltage is used by the external blocks (plug-in microphone, ADCs, etc). This voltage is achieved by the reference buffer and is supplied to the REF_OUT bump. Reference buffer has a load capability of 1mA and when not used can be disabled while the output is pulled by an internal resistor to the ground. A presented diagram shows a typical application of REF_OUT signal for battery temperature measurement purpose, using an internal battery thermistor.

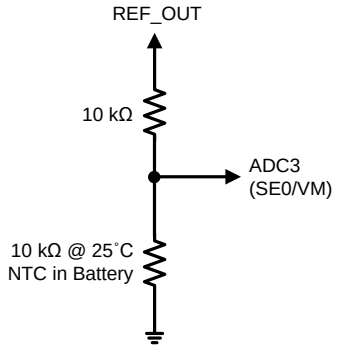


Figure 24. Typical REF_OUT Battery Temperature Measurement Application Diagram

REFERENCE BUFFER ELECTRICAL CHARACTERISTICS

Typical values and limits appearing in normal type apply for T_J = 25ºC. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, T_J = −40°C to +125°C. Unless otherwise specified, the following applies for V_{BATT} = 3.6V. (2)

Symbol	Parameter	Test Conditions	Typ	Limits		Unit
				Min	Max	
V_{REF}	Reference voltage accuracy	I_{LOAD} = 0mA	0.3			%
		I_{LOAD} = 1mA	1			
I_{LOAD}	Load Current			−1	+1	mA
R_{PULL_DOWN}	Integral Nonlinearity		400			kΩ

(2) All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are Specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

UVLO OPERATION

UVLO measures system voltage on pin VDD and compares it to selected voltages. The function uses 2 comparators, which are configured in register address 0x85 (possible values are stated in the table below). These comparators are combined into UVLO_N state, which can affect startup, cause shutdown or generate interrupt. The state is readable in register address 0x8E bit 2.

UVLO_N state can change on following conditions:

- If system voltage is lower than UVLO LEVEL1 and UVLO LEVEL2, then UVLO_N state is set to '0'.
- If system voltage is higher than UVLO LEVEL1 and UVLO LEVEL2, then UVLO_N state is set to '1'.

Using different values for levels 1 and 2 provides a window for voltage drops under high load working conditions.

UVLO_N state '0' indicates that the voltage is below normal working range, so the system is not allowed to start up. This state can also cause the system to shut down. UVLO_N state '1' indicates that the voltage is in normal working range, so the system is allowed to start up and operate. State transition '1'->'0' causes an UVLO interrupt, which can be sent to IRQ_N output.

CURRENT SINKS

LP3925 provides 3 current sinks, which can sink current for LEDs, vibration motors or other external functions. Current sinks have selectable DC current value and also PWM control options. SINK1, SINK2 and SINK3 are multifunction pins, so current sink function and DC current value are selectable with respective GPIO control bits (described in the table in Multifunctional pins section). SINK1 has a 250 mA maximum current value, SINK2 and SINK3 provide up to 100 mA. If the pin is configured as a current sink with a certain current, then PWM CODE bits will switch that current on and off, according to the PWM algorithm.

The smallest unit in PWM control is a time slot. The length of a time slot is set with ISINK PWM TIME SLOT SIZE bits. Smaller time slot causes faster switching, but increases non-linearity. 7 time slots form a PWM cycle. Cycle is the current sink on-off switching period, so the main PWM frequency can be calculated as: Fpwm = 1/(7*Ttimeslot).

9 cycles, which is 9*7=63 time slots, form a PWM pattern. ISINK PWM CODE bits select, during how many of these 63 time slots the current sink is active. Code 000000 means that the sink is always off. Code 111111 (63 in decimal) means that the sink is always on.

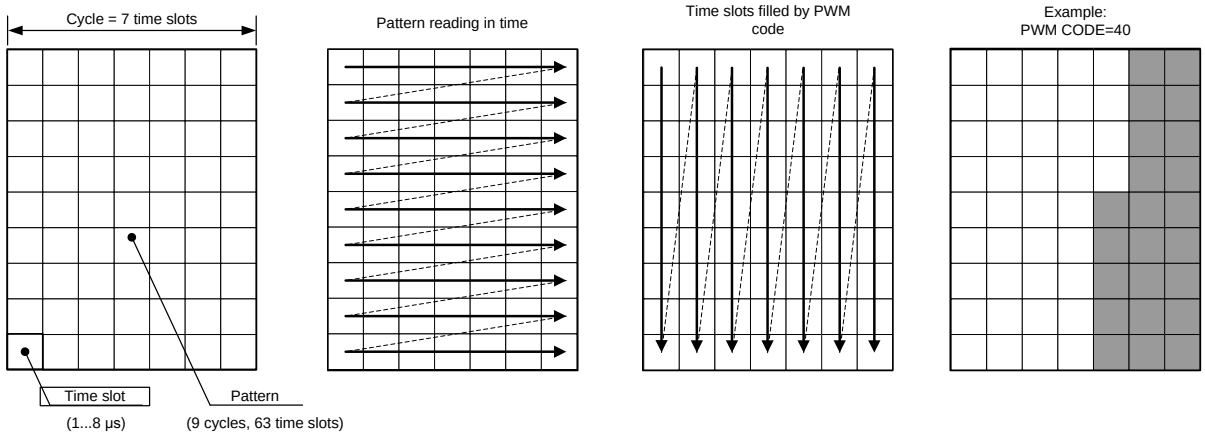


Figure 25. Current Sinks PWM Control

SUPPORT FUNCTIONS

REFERENCE

LP3925 has internal reference block creating all necessary references and biasing for all blocks.

OSCILLATOR

There is internal oscillator giving clock to the bucks and to logic control.

Table 11. V_{VBATT} = 3.6V

Parameter	Typ	Min	Max	Unit
Oscillator Frequency	4.0	3.9	4.1	MHz

THERMAL SHUTDOWN

The Thermal Shutdown (TSD) function monitors the chip temperature to protect the chip from temperature damage caused by excessive power dissipation. The temperature monitoring function has two threshold values TSD_H and TSD_L that result in protective actions.

When TSD_L +125°C is exceeded, then IRQ_N is set to low and “1” is written to TSD_L bit in both STATUS register and in INTERRUPT register. If the temperature exceeds TSD_H +160°C, then PMU initiates Shutdown. The POWER UP operation after Thermal Shutdown can be initiated only after the chip has cooled down to the +115°C threshold

Parameter	Typ	Unit
TSDH (1)	160	°C
TSDL (1)	125	
TSDL Hysteresis (1)	10	

(1) Specified by design.

I²C-COMPATIBLE SERIAL BUS INTERFACE

INTERFACE BUS OVERVIEW

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communications between the IC’s connected to the bus. The two interface lines are the Serial Data Line (SDA), and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pullup resistor of 1.5 kΩ, and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the serial clock (SCL).

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock’s high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

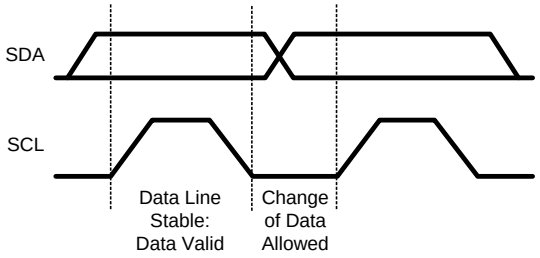


Figure 26. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

START AND STOP

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

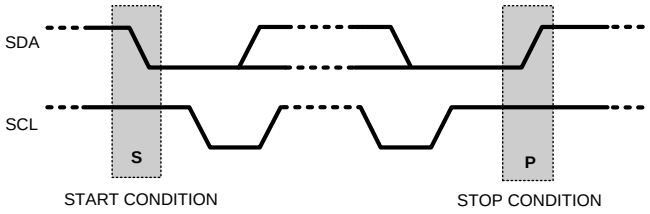


Figure 27. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pulldown the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

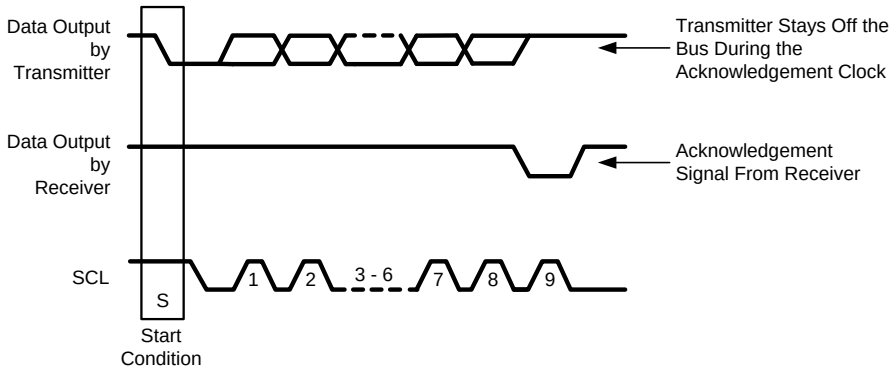


Figure 28. Bus Acknowledge Cycle

"ACKNOWLEDGE AFTER EVERY BYTE" RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule.

When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This "negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP3925 operates as a slave device with the address **7h'xx (binary nnnnnnnn)**. Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

CONTROL REGISTER WRITE CYCLE

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

CONTROL REGISTER READ CYCLE

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = '0').
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.

- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = “1”).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = ‘0’>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = ‘1’>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = ‘0’>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>

REGISTER READ AND WRITE DETAIL

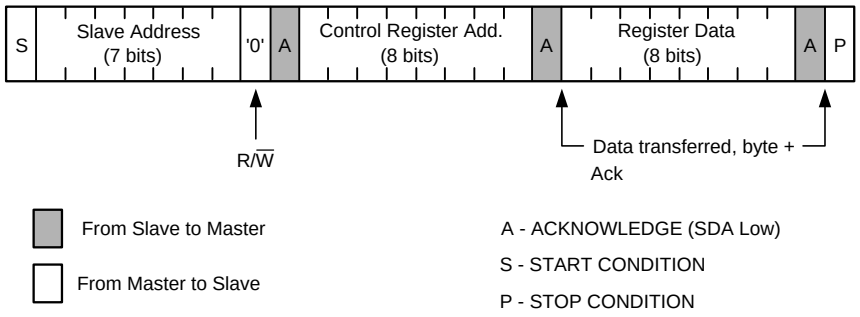


Figure 29. Register Write Format

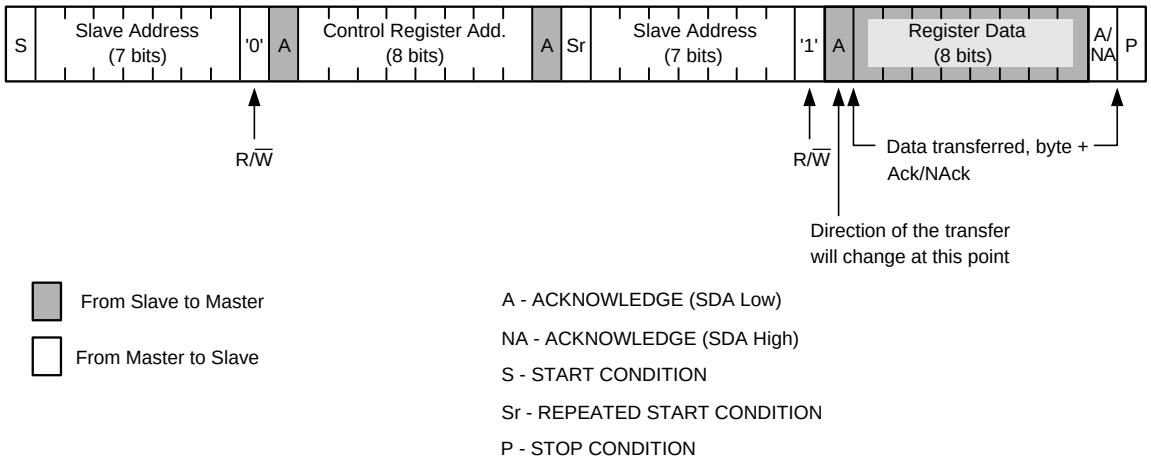


Figure 30. Register Read Format

For more detailed control register information, or to order samples, please contact your local Texas Instruments sales office or visit http://www.ti.com.

REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	52

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LP3925RME-A/NOPB	ACTIVE	DSBGA	YQB	81	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM		V030	Samples
LP3925RME-E/NOPB	ACTIVE	DSBGA	YQB	81	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM		V030	Samples
LP3925RMX-A/NOPB	ACTIVE	DSBGA	YQB	81	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM		V030	Samples
LP3925RMX-E/NOPB	ACTIVE	DSBGA	YQB	81	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM		V030	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

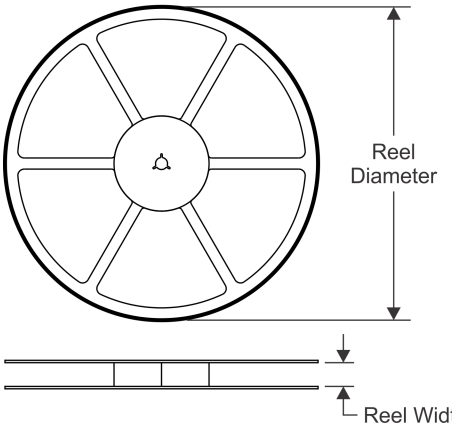
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

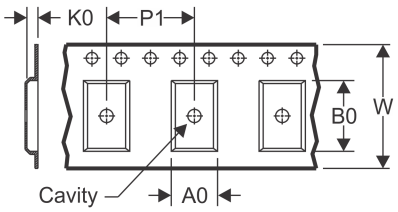
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

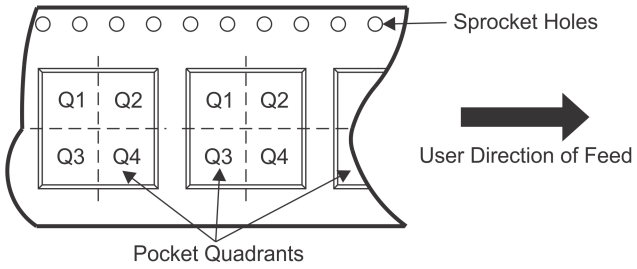


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

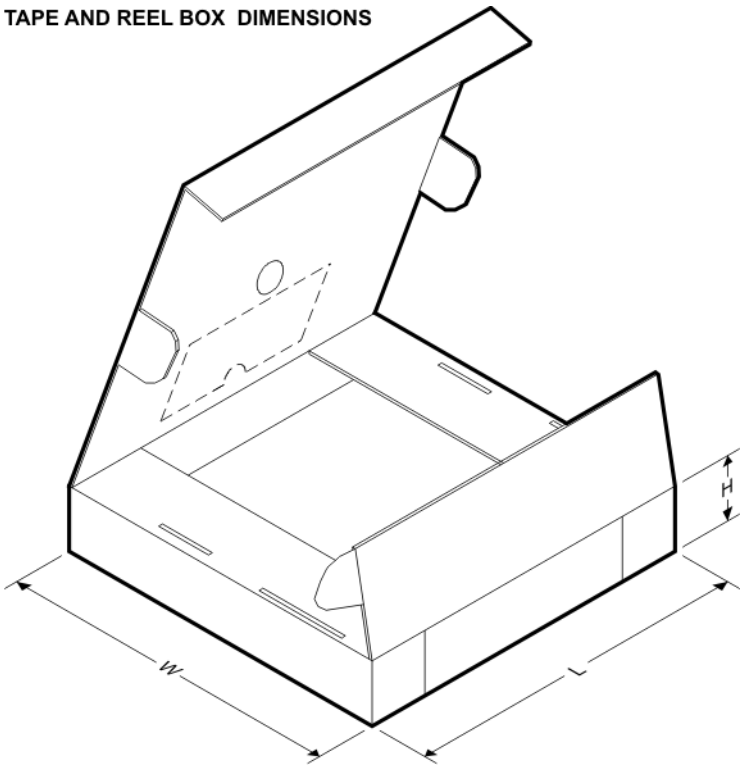
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3925RME-A/NOPB	DSBGA	YQB	81	250	178.0	12.4	3.81	3.81	0.76	8.0	12.0	Q1
LP3925RME-E/NOPB	DSBGA	YQB	81	250	178.0	12.4	3.81	3.81	0.76	8.0	12.0	Q1
LP3925RMX-A/NOPB	DSBGA	YQB	81	1000	178.0	12.4	3.81	3.81	0.76	8.0	12.0	Q1
LP3925RMX-E/NOPB	DSBGA	YQB	81	1000	178.0	12.4	3.81	3.81	0.76	8.0	12.0	Q1

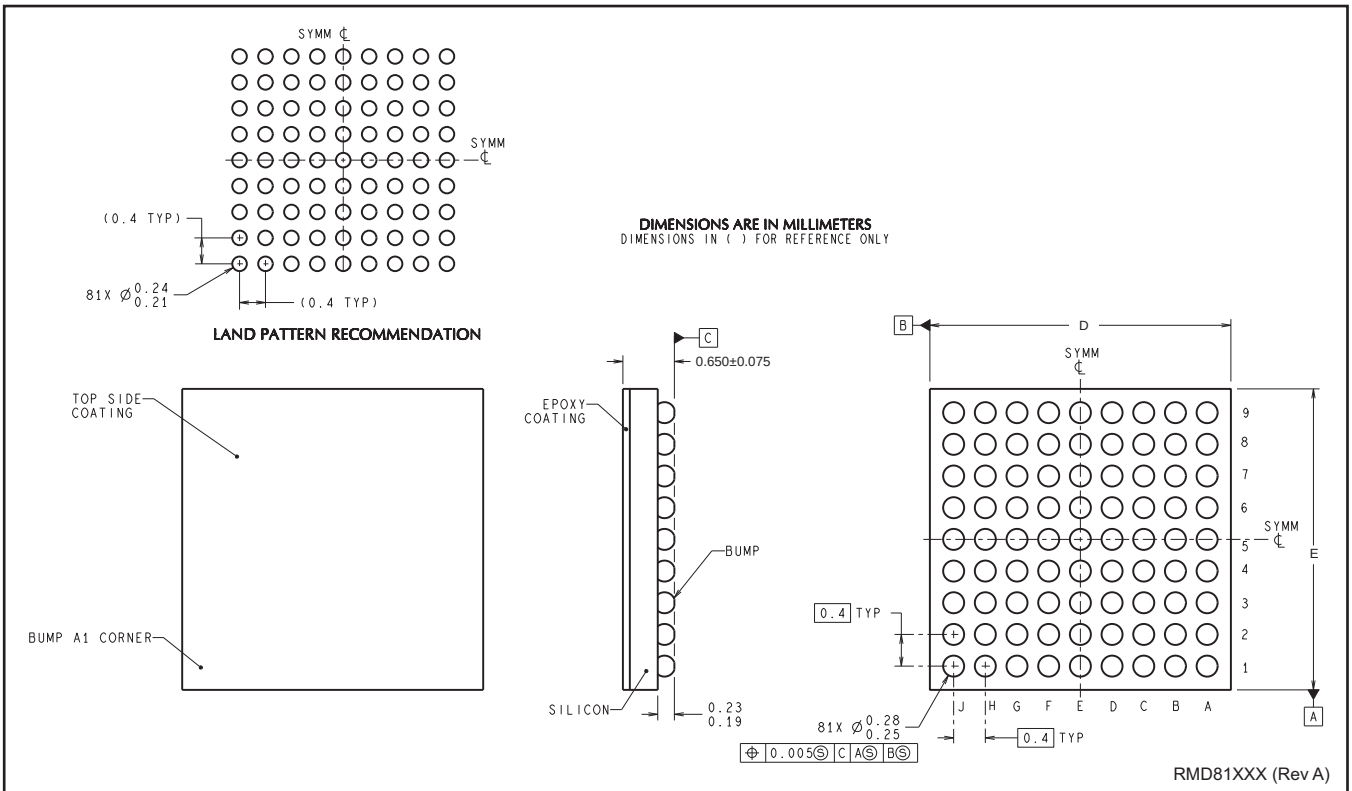
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3925RME-A/NOPB	DSBGA	YQB	81	250	203.0	190.0	41.0
LP3925RME-E/NOPB	DSBGA	YQB	81	250	203.0	190.0	41.0
LP3925RMX-A/NOPB	DSBGA	YQB	81	1000	206.0	191.0	90.0
LP3925RMX-E/NOPB	DSBGA	YQB	81	1000	206.0	191.0	90.0

YQB0081



D: Max = 3.64 mm, Min = 3.58 mm

E: Max = 3.64 mm, Min = 3.58 mm

4214915/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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