LM3269 Seamless-Transition Buck-Boost Converter for 3G and 4G RF Power Amplifiers

Check for Samples: LM3269

FEATURES

- **Operates From a Single Li-Ion Cell: 2.7V to 5.5V**
- **Adjustable Output Voltage: 0.6V to 4.2V**
- **Automatic PFM/PWM Mode Change**
- **750 mA Maximum Load Capability for V_{BATT} ≥ 3.0V, V_{OUT} = 3.8V**
- **2.4 MHz (typ.) Switching Frequency**
- **Seamless Buck-Boost Mode Transition**
- **Fast Output Voltage Transition: 1.4V to 3.0V in 10 µs**
- **High-Efficiency: 95% typ. at V_{BATT} = 3.7V, V_{OUT} = 3.3V, at 300 mA**
- **Input Over-current Limit**
- **Internal Compensation**
- **12-bump DSBGA Package**

APPLICATIONS

- **Power Supply for 3G/4G Power Amplifiers**
- **Cellular Phones**
- **Portable Hard Disk Drives**
- **PDAs**

DESCRIPTION

The LM3269 is buck-boost DC/DC converter designed to generate output voltages above or below a given input voltage and is particularly suitable for portable applications powered by a single-cell Li-ion battery.

The LM3269 operates at a 2.4 MHz typical switching frequency in full synchronous operation and provides seamless transitions between buck and boost operating regimes. The LM3269 operates in energy-saving Pulse Frequency Modulation (PFM) mode for increased efficiencies and current savings during low-power RF transmission modes.

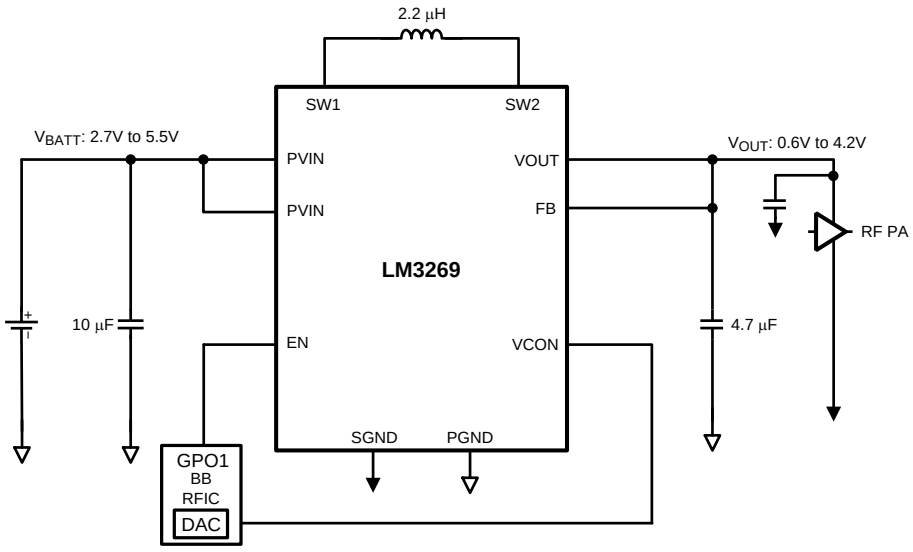
The power converter topology needs only one inductor and two capacitors. A unique internal power switch topology enables high overall efficiency.

The LM3269 is internally compensated for buck and boost modes of operation, thus providing an optimal transient response.

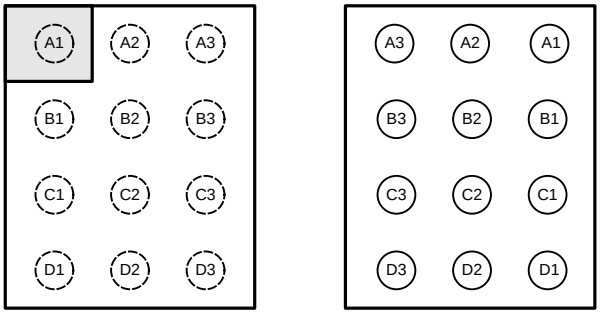
The LM3269 is available in an 12-bump lead-free DSBGA package of size 2.0 mm x 2.5 mm x 0.6 mm.

If you are considering using the LM3269 in a system design, please review the PCB Layout Considerations section at the end of this document.

TYPICAL APPLICATION CIRCUIT



Connection Diagrams and Package Mark Information



Top View Bottom View

Figure 1. 12-Bump Thin DSBGA Package, Large Bump

PIN DESCRIPTIONS

Pin #	Name	Description
A1	NC	Non Connection. Leave this pin floating; **do not** connect to PVIN or PGND.
B1	VCON	Voltage Control analog input. VCON controls the output voltage in PWM and PFM modes.
C1	FB	Feedback input to inverting input of error amplifier. Connect output voltage directly to this node at load point.
D1	VOUT	Regulated output voltage of the LM3269. Connect this to a 4.7 µF ceramic output filter capacitor to GND.
A2	NC	Non Connection. Leave this pin floating, **do not** connect to PVIN or PGND.
B2	EN	Enable pin. Pulling this pin higher than 1.2V enables part to function.
C2	SGND	Signal Ground for analog circuits and control circuitry.
D2	SW2	Switch pin for Internal Power Switches. Connect inductor between SW1 and SW2.
A3	PVIN	Power MOSFET input and power current input pin. Optional low-pass filtering may help buck and buck-boost modes for radiated EMI and noise reduction.
B3	PVIN	Power MOSFET input and power current input pin. Optional low-pass filtering may help buck and buck-boost modes for radiated EMI and noise reduction.
C3	SW1	Switch pin for Internal Power Switches. Connect inductor between SW1 and SW2.
D3	PGND	Power Ground for Power MOSFETs and gate drive circuitry.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

PVIN, VOUT to GND	−0.2V to +6.0V
EN, VCON to SGND, PGND	−0.2V to (PVIN +0.2V) w/6.0V max.
FB to PGND	−0.2V to (VOUT+0.2V) w/6.0V max.
SW1, SW2	(PGND −0.2V) to (PVIN +0.2V) w/6.0V
Continuous Power Dissipation(4)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering)	See(5)
ESD Rating(6) Human Body Model	2kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).
(5) **For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112:** *DSBGA Wafer Level Chip Scale Package* (SNVA009).
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)

OPERATING RATINGS(1)(2)(3)

Input Voltage Range	2.7V to 5.5V
Output Voltage Range	0.6V to 4.2V
Recommended Load Current	0 to 750 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(4)	−30°C to +85°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply verified performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA}), YZR Package(1)	85°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

ELECTRICAL CHARACTERISTICS[1][2]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_J = T_A \le +85°C$). Unless otherwise noted, specifications apply to the LM3269 Typical Application Circuit with: PVIN = EN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB,\ min}$	Min FB voltage	VCON = 0.2V	**0.53**	0.60	**0.67**	V
$V_{FB,\ max}$	Max FB voltage	VCON = 1.4V	**4.13**	4.2	**4.27**	
I_{Q_PWM}	Quiescent current	No switching[3]		0.9	**1.2**	mA
I_{SHDN}	Shutdown supply current	EN = 0V, VCON = 0V, SW1 = SW2 = V_{OUT} = 0V		0.02	**5.0**	µA
I_{LIM_L}	Input current limit (large)	Open Loop[4] VCON = 1.2V	**1500**	1700	**1900**	mA
I_{LIM_S}	Input current limit (small)	Open Loop[4] VCON = 0.2V	750	850		
F_{OSC_PWM}	Internal oscillator frequency	PWM	**2.1**	2.4	**2.7**	MHz
Gain	Internal gain[5]	0.2V ≤ VCON ≤ 1.4V		3		V/V
I_{EN}	EN pin pulldown current			5	10	µA
I_{VCON}	VCON pin leakage current		**−1**		**+1**	
V_{IH}	Logic high input threshold for EN		**1.2**			V
V_{IL}	Logic low input threshold for EN				**0.6**	
$I_{OUT\_LEAKAGE}$	Leakage into VOUT pin of buck-boost	EN = 0, $V_{OUT} \le 4.2V$ PVIN ≤ 5.5V			**5**	µA

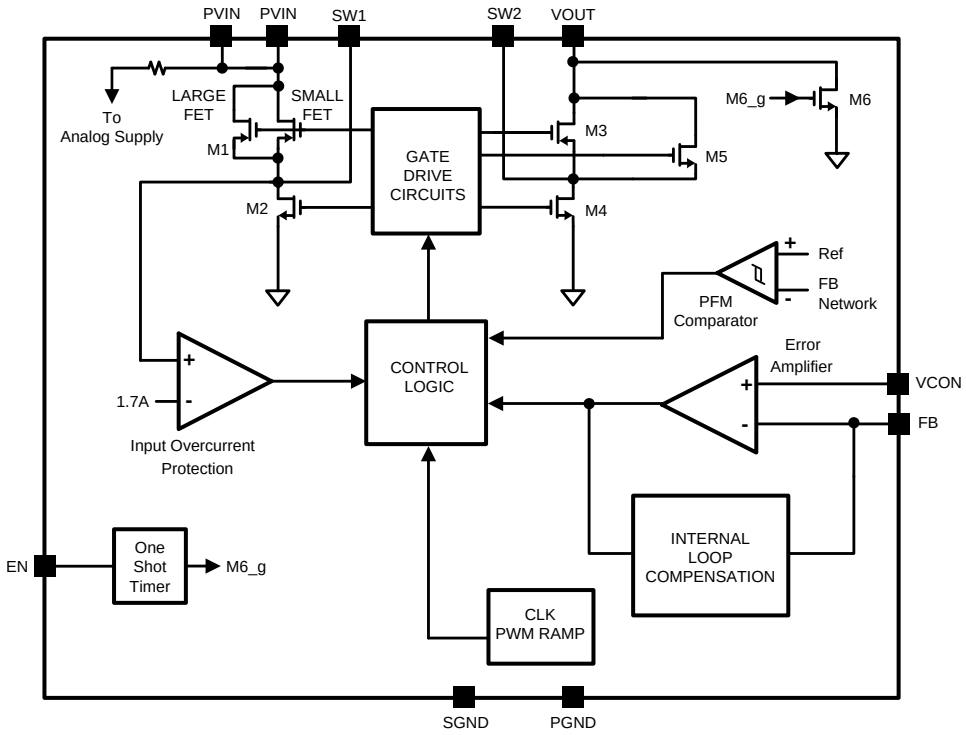
(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not verified, but do represent the most likely norm.
(3) I_Q specified here is when the part is not switching. For operating quiescent current at no load, refer to the datasheet curve.
(4) The parameters in the electrical characteristics table are tested under open loop conditions at PVIN = 3.6V.
(5) To calculate V_{OUT}, use the following equation: $V_{OUT} = VCON \times 3$.

SYSTEM CHARACTERISTICS

The following spec table entries are specified by design and verification providing the component values in the typical application circuit are used (L = 2.2 µH, DCR = 110 mΩ, MIPSZ2520D2R2/FDK; C_{IN} = 10 µF, 6.3V, C1608X5R0J106K/TDK (0603); C_{OUT} = 4.7 µF, 6.3V, C1608X5R0J475M/TDK (0603). **These parameters are not verified by production testing.** Min and Max limits in **boldface** apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ 85°C) and over the V_{BATT} = PVIN = 2.7V to 5.5V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{ON}	Turn-on time (time for output to reach 0V→90% × 3.5V)	EN = L to H, V_{BATT} = 3.7V, V_{OUT} = 3.5V, I_{OUT} = 0 mA		**35**	**50**	µs
I_{OUT_MAX}	Max output current	V_{BATT} ≥ 3.0V, V_{OUT} = 3.8V	**750**			mA
F_{OSC_PFM}	PFM operating frequency	V_{BATT} = 3.7V, V_{OUT} = 0.6V, I_{OUT} = 13mA		63		kHz
D_{MAX}	Maximum duty cycle	Boost			**50**	%
		Buck			**100**	
V_{CON_LIN}	VCON linearity	0.2V ≤ VCON ≤ 1.4V	**−2.5**		**+2.5**	%
V_{O_RIPPLE}	Ripple voltage	V_{BATT} ≥ 3.2V, 0.6 ≤ V_{OUT} ≤ 4.2V, 0 mA ≤ I_{OUT} ≤ 430 mA, T_A = 25°C		15	**50**	mV
	PFM ripple	V_{OUT} = 0.6V, I_{OUT} = 5mA		45		
	Ripple voltage in mode transition	V_{BATT} = 3.0V to 5.0V, T_R = T_F = 30s, 3.3V ≤ V_{OUT} ≤ 4.2V			**50**	
ΔV_{OUT}	Line regulation	V_{BATT} = 2.7V to 4.7V, V_{OUT} = 3.8V, I_{OUT} = 500 mA			**10**	mV
	Load regulation	I_{OUT} = 0 mA to 500 mA, V_{BATT} = 2.7V to 4.7V			**20**	
V_{OUT_TR}	VOUT rise time VCON change to 90%	V_{BATT} = 3.2V to 4.7V, V_{OUT} = 1.4V to 3.0V, 0.1 µs < $Tr_{\_VCON}$ < 1 µs, R_{LOAD} = 11.4Ω		10		µs
η	Efficiency	V_{BATT} = 3.7V, V_{OUT} = 0.6V, I_{OUT} = 10 mA		**61**		%
		V_{BATT} = 3.7V, V_{OUT} = 1.0V I_{OUT} = 20 mA		**78**		
		V_{BATT} = 3.7V, V_{OUT} = 1.4V I_{OUT} = 50 mA		**85**		
		V_{BATT} = 3.7V, V_{OUT} = 2.7V I_{OUT} = 200 mA		**95**		
		V_{BATT} = 3.7V, V_{OUT} = 3.3V, I_{OUT} = 480 mA		**94**		
		V_{BATT} = 3.0V, V_{OUT} = 3.6V, I_{OUT} = 200 mA		**95**		

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

(PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

Shutdown Current vs. Temperature (VCON = V_{OUT} = SW1 = SW2 = EN = 0V)

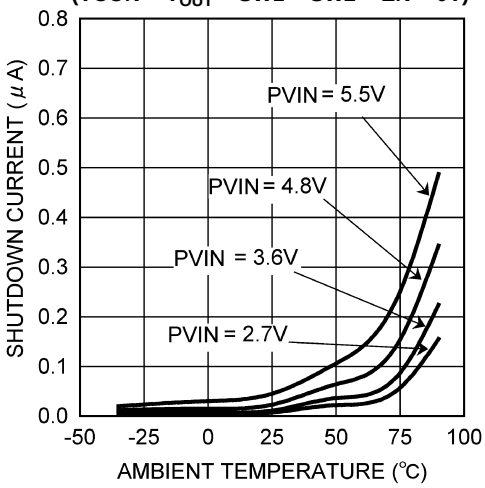


Figure 2.

Switching Frequency vs. Temperature (V_{OUT} = 3.5V, I_{OUT} = 300 mA)

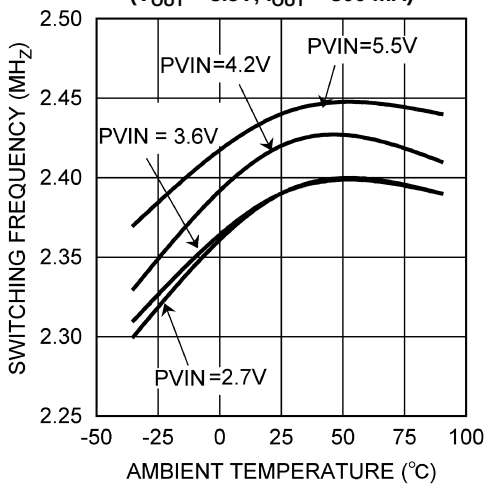


Figure 3.

VCON Voltage vs. Output Voltage (No Load)

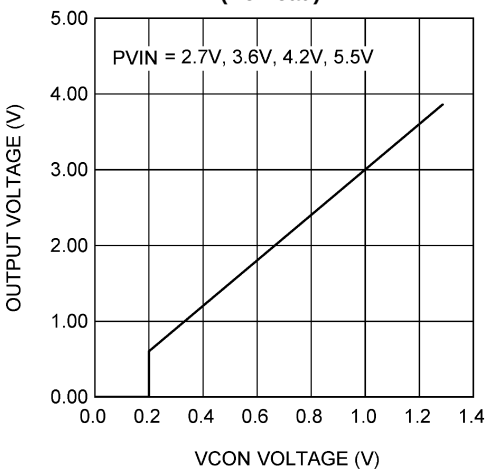


Figure 4.

PFM Efficiency (V_{OUT} = 0.6V)

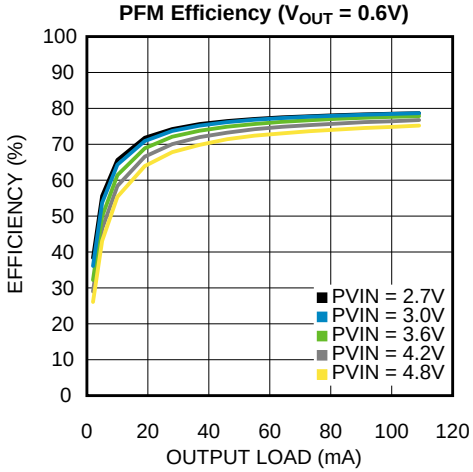


Figure 5.

PFM Efficiency (V_{OUT} = 1.0V)

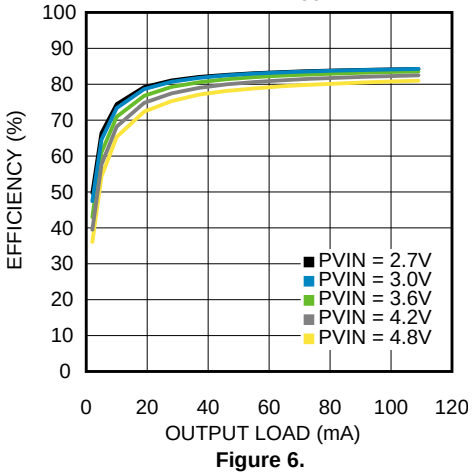


Figure 6.

PFM Efficiency (V_{OUT} = 1.4V)

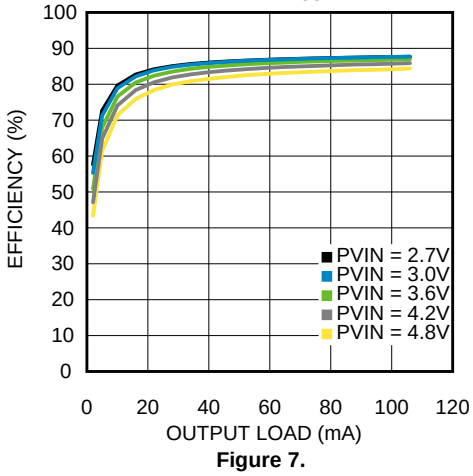


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

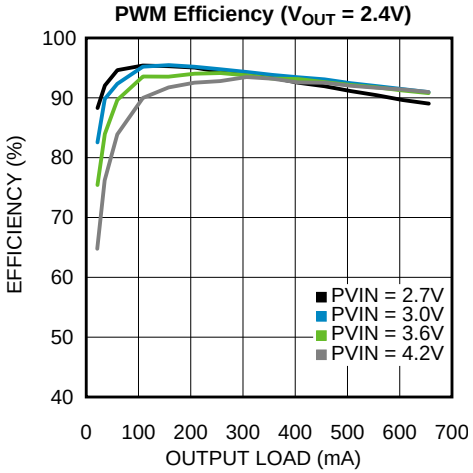


Figure 8.

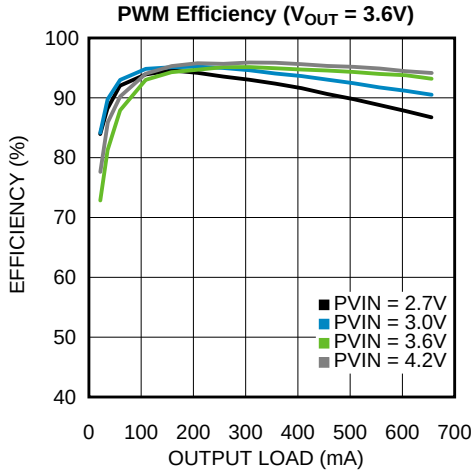


Figure 9.

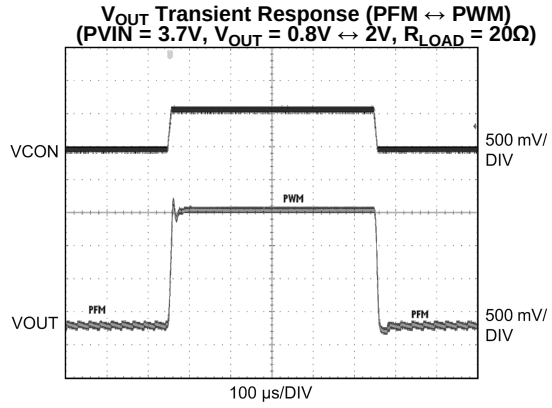


Figure 10.

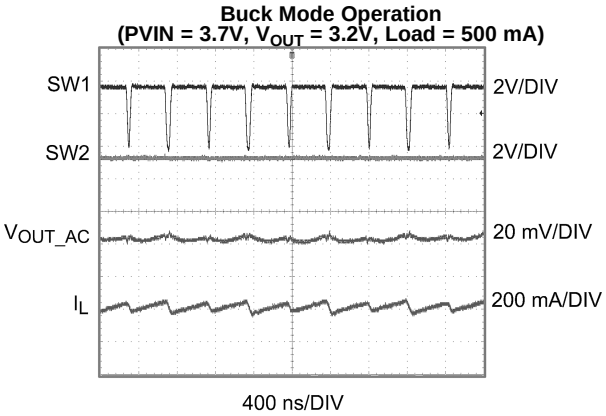


Figure 11.

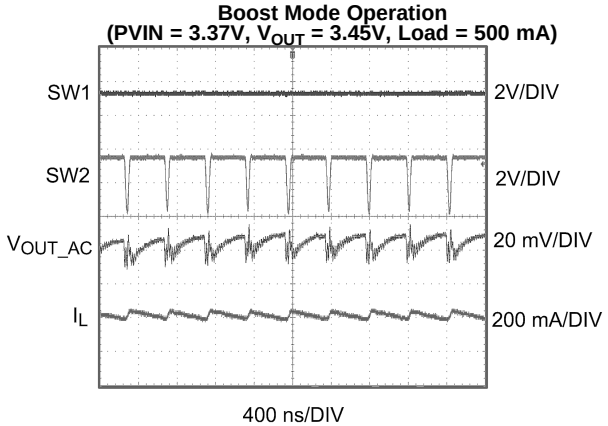


Figure 12.

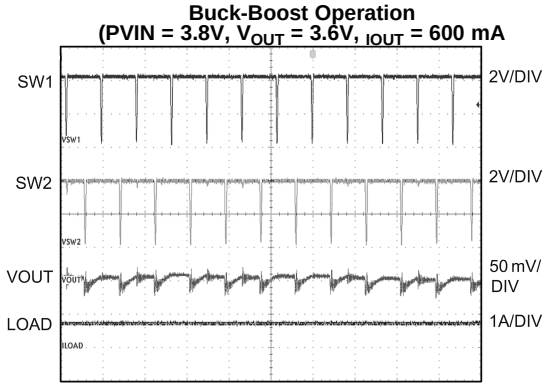


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

Startup
(PVIN = 3.6V, V_{OUT} = 3.45V, Load = 350 mA)

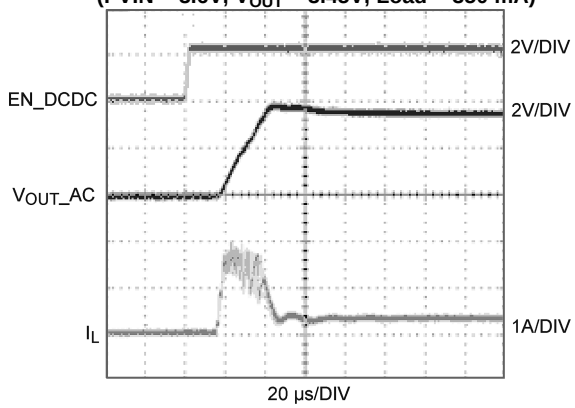


Figure 14.

Line Transient for DC/DC
(PVIN Step = 3.6V ↔ 4.2V, V_{OUT} = 3.0V, Load = 320 mA)

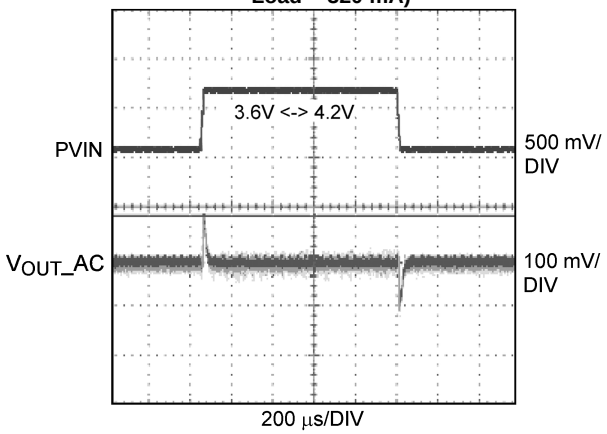


Figure 15.

Load Transient DC/DC
(PVIN = 3.8V, V_{OUT} = 3.45V)

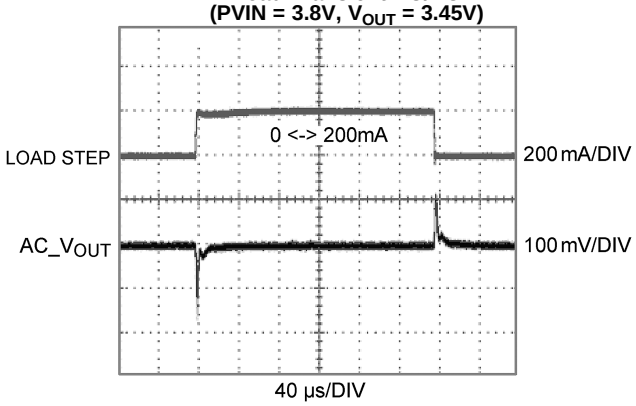


Figure 16.

OPERATION DESCRIPTION

The LM3269 buck-boost converter provides high-efficiency, low-noise power for RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery-powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency for a wide range of power levels from a single Li-Ion battery cell. The capability of the LM3269 to provide an output voltage lower than, as well as higher than, the input battery voltage enables the PA to operate with high linearity for a wide range of battery voltages, thereby extending the usable voltage range of the battery. The converter feedback loop is internally compensated for both buck and boost operation, and the architecture is such that it provides seamless transition between buck and boost modes of operation. The LM3269 operates in energy saving Pulse Frequency Modulation (PFM) mode for increased efficiencies and current savings during low-power RF transmission modes. The output voltage is dynamically programmable from 0.6V to 4.2V by adjusting the voltage on the control pin VCON without the need for external feedback resistors. The fast output voltage transient response of the LM3269 makes it suitable for adaptively adjusting the PA supply voltage depending on its transmitting power, which prolongs battery life.

Additional features include current overload protection, output over-voltage clamp, and thermal overload shutdown.

The LM3269 is constructed using a chip-scale 12-bump DSBGA package that offers the smallest possible size for space-critical applications such as cell phones, where board area is an important design consideration. Use of high switching frequency (2.4 MHz, typ.) reduces the size of external components. As shown in the Typical Application Circuit, only three external power components are required for circuit operation. Use of DSBGA package requires special design considerations for implementation. (See DSBGA Package Assembly And Use) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications where its edges are not subjected to high-intensity ambient red or infrared light. In addition, the system controller should set EN low during power-up and other low supply voltage conditions. (See Enable and Shutdown Mode below.)

Enable and Shutdown Mode

Setting the EN digital pin low (< 0.6V) places the LM3269 in shutdown mode (0.01 µA typ.). During shutdown, the output of the LM3269 is tri-stated, maintaining charge storage on the output capacitor. Setting EN high (>1.2V) enables normal operation. EN should be set low to turn off the LM3269 during power-up and under-voltage conditions when the power supply (PVIN) is less than the 2.7V minimum operating voltage.

$V_{CON,ON}$

The output is disabled when VCON is below 125 mV (typ.). It is enabled when VCON is above 150 mV (typ.). The threshold has approximately 25 mV (typ.) of hysteresis.

Dynamically Adjustable Output Voltage

The LM3269 features a dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.6V to 4.2V by changing the voltage on the analog VCON pin. This feature is useful in cell phone RF PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced; therefore the supply voltage to the PA can be reduced, promoting longer battery life. In order to adaptively adjust the supply voltage to the PA in real time in a cell-phone application, the output voltage transition should be fast enough to meet the RF transmit signal specifications. The LM3269 offers ultra-fast output voltage transition without drawing very large currents from the battery supply. For a current limit of 1700 mA (typ.), the output voltage can transition from 1.4V to 3.0V in 10 µs with a load resistance of 11.4Ω.

Seamless Buck Transition

The LM3269 features a unique internal power switch topology that improves converter efficiency, especially compared to typical non-inverting buck-boost converters. The LM3269 operates either as buck converter or a boost converter, depending upon the input and output voltage conditions. This creates a boundary between the buck and boost mode of operation. When the input battery voltage is close to the set output voltage, the converter automatically switches seamlessly such that the output voltage does not see any perturbations at the mode boundary. The excellent mode transition capability of the LM3269 enables low noise output with highest efficiency. Internal feedback loop compensation ensures stable operation in buck, boost and buck-boost mode transition operation.

Thermal Overload Protection

The LM3269 has a thermal overload protection function that operates to protect itself from short-term misuse and over-load conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. All power MOSFET switches are turned off in PWM mode. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

Pulse Frequency Modulation (PFM) Mode

The LM3269 enters PFM mode and operates with reduced switching frequency and supply current to maintain very high efficiencies when the output voltage is less than 1.5V. In PFM mode, the LM3269 will support up to 120 mA max. In PFM, if the output voltage exceeds 1.5V, the device will automatically transition into a forced PWM mode of operation.

APPLICATION INFORMATION

Setting the Output Voltage

The LM3269 features a pin-controlled variable output voltage which eliminates the need for external feedback resistors. It can be programmed for an output voltage from 0.6V to 4.2V by setting the voltage on the VCON pin, as in the following formula.

$$V_{OUT} = 3 \times VCON \quad (1)$$

When VCON is between 0.2V and 1.4V, the output voltage will follow this formula.

Output Current Capacity

The LM3269 load capability is as shown in Table 1.

Table 1. Output Voltage vs. Maximum Output Current Derating

V_{OUT}	V_{BATT}	Maximum I_{OUT} Capability
4.2V	> 3.0V	650 mA
	2.7V to 3.0V	500 mA
3.8V	> 3.0V	750 mA
	2.7V to 3.0V	600 mA
< 1.5V	2.7V to 5.5V	120 mA (in PFM mode)

Recommended External Components

Inductor Selection

A 2.2 µH inductor with a saturation current rating over 1500 mA and low inductance drop at the full DC bias condition is recommended for almost all applications. An inductor with a smaller DC resistance, such as 110 mΩ (depending on case size of resistor), should be used for good efficiency.

Table 2. Suggested Inductors (2.2 µH)

Vendor	Model	Dimensions (mm)	I_{SAT} (30% drop)	I_{RATING} (Δ40°)	DCR
FDK	MIPSZ2520D2R2	2.5 x 2.0 x 1.0	1.5A	1.1A	110 mΩ
Murata	LQH2HPN1R0NG0	2.5 x 2.0 x 1.2	2.0A	1.2A	112 mΩ
Samsung	CIG22H2R2MNE	2.5 x 2.0 x 1.2	1.9A	1.6A	116 mΩ
TDK	TFM201610A2R2M	2.0 x 1.6 x 1.0	1.7A	1.3A	180 mΩ
TOKO	DFE201612C2R2N	2.0 x 1.6 x 1.2	2.1A	1.3A	155 mΩ

Input Capacitor Selection

A ceramic input capacitor of 10 µF, 6.3V, 0603 (1608) is recommended for use in most applications. Place the input capacitor as close as possible to the PVIN pin and PGND pin of the device. A larger value of higher voltage rating may be used to improve input filtering. Use X7R, X5R, or B types; do not use Y5V or F. DC board characteristics of ceramic capacitors must be considered when selecting case sizes like 0402 (1005). The input filter capacitor supplies current to the PFET (high-side) switch in first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current.

Output Capacitor Selection

Use a 4.7 µF capacitor for the output capacitor. Use of capacitor types such as X5R, X7R are recommended for the filter. These provide an optimal balance between small size, cost, reliability, and performance for cell phones and similar applications. Table 3 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However, they have a bigger percentage drop in value with DC bias. A 0603

(1608) case size capacitor is recommended for output. For RF Power Amplifier applications, split the output capacitor between DC-DC converter and RF Power Amplifier(s). (4.7µF(0402 (1005)) + PA input cap (0402(1005)/0201(0603)) is recommended.) The optimum capacitance split is application dependent. Place all the output capacitors very close to their respective device. **If using a 4.7 µF, 0402 (1005) as the output capacitor, the total recommended actual capacitance on V_{OUT} bus should be at least 7 µF (4.7 µF + PA decoupling caps) to take into account the 0402 (1005) DC bias degradation and other tolerances (see Table 4).**

Table 3. Suggested Capacitors:

Model	Vendor
10 µF for C_{IN}	
C1608X5R0J106K (0603)	TDK
CL05A106MQ5NUN (0402)	Samsung
4.7 µF for C_{OUT}	
C1608X5R0J475M (0603)	TDK
CL05A475MQ5NRN (0402)	Samsung
C1005X5RR0J475M (0402)	TDK

Table 4. Recommended Capacitance Specifications

BUS	MIN (µF)	Typical (µF)	MAX (µF)
PVIN	-	10	-
VOUT	7		10

DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap from holding the device off the surface of the board and interfering with mounting. See Application Note AN-1112 (SNVA009) for specific instructions how to do this.

The 12-bump package used for the LM3269 has 300 micron solder balls. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 9.5 mil wide, for a section approximately 5 mil long, as a thermal relief. Then each trance should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3269 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3, B3 and D3. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light (in the red and infrared range) shining on the package's exposed die edges.

PCB LAYOUT CONSIDERATIONS

Overview

PC board layout is critical to successfully designing a DC-DC converter into a product. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

PCB

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

EMI

By its very nature, any switching converter generates electrical noise. The circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3269, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To help minimize radiated noise:

- Place the LM3269 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle (buck mode), current flows from the input filter capacitor, through the internal PFET of the LM3269 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle (buck mode), current is pulled up from ground, through the internal synchronous NFET of the LM3269 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible.

To help minimize conducted noise in the ground-plane:

- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bumps of the LM3269 and its input/output filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) by multiple vias. These multiple vias help to minimize ground bounce at the LM3269 by giving it a low-impedance ground connection.

To help minimize coupling to the DC-DC converter's own voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path (FB), as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components. If possible, connect FB bump directly to VOUT bump.

To decouple common power supply lines, series impedances may be used to strategically isolate circuits:

- Take advantage of the inherent inductance of circuit traces to reduce coupling among function blocks, by way of the power supply traces.
- Use star connection for separately routing VBATT to PVIN and VBATT_PA (VCC1).
- Inserting a single ferrite bead in-line with a power supply trace may offer a favorable tradeoff in terms of board area, by allowing the use of fewer bypass capacitors.

Manufacturing Considerations

The LM3269 package employs a 12-bump (4x4) array of 300 micron solder balls, with a 0.5 mm pad pitch. A few simple design rules will go a long way to ensuring a good layout.

- Pad size should be 0.265 ± 0.02 mm. Solder mask opening should be 0.375 ± 0.02 mm.
- As a thermal relief, connect to each pad with 9.5 mil wide, 5 mil long traces and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly. Refer to TI Application Note AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009).

LM3269 RF Evaluation Board

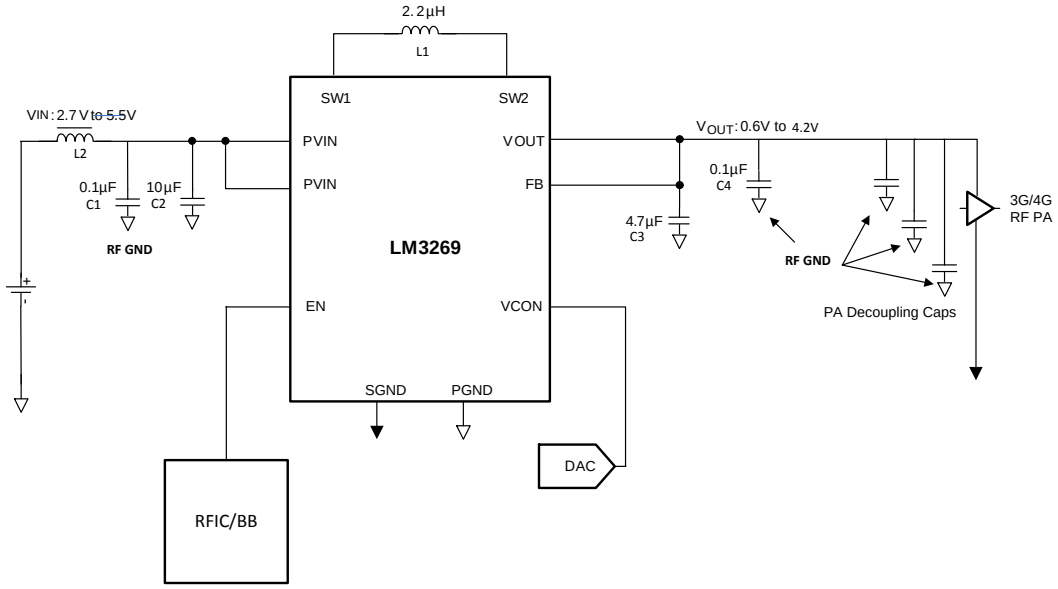


Figure 17. Simplified LM3269 RF Evaluation Board Schematic

1. Input Capacitor C2 should be placed closer to LM3269 than C1.
2. Optional to add a 100nF (C1) on input of LM3269 for high frequency filtering.
3. Bulk Output Capacitor C3 should be placed closer to LM3269 than C4.
4. Optional to add a 100nF (C4) on output of LM3269 for high frequency filtering.
5. Connect both GND terminals of C1 and C4 directly to System RF GND layer of phone board.
6. Connect bumps SGND (C2) directly to System GND.
7. TI has seen improvement in high frequency filtering for small bypass caps (C1 and C4) when they are connected to System GND instead of same ground as PGND. These capacitors should be 0201 (0603 metric) case size for minimum footprint and best high frequency characteristics.
8. A ferrite bead (L2) may help to improve high frequency noise.

Table 5. Recommended Components

Designator	Part Number	Value	Case Size	Vendor
C1*	GMR033R60J104KE19D	0.1 µF	0201 (0603 metric)	Murata
C2	C1608X5R0J106	10 µF	0603 (1608 metric)	TDK
C3	C1608X5RR0J475M	4.7 µF	0603 (1608 metric)	TDK
C4*	GRM033R60J104KE19D	0.1 µF	0201 (0603 metric)	Murata
L1	MIPSZ2520D2R2	2.2 µH	1008 (2520 metric)	FDK
L2*	BLM15AX100SN1	10Ω	0402 (1005 metric)	Murata
*Optional high frequency caps and high-frequency ferrit bead.				

Component Placement

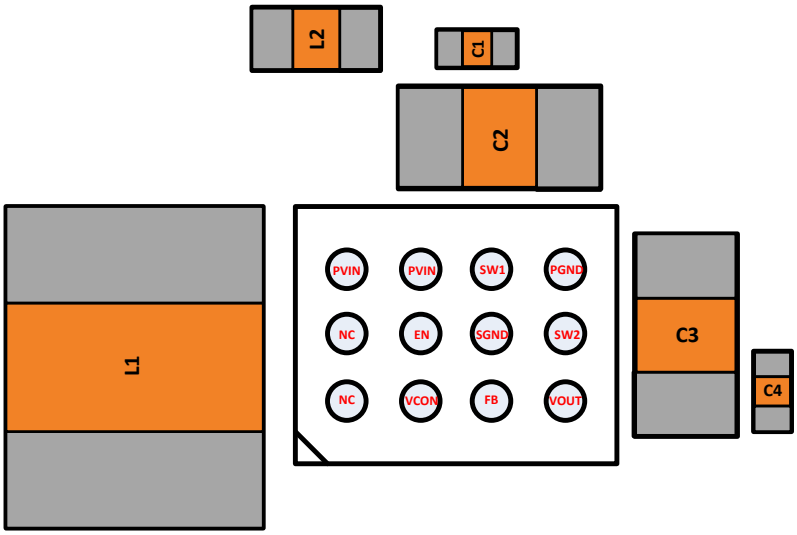


Figure 18. LM3269 Recommended Parts Placement (Top View)

PCB Considerations by Layer

VBATT

Use a star connection from VBATT to LM3269 and VBATT to PA VBATT (VCC1) connection. Do not daisy-chain VBATT connection to LM3269 circuit and then to PA device VBATT connection.

Top Layer

1. Create a PGND island as shown. PGND pads of C2 (CIN) and C3 (COUT) must be isolated from each other. This PGND island will connect to the dedicated system ground with many vias.
2. Each SW (C3) and (D2) bump will have a via in pad and an additional via next to it, to drop down the SW trace to layer
3. SGND bump (C2) will have a via in pad, and directly connecting it to the system ground.
4. FB (C1) should connect directly to the VOUT bump (D1).
5. Have PVIN vias next to optional ferrite bead.
6. Leave NC bumps (A1 and A2) floating; Do not connect to VBATT or GND

Layer 2

7. VCON and Digital logic signals may be routed on this layer.
8. VOUT (VCC2 of PA) can be routed on this layer.
9. PVIN for the LM3269 can be routed on this layer.

Layer 3

10. Each SW trace is routed on this layer. The width of each trace should be 15 mils (0.381mm) for current capabilities. Have two vias bring each SW trace up to the inductor pads.

Layer 4

11. Connect the PGND, SGND, and high Frequency vias from the top layer on this layer.

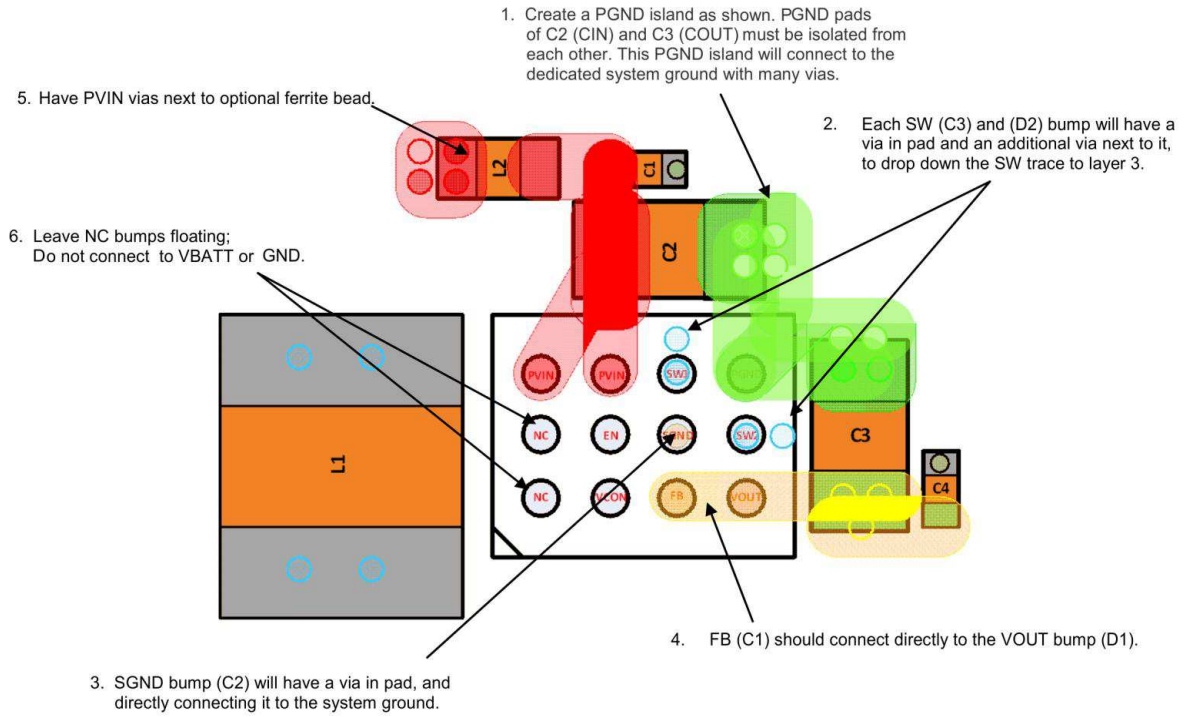


Figure 19. Top Layer

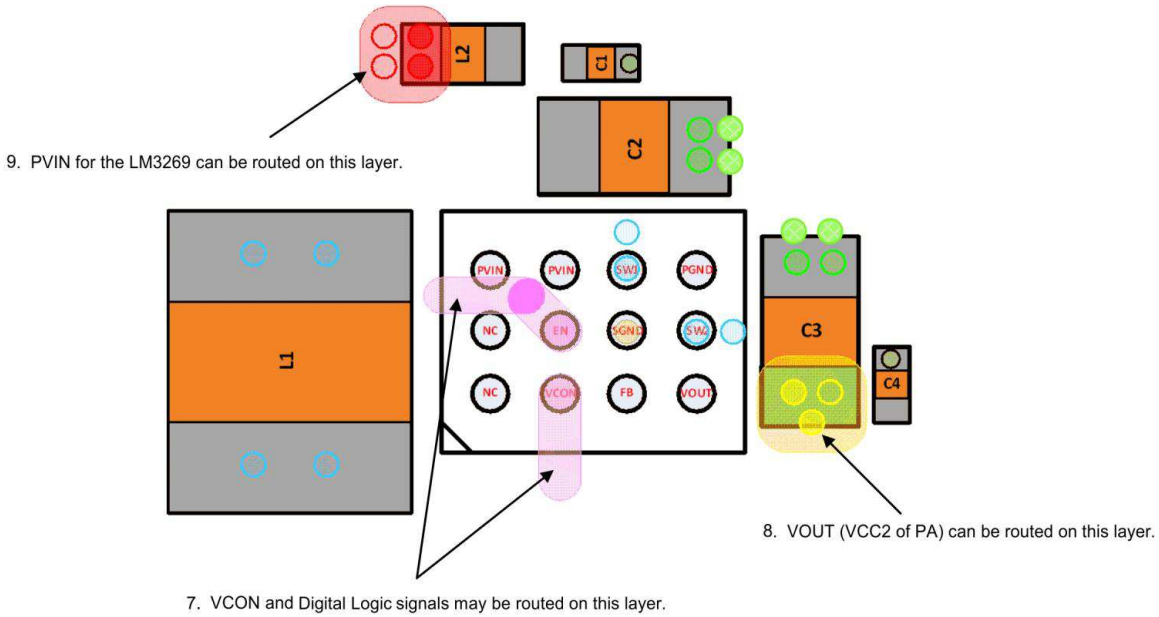


Figure 20. Board Layer 2 - Logic and PVIN Routing

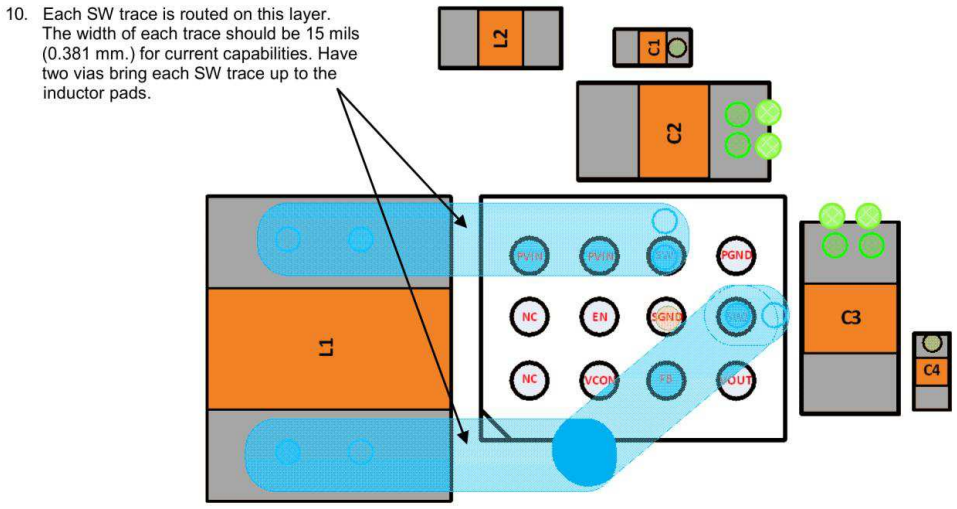


Figure 21. Board Layer 3 - SW Routing

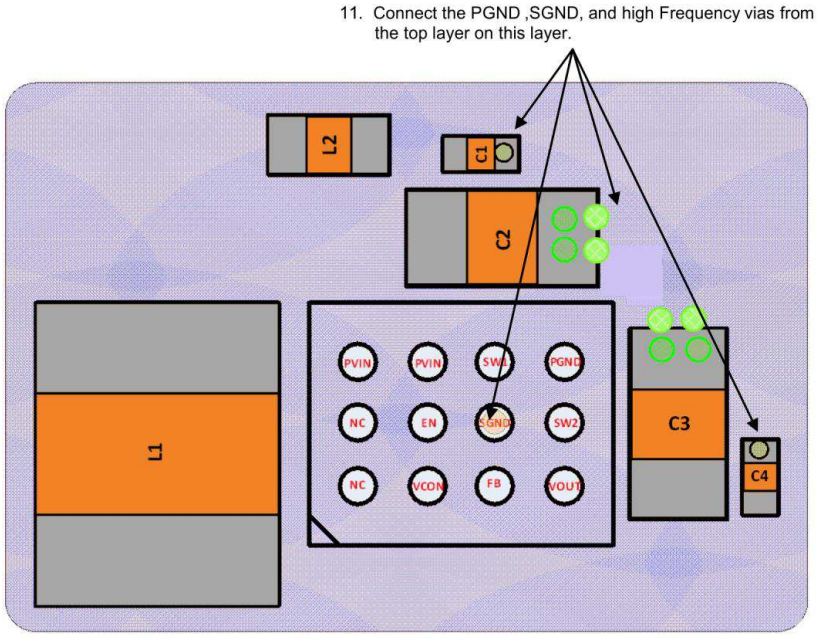


Figure 22. Board Layer 4 - System

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM3269TLE/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		3269	Samples
LM3269TLX/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		3269	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

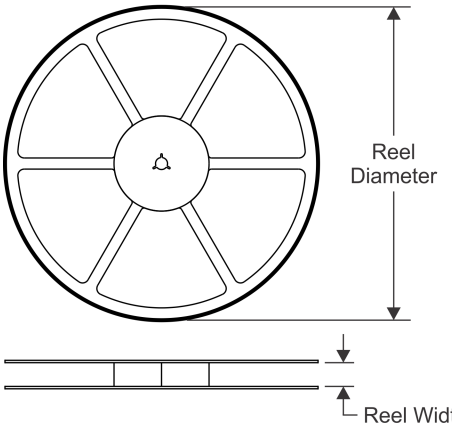
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

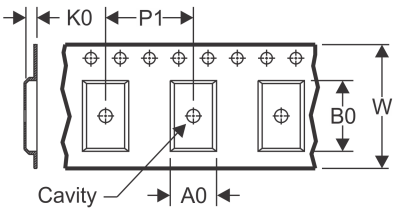
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

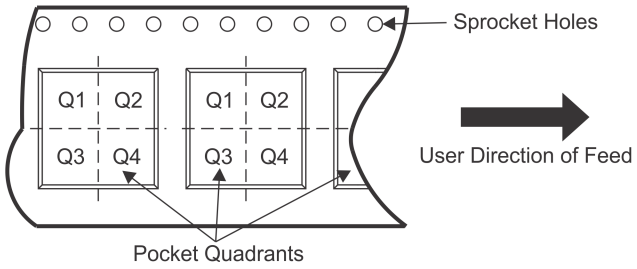


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

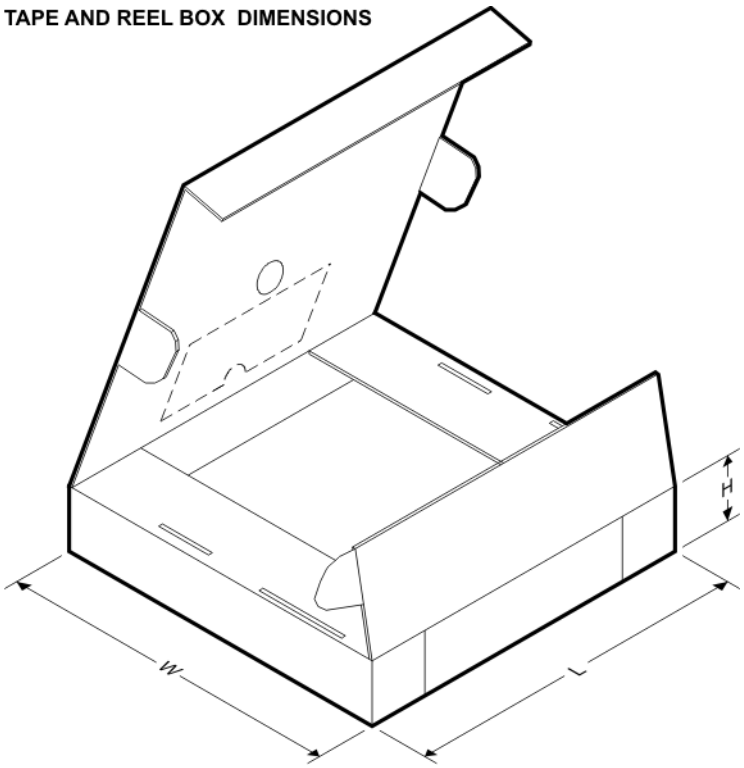
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3269TLE/NOPB	DSBGA	YZR	12	250	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1
LM3269TLX/NOPB	DSBGA	YZR	12	3000	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1

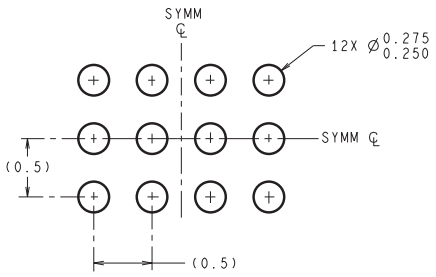
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

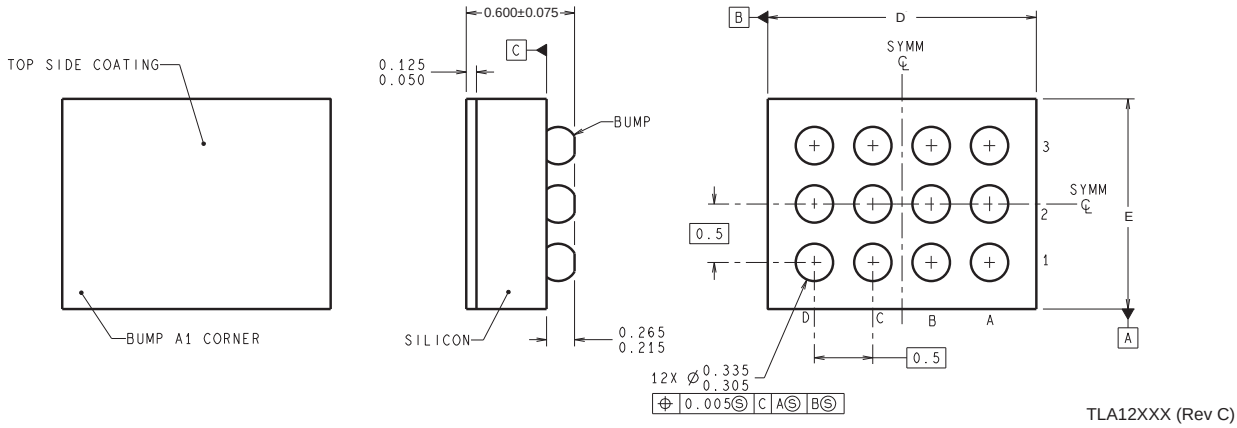
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3269TLE/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM3269TLX/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 2.529 mm, Min =2.469 mm

E: Max = 2.022 mm, Min =1.961 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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