LP8556 High-Efficiency LED Backlight Driver for Tablets

Check for Samples: LP8556

FEATURES

- **High Efficiency DC/DC Boost Converter with Integrated 0.19Ω Power MOSFET and Three Switching Frequency Options: 312 / 625 / 1250 kHz**
- **2.7V to 36V Boost Switch Input Voltage Range Supports Multi-cell Li-Ion Batteries (2.7V - 20V VDD Input Range)**
- **7V to 43V Boost Switch Output Voltage Range Supports as few as 3 WLEDs in Series per Channel and as Many as 12**
- **Configurable Channel Count (1 to 6)**
- **Up to 50 mA per Channel**
- **PWM and / or I^2C Brightness Control**
- **Phase-Shift PWM Mode Reduces Audible Noise**
- **Adaptive Dimming for Higher LED Drive Optical Efficiency**
- **Programmable Edge-rate Control and Spread Spectrum Scheme Minimize Switching Noise and Improve EMI Performance**
- **LED Fault (short/open) Detection, UVLO, TSD, OCP and OVP (up to 6 Threshold Options)**
- **Available in Tiny 20-bump, 1.715 mm x 2.376 mm x 0.6 mm, 0.4 mm pitch, DSBGA Package, and 24-pad, 4 mm x 4 mm x 0.8 mm, 0.5 mm Pitch, WQFN Package.**

APPLICATIONS

- **Tablet LCD Display LED Backlight**

DESCRIPTION

LP8556 is a white LED driver featuring an asynchronous boost converter and six high precision current sinks that can be controlled by a PWM signal or an I^2C master.

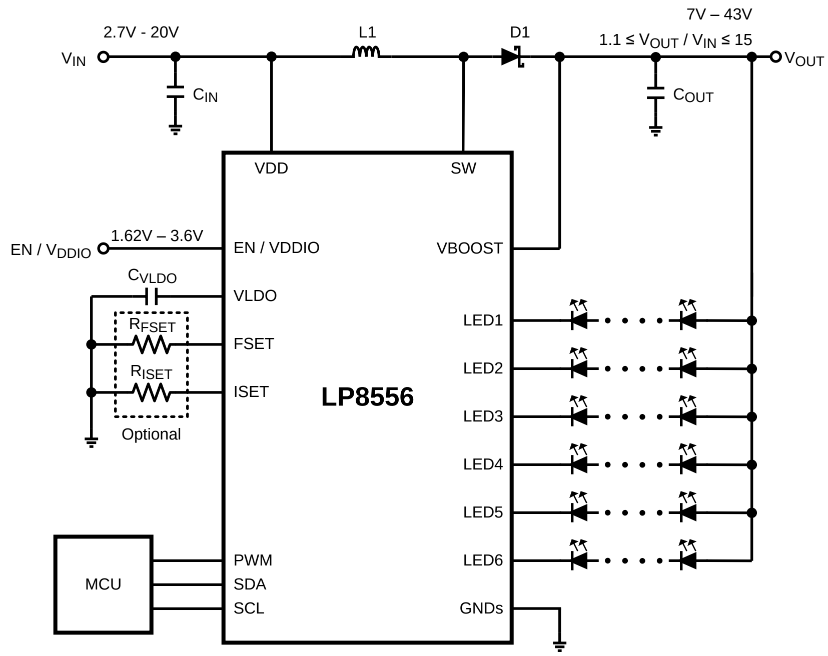
The boost converter uses adaptive output voltage control for setting the optimal LED driver voltages as low as 7V and as high as 43V. This feature minimizes the power consumption by adjusting the output voltage to the lowest sufficient level under all conditions. The converter can operate at three switching frequencies: 312, 625 and 1250 kHz settable with an external resistor or pre-configured via EPROM. Programmable slew rate control and spread spectrum scheme minimize switching noise and improve EMI performance.

LED current sinks can be set with the PWM dimming resolution of up to 15 bits. Proprietary adaptive dimming mode allows higher system power saving. In addition, phase shifted LED PWM dimming allows reduced audible noise and smaller boost output capacitors.

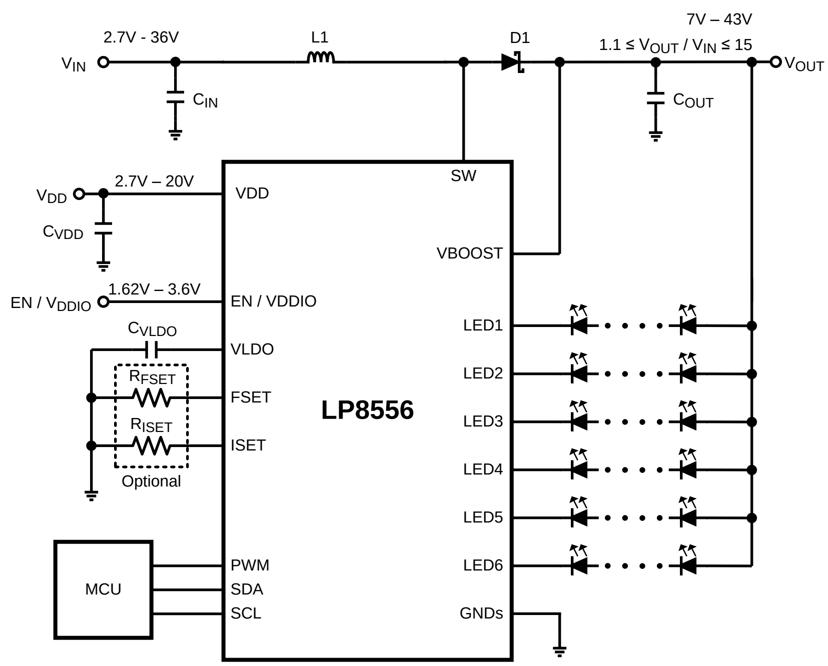
The LP8556 has a full set of safety features that ensure robust operation of the device and external components. The set consists of input under-voltage lockout, thermal shutdown, over-current protection, up to 6 levels of over-voltage protection, LED open and short detection.

The LP8556 operates over the ambient temperature range of -30°C to +85°C. It is available in space saving 20-bump DSBGA and 24-pad WQFN packages.

Typical Application



Typical Application (2)



Recommended Inductance for the Boost Power Stage

Assumes 20 mA as the maximum LED current per string and 3.3V as the maximum LED forward voltage.

Number of LED Strings	Number of LEDs per String	Boost Input Voltage Range [V]	L1 Inductance [µH]		
			f_{SW} = 1250 kHz	f_{SW} = 625 kHz	f_{SW} = 312 kHz
6	6	2.7V - 4.4V	3.3 µH - 6.8 µH	6.8 µH - 15 µH	10 µH - 33 µH
		5.4V - 8.8V	10 µH - 22 µH	22 µH - 47 µH	47 µH - 100 µH
6	8	2.7V - 4.4V	4.7 µH - 10 µH	10 µH - 15 µH	22 µH - 33 µH
		5.4V - 8.8V	10 µH - 22 µH	22 µH - 68 µH	47 µH - 100 µH
4	10	5.4V - 8.8V	6.8 µH - 22 µH	22 µH - 47 µH	47 µH - 100 µH
4	12	5.4V - 8.8V	10 µH - 22 µH	22 µH - 47 µH	33 µH - 100 µH

Recommended Capacitances for the Boost and LDO Power Stages (1)

Switching Frequency [kHz]	C_{IN} [µF]	C_{OUT} [µF]	C_{VLDO} [µF]
1250	2.2	4.7	10
625	2.2	4.7	10
312	4.7	10	10

(1) Capacitance of Multi Layer Ceramic Capacitors (MLCC) can change significantly with the applied DC voltage. Use capacitors with good capacitance vs. DC bias characteristics. In general, MLCC in bigger packages have lower capacitance de-rating than physically smaller capacitors.

Connection Diagrams (DSBGA)

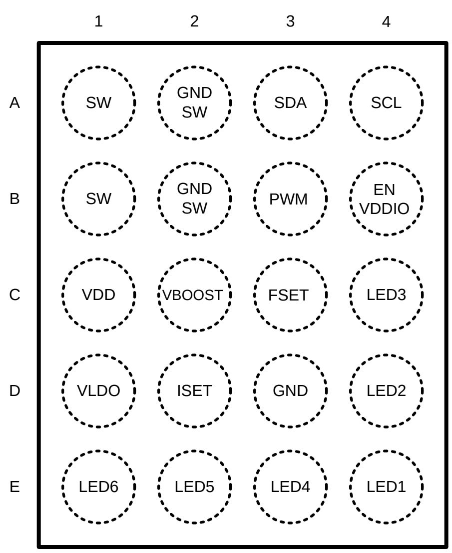


Figure 1. 20-bump DSBGA Package – Top View See Package Number YFQ0020

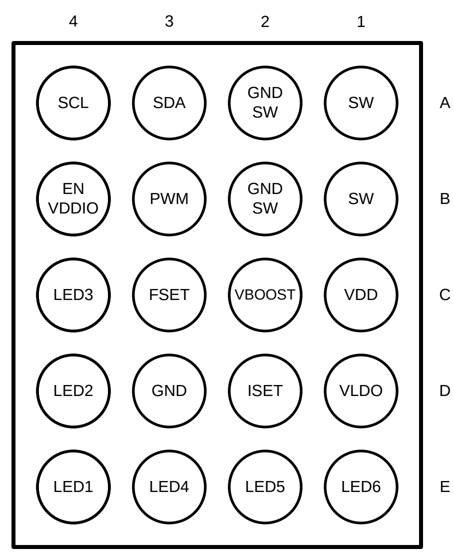


Figure 2. Bottom View

Connection Diagrams (WQFN)

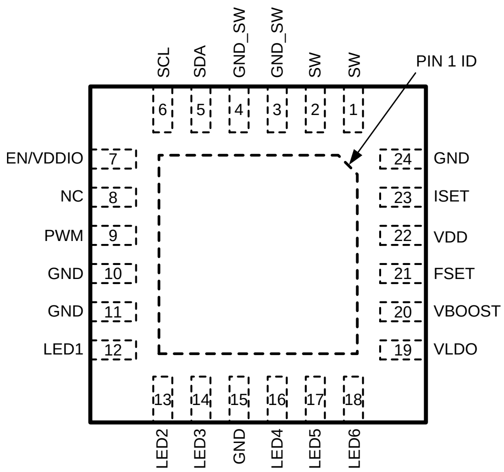


Figure 3. 24–pin WQFN Package – Top View
See Package Number RTW0024A

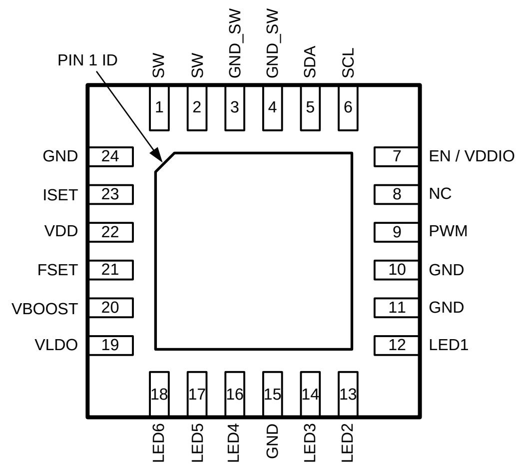


Figure 4. Bottom View

PIN DESCRIPTIONS

uSMD	WQFN	Name	Type (1)	Description
A1, B1	1, 2	SW	A	A connection to the drain terminal of the integrated power MOSFET.
A2, B2	3, 4	GND_SW	G	A connection to the source terminal of the integrated power MOSFET.
A3	5	SDA	I/O	I^2C data input/output pin.
A4	6	SCL	I	I^2C clock input pin.
B3	9	PWM	I	PWM dimming input. Supply a 75 Hz to 25 kHz PWM signal to control dimming. This pin must be connected to GND if unused.
B4	7	EN / VDDIO	P	Dual purpose pin serving both as a Chip enable and as a power supply reference for PWM, SDA and SCL inputs. Drive this pin with a logic gate capable of sourcing a minimum of 1 mA.
C1	22	VDD	P	Device power supply pin. Provide 2.7V to 20V supply to this pin. This pin is an input of the internal LDO regulator. The output of the internal LDO is what powers the device.
C2	20	VBOOST	A	Boost converter output pin. The internal Feedback (FB) and Over-voltage Protection (OVP) circuitry monitors the voltage on this pin. Connect the converter output capacitor bank close to this pin.
C3	21	FSET	A	A connection for setting the boost frequency and PWM output dimming frequency by using an external resistor. Connect a resistor, R_{FSET}, between this pin and the ground reference (See Table 5). This pin may be left floating if PWM_FSET_EN=0 AND BOOST_FSET_EN=0 (See Table 9).
C4	14	LED3	A	LED driver - current sink terminal. If unused, it may be left floating.
D1	19	VLDO	P	Internal LDO output pin. Connect a capacitor, C_{VLDO}, between this pin and the ground reference.
D2	23	ISET	A	A connection for the LED current set resistor. Connect a resistor, R_{ISET}, between this pin and the ground reference. This pin may be left floating if ISET_EN=0 (See Table 9).
D3	10, 11, 15, 24, DAP	GND	I	Ground pin.
D4	13	LED2	A	LED driver - current sink terminal. If unused, it may be left floating.
E1	18	LED6	A	LED driver - current sink terminal. If unused, it may be left floating.
E2	17	LED5	A	LED driver - current sink terminal. If unused, it may be left floating.
E3	16	LED4	A	LED driver - current sink terminal. If unused, it may be left floating.
E4	12	LED1	A	LED driver - current sink terminal. If unused, it may be left floating.
-	8	NC	-	No Connect pin.

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Digital Input Pin, I/O: Digital Input/Output Pin

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

	Min	Max	Units
V_{DD}	-0.3	24	V
Voltage on Logic Pins (SCL, SDA, PWM)	-0.3	6	V
Voltage on Analog Pins (VLDO, EN / VDDIO)	-0.3	6	V
Voltage on Analog Pins (FSET, ISET)	-0.3	VLDO+0.3	V
V (LED1...LED6,SW, VBOOST)	-0.3	50	V
Junction Temperature (T_{J-MAX})[3]		125	°C
Storage Temperature Range	-65	150	°C
Maximum Lead Temperature (Soldering)		260	°C
HBM[4]	2		kV
CDM[5]	500		V

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125 °C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(4) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Operating Ratings[1][2]

	Min	Max	Units
VDD Range	2.7	20	V
EN / VDDIO Range	1.62	3.6	V
V (LED1...LED6, SW, VBOOST)	0	48	V
Junction Temperature Range (T_J)	-30	125	°C
Ambient Temperature Range (T_A)	-30	85	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pins.

Thermal Properties[1]

	Min	Max	Units
Junction-to-Ambient Thermal Resistance (θ_{JA}), TMD Package	40	73	°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}), SQA Package	35	50	°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics[1][2]

Limits in standard typeface are for T_A = 25 °C. Limits in **boldface** type apply over the full operating ambient temperature range (-30 °C ≤ T_A ≤ +85 °C). Unless otherwise specified: VDD=12V, EN / VDDIO = 1.8V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDIO}	Supply voltage for digital I/Os		1.62		3.6	V
V_{DD}	Input voltage for the internal LDO		2.7		20	V
I_{DD}	Standby Supply Current	EN / VDDIO=0V, LDO disabled			**1.6**	µA
	Normal Mode Supply Current	LDO enabled, Boost disabled		0.9	1.5	mA
		LDO enabled, Boost enabled, no load		2.2	3.65	
f_{OSC}	Internal Oscillator Frequency Accuracy		-4 **-7**		+4 **+7**	%
V_{LDO}	LDO Output Voltage	V_{DD} ≥ 3.1V	2.95	3.05	3.15	V
		2.7V ≤ V_{DD} < 3.1V		V_{DD} - 0.05		
T_{TSD}	Thermal Shutdown Threshold	See[3]		150		°C
T_{TSD_hyst}	Thermal Shutdown Hysteresis			20		°C

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(3) Guaranteed by design and not tested in production.

Boost Converter Electrical Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{DS_ON}	Switch ON resistance	I_{SW} = 0.5A		0.19		Ω
V_{BOOST_MIN}	Boost minimum output voltage	VBOOST_RANGE = 0 VBOOST_RANGE = 1		7 16		V
V_{BOOST_MAX}	Boost maximum output voltage	VBOOST_MAX = 100, VBOOST_RANGE = 0 VBOOST_MAX = 101, VBOOST_RANGE = 0 VBOOST_MAX = 110, VBOOST_RANGE = 0 VBOOST_MAX = 111, VBOOST_RANGE = 0	19.0 24.0 28.0 32	21 25 30 34	22 27 32 37	V
		VBOOST_MAX = 010, VBOOST_RANGE = 1 VBOOST_MAX = 011, VBOOST_RANGE = 1 VBOOST_MAX = 100, VBOOST_RANGE = 1 VBOOST_MAX = 101, VBOOST_RANGE = 1 VBOOST_MAX = 110, VBOOST_RANGE = 1 VBOOST_MAX = 111, VBOOST_RANGE = 1	17.9 22.8 27.8 32.7 37.2 41.8	21 25 30 34.5 39 43	23.1 27.2 31.5 36.6 40.8 44.2	V
I_{LOAD_MAX}	Maximum continuous output load current	V_{IN} = 3V, V_{OUT} = 18V		220		mA
		V_{IN} = 3V, V_{OUT} = 24V		160		
		V_{IN} = 3V, V_{OUT} = 30V		120		
V_{OUT}/V_{IN}	Conversion ratio[2]	f_{SW} = 625 kHz			15	
		f_{SW} = 1250 kHz			12	
f_{SW}	Switching frequency	BOOST_FREQ = 00 BOOST_FREQ = 01 BOOST_FREQ = 10		312 625 1250		kHz
V_{OVP}	Over-voltage protection voltage	VBOOST_RANGE = 1		V_{BOOST} + 1.6V		V
V_{UVLO}	V_{IN} under-voltage lockout threshold	UVLO_EN=1				V
		UVLO_TH = 0, falling UVLO_TH = 1, falling		2.5 5.2		
V_{UVLO_hyst}	V_{UVLO} hysteresis	V_{UVLO}[rising] V_{UVLO}[falling], UVLO_TH = 0		50		mV
		V_{UVLO}[rising] V_{UVLO}[falling], UVLO_TH = 1		100		
t_{PULSE}	Switch minimum pulse width	no load		50		ns

(1) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(2) Guaranteed by design and not tested in production.

Boost Converter Electrical Characteristics[1] (continued)

Symbol	Parameter	Condition		Min	Typ	Max	Units
$t_{STARTUP}$	Startup time	See[3]			8		ms
I_{SW_LIM}	SW pin current limit[4]	IBOOST_LIM_2X = 0	IBOOST_LIM = 00 IBOOST_LIM = 01 IBOOST_LIM = 10 IBOOST_LIM = 11	0.66 0.88 1.12 1.35	0.9 1.2 1.5 1.8	1.16 1.40 1.73 2.07	A
		IBOOST_LIM_2X = 1	IBOOST_LIM = 00 IBOOST_LIM = 01 IBOOST_LIM = 10		1.6 2.1 2.6		A
ΔV_{SW} / t_{off_on}	SW pin slew rate during OFF to ON transition	EN_DRV3 = 0 AND EN_DRV2 = 0 EN_DRV3 = 0 AND EN_DRV2 = 1 EN_DRV3 = 1 AND EN_DRV2 = 1			3.7 5.3 7.5		V / ns
ΔV_{SW} / t_{on_off}	SW pin slew rate during ON to OFF transition	EN_DRV3 = 0 AND EN_DRV2 = 0 EN_DRV3 = 0 AND EN_DRV2 = 1 EN_DRV3 = 1 AND EN_DRV2 = 1			1.9 4.4 4.8		V / ns
Δt_{ON} / t_{SW}	Peak to peak switch ON time deviation to SW period ratio (Spread spectrum feature)	SSCLK_EN = 1			1		%

(3) Startup time is measured from the moment boost is activated until the VBOOST crosses 90% of its target value.
(4) 1.8A is the maximum I_{SW_LIM} supported with the DSBGA package. For applications requiring the I_{SW_LIM} to be greater than 1.8A and up to 2.6A, WQFN package should be considered.

LED Driver Electrical Characteristics[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LED\_LEAKAGE}$	Leakage current	Outputs LED1...LED6, V_{OUT} = 48V		0.1	**1**	µA
I_{LED_MAX}	Maximum Sink Current LED1...LED6			50		mA
I_{LED}	LED Current Accuracy[2]	Output current set to 23 mA	-3 **-4**	1	+3 **+4**	%
I_{MATCH}	Matching	Output current set to 23 mA		0.5		%
PWM_{DUTY}	LED PWM output pulse duty cycle[3]	100 Hz < f_{PWM} ≤ 200 Hz	0.02		100	%
		200 Hz < f_{PWM} ≤ 500 Hz	0.02		100	
		500 Hz < f_{PWM} ≤ 1 kHz	0.02		100	
		1 kHz < f_{PWM} ≤ 2 kHz	0.04		100	
		2 kHz < f_{PWM} ≤ 5 kHz	0.1		100	
		5 kHz < f_{PWM} ≤ 10 kHz	0.2		100	
		10 kHz < f_{PWM} ≤ 20 kHz	0.4		100	
		20 kHz < f_{PWM} ≤ 30 kHz	0.6		100	
		30 kHz < f_{PWM} ≤ 39 kHz	0.8		100	
f_{LED}	PWM output frequency	PWM_FREQ = 1111		38.5		kHz
V_{SAT}	Saturation Voltage[4]	Output current set to 23 mA		200		mV

(1) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(2) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1 to OUT6), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN/AVG). The largest number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts. Note that some manufacturers have different definitions in use.
(3) Guaranteed by design and not tested in production.
(4) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1V.

PWM Interface Characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PWM}	PWM Frequency Range(2)		75		25000	Hz
t_{MIN_ON}	Minimum Pulse ON time			1		µs
t_{MIN_OFF}	Minimum Pulse OFF time			1		
$t_{STARTUP}$	Turn on delay from standby to backlight on	PWM input active, VDDIO pin transitions from 0V to 1.8V.		10		ms
t_{STBY}	Turn off delay	PWM input low time for turn off		50		ms
PWM_{RES}	PWM Input Resolution	f_{IN} < 9.0 kHz		8		bits

(1) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.
(2) Guaranteed by design and not tested in production.

Logic Interface Characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Units
Logic Inputs (PWM, SDA, SCL)						
V_{IL}	Input Low Level				**0.3 X VDDIO**	V
V_{IH}	Input High Level		**0.7 X VDDIO**			V
I_I	Input Current	(V_{DDIO} = 0V or 3.6V) AND (V_I = 0V or 3.6V)	**-1.0**		**1.0**	µA
Logic Outputs (SDA)						
V_{OL}	Output Low Level	I_{OUT} = 3 mA (pull-up current)		0.3	**0.4**	V
I_L	Output Leakage Current	V_{OUT} = 5V	**-1.0**		**1.0**	µA

(1) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

I²C Serial Bus Timing Parameters (SDA, SCL)(1)

Symbol	Parameter	Limit Min	Limit Max	Units
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load Parameter for Each Bus Line Load of 1 pF corresponds to 1 ns.	10	200	ns

(1) Guaranteed by design and not tested in production.

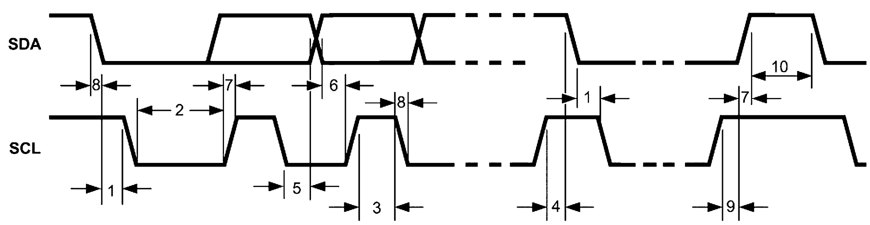


Figure 5. I2C Compatible Timing

Typical Performance Characteristics

Unless otherwise specified: V_{IN} = 3.8V, C_{VLDO} = 10 µF, L1 = 4.7 µH, C_{IN} = 2.2 µF, C_{OUT} = 4.7 µF, f_{SW} = 1.25 MHz

Boost and LED Drive Efficiency, V_{IN} = 3.8V

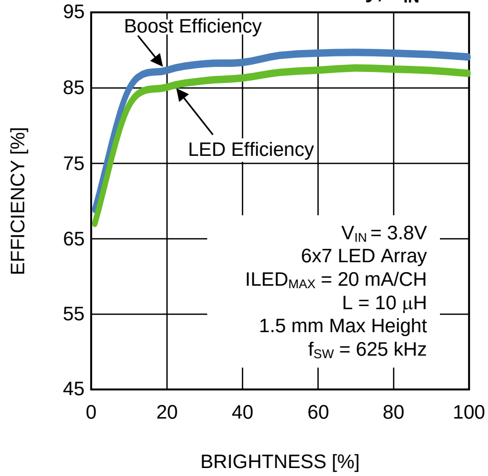


Figure 6.

Boost and LED Drive Efficiency, V_{IN} = 6.3V

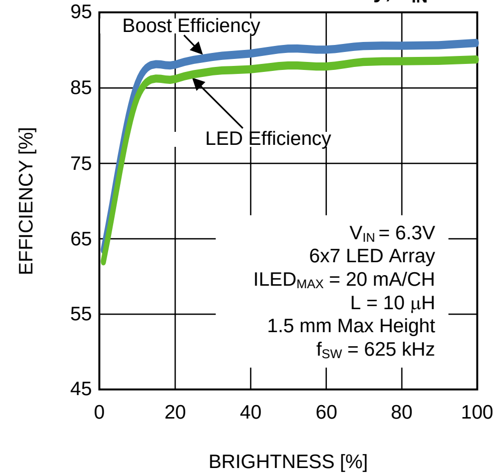


Figure 7.

Boost and LED Drive Efficiency, V_{IN} = 8.6V

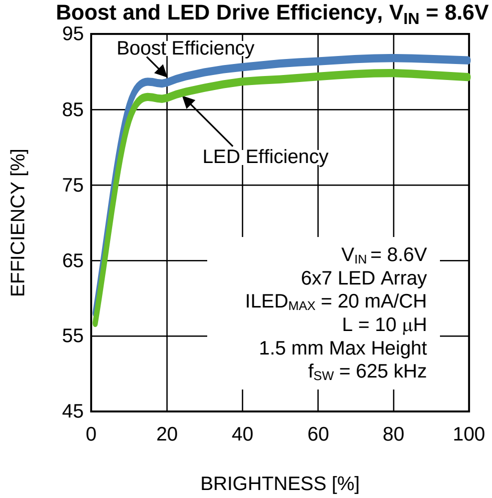


Figure 8.

Boost and LED Drive Efficiency, V_{IN} = 12.9V

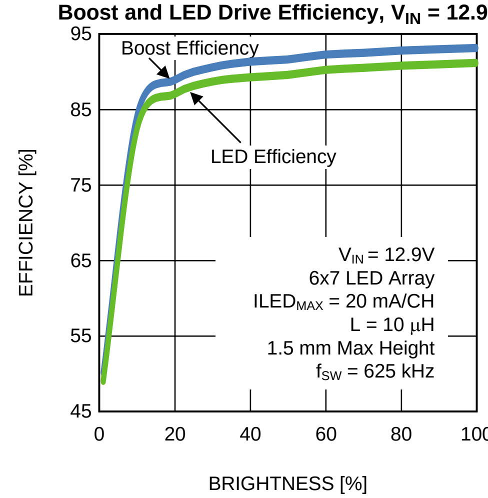


Figure 9.

Optical Efficiency with 10" Panel

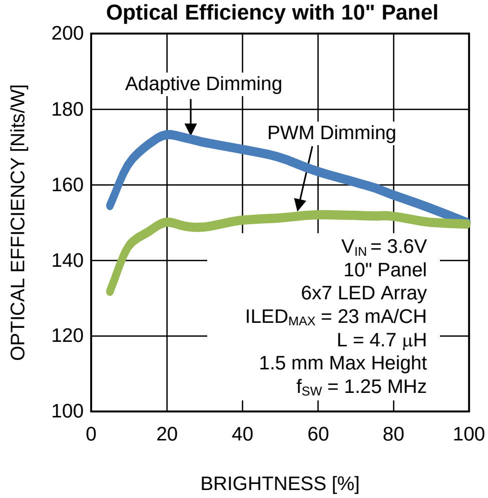


Figure 10.

Luminance as a Function of Brightness

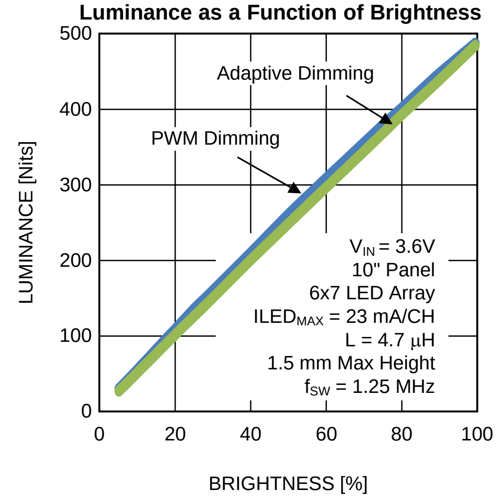


Figure 11.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.8V, C_{VLDO} = 10 µF, L1 = 4.7 µH, C_{IN} = 2.2 µF, C_{OUT} = 4.7 µF, f_{SW} = 1.25 MHz

Input Power as a Function of Brightness

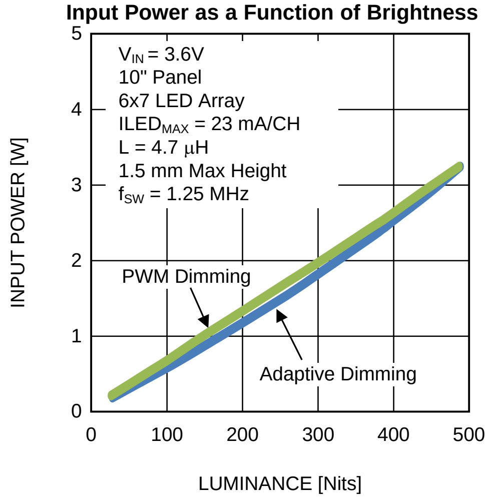


Figure 12.

Power Savings with Adaptive Dimming When Compared to PWM Dimming

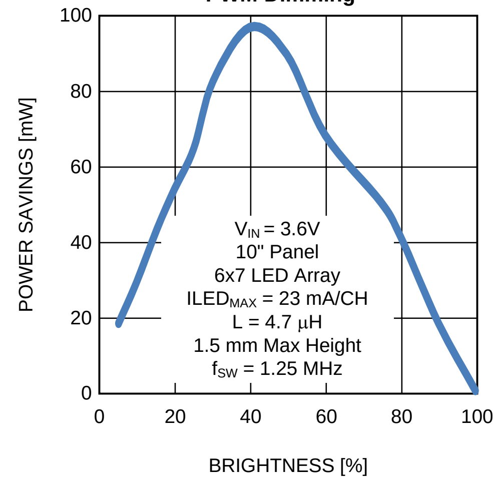


Figure 13.

Steady State Operation Waveforms

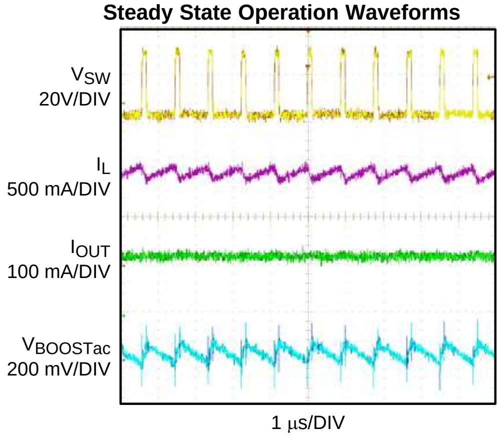


Figure 14.

Start-up Waveforms

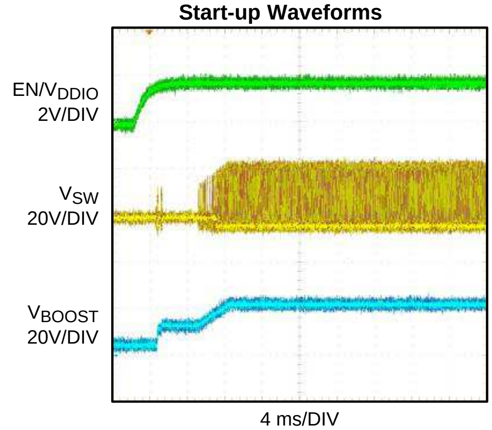


Figure 15.

FUNCTIONAL OVERVIEW

LP8556 is a white LED driver featuring an asynchronous boost converter and six high precision current sinks that can be controlled by a PWM signal or an I^2C master.

The boost converter uses adaptive output voltage control for setting the optimal LED driver voltages as high as 43V. This feature minimizes the power consumption by adjusting the voltage to the lowest sufficient level under all conditions. The converter can operate at three switching frequencies: 312, 625 and 1250 kHz pre-configured via EPROM or settable via an external resistor. Programmable slew rate control and spread spectrum scheme minimize switching noise and improve EMI performance.

LED current sinks can be set with the PWM dimming resolution of up to 15 bits. Proprietary adaptive dimming mode allows higher system power saving. In addition, phase shifted LED PWM dimming allows reduced audible noise and smaller boost output capacitors.

The LP8556 has a full set of safety features that ensure robust operation of the device and external components. The set consists of input under-voltage lockout, thermal shutdown, over-current protection, up to six levels of over-voltage protection, LED open and short detection.

Block Diagram

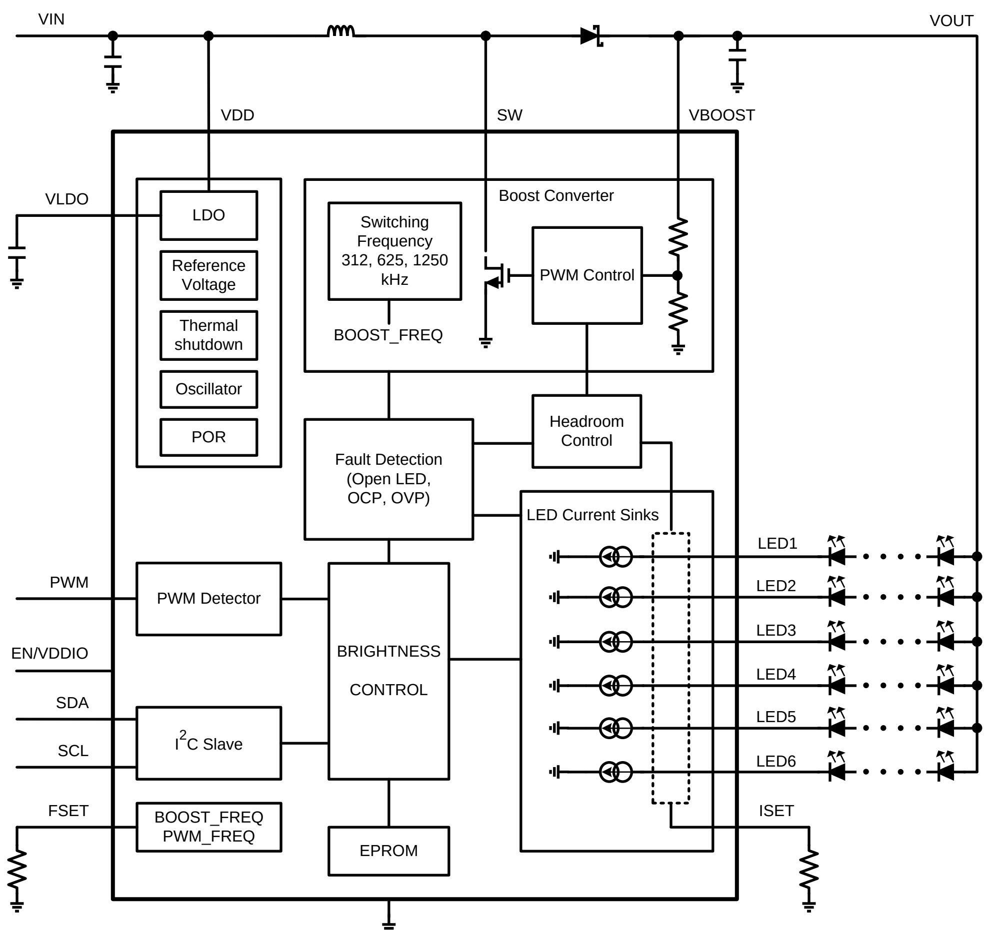


Figure 16. LP8556 Block Diagram

Boost Converter Overview

OPERATION

The LP8556 boost DC/DC converter generates a 7V to approximately 43V boost output voltage from a 2.7V to 36V boost input voltage. The boost output voltage minimum, maximum value and range can be set digitally by pre-configuring EPROM memory (VBOOST_RANGE, VBOOST and VBOOST_MAX fields).

The converter is a magnetic switching PWM mode DC/DC boost converter with a current limit. It uses CPM (current programmed mode) control, where the inductor current is measured and controlled with the feedback. During startup, the soft-start function reduces the peak inductor current. LP8556 has an internal 20 MHz oscillator which is used for clocking the boost. The following figure shows the boost block diagram.

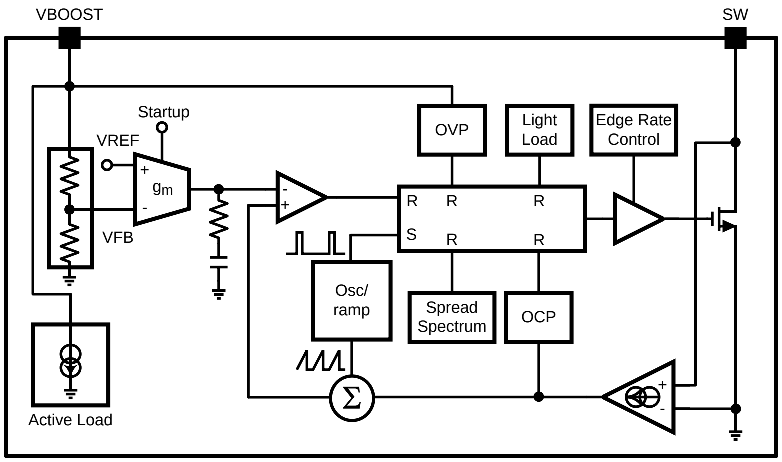


Figure 17. LP8556 Boost Converter Block Diagram

SETTING BOOST SWITCHING FREQUENCY

The LP8556 boost converter switching frequency can be set either by an external resistor (BOOST_FSET_EN = 1 selection), R_{FSET}, or by pre-configuring EPROM memory with the choice of boost frequency (BOOST_FREQ field). Table 1 summarizes setting of the switching frequency. Note that the R_{FSET} is shared for setting the PWM dimming frequency in addition to setting the boost switching frequency. Setting the boost switching frequency and PWM dimming frequency using an external resistor is separately shown in Table 5.

Table 1. Configuring Boost Switching Frequency via EPROM

R_{FSET} [Ω]	BOOST_FSET_EN	BOOST_FREQ[1:0]	f_{SW} [kHz]
don't care	0	00	312
don't care	0	01	625
don't care	0	10	1250
don't care	0	11	undefined
(1)	1	don't care	(1)

(1) See Table 5

OUTPUT VOLTAGE CONTROL

LP8556 supports two modes of controlling the Boost output voltage, Adaptive Boost Voltage Control and Manual Boost Output Control. Each of the two modes are detailed below.

ADAPTIVE CONTROL:

LP8556 supports a mode of output voltage control called Adaptive Boost Control mode. In this mode, the voltage at the LED pins is periodically monitored by the control loop and adaptively adjusted to the optimum value based on the comparator thresholds set using LED DRIVER_HEADROOM, LED_COMP_HYST, BOOST_STEP_UP, BOOST_STEP_DOWN fields in the EPROM. Settings under LED DRIVER_HEADROOM along with LED_COMP_HYST fields determine optimum boost voltage for a given condition. Boost voltage will be raised if the voltage measured at any of the LED strings falls below the threshold setting determined with LED DRIVER_HEADROOM field. Likewise, boost voltage will be lowered if the voltage measured at any of the LED strings is above the combined setting determined under LED DRIVER_HEADROOM and LED_COMP_HYST fields. LED_COMP_HYST field serves to fine tune the headroom voltage for a given peak LED current. The boost voltage up/down step size can be controlled with the BOOST_STEP_UP and BOOST_STEP_DN fields.

The initial boost voltage is configured with the VBOOST field. This field also sets the minimum boost voltage. The VBOOST_MAX field sets the maximum boost voltage. When an LED pin is open, the monitored voltage will never have enough headroom and the adaptive mode control loop will keep raising the boost voltage. The VBOOST_MAX field allows the boost voltage to be limited to stay under the voltage rating of the external components.

NOTE

Only LED strings that are enabled are monitored and PS_MODE field determines which LED strings are enabled.

This Adaptive mode is selected using ADAPTIVE bit set to 1 (CFGA EPROM Register) and is the recommended mode of boost control.

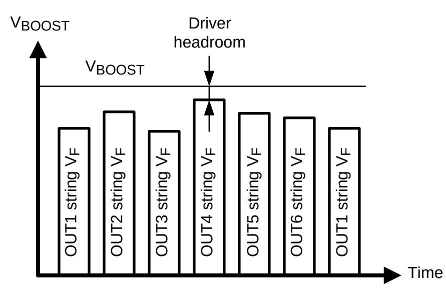


Figure 18. Boost Adaptive Control Principle

MANUAL CONTROL:

User can control the boost output voltage with the VBOOST EPROM field when adaptive mode is not used. The following expression shows the relationship between the boost output voltage and the VBOOST field:

$$V_{BOOST} = V_{BOOST\_MIN} + 0.42 * VBOOST[dec] \quad (1)$$

The expression is only valid when the calculated values are between the minimum boost output voltage and the maximum boost output voltage. The minimum boost output voltage is set with the VBOOST_RANGE field. The maximum boost output voltage is set with the VBOOST_MAX EPROM field.

EMI REDUCTION

The LP8556 features two EMI reduction schemes.

First scheme, Programmable Slew Rate Control, uses a combination of three drivers for boost switch. Enabling all three drivers allows boost switch on/off transition times to be the shortest. On the other hand, enabling just one driver allows boost switch on/off transition times to be the longest. The longer the transition times, the lower the switching noise on the SW terminal. It should also be noted that the shortest transition times bring the best efficiency as the switching losses are the lowest.

EN_DRV2 and EN_DRV3 bits in the EPROM determine the boost switch driver configuration. Refer to the SW pin slew rate parameter listed under Boost Converter Electrical Characteristics(2) for the slew rate options.

The second EMI reduction scheme is the spread spectrum scheme which deliberately spreads the frequency content of the boost switching waveform, which inherently has a narrow bandwidth, makes the switching waveform's bandwidth wider and ultimately reduces its EMI spectral density.

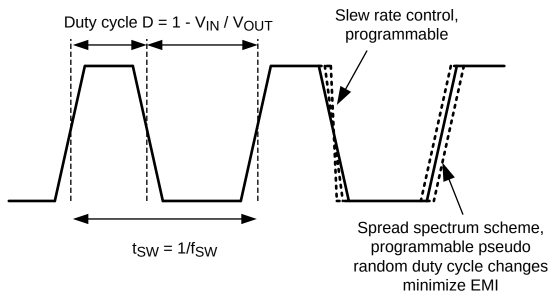


Figure 19. Principles of EMI Reduction Schemes

(2) Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Brightness Control

LP8556 enables various methods of brightness control. The brightness can be controlled using an external PWM signal or the Brightness register accessible by users via an I^2C interface or both. How these two input sources are selected and combined is set by the BRT_MODE EPROM bits and described in the following sections, Figure 20, and Table 2. The LP8556 can also be preconfigured via EPROM memory to allow direct and unaltered brightness control by an external PWM signal. This mode of operation is obtained by setting PWM_DIRECT EPROM bit to '1' (CFG5[7] = 1).

BRT_MODE = 00

With BRT_MODE = 00, the LED output is controlled by the PWM input duty cycle. The PWM detector block measures the duty cycle at the PWM pin and uses this 16-bit value to generate an internal to the device PWM data. Before the output is generated, the PWM data goes through the PWM Curve Shaper block. Then, the data goes into the Adaptive Dimming function which determines the range of the PWM and Current control as described in OUTPUT DIMMING SCHEMES. The outcome of the Adaptive Dimming function is 12-bit Current and / or up to 6 PWM output signals. The current is then passed through the non-linear compensation block while the output PWM signals are channeled through the Dither block.

BRT_MODE = 01

With BRT_MODE = 01, the PWM output is controlled by the PWM input duty cycle and the Brightness register. The PWM detector block measures the duty cycle at the PWM pin and uses this 16-bit value to generate the PWM data. Before the output is generated, the PWM data is first multiplied with BRT[7:0] register, then it goes through the PWM Curve Shaper block. Then, the data goes into the Adaptive Dimming function which determines the range of the PWM and Current control as described in OUTPUT DIMMING SCHEMES . The outcome of the Adaptive Dimming function is 12-bit Current and / or up to 6 PWM output signals. The current is then passed through the non-linear compensation block while the output PWM signals are channeled through the Dither block.

BRT_MODE = 10

With BRT_MODE = 10, the PWM output is controlled only by the Brightness register. From BRT[7:0] register, the data goes through the PWM Curve Shaper block. Then, the data goes into the Adaptive Dimming function which determines the range of the PWM and Current control as described in OUTPUT DIMMING SCHEMES . The outcome of the Adaptive Dimming function is 12-bit Current and / or up to 6 PWM output signals. The current is then passed through the non-linear compensation block while the output PWM signals are channeled through the Dither block.

BRT_MODE = 11

With BRT_MODE = 11, the PWM control signal path is similar to the path when BRT_MODE = 01 except that the PWM input signal is multiplied with BRT[7:0] data after the Curve Shaper block.

Table 2. Brightness Control Methods Truth Table

PWM_DIRECT	BRT_MODE [1:0]	Brightness Control Source	Output ILED Form
0	00	External PWM Signal	Adaptive. See OUTPUT DIMMING SCHEMES
0	01	External PWM Signal and Brightness Register (multiplied before Curve Shaper)	
0	10	Brightness Register	
0	11	External PWM Signal and Brightness Register (multiplied after Curve Shaper)	
1	don't care	External PWM Signal	Same as the external PWM input

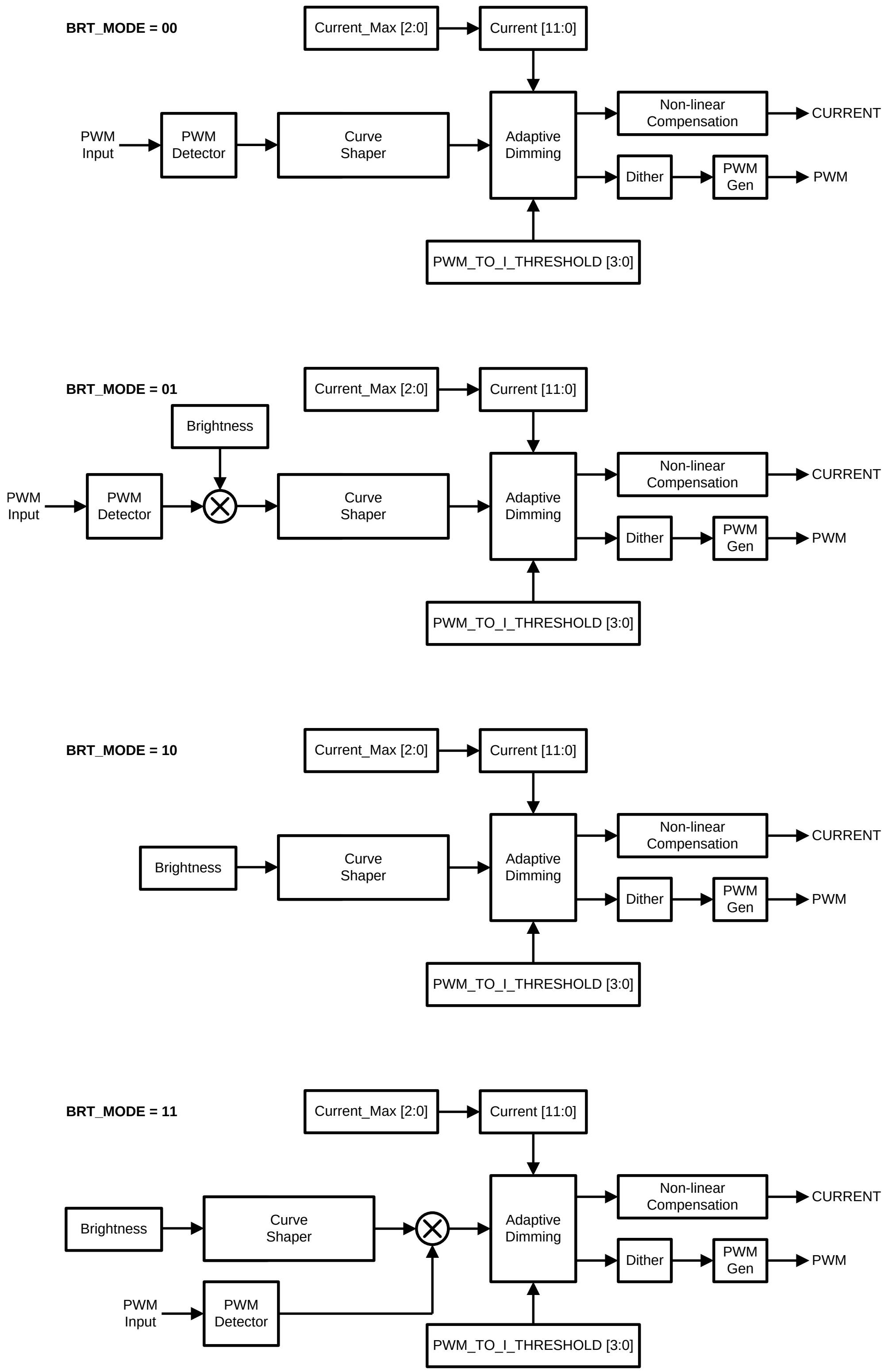


Figure 20. Brightness Control Signal Path Block Diagrams

OUTPUT DIMMING SCHEMES

The LP8556 supports three types of output dimming control methods: PWM Control, Pure Current Control and Adaptive Dimming (Hybrid PWM & Current) Control.

PWM Control

PWM control is the traditional way of controlling the brightness using PWM of the outputs with a same LED current across the entire brightness range. Brightness control is achieved by varying the duty cycle proportional to the input PWM. PWM frequency is set either using an external set Resistor (R_{FSET}) or using the PWM_FREQ EPROM field. The maximum LED current is set either using an external set Resistor (R_{ISET}) and CURRENT and CURRENT_MAX EPROM bits or just using the CURRENT and CURRENT_MAX EPROM bits. Note that the output PWM signal is de-coupled and generated independent of the input PWM signal eliminating display flicker issues and allowing better noise immunity

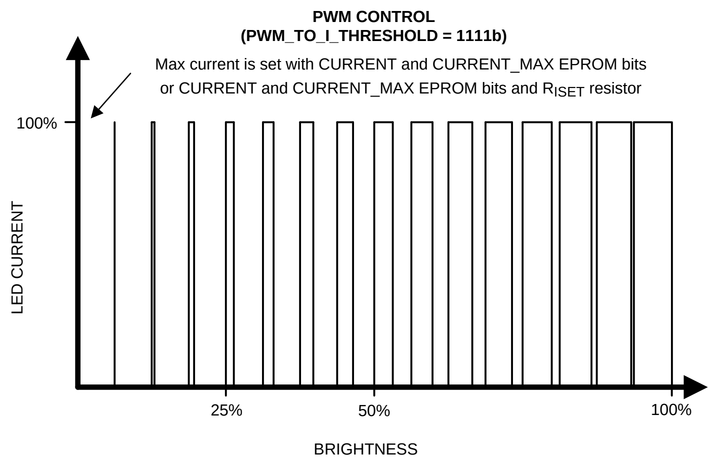


Figure 21. PWM Only Output Dimming Scheme

Pure Current Control

In Pure Current Control mode, brightness control is achieved by changing the LED current proportionately from maximum value to a minimum value across the entire brightness range. Like in PWM Control mode, the maximum LED current is set either using an external set Resistor (R_{ISET}) and CURRENT and CURRENT_MAX EPROM bits or just using the CURRENT and CURRENT_MAX EPROM bits. Current resolution in this mode is 12-bits.

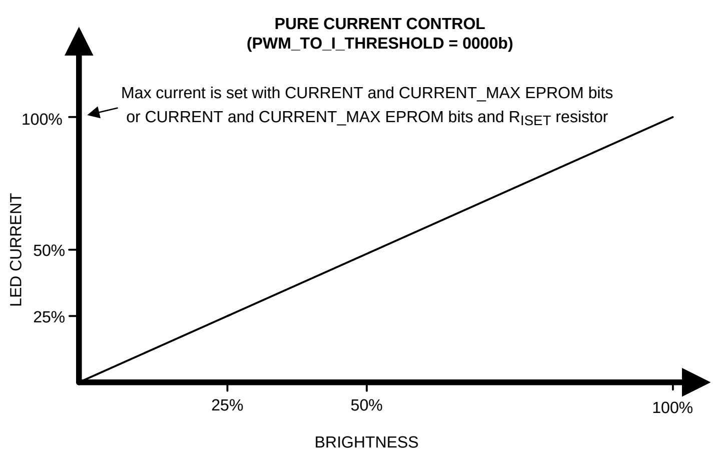


Figure 22. Pure Current / Analog Output Dimming Scheme

Adaptive Control

Adaptive dimming control combines PWM Control and Pure Current Control dimming methods. With the adaptive dimming, it is possible to achieve better optical efficiency from the LEDs compared to pure PWM control while still achieving smooth and accurate control at low brightness levels. Current resolution in this mode is 12-bits. Switch point from Current to PWM control can be set with the PWM_TO_I_THRESHOLD EPROM field from 0% to 100% of the brightness range to get good compromise between good matching of the LEDs brightness/white point at low brightness and good optical efficiency.

PWM frequency is set either using an external set Resistor (R_{FSET}) or using the PWM_FREQ EPROM bits. The maximum LED current is set either using an external set Resistor (R_{ISET}) and CURRENT and CURRENT_MAX EPROM bits or just using the CURRENT and CURRENT_MAX EPROM bits.

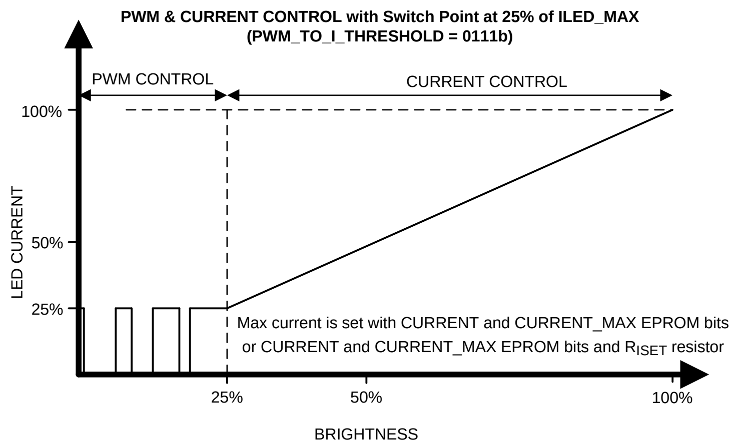


Figure 23. Adaptive Output Dimming Scheme

SETTING FULL SCALE LED CURRENT

The maximum or full scale LED current is set either using an external set Resistor (R_{ISET}) and CURRENT and CURRENT_MAX EPROM bits or just using the CURRENT and CURRENT_MAX EPROM bits. Table 3 summarizes setting of the full scale LED current.

Table 3. Setting Full Scale LED Current

R_{ISET} [Ω]	ISET_EN	CURRENT_MAX	CURRENT[11:0]	Full Scale ILED [mA]
don't care	0	000	FFFh	5
don't care	0	001	FFFh	10
don't care	0	010	FFFh	15
don't care	0	011	FFFh	20
don't care	0	100	FFFh	23
don't care	0	101	FFFh	25
don't care	0	110	FFFh	30
don't care	0	111	FFFh	50
don't care	0	000 - 111	001h - FFFh	(1)
24k	1	000	FFFh	5
24k	1	001	FFFh	10
24k	1	010	FFFh	15
24k	1	011	FFFh	20
24k	1	100	FFFh	23
24k	1	101	FFFh	25
24k	1	110	FFFh	30
24k	1	111	FFFh	50
12k - 100k	1	000 - 111	001h - FFFh	(1)

(1) See CFG0

SETTING PWM DIMMING FREQUENCY

LP8556 PWM dimming frequency can be set either by an external resistor, R_{FSET}, or by pre-configuring EPROM Memory (CFG5 register, PWM_FREQ[3:0] bits). Table 4 summarizes setting of the PWM dimming frequency. Note that the R_{FSET} is shared for setting the boost switching frequency, too. Setting the boost switching frequency and PWM dimming frequency using an external resistor is shown in Table 5.

Table 4. Configuring PWM Dimming Frequency via EPROM

R_{FSET} [kΩ]	PWM_FSET_EN	PWM_FREQ[3:0]	f_{PWM} [Hz] (Resolution)
don't care	0	0000	4808 (12-bit)
		0001	6010 (11-bit)
		0010	7212 (11-bit)
		0011	8414 (11-bit)
		0100	9616 (11-bit)
		0101	12020 (10-bit)
		0110	13222 (10-bit)
		0111	14424 (10-bit)
		1000	15626 (10-bit)
		1001	16828 (10-bit)
		1010	18030 (10-bit)
		1011	19232 (10-bit)
		1100	24040 (9-bit)
		1101	28848 (9-bit)
		1110	33656 (9-bit)
		1111	38464 (9-bit)
(1)	1	don't care	(1)

(1) See Table 5

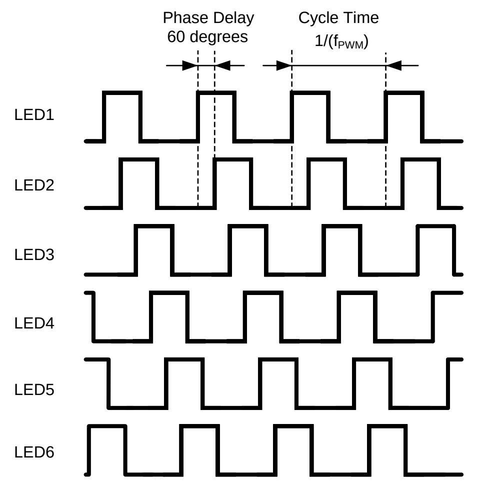
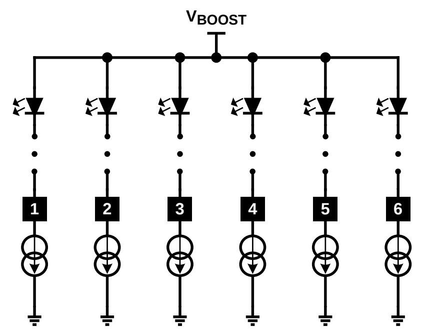
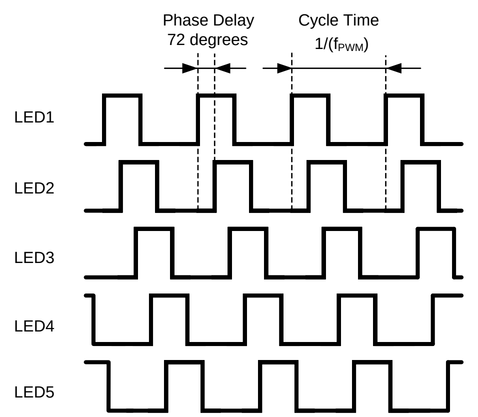
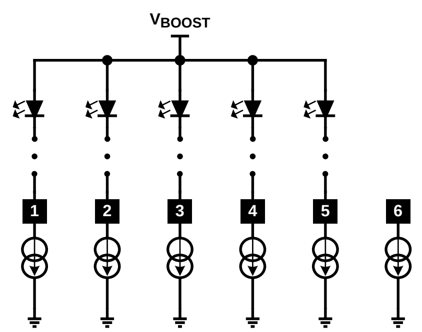
Table 5. Setting Switching and PWM Dimming Frequency with an External Resistor

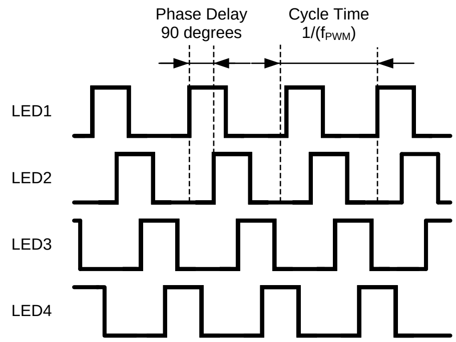
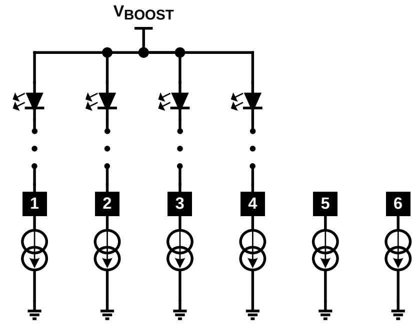
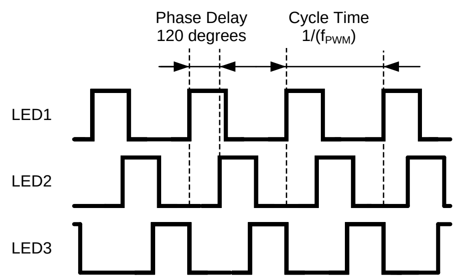
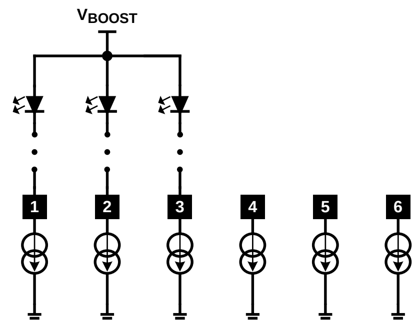
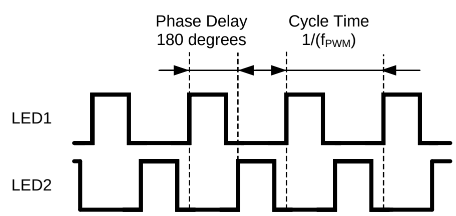
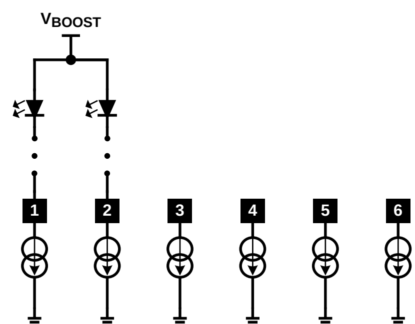
R_{FSET} [kΩ] (Tolerance)	f_{SW} [kHz]	f_{PWM} [Hz] (Resolution)
Floating or FSET pin pulled HIGH	1250	9616 (11-bit)
470k - 1M (±5%)	312	2402 (12-bit)
300k, 330k (±5%)	312	4808 (12-bit)
200k (±5%)	312	6010 (11-bit)
147k, 150k, 154k, 158k (±1%)	312	9616 (11-bit)
121k (±1%)	312	12020 (10-bit)
100k (±1%)	312	14424 (10-bit)
86.6k (±1%)	312	16828 (10-bit)
75.0k (±1%)	312	19232 (10-bit)
63.4k (±1%)	625	2402 (12-bit)
52.3k, 53.6k (±1%)	625	4808 (12-bit)
44.2k, 45.3k (±1%)	625	6010 (11-bit)
39.2k (±1%)	625	9616 (11-bit)
34.0k (±1%)	625	12020 (10-bit)
30.1k (±1%)	625	14424 (10-bit)
26.1k (±1%)	625	16828 (10-bit)
23.2k (±1%)	625	19232 (10-bit)
20.5k (±1%)	1250	2402 (12-bit)
18.7k (±1%)	1250	4808 (12-bit)
16.5k (±1%)	1250	6010 (11-bit)
14.7k (±1%)	1250	9616 (11-bit)
13.0k (±1%)	1250	12020 (10-bit)
11.8k (±1%)	1250	14424 (10-bit)
10.7k (±1%)	1250	16828 (10-bit)
9.76k (±1%)	1250	19232 (10-bit)
FSET pin shorted to GND	1250	Same as PWM input

PHASE SHIFT PWM SCHEME

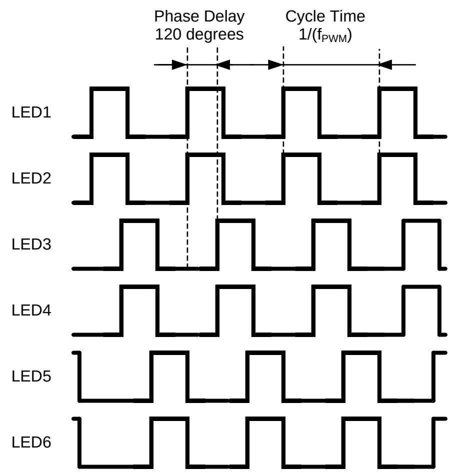
Phase shift PWM scheme allows delaying the time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the boost output is greatly decreased. This reduces the ripple seen on the boost output and allows smaller output capacitors. Reduced ripple also reduces the output ceramic capacitor audible ringing. PSPWM scheme also increases the load frequency seen on the boost output six times and therefore transfers the possible audible noise to the frequencies outside of the audible range.

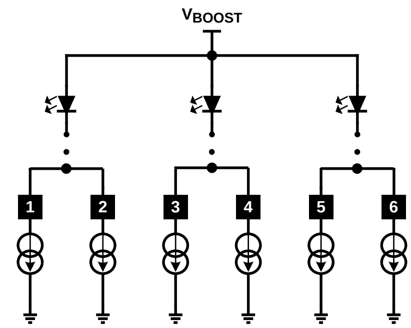
Description of the PSPWM mode is seen in the following diagrams. PSPWM mode is set with <PS_MODE[2:0]> bits.

<table>
<tr><th>PS_MODE[2:0]</th><th>Waveforms</th><th>Connection</th></tr>
<tr><td rowspan="2">000</td><td>
</td><td>
</td></tr>
<tr><td colspan="2">6 LED strings with 60 degree phase shift. One driver for each LED string.</td></tr>
<tr><td rowspan="2">001</td><td>
</td><td>
</td></tr>
<tr><td colspan="2">5 LED strings with 72 degree phase shift. One driver for each LED string.
(Driver #6 not used).</td></tr>
</table>

<table>
<tr><td rowspan="2">010</td><td>
</td><td>
</td></tr>
<tr><td colspan="2">4 LED strings with 90 degree phase shift. One driver for each LED string.
(Drivers #5 and #6 not used).</td></tr>
<tr><td rowspan="2">011</td><td>
</td><td>
</td></tr>
<tr><td colspan="2">3 LED strings with 120 degree phase shift. One driver for each LED string.
(Drivers #4, #5 and #6 not used).</td></tr>
<tr><td rowspan="2">100</td><td>
</td><td>
</td></tr>
<tr><td colspan="2">2 LED strings with 180 degree phase shift. One driver for each LED string.
(Drivers #3, #4, #5 and #6 not used).</td></tr>
</table>

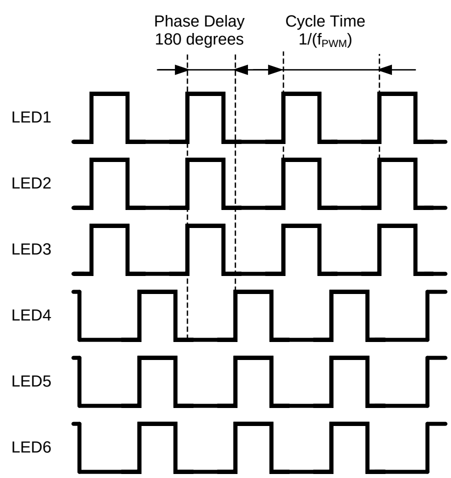
101

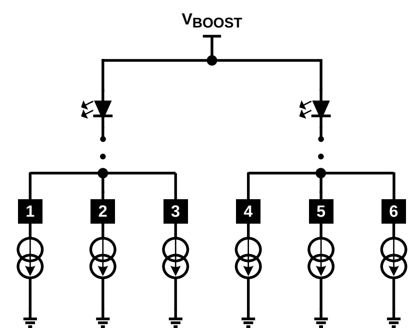




3 LED strings with 120 degree phase shift. Two drivers for each LED string.
(Drivers 1&2, 3&4 and 5&6 are tied and with the same phase).

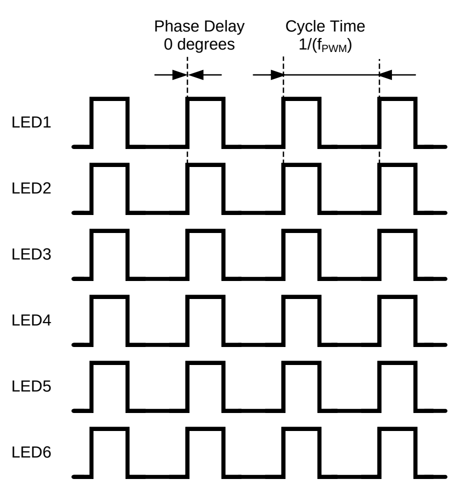
110

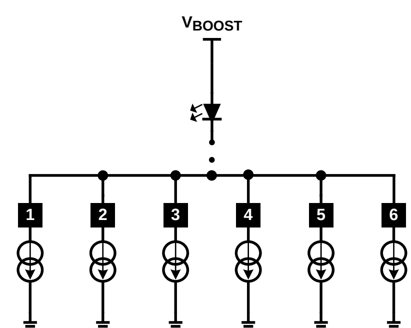




2 LED strings with 180 degree phase shift. Three divers for each LED string.
(Drivers 1&2&3 and 4&5&6 are tied and with the same phase).

111





1 LED string driven by all six drivers.
(All drivers are tied and with the same phase).

SLOPE AND ADVANCED SLOPE

Transition time between two brightness values can be programmed with EPROM bits <PWM_SLOPE[2:0]> from 0 to 500 ms. Same slope time is used for sloping up and down. With advanced slope the brightness changes can be made more pleasing to a human eye.

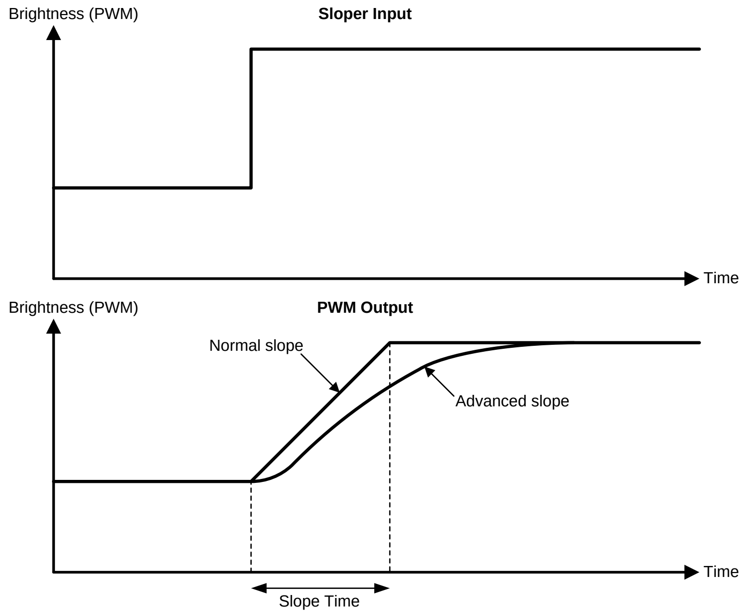


Figure 24. Sloper Operation

DITHERING

Special dithering scheme can be used during brightness changes and in steady state condition. It allows increased resolution and smaller average steps size during brightness changes. Dithering can be programmed with EPROM bits <DITHER[1:0]> from 0 to 3 bits. <STEADY_DITHER> EPROM bit sets whether the dithering is used also in steady state or only during slopes. Example below is for 1-bit dithering. E.g. for 3-bit dithering, every 8th pulse is made 1 LSB longer to increase the average value by 1/8th.

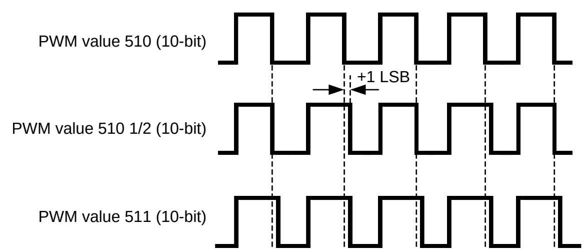


Figure 25. Example of the Dithering, 1-bit dither, 10-bit resolution

Fault Detection

LP8556 has fault detection for LED open and short conditions, UVLO, over-current and thermal shutdown. The cause for the fault can be read from status register. Reading the fault register will also reset the fault.

LED FAULT DETECTION

With LED fault detection, the voltages across the LED drivers are constantly monitored. Shorted or open LED strings are detected.

OPEN DETECT: The logic uses the LOW comparators and the requested boost voltage to detect the OPEN condition. If the logic is asking the boost for the maximum allowed voltage and a LOW comparator is asserted, then the OPEN bit is set in the STATUS register (ADDR=02h). In normal operation, the adaptive headroom control loop raises the requested boost voltage when the LOW comparator is asserted. If it has raised it as high as it can and an LED string still needs more voltage, then it is assumed to be disconnected from the boost voltage (open or grounded). The actual boost voltage is not part of the OPEN condition decision; only the requested boost voltage and the LOW comparators.

SHORT DETECT: The logic uses all three comparators (HIGH, MID and LOW) to detect the SHORT condition. When the MID and LOW comparators are de-asserted, the headroom control loop considers that string to be optimized - enough headroom, but not excessive. If at least one LED string is optimized and at least one other LED string has its HIGH comparator asserted, then the SHORT condition is detected. It is important to note that the SHORT condition requires at least two strings for detection: one in the optimized headroom zone (LOW/MID/HIGH comparators all de-asserted) and one in the excessive headroom zone (HIGH comparator asserted).

Fault is cleared by reading the fault register.

UNDER-VOLTAGE DETECTION

LP8556 has detection for too-low VIN voltage. Threshold level for the voltage is set with EPROM register bits as shown in the following table:

Table 6. UVLO Truth Table

UVLO_EN	UVLO_TH	Threshold (V)
0	don't care	OFF
1	0	2.5V
1	1	5.2V

When under voltage is detected the LED outputs and the boost will shutdown and the corresponding fault bit is set in the fault register. The LEDs and the boost will start again when the voltage has increased above the threshold level. Hysteresis is implemented to threshold level to avoid continuous triggering of fault when threshold is reached.

Fault is cleared by setting the EN / VDDIO pin low or by reading the fault register.

OVER-CURRENT PROTECTION

LP8556 has detection for too-high loading on the boost converter. When over-current fault is detected, the the boost will shutdown and the corresponding fault bit is set in the fault register. The boost will start again when the current has dropped below the OCP threshold.

Fault is cleared by reading the fault register.

THERMAL SHUTDOWN

If the LP8556 reaches thermal shutdown temperature (150 °C) the LED outputs and boost will shut down to protect it from damage. Device will re-activate again when temperature drops below 130 °C degrees.

Fault is cleared by reading the fault register.

I²C Compatible Serial Bus Interface

INTERFACE BUS OVERVIEW

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). These lines should be connected to a positive supply via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave depending on whether it generates or receives the SCL. The LP8556 can operate as an I²C slave.

DATA TRANSACTIONS

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock SCL. Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

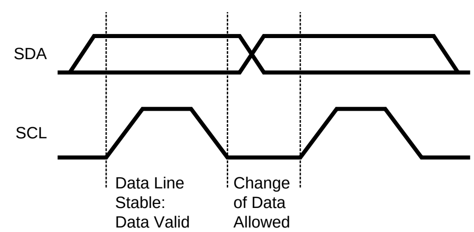


Figure 26. Bit Transfer

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

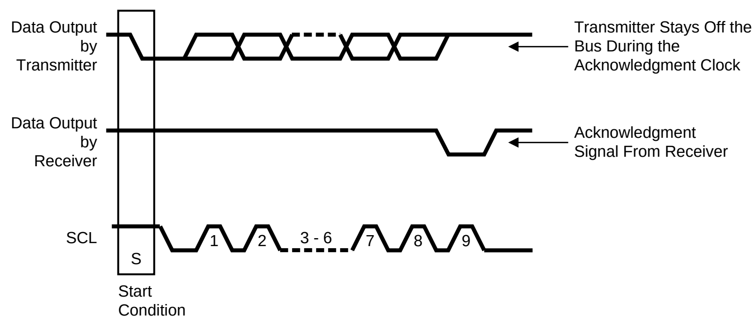


Figure 27. Start and Stop

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

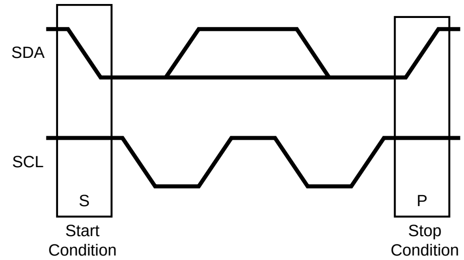


Figure 28. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

ACKNOWLEDGE CYCLE

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

“ACKNOWLEDGE AFTER EVERY BYTE” RULE

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

ADDRESSING TRANSFER FORMATS

Each device on the bus has a unique slave address. The LP8556 operates as a slave device with 7-bit address combined with data direction bit. Slave address is 2Ch as 7-bit or 58h for write and 59h for read in 8-bit format.

Before any data is transmitted, the master transmits the the slave I.D. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

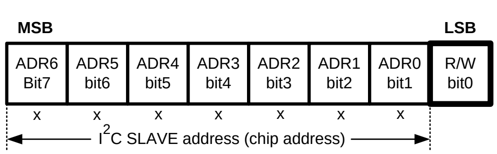


Figure 29. I²C Chip Address (0x2C)

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes the control register address will be incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 7. Data Read and Write Cycles

	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr.>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> … additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w='0'>[Ack] <Register Addr.>[Ack] <Register Data>[Ack] … additional writes to subsequent register address possible <Stop Condition>

<>Data from master [ ] Data from slave

Register Read and Write Detail

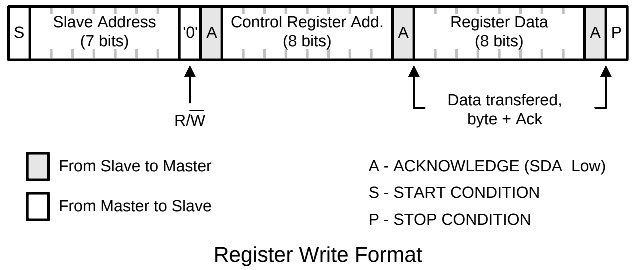


Figure 30. Register Write Format

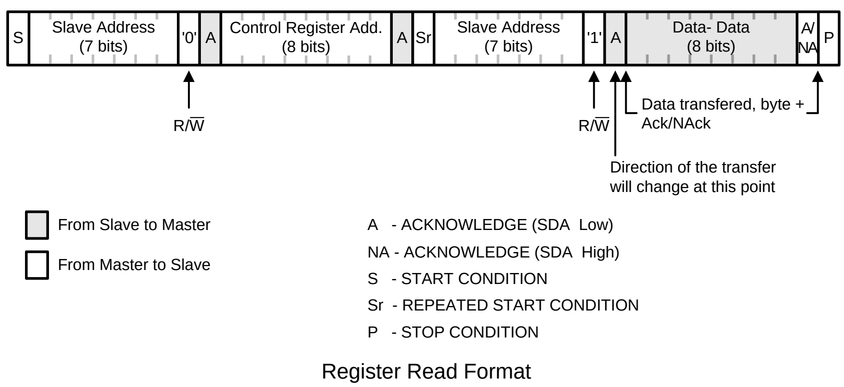


Figure 31. Register Read Format

Table 8. Register Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	RESET
00H	Brightness Control	BRT[7:0]								0000 0000
01H	Device Control	FAST					BRT_MODE		BL_CTL	0000 0000
02H	Status	OPEN	SHORT	VREF_OK	VBOOST_OK	OVP	OCP	TSD	UVLO	0000 0000
03H	ID	PANEL	MFG				REV			1111 1100
04H	Direct Control			LED						0000 0000
16H	LED Enable			LED_EN						0011 1111

Table 9. EPROM Memory Map

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
98H	CFG98	IBOOST_LIM_2X	RESERVED			RESERVED			
9EH	CFG9E	RESERVED		VBOOST_RANGE	RESERVED	HEADROOM_OFFSET			
A0H	CFG0	CURRENT LSB							
A1H	CFG1	PDET_STDBY	CURRENT_MAX			CURRENT MSB			
A2H	CFG2	RESERVED		UVLO_EN	UVLO_TH	BL_ON	ISET_EN	BOOST_FSET_EN	PWM_FSET_EN

Table 9. EPROM Memory Map (continued)

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
A3H	CFG3	RESERVED	SLOPE			FILTER		PWM_INPUT_HYSTERESIS	
A4H	CFG4	PWM_TO_I_THRESHOLD				RESERVED	STEADY_DITHER	DITHER	
A5H	CFG5	PWM_DIRECT	PS_MODE			PWM_FREQ			
A6H	CFG6	BOOST_FREQ		VBOOST					
A7H	CFG7	RESERVED		EN_DRV3	EN_DRV2	RESERVED		IBOOST_LIM	
A8H	CFG8	RESERVED		RESERVED		RESERVED		RESERVED	
A9H	CFG9	VBOOST_MAX			JUMP_EN	JUMP_THRESHOLD		JUMP_VOLTAGE	
AAH	CFGA	SSCLK_EN	RESERVED	RESERVED		ADAPTIVE	DRIVER_HEADROOM		
ABH	CFGB	RESERVED							
ACH	CFGC	RESERVED				RESERVED			
ADH	CFGD	RESERVED							
AEH	CFGE	STEP_UP		STEP_DN		LED_FAULT_TH		LED_COMP_HYST	
AFH	CFGF	REVISION							

Register Bit Explanations

BRIGHTNESS CONTROL

Address 00h

Reset value 0000 0000b

Brightness Control register							
7	6	5	4	3	2	1	0
BRT[7:0]							

Name	Bit	Access	Description
BRT	7:0	R/W	Backlight PWM 8-bit linear control.

DEVICE CONTROL

Address 01h

Reset value 0000 0000b

Device Control register							
7	6	5	4	3	2	1	0
FAST					BRT_MODE[1:0]		BL_CTL

Name	Bit	Access	Description
FAST	7		Skip refresh of trim and configuration registers from EPROMs when exiting the low power STANDBY mode. 0 = read EPROMs before returning to the ACTIVE state 1 = only read EPROMs once on initial power-up.
BRT_MODE	2:1	R/W	Brightness source mode Figure 20
			00b = PWM input only
			01b = PWM input and Brightness register (combined before shaper block)
			10b = Brightness register only
			11b = PWM input and Brightness register (combined after shaper block)

Device Control register			
BL_CTL	0	R/W	Enable backlight when Brightness Register is used to control brightness (BRT_MODE = 10).
			0 = Backlight disabled and chip turned off 1 = Backlight enabled and chip turned on
			This bit has no effect when PWM pin control is selected for brightness control (BRT_MODE = 00). In this mode the state of PWM pin enable or disables the chip.

STATUS

Address 02h

Reset value 0000 0000b

Fault register							
7	6	5	4	3	2	1	0
OPEN	SHORT	VREF_OK	VBOOST_OK	OVP	OCP	TSD	UVLO

Name	Bit	Access	Description
OPEN	7	R	LED open fault detection
			0 = No fault
			1 = LED open fault detected. The value is not latched.
SHORT	6	R	LED short fault detection
			0 = No fault
			1 = LED short fault detected. The value is not latched.
VREF_OK	5	R	Internal VREF node monitor status
			1 = VREF voltage is OK.
VBOOST_OK	4	R	Boost output voltage monitor status
			0 = Boost output voltage has not reached its target (VBOOST < Vtarget - 2.5V)
			1 = Boost output voltage is OK. The value is not latched.
OVP	3	R	Overvoltage protection
			0 = No fault
			1 = Overvoltage condition occurred. Fault is cleared by reading the register 02h.
OCP	2	R	Over current protection
			0 = No fault
			1 = Over current detected in boost output. OCP detection block monitors the boost output and if the boost output has been too low for more than 50 ms it will generate OCP fault and disable the boost. Fault is cleared by reading the register 02h. After clearing the fault boost will startup again.
TSD	1	R	Thermal shutdown
			0 = No fault
			1 = Thermal fault generated, 150 °C reached. Boost converter and LED outputs will be disabled until the temperature has dropped down to 130 °C. Fault is cleared by reading this register.
UVLO	0	R	Under voltage detection
			0 = No fault
			1 = Under voltage detected on the V_{DD} pin. Boost converter and LED outputs will be disabled until V_{DD} voltage is above the UVLO threshold voltage. Threshold voltage is set with EPROM bits. Fault is cleared by reading this register.

IDENTIFICATION

Address 03h

Reset value 1111 1100b

Identification register							
7	6	5	4	3	2	1	0
PANEL	MFG[3:0]				REV[2:0]		

Name	Bit	Access	Description
PANEL	7	R	Panel ID code
MFG	6:3	R	Manufacturer ID code
REV	2:0	R	Revision ID code

DIRECT CONTROL

Address 04h

Reset value 0000 0000b

Direct Control register							
7	6	5	4	3	2	1	0
		OUT[5:0]					

Name	Bit	Access	Description
OUT	5:0	R/W	Direct control of the LED outputs
			0 = Normal operation. LED output are controlled with the adaptive dimming block
			1 = LED output is forced to 100% PWM.

LED String Enable

Address 16h

Reset value 0011 1111b

Temp LSB register							
7	6	5	4	3	2	1	0
		LED_EN[5:0]					

Name	Bit	Access	Description
LED_EN	5:0	R/W	Bits 5:0 correspond to LED Strings 6:1 respectively. Bit value 1 = LED String Enabled Bit value 0 = LED String Disabled Note: To disable string(s), it is recommended to disable higher order string(s). For example, - for 5 String configuration, disable 6th String. - for 4 string configuration, disable 6th and 5th string. These bits are ANDed with the internal LED enable bits that are generated with the PS_MODE logic.

EPROM Bit Explanations

LP8556TM (DSBGA) Configurations and Pre-configured EPROM Settings

ADDRESS	LP8556-E00	LP8556-E01	LP8556-E02	LP8556-E03	LP8556-E04	LP8556-E05 (1)
98h[7]	0b	0b	0b	0b	0b	0b
9Eh	22h	22h	22h	24h	24h	22h
A0h	FFh	FFh	FFh	FFh	FFh	
A1h	CFh	4Fh	5Fh	BFh	3Fh	
A2h	2Fh	20h	20h	28h	2Fh	
A3h	5Eh	03h	5Eh	5Eh	5Eh	
A4h	72h	12h	72h	72h	72h	
A5h	14h	0Ch	04h	14h	04h	
A6h	80h	80h	80h	80h	80h	
A7h	FFh	FFh	FFh	FFh	FFh	
A8h	00h	00h	00h	00h	00h	
A9h	A0h	80h	80h	A0h	60h	
AAh	0Fh	0Fh	0Fh	0Fh	0Fh	
ABh	00h	00h	00h	00h	00h	
ACh	00h	00h	00h	00h	00h	
ADh	00h	00h	00h	00h	00h	
AEh	0Fh	0Fh	0Fh	0Fh	0Fh	
AFh	02h	02h	04h	02h	02h	

(1) LP8556-E05 is a device option with un-configured EPROM settings. This option is for users that desire programming the device by themselves. Bits 98h[7] and 9Eh[5] are always pre-configured.

LP8556TM (DSBGA) Configurations and Pre-configured EPROM Settings Continued

ADDRESS	LP8556-E06	LP8556-E07	LP8556-E08	LP8556-E09	LP8556-E10	LP8556-E11
98h[7]	0b	0b	0b	0b	0b	
9Eh	22h	04h	22h	22h	24h	
A0h	FFh	FFh	FFh	FFh	EBh	
A1h	DBh	BFh	CFh	CFh	3Dh	
A2h	2Fh	0Dh	2Fh	2Fh	2Fh	
A3h	02h	02h	5Eh	02h	37h	
A4h	72h	72h	72h	72h	77h	
A5h	14h	20h	24h	04h	1Bh	
A6h	40h	4Eh	80h	80h	40h	
A7h	FFh	FEh	FFh	FFh	FEh	
A8h	21h	21h	00h	00h	21h	
A9h	DBh	C0h	A0h	A0h	9Bh	
AAh	0Fh	0Fh	0Fh	0Fh	3Fh	
ABh	00h	00h	00h	00h	00h	
ACh	00h	00h	00h	00h	00h	
ADh	00h	00h	00h	00h	00h	
AEh	0Fh	0Fh	0Fh	0Fh	0Fh	
AFh	02h	02h	02h	03h	00h	

LP8556SQ (WQFN) Configurations and Pre-configured EPROM Settings

ADDRESS	LP8556-E00	LP8556-E08	LP8556-E09
98h[7]	1b	1b	1b
9Eh	22h	22h	22h
A0h	FFh	FFh	FFh
A1h	CFh	CFh	CFh
A2h	2Fh	2Fh	2Fh
A3h	5Eh	5Eh	02h
A4h	72h	72h	72h
A5h	14h	24h	04h
A6h	80h	80h	80h
A7h	FEh	FEh	FEh
A8h	00h	00h	00h
A9h	A0h	A0h	A0h
AAh	0Fh	0Fh	0Fh
ABh	00h	00h	00h
ACh	00h	00h	00h
ADh	00h	00h	00h
AEh	0Fh	0Fh	0Fh
AFh	00h	00h	00h

CFG98

Address 98h

CFG98 register							
7	6	5	4	3	2	1	0
IBOOST_LIM_2X							

Name	Bit	Access	Description
IBOOST_LIM_2X	7	R/W	Select the inductor current limit range. When IBOOST_LIM_2X = 0, the inductor current limit can be set to 0.9A, 1.2A, 1.5A or 1.8A. When IBOOST_LIM_2X = 1, the inductor current limit can be set to 1.6A, 2.1A, or 2.6A . This option is supported only on WQFN package and not on DSBGA package. See (1).

(1) 1.8A is the maximum I_{SW_LIM} supported with the DSBGA package. For applications requiring the I_{SW_LIM} to be greater than 1.8A and up to 2.6A, WQFN package should be considered.

CFG9E

Address 9Eh

CFG9E register							
7	6	5	4	3	2	1	0
		VBOOST_RANGE		HEADROOM_OFFSET			

Name	Bit	Access	Description
VBOOST_RANGE	5	R/W	Select VBOOST range. When VBOOST_RANGE = 0, the output voltage range is from 7V to 34V When VBOOST_RANGE = 1, the output voltage range is from 16V to 43V
HEADROOM_OFFSET	3:0	R/W	LED driver headroom offset. This adjusts the LOW comparator threshold together with LED_HEADROOM bits and contributes to the MID comparator threshold. 0000 = 460 mV 0001 = 390 mV 0010 = 320 mV 0100 = 250 mV 1000 = 180 mV

CFG0

Address A0h

CFG0 register							
7	6	5	4	3	2	1	0
CURRENT LSB[7:0]							

Name	Bit	Access	Description		
CURRENT LSB	7:0	R/W	The 8-bits in this register (LSB) along the 4-bits defined in CFG1 Register (MSB) allow LED current to be set in 12-bit fine steps. These 12-bits further scale the maximum LED current set using CFG1 Register, CURRENT_MAX bits (denoted as IMAX). If ISET_EN = 0, the LED current is defined with the bits as shown below. If ISET_EN = 1, then the external resistor connected to the ISET pin scales the LED current as shown below.		
				ISET_EN = 0	ISET_EN = 1
			0000 0000 0000	0A	0A
			0000 0000 0001	(1/4095) x I_{MAX}	(1/4095) x I_{MAX} x 20000 x 1.2V / R_{ISET}
			0000 0000 0010	(2/4095) x I_{MAX}	(2/4095) x I_{MAX} x 20000 x 1.2V / R_{ISET}
			...	...	...
			0111 1111 1111	(2047/4095) x I_{MAX}	(2047/4095) x I_{MAX} x 20000 x 1.2V / R_{ISET}
			...	...	...
			1111 1111 1101	(4093/4095) x I_{MAX}	(4093/4095) x I_{MAX} x 20000 x 1.2V / R_{ISET}
			1111 1111 1110	(4094/4095) x I_{MAX}	(4094/4095) x I_{MAX} x 20000 x 1.2V / R_{ISET}
			1111 1111 1111	(4095/4095) x I_{MAX}	(4095/4095) x I_{MAX} x 20000 x 1.2V / R_{ISET}

CFG1

Address A1h

CFG1 register							
7	6	5	4	3	2	1	0
PDET_STDBY	CURRENT_MAX[2:0]			CURRENT MSB[11:8]			

Name	Bit	Access	Description
PDET_STDBY	7	R/W	Enable Standby when PWM input is constant low (approx. 50 ms timeout).
CURRENT_MAX	6:4	R/W	Set Maximum LED current as shown below. This maximum current is scaled as described in the CFG0 Register. 000 = 5 mA 001 = 10 mA 010 = 15 mA 011 = 20 mA 100 = 23 mA 101 = 25 mA 110 = 30 mA 111 = 50 mA
CURRENT MSB	3:0	R/W	These bits form the 4 MSB bits for LED Current as described in CFG0 Register

CFG2

Address A2h

CFG2 register							
7	6	5	4	3	2	1	0
RESERVED		UVLO_EN	UVLO_TH	BL_ON	ISET_EN	BOOST_ _FSET_EN	PWM_ _FSET_EN

Name	Bit	Access	Description
RESERVED	7:6	R/W	
UVLO_EN	5	R/W	Undervoltage lockout protection enable.
UVLO_TH	4	R/W	UVLO threshold levels: 0 = 2.5V 1 = 5.2V
BL_ON	3	R/W	Enable backlight. This bit must be set for PWM only control. 0 = Backlight disabled. This selection is recommended for systems with an I2C master. With an I2C master, the backlight can be controlled by writing to the register 01h. 1 = Backlight enabled. This selection is recommended for systems with PWM only control.
ISET_EN	2	R/W	Enable LED current set resistor. 0 = Resistor is disabled and current is set with CURRENT and CURRENT_MAX EPROM register bits. 1 = Resistor is enabled and current is set with the R_{ISET} resistor AND CURRENT AND CURRENT_MAX EPROM register bits.
BOOST_FSET_EN	1	R/W	Enable configuration of the switching frequency via FSET pin. 0 = Configuration of the switching frequency via FSET pin is is disabled. The switching frequency is set with BOOST_FREQ EPROM register bits. 1 = Configuration of the switching frequency via FSET pin is is enabled.
PWM_FSET_EN	0	R/W	Enable configuration of the PWM dimming frequency via FSET pin. 0 = Configuration of the switching frequency via FSET pin is is disabled. The switching frequency is set with PWM_FREQ EPROM register bits. 1 = Configuration of the PWM dimming frequency via FSET pin is is enabled.

CFG3

Address A3h

CFG3 register							
7	6	5	4	3	2	1	0
RESERVED	SLOPE[2:0]			FILTER[1:0]		PWM_INPUT_HYSTERESIS[1:0]	

Name	Bit	Access	Description
RESERVED	7	R/W	
SLOPE	6:4	R/W	Select brightness change transition duration 000 = 0 ms (immediate change) 001 = 1 ms 010 = 2 ms 011 = 50 ms 100 = 100 ms 101 = 200 ms 110 = 300 ms 111 = 500 ms
FILTER	3:2	R/W	Select brightness change transition filtering strength 00 = No filtering. 01 = light smoothing 10 = medium smoothing 11 = heavy smoothing
PWM_INPUT_ _HYSTERESIS	1:0	R/W	PWM input hysteresis function. 00 = OFF 01 = 1-bit hysteresis with 13-bit resolution 10 = 1-bit hysteresis with 12-bit resolution 11 = 1-bit hysteresis with 8-bit resolution

CFG4

Address A4h

CFG4 register							
7	6	5	4	3	2	1	0
PWM_TO_I_THRESHOLD[3:0]				RESERVED	STEADY_ _DITHER	DITHER[1:0]	

Name	Bit	Access	Description
PWM_TO_I_ _THRESHOLD	7:4	R/W	Select switch point between PWM and pure current dimming 0000 = current dimming across entire range 0001 = switch point at **10%** of the maximum LED current. 0010 = switch point at **12.5%** of the maximum LED current. 0011 = switch point at **15%** of the maximum LED current. 0100 = switch point at **17.5%** of the maximum LED current. 0101 = switch point at **20%** of the maximum LED current. 0110 = switch point at **22.5%** of the maximum LED current. 0111 = switch point at **25%** of the maximum LED current. This is a recommended selection. 1000 = switch point at **33.33%** of the maximum LED current. 1001 = switch point at **41.67%** of the maximum LED current. 1010 = switch point at **50%** of the maximum LED current. 1011 to 1111 = PWM dimming across entire range
RESERVED	3	R/W	
STEADY_DITHER	2	R/W	Dither function method select: 0 = Dither only on transitions 1 = Dither at all times
DITHER	1:0	R/W	Dither function control 00 = Dithering disabled 01 = 1-bit dithering 10 = 2-bit dithering 11 = 3-bit dithering

CFG5

Address A5h

CFG5 register							
7	6	5	4	3	2	1	0
PWM_DIRECT	PS_MODE[2:0]			PWM_FREQ[3:0]			

Name	Bit	Access	Description
PWM_DIRECT	7	R/W	Intended for certain test mode purposes. When enabled, the entire pipeline is bypassed and PWM output is connected with PWM input.
PS_MODE	6:4	R/W	Select PWM output phase configuration: 000 = 6-phase, 6 drivers (0°, 60°, 120°, 180°, 240°, 320°) 001 = 5-phase, 5 drivers (0°, 72°, 144°, 216°, 288°, OFF) 010 = 4-phase, 4 drivers (0°, 90°, 180°, 270°, OFF, OFF) 011 = 3-phase, 3 drivers (0°, 120°, 240°, OFF, OFF, OFF) 100 = 2-phase, 2 drivers (0°, 180°, OFF, OFF, OFF, OFF) 101 = 3-phase, 6 drivers (0°, 0°, 120°, 120°, 240°, 240°) 110 = 2-phase, 6 drivers (0°, 0°, 0°, 180°, 180°, 180°) 111 = 1-phase, 6 drivers (0°, 0°, 0°, 0°, 0°, 0°)

CFG5 register			
PWM_FREQ	3:0	R/W	0h = 4,808Hz (11-bit) 1h = 6,010Hz (10-bit) 2h = 7,212Hz (10-bit) 3h = 8,414Hz (10-bit) 4h = 9,616Hz (10-bit) 5h = 12,020Hz (9-bit) 6h = 13,222Hz (9-bit) 7h = 14,424Hz (9-bit) 8h = 15,626Hz (9-bit) 9h = 16,828Hz (9-bit) Ah = 18,030Hz (9-bit) Bh = 19,232Hz (9-bit) Ch = 24,040Hz (8-bit) Dh = 28,848Hz (8-bit) Eh = 33,656Hz (8-bit) Fh = 38,464Hz(8-bit)

CFG6

Address A6h

CFG6 register							
7	6	5	4	3	2	1	0
BOOST_FREQ[1:0]		VBOOST[5:0]					

Name	Bit	Access	Description
BOOST_FREQ	7:6	R/W	Set boost switching frequency when BOOST_FSET_EN = 0. 00 = 312 kHz 01 = 625 kHz 10 = 1250 kHz 11 = undefined
VBOOST	5:0	R/W	Boost output voltage. When ADAPTIVE = 1, this is the boost minimum and initial voltage.

CFG7

Address A7h

CFG7 register							
7	6	5	4	3	2	1	0
RESERVED		EN_DRV3	EN_DRV2	RESERVED		IBOOST_LIM[1:0]	

Name	Bit	Access	Description
RESERVED	7:6		
EN_DRV3	5	R/W	Selects boost driver strength to set boost slew rate. See EMI REDUCTION section for more detail. 0 = Driver3 disabled 1 = Driver3 enabled
EN_DRV2	4	R/W	Selects boost driver strength to set boost slew rate. See EMI REDUCTION section for more detail. 0 = Driver2 disabled 1 = Driver2 enabled
RESERVED	3:2	R/W	
IBOOST_LIM	1:0	R/W	Select boost inductor current limit (IBOOST_LIM_2X = 0 / IBOOST_LIM_2X = 1) 00 = 0.9A / 1.6A 01 = 1.2A / 2.1A 10 = 1.5A / 2.6A 11 = 1.8A / not permitted

CFG9

Address A9h

CFG9 register							
7	6	5	4	3	2	1	0
VBOOST_MAX[2:0]			JUMP_EN	JUMP_THRESHOLD[1:0]		JUMP_VOLTAGE[1:0]	

Name	Bit	Access	Description
VBOOST_MAX	7:5	R/W	Select the maximum boost voltage (typ values) (VBOOST_RANGE = 0 / VBOOST_RANGE = 1) 010 = NA / 21V 011 = NA / 25V 100 = 21V / 30V 101 = 25V / 34.5V 110 = 30V / 39V 111 = 34V / 43V
JUMP_EN	4	R/W	Enable JUMP detection on the PWM input.
JUMP_THRESHOLD	3:2	R/W	Select JUMP threshold: 00 = 10% 01 = 30% 10 = 50% 11 = 70%
JUMP_VOLTAGE	1:0	R/W	Select JUMP voltage: 00 = 0.5V 01 = 1V 10 = 2V 11 = 4V

CFGA

Address AAh

CFGA register							
7	6	5	4	3	2	1	0
SSCLK_EN	RESERVED	RESERVED		ADAPTIVE	DRIVER_HEADROOM[2:0]		

Name	Bit	Access	Description
SSCLK_EN	7	R/W	Enable spread spectrum function.
RESERVED	6	R/W	
RESERVED	5:4	R/W	
ADAPTIVE	3	R/W	Enable adaptive boost control.
DRIVER_HEADROOM	2:0	R/W	LED driver headroom control. This sets the LOW comparator threshold and contributes to the MID comparator threshold. 000 = HEADROOM_OFFSET + 875 mV 001 = HEADROOM_OFFSET + 750 mV 010 = HEADROOM_OFFSET + 625 mV 011 = HEADROOM_OFFSET + 500 mV 100 = HEADROOM_OFFSET + 375 mV 101 = HEADROOM_OFFSET + 250 mV 110 = HEADROOM_OFFSET + 125 mV 111 = HEADROOM_OFFSET mV

CFGE

Address AEh

CFGE register							
7	6	5	4	3	2	1	0
STEP_UP[1:0]		STEP_DN[1:0]		LED_FAULT_TH[2:0]		LED_COMP_HYST[1:0]	

Name	Bit	Access	Description
STEP_UP	7:6	R/W	Adaptive headroom UP step size 00 = 105 mV 01 = 210 mV 10 = 420 mV 11 = 840 mV
STEP_DN	5:4	R/W	Adaptive headroom DOWN step size 00 = 105 mV 01 = 210 mV 10 = 420 mV 11 = 840 mV
LED_FAULT_TH	3:2	R/W	LED headroom fault threshold. This sets the HIGH comparator threshold. 00 = 5V 01 = 4V 10 = 3V 11 = 2V
LED_COMP_HYST	1:0	R/W	LED headrom comparison hysteresis. This sets the MID comparator threshold. 00 = DRIVER_HEADROOM + 1000 mV 01 = DRIVER_HEADROOM + 750 mV 10 = DRIVER_HEADROOM + 500 mV 11 = DRIVER_HEADROOM + 250 mV

CFGF

Address AFh

CFGF register							
7	6	5	4	3	2	1	0
REVISION							

Name	Bit	Access	Description
REV	7:0	R/W	EPROM Settings Revision ID code

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8556SQ-E00/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E0	Samples
LP8556SQ-E08/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E8	Samples
LP8556SQ-E09/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E9	Samples
LP8556SQE-E00/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E0	Samples
LP8556SQE-E08/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E8	Samples
LP8556SQE-E09/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E9	Samples
LP8556SQX-E00/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E0	Samples
LP8556SQX-E08/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E8	Samples
LP8556SQX-E09/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L8556E9	Samples
LP8556TME-E02/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E2	Samples
LP8556TME-E03/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E3	Samples
LP8556TME-E04/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E4	Samples
LP8556TME-E05/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E5	Samples
LP8556TME-E06/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E6	Samples
LP8556TME-E07/NOPB	PREVIEW	DSBGA	YFQ	20	250	TBD	Call TI	Call TI	-40 to 85		
LP8556TME-E09/NOPB	ACTIVE	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E9	Samples
LP8556TME-E12/NOPB	PREVIEW	DSBGA	YFQ	20	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6E12	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8556TMX-E02/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E2	Samples
LP8556TMX-E03/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E3	Samples
LP8556TMX-E04/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E4	Samples
LP8556TMX-E05/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E5	Samples
LP8556TMX-E06/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E6	Samples
LP8556TMX-E09/NOPB	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		56E9	Samples
LP8556TMX-E12/NOPB	PREVIEW	DSBGA	YFQ	20		Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	6E12	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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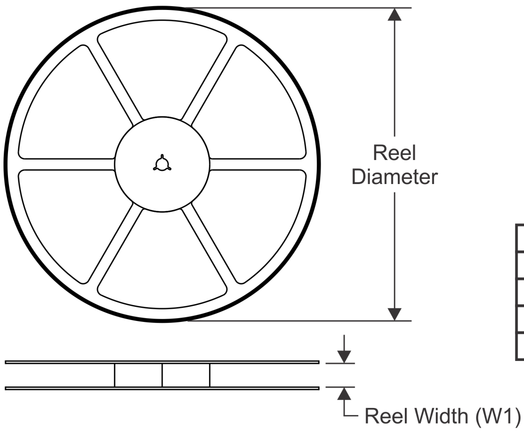
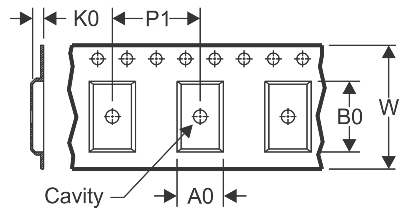
TAPE AND REEL INFORMATION

REEL DIMENSIONS

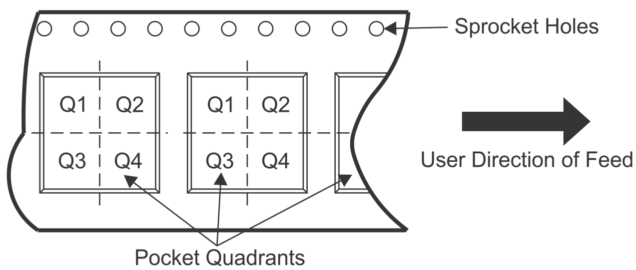


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

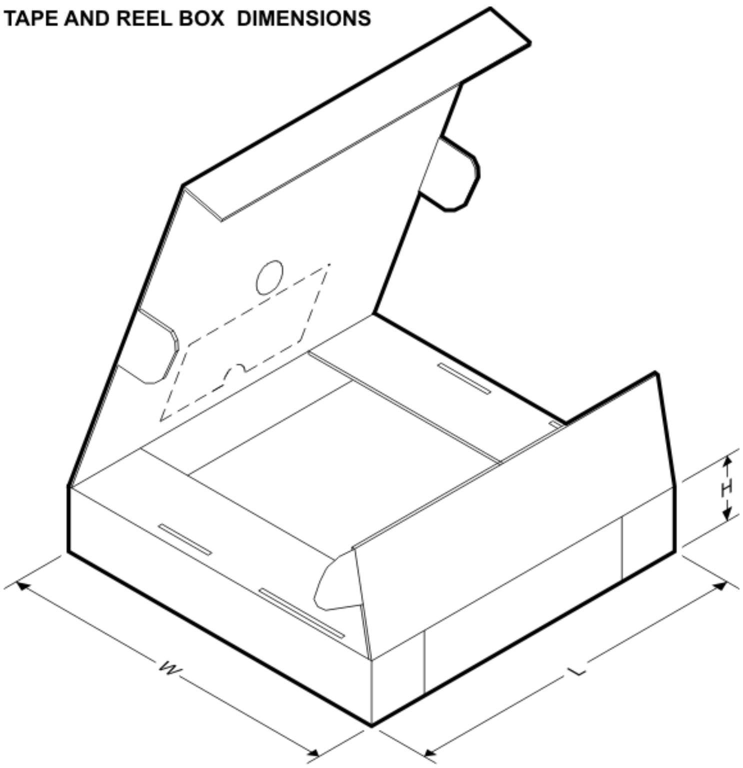


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8556SQ-E00/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQ-E08/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQ-E09/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQE-E00/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQE-E08/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQE-E09/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQX-E00/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQX-E08/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556SQX-E09/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP8556TME-E02/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TME-E03/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TME-E04/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TME-E05/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TME-E06/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TME-E09/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TMX-E02/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TMX-E03/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TMX-E04/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8556TMX-E05/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TMX-E06/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1
LP8556TMX-E09/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.83	2.49	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

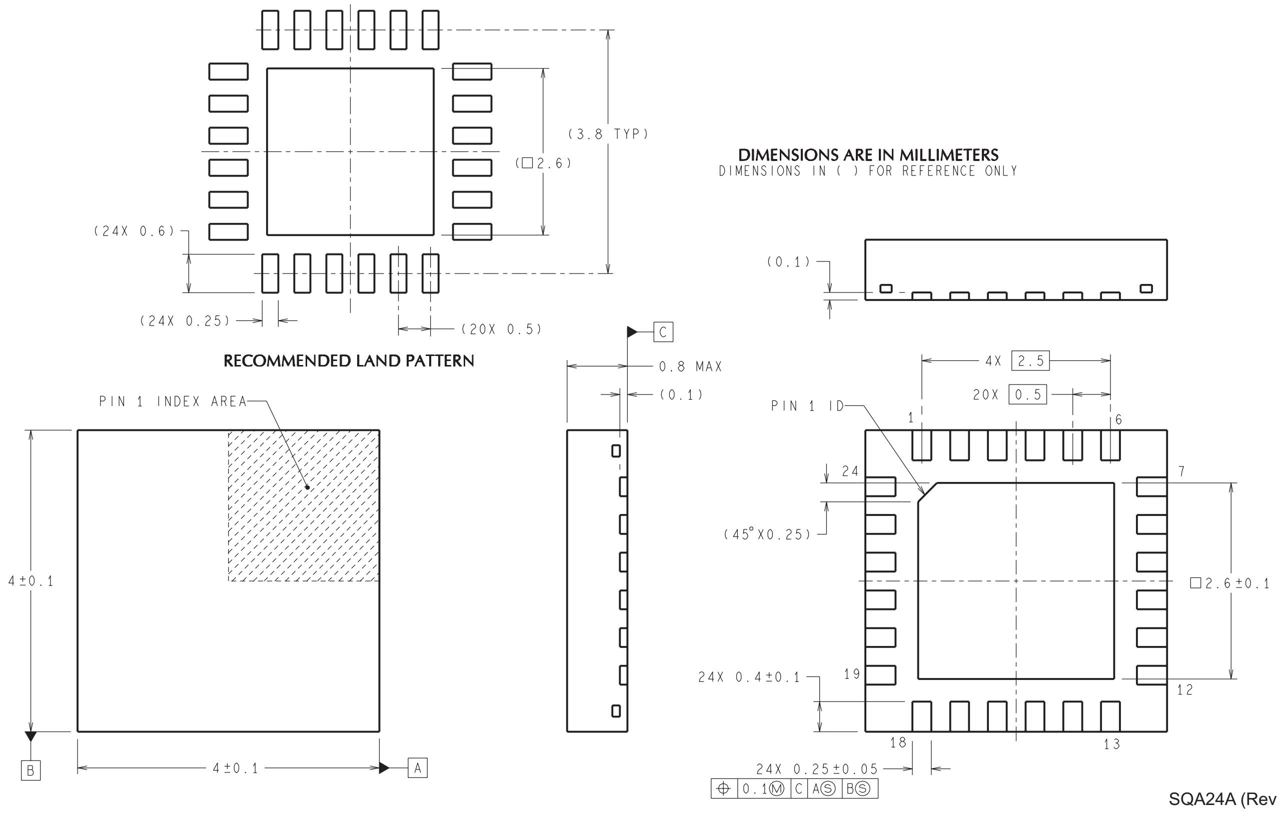


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8556SQ-E00/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LP8556SQ-E08/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LP8556SQ-E09/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LP8556SQE-E00/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LP8556SQE-E08/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LP8556SQE-E09/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LP8556SQX-E00/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0
LP8556SQX-E08/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0
LP8556SQX-E09/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0
LP8556TME-E02/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LP8556TME-E03/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LP8556TME-E04/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LP8556TME-E05/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LP8556TME-E06/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0

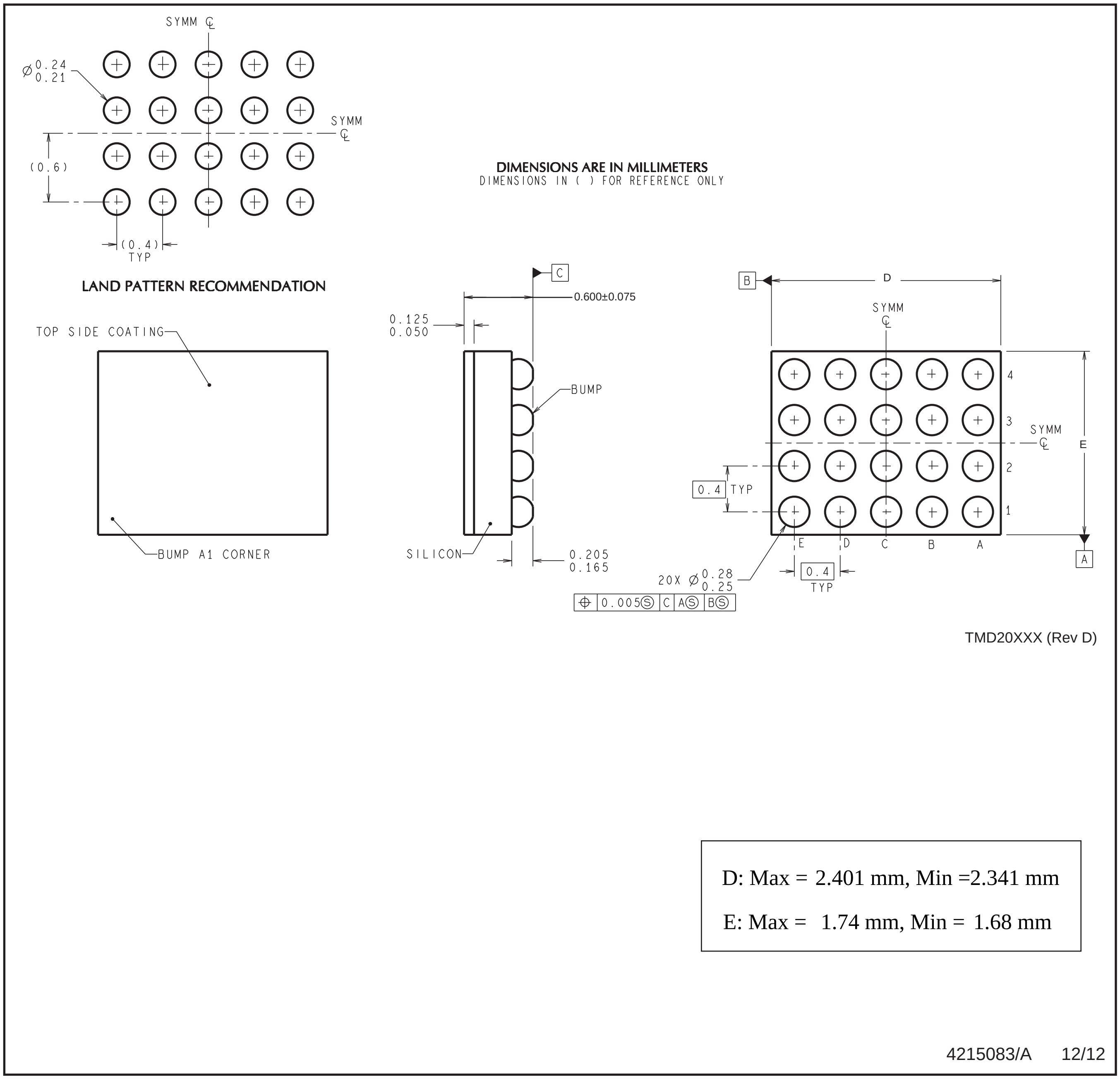
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8556TME-E09/NOPB	DSBGA	YFQ	20	250	210.0	185.0	35.0
LP8556TMX-E02/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0
LP8556TMX-E03/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0
LP8556TMX-E04/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0
LP8556TMX-E05/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0
LP8556TMX-E06/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0
LP8556TMX-E09/NOPB	DSBGA	YFQ	20	3000	210.0	185.0	35.0

RTW0024A



SQA24A (Rev B)

YFQ0020



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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