SM74611 Smart Bypass Diode

Check for Samples: SM74611

FEATURES

- **Maximum reverse voltage (V_R) of 30 V**
- **Maximum forward current (I_F) of 15A**
- **Low average forward voltage (26mV at 8A)**
- **Less power dissipation than Schottky diode**
- **Lower leakage current than Schottky diode**
- **Footprint and pin compatible with conventional D2PAK Schottky diode**
- **Operating range (Tj) of -40°C to 125°C**

APPLICATIONS

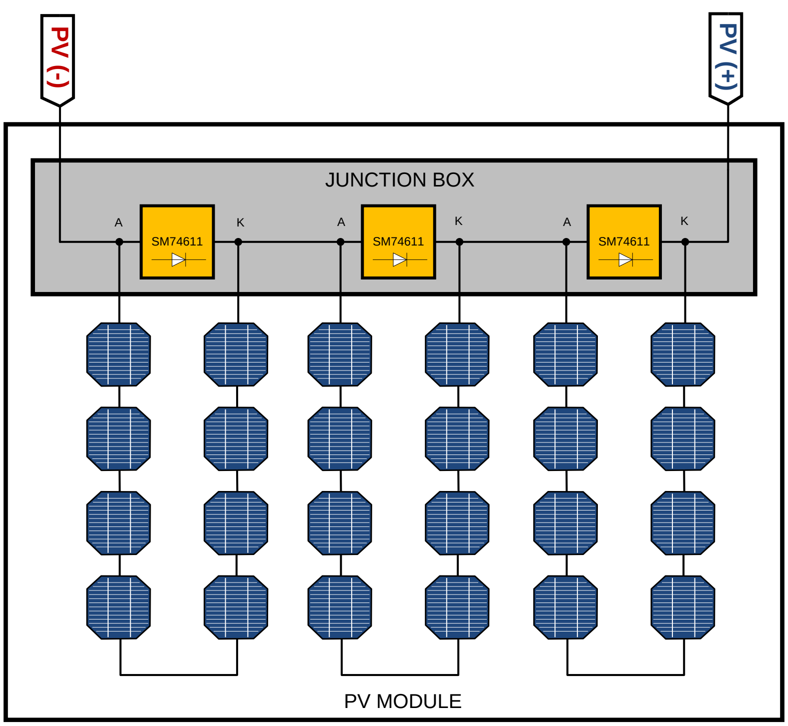
- **Bypass Diodes for Photovoltaic Panels**
- **Bypass Diodes for Microinverter and Power Optimizer**

DESCRIPTION

The SM74611 is a smart bypass diode used in photovoltaic applications. It serves the purpose of providing an alternate path for string current when parts of the panel are shaded during normal operation. Without bypass diodes, the shaded cells will exhibit a hot spot which is caused by excessive power dissipation in the reverse biased cells. Currently, conventional P-N junction diodes or Schottky diodes are used to mitigate this issue. Unfortunately the forward voltage drop for these diodes is still considered high (~0.6V for normal diodes and 0.4V for Schottky). With 10A of currents flowing through these diodes, the power dissipation can reach as high as 6W. This in turn will raise the temperature inside the junction box where these diodes normally reside and reduce module reliability.

The advantage of the SM74611 is that it has a lower forward voltage drop than P-N junction and Schottky diodes. It has a typical average forward voltage drop of 26mV at 8A of current. This translates into typical power dissipation of 208mW, which is significantly lower than the 3.2W of conventional Schottky diodes. The SM74611 is also footprint and pin compatible with conventional D2PAK Schottky diodes, making it a drop-in replacement in many applications.

TYPICAL APPLICATION CIRCUITS



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

CONNECTION DIAGRAM

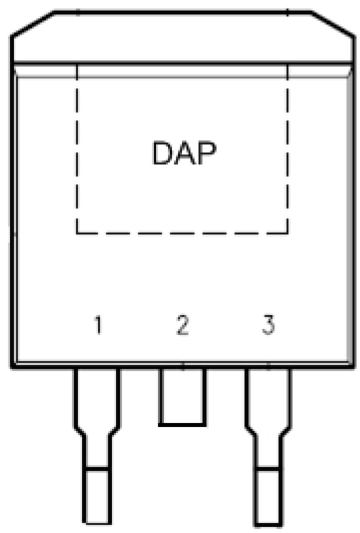


Figure 1. D2PAK

PIN DESCRIPTIONS

Pin		DESCRIPTION
NO.	NAME	
1,3 (1)	ANODE	Connect both of these pins to the negative side of the PV cells
2,DAP (2)	CATHODE	Pin 2 and the DAP are shorted internally. Connect the DAP to the positive side of the PV cells

(1) Pin 1 and Pin 3 should be connected together for proper operation
(2) Package drawing at the end of datasheet is shown without Pin 2 being trimmed

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

DC Reverse Voltage	30V
Forward Current	15A
Ambient Storage Temperature	-65°C to 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

RECOMMENDED OPERATING CONDITIONS (1)

DC Reverse Voltage	28V
Junction Temperature Range (T_J)	-40°C to 125°C
Forward Current	0-15A

(1) System must be thermally managed so as not to exceed maximum junction temperature

ESD RATINGS

All Pins, Human Body Model (HBM)	>1kV
All Pins, Charge Model (CDM)	>250V

ELECTRICAL CHARACTERISTICS(1)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{F(AVG)}$	Forward Current				8	15	A
$V_{F(AVG)}$	Forward Voltage	I_F = 8A	T_J = 25°C		26		mV
P_D	Power Dissipation	I_F = 8A	T_J = 25°C		208		mW
			T_J = 125°C		450	**575**	
		I_F = 15A	T_J = 25°C		695		
			T_J = 125°C		1389		
D	Duty Cycle	I_F = 8A	T_J = 25°C		99.5		%
			T_J = 125°C		96.0		
R_{JC}	Thermal Resistance, FET Junction to Case (D2PAK)				0.5		°C/W
I_R	Reverse Leakage Current	$V_{REVERSE}$ = 28V	T_J = 25°C		0.3		µA
			T_J = 125°C		3.3		

(1) Limits appearing in **boldface** type apply over the entire junction temperature range for operation. Limits appearing in normal type apply for T_A = T_J = 25°C.

TYPICAL CHARACTERISTICS

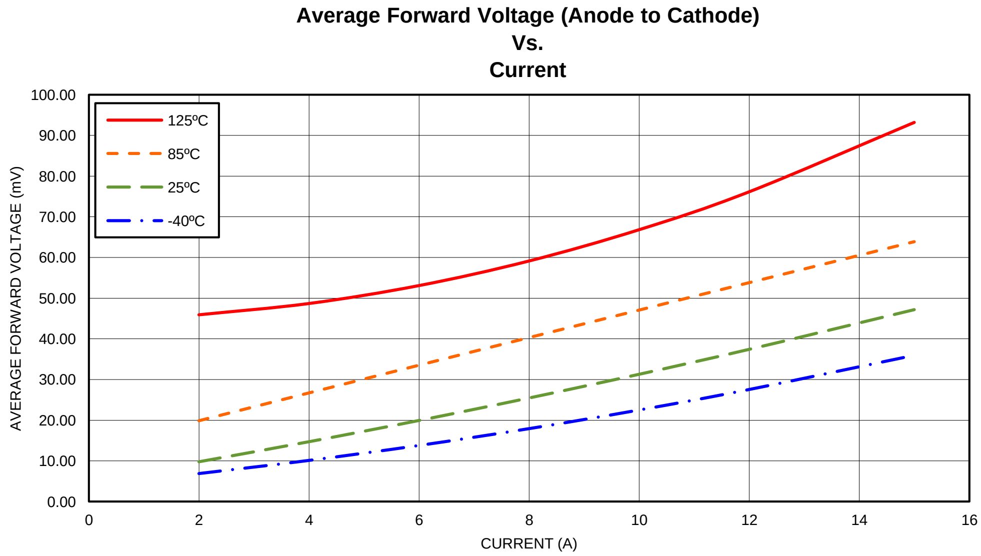


Figure 2. Average Forward Voltage (Anode to Cathode) Over Temperature

TYPICAL CHARACTERISTICS (continued)

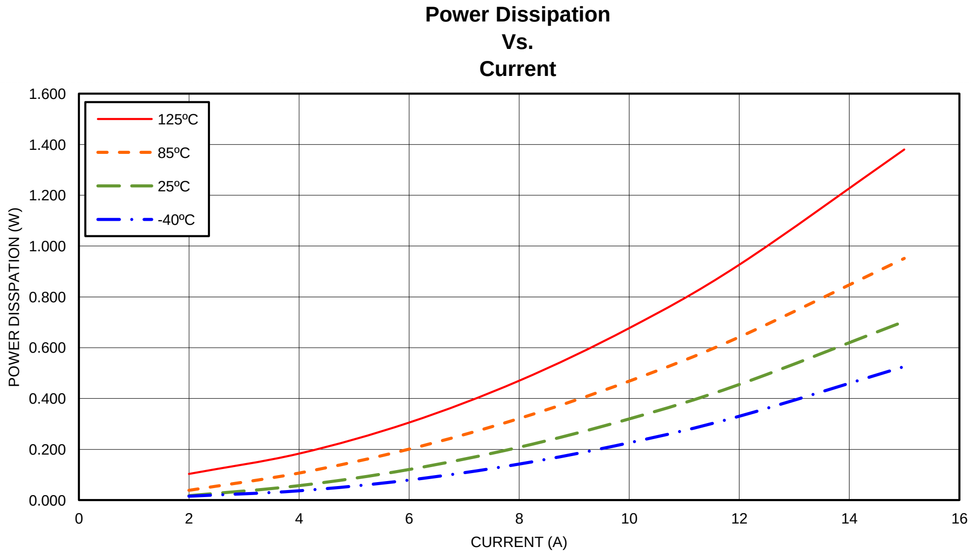


Figure 3. Power Dissipation Over Temperature

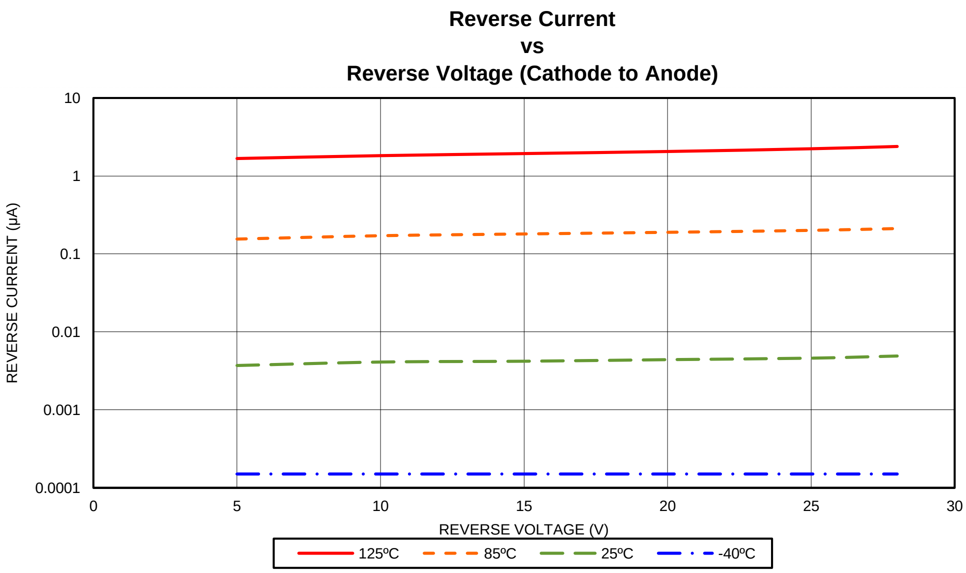


Figure 4. Reverse Current Over Temperature

APPLICATION INFORMATION

The SM74611 is designed for use as a bypass diode in photovoltaic modules. The SM74611 utilizes a charge pump to drive an N-channel FET to provide a resistive path for the bypass current to flow. Please refer to Figure 5 and Figure 6 for operational description below

From t_0 to t_1:

When cells in the solar panels are shaded, the FET Q1 is off and the bypass current will flow through the body diode of the FET as shown on Figure 5. This current will produce a voltage drop (V_F) across ANODE and CATHODE terminal of the bypass diode. During this time, the charge pump circuitry is active and charging capacitor C1 to a higher voltage.

At t_1:

Once the voltage on the capacitor reaches its predetermined voltage level, the charge pump is disabled and the capacitor voltage is used to drive the FET through the FET driver stage.

From t_1 to t_2 :

When the FET is active, it provides a low resistive path for the bypass current to flow thus minimizing the power dissipation across ANODE and CATHODE. Since the FET is active, the voltage across the ANODE and CATHODE is too low to operate the charge pump. During this time, the stored charge on C1 is used to supply the controller as well as drive the FET.

At t_2:

When the voltage on the capacitor C1 reaches its predetermined lower level, the FET driver shuts off the FET. The bypass current will then begin to flow through the body diode of the FET, causing the FET body diode voltage drop of approximately 0.6V to appear across ANODE and CATHODE. The charge pump circuitry is re-activated and begins charging the capacitor C1. This cycle repeats until the shade on the panel is removed and the string current begins to flow through the PV cells instead of the body diode of the FET.

The key factor to minimizing the power dissipation on the device is to keep the FET on at a high duty cycle. The average forward voltage drop will then be reduced to a much lower voltage than for a Schottky or regular P-N junction diode.

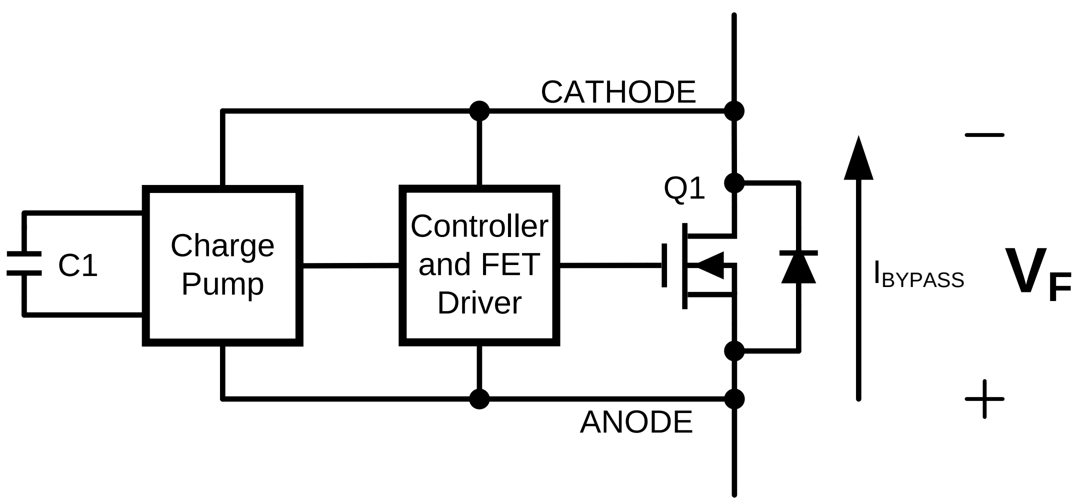


Figure 5. SM74611 Block Diagram

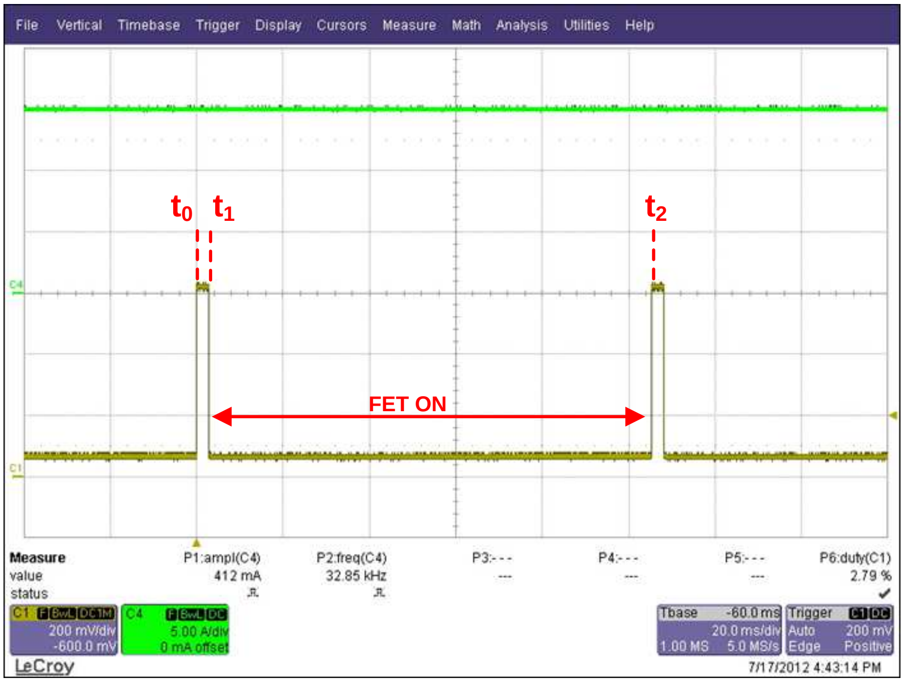


Figure 6. ANODE to CATHODE voltage (Ch1) with I_{BYPASS} = 15A (Ch4) for SM74611 in Junction Box at 85˚C ambient

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SM74611KTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	SM74611KTT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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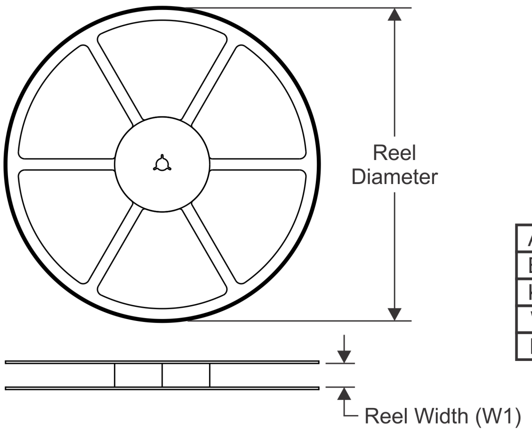
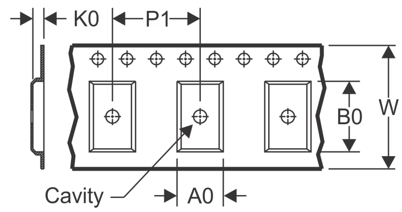
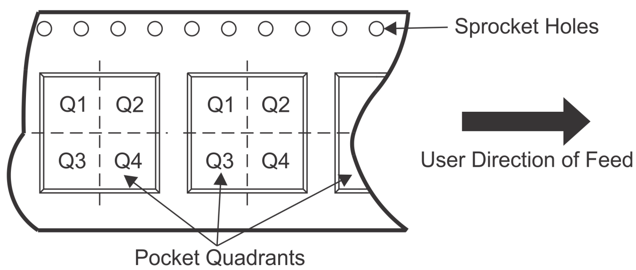


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

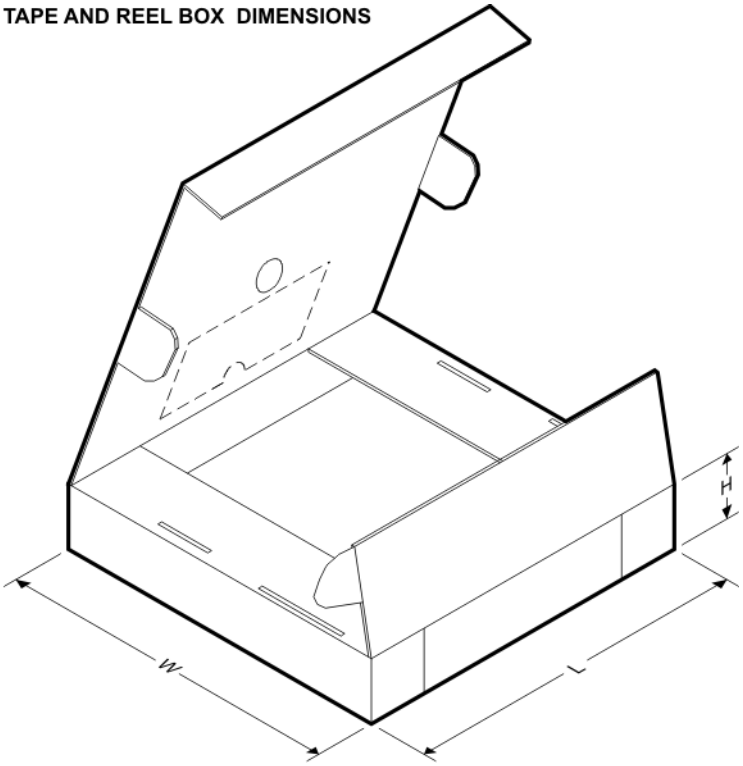
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SM74611KTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

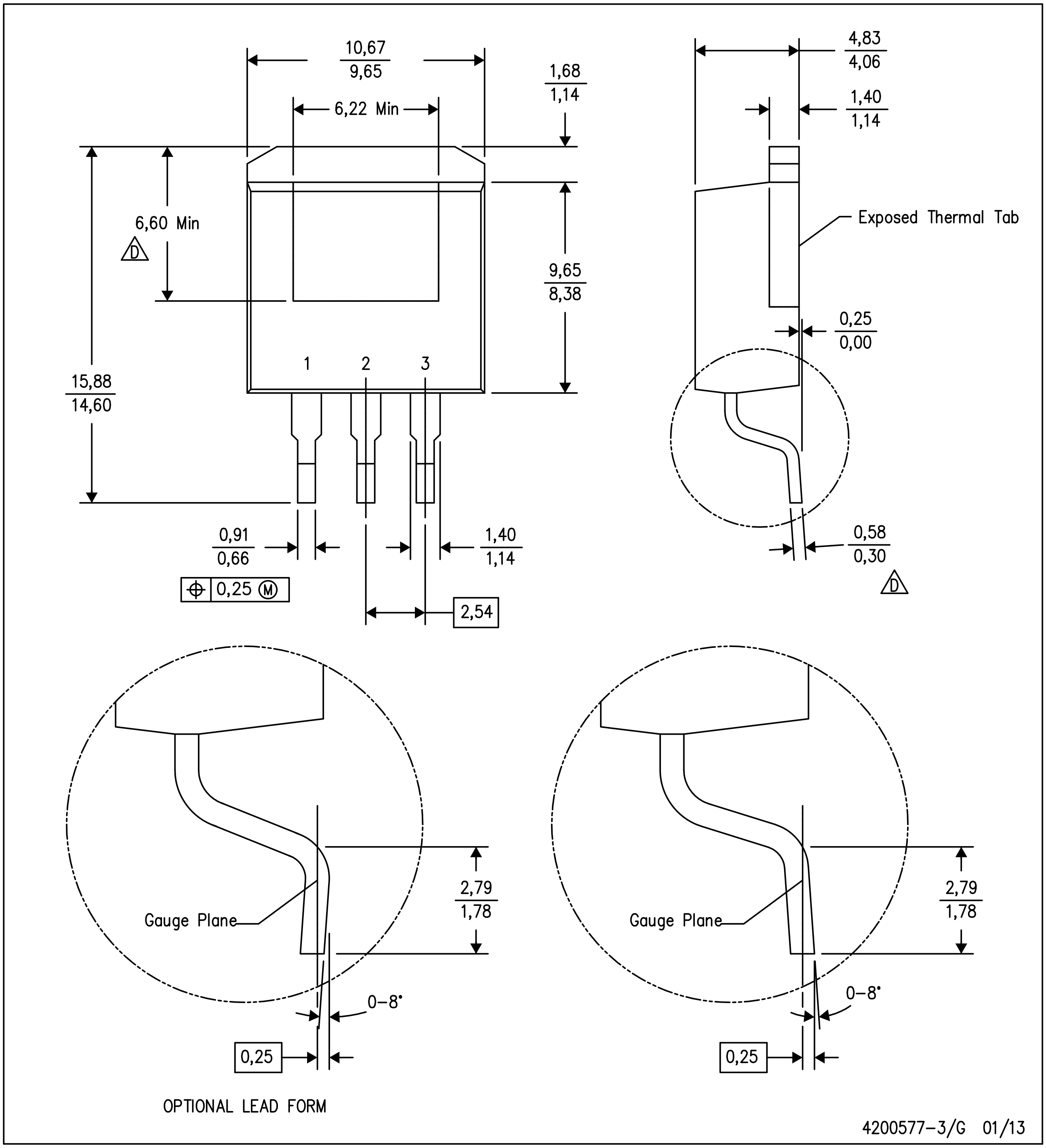
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SM74611KTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

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