![TEXAS INSTRUMENTS]

LMX2525

LMX2525 PLLatinum™ Dual Frequency Synthesizer System with Integrated VCOs

Check for Samples: LMX2525

FEATURES

- **Small Size**
  - **5.0 mm X 4.0 mm X 0.75 mm 24-Pin WQFN Package**
- **RF Synthesizer System**
  - **Two Integrated VCOs**
  - **Integrated Loop Filter**
  - **Low Spurious, Low Phase Noise Fractional-N RF PLL Based on 10-Bit Delta Sigma Modulator**
  - **Frequency Resolution Down to 20 kHz**
- **Supports Various Reference Frequencies**
  - **12.6 MHz, 14.4 MHz, 25.2MHz, and 26.0 MHz**
- **Fast Lock Time: 300 µs**
- **Low Current Consumption**
  - **10 mA at 2.8 V in PDC800 Mode**
- **2.5 V to 3.3 V Operation**
- **Digital Filtered Lock Detect Output**
- **Hardware and Software Power Down Control**

APPLICATIONS

- **Japan PDC Systems at 800 MHz and 1500 MHz Frequency Bands**

DESCRIPTION

LMX2525 is a highly integrated, high performance, low power frequency synthesizer system optimized for dual-band Japan PDC mobile handsets. Using a proprietary digital phase locked loop technique, LMX2525 generates very stable, low noise local oscillator signals for up and down conversion in wireless communications devices.

LMX2525 includes dual voltage controlled oscillators (VCOs) for the upper and lower Japan PDC frequency bands, a loop filter, and a fractional-N RF PLL based on a delta sigma modulator. In concert, these blocks form a closed loop RF synthesizer system. The RF synthesizer system supports two frequency bands: PDC1500 and PDC800.

Serial data is transferred to the device via a three-wire MICROWIRE interface (DATA, LE, CLK).

Operating supply voltage ranges from 2.5 V to 3.3 V. LMX2525 features low current consumption: 10 mA at 2.8 V when operating in the PDC800 mode.

LMX2525 is available in a 24-pin WQFN package.
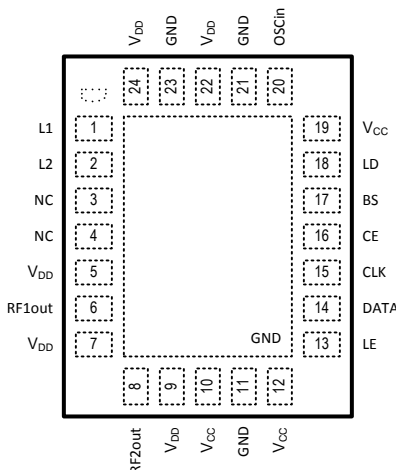
Functional Block Diagram
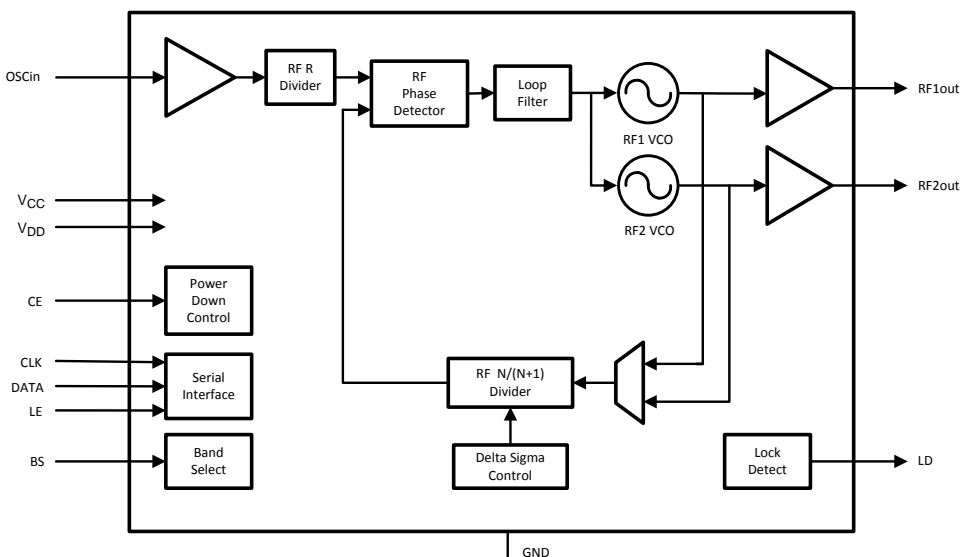
Connection Diagram

Figure 1. 24-Pin 5x4 WQFN (NHW0024B) Package

Note: Analog ground connected through exposed die attached pad.

PIN DESCRIPTIONS

Pin Number	Name	I/O	Description
1	L1	—	RF2 VCO tank pin. An external inductor is required between pins L1 and L2 to set the resonant frequency of RF2 VCO (PDC800).
2	L2	—	RF2 VCO tank pin. An external inductor is required between pins L1 and L2 to set the resonant frequency of RF2 VCO (PDC800).
3	NC	—	Do not connect to any node on the printed circuit board.
4	NC	—	Do not connect to any node on the printed circuit board.
5	V_{DD}	—	Supply voltage for RF analog circuitry
6	RF1out	O	RF output of RF1 VCO for PDC1500
7	V_{DD}	—	Supply voltage for RF analog circuitry
8	RF2out	O	RF output of RF2 VCO for PDC800
9	V_{DD}	—	Supply voltage for analog circuitry
10	V_{CC}	—	Supply voltage for digital circuitry
11	GND	—	Ground for digital circuitry
12	V_{CC}	—	Supply voltage for digital circuitry
13	LE	I	MICROWIRE Latch Enable
14	DATA	I	MICROWIRE Data
15	CLK	I	MICROWIRE Clock
16	CE	I	Chip enable control pin
17	BS	I	Band select control pin
18	LD	O	Lock detect pin
19	V_{CC}	—	Supply voltage for digital circuitry
20	OSCin	I	Reference frequency input
21	GND	—	Ground for digital circuitry
22	V_{DD}	—	Supply voltage for analog circuitry
23	GND	—	Ground for analog circuitry
24	V_{DD}	—	Supply voltage for RF analog circuitry
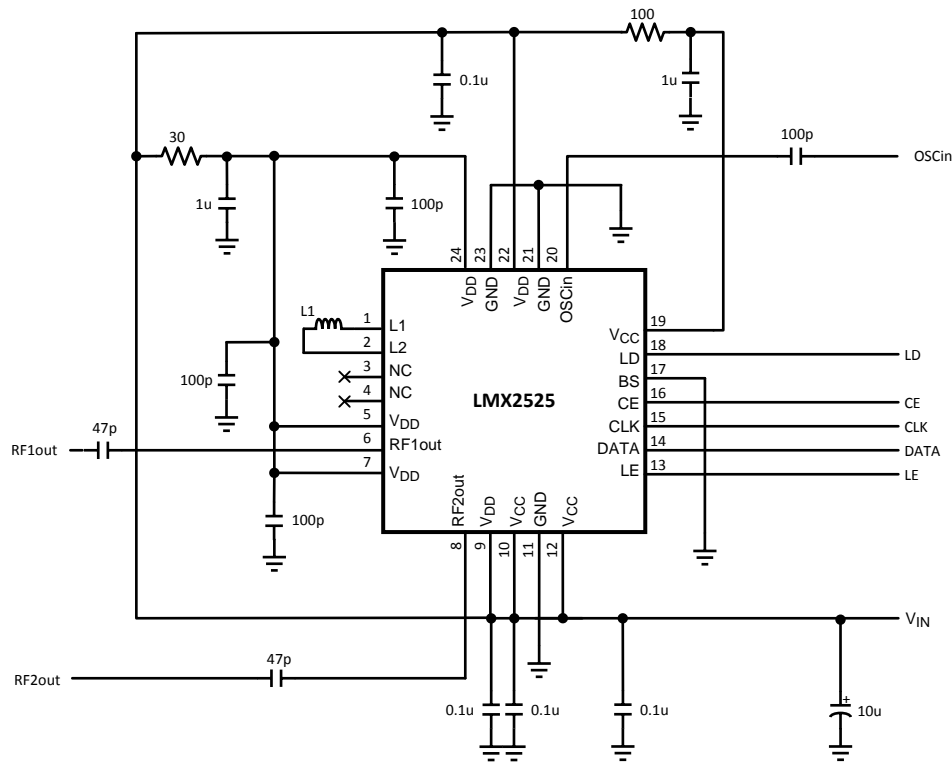
Product Folder Links: *LMX2525*

Typical Application Circuit

Refer to RF2 VCO Tuning Range vs. External Inductance plot to aid in selecting the appropriate external inductance,
PCB trace and L1, for the desired frequency range.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2][3][4]

Parameter	Symbol	Ratings	Units
Supply Voltage	V_{CC}, V_{DD}	-0.5 to 3.6	V
Voltage on any pin to GND	V_I	-0.3 to V_{CC} + 0.3	V
		-0.3 to V_{DD} + 0.3	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate
    conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed
    specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the
    conditions listed.
(2) This device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this
    device should be done at ESD protected workstations.
(3) GND = 0 V.
(4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and
    specifications.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	-30	25	85	°C
Supply Voltage (to GND)	V_{CC}, V_{DD}	2.5		3.3	V

Product Folder Links: *LMX2525*

Electrical Characteristics[1]

(V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for T_A = 25 °C; Limits in **boldface** type apply over the operating temperature range from -20 °C ≤ T_A ≤ 75 °C unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC} PARAMETERS						
I_{CC} + I_{DD}	Supply Current[2]	OB_CRL [1:0] = 10		10.6	12.0 **12.3**	mA
		OB_CRL [1:0] = 00		10.0	11.5 **11.8**	mA
I_{CC} + I_{DD}	Supply Current[3]	OB_CRL [1:0] = 10		15.0	16.5 **16.8**	mA
		OB_CRL [1:0] = 00		14.2	15.6 **15.9**	mA
I_{PD}	Power Down Current	CE = LOW or RF_PD = 1			20	µA
REFERENCE OSCILLATOR PARAMETERS						
f_{OSCin}	Reference Oscillator Input Frequency[4]	Supports 12.6, 14.4, 25.2 and 26.0 MHz.	12.6	14.4	26.0	MHz
V_{OSCin}	Reference Oscillator Input Sensitivity			0.5	V_{CC}	Vp-p
RF1 VCO FOR PDC1500						
f_{RF1out}	Frequency Range[5]	RF1 VCO for PDC1500	1270.22		1394.95	MHz
P_{RF1out}	Output Power	OB_CRL [1:0] = 11	**-5**	-2	**1**	dBm
		OB_CRL [1:0] = 10	**-7**	-4	**-1**	dBm
		OB_CRL [1:0] = 01	**-10**	-7	**-4**	dBm
		OB_CRL [1:0] = 00	**-13**	-10	**-7**	dBm
	Lock Time	Full frequency span within each band in High Speed Mode (HS = 1).			**300**[6]	µs
		Between bands High Speed Mode (HS = 1).			**300**[6]	µs
		Full frequency span within each band in Normal Mode (HS = 0). [7]			**500**[6]	µs
					375[8]	µs
		Between bands in Normal Mode (HS = 0).			**500**[6]	µs
					400[8]	µs
	RMS Phase Error			1.3		degrees
$L(f)_{RF1out}$	Phase Noise when RF1 VCO for PDC1500 is activated in Normal Mode (HS = 0).	@ 25 kHz offset		-95	-93 **-91**	dBc/Hz
		@ 50 kHz offset		-106	-103 **-101**	dBc/Hz
		@ 100 kHz offset		-115	-113 **-111**	dBc/Hz
		@ 1 MHz offset			-135 **-133**	dBc/Hz
	2nd Harmonic Suppression				**-25**	dBc

(1) All limits are ensured. All electrical characteristics having room temperature limits are tested during production with T_A = 25 °C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) RF PLL and VCO in PDC800 mode.
(3) RF PLL and VCO in PDC1500 mode.
(4) The reference frequency must be programmed using the OSC_FREQ control bit. For other reference frequencies, please contact National Semiconductor.
(5) For other frequency ranges, please contact National Semiconductor.
(6) Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/-1 kHz of the final frequency.
(7) Lock time specification also applies to power up with MICROWIRE serial interface.
(8) Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/-3 kHz of the final frequency.

Electrical Characteristics[(1)] (continued)

(V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for T_A = 25 °C; Limits in **boldface** type apply over the operating temperature range from -20 °C ≤ T_A ≤ 75 °C unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
	3rd Harmonic Suppression	OB_CRL [1:0] = 11, 10, 01			**-20**	dBc
		OB_CRL [1:0] = 00			-14 **-11**	dBc
	Spurious Tones	@ ≤ 25 kHz offset			**-45**	dBc
		@ 25 kHz < offset ≤ 50 kHz			**-60**	dBc
		@ 50 kHz < offset ≤ 100 kHz			**-69**	dBc
		@ offset > 100 kHz			**-75**	dBc
RF2 VCO FOR PDC800						
f_{RF2out}	Frequency Range[(5)]	RF2 VCO for PDC800	633.15		768.00	MHz
P_{RF2out}	Output Power	OB_CRL [1:0] = 11	**-6**	-3	**0**	dBm
		OB_CRL [1:0] = 10	**-9**	-6	**-3**	dBm
		OB_CRL [1:0] = 01	**-11**	-8	**-5**	dBm
		OB_CRL [1:0] = 00	**-15**	-12	**-9**	dBm
	Lock Time	Full frequency span within each band in High Speed Mode (HS = 1).			**300**[(6)]	µs
		Between bands High Speed Mode (HS = 1).			**300**[(6)]	µs
		Full frequency span within each band in Normal Mode (HS = 0).[(7)]			**500**[(6)]	µs
					375 [(8)]	µs
		Between bands in Normal Mode (HS = 0).			**500**[(6)]	µs
					400[(8)]	µs
	RMS Phase Error			1.3		degrees
$L(f)_{RF2out}$	Phase Noise when RF2 VCO for PDC800 is activated in Normal Mode (HS = 0).	@ 25 kHz offset		-95	-93 **-91**	dBc/Hz
		@ 50 kHz offset		-106	-103 **-101**	dBc/Hz
		@ 100 kHz offset		-115	-113 **-111**	dBc/Hz
		@ 1 MHz offset			-135 **-133**	dBc/Hz
	2nd Harmonic Suppression				**-25**	dBc
	3rd Harmonic Suppression	OB_CRL[1:0] = 11, 10, 01			**-20**	dBc
		OB_CRL[1:0] = 00			-14 **-11**	dBc
	Spurious Tones	@ ≤ 25 kHz offset			**-45**	dBc
		@ 25 kHz < offset ≤ 50 kHz			**-60**	dBc
		@ 50 kHz < offset ≤ 100 kHz			**-69**	dBc
		@ offset > 100 kHz			**-75**	dBc
DIGITAL INTERFACE (DATA, CLK, LE, LD, CE, BS)						
V_{IH}	High-Level Input Voltage		0.8 V_{CC}		V_{CC}	V
			0.8 V_{DD}		V_{DD}	V
V_{IL}	Low-Level Input Voltage		-0.3		0.2 V_{CC}	V
			-0.3		0.2 V_{DD}	V
I_{IH}	High-Level Input Current		-10		10	µA
I_{IL}	Low-Level Input Current		-10		10	µA
	Input Capacitance			3		pF
	Rise/Fall Time			30		ns

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Electrical Characteristics[1] (continued)

(V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for T_A = 25 °C; Limits in **boldface** type apply over the operating temperature range from -20 °C ≤ T_A ≤ 75 °C unless otherwise noted.)

| Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	High-Level Output Voltage		V_{CC} - 0.4			V
			V_{DD} - 0.4			V
V_{OL}	Low-Level Output Voltage				0.4	V
	Output Capacitance				5	pF
MICROWIRE INTERFACE TIMING						
t_{CS}	Data to Clock Set Up Time		50			ns
t_{CH}	Data to Clock Hold Time		10			ns
t_{CWH}	Clock Pulse Width HIGH		50			ns
t_{CWL}	Clock Pulse Width LOW		50			ns
t_{DS}	Latch Enable LOW to Data Set Up Time		50			ns
t_{ES}	Clock to Latch Enable Set Up Time		50			ns
t_{EW}	Latch Enable Pulse Width		50			ns

MICROWIRE Interface Timing Diagram
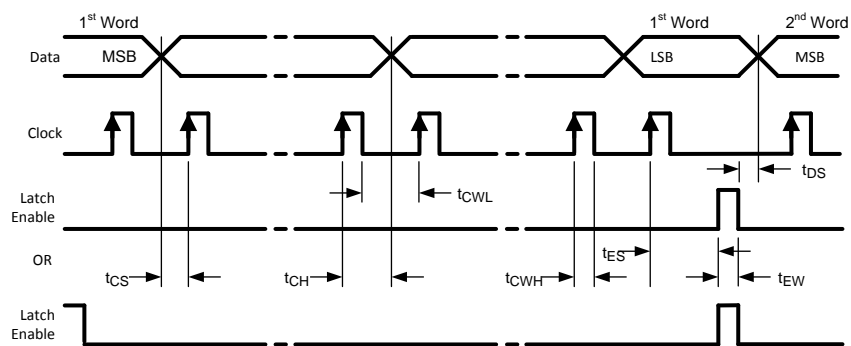
Figure 2. MICROWIRE Interface Timing Diagram

Typical Performance Characteristics[1]
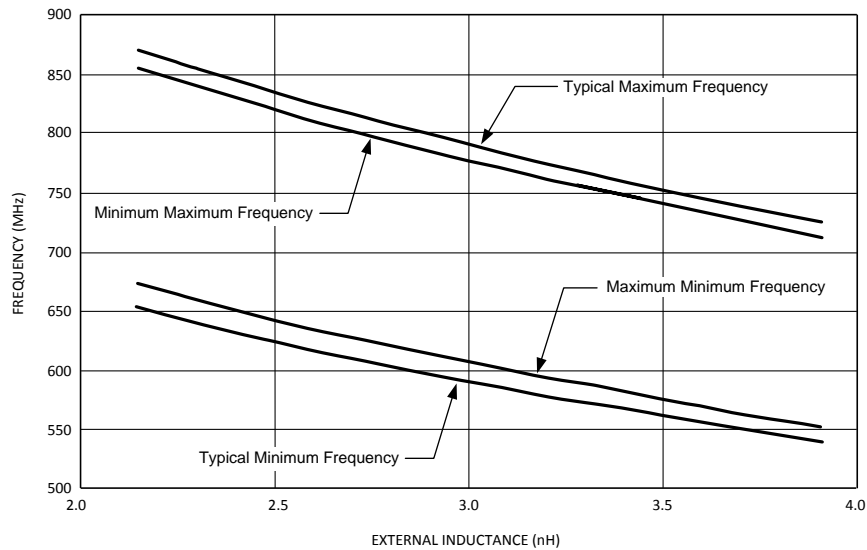
The frequency range is defined as the difference between the highest frequency and the lowest frequency of a given unit. For a chosen external inductance, the typical frequency range equals the difference between the Typical Maximum Frequency and the Typical Minimum Frequency. Typical frequency range may be assumed on any unit with that chosen external inductance, even if the unit has worst case Maximum Frequency or worst case Minimum Frequency.

Figure 3. RF2 VCO Tuning Range vs. External Inductance V_{IN} = 2.8 V

(1) Typical performance characteristics do not ensure specific performance limits. For ensured specifications, refer to the Electrical Characteristics section.

FUNCTIONAL DESCRIPTION

GENERAL

The LMX2525 is a highly integrated frequency synthesizer system for Japan PDC wireless communication systems. The LMX2525 supports dual band operation for 800 MHz and 1500 MHz.

The LMX2525 includes all functional blocks for the RF PLL including RF VCOs, frequency dividers, PFDs, and loop filters. Only external passive elements for the RF2 VCO tank and supply bypassing are required to complete the RF synthesizer.

The LMX2525 uses a patent pending Fractional-N synthesizer architecture based on a delta sigma modulator to support fine frequency resolution. Four of the most common reference frequencies for PDC applications, 12.6 MHz, 14.4 MHz, 25.2 MHz and 26.0 MHz, are supported. The unique feature of this architecture is its low spurious modulation effect.

The use of a fractional synthesizer based on a delta sigma modulator allows for faster lock and system set-up times, which reduces system power consumption. The loop filter is included on chip to minimize the external noise coupling and to reduce the form factor applicable to the board level application. Only one of the two RF VCOs is activated at a given time, and each output is provided through its own output pin.

RF PLL SECTION

Frequency Selection

The divide ratio can be calculated using the following equations:

$f_{VCO} = \{8 \times RF\_B + RF\_A + (RF\_FN / FD)\} \times (f_{OSC} / R)$ where $(RF\_A < RF\_B)$ for PDC1500

$f_{VCO} = \{4 \times RF\_B + RF\_A + (RF\_FN / FD)\} \times (f_{OSC} / R)$ where $(RF\_A < RF\_B)$ for PDC800

where

- f_{VCO}: Output frequency of voltage controlled oscillator (VCO)
- RF_B: Preset divide ratio of binary 4-bit programmable counter ($2 \leq RF\_B \leq 15$)
- RF_A: Preset divide ratio of binary 3-bit swallow counter ($0 \leq RF\_A \leq 7$ for PDC1500 and $0 \leq RF\_A \leq 3$ for PDC800)
- RF_FN: Preset numerator of binary 10-bit modulus counter ($0 \leq RF\_FN < FD$)
- FD: Preset denominator for modulus counter ($FD = f_{OSC}/(R \times f_{CH})$ where f_{CH} is the channel spacing)
- f_{OSC}: Reference oscillator frequency
- R: Internal reference oscillator frequency divider (1 for 12.6 MHz and 14.4 MHz, 2 for 25.2 MHz and 26.0 MHz)

The denominator, FD, in the above equation is dependent on the channel spacing and reference oscillator frequency. The channel spacing will change based on the Rx/Tx and BS bits. Table 8 in the R0 Register section summarizes the values of FD.

VCO Frequency Tuning

The center frequency of the RF VCOs are determined by the resonant frequency of the tank circuit, illustrated in Figure 4. With an internal fixed bonding-wire inductor and an external inductance, the center frequency of the VCO is given as follows:

$$f_{center} = \frac{1}{2\pi\sqrt{(L_{fixed} + L_{external}) \cdot C_{total}}}$$

where C_{total} is the total capacitance of the VCO, including the parasitic capacitance and the nominal self-tuning capacitance. Note, the external inductance consists of the PCB traces and lumped element inductor. The output frequency tuning range can be optimized for the specific application by selecting the appropriate external inductance. Refer to RF2 VCO Tuning Range vs. External Inductance plot to aid in selecting the appropriate external inductance. Care should be taken to ensure proper frequency coverage when choosing the tolerance of the lumped element inductor. For the 1500 MHz band, the internal bonding-wires provide the necessary inductance to set the VCO center frequency.
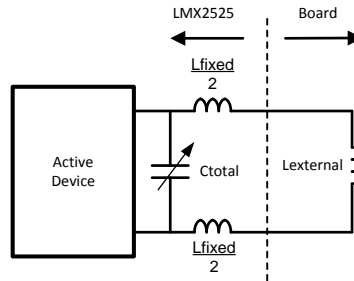
Figure 4. External Inductor Connection

In real implementation, the inductance of L_{fixed} and $L_{external}$ can vary from its nominal value. The LMX2525 utilizes a built-in tracking algorithm to compensate for variations up to ±15% and tunes the VCO to the required frequency. During the frequency acquisition period, the loop bandwidth is extended to achieve the frequency lock. After the frequency lock, the loop bandwidth of the PLL is set to the nominal value and the phase lock is achieved. The transition between the two operating modes is very smooth and extremely fast to meet the stringent PDC requirements for lock time and phase noise.

POWER DOWN MODE

The LMX2525 includes the power down mode to reduce the power consumption. The LMX2525 enters the power down mode either by taking the CE pin LOW or by setting the RF_PD bit in the R0 register. If the CE pin is set LOW, the circuit is powered down regardless of the register values. When the CE pin is HIGH, the RF_PD bit controls power to the RF circuitry. Data can be written to the registers even when the CE pin is set LOW. The following truth table summarizes the power down logic.

Table 1. Power Down Modes

CE Pin	RF_PD Bit	Mode
HIGH	0	Active
HIGH	1	Not Active
LOW	0	Not Active
LOW	1	Not Active

BAND SELECT MODE

The BS pin and BS bit can be used to select one of the two RF VCO outputs. When using the BS pin, the BS bit must be set to 0, and when using the BS bit, the BS pin must be tied to ground. When using the BS pin, the state of the input must exceed the minimum band select set up time prior to the LE signal transition. The truth table summarizing the band select logic is as follows:

Table 2. Band Select Modes

BS Pin	BS Bit	Mode
HIGH	0	PDC1500
LOW	0	PDC800
LOW	1	PDC1500

LOCK DETECT MODE

The LD output can be used to indicate the lock status of the PLL. Bit 6 in Register R1 determines the signal that appears on the LD pin. When the PLL is not locked, the LD pin remains LOW. After obtaining phase lock, the LD pin will have a logical HIGH level. The LD output is always LOW when the LD register bit is 0 and in power down mode.

Table 3. Lock Detect Modes

LD Bit	Mode
0	Disable (GND)
1	Enable

Table 4. Lock Detect Logic

RF PLL Section	LD Output
Locked	HIGH
Not Locked	LOW
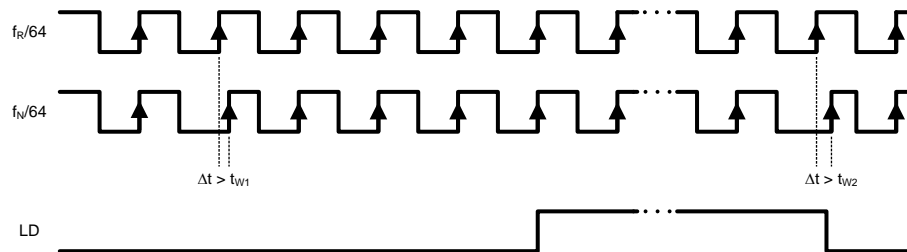
A. LD output becomes LOW when the phase error is larger than t_{W2}.

B. LD output becomes HIGH when the phase error is less than t_{W1} for four or more consecutive cycles.

C. Phase Error is determined on the leading edge. Only errors greater than t_{W1} and t_{W2} are labeled.

D. t_{W1} is 5 ns for PDC1500 and 10 ns for PDC800. t_{W2} is 10 ns for both bands.

E. The lock detect comparison occurs with every 64th cycle of f_R and f_N.

Figure 5. Lock Detect Timing Diagram Waveform
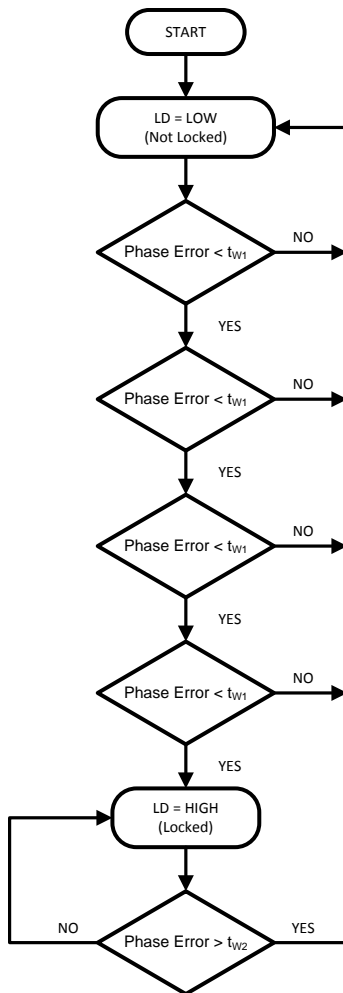
Figure 6. Lock Detect Flow Diagram

LOCKING MODES

Two frequency-locking modes are provided: a Normal mode and a High Speed mode for faster lock times. The HS bit in register R0 controls the locking mode.

Table 5. Locking Modes

HS Bit	Mode
0	Normal mode
1	High Speed mode

MICROWIRE INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: CLK, DATA, and LE (Latch Enable). Serial data is clocked into the 24-bit shift register on the rising edge of the clock. The last bits decode the internal control register address. When the latch enable (LE) transitions from LOW to HIGH, data stored in the shift registers is loaded into the corresponding control register. The data is loaded MSB first.

Programming Description

GENERAL PROGRAMMING INFORMATION

The serial interface has a 24-bit shift register to store the incoming data bits temporarily. The incoming data is first loaded into the shift register from MSB to LSB. The data is shifted at the rising edge of the clock signal. When the latch enable signal transitions from LOW to HIGH, the data stored in shift register is transferred to the proper register depending on the address bit setting. The selection of the particular register is determined by the control bits indicated in boldface text.

At initial start-up, the MICROWIRE loading requires three default words (registers R2, loaded first, to R0, loaded last). After the device has been initially programmed, the RF VCO frequency can be changed using a single register (R0).

The control register content map describes how the bits within each control register are allocated to the specific control functions.

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Table 6. COMPLETE REGISTER MAP[1][2]

Register	MSB							SHIFT REGISTER BIT LOCATION																	LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0 (Default)	RX/TX	RF_PD	HS	0	BS	RF_B [3:0]				RF_A [2:0]			RF_FN [9:0]										0	0
R1 (Default)	SPI_DEF	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	LD	OB_CRL [1:0]		OSC_FREQ [1:0]		0	1
R2 (Default)	1	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0
R3	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	**0**	1	1
R4	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	1	0	**0**	1	1	1
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	1	1	1	1

(1) **Note:** R0 control register will be used when hot start frequency change.
(2) **Note:Boldface** text represent address bits.

R0 REGISTER

The R0 register address bits (R0 [1:0]) are "00".

The Rx/Tx bit selects between receive and transmit modes and, in conjunction with the band select bit (BS), the channel spacing to be synthesized.

The RF_PD bit selects the power down mode of the RF PLL and selected VCO.

The HS bit selects between normal and high speed locking mode.

The BS bit determines which of the two internal VCOs (PDC800 or PDC1500) is active.

The RF N counter consists of the 4-bit programmable counter (RF_B counter), the 3-bit swallow counter (RF_A counter) and the 10-bit delta sigma modulator (RF_FN counter). The equations for calculating the counter values are presented below.

Table 7. R0 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Data Field																					Address Field	
R0 (Default)	RX/TX	RF_PD	HS	0	BS	RF_B [3:0]				RF_A [2:0]			RF_FN [9:0]										0	0

Name	Functions
RX/TX	**RX/TX Mode** 0 = Rx 1 = Tx
RF_PD	**Power Down of RF Synthesizer** 0 = RF synthesizer on (Active mode) 1 = RF synthesizer powered down
HS	**Locking Mode** 0 = Normal Mode 1 = High Speed Mode
BS	**Band Select** 1 = RF1 VCO (PDC1500) 0 = RF2 VCO (PDC800)
RF_B [3:0]	**RF_B Counter** 4-bit programmable counter $0 \leq RF\_B \leq 15$ for both bands
RF_A [2:0]	**RF_A Counter** 3-bit swallow counter $0 \leq RF\_A \leq 7$ for PDC1500 $0 \leq RF\_A \leq 3$ for PDC800
RF_FN [9:0]	**RF_FN Counter** 10-bit modulus counter $0 \leq RF\_FN < FD$ See Table 8 for FD values.

Counter Name	Symbol	Functions
Modulus Counter	RF_FN	**RF N Divider** $N = 8 \times RF\_B + RF\_A + RF\_FN/FD$ (PDC1500) $N = 4 \times RF\_B + RF\_A + RF\_FN/FD$ (PDC800)
Programmable Counter	RF_B	
Swallow Counter	RF_A	

PULSE SWALLOW FUNCTION

$f_{VCO} = \{8 \times RF\_B + RF\_A + (RF\_FN / FD)\} \times f_{OSC} / R$ where (RF_A < RF_B) for PDC1500

$f_{VCO} = \{4 \times RF\_B + RF\_A + (RF\_FN / FD)\} \times f_{OSC} / R$ where (RF_A < RF_B) for PDC800

f_{VCO}: Output frequency of voltage controlled oscillator (VCO)

RF_B: Preset divide ratio of binary 4-bit programmable counter (2 ≤ RF_B ≤ 15)

RF_A: Preset divide ratio of binary 3-bit swallow counter (0 ≤ RF_A ≤ 7 for PDC1500 and 0 ≤ RF_A ≤ 3 for PDC800)

RF_FN: Preset numerator of binary 10-bit modulus counter (0 ≤ RF_FN < FD)

FD: Preset denominator for modulus counter (FD = $f_{OSC}/(R \times f_{CH})$ where f_{CH} is the channel spacing)

f_{OSC}: Reference oscillator frequency

R: Internal reference oscillator frequency divider

OSC_FREQ [1:0]	Reference Oscillator Frequency (MHz)	R Divider
00	12.6	1
01	14.4	1
10	25.2	2
11	26.0	2

The value of the denominator (FD) is depended on the channel spacing and reference oscillator frequency. Table 8 summarizes the denominator values based on the settings of the Rx/Tx, BS, and OSC_FREQ [1:0] bits.

Table 8. Demonimator Values

Rx/Tx	BS	OSC_FREQ [1:0]	Reference Oscillator Frequency (MHz)	R	f_{CH} (kHz)	Denominator(FD)
0	0	00	12.6	1	25.0	504
0	0	01	14.4	1	25.0	576
0	0	10	25.2	2	25.0	504
0	0	11	26.0	2	25.0	520
0	1	00	12.6	1	25.0	504
0	1	01	14.4	1	25.0	576
0	1	10	25.2	2	25.0	504
0	1	11	26.0	2	25.0	520
1	0	00	12.6	1	20.0	630
1	0	01	14.4	1	20.0	720
1	0	10	25.2	2	20.0	630
1	0	11	26.0	2	20.0	650
1	1	00	12.6	1	22.22	567
1	1	01	14.4	1	22.22	648
1	1	10	25.2	2	22.22	567
1	1	11	26.0	2	22.22	585

R1 REGISTER

The R1 register address bits (R1 [1:0]) are "01".

The SPI_DEF bit allows for the programming of words R3 to R5. Under most circumstances, the SPI_DEF bit should be set to 1.

The LD bit sets the function of the lock detect pin. Enabling the lock detect function provides a digital lock detect output of the active RF synthesizer at the LD pin.

The OB_CRL [1:0] bits determine the power level of the RF output buffer. The power level can be adjusted to best meet the system requirement. Refer to the Electrical Characteristics section for power output specifications.

The reference frequency selection bits, OSC_FREQ [1:0], are used to set the reference clock and R divider for use with one of the following reference frequencies: 12.6 MHz, 14.4 MHz, 25.2 MHz or 26.0 MHz. The LMX2525 uses the OSC_FREQ bits along with the BS and RX/TX bits to determine the correct divide ratios needed to meet the required channel spacing for the mode of operation selected. Refer to Table 8 for a summary of denominator values.

Table 9. R1 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Data Field																					Address Field	
R1 (Default)	SPI_DEF	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	LD	OB_CRL [1:0]		OSC_FREQ [1:0]		0	1

Name	Functions
SPI_DEF	**Default Register Selection** 0 = OFF (Use values set in R0 to R5) 1 = ON (Use default values set in R0 to R2)
LD	**Lock Detect** 0 = Disable (GND) 1 = Enable
OB_CRL [1:0]	**Output Buffer Control** 00 = Minimum Output Power 01 = 10 = 11 = Maximum Output Power
OSC_FREQ [1:0]	**Reference Frequency Selection** 00 = 12.6 MHz 01 = 14.4 MHz 10 = 25.2 MHz 11 = 26.0 MHz

R2 REGISTER

The R2 register address bits (R2 [1:0]) are "10".

Table 10. R2 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Data Field																					Address Field	
R2 (Default)	1	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0

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R3 REGISTER

The R3 register address bits (R3 [2:0]) are "011". This register is only written to if the SPI_DEF bit is set to 0.

Table 11. R3 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																					Address Field		
R3	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

R4 REGISTER

The R4 register address bits (R4 [3:0]) are "0111". This register is only written to if the SPI_DEF bit is set to 0.

Table 12. R4 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field			
R4	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	1	0	0	1	1	1

R5 REGISTER

The R5 register address bits (R5 [4:0]) are "01111". This register is only written to if the SPI_DEF bit is set to 0.

Table 13. R5 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																			Address Field				
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

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