1 Second Generation Aureus™ DSPs

1.1 Features

- DA707/B/DA787B: 32-/64-Bit 250-MHz Floating-Point DSP
- Upgrades to C67x+ CPU From DA6xx Family:
  - 2X CPU Registers [64 General-Purpose]
  - New Audio-Specific Instructions
  - Compatible With the DA6xx C67x CPU
- Enhanced Memory System
  - 192K-Byte Unified Program/Data RAM
  - 768K-Byte Unified Program/Data ROM
  - Single-Cycle Data Access From CPU
  - Large Program Cache (32K-Byte) Supports RAM, ROM, and External Memory
- External Memory Interface (EMIF) Supports:
  - 100-MHz SDRAM (16-Bit)
  - Async NOR Flash, SRAM (8- or 16-Bit)
  - NAND Flash (8- or 16-Bit)
- Enhanced I/O System
  - High-Performance Crossbar Switch
  - Dedicated McASP DMA Bus
  - Deterministic I/O Performance
- dMAX Dual Data Movement Accelerator:
  - Memory-to-Memory Transfers
  - Memory-to-Peripheral Transfers
  - Packing/Unpacking Delay Data
  - Circular Addressing
  - Non-Sequential Addressing for Reverb
- Three Multichannel Audio Serial Ports
  - Transmit/Receive Clocks up to 50 MHz
  - Five Clock Zones and 16 Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
  - DIT Only (McASP2)
- Two 10-MHz SPI Ports With 3-, 4-, and 5-Pin Options
- Two Inter-Integrated Circuit (I2C) Ports
- Real-Time Interrupt Counter/Watchdog
- Oscillator- and Software-Controlled PLL
- Commercial or Extended Temperature
- 144-Pin, 0.5-mm, PowerPAD™ Thin Quad Flatpack (TQFP) [RFP Suffix]
- Security Features Available

- Applications
  - A/V and DVD Receiver
  - Multizone A/V Receiver
  - HDD Jukebox
  - Navigation Systems
  - High-Speed Encode With Simultaneous Multichannel Decode
- Software Support
  - Dolby® Digital, Dolby® Digital EX, Dolby® Pro Logic® IIx, Dolby® Headphone, Dolby® Virtual Surround
  - DTS® 5.1, DTS-ES™ 6.1, DTS Neo:6™, DTS 96/24™, DTS-ES 96/24™ (DA787B only)
  - MPEG-2 AAC LC Decode
  - MPEG-4 AAC LC Encode/Decode
  - THX® Select 2, THX® Ultra 2, Neural-THX® Surround
  - MP3 Encode, MP3 Decode
  - WMA8 Encode, WMA9 Decode
  - HDCD® Decode
  - ATRAC3plus® Encode, ATRAC3plus® Decode
  - Audyssey MultEQ XT®, MultEQ®, PrevEQ®, 2EQ®
  - SRS® Circle Surround™ II (CS II)
  - TI Bass Boost
  - TI Perfect Playback™ Compressed Audio Enhancer
  - TI Virtualizer/Headphone
  - TI Effects Library
  - TI DSD-to-PCM Decode
  - TI Filter Library
  - TI Performance Audio Framework (PA/F)
  - TI DSP/BIOS™
  - Chip Support Library and DSP Library

1.2 Trademarks

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Contents

2 Device Overview

The TMS320DA707/B/TMS320DA787B is the second generation of Texas Instruments' Aureus™ family of high-performance 32-/64-bit floating-point digital signal processors.

Note: The **TMS320DA787B** supports DTS® 5.1, DTS-ES™ 6.1, DTS Neo:6™, DTS 96/24™, and DTS-ES 96/24™. If the application requires DTS algorithms, the TMS320DA787B DSP should be used.

Figure 2-1 illustrates a high-level block diagram of the device and other devices to which it may typically connect. An overview of each major block follows the figure.

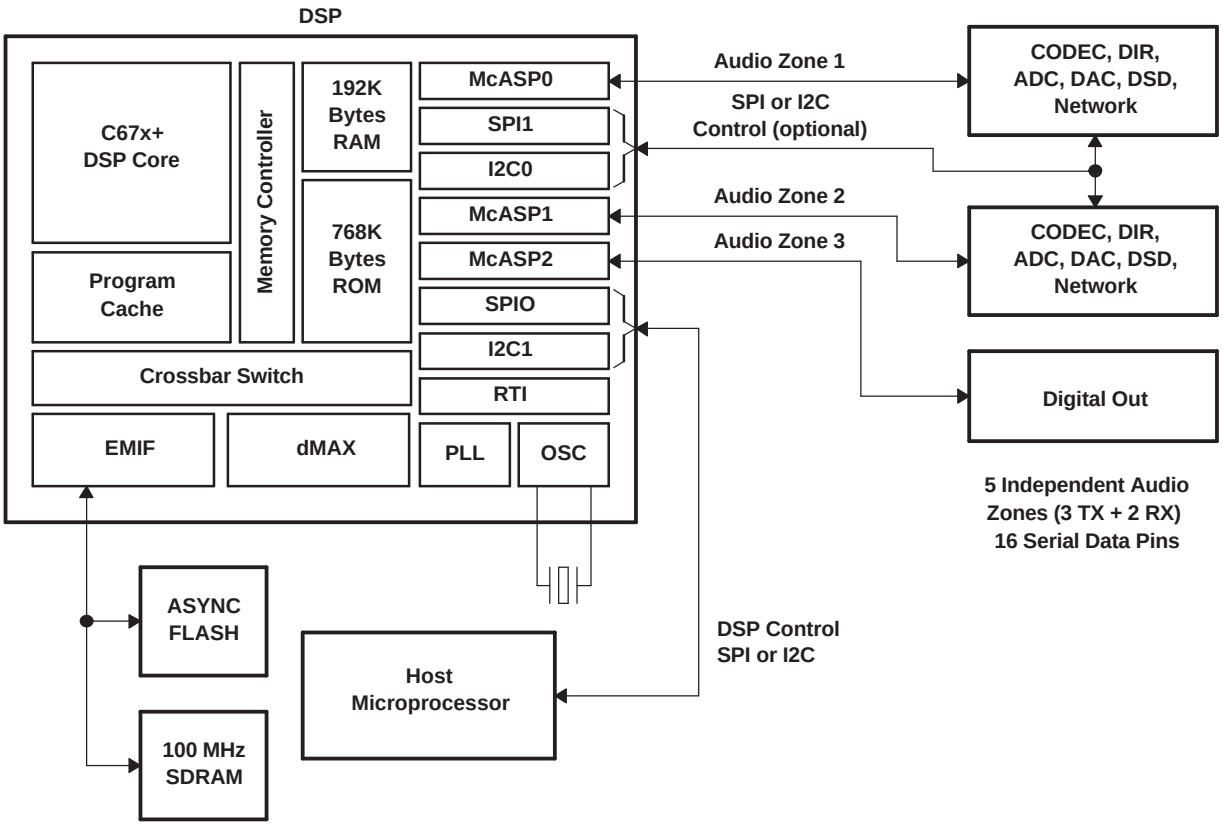

Figure 2-1. DA707/B/DA787B Aureus™ Audio DSP System Diagram

2.1 Enhanced C67x+ CPU

The C67x+ CPU is an enhanced version of the C67x CPU used on the DA6xxx first-generation Aureus™ DSP. It is compatible with the C67x CPU but offers significant improvements in speed, code density, and floating-point performance per clock cycle. At 250 MHz, the CPU is capable of a maximum performance of 2000 MIPS/1500 MFLOPS by executing up to eight instructions (six of which are floating-point instructions) in parallel each cycle. The CPU natively supports 32-bit fixed-point, 32-bit single-precision floating-point, and 64-bit double-precision floating-point arithmetic.

2.2 Efficient Memory System

The memory controller maps the large on-chip 192K-byte RAM and 768K-byte ROM as unified program/data memory. Development is simplified since there is no fixed division between program and data memory size as on some other devices.

The memory controller supports single-cycle data accesses from the C67x+ CPU to the RAM and ROM. Up to four simultaneous accesses are supported:

- Two 64-bit data accesses from the C67x+ CPU
- One 256-bit program fetch from the core and program cache
- One 32-bit data access from the peripheral system (dMAX)

The large (32K-byte) program cache translates to a high hit rate for most applications. This prevents most program/data access conflicts to the on-chip memory. It also enables effective program execution from an off-chip memory such as an SDRAM.

The ability to create an expandable system makes the DA707/B/DA787B an excellent choice for a DSP used in platform designs.

2.3 High-Performance Crossbar Switch

A high-performance crossbar switch acts as a central hub between the different bus masters (CPU, dMAX) and different targets (peripherals and memory).

Multiple transfers occur in parallel through the crossbar as long as there is no conflict between bus masters for a particular target. When a conflict does occur, the arbitration is a simple and deterministic fixed-priority scheme.

The dMAX is given highest priority since it is responsible for the most time-critical I/O transfers; it is followed by the CPU.

2.4 dMAX Dual Data Movement Accelerator

The dMAX is an extremely flexible data movement accelerator that supports audio-specific modes. It includes two accelerator sub-units (MAX0 and MAX1) that operate independently and simultaneously. The dMAX can be used for traditional data transfers such as memory-to-memory transfers and memory-to-peripheral transfers. It also can perform value-added functions by preprocessing data as it passes through the MAX units; for example, it can pack and unpack delay buffers on-the-fly to reduce memory usage. It also supports audio-specific addressing modes like circular addressing and non-sequential addressing. In particular, support for non-sequential addressing accelerates reverb by off-loading the normally inefficient random accesses from the CPU.

2.5 External Memory Interface (EMIF) for Flexibility and Expansion

The external memory interface on the DA707/B/DA787B supports a single bank of SDRAM and a single bank of asynchronous memory. The EMIF data width is 16 bits wide on the 144-pin RFP package.

SDRAM support includes x16 SDRAM devices with 1, 2, or 4 banks.

The DA707/B/DA787B DSP supports SDRAM devices up to 128M bits.

Asynchronous memory support is typically used to boot from a parallel non-multiplexed NOR flash device that can be 8 or 16 bits wide. Booting from larger flash devices than are natively supported by the dedicated EMIF address lines is accomplished by using general-purpose I/O pins for upper address lines.

The asynchronous memory interface can also be configured to support 8- or 16-bit-wide NAND flash. It includes a hardware ECC calculation (for single-bit errors) that can operate on blocks of data up to 512 bytes.

2.6 Multichannel Audio Serial Ports (McASP0, McASP1, and McASP2) - Up to 16 Stereo Channels I2S

The multichannel audio serial port (McASP) seamlessly interfaces to CODECs, DACs, ADCs, and other devices. It supports the ubiquitous IIS format as well as many variations of this format, including Time Division Multiplex (TDM) formats with up to 32 time slots.

Each McASP includes a transmit and receive section which may operate independently or synchronously; furthermore, each section includes its own flexible clock generator and extensive error-checking logic.

As data passes through the McASP, it can be realigned so that the fixed-point representation used by the application code can be independent of the representation used by the external devices without requiring any CPU overhead to make the conversion.

The McASP is a configurable module and supports between 2 and 16 serial data pins. It also has the option of supporting a Digital Interface Transmitter (DIT) mode with a full 384 bits of channel status and user data memory.

2.7 Inter-Integrated Circuit Serial Ports (I2C0, I2C1)

The DA707/B/DA787B includes two inter-integrated circuit (I2C) serial ports. A typical application is to configure one I2C serial port as a slave to an external user-interface microcontroller. The other I2C serial port may then be used by the DA707/B/DA787B DSP to control external peripheral devices, such as a CODEC or network controller, which are functionally peripherals of the DSP device.

The two I2C serial ports are pin-multiplexed with the SPI0 serial port.

2.8 Serial Peripheral Interface Ports (SPI0, SPI1)

As in the case of the I2C serial ports, the DA707/B/DA787B DSP also includes two serial peripheral interface (SPI) ports. This allows one SPI port to be configured as a slave to control the DSP while the other SPI serial port is used by the DSP to control external peripherals.

The SPI ports support a basic 3-pin mode as well as optional 4- and 5-pin modes. The optional pins include a slave chip-select pin and an enable pin which implements handshaking automatically in hardware for maximum SPI throughput.

The SPI0 port is pin-multiplexed with the two I2C serial ports (I2C0 and I2C1). The SPI1 serial port is pin-multiplexed with five of the serial data pins from McASP0 and McASP1.

2.9 Real-Time Interrupt Timer (RTI)

The real-time interrupt timer module includes:

- Two 32-bit counter/prescaler pairs
- Two input captures (tied to McASP DMA events for sample rate measurement)
- Four compares with automatic update capability
- Digital Watchdog (optional) for enhanced system robustness

2.10 Clock Generation (PLL and OSC)

The DA707/B/DA787B DSP includes an on-chip oscillator that supports crystals in the range of 12 MHz to 25 MHz. Alternatively, the clock can be provided externally through the CLKIN pin.

The DSP includes a flexible, software-programmable phase-locked loop (PLL) clock generator. Three different clock domains (SYSCLK1, SYSCLK2, and SYSCLK3) are generated by dividing down the PLL output. SYSCLK1 is the clock used by the CPU, memory controller, and memories. SYSCLK2 is used by the peripheral subsystem and dMAX. SYSCLK3 is used exclusively for the EMIF.

2.11 Security Features

The DA707/B/DA787B DSP incorporates several security features to protect the customer's IP. The CPU always boots directly from the ROM, all other boot modes are implemented as part of a software bootloader stored in the ROM.

In addition, the DSP can be special ordered with:

- The JTAG emulation port locked with a customer-specific key hardwired into the device
- Certain boot modes permanently disabled by hardwire.

For strongest security, the DSP can be ordered with a custom mask ROM.

2.12 DA7xx DSP Family

The DA707/B/DA787B DSP is a member of the DA7xx DSP family. A comparison of this device to other members in the DA7xx DSP family is shown in Table 2-1.

Table 2-1. DA7xx DSP Family Comparison Table

FEATURE	DA710/DA710B	DA708/DA708B	DA707/DA707B/ DA787B	DA705/DA705B
CPU	C67x+	C67x+	C67x+	C67x+
Frequency	300 MHz/300 MHz, 275 MHz	250 MHz/266 MHz	250 MHz	250 MHz
Frequency – Automotive Grade	250 MHz/275 MHz	250 MHz	250 MHz	250 MHz
RAM	256K Bytes	256K Bytes	192K Bytes	192K Bytes
ROM	768K Bytes	768K Bytes	768K Bytes	768K Bytes
McASP Modules	3	3 (McASP2 is DIT Only)	3 (McASP2 is DIT Only)	3 (McASP2 is DIT Only)
McASP Data Pins	16	16	16	16
SPI	2 With 3-, 4-, 5-Pin Options	2 With 3-, 4-, 5-Pin Options	2 With 3-, 4-, 5-Pin Options	2 With 3-, 4-, 5-Pin Options
I2C	2	2	2	2
dMAX	1	1	1	1
EMIF	32-Bit, 100 MHz/133 MHz	16-Bit, 100 MHz/133 MHz	16-Bit, 100 MHz	–
UHPI	1 32-Bit	–	–	–
Oscillator	1	1	1	1
Core Voltage	1.14 V to 1.32 V	1.14 V to 1.32 V	1.14 V to 1.32 V	1.14 V to 1.32 V
I/O Voltage	3.13 V to 3.47 V	3.13 V to 3.47 V	3.13 V to 3.47 V	3.13 V to 3.47 V
Junction Temperature Range	0°C to 95°C	0°C to 95°C	0°C to 95°C	0°C to 95°C
Junction Temperature Range – Automotive Grade	–40°C to 110°C	–40°C to 110°C	–40°C to 110°C	–40°C to 110°C
Product Status:(1) Product Preview (PP) Advance Information (AI) Production Data (PD)	DA710: PD DA710B: PD	DA708: PD DA708B: PD	DA707: PD DA707B: PD DA787B: PD	DA705: PD DA705B: PD
		Pinout and Package Compatible		
	Software-Compatible			

(1) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.
ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.
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2.13 Pin Maps

Figure 2-2 shows the pin assignments on the 144-pin RFP package.

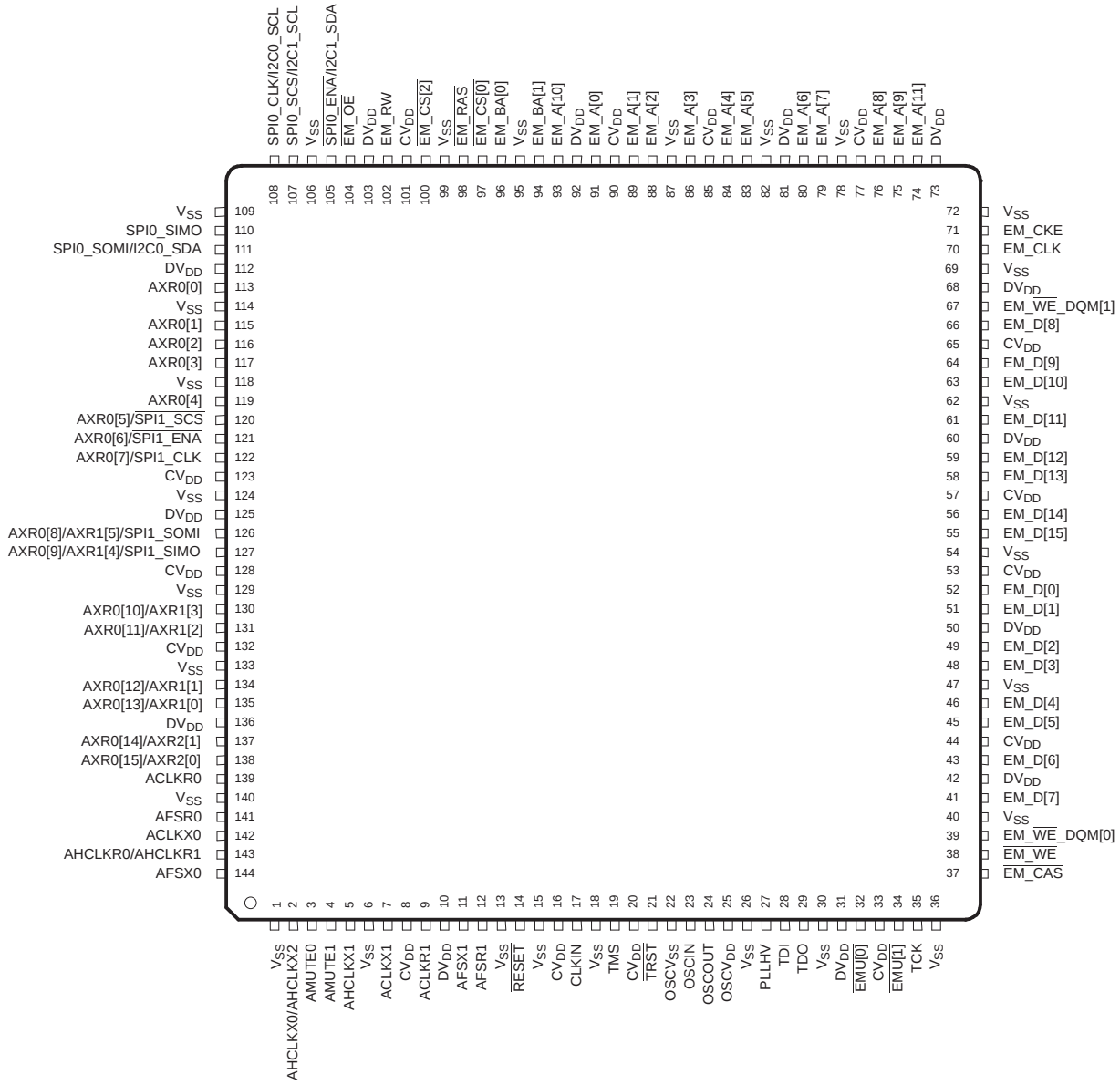


Figure 2-2. 144-Pin Low-Profile Quad Flatpack (RFP Suffix)—Top View

2.14 Terminal Functions

Table 2-2, the Terminal Functions table, identifies the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin type (I, O, IO, OZ, or PWR), whether the pin/ball has any internal pullup/pulldown resistors, whether the pin/ball is configurable as an IO in GPIO mode, and a functional pin description.

Table 2-2. Terminal Functions

SIGNAL NAME	PIN NO.	TYPE(1)	PULL(2)	GPIO(3)	DESCRIPTION
External Memory Interface (EMIF) Address and Control					
EM_A[0]	91	O	-	N	EMIF Address Bus
EM_A[1]	89	O	-	N	
EM_A[2]	88	O	-	N	
EM_A[3]	86	O	-	N	
EM_A[4]	84	O	-	N	
EM_A[5]	83	O	-	N	
EM_A[6]	80	O	-	N	
EM_A[7]	79	O	-	N	
EM_A[8]	76	O	-	N	
EM_A[9]	75	O	-	N	
EM_A[10]	93	O	-	N	
EM_A[11]	74	O	-	N	
EM_BA[0]	96	O	-	N	SDRAM Bank Address and Asynchronous Memory Low-Order Address
EM_BA[1]	94	O	-	N	
$\overline{\text{EM\_CS[0]}}$	97	O	-	N	SDRAM Chip Select
$\overline{\text{EM\_CS[2]}}$	100	O	-	N	Asynchronous Memory Chip Select
$\overline{\text{EM\_CAS}}$	37	O	-	N	SDRAM Column Address Strobe
$\overline{\text{EM\_RAS}}$	98	O	-	N	SDRAM Row Address Strobe
$\overline{\text{EM\_WE}}$	38	O	-	N	SDRAM Write Enable
EM_CKE	71	O	-	N	SDRAM Clock Enable
EM_CLK	70	O	-	N	SDRAM Clock
EM_$\overline{\text{WE}}$_DQM[0]	39	O	-	N	Write Enable or Byte Enable for EM_D[7:0]
EM_$\overline{\text{WE}}$_DQM[1]	67	O	-	N	Write Enable or Byte Enable for EM_D[15:8]
$\overline{\text{EM\_OE}}$	104	O	-	N	SDRAM Output Enable
EM_R$\overline{\text{W}}$	102	O	-	N	Asynchronous Memory Read/not Write

(1) TYPE column refers to pin direction in functional mode. If a pin has more than one function with different directions, the functions are separated with a slash (/).
(2) PULL column:
IPD = Internal Pulldown resistor
IPU = Internal Pullup resistor
(3) If the GPIO column is 'Y', then in GPIO mode, the pin is configurable as an IO unless otherwise marked.

Table 2-2. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	TYPE[1]	PULL[2]	GPIO[3]	DESCRIPTION
External Memory Interface (EMIF) Data Bus					
EM_D[0]	52	IO	-	N	EMIF Data Bus [Lower 16 Bits]
EM_D[1]	51	IO	-	N	
EM_D[2]	49	IO	-	N	
EM_D[3]	48	IO	-	N	
EM_D[4]	46	IO	-	N	
EM_D[5]	45	IO	-	N	
EM_D[6]	43	IO	-	N	
EM_D[7]	41	IO	-	N	
EM_D[8]	66	IO	-	N	
EM_D[9]	64	IO	-	N	
EM_D[10]	63	IO	-	N	
EM_D[11]	61	IO	-	N	
EM_D[12]	59	IO	-	N	
EM_D[13]	58	IO	-	N	
EM_D[14]	56	IO	-	N	
EM_D[15]	55	IO	-	N	

Table 2-2. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	TYPE[1]	PULL[2]	GPIO[3]	DESCRIPTION
McASP0, McASP1, McASP2, and SPI1 Serial Ports					
AHCLKR0/AHCLKR1	143	IO	-	Y	McASP0 and McASP1 Receive Master Clock
ACLKR0	139	IO	-	Y	McASP0 Receive Bit Clock
AFSR0	141	IO	-	Y	McASP0 Receive Frame Sync (L/R Clock)
AHCLKX0/AHCLKX2	2	IO	-	Y	McASP0 and McASP2 Transmit Master Clock
ACLKX0	142	IO	-	Y	McASP0 Transmit Bit Clock
AFSX0	144	IO	-	Y	McASP0 Transmit Frame Sync (L/R Clock)
AMUTE0	3	O	-	Y	McASP0 MUTE Output
AXR0[0]	113	IO	-	Y	McASP0 Serial Data 0
AXR0[1]	115	IO	-	Y	McASP0 Serial Data 1
AXR0[2]	116	IO	-	Y	McASP0 Serial Data 2
AXR0[3]	117	IO	-	Y	McASP0 Serial Data 3
AXR0[4]	119	IO	-	Y	McASP0 Serial Data 4
AXR0[5]/$\overline{\text{SPI1\_SCS}}$	120	IO	-	Y	McASP0 Serial Data 5 ***or*** SPI1 Slave Chip Select
AXR0[6]/$\overline{\text{SPI1\_ENA}}$	121	IO	-	Y	McASP0 Serial Data 6 ***or*** SPI1 Enable (Ready)
AXR0[7]/SPI1_CLK	122	IO	-	Y	McASP0 Serial Data 7 ***or*** SPI1 Serial Clock
AXR0[8]/AXR1[5]/ SPI1_SOMI	126	IO	-	Y	McASP0 Serial Data 8 ***or*** McASP1 Serial Data 5 ***or*** SPI1 Data Pin Slave Out Master In
AXR0[9]/AXR1[4]/ SPI1_SIMO	127	IO	-	Y	McASP0 Serial Data 9 ***or*** McASP1 Serial Data 4 ***or*** SPI1 Data Pin Slave In Master Out
AXR0[10]/AXR1[3]	130	IO	-	Y	McASP0 Serial Data 10 ***or*** McASP1 Serial Data 3
AXR0[11]/AXR1[2]	131	IO	-	Y	McASP0 Serial Data 11 ***or*** McASP1 Serial Data 2
AXR0[12]/AXR1[1]	134	IO	-	Y	McASP0 Serial Data 12 ***or*** McASP1 Serial Data 1
AXR0[13]/AXR1[0]	135	IO	-	Y	McASP0 Serial Data 13 ***or*** McASP1 Serial Data 0
AXR0[14]/AXR2[1]	137	IO	-	Y	McASP0 Serial Data 14 ***or*** McASP2 Serial Data 1
AXR0[15]/AXR2[0]	138	IO	-	Y	McASP0 Serial Data 15 ***or*** McASP2 Serial Data 0
ACLKR1	9	IO	-	Y	McASP1 Receive Bit Clock
AFSR1	12	IO	-	Y	McASP1 Receive Frame Sync (L/R Clock)
AHCLKX1	5	IO	-	Y	McASP1 Transmit Master Clock
ACLKX1	7	IO	-	Y	McASP1 Transmit Bit Clock
AFSX1	11	IO	-	Y	McASP1 Transmit Frame Sync (L/R Clock)
AMUTE1	4	O	-	Y	McASP1 MUTE Output
SPI0, I2C0, and I2C1 Serial Port Pins					
SPI0_SOMI/I2C0_SDA	111	IO	-	Y	SPI0 Data Pin Slave Out Master In ***or*** I2C0 Serial Data
SPI0_SIMO	110	IO	-	Y	SPI0 Data Pin Slave In Master Out
SPI0_CLK/I2C0_SCL	108	IO	-	Y	SPI0 Serial Clock ***or*** I2C0 Serial Clock
$\overline{\text{SPI0\_SCS}}$/I2C1_SCL	107	IO	-	Y	SPI0 Slave Chip Select ***or*** I2C1 Serial Clock
$\overline{\text{SPI0\_ENA}}$/I2C1_SDA	105	IO	-	Y	SPI0 Enable (Ready) ***or*** I2C1 Serial Data

Table 2-2. Terminal Functions (continued)

SIGNAL NAME	PIN NO.	TYPE[1]	PULL[2]	GPIO[3]	DESCRIPTION
Clocks					
OSCIN	23	I	-	N	1.2-V Oscillator Input
OSCOUT	24	O	-	N	1.2-V Oscillator Output
$OSCV_{DD}$	25	PWR	-	N	Oscillator 1.2-V V_{DD} tap point (for filter only)
$OSCV_{SS}$	22	PWR	-	N	Oscillator V_{SS} tap point (for filter only)
CLKIN	17	I	-	N	Alternate clock input (3.3-V LVCMOS Input)
PLLHV	27	PWR	-	N	PLL 3.3-V Supply Input (requires external filter)
Device Reset					
$\overline{\text{RESET}}$	14	I	-	N	Device reset pin
Emulation/JTAG Port					
TCK	35	I	IPU	N	Test Clock
TMS	19	I	IPU	N	Test Mode Select
TDI	28	I	IPU	N	Test Data In
TDO	29	OZ	IPU	N	Test Data Out
$\overline{\text{TRST}}$	21	I	IPD	N	Test Reset
$\overline{\text{EMU[0]}}$	32	IO	IPU	N	Emulation Pin 0
$\overline{\text{EMU[1]}}$	34	IO	IPU	N	Emulation Pin 1
Power Pins					
Core Supply (CV_{DD})	8, 16, 20, 33, 44, 53, 57, 65, 77, 85, 90, 101, 123, 128, 132				
IO Supply (DV_{DD})	10, 31, 42, 50, 60, 68, 73, 81, 92, 103, 112, 125, 136				
Ground (V_{SS})	1, 6, 13, 15, 18, 26, 30, 36, 40, 47, 54, 62, 69, 72, 78, 82, 87, 95, 99, 106, 109, 114, 118, 124, 129, 133, 140				

2.15 Device Block Diagram

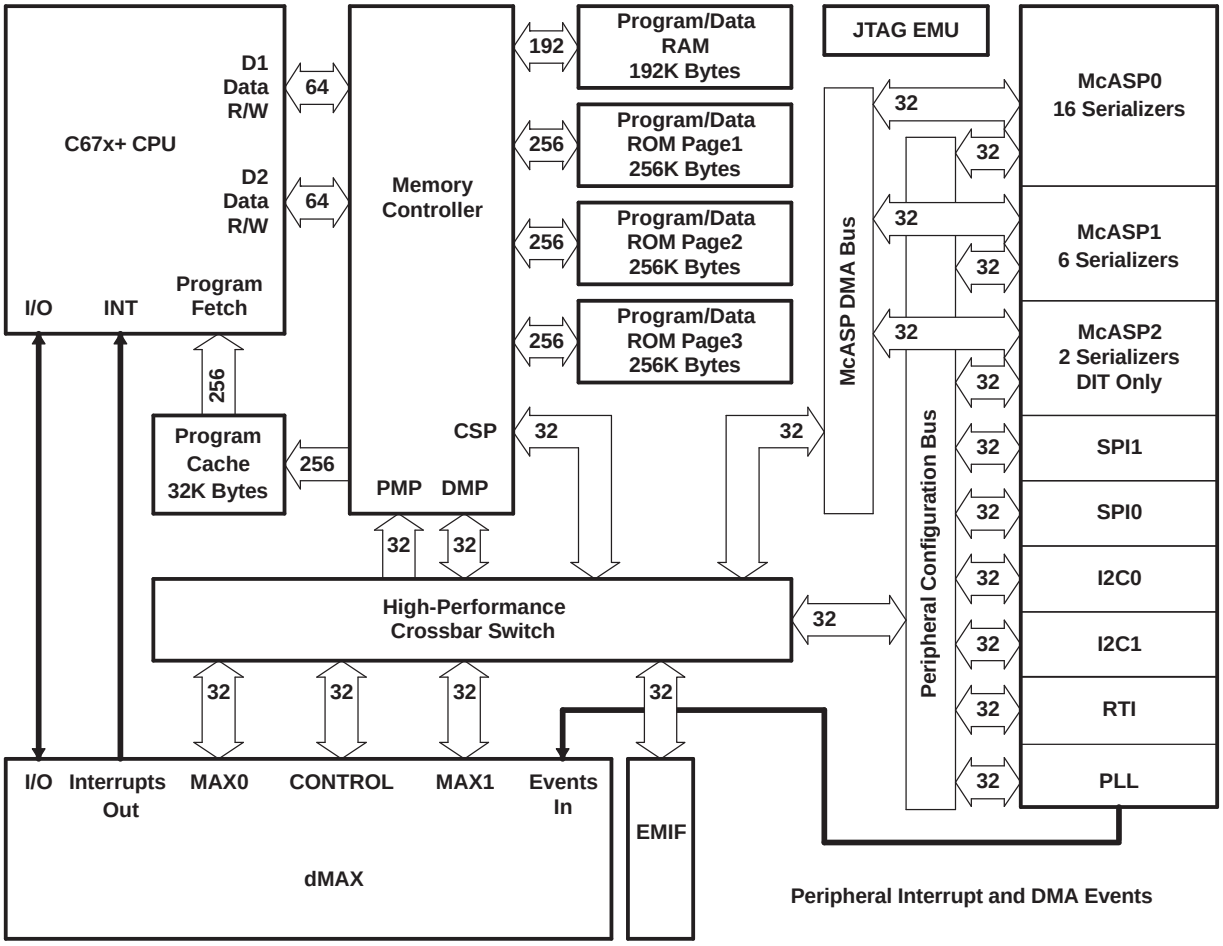


Figure 2-3. DA707/B/DA787B DSP Block Diagram

2.16 Device Description

The following sections describe each major functional block on the DA707/B/DA787B DSP.

2.16.1 Enhanced C67x+ CPU

The DA707/B/DA787B DSP is based on the C67x+ CPU core. This core is code-compatible with the C67x CPU core used on the DA610 DSP family, but with significant enhancements.

First, the C67x+ CPU core operating frequency has been increased to 250 MHz(1) while operating at 1.2 V. This is a significant increase from the 225 MHz maximum of DA610 at the same core voltage.

The register file sizes have *doubled* from 32 general-purpose registers on the DA610 DSP to 64 general-purpose registers on the DA707/B/DA787B family. These additional registers are of great use since they allow the optimizing C compiler to software-pipeline more complex loops by decreasing register pressure significantly. This results in higher performance for code which is recompiled for the DA707/B/DA787B DSP core.

On the DA707/B/DA787B DSP, execution packet spanning fetch packet boundaries is now supported. This provides a code size improvement over the DA610 DSP because it removes any inefficiency in how execution packets are packed into fetch packets.

New floating-point instructions have been added to the C67x CPU core which improve performance specifically during audio processing. These instructions new are listed in Table 2-3.

(1) CPU speed is device-dependent.

Table 2-3. New Floating-Point Instructions for C67x+ CPU

INSTRUCTION	FLOATING-POINT OPERATION(1)	IMPROVES
MPYSPDP	SP x DP → DP	Faster than MPYDP. Improves high Q biquads (bass management) and FFT.
MPYSP2DP	SP x SP → DP	Faster than MPYDP. Improves Long FIRs (EQ).
ADDSP (new to CPU “S” Unit)	SP + SP → SP	Now up to four floating-point add and subtract operations in parallel. Improves FFT performance and symmetric FIR.
ADDDP (new to CPU “S” Unit)	DP + DP → DP	
SUBSP (new to CPU “S” Unit)	SP – SP → SP	
SUBDP (new to CPU “S” Unit)	DP – DP → DP	

(1) SP means IEEE Single-Precision (32-bit) operations and DP means IEEE Double-Precision (64-bit) operations.

The CPU cross-path performance between side A and side B has been improved. The number of times the cross-path operand can be sourced in a single cycle has been increased from one to two. In addition, the cross-path register read(s) are not counted as part of the limit of four reads of the same register in a single cycle.

Finally, two new registers, which are dedicated to communication with the dMAX unit, have been added to the CPU. These registers are the dMAX Event Trigger Register (DETR) and the dMAX Event Status Register (DESR). They allow the CPU and dMAX to communicate without requiring any accesses to the memory system.

2.16.2 CPU Interrupt Assignments

Table 2-4 lists the interrupt channel assignments on the DA707/B/DA787B device. If more than one source is listed, the interrupt channel is shared and an interrupt on this channel could have come from any of the enabled peripherals on that channel.

Note that most peripheral interrupt and DMA events are routed first through the dMAX unit (see Table 3-2.)

After being processed, the dMAX unit can generate a CPU interrupt. This allows the dMAX to take a significant portion of the interrupt processing burden off of the CPU.

Table 2-4. CPU Interrupt Assignments

CPU INTERRUPT	INTERRUPT SOURCE
INT0	RESET
INT1	NMI (From dMAX)
INT2	Reserved
INT3	Reserved
INT4	RTI Interrupt 0
INT5	RTI Interrupt 1, 2, 3, and RTI Overflow Interrupt 0 and 1.
INT6	Reserved
INT7	dMAX Event 0
INT8	dMAX Event 1
INT9	dMAX Event 2
INT10	dMAX Event 3
INT11	dMAX Event 4
INT12	dMAX Event 5
INT13	dMAX Event 6
INT14	I2C0, I2C1, SPI0, SPI1 Interrupts
INT15	dMAX Event 7

2.16.3 Internal Program/Data ROM and RAM

The organization of program/data ROM and RAM on DA707/B/DA787B is simple and efficient. ROM is organized as three 256-bit-wide pages with four 64-bit-wide banks. RAM is organized as a single 256-bit-wide page with eight 32-bit-wide banks.

The internal memory organization is illustrated in Figure 2-4 (ROM) and Figure 2-5 (RAM).

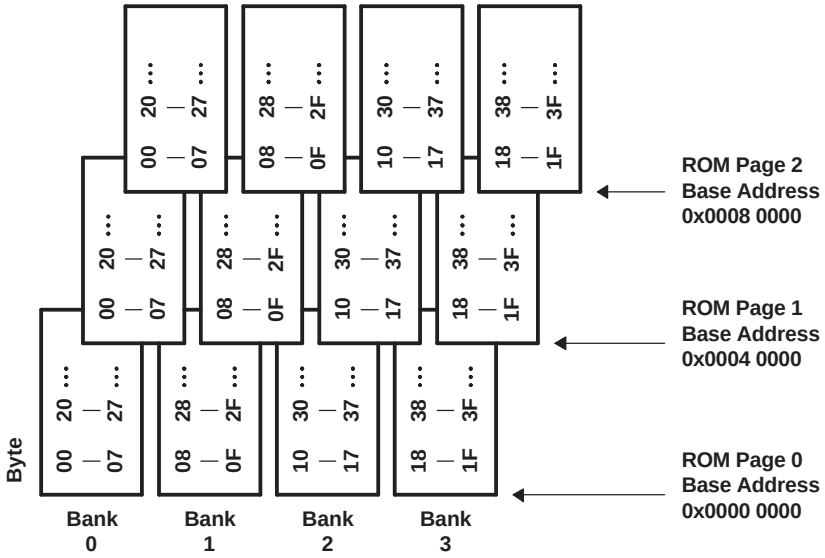


Figure 2-4. Program/Data ROM Organization

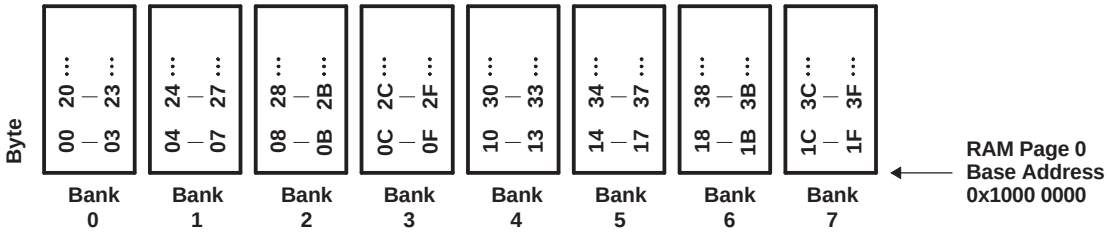


Figure 2-5. Program/Data RAM Organization

The DA707/B/DA787B memory controller supports up to four parallel accesses to the internal RAM and ROM as long as there are no bank conflicts:

- Two 64-bit data accesses from the C67x+ CPU
- One 256-bit-wide program fetch from the program cache
- One 32-bit data access from the peripheral system (dMAX)

A program cache miss is 256 bits wide and conflicts only with data accesses to the same page. Multiple data accesses to different pages, or to the same page but different banks will occur without conflict.

The organization of the DA707/B/DA787B internal memory system into multiple pages (4 total) and a large number of banks (20 total) means that it is straightforward to optimize DSP code to avoid data conflicts. Several factors, including the large program cache and the partitioning of the memory system into multiple pages, minimize the number of program versus data conflicts.

The result is an efficient memory system which allows easy tuning towards the maximum possible CPU performance.

2.16.4 Program Cache

The DA707/B/DA787B DSP executes code directly from a large on-chip 32K-byte program cache. The program cache has these key features:

- Wide 256-bit path to internal ROM/RAM
- Single-cycle access on cache hits
- 2-cycle miss penalty to internal ROM/RAM
- Caches external memory as well as ROM/RAM
- Direct-mapped
- Modes: Enable, Freeze, Bypass
- Software invalidate to support code overlay

The program cache line size is 256 bits wide and is matched with a 256-bit-wide path between cache and internal memory. This allows the program cache to fill an entire line (corresponding to eight C67x+ CPU instructions) with only a single miss penalty of 2 cycles.

The program cache control registers are listed in Table 2-5.

Table 2-5. Program Cache Control Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x2000 0000	L1PISAR	L1P Invalidate Start Address
0x2000 0004	L1PICR	L1P Invalidate Control Register

CAUTION

Any application which modifies the contents of program RAM (for example, a program overlay) must invalidate the addresses from program cache to maintain coherency by explicitly writing to the L1PISAR and L1PICR registers.

The Cache Mode (Enable, Freeze, Bypass) is configured through a CPU internal register (CSR, bits 7:5). These options are listed in Table 2-6. Typically, only the Cache Enable Mode is used. But advanced users may utilize Freeze and Bypass modes to tune performance.

Table 2-6. Cache Modes Set Through PCC Field of CSR CPU Register on DA707/B/DA787B

CPU CSR[7:5]	CACHE MODE
000b	Enable (Deprecated - Means direct mapped RAM on some C6000 devices)
010b	Enable - Cache is enabled, cache misses cause a line fill.
011b	Freeze - Cache is enabled, but contents are unchanged by misses.
100b	Bypass - Forces cache misses, cache contents frozen.
Other Values	Reserved - Not Supported

CAUTION

Although the reset value of CSR[7:5] (PCC field) is 000b, the value may be modified during the boot process by the ROM code. Refer to the appropriate ROM data sheet for more details. However, note that the cache may be disabled when control is actually passed to application code. Therefore, it may be necessary to write '010b' to the PCC field to explicitly enable the cache at the start of application code.

CAUTION

Changing the cache mode through CSR[7:5] does not invalidate any lines already in the cache. To invalidate the cache after modifications are made to program space, the control registers L1PISAR and L1PICR must be used.

2.16.5 High-Performance Crossbar Switch

The DA707/B/DA787B DSP includes a high-performance crossbar switch that acts as a central hub between bus masters and targets. Figure 2-6 illustrates the connectivity of the crossbar switch.

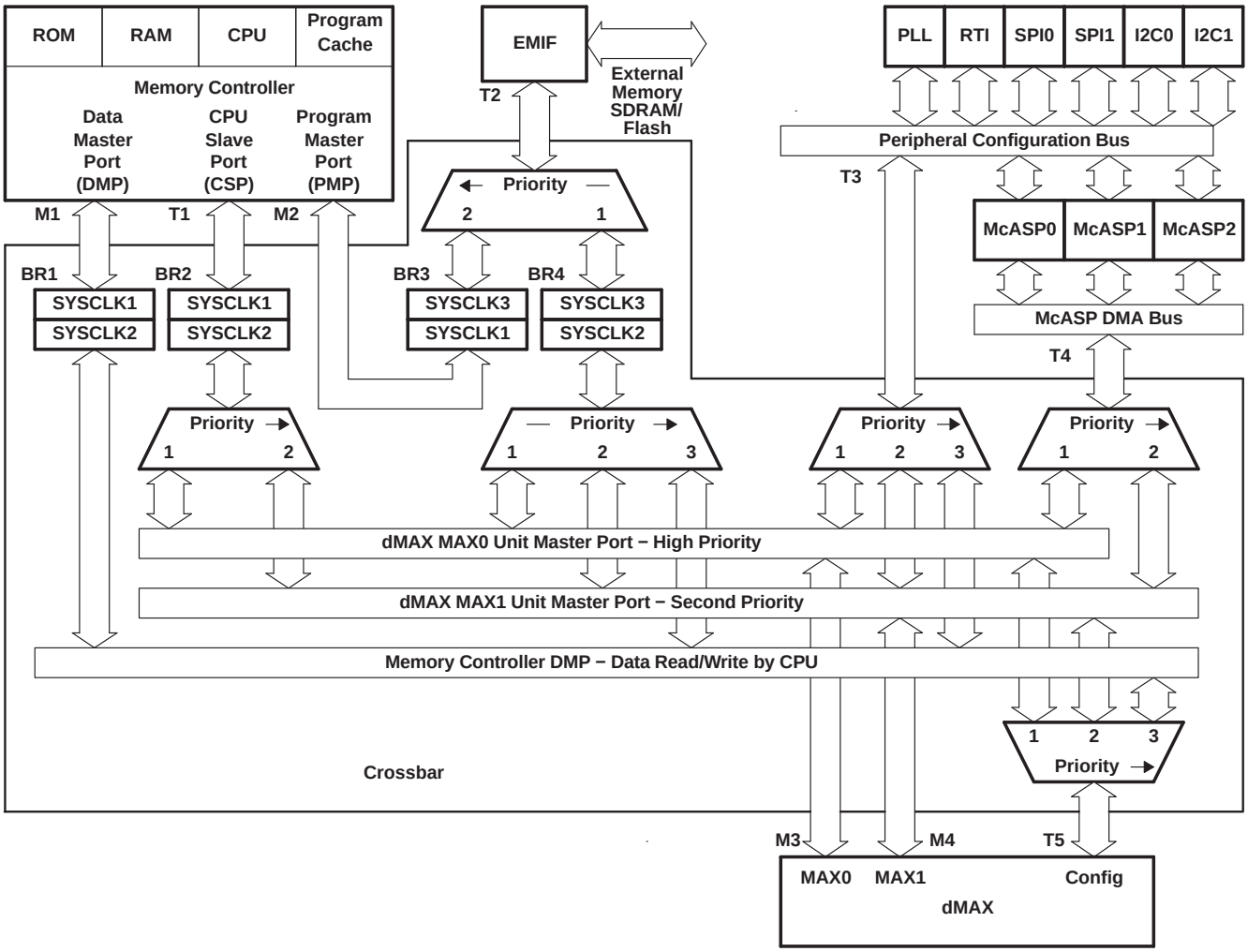


Figure 2-6. Block Diagram of Crossbar Switch

As shown in Figure 2-6, there are four bus masters:

M1	Memory controller DMP for CPU data accesses to peripherals and EMIF.
M2	Memory controller PMP for program cache fills from the EMIF.
M3	dMAX MAX0 master port for high-priority DMA accesses.
M4	dMAX MAX1 master port for lower-priority DMA accesses.

The four bus masters arbitrate for five different target groups:

T1	On-chip memories through the CPU Slave Port (CSP).
T2	Memories on the external memory interface (EMIF).
T3	Peripheral registers through the peripheral configuration bus.
T4	McASP serializers through the dedicated McASP DMA bus.
T5	dMAX configuration memories and registers.

The crossbar switch supports parallel accesses from different bus masters to different targets. When two or more bus masters contend for the same target beginning at the same cycle, then the highest-priority master is given ownership of the target while the other master(s) are stalled. However, once ownership of the target is given to a bus master, it is allowed to complete its access before ownership is arbitrated again. Following are two examples.

Example 1: Simultaneous accesses without conflict

- dMAX MAX0 accesses McASP Data Port for transfer of audio data.
- dMAX MAX1 accesses SPI port for control processing.
- CPU fills program cache from EMIF.

Example 2: Conflict over a shared resource

- dMAX MAX0 accesses RTI port for McASP sample rate measurement.
- dMAX MAX1 accesses SPI port for control processing.

In Example 2, both masters contend for the same target, the peripheral configuration bus. The MAX0 access will be given priority over the MAX1 access.

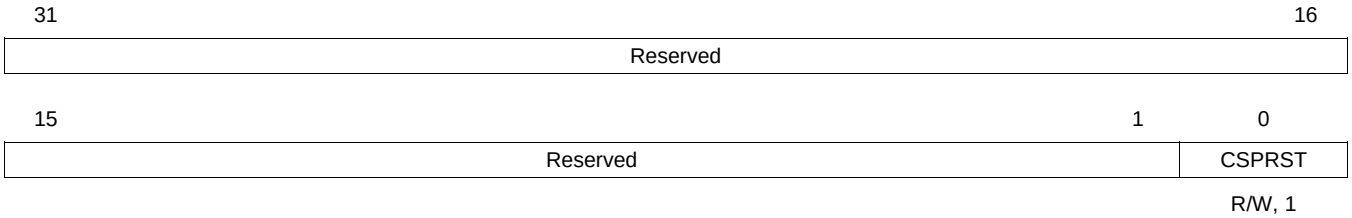
The master priority is illustrated in Figure 2-6 by the numbers 1 through 3 in the bus arbiter symbols. Note that the EMIF arbitration is distributed so that only one bridge crossing is necessary for PMP accesses. The effect is that PMP has 4th priority to the EMIF but lower latency.

A bus bridge is needed between masters and targets which run at different clock rates. The bus bridge contains a small FIFO to allow the bridge to accept an incoming (burst) access at one clock rate and pass it through the bridge to a target running at a different rate. Table 2-7 lists the FIFO properties of the four bridges (BR1, BR2, BR3, and BR4) in Figure 2-6.

Table 2-7. Bus Bridges

LABEL	BRIDGE DESCRIPTION	MASTER CLOCK	TARGET CLOCK
BR1	DMP Bridge to peripherals, dMAX, EMIF	SYSCLK1	SYSCLK2
BR2	dMAX to ROM/RAM (CSP)	SYSCLK2	SYSCLK1
BR3	PMP to EMIF	SYSCLK1	SYSCLK3
BR4	CPU and dMAX to EMIF	SYSCLK2	SYSCLK3

Figure 2-7 shows the bit layout of the device-level bridge control register (CFGBRIDGE) and Table 2-8 contains a description of the bits.



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 2-7. CFGBRIDGE Register Bit Layout (0x4000 0024)

Table 2-8. CFGBRIDGE Register Bit Field Description (0x4000 0024)

BIT NO.	NAME	RESET VALUE	READ WRITE	DESCRIPTION
31:1	Reserved	N/A	N/A	Reads are indeterminate. Only 0s should be written to these bits.
0	CSPRST	1	R/W	Resets the CSP Bridge (BR2 in Figure 2-6). 1 = Bridge Reset Asserted 0 = Bridge Reset Released

CAUTION

The CSPRST bit must be asserted after any change to the PLL that affects SYSCLK1 and SYSCLK2 and must be released before any accesses to the CSP bridge occur from the dMAX.

2.17 Device Memory Map

A high-level memory map of the DA707/B/DA787B DSP appears in Table 2-9. The base address of each region is listed. ***Any address past the end address must not be read or written.*** The table also lists whether the regions are word-addressable or byte- and word-addressable.

Table 2-9. DA707/B/DA787B Memory Map

DESCRIPTION	BASE ADDRESS	END ADDRESS	BYTE- OR WORD-ADDRESSABLE
Internal ROM Page 0 (256K Bytes)	0x0000 0000	0x0003 FFFF	Byte and Word
Internal ROM Page 1 (256K Bytes)	0x0004 0000	0x0007 FFFF	Byte and Word
Internal ROM Page 2 (256K Bytes)	0x0008 0000	0x000B FFFF	Byte and Word
Internal RAM Page 0 (192K Bytes)	0x1000 0000	0x1002 FFFF	Byte and Word
Memory and Cache Control Registers	0x2000 0000	0x2000 001F	Word Only
Emulation Control Registers (Do Not Access)	0x3000 0000	0x3FFF FFFF	Word Only
Device Configuration Registers	0x4000 0000	0x4000 0083	Word Only
PLL Control Registers	0x4100 0000	0x4100 015F	Word Only
Real-time Interrupt (RTI) Control Registers	0x4200 0000	0x4200 00A3	Word Only
Reserved	0x4300 0000	0x4300 0043	
McASP0 Control Registers	0x4400 0000	0x4400 02BF	Word Only
McASP1 Control Registers	0x4500 0000	0x4500 02BF	Word Only
McASP2 Control Registers	0x4600 0000	0x4600 02BF	Word Only
SPI0 Control Registers	0x4700 0000	0x4700 007F	Word Only
SPI1 Control Registers	0x4800 0000	0x4800 007F	Word Only
I2C0 Control Registers	0x4900 0000	0x4900 007F	Word Only
I2C1 Control Registers	0x4A00 0000	0x4A00 007F	Word Only
McASP0 DMA Port (any address in this range)	0x5400 0000	0x54FF FFFF	Word Only
McASP1 DMA Port (any address in this range)	0x5500 0000	0x55FF FFFF	Word Only
McASP2 DMA Port (any address in this range)	0x5600 0000	0x56FF FFFF	Word Only
dMAX Control Registers	0x6000 0000	0x6000 008F	Word Only
dMAX MAX0 Configuration Memory (4K Bytes)	0x6100 0000	0x6100 0FFF	Word Only
dMAX MAX0 Dual-Port Data Memory (512 Bytes)	0x6100 8000	0x6100 81FF	Byte and Word
dMAX MAX1 Configuration Memory (4K Bytes)	0x6200 0000	0x6200 0FFF	Word Only
dMAX MAX1 Dual-Port Data Memory (512 Bytes)	0x6200 8000	0x6200 81FF	Byte and Word
External SDRAM space on EMIF	0x8000 0000	0x8FFF FFFF	Byte and Word
External Asynchronous / Flash space on EMIF	0x9000 0000	0x9FFF FFFF	Byte and Word
EMIF Control Registers	0xF000 0000	0xF000 00BF	Word Only(1)

(1) The upper byte of the EMIF's SDRAM Configuration Register (SDCR[31:24]) is byte-addressable to support placing the EMIF into the Self-Refresh State without triggering the SDRAM Initialization Sequence.

3 Peripheral and Electrical Specifications

3.1 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320DA707/B/TMS320DA787B (DA707/B/DA787B) DSP.

All electrical and switching characteristics in this data manual are valid over the recommended operating conditions unless otherwise specified.

3.2 Absolute Maximum Ratings(1)(2)

Over Operating Junction Temperature Range (Unless Otherwise Noted)

			UNIT
Supply voltage range, CV_{DD}, $OSCV_{DD}$(3)		–0.3 to 1.8	V
Supply voltage range, DV_{DD} , PLLHV		–0.3 to 4	V
Input Voltage Range	All pins except OSCIN	–0.3 to DV_{DD} + 0.5	V
	OSCIN pin	–0.3 to CV_{DD} + 0.5	
Output Voltage Range	All pins except OSCOUT	–0.3 to DV_{DD} + 0.5	V
	OSCOUT pin	–0.3 to CV_{DD} + 0.5	
Clamp Current		±20	mA
Operating junction temperature range T_J	Commercial Grade	0 to 95	°C
	Automotive Grade (A Suffix)	–40 to 110	
Storage temperature range, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with referenced to V_{SS} unless otherwise specified.
(3) If $OSCV_{DD}$ and $OSCV_{SS}$ pins are used as filter pins for reduced oscillator jitter, they should not be connected to CV_{DD} and V_{SS} externally.

3.3 Recommended Operating Conditions(1)

			MIN	NOM	MAX	UNIT
CV_{DD}	Core Supply Voltage		1.14	1.2	1.32	V
DV_{DD}	I/O Supply Voltage		3.13	3.3	3.47	V
T_A	Operating Ambient Temperature Range	Commercial Grade	0		70	°C
		Automotive Grade (A Suffix)	–40		85	

(1) All voltage values are with referenced to V_{SS} unless otherwise specified.

3.4 Electrical Characteristics

Over Operating Junction Temperature Range (Unless Otherwise Noted)

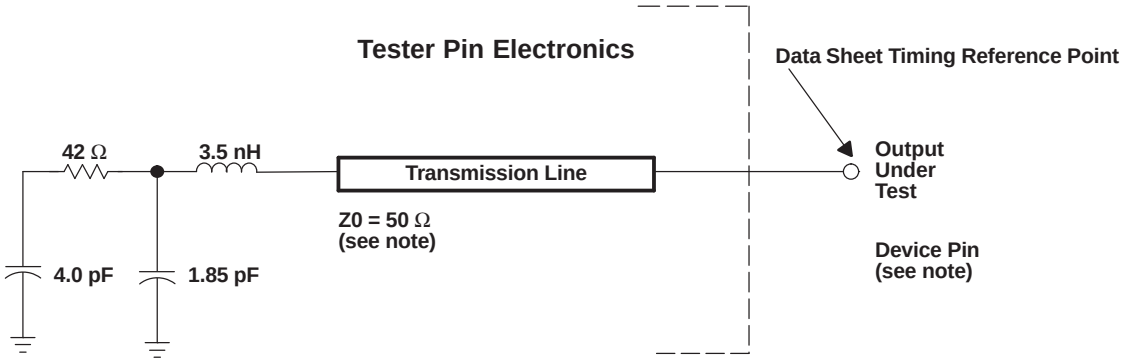
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage	I_O = –100 µA	DV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 100 µA			0.2	V
I_{OH}	High-Level Output Current	V_O = 0.8 DV_{DD}			–8	mA
I_{OL}	Low-Level Output Current	V_O = 0.22 DV_{DD}			8	mA
V_{IH}	High-Level Input Voltage		2		DV_{DD}	V
V_{IL}	Low-Level Input Voltage		0		0.8	V
V_{HYS}	Input Hysterisis			0.13 DV_{DD}		V
I_I, I_{OZ}	Input Current and Off State Output Current	Pins without pullup or pulldown			±10	µA
		Pins with internal pullup	–50		–170	
		Pins with internal pulldown	50		170	
t_{tr}	Input Transition Time				25	ns
C_I	Input Capacitance				7	pF
C_O	Output Capacitance				7	pF
I_{DD2V} (CV_{DD} Supply)	Peak Current(1)	CV_{DD} = 1.26 V, T_J = 95 °C, SYSCLK1 = 250 MHz, SYSCLK2 = 125 MHz, SYSCLK3 = 100 MHz		850		mA
		CV_{DD} = 1.26 V, T_J = 110 °C, SYSCLK1 = 250 MHz, SYSCLK2 = 125 MHz, SYSCLK3 = 100 MHz		950		
	Typical Average Current,(2) Performance Audio Application	CV_{DD} = 1.26 V, T_J = 95 °C, SYSCLK1 = 250 MHz, SYSCLK2 = 125 MHz, SYSCLK3 = 100 MHz		600		mA
		CV_{DD} = 1.26 V, T_J = 110 °C, SYSCLK1 = 250 MHz, SYSCLK2 = 125 MHz, SYSCLK3 = 100 MHz		700		
	Clocks Disabled Input Current on CV_{DD} Supply	CV_{DD} = 1.26 V, T_J = 95 °C			270	mA
		CV_{DD} = 1.26 V, T_J = 110 °C			370	
I_{DD3V} (DV_{DD} Supply)	Typical Average Current, Performance Audio Application	DV_{DD} = 3.3 V, SYSCLK1 = 250 MHz, SYSCLK2 = 125 MHz, SYSCLK3 = 100 MHz		40		mA

(1) Peak Current is measured using a high-activity test case and is representative of the typical high current transient response for which the DSP power supply should be designed.

(2) This number represents an estimate of the worst-case time-average power dissipation for the purpose of thermal budgeting. The number is based upon Texas Instruments PA/F based A/V receiver application software. This number is application-dependent so it should be measured in system running the final application code.

3.5 Parameter Information

3.5.1 Parameter Information Device-Specific Information



A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not neccessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 3-1. Test Load Circuit for AC Timing Measurements

3.5.1.1 Signal Transition Levels

All input and output timing parameters are referenced to 1.5 V for both "0" and "1" logic levels.

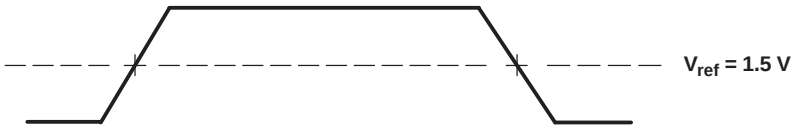


Figure 3-2. Input and Output Voltage Reference Levels for AC Timing Measurements

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

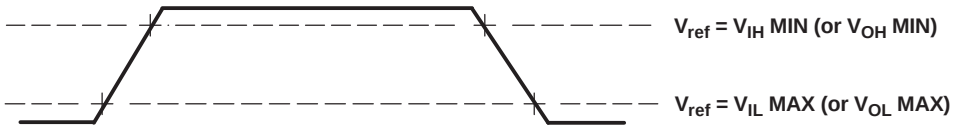


Figure 3-3. Rise and Fall Transition Time Voltage Reference Levels

3.5.1.2 Signal Transition Rates

All timings are tested with an input edge rate of 4 Volts per nanosecond (4 V/ns).

3.6 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
dis	disable time	Z	High impedance
en	enable time		
f	fall time		
h	hold time		
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		
X	Unknown, changing, or don't care level		

3.7 Power Supply Sequencing

This device does not require specific power-up sequencing between the DV_{DD} and CV_{DD} voltage rails; however, there are some considerations that the system designer should take into account:

1. Neither supply should be powered up for an extended period of time (>1 second) while the other supply is powered down.
2. The I/O buffers powered from the DV_{DD} rail also require the CV_{DD} rail to be powered up in order to be controlled; therefore, an I/O pin that is supposed to be 3-stated by default may actually drive momentarily until the CV_{DD} rail has powered up. Systems should be evaluated to determine if there is a possibility for contention that needs to be addressed. In most systems where both the DV_{DD} and CV_{DD} supplies ramp together, as long as CV_{DD} tracks DV_{DD} closely, any contention is also mitigated by the fact that the CV_{DD} rail would reach its specified operating range well before the DV_{DD} rail has fully ramped.

3.8 Reset

3.8.1 Reset Electrical Data/Timing

Table 3-1 assumes testing over recommended operating conditions.

Table 3-1. Reset Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{w(RSTL)}$	Pulse width, $\overline{\text{RESET}}$ low	100		ns
2	$t_{su(BPV-RSTH)}$	Setup time, boot pins valid before $\overline{\text{RESET}}$ high	20		ns
3	$t_{h(RSTH-BPV)}$	Hold time, boot pins valid after $\overline{\text{RESET}}$ high	20		ns

3.9 dMAX Data Movement Accelerator

The DA707/B/DA787B DSP includes an accelerated Data Movement subsystem called dMAX. This unit consists of two configurable bus masters, MAX0 and MAX1. MAX0 has higher priority than MAX1. The MAX units operate independently at the SYSCLK2 clock rate.

Like a traditional DMA engine, each MAX unit can transfer data from memory to memory, from memory to peripheral, and from peripheral to memory. Also the MAX units can perform advanced transfer operations such as those involving circular addressing modes.

Even more complex memory access patterns can be performed by the MAX units without any CPU intervention. For example, MAX units support fetching a group of samples from different taps in a delay line even if the taps are not uniformly spaced. The MAX units are even capable of handling dynamically changing tap locations from event to event.

In addition, the MAX units can perform some preprocessing of the data during a transfer. One example of this type of preprocessing is packing and unpacking 24-bit samples into 32-bit words in memory. Another example is converting data between a reduced precision 16-bit for storage and standard 32- or 64-bit floating-point formats for CPU processing.

As Figure 3-4 illustrates, each MAX unit has its own configuration memory. Texas Instruments provides configuration images for the dMAX unit which can be loaded during device initialization to configure the MAX units to perform various functions.

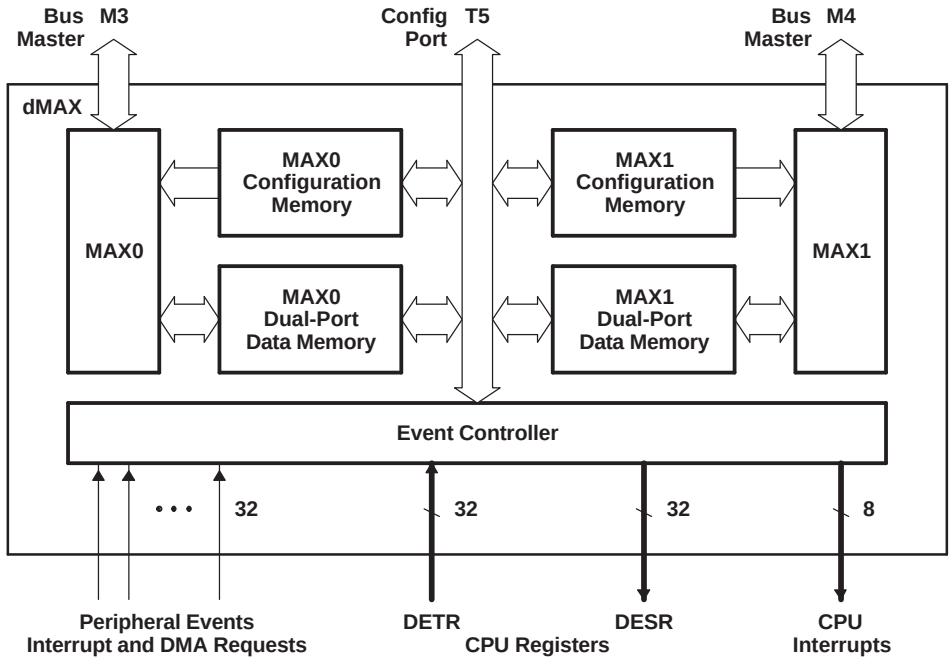


Figure 3-4. dMAX Accelerator Block Diagram

Each MAX unit also has its own dual-port data memory that is generally used to pass parameters between the CPU and dMAX at run time.

The dMAX unit includes an event controller which takes in up to 32 different events (interrupt and DMA requests) from the DA707/B/DA787B peripherals. Each event input can be enabled or disabled and assigned to one of the two MAX units on an event-by-event basis. The event controller also provides two hardware priority encoders to assist the MAX units in servicing the highest-priority events first. The assignment of these events is described in Table 3-2.

The dMAX also includes direct links to the CPU on chip. It can assert up to eight different CPU interrupts. In addition, it has direct connections to the CPU internal DETR and DESR registers for extremely fast signalling.

Table 3-2. dMAX Peripheral Event Input Assignments

dMAX EVENT INPUT	EVENT SOURCE
0	DETR[0] (CPU Register Bit)
1	DETR[16] (CPU Register Bit)
2	RTI DMA Request 0
3	RTI DMA Request 1
4	McASP0 Transmit DMA Request
5	McASP0 Receive DMA Request
6	McASP1 Transmit DMA Request
7	McASP1 Receive DMA Request
8	McASP2 Transmit DMA Request
9	McASP2 Receive DMA Request
10	DETR[1] (CPU Register Bit)
11	DETR[17] (CPU Register Bit)
12	Reserved
13	SPI0 DMA Request (Transmit and Receive)
14	SPI1 DMA Request (Transmit and Receive)
15	RTI DMA Request 2
16	RTI DMA Request 3
17	DETR[2] (CPU Register Bit)
18	DETR[18] (CPU Register Bit)
19	I2C0 Transmit DMA Event
20	I2C0 Receive DMA Event
21	I2C1 Transmit DMA Event
22	I2C1 Receive DMA Event
23	DETR[3] (CPU Register Bit)
24	DETR[19] (CPU Register Bit)
25	reserved
26	McASP0 Error Interrupts (AMUTEIN0, Transmit, and Receive)
27	McASP1 Error Interrupts (AMUTEIN1, Transmit, and Receive)
28	McASP2 Error Interrupts (AMUTEIN2, Transmit, and Receive)
29	RTI Overflow Interrupts (OVLREQ0 and OVLREQ1)
30	DETR[20] (CPU Register Bit)
31	DETR[21] (CPU Register Bit)

3.9.1 dMAX Peripheral Registers Description(s)

Table 3-3 is a list of the dMAX registers.

Table 3-3. dMAX Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x6000 0008	DEPR	Event Polarity Register
0x6000 000C	DEER	Event Enable Register
0x6000 0010	DEDR	Event Disable Register
0x6000 0014	DEHPR	Event High Priority Register
0x6000 0018	DELPR	Event Low Priority Register
0x6000 001C	DEFR	Event Flag Register
0x6000 0034	DER0	Event Register 0
0x6000 0054	DER1	Event Register 1
0x6000 0074	DER2	Event Register 2
0x6000 0094	DER3	Event Register 3
0x6000 0040	DFSR0	FIFO Status Register 0
0x6000 0060	DFSR1	FIFO Status Register 1
0x6000 0080	DTCR0	Transfer Complete Register 0
0x6000 00A0	DTCR1	Transfer Complete Register 1
N/A	DETR	Event Trigger Register (Located in C67x+ DSP Register File)
N/A	DESR	Event Status Register (Located in C67x+ DSP Register File)

3.10 External Interrupts

The DA707/B/DA787B DSP supports two categories of external interrupts:

1. External interrupts with dedicated edge-detect hardware.
2. External interrupts implemented by dMAX polling.

The AMUTEIN0, AMUTEIN1, and AMUTEIN2 external interrupts make up the first category of external edge-sensitive interrupts. The interrupt signal should remain asserted for at least two SYSCLK2 cycles to ensure that the edge is detected by the dMAX. The dMAX can then be configured to act on these interrupts and/or pass them on to the DSP CPU. There are six pins from which three can be chosen to map to the AMUTEIN0, AMUTEIN1, and AMUTEIN2 interrupts. These pins are listed in the CFGMCASP0, CFGMCASP1, and CFGMCASP2 register descriptions (see Table 3-11, Table 3-12, and Table 3-13, respectively).

The AMUTEIN0, AMUTEIN1, and AMUTEIN2 inputs can be used in parallel by both the dMAX (for interrupt purposes) and the McASP serial ports as an input to the AMUTE logic. Also, the edge polarity for interrupt generation is configurable through dMAX control registers. Independently, the McASP registers control the polarity of the level-sensitive McASP AMUTE input.

The second category is implemented by configuring the dMAX to periodically poll a pin and trigger an interrupt when this pin changes state. The pin can be any pin configurable as general-purpose I/O. The pin must remain asserted long enough for the dMAX to capture the change in state. The exact time is dependent upon the specific dMAX configuration and the load on the dMAX due to other tasks. However, a typical case may require the external interrupt to be asserted for a minimum of 10 µs.

3.11 External Memory Interface (EMIF)

3.11.1 EMIF Device-Specific Information

The DA707/B/DA787B DSP includes an external memory interface (EMIF) for optional SDRAM, NOR FLASH, NAND FLASH, or SRAM. The key features of this EMIF are:

- One chip select ($\overline{\text{EM\_CS[0]}}$) dedicated for x16 SDRAM (x8 not supported)
- One chip select ($\overline{\text{EM\_CS[2]}}$) dedicated for x8 or x16 NOR Flash; x8 or x16 Asynchronous SRAM; or x8 or x16 NAND Flash
- Data bus width is 16 bits on the 144-pin RFP package
- SDRAM burst length of 16 bytes
- NAND Flash logic calculates ECC on blocks of up to 512 bytes
- ECC logic suitable for single-bit errors

Figure 3-5 shows a typical example of EMIF-to-memory hookup on the DA707/B/DA787B DSP.

As the figures illustrate, the DA707/B/DA787B DSP includes a limited number of EMIF address lines. These are sufficient to connect to SDRAM seamlessly. Asynchronous memory such as FLASH typically will need to use additional GPIO pins to act as upper address lines during device boot up when the FLASH contents are copied into SDRAM. (Normally, code is executed from SDRAM since SDRAM has faster access times).

Any pins listed with a 'Y' in the GPIO column of Table 2-2 may be used for this purpose, as long as it can be assured that they be pulled low at (and after) reset and held low until configured as outputs by the DSP.

The standard ROM-based bootloader in the DA707/B/DA787B DSP does not manipulate these pins. It only loads a small secondary bootloader from external flash into memory.

The secondary bootloader, which is stored in the external flash, needs to manipulate the GPIO pins to complete the boot procedure. Since the GPIO selection is effectively contained in the FLASH image, the actual pins can be tailored to a specific application.

Note that EM_BA[1:0] are used as low-order address lines for the asynchronous interface. For example, in Figure 3-5, the flash memory is not byte-addressable and its A[0] input selects a 16-bit value. The corresponding DSP address comes from EM_BA[1]. The remaining address lines from the DSP (EM_A[11:0]) drive a word address into the flash inputs A[12:1].

For a more detailed explanation of the DA707/B/DA787B EMIF operation please refer to the document *TMS320C672x External Memory Interface (EMIF) User's Guide* (literature number SPRU711).

NOTE

There is no EM_WAIT on the DA707/B/DA787B device.

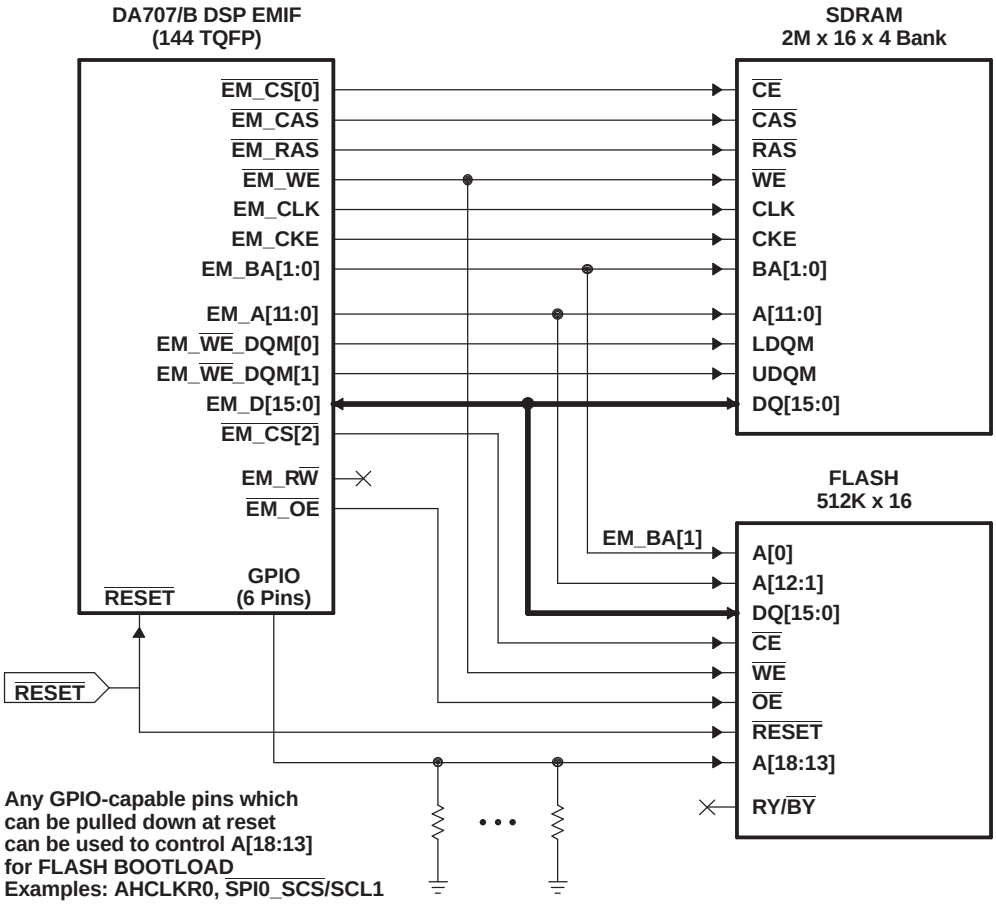


Figure 3-5. DA707/B/DA787B DSP 16-Bit EMIF (144-Pin RFP) Example

3.11.2 EMIF Peripheral Registers Description(s)

Table 3-4 is a list of the EMIF registers. For more information about these registers, see the *TMS320C672x DSP External Memory Interface (EMIF) User's Guide* (literature number SPRU711).

Table 3-4. EMIF Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0xF000 0004	AWCCR	Asynchronous Wait Cycle Configuration Register
0xF000 0008	SDCR	SDRAM Configuration Register
0xF000 000C	SDRCR	SDRAM Refresh Control Register
0xF000 0010	A1CR	Asynchronous 1 Configuration Register
0xF000 0020	SDTIMR	SDRAM Timing Register
0xF000 003C	SDSRETR	SDRAM Self Refresh Exit Timing Register
0xF000 0040	EIRR	EMIF Interrupt Raw Register
0xF000 0044	EIMR	EMIF Interrupt Mask Register
0xF000 0048	EIMSR	EMIF Interrupt Mask Set Register
0xF000 004C	EIMCR	EMIF Interrupt Mask Clear Register
0xF000 0060	NANDFCR	NAND Flash Control Register
0xF000 0064	NANDFSR	NAND Flash Status Register
0xF000 0070	NANDF1ECC	NAND Flash 1 ECC Register

3.11.3 EMIF Electrical Data/Timing

Table 3-5 through Table 3-8 assume testing over recommended operating conditions (see Figure 3-6 through Figure 3-11).

Table 3-5. EMIF SDRAM Interface Timing Requirements

NO.			MIN	MAX	UNIT
19	$t_{su(EM\_DV-EM\_CLKH)}$	Input setup time, read data valid on D[15:0] before EM_CLK rising	3		ns
20	$t_{h(EM\_CLKH-EM\_DIV)}$	Input hold time, read data valid on D[15:0] after EM_CLK rising	1.9		ns

Table 3-6. EMIF SDRAM Interface Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(EM\_CLK)}$	Cycle time, EMIF clock EM_CLK	10		ns
2	$t_{w(EM\_CLK)}$	Pulse width, EMIF clock EM_CLK high or low	3		ns
3	$t_{d(EM\_CLKH-EM\_CSV)S}$	Delay time, EM_CLK rising to $\overline{\text{EM\_CS[0]}}$ valid		7.7	ns
4	$t_{oh(EM\_CLKH-EM\_CSIV)S}$	Output hold time, EM_CLK rising to $\overline{\text{EM\_CS[0]}}$ invalid	1.15		ns
5	$t_{d(EM\_CLKH-EM\_WE-DQMV)S}$	Delay time, EM_CLK rising to EM_$\overline{\text{WE}}$_DQM[1:0] valid		7.7	ns
6	$t_{oh(EM\_CLKH-EM\_WE-DQMIV)S}$	Output hold time, EM_CLK rising to EM_$\overline{\text{WE}}$_DQM[1:0] invalid	1.15		ns
7	$t_{d(EM\_CLKH-EM\_AV)S}$	Delay time, EM_CLK rising to EM_A[11:0] and EM_BA[1:0] valid		7.7	ns
8	$t_{oh(EM\_CLKH-EM\_AIV)S}$	Output hold time, EM_CLK rising to EM_A[11:0] and EM_BA[1:0] invalid	1.15		ns
9	$t_{d(EM\_CLKH-EM\_DV)S}$	Delay time, EM_CLK rising to EM_D[15:0] valid		7.7	ns
10	$t_{oh(EM\_CLKH-EM\_DIV)S}$	Output hold time, EM_CLK rising to EM_D[15:0] invalid	1.15		ns
11	$t_{d(EM\_CLKH-EM\_RASV)S}$	Delay time, EM_CLK rising to $\overline{\text{EM\_RAS}}$ valid		7.7	ns
12	$t_{oh(EM\_CLKH-EM\_RASIV)S}$	Output hold time, EM_CLK rising to $\overline{\text{EM\_RAS}}$ invalid	1.15		ns
13	$t_{d(EM\_CLKH-EM\_CASV)S}$	Delay time, EM_CLK rising to $\overline{\text{EM\_CAS}}$ valid		7.7	ns
14	$t_{oh(EM\_CLKH-EM\_CASIV)S}$	Output hold time, EM_CLK rising to $\overline{\text{EM\_CAS}}$ invalid	1.15		ns
15	$t_{d(EM\_CLKH-EM\_WEV)S}$	Delay time, EM_CLK rising to $\overline{\text{EM\_WE}}$ valid		7.7	ns
16	$t_{oh(EM\_CLKH-EM\_WEIV)S}$	Output hold time, EM_CLK rising to $\overline{\text{EM\_WE}}$ invalid	1.15		ns
17	$t_{dis(EM\_CLKH-EM\_DHZ)S}$	Delay time, EM_CLK rising to EM_D[15:0] 3-stated		7.7	ns
18	$t_{ena(EM\_CLKH-EM\_DLZ)S}$	Output hold time, EM_CLK rising to EM_D[15:0] driving	1.15		ns

Table 3-7. EMIF Asynchronous Interface Timing Requirements(1)(2)

NO.			MIN	MAX	UNIT
28	$t_{su(EM\_DV-EM\_CLKH)A}$	Input setup time, read data valid on EM_D[15:0] before EM_CLK rising	5		ns
29	$t_{h(EM\_CLKH-EM\_DIV)A}$	Input hold time, read data valid on EM_D[15:0] after EM_CLK rising	2		ns

(1) E = SYSCLK3 (EM_CLK) period.
(2) These parameters apply to memories selected by $\overline{\text{EM\_CS[2]}}$ in both normal and NAND modes.

Table 3-8. EMIF Asynchronous Interface Switching Characteristics(1)

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{c(EM\_CLK)}$	Cycle time, EMIF clock EM_CLK	10		ns
2	$t_{w(EM\_CLK)}$	Pulse width, high or low, EMIF clock EM_CLK	3		ns
17	$t_{dis(EM\_CLKH-EM\_DHZ)S}$	Delay time, EM_CLK rising to EM_D[15:0] 3-stated		7.7	ns
18	$t_{ena(EM\_CLKH-EM\_DLZ)S}$	Output hold time, EM_CLK rising to EM_D[15:0] driving	1.15		ns
21	$t_{d(EM\_CLKH-EM\_CS2V)A}$	Delay time, from EM_CLK rising edge to $\overline{\text{EM\_CS[2]}}$ valid	0	8	ns
22	$t_{d(EM\_CLKH-EM\_WE\_DQMV)A}$	Delay time, EM_CLK rising to EM_$\overline{\text{WE}}$_DQM[1:0] valid	0	8	ns
23	$t_{d(EM\_CLKH-EM\_AV)A}$	Delay time, EM_CLK rising to EM_A[11:0] and EM_BA[1:0] valid	0	8	ns
24	$t_{d(EM\_CLKH-EM\_DV)A}$	Delay time, EM_CLK rising to EM_D[15:0] valid	0	8	ns
25	$t_{d(EM\_CLKH-EM\_OEV)A}$	Delay time, EM_CLK rising to $\overline{\text{EM\_OE}}$ valid	0	8	ns
26	$t_{d(EM\_CLKH-EM\_RW)A}$	Delay time, EM_CLK rising to EM_$\overline{\text{RW}}$ valid	0	8	ns
27	$t_{dis(EM\_CLKH-EM\_DDIS)A}$	Delay time, EM_CLK rising to EM_D[15:0] 3-stated	0	8	ns
32	$t_{d(EM\_CLKH-EM\_WE)A}$	Delay time, EM_CLK rising to $\overline{\text{EM\_WE}}$ valid	0	8	ns

(1) These parameters apply to memories selected by $\overline{\text{EM\_CS[2]}}$ in both normal and NAND modes.

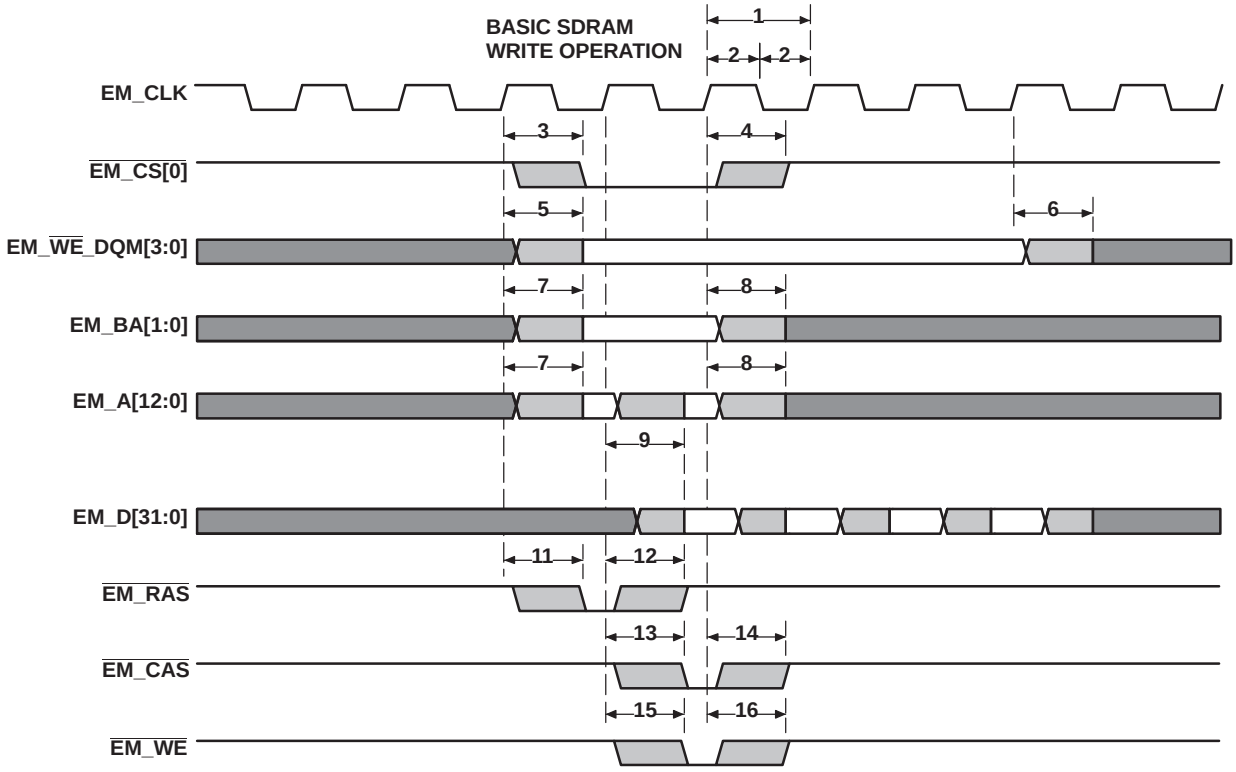


Figure 3-6. Basic SDRAM Write Operation

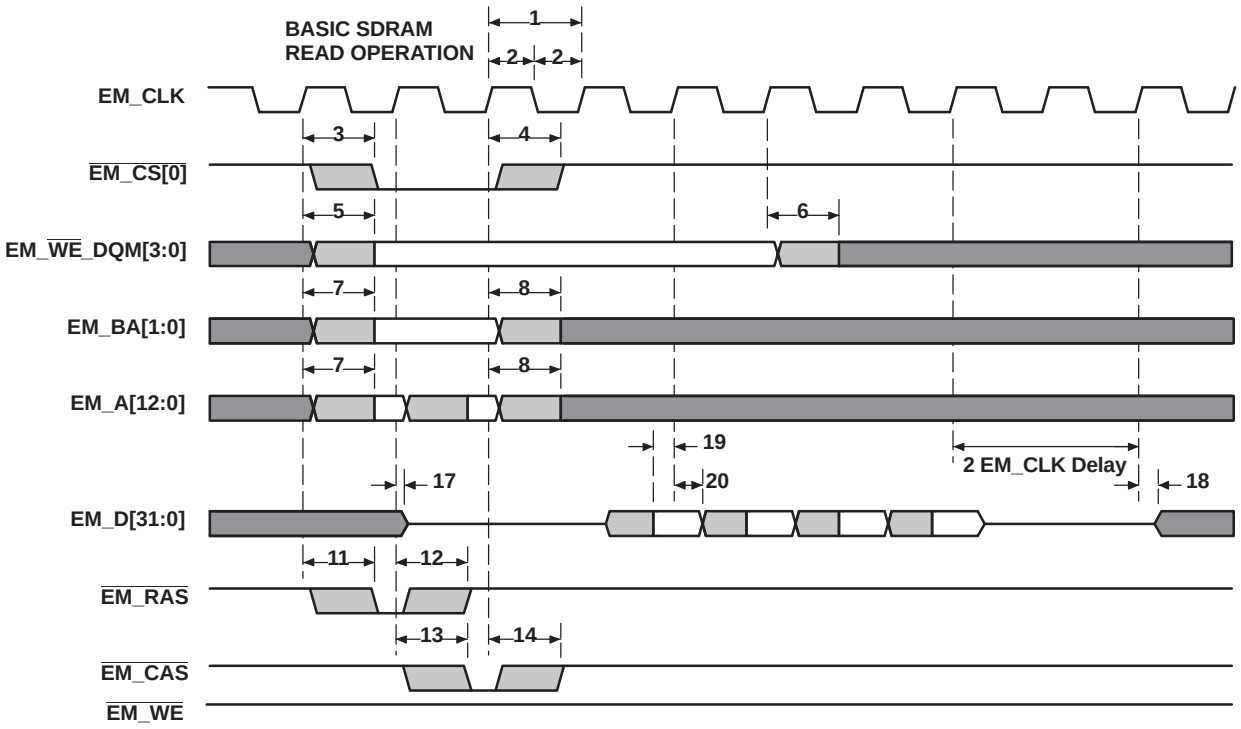


Figure 3-7. Basic SDRAM Read Operation

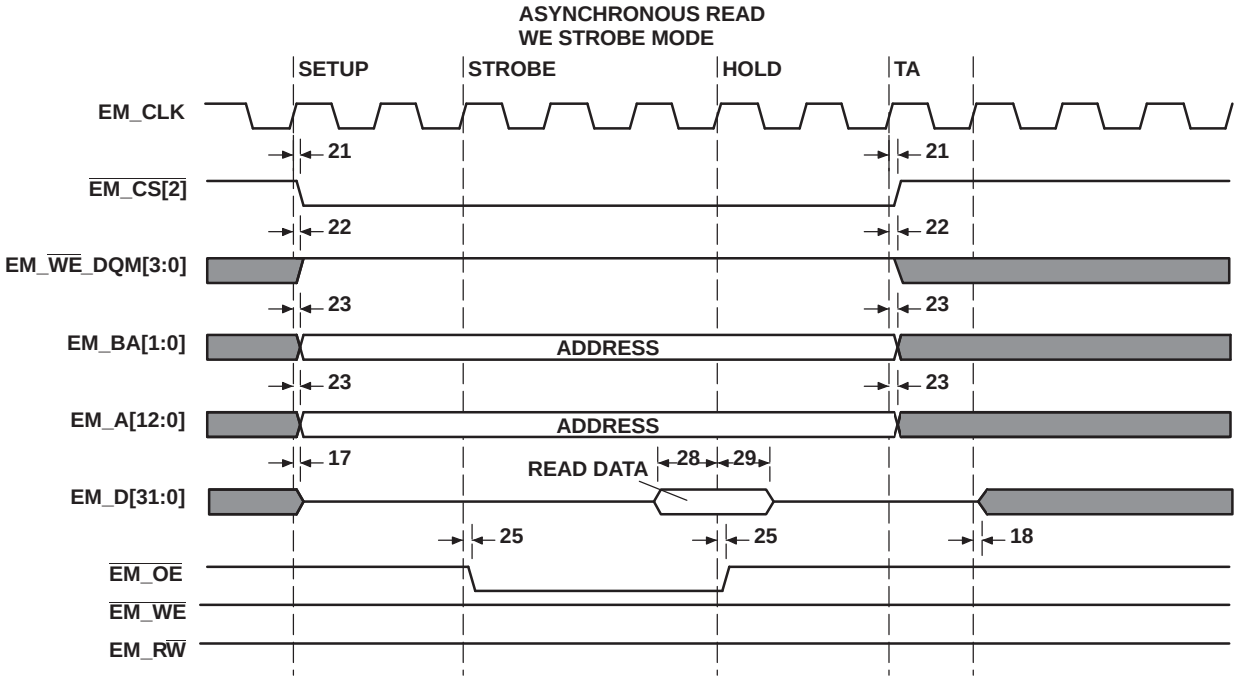


Figure 3-8. Asynchronous Read WE Strobe Mode

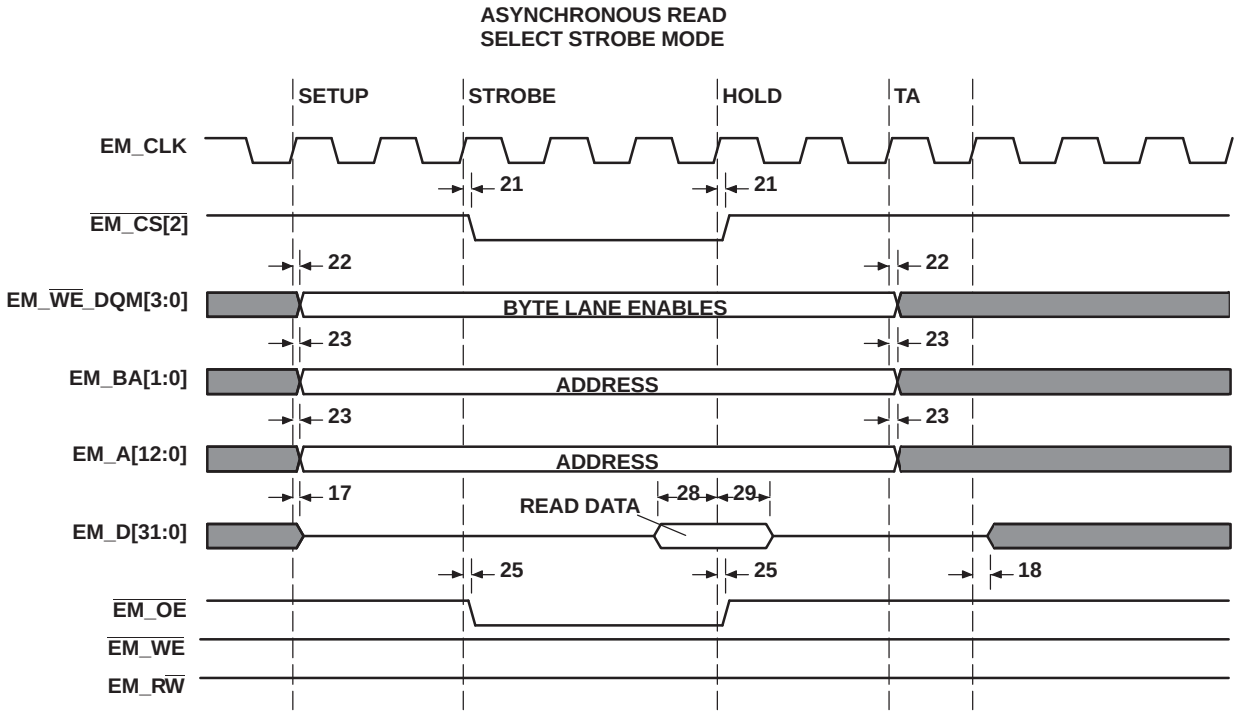


Figure 3-9. Asynchronous Read Select Strobe Mode

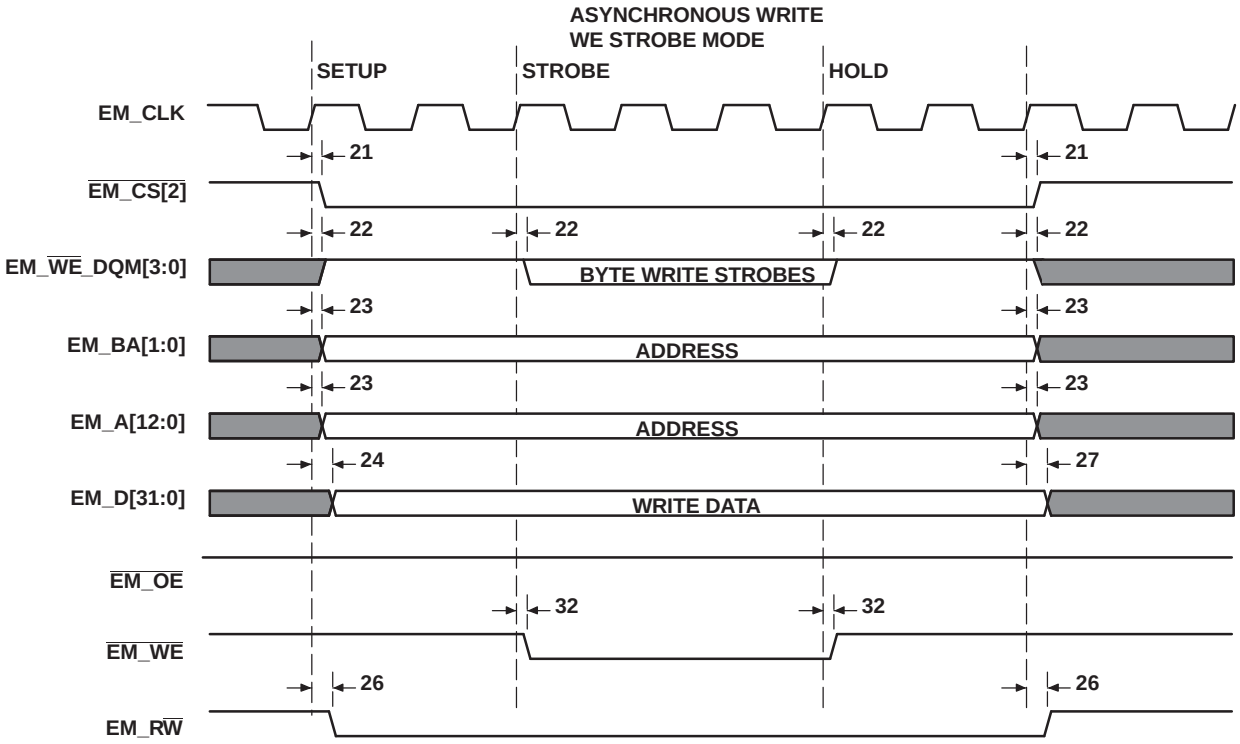


Figure 3-10. Asynchronous Write WE Strobe Mode

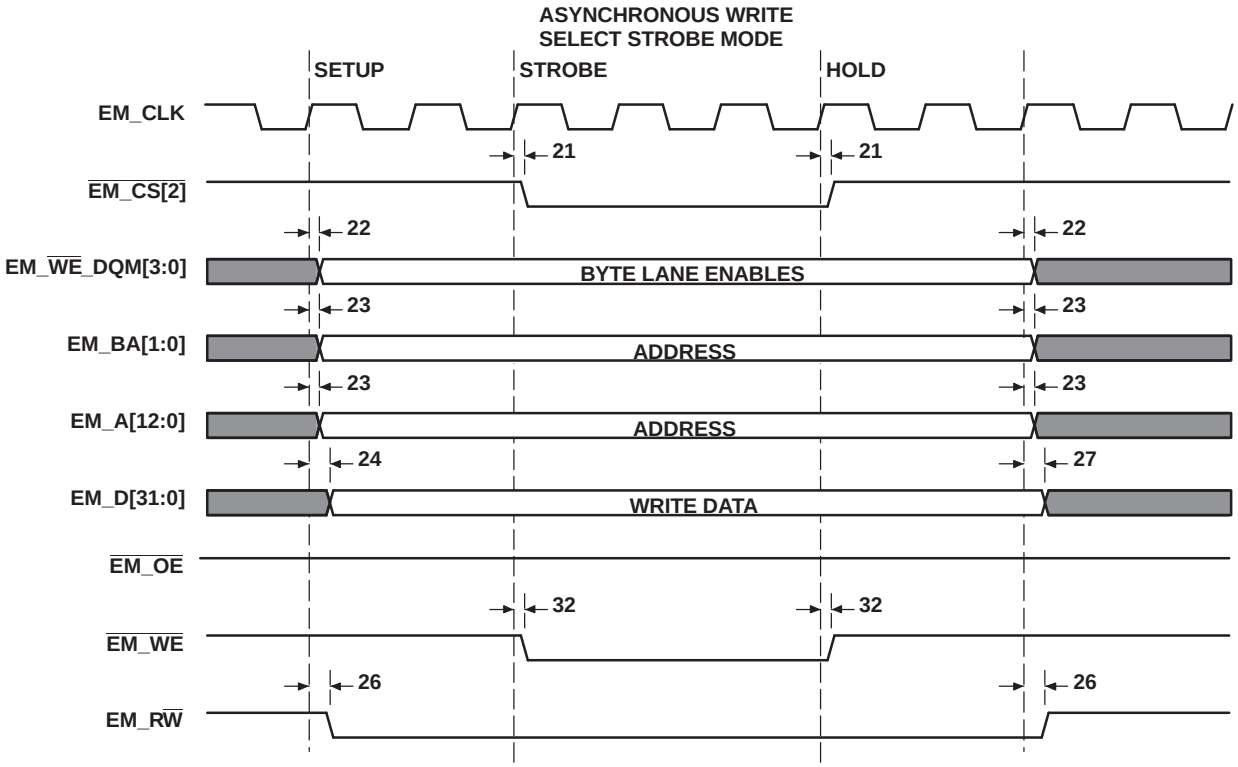


Figure 3-11. Asynchronous Write Select Strobe Mode

3.12 Multichannel Audio Serial Ports (McASP0, McASP1, and McASP2)

The McASP serial port is specifically designed for multichannel audio applications. Its key features are:

- Flexible clock and frame sync generation logic and on-chip dividers
- Up to sixteen transmit or receive data pins and serializers
- Large number of serial data format options, including:
  - TDM Frames with 2 to 32 time slots per frame (periodic) or 1 slot per frame (burst).
  - Time slots of 8,12,16, 20, 24, 28, and 32 bits.
  - First bit delay 0, 1, or 2 clocks.
  - MSB or LSB first bit order.
  - Left- or right-aligned data words within time slots
- DIT Mode (optional) with 384-bit Channel Status and 384-bit User Data registers.
- Extensive error checking and mute generation logic
- All unused pins GPIO-capable

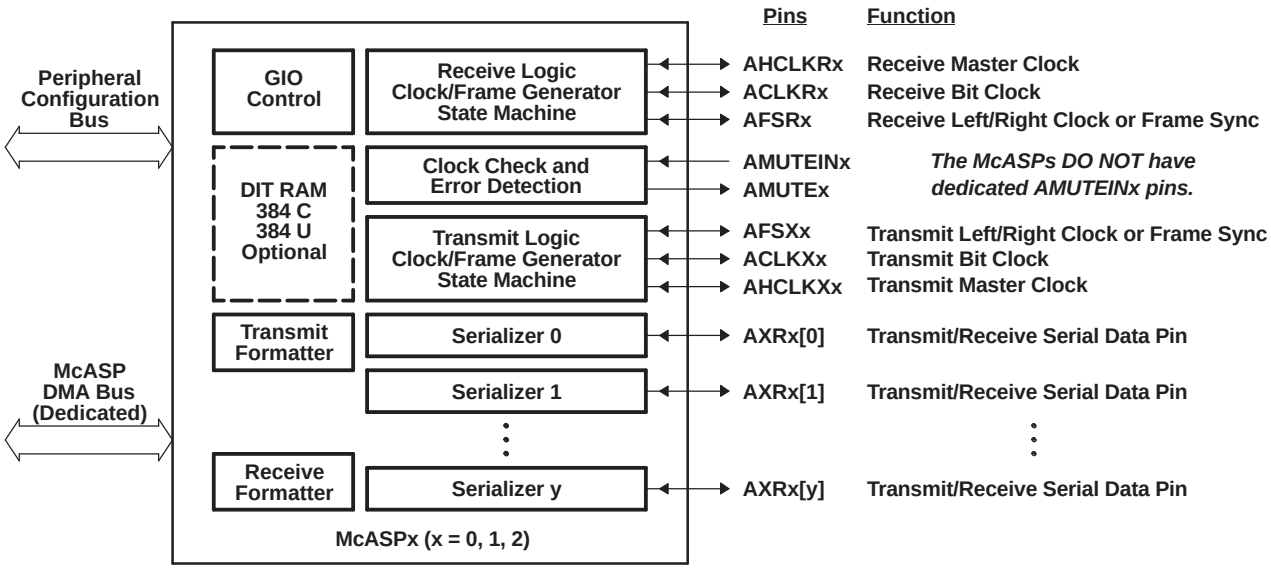


Figure 3-12. McASP Block Diagram

The three McASPs on DA707/B/DA787B have different configurations (see Table 3-9).

Table 3-9. McASP Configurations on DA707/B/DA787B DSP

McASP	DIT	CLOCK PINS	DATA PINS	COMMENTS
McASP0	No	AHCLKX0/AHCLKX2, ACLKX0, AFSX0 AHCLKR0/AHCLKR1, ACLKR0, AFSR0	Up to 16	AHCLKX0/AHCLKX2 share pin. AHCLKR0/AHCLKR1 share pin.
McASP1	No	AHCLKX1, ACLKX1, AFSX1, ACLKR1, AFSR1	Up to 6	AHCLKR0/AHCLKR1 share pin
McASP2	Yes	(The ACLKX0/ACLKX2 shared pin can be used as DIT reference clock.)	Up to 2	On the 144-pin RFP package, functions only as DIT since only AHCLKX0/AHCLKX2 is available.

NOTE: The McASPs ***do not*** have dedicated AMUTEINx pins. Instead they can select one of the pins listed in Table 3-11, Table 3-12, and Table 3-13 to use as a mute input.

3.12.1 McASP Peripheral Registers Description(s)

Table 3-10 is a list of the McASP registers. For more information about these registers, see the *TMS320C672x DSP Multichannel Audio Serial Port (McASP) Reference Guide* (literature number SPRU878).

Table 3-10. McASP Registers Accessed Through Peripheral Configuration Bus

McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
Device-Level Configuration Registers Controlling McASP				
0x4000 0018	0x4000 001C	0x4000 0020	CFGMCASPx	Selects the peripheral pin to be used as AMUTEINx
McASP Internal Registers				
0x4400 0000	0x4500 0000	0x4600 0000	PID	Peripheral identification register
0x4400 0004	0x4500 0004	0x4600 0004	PWRDEMU	Power down and emulation management register
0x4400 0010	0x4500 0010	0x4600 0010	PFUNC	Pin function register
0x4400 0014	0x4500 0014	0x4600 0014	PDIR	Pin direction register
0x4400 0018	0x4500 0018	0x4600 0018	PDOUT	Pin data output register
0x4400 001C	0x4500 001C	0x4600 001C	PDIN (reads)	Read returns: Pin data input register
			PDSET (writes)	Writes affect: Pin data set register (alternate write address: PDOUT)
0x4400 0020	0x4500 0020	0x4600 0020	PDCLR	Pin data clear register (alternate write address: PDOUT)
0x4400 0044	0x4500 0044	0x4600 0044	GBLCTL	Global control register
0x4400 0048	0x4500 0048	0x4600 0048	AMUTE	Audio mute control register
0x4400 004C	0x4500 004C	0x4600 004C	DLBCTL	Digital loopback control register
0x4400 0050	0x4500 0050	0x4600 0050	DITCTL	DIT mode control register
0x4400 0060	0x4500 0060	0x4600 0060	RGBLCTL	Receiver global control register: Alias of GBLCTL, only receive bits are affected - allows receiver to be reset independently from transmitter
0x4400 0064	0x4500 0064	0x4600 0064	RMASK	Receive format unit bit mask register
0x4400 0068	0x4500 0068	0x4600 0068	RFMT	Receive bit stream format register
0x4400 006C	0x4500 006C	0x4600 006C	AFSRCTL	Receive frame sync control register
0x4400 0070	0x4500 0070	0x4600 0070	ACLKRCTL	Receive clock control register
0x4400 0074	0x4500 0074	0x4600 0074	AHCLKRCTL	Receive high-frequency clock control register
0x4400 0078	0x4500 0078	0x4600 0078	RTDM	Receive TDM time slot 0-31 register
0x4400 007C	0x4500 007C	0x4600 007C	RINTCTL	Receiver interrupt control register
0x4400 0080	0x4500 0080	0x4600 0080	RSTAT	Receiver status register
0x4400 0084	0x4500 0084	0x4600 0084	RSLOT	Current receive TDM time slot register
0x4400 0088	0x4500 0088	0x4600 0088	RCLKCHK	Receive clock check control register
0x4400 008C	0x4500 008C	0x4600 008C	REVTCTL	Receiver DMA event control register
0x4400 00AC	0x4500 00AC	0x4600 00AC	XGBLCTL	Transmitter global control register. Alias of GBLCTL, only transmit bits are affected - allows transmitter to be reset independently from receiver
0x4400 00A4	0x4500 00A4	0x4600 00A4	XMASK	Transmit format unit bit mask register
0x4400 00A8	0x4500 00A8	0x4600 00A8	XFMT	Transmit bit stream format register
0x4400 00AC	0x4500 00AC	0x4600 00AC	AFSXCTL	Transmit frame sync control register
0x4400 00B0	0x4500 00B0	0x4600 00B0	ACLKXCTL	Transmit clock control register
0x4400 00B4	0x4500 00B4	0x4600 00B4	AHCLKXCTL	Transmit high-frequency clock control register
0x4400 00B8	0x4500 00B8	0x4600 00B8	XTDM	Transmit TDM time slot 0-31 register
0x4400 00BC	0x4500 00BC	0x4600 00BC	XINTCTL	Transmitter interrupt control register
0x4400 00C0	0x4500 00C0	0x4600 00C0	XSTAT	Transmitter status register
0x4400 00C4	0x4500 00C4	0x4600 00C4	XSLOT	Current transmit TDM time slot register
0x4400 00C8	0x4500 00C8	0x4600 00C8	XCLKCHK	Transmit clock check control register
0x4400 00CC	0x4500 00CC	0x4600 00CC	XEVTCTL	Transmitter DMA event control register
–	–	0x4600 0100	DITCSRA0	Left channel status register 0
–	–	0x4600 0104	DITCSRA1	Left channel status register 1
–	–	0x4600 0108	DITCSRA2	Left channel status register 2

Table 3-10. McASP Registers Accessed Through Peripheral Configuration Bus (continued)

McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
–	–	0x4600 010C	DITCSRA3	Left channel status register 3
–	–	0x4600 0110	DITCSRA4	Left channel status register 4
–	–	0x4600 0114	DITCSRA5	Left channel status register 5
–	–	0x4600 0118	DITCSRB0	Right channel status register 0
–	–	0x4600 011C	DITCSRB1	Right channel status register 1
–	–	0x4600 0120	DITCSRB2	Right channel status register 2
–	–	0x4600 0124	DITCSRB3	Right channel status register 3
–	–	0x4600 0128	DITCSRB4	Right channel status register 4
–	–	0x4600 012C	DITCSRB5	Right channel status register 5
–	–	0x4600 0130	DITUDRA0	Left channel user data register 0
–	–	0x4600 0134	DITUDRA1	Left channel user data register 1
–	–	0x4600 0138	DITUDRA2	Left channel user data register 2
–	–	0x4600 013C	DITUDRA3	Left channel user data register 3
–	–	0x4600 0140	DITUDRA4	Left channel user data register 4
–	–	0x4600 0144	DITUDRA5	Left channel user data register 5
–	–	0x4600 0148	DITUDRB0	Right channel user data register 0
–	–	0x4600 014C	DITUDRB1	Right channel user data register 1
–	–	0x4600 0150	DITUDRB2	Right channel user data register 2
–	–	0x4600 0154	DITUDRB3	Right channel user data register 3
–	–	0x4600 0158	DITUDRB4	Right channel user data register 4
–	–	0x4600 015C	DITUDRB5	Right channel user data register 5
0x4400 0180	0x4500 0180	0x4600 0180	SRCTL0	Serializer control register 0
0x4400 0184	0x4500 0184	0x4600 0184	SRCTL1	Serializer control register 1
0x4400 0188	0x4500 0188	–	SRCTL2	Serializer control register 2
0x4400 018C	0x4500 018C	–	SRCTL3	Serializer control register 3
0x4400 0190	0x4500 0190	–	SRCTL4	Serializer control register 4
0x4400 0194	0x4500 0194	–	SRCTL5	Serializer control register 5
0x4400 0198	–	–	SRCTL6	Serializer control register 6
0x4400 019C	–	–	SRCTL7	Serializer control register 7
0x4400 01A0	–	–	SRCTL8	Serializer control register 8
0x4400 01A4	–	–	SRCTL9	Serializer control register 9
0x4400 01A8	–	–	SRCTL10	Serializer control register 10
0x4400 01AC	–	–	SRCTL11	Serializer control register 11
0x4400 01B0	–	–	SRCTL12	Serializer control register 12
0x4400 01B4	–	–	SRCTL13	Serializer control register 13
0x4400 01B8	–	–	SRCTL14	Serializer control register 14
0x4400 01BC	–	–	SRCTL15	Serializer control register 15
0x4400 0200	0x4500 0200	0x4600 0200	XBUF0(1)	Transmit buffer register for serializer 0
0x4400 0204	0x4500 0204	0x4600 0204	XBUF1(1)	Transmit buffer register for serializer 1
0x4400 0208	0x4500 0208	–	XBUF2(1)	Transmit buffer register for serializer 2
0x4400 020C	0x4500 020C	–	XBUF3(1)	Transmit buffer register for serializer 3
0x4400 0210	0x4500 0210	–	XBUF4(1)	Transmit buffer register for serializer 4
0x4400 0214	0x4500 0214	–	XBUF5(1)	Transmit buffer register for serializer 5
0x4400 0218	–	–	XBUF6(1)	Transmit buffer register for serializer 6
0x4400 021C	–	–	XBUF7(1)	Transmit buffer register for serializer 7

(1) Writes to XRBUF originate from peripheral configuration bus only when XBUSEL = 1 in XFMT.

Table 3-10. McASP Registers Accessed Through Peripheral Configuration Bus (continued)

McASP0 BYTE ADDRESS	McASP1 BYTE ADDRESS	McASP2 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x4400 0220	–	–	XBUF8(1)	Transmit buffer register for serializer 8
0x4400 0224	–	–	XBUF9(1)	Transmit buffer register for serializer 9
0x4400 0228	–	–	XBUF10(1)	Transmit buffer register for serializer 10
0x4400 022C	–	–	XBUF11(1)	Transmit buffer register for serializer 11
0x4400 0230	–	–	XBUF12(1)	Transmit buffer register for serializer 12
0x4400 0234	–	–	XBUF13(1)	Transmit buffer register for serializer 13
0x4400 0238	–	–	XBUF14(1)	Transmit buffer register for serializer 14
0x4400 023C	–	–	XBUF15(1)	Transmit buffer register for serializer 15
0x4400 0280	0x4500 0280	0x4600 0280	RBUF0(2)	Receive buffer register for serializer 0
0x4400 0284	0x4500 0284	0x4600 0284	RBUF1(2)	Receive buffer register for serializer 1
0x4400 0288	0x4500 0288	–	RBUF2(2)	Receive buffer register for serializer 2
0x4400 028C	0x4500 028C	–	RBUF3(2)	Receive buffer register for serializer 3
0x4400 0290	0x4500 0290	–	RBUF4(2)	Receive buffer register for serializer 4
0x4400 0294	0x4500 0294	–	RBUF5(2)	Receive buffer register for serializer 5
0x4400 0298	–	–	RBUF6(2)	Receive buffer register for serializer 6
0x4400 029C	–	–	RBUF7(2)	Receive buffer register for serializer 7
0x4400 02A0	–	–	RBUF8(2)	Receive buffer register for serializer 8
0x4400 02A4	–	–	RBUF9(2)	Receive buffer register for serializer 9
0x4400 02A8	–	–	RBUF10(2)	Receive buffer register for serializer 10
0x4400 02AC	–	–	RBUF11(2)	Receive buffer register for serializer 11
0x4400 02B0	–	–	RBUF12(2)	Receive buffer register for serializer 12
0x4400 02B4	–	–	RBUF13(2)	Receive buffer register for serializer 13
0x4400 02B8	–	–	RBUF14(2)	Receive buffer register for serializer 14
0x4400 02BC	–	–	RBUF15(2)	Receive buffer register for serializer 15

(2) Reads from XRBUF originate on peripheral configuration bus only when RBUSEL = 1 in RFMT.

Figure 3-13 shows the bit layout of the CFGMCASP0 register and Table 3-11 contains a description of the bits.

31	8
Reserved	

7	3	2	0
Reserved		AMUTEIN0	
		R/W, 0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-13. CFGMCASP0 Register Bit Layout (0x4000 0018)

Table 3-11. CFGMCASP0 Register Bit Field Description (0x4000 0018)

BIT NO.	NAME	RESET VALUE	READ WRITE	DESCRIPTION
31:3	Reserved	N/A	N/A	Reads are indeterminate. Only 0s should be written to these bits.
2:0	AMUTEIN0	0	R/W	AMUTEIN0 Selects the source of the input to the McASP0 mute input. 000 = Select the input to be a constant '0' 001 = Select the input from AXR0[7]/SPI1_CLK 010 = Select the input from AXR0[8]/AXR1[5]/SPI1_SOMI 011 = Select the input from AXR0[9]/AXR1[4]/SPI1_SIMO 100 = Reserved 101 = Select the input from SPI0_SIMO 110 = Select the input from $\overline{\text{SPI0\_SCS}}$/I2C1_SCL 111 = Select the input from $\overline{\text{SPI0\_ENA}}$/I2C1_SDA

Figure 3-14 shows the bit layout of the CFGMCASP1 register and Table 3-12 contains a description of the bits.

31	8
Reserved	

7	3	2	0
Reserved		AMUTEIN1	
		R/W, 0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-14. CFGMCASP1 Register Bit Layout (0x4000 001C)

Table 3-12. CFGMCASP1 Register Bit Field Description (0x4000 001C)

BIT NO.	NAME	RESET VALUE	READ WRITE	DESCRIPTION
31:3	Reserved	N/A	N/A	Reads are indeterminate. Only 0s should be written to these bits.
2:0	AMUTEIN1	0	R/W	AMUTEIN1 Selects the source of the input to the McASP1 mute input. 000 = Select the input to be a constant '0' 001 = Select the input from AXR0[7]/SPI1_CLK 010 = Select the input from AXR0[8]/AXR1[5]/SPI1_SOMI 011 = Select the input from AXR0[9]/AXR1[4]/SPI1_SIMO 100 = Reserved 101 = Select the input from SPI0_SIMO 110 = Select the input from $\overline{\text{SPI0\_SCS}}$/I2C1_SCL 111 = Select the input from $\overline{\text{SPI0\_ENA}}$/I2C1_SDA

Figure 3-15 shows the bit layout of the CFGMCASP2 register and Table 3-13 contains a description of the bits.

31	8
Reserved	

7	3	2	0
Reserved		AMUTEIN2	
		R/W, 0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-15. CFGMCASP2 Register Bit Layout (0x4000 0020)

Table 3-13. CFGMCASP2 Register Bit Field Description (0x4000 0020)

BIT NO.	NAME	RESET VALUE	READ WRITE	DESCRIPTION
31:3	Reserved	N/A	N/A	Reads are indeterminate. Only 0s should be written to these bits.
2:0	AMUTEIN2	0	R/W	AMUTEIN2 Selects the source of the input to the McASP2 mute input. 000 = Select the input to be a constant '0' 001 = Select the input from AXR0[7]/SPI1_CLK 010 = Select the input from AXR0[8]/AXR1[5]/SPI1_SOMI 011 = Select the input from AXR0[9]/AXR1[4]/SPI1_SIMO 100 = Reserved 101 = Select the input from SPI0_SIMO 110 = Select the input from $\overline{\text{SPI0\_SCS}}$/I2C1_SCL 111 = Select the input from $\overline{\text{SPI0\_ENA}}$/I2C1_SDA

3.12.2 McASP Electrical Data/Timing

3.12.2.1 Multichannel Audio Serial Port (McASP) Timing

Table 3-14 and Table 3-15 assume testing over recommended operating conditions (see Figure 3-16 and Figure 3-17).

Table 3-14. McASP Timing Requirements(1)(2)

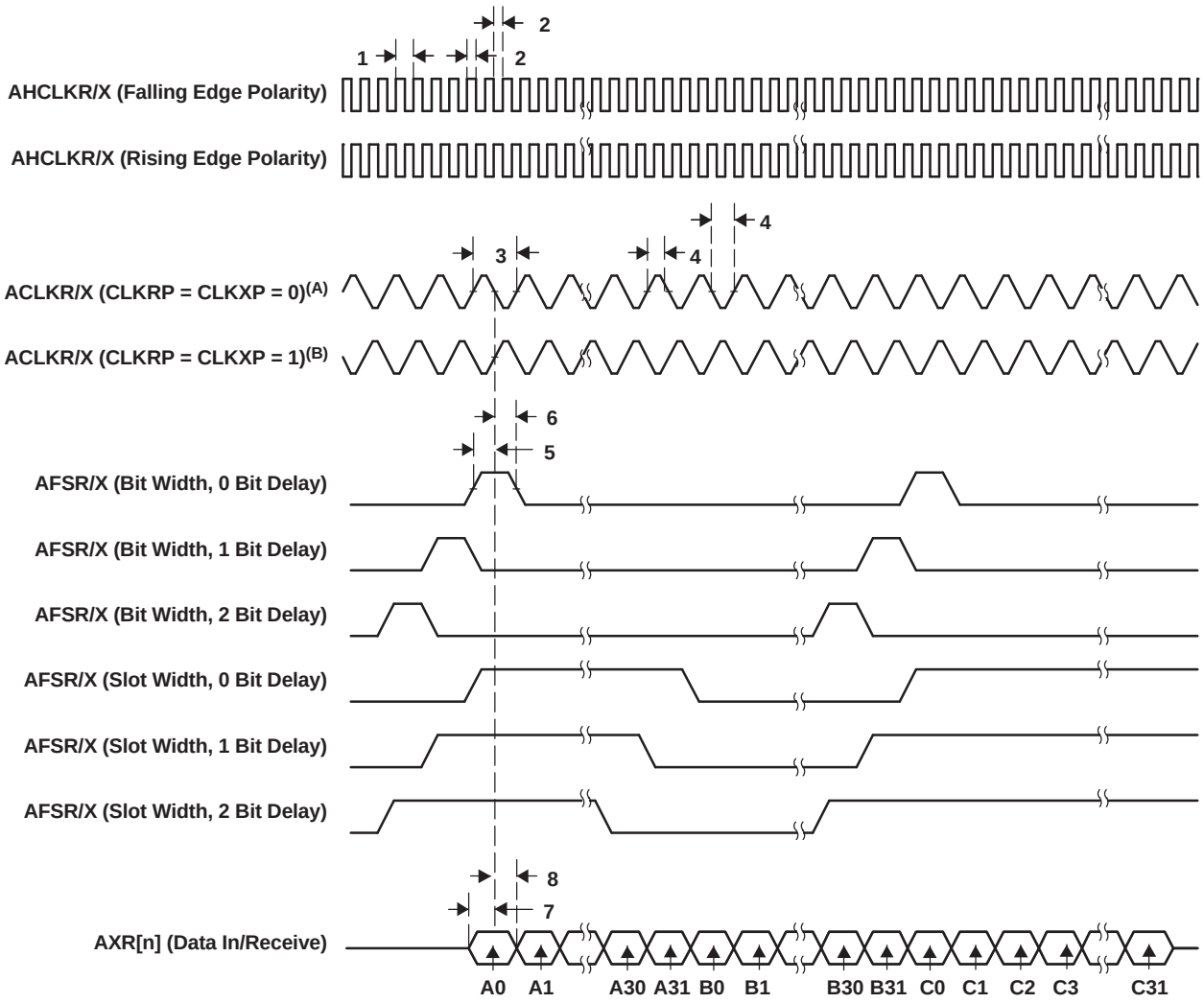
NO.			MIN	MAX	UNIT
1	$t_{c(AHCKRX)}$	Cycle time, AHCLKR external, AHCLKR input	20		ns
		Cycle time, AHCLKX external, AHCLKX input	20		
2	$t_{w(AHCKRX)}$	Pulse duration, AHCLKR external, AHCLKR input	7.5		ns
		Pulse duration, AHCLKX external, AHCLKX input	7.5		
3	$t_{c(ACKRX)}$	Cycle time, ACLKR external, ACLKR input	greater of 2P or 20 ns		ns
		Cycle time, ACLKX external, ACLKX input	greater of 2P or 20 ns		
4	$t_{w(ACKRX)}$	Pulse duration, ACLKR external, ACLKR input	10		ns
		Pulse duration, ACLKX external, ACLKX input	10		
5	$t_{su(AFRXC-ACKRX)}$	Setup time, AFSR input to ACLKR internal	8		ns
		Setup time, AFSX input to ACLKX internal	8		
		Setup time, AFSR input to ACLKR external input	3		
		Setup time, AFSX input to ACLKX external input	3		
		Setup time, AFSR input to ACLKR external output	3		
		Setup time, AFSX input to ACLKX external output	3		
6	$t_{h(ACKRX-AFRX)}$	Hold time, AFSR input after ACLKR internal	0		ns
		Hold time, AFSX input after ACLKX internal	0		
		Hold time, AFSR input after ACLKR external input	3		
		Hold time, AFSX input after ACLKX external input	3		
		Hold time, AFSR input after ACLKR external output	3		
		Hold time, AFSX input after ACLKX external output	3		
7	$t_{su(AXR-ACKRX)}$	Setup time, AXRn input to ACLKR internal	8		ns
		Setup time, AXRn input to ACLKR external input	3		
		Setup time, AXRn input to ACLKR external output	3		
8	$t_{h(ACKRX-AXR)}$	Hold time, AXRn input after ACLKR internal	3		ns
		Hold time, AXRn input after ACLKR external input	3		
		Hold time, AXRn input after ACLKR external output	3		

(1) ACLKX internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR internal – ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR external input – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period

Table 3-15. McASP Switching Characteristics[1]

NO.	PARAMETER		MIN	MAX	UNIT
9	$t_{c(AHCKRX)}$	Cycle time, AHCLKR internal, AHCLKR output	20		ns
		Cycle time, AHCLKR external, AHCLKR output	20		
		Cycle time, AHCLKX internal, AHCLKX output	20		
		Cycle time, AHCLKX external, AHCLKX output	20		
10	$t_{w(AHCKRX)}$	Pulse duration, AHCLKR internal, AHCLKR output	(AHR/2) – 2.5[2]		ns
		Pulse duration, AHCLKR external, AHCLKR output	(AHR/2) – 2.5[2]		
		Pulse duration, AHCLKX internal, AHCLKX output	(AHX/2) – 2.5[3]		
		Pulse duration, AHCLKX external, AHCLKX output	(AHX/2) – 2.5[3]		
11	$t_{c(ACKRX)}$	Cycle time, ACLKR internal, ACLKR output	greater of 2P or 20 ns[4]		ns
		Cycle time, ACLKR external, ACLKR output	greater of 2P or 20 ns[4]		
		Cycle time, ACLKX internal, ACLKX output	greater of 2P or 20 ns[4]		
		Cycle time, ACLKX external, ACLKX output	greater of 2P or 20 ns[4]		
12	$t_{w(ACKRX)}$	Pulse duration, ACLKR internal, ACLKR output	(AR/2) – 2.5[5]		ns
		Pulse duration, ACLKR external, ACLKR output	(AR/2) – 2.5[5]		
		Pulse duration, ACLKX internal, ACLKX output	(AX/2) – 2.5[6]		
		Pulse duration, ACLKX external, ACLKX output	(AX/2) – 2.5[6]		
13	$t_{d(ACKRX-FRX)}$	Delay time, ACLKR internal, AFSR output		5	ns
		Delay time, ACLKX internal, AFSX output		5	
		Delay time, ACLKR external input, AFSR output		10	
		Delay time, ACLKX external input, AFSX output		10	
		Delay time, ACLKR external output, AFSR output		10	
		Delay time, ACLKX external output, AFSX output		10	
		Delay time, ACLKR internal, AFSR output	–1		
		Delay time, ACLKX internal, AFSX output	–1		
		Delay time, ACLKR external input, AFSR output	0		
		Delay time, ACLKX external input, AFSX output	0		
		Delay time, ACLKR external output, AFSR output	0		
		Delay time, ACLKX external output, AFSX output	0		
14	$t_{d(ACLKX-AXRV)}$	Delay time, ACLKX internal, AXRn output	–1	5	ns
		Delay time, ACLKX external input, AXRn output	0	10	
		Delay time, ACLKX external output, AXRn output	0	10	
15	$t_{dis(ACKX-AXRHZ)}$	Disable time, ACLKX internal, AXRn output	–3	10	ns
		Disable time, ACLKX external input, AXRn output	–3	10	
		Disable time, ACLKX external output, AXRn output	–3	10	

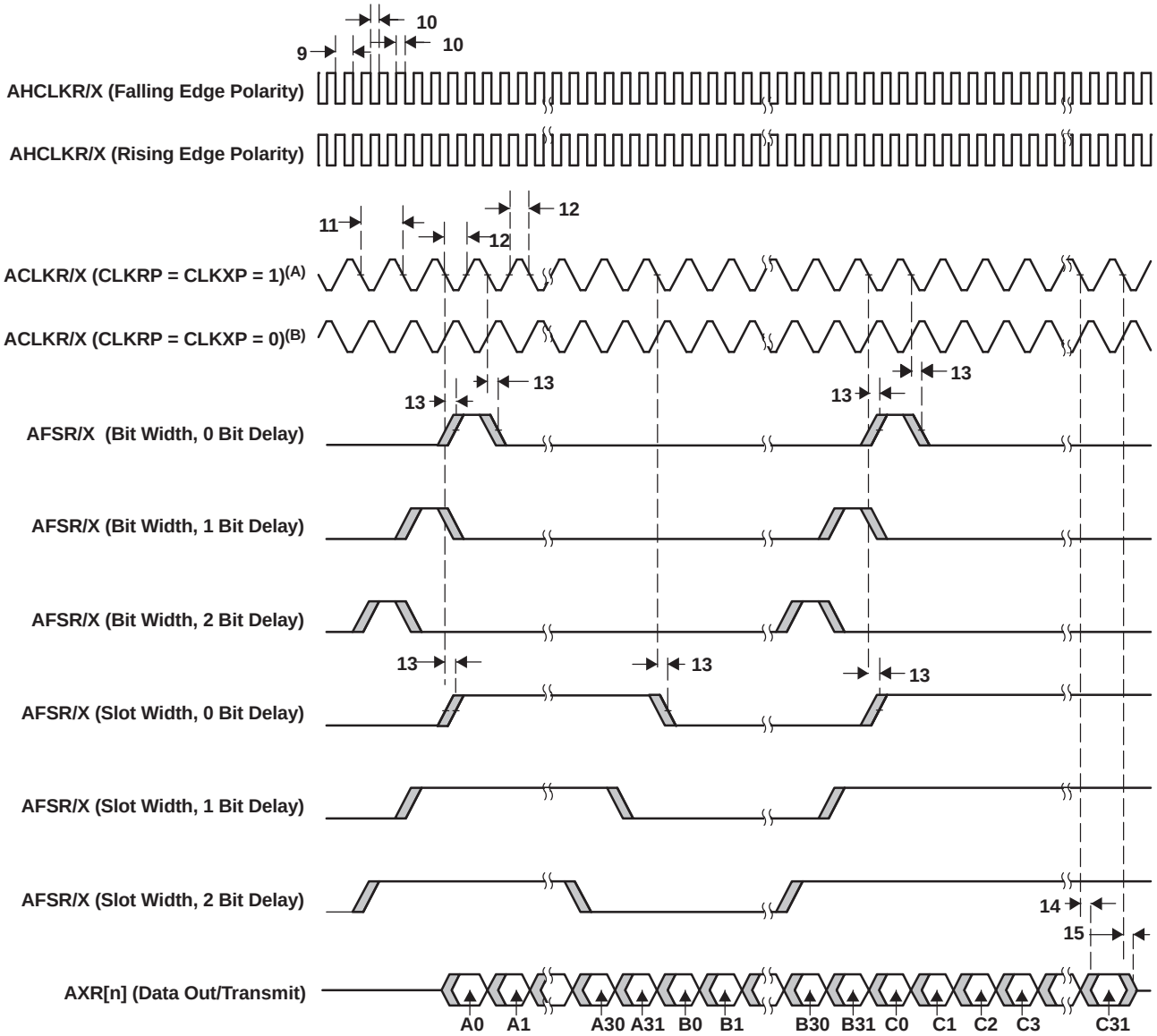
(1) ACLKX internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output – ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR internal – ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR external input – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output – ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AHR - Cycle time, AHCLKR.
(3) AHX - Cycle time, AHCLKX.
(4) P = SYSCLK2 period
(5) AR - ACLKR period.
(6) AX - ACLKX period.



A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

Figure 3-16. McASP Input Timings



A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

Figure 3-17. McASP Output Timings

3.13 Serial Peripheral Interface Ports (SPI0, SPI1)

Figure 3-18 is a block diagram of the SPI module, which is a simple shift register and buffer plus control logic. Data is written to the shift register before transmission occurs and is read from the buffer at the end of transmission. The SPI can operate either as a master, in which case, it initiates a transfer and drives the SPIx_CLK pin, or as a slave. Four clock phase and polarity options are supported as well as many data formatting options.

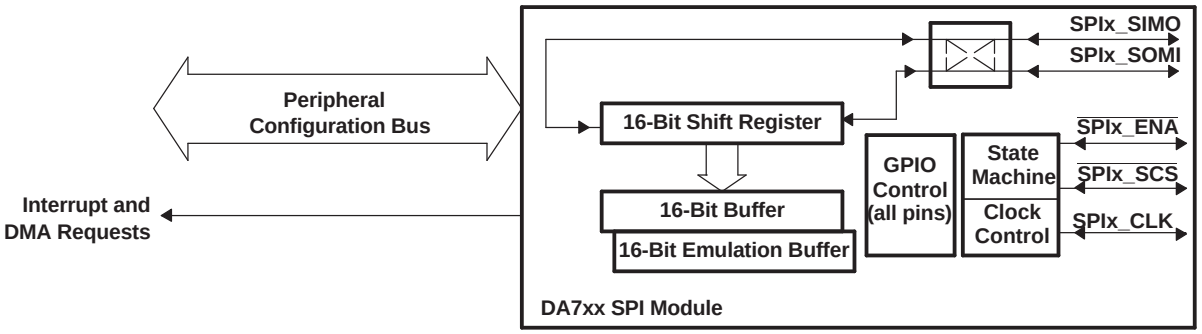


Figure 3-18. Block Diagram of SPI Module

The SPI supports 3-, 4-, and 5-pin operation with three basic pins (SPIx_CLK, SPIx_SIMO, and SPIx_SOMI) and two optional pins ($\overline{\text{SPIx\_SCS}}$, $\overline{\text{SPIx\_ENA}}$).

The optional $\overline{\text{SPIx\_SCS}}$ (Slave Chip Select) pin is most useful to enable in slave mode when there are other slave devices on the same SPI port. The DA707/B/DA787B will only shift data and drive the SPIx_SOMI pin when $\overline{\text{SPIx\_SCS}}$ is held low.

In slave mode, $\overline{\text{SPIx\_ENA}}$ is an optional output and can be driven in either a push-pull or open-drain manner. The $\overline{\text{SPIx\_ENA}}$ output provides the status of the internal transmit buffer (SPIDAT0/1 registers). In four-pin mode with the enable option, $\overline{\text{SPIx\_ENA}}$ is asserted only when the transmit buffer is full, indicating that the slave is ready to begin another transfer. In five-pin mode, the $\overline{\text{SPIx\_ENA}}$ is additionally qualified by $\overline{\text{SPIx\_SCS}}$ being asserted. This allows a single handshake line to be shared by multiple slaves on the same SPI bus.

In master mode, the $\overline{\text{SPIx\_ENA}}$ pin is an optional input and the master can be configured to delay the start of the next transfer until the slave asserts $\overline{\text{SPIx\_ENA}}$. The addition of this handshake signal simplifies SPI communications and, on average, increases SPI bus throughput since the master does not need to delay each transfer long enough to allow for the worst-case latency of the slave device. Instead, each transfer can begin as soon as both the master and slave have actually serviced the previous SPI transfer.

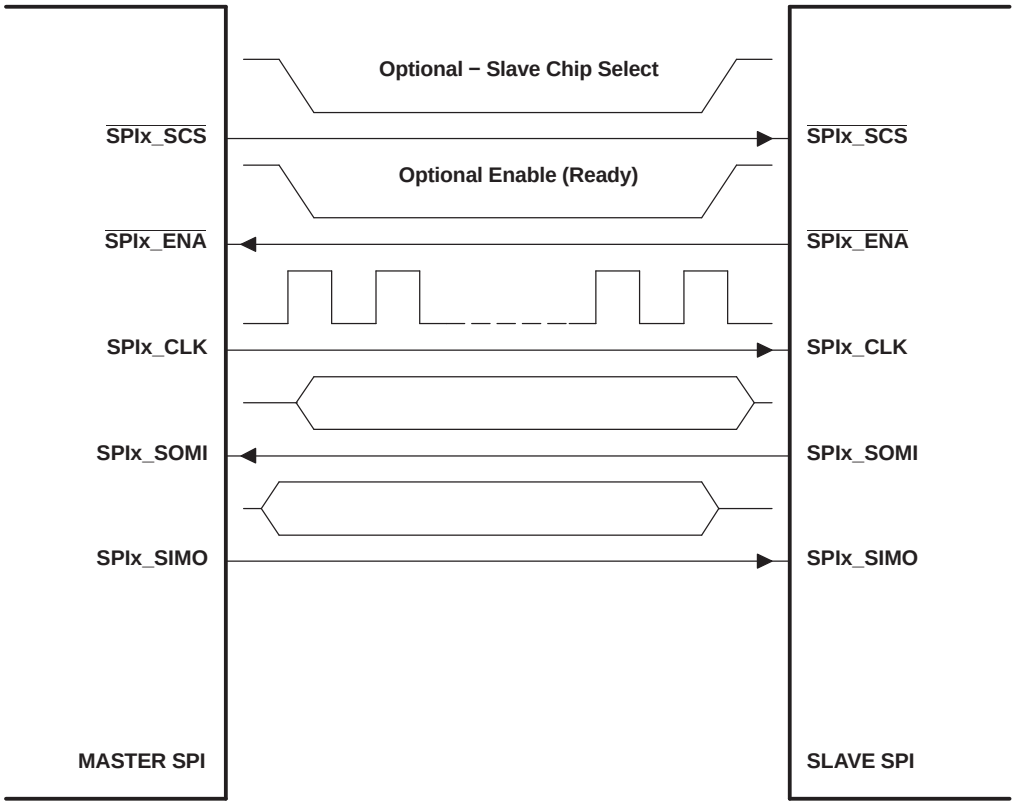


Figure 3-19. Illustration of SPI Master-to-SPI Slave Connection

3.13.1 SPI Peripheral Registers Description(s)

Table 3-16 is a list of the SPI registers.

Table 3-16. SPIx Configuration Registers

SPI0 BYTE ADDRESS	SPI1 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x4700 0000	0x4800 0000	SPIGCR0	Global Control Register 0
0x4700 0004	0x4800 0004	SPIGCR1	Global Control Register 1
0x4700 0008	0x4800 0008	SPIINT0	Interrupt Register
0x4700 000C	0x4800 000C	SPILVL	Interrupt Level Register
0x4700 0010	0x4800 0010	SPIFLG	Flag Register
0x4700 0014	0x4800 0014	SPIPC0	Pin Control Register 0 (Pin Function)
0x4700 0018	0x4800 0018	SPIPC1	Pin Control Register 1 (Pin Direction)
0x4700 001C	0x4800 001C	SPIPC2	Pin Control Register 2 (Pin Data In)
0x4700 0020	0x4800 0020	SPIPC3	Pin Control Register 3 (Pin Data Out)
0x4700 0024	0x4800 0024	SPIPC4	Pin Control Register 4 (Pin Data Set)
0x4700 0028	0x4800 0028	SPIPC5	Pin Control Register 5 (Pin Data Clear)
0x4700 002C	0x4800 002C	Reserved	Reserved - Do not write to this register
0x4700 0030	0x4800 0030	Reserved	Reserved - Do not write to this register
0x4700 0034	0x4800 0034	Reserved	Reserved - Do not write to this register
0x4700 0038	0x4800 0038	SPIDAT0	Shift Register 0 (without format select)
0x4700 003C	0x4800 003C	SPIDAT1	Shift Register 1 (with format select)
0x4700 0040	0x4800 0040	SPIBUF	Buffer Register
0x4700 0044	0x4800 0044	SPIEMU	Emulation Register
0x4700 0048	0x4800 0048	SPIDELAY	Delay Register
0x4700 004C	0x4800 004C	SPIDEF	Default Chip Select Register
0x4700 0050	0x4800 0050	SPIFMT0	Format Register 0
0x4700 0054	0x4800 0054	SPIFMT1	Format Register 1
0x4700 0058	0x4800 0058	SPIFMT2	Format Register 2
0x4700 005C	0x4800 005C	SPIFMT3	Format Register 3
0x4700 0060	0x4800 0060	TGINTVECT0	Interrupt Vector for SPI INT0
0x4700 0064	0x4800 0064	TGINTVECT1	Interrupt Vector for SPI INT1

3.13.2 SPI Electrical Data/Timing

3.13.2.1 Serial Peripheral Interface (SPI) Timing

Table 3-17 through Table 3-24 assume testing over recommended operating conditions (see Figure 3-20 through Figure 3-23).

Table 3-17. General Timing Requirements for SPIx Master Modes(1)

NO.				MIN	MAX	UNIT
1	$t_{c(SPC)M}$	Cycle Time, SPIx_CLK, All Master Modes		greater of 8P or 100 ns	256P	ns
2	$t_{w(SPCH)M}$	Pulse Width High, SPIx_CLK, All Master Modes		greater of 4P or 45 ns		ns
3	$t_{w(SPCL)M}$	Pulse Width Low, SPIx_CLK, All Master Modes		greater of 4P or 45 ns		ns
4	$t_{d(SIMO\_SPC)M}$	Delay, initial data bit valid on SPIx_SIMO to initial edge on SPIx_CLK(2)	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + 2P		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + 2P		
5	$t_{d(SPC\_SIMO)M}$	Delay, subsequent bits valid on SPIx_SIMO after transmit edge of SPIx_CLK	Polarity = 0, Phase = 0, from SPIx_CLK rising		15	ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling		15	
			Polarity = 1, Phase = 0, from SPIx_CLK falling		15	
			Polarity = 1, Phase = 1, from SPIx_CLK rising		15	
6	$t_{oh(SPC\_SIMO)M}$	Output hold time, SPIx_SIMO valid after receive edge of SPIxCLK, except for final bit(3)	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)M}$ – 10		ns
			Polarity = 0, Phase = 1, from SPIx_CLK rising	$0.5t_{c(SPC)M}$ – 10		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)M}$ – 10		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	$0.5t_{c(SPC)M}$ – 10		
7	$t_{su(SOMI\_SPC)M}$	Input Setup Time, SPIx_SOMI valid before receive edge of SPIx_CLK	Polarity = 0, Phase = 0, to SPIx_CLK falling	0.5P + 15		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	0.5P + 15		
8	$t_{ih(SPC\_SOMI)M}$	Input Hold Time, SPIx_SOMI valid after receive edge of SPIx_CLK	Polarity = 0, Phase = 0, from SPIx_CLK falling	0.5P + 5		ns
			Polarity = 0, Phase = 1, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	0.5P + 5		

(1) P = SYSCLK2 period
(2) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPIx_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPIx_SOMI.
(3) The final data bit will be held on the SPIx_SIMO pin until the SPIDAT0 or SPIDAT1 register is written with new data.

Table 3-18. General Timing Requirements for SPIx Slave Modes[1]

NO.				MIN	MAX	UNIT
9	$t_{c(SPC)S}$	Cycle Time, SPIx_CLK, All Slave Modes		greater of 8P or 100 ns	256P	ns
10	$t_{w(SPCH)S}$	Pulse Width High, SPIx_CLK, All Slave Modes		greater of 4P or 45 ns		ns
11	$t_{w(SPCL)S}$	Pulse Width Low, SPIx_CLK, All Slave Modes		greater of 4P or 45 ns		ns
12	$t_{su(SOMI\_SPC)S}$	Setup time, transmit data written to SPI and output onto SPIx_SOMI pin before initial clock edge from master.[2][3]	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	2P		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	2P		
13	$t_{d(SPC\_SOMI)S}$	Delay, subsequent bits valid on SPIx_SOMI after transmit edge of SPIx_CLK	Polarity = 0, Phase = 0, from SPIx_CLK rising		2P + 15	ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling		2P + 15	
			Polarity = 1, Phase = 0, from SPIx_CLK falling		2P + 15	
			Polarity = 1, Phase = 1, from SPIx_CLK rising		2P + 15	
14	$t_{oh(SPC\_SOMI)S}$	Output hold time, SPIx_SOMI valid after receive edge of SPIxCLK, except for final bit[4]	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)S} - 10$		ns
			Polarity = 0, Phase = 1, from SPIx_CLK rising	$0.5t_{c(SPC)S} - 10$		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)S} - 10$		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	$0.5t_{c(SPC)S} - 10$		
15	$t_{su(SIMO\_SPC)S}$	Input Setup Time, SPIx_SIMO valid before receive edge of SPIx_CLK	Polarity = 0, Phase = 0, to SPIx_CLK falling	0.5P + 15		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 0, to SPIx_CLK rising	0.5P + 15		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	0.5P + 15		
16	$t_{ih(SPC\_SIMO)S}$	Input Hold Time, SPIx_SIMO valid after receive edge of SPIx_CLK	Polarity = 0, Phase = 0, from SPIx_CLK falling	0.5P + 5		ns
			Polarity = 0, Phase = 1, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	0.5P + 5		
			Polarity = 1, Phase = 1, from SPIx_CLK falling	0.5P + 5		

(1) P = SYSCLK2 period
(2) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPIx_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPIx_SIMO.
(3) Measured from the termination of the write of new data to the SPI module, as evidenced by new output data appearing on the SPIx_SOMI pin. In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by either the DSP CPU or the dMAX.
(4) The final data bit will be held on the SPIx_SOMI pin until the SPIDAT0 or SPIDAT1 register is written with new data.

Table 3-19. Additional[1] SPI Master Timings, 4-Pin Enable Option[2][3]

NO.				MIN	MAX	UNIT
17	$t_{d(ENA\_SPC)M}$	Delay from slave assertion of $\overline{SPIx\_ENA}$ active to first SPIx_CLK from master.[4]	Polarity = 0, Phase = 0, to SPIx_CLK rising		3P + 15	ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising		$0.5t_{c(SPC)M}$ + 3P + 15	
			Polarity = 1, Phase = 0, to SPIx_CLK falling		3P + 15	
			Polarity = 1, Phase = 1, to SPIx_CLK falling		$0.5t_{c(SPC)M}$ + 3P + 15	
18	$t_{d(SPC\_ENA)M}$	Max delay for slave to deassert $\overline{SPIx\_ENA}$ after final SPIx_CLK edge to ensure master does not begin the next transfer.[5]	Polarity = 0, Phase = 0, from SPIx_CLK falling		$0.5t_{c(SPC)M}$	ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling		0	
			Polarity = 1, Phase = 0, from SPIx_CLK rising		$0.5t_{c(SPC)M}$	
			Polarity = 1, Phase = 1, from SPIx_CLK rising		0	

(1) These parameters are in addition to the general timings for SPI master modes (Table 3-17).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{SPIx\_ENA}$ assertion.
(5) In the case where the master SPI is ready with new data before $\overline{SPIx\_ENA}$ deassertion.

Table 3-20. Additional[1] SPI Master Timings, 4-Pin Chip Select Option[2][3]

NO.				MIN	MAX	UNIT
19	$t_{d(SCS\_SPC)M}$	Delay from $\overline{SPIx\_SCS}$ active to first SPIx_CLK[4][5]	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P – 10		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + 2P – 10		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P – 10		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + 2P – 10		
20	$t_{d(SPC\_SCS)M}$	Delay from final SPIx_CLK edge to master deasserting $\overline{SPIx\_SCS}$[6][7]	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)M}$		ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling	0		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)M}$		
			Polarity = 1, Phase = 1, from SPIx_CLK rising	0		

(1) These parameters are in addition to the general timings for SPI master modes (Table 3-17).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{SPIx\_SCS}$ assertion.
(5) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, $\overline{SPIx\_SCS}$ will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

Table 3-21. Additional[1] SPI Master Timings, 5-Pin Option[2][3]

NO.				MIN	MAX	UNIT
18	$t_{d(SPC\_ENA)M}$	Max delay for slave to deassert $\overline{SPIx\_ENA}$ after final SPIx_CLK edge to ensure master does not begin the next transfer.[4]	Polarity = 0, Phase = 0, from SPIx_CLK falling		$0.5t_{c(SPC)M}$	ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling		0	
			Polarity = 1, Phase = 0, from SPIx_CLK rising		$0.5t_{c(SPC)M}$	
			Polarity = 1, Phase = 1, from SPIx_CLK rising		0	
20	$t_{d(SPC\_SCS)M}$	Delay from final SPIx_CLK edge to master deasserting $\overline{SPIx\_SCS}$ [5][6]	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)M}$		ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling	0		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)M}$		
			Polarity = 1, Phase = 1, from SPIx_CLK rising	0		
21	$t_{d(SCSL\_ENAL)M}$	Max delay for slave SPI to drive $\overline{SPIx\_ENA}$ valid after master asserts $\overline{SPIx\_SCS}$ to delay the master from beginning the next transfer.			0.5P	ns
22	$t_{d(SCS\_SPC)M}$	Delay from $\overline{SPIx\_SCS}$ active to first SPIx_CLK[7][8][9]	Polarity = 0, Phase = 0, to SPIx_CLK rising	2P – 10		ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising	$0.5t_{c(SPC)M}$ + 2P – 10		
			Polarity = 1, Phase = 0, to SPIx_CLK falling	2P – 10		
			Polarity = 1, Phase = 1, to SPIx_CLK falling	$0.5t_{c(SPC)M}$ + 2P – 10		
23	$t_{d(ENA\_SPC)M}$	Delay from assertion of $\overline{SPIx\_ENA}$ low to first SPIx_CLK edge.[10]	Polarity = 0, Phase = 0, to SPIx_CLK rising		3P + 15	ns
			Polarity = 0, Phase = 1, to SPIx_CLK rising		$0.5t_{c(SPC)M}$ + 3P + 15	
			Polarity = 1, Phase = 0, to SPIx_CLK falling		3P + 15	
			Polarity = 1, Phase = 1, to SPIx_CLK falling		$0.5t_{c(SPC)M}$ + 3P + 15	

(1) These parameters are in addition to the general timings for SPI master modes (Table 3-17).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{SPIx\_ENA}$ deassertion.
(5) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, $\overline{SPIx\_SCS}$ will remain asserted.
(6) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
(7) If $\overline{SPIx\_ENA}$ is asserted immediately such that the transmission is not delayed by $\overline{SPIx\_ENA}$.
(8) In the case where the master SPI is ready with new data before $\overline{SPIx\_SCS}$ assertion.
(9) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(10) If $\overline{SPIx\_ENA}$ was initially deasserted high and SPIx_CLK is delayed.

Table 3-22. Additional[1] SPI Slave Timings, 4-Pin Enable Option[2][3]

NO.				MIN	MAX	UNIT
24	$t_{d(SPC\_ENAH)S}$	Delay from final SPIx_CLK edge to slave deasserting $\overline{\text{SPIx\_ENA}}$.	Polarity = 0, Phase = 0, from SPIx_CLK falling	P – 10	3P + 15	ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling	$-0.5t_{c(SPC)M}$ + P – 10	$-0.5t_{c(SPC)M}$ + 3P + 15	
			Polarity = 1, Phase = 0, from SPIx_CLK rising	P – 10	3P + 15	
			Polarity = 1, Phase = 1, from SPIx_CLK rising	$-0.5t_{c(SPC)M}$ + P – 10	$-0.5t_{c(SPC)M}$ + 3P + 15	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 3-18).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 3-23. Additional[1] SPI Slave Timings, 4-Pin Chip Select Option[2][3]

NO.				MIN	MAX	UNIT
25	$t_{d(SCSL\_SPC)S}$	Required delay from $\overline{\text{SPIx\_SCS}}$ asserted at slave to first SPIx_CLK edge at slave.		P		ns
26	$t_{d(SPC\_SCSH)S}$	Required delay from final $\overline{\text{SPIx\_CLK}}$ edge before $\overline{\text{SPIx\_SCS}}$ is deasserted.	Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)M}$ + P + 10		ns
			Polarity = 0, Phase = 1, from SPIx_CLK falling	P + 10		
			Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)M}$ + P + 10		
			Polarity = 1, Phase = 1, from SPIx_CLK rising	P + 10		
27	$t_{ena(SCSL\_SOMI)S}$	Delay from master asserting $\overline{\text{SPIx\_SCS}}$ to slave driving SPIx_SOMI valid			P + 15	ns
28	$t_{dis(SCSH\_SOMI)S}$	Delay from master deasserting $\overline{\text{SPIx\_SCS}}$ to slave 3-stating SPIx_SOMI			P + 15	ns

(1) These parameters are in addition to the general timings for SPI slave modes (Table 3-18).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

Table 3-24. Additional[1] SPI Slave Timings, 5-Pin Option[2][3]

NO.			MIN	MAX	UNIT
25	$t_{d(SCSL\_SPC)S}$	Required delay from $\overline{SPIx\_SCS}$ asserted at slave to first SPIx_CLK edge at slave.	P		ns
26	$t_{d(SPC\_SCSH)S}$	Required delay from final SPIx_CLK edge before $\overline{SPIx\_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPIx_CLK falling	$0.5t_{c(SPC)M}$ + P + 10		ns
		Required delay from final SPIx_CLK edge before $\overline{SPIx\_SCS}$ is deasserted. Polarity = 0, Phase = 1, from SPIx_CLK falling	P + 10		
		Required delay from final SPIx_CLK edge before $\overline{SPIx\_SCS}$ is deasserted. Polarity = 1, Phase = 0, from SPIx_CLK rising	$0.5t_{c(SPC)M}$ + P + 10		
		Required delay from final SPIx_CLK edge before $\overline{SPIx\_SCS}$ is deasserted. Polarity = 1, Phase = 1, from SPIx_CLK rising	P + 10		
27	$t_{ena(SCSL\_SOMI)S}$	Delay from master asserting $\overline{SPIx\_SCS}$ to slave driving SPIx_SOMI valid		P + 15	ns
28	$t_{dis(SCSH\_SOMI)S}$	Delay from master deasserting $\overline{SPIx\_SCS}$ to slave 3-stating SPIx_SOMI		P + 15	ns
29	$t_{ena(SCSL\_ENA)S}$	Delay from master deasserting $\overline{SPIx\_SCS}$ to slave driving $\overline{SPIx\_ENA}$ valid		15	ns
30	$t_{dis(SPC\_ENA)S}$	Delay from final clock receive edge on SPIx_CLK to slave 3-stating or driving high $\overline{SPIx\_ENA}$.[4] Polarity = 0, Phase = 0, from SPIx_CLK falling		2P + 15	ns
		Delay from final clock receive edge on SPIx_CLK to slave 3-stating or driving high $\overline{SPIx\_ENA}$.[4] Polarity = 0, Phase = 1, from SPIx_CLK rising		2P + 15	
		Delay from final clock receive edge on SPIx_CLK to slave 3-stating or driving high $\overline{SPIx\_ENA}$.[4] Polarity = 1, Phase = 0, from SPIx_CLK rising		2P + 15	
		Delay from final clock receive edge on SPIx_CLK to slave 3-stating or driving high $\overline{SPIx\_ENA}$.[4] Polarity = 1, Phase = 1, from SPIx_CLK falling		2P + 15	

(1) These parameters are in addition to the general timings for SPI slave modes (Table 3-18).
(2) P = SYSCLK2 period
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
(4) $\overline{SPIx\_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is 3-stated. If 3-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.

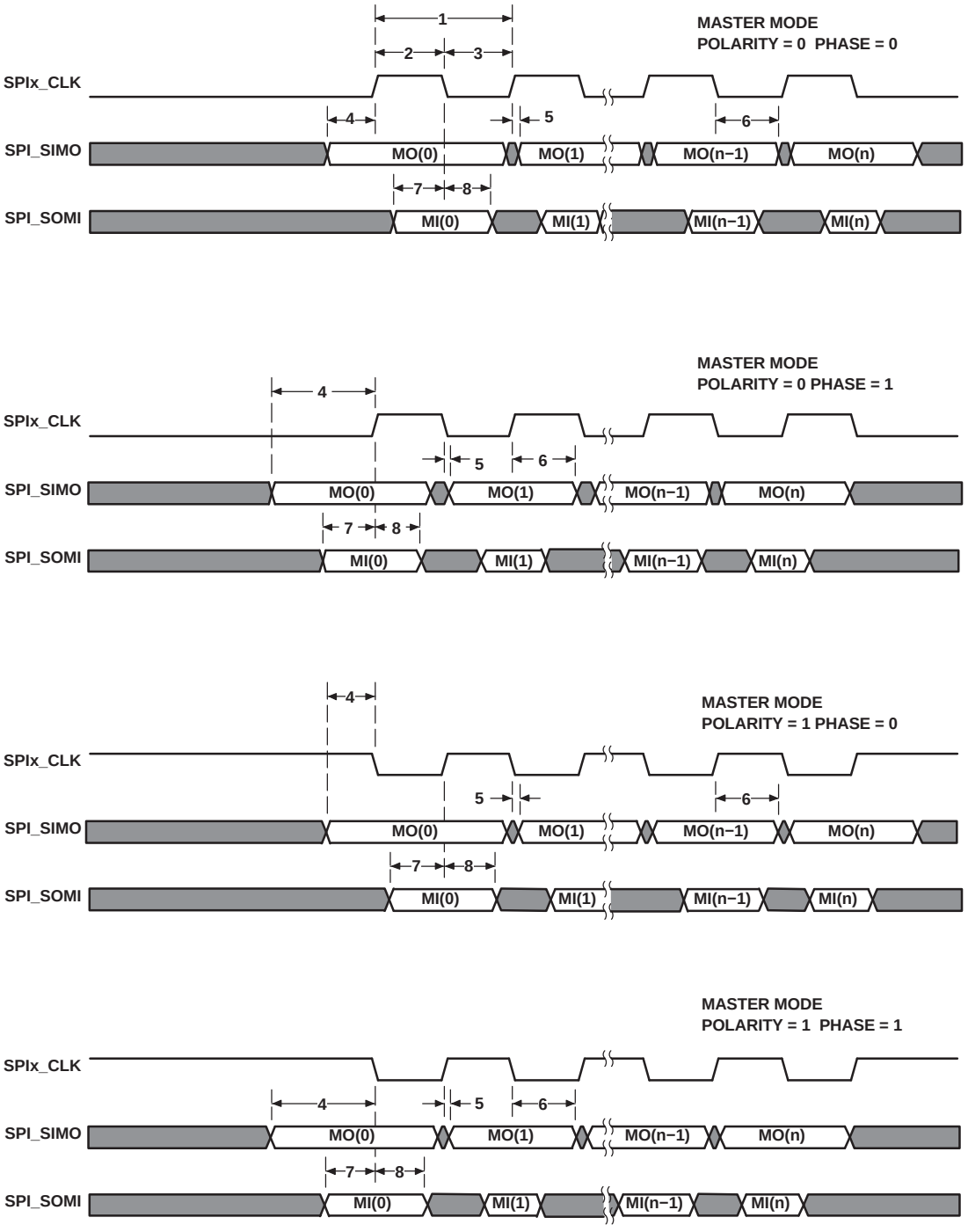


Figure 3-20. SPI Timings—Master Mode

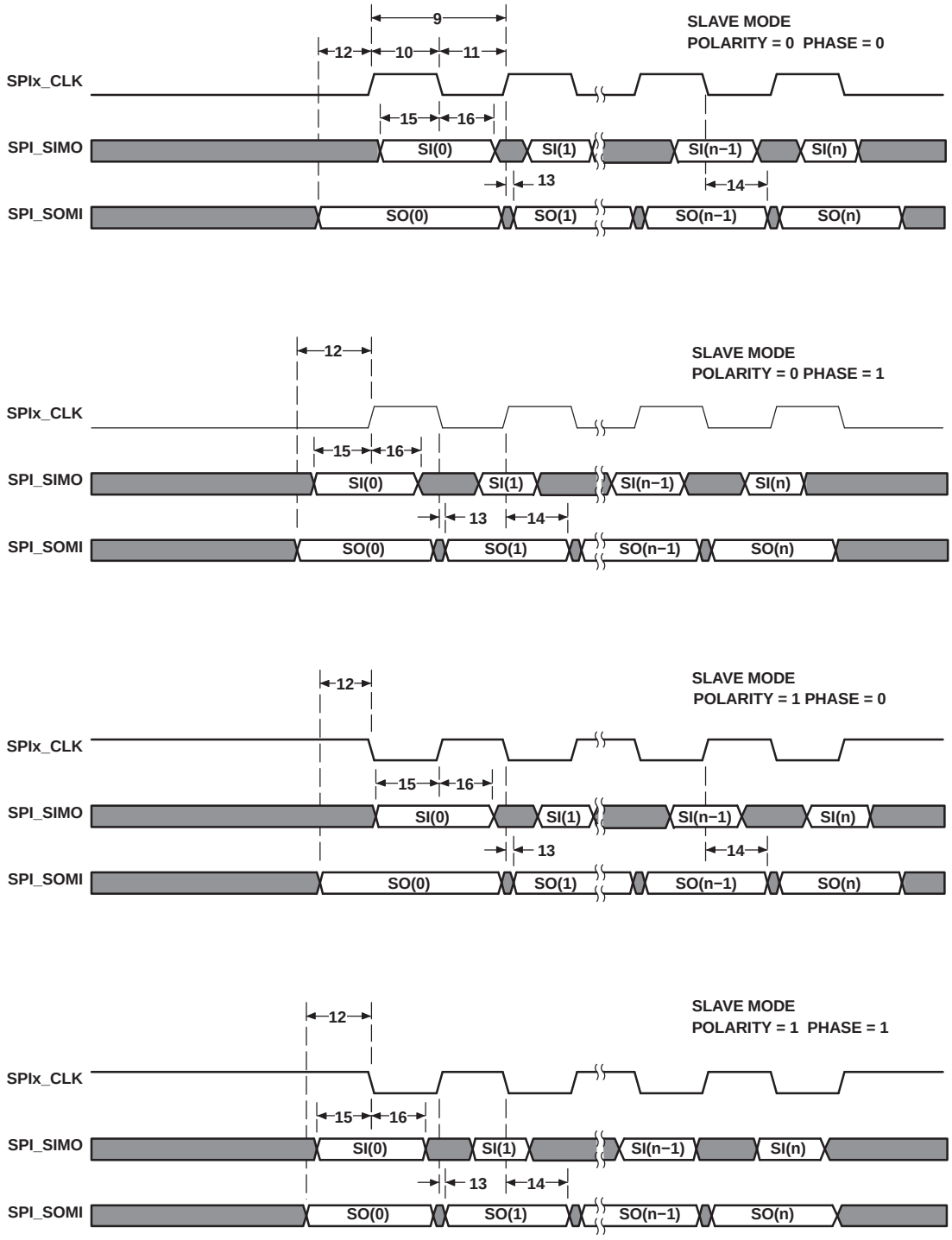


Figure 3-21. SPI Timings—Slave Mode

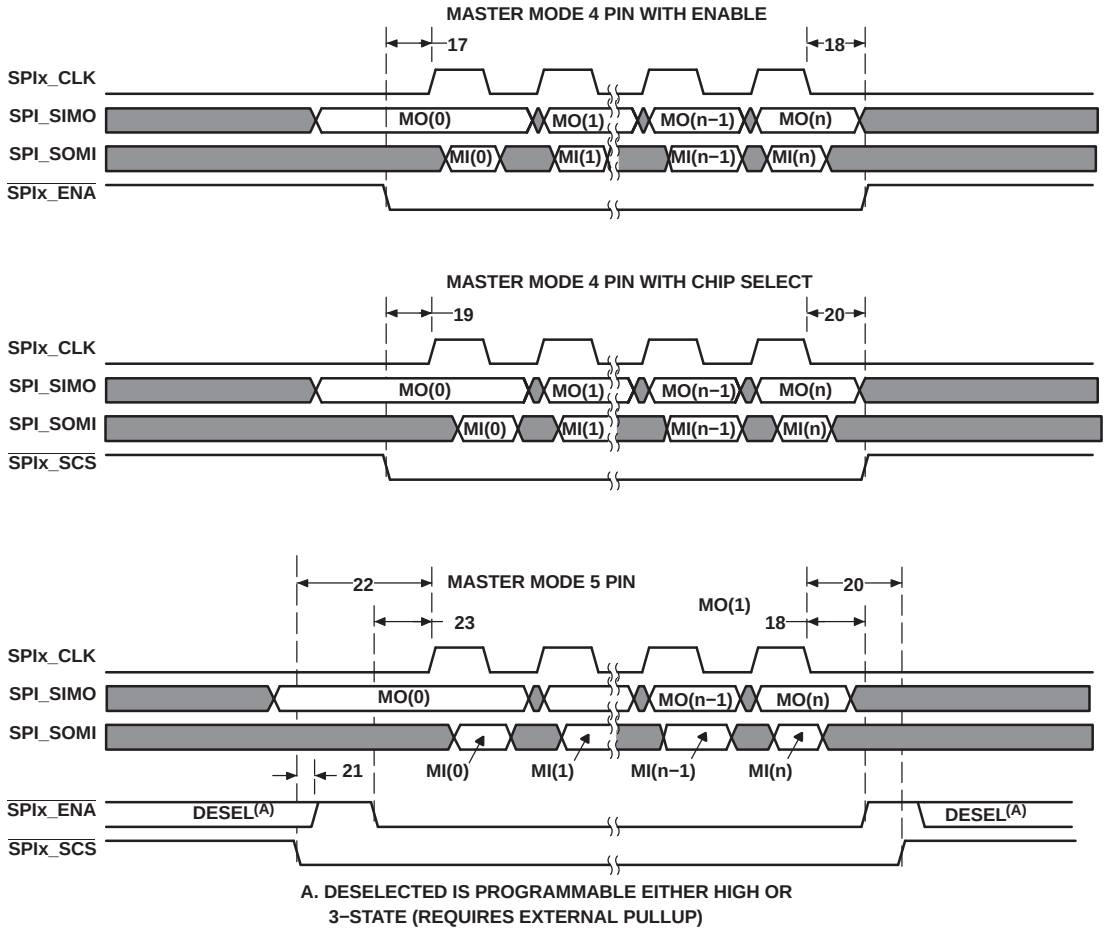


Figure 3-22. SPI Timings—Master Mode (4-Pin and 5-Pin)

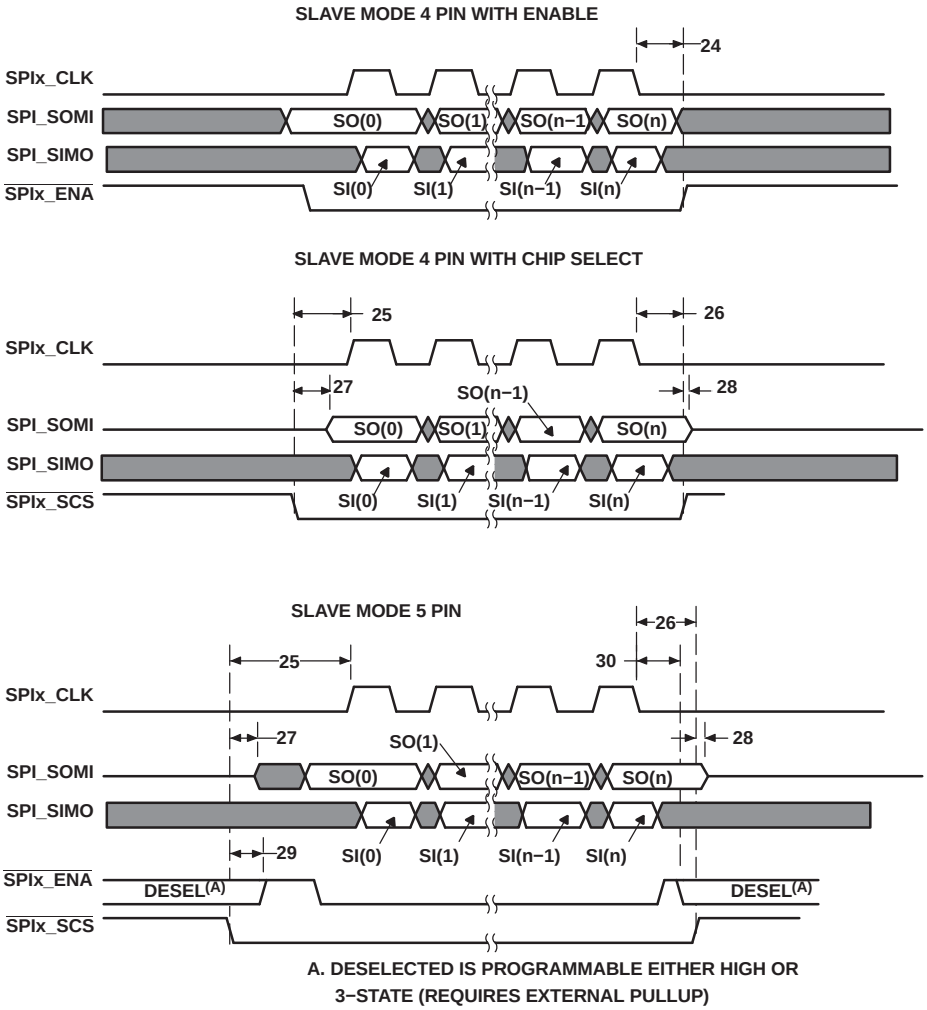


Figure 3-23. SPI Timings—Slave Mode (4-Pin and 5-Pin)

3.14 Inter-Integrated Circuit Serial Ports (I2C0, I2C1)

3.14.1 I2C Device-Specific Information

Having two I2C modules on the DA707/B/DA787B simplifies system architecture, since one module may be used by the DSP to control local peripherals ICs (DACs, ADCs, etc.) while the other may be used to communicate with other controllers in a system or to implement a user interface. Figure 3-24 is block diagram of the DA707/B/DA787B I2C Module.

Each I2C port supports:

- Compatible with Philips® I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- General-Purpose I/O Capability if not used as I2C

CAUTION

The DA707/B/DA787B I2C pins use a standard ±8 mA LVCMOS buffer, not the slow I/O buffer defined in the I2C specification. Series resistors may be necessary to reduce noise at the system level.

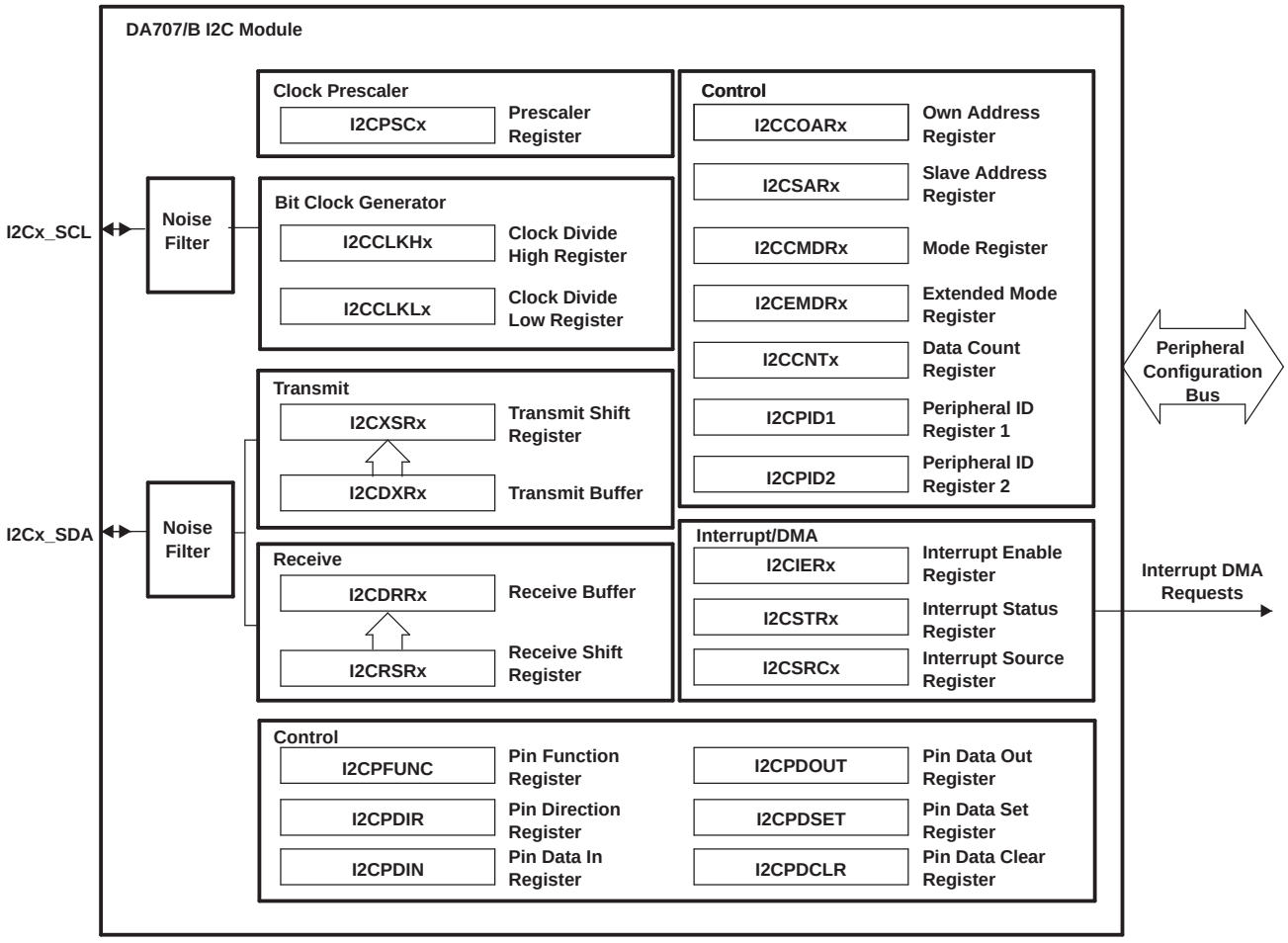


Figure 3-24. I2C Module Block Diagram

3.14.2 I2C Peripheral Registers Description(s)

Table 3-25 is a list of the I2C registers.

Table 3-25. I2Cx Configuration Registers

I2C0 BYTE ADDRESS	I2C1 BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x4900 0000	0x4A00 0000	I2COAR	Own Address Register
0x4900 0004	0x4A00 0004	I2CIER	Interrupt Enable Register
0x4900 0008	0x4A00 0008	I2CSTR	Interrupt Status Register
0x4900 000C	0x4A00 000C	I2CCLKL	Clock Low Time Divider Register
0x4900 0010	0x4A00 0010	I2CCLKH	Clock High Time Divider Register
0x4900 0014	0x4A00 0014	I2CCNT	Data Count Register
0x4900 0018	0x4A00 0018	I2CDRR	Data Receive Register
0x4900 001C	0x4A00 001C	I2CSAR	Slave Address Register
0x4900 0020	0x4A00 0020	I2CDXR	Data Transmit Register
0x4900 0024	0x4A00 0024	I2CMDR	Mode Register
0x4900 0028	0x4A00 0028	I2CISR	Interrupt Source Register
0x4900 002C	0x4A00 002C	I2CEMDR	Extended Mode Register
0x4900 0030	0x4A00 0030	I2CPSC	Prescale Register
0x4900 0034	0x4A00 0034	I2CPID1	Peripheral Identification Register 1
0x4900 0038	0x4A00 0038	I2CPID2	Peripheral Identification Register 2
0x4900 0048	0x4A00 0048	I2CPFUNC	Pin Function Register
0x4900 004C	0x4A00 004C	I2CPDIR	Pin Direction Register
0x4900 0050	0x4A00 0050	I2CPDIN	Pin Data Input Register
0x4900 0054	0x4A00 0054	I2CPDOUT	Pin Data Output Register
0x4900 0058	0x4A00 0058	I2CPDSET	Pin Data Set Register
0x4900 005C	0x4A00 005C	I2CPDCLR	Pin Data Clear Register

3.14.3 I2C Electrical Data/Timing

3.14.3.1 Inter-Integrated Circuit (I2C) Timing

Table 3-26 and Table 3-27 assume testing over recommended operating conditions (see Figure 3-25 and Figure 3-26).

Table 3-26. I2C Input Timing Requirements

NO.				MIN	MAX	UNIT
1	$t_{c(SCL)}$	Cycle time, I2Cx_SCL	Standard Mode	10		µs
			Fast Mode	2.5		
2	$t_{su(SCLH-SDAL)}$	Setup time, I2Cx_SCL high before I2Cx_SDA low	Standard Mode	4.7		µs
			Fast Mode	0.6		
3	$t_{h(SCLL-SDAL)}$	Hold time, I2Cx_SCL low after I2Cx_SDA low	Standard Mode	4		µs
			Fast Mode	0.6		
4	$t_{w(SCLL)}$	Pulse duration, I2Cx_SCL low	Standard Mode	4.7		µs
			Fast Mode	1.3		
5	$t_{w(SCLH)}$	Pulse duration, I2Cx_SCL high	Standard Mode	4		µs
			Fast Mode	0.6		
6	$t_{su(SDA-SCLH)}$	Setup time, I2Cx_SDA before I2Cx_SCL high	Standard Mode	250		ns
			Fast Mode	100		
7	$t_{h(SDA-SCLL)}$	Hold time, I2Cx_SDA after I2Cx_SCL low	Standard Mode	0		µs
			Fast Mode	0	0.9	
8	$t_{w(SDAH)}$	Pulse duration, I2Cx_SDA high	Standard Mode	4.7		µs
			Fast Mode	1.3		
9	$t_{r(SDA)}$	Rise time, I2Cx_SDA	Standard Mode		1000	ns
			Fast Mode	$20 + 0.1C_b$	300	
10	$t_{r(SCL)}$	Rise time, I2Cx_SCL	Standard Mode		1000	ns
			Fast Mode	$20 + 0.1C_b$	300	
11	$t_{f(SDA)}$	Fall time, I2Cx_SDA	Standard Mode		300	ns
			Fast Mode	$20 + 0.1C_b$	300	
12	$t_{f(SCL)}$	Fall time, I2Cx_SCL	Standard Mode		300	ns
			Fast Mode	$20 + 0.1C_b$	300	
13	$t_{su(SCLH-SDAH)}$	Setup time, I2Cx_SCL high before I2Cx_SDA high	Standard Mode	4		µs
			Fast Mode	0.6		
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	Standard Mode	N/A		ns
			Fast Mode	0	50	
15	C_b	Capacitive load for each bus line	Standard Mode		400	pF
			Fast Mode		400	

Table 3-27. I2C Switching Characteristics(1)

NO.	PARAMETER			MIN	MAX	UNIT
16	$t_{c(SCL)}$	Cycle time, I2Cx_SCL	Standard Mode	10		µs
			Fast Mode	2.5		
17	$t_{su(SCLH-SDAL)}$	Setup time, I2Cx_SCL high before I2Cx_SDA low	Standard Mode	4.7		µs
			Fast Mode	0.6		
18	$t_{h(SDAL-SCLL)}$	Hold time, I2Cx_SCL low after I2Cx_SDA low	Standard Mode	4		µs
			Fast Mode	0.6		

(1) I2C must be configured correctly to meet the timings in Table 3-27.

Table 3-27. I2C Switching Characteristics (continued)

NO.	PARAMETER			MIN	MAX	UNIT
19	$t_{w(SCLL)}$	Pulse duration, I2Cx_SCL low	Standard Mode	4.7		µs
			Fast Mode	1.3		
20	$t_{w(SCLH)}$	Pulse duration, I2Cx_SCL high	Standard Mode	4		µs
			Fast Mode	0.6		
21	$t_{su(SDAV-SCLH)}$	Setup time, I2Cx_SDA valid before I2Cx_SCL high	Standard Mode	250		ns
			Fast Mode	100		
22	$t_{h(SCLL-SDAV)}$	Hold time, I2Cx_SDA valid after I2Cx_SCL low	Standard Mode	0		µs
			Fast Mode	0	0.9	
23	$t_{w(SDAH)}$	Pulse duration, I2Cx_SDA high	Standard Mode	4.7		µs
			Fast Mode	1.3		
28	$t_{su(SCLH-SDAH)}$	Setup time, I2Cx_SCL high before I2Cx_SDA high	Standard Mode	4		µs
			Fast Mode	0.6		
29	C_b	Capacitive load on each bus line from this device	Standard Mode		10	pF
			Fast Mode		10	

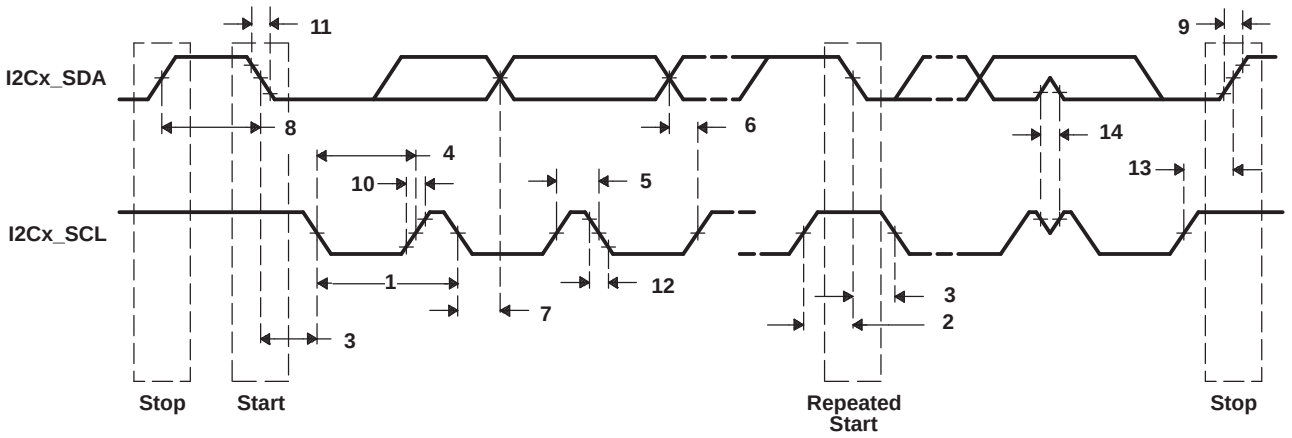


Figure 3-25. I2C Receive Timings

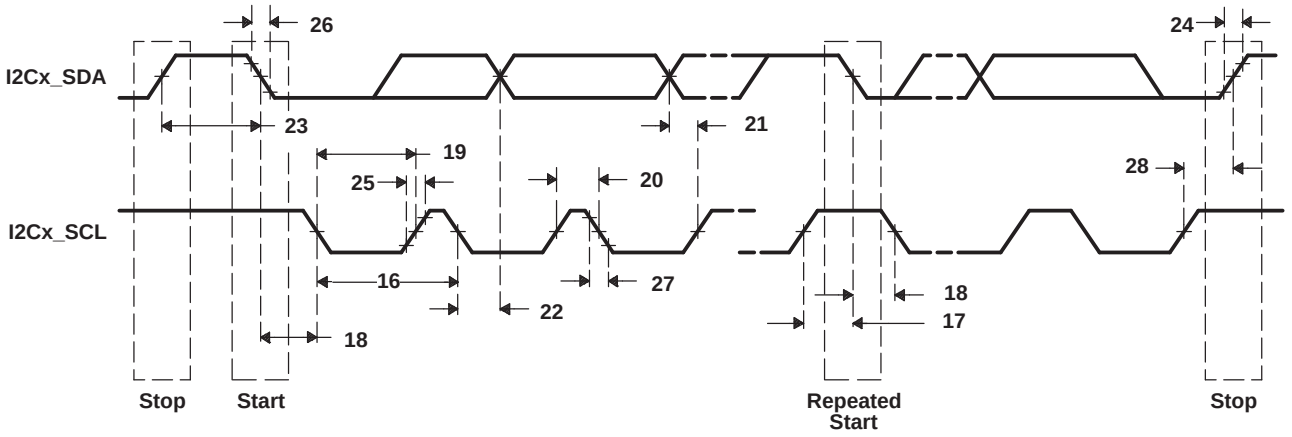


Figure 3-26. I2C Transmit Timings

3.15 Real-Time Interrupt (RTI) Timer With Digital Watchdog

3.15.1 RTI/Digital Watchdog Device-Specific Information

DA707/B/DA787B includes an RTI timer module which is used to generate periodic interrupts. This module also includes an optional digital watchdog feature. Figure 3-27 contains a block diagram of the RTI module.

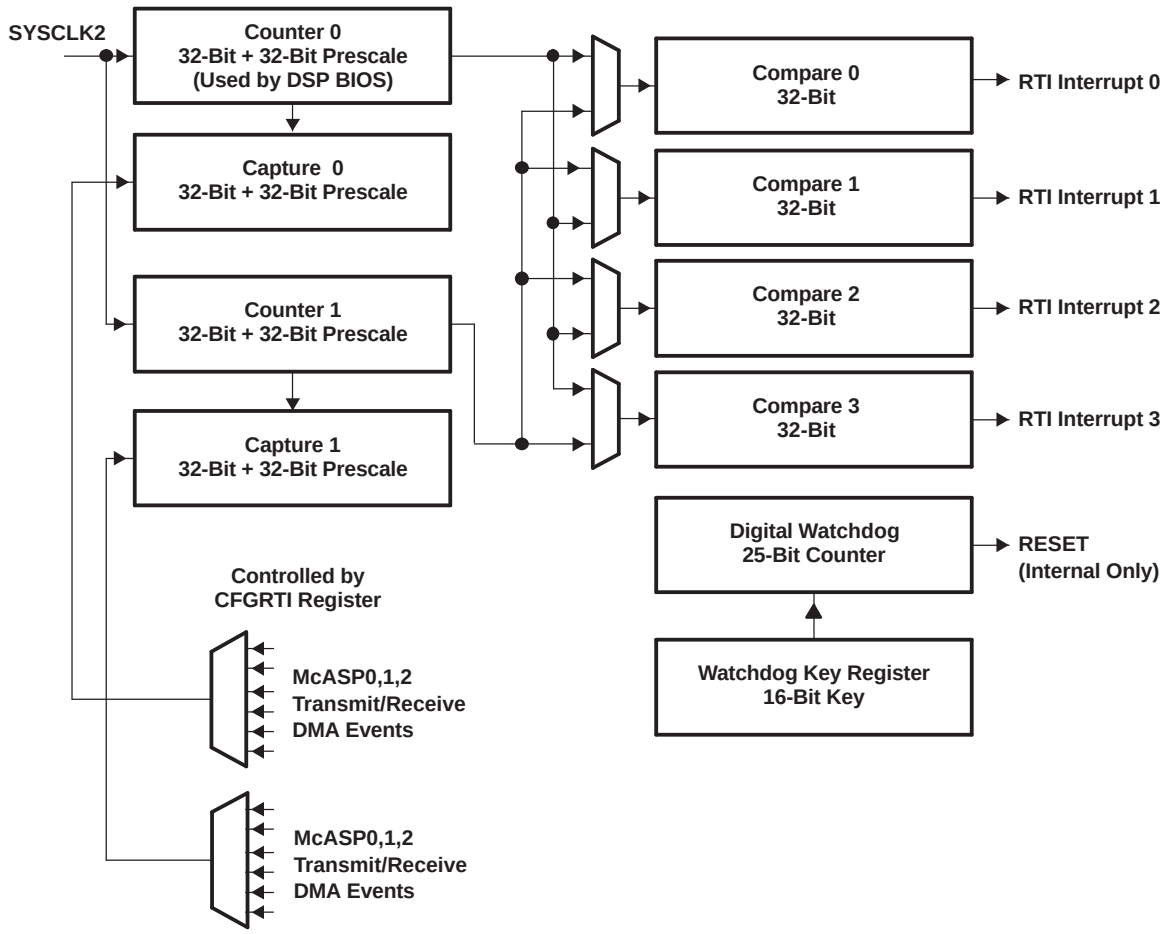


Figure 3-27. RTI Timer Block Diagram

The RTI timer module consists of two independent counters which are both clocked from SYSCLK2 (but may be started individually and may have different prescaler settings).

The counters provide the timebase against which four output comparators operate. These comparators may be programmed to generate periodic interrupts. The comparators include an adder which automatically updates the compare value after each periodic interrupt. This means that the DSP only needs to initialize the comparator once with the interrupt period.

The two input captures can be triggered from any of the McASP0, McASP1, or McASP2 DMA events. The device configuration register which selects the McASP events to measure is defined in Table 3-29.

Measuring the time difference between these events provides an accurate measure of the sample rates at which the McASPs are transmitting and receiving. This measurement can be useful as a hardware assist for a software asynchronous sample rate converter algorithm.

The digital watchdog is disabled by default. Once enabled, a sequence of two 16-bit key values (0xE51A followed by 0xA35C in two separate writes) must be continually written to the key register before the watchdog counter counts down to zero; otherwise, the DSP will be reset. This feature can be used to provide an added measure of robustness against a software failure. If the application fails and ceases to write to the watchdog key; the watchdog will respond by resetting the DSP and thereby restarting the application.

Note that Counter 0 and Compare 0 are used by DSP BIOS to generate the tick counter it requires; however, Capture 0 is still available for use by the application as well as the remaining RTI resources.

3.15.2 RTI/Digital Watchdog Registers Description(s)

Table 3-28 is a list of the RTI registers.

Table 3-28. RTI Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
Device-Level Configuration Registers Controlling RTI		
0x4000 0014	CFGRTI	Selects the sources for the RTI input captures from among the six McASP DMA event.
RTI Internal Registers		
0x4200 0000	RTIGCTRL	Global Control Register. Starts / stops the counters.
0x4200 0004	Reserved	Reserved bit.
0x4200 0008	RTICAPCTRL	Capture Control. Controls the capture source for the counters.
0x4200 000C	RTICOMPCTRL	Compare Control. Controls the source for the compare registers.
0x4200 0010	RTIFRC0	Free-Running Counter 0. Current value of free-running counter 0.
0x4200 0014	RTIUC0	Up-Counter 0. Current value of prescale counter 0.
0x4200 0018	RTICPUC0	Compare Up-Counter 0. Compare value compared with prescale counter 0.
0x4200 0020	RTICAFRC0	Capture Free-Running Counter 0. Current value of free-running counter 0 on external event.
0x4200 0024	RTICAUC0	Capture Up-Counter 0. Current value of prescale counter 0 on external event.
0x4200 0030	RTIFRC1	Free-Running Counter 1. Current value of free-running counter 1.
0x4200 0034	RTIUC1	Up-Counter 1. Current value of prescale counter 1.
0x4200 0038	RTICPUC1	Compare Up-Counter 1. Compare value compared with prescale counter 1.
0x4200 0040	RTICAFRC1	Capture Free-Running Counter 1. Current value of free-running counter 1 on external event.
0x4200 0044	RTICAUC1	Capture Up-Counter 1. Current value of prescale counter 1 on external event.
0x4200 0050	RTICOMP0	Compare 0. Compare value to be compared with the counters.
0x4200 0054	RTIUDCP0	Update Compare 0. Value to be added to the compare register 0 value on compare match.
0x4200 0058	RTICOMP1	Compare 1. Compare value to be compared with the counters.
0x4200 005C	RTIUDCP1	Update Compare 1. Value to be added to the compare register 1 value on compare match.
0x4200 0060	RTICOMP2	Compare 2. Compare value to be compared with the counters.
0x4200 0064	RTIUDCP2	Update Compare 2. Value to be added to the compare register 2 value on compare match.
0x4200 0068	RTICOMP3	Compare 3. Compare value to be compared with the counters.
0x4200 006C	RTIUDCP3	Update Compare 3. Value to be added to the compare register 3 value on compare match.
0x4200 0070	Reserved	Reserved bit.
0x4200 0074	Reserved	Reserved bit.
0x4200 0080	RTISETINT	Set Interrupt Enable. Sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.
0x4200 0084	RTICLEARINT	Clear Interrupt Enable. Clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.
0x4200 0088	RTIINTFLAG	Interrupt Flags. Interrupt pending bits.

Table 3-28. RTI Registers (continued)

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x4200 0090	RTIDWDCTRL	Digital Watchdog Control. Enables the Digital Watchdog.
0x4200 0094	RTIDWDPRLD	Digital Watchdog Preload. Sets the experation time of the Digital Watchdog.
0x4200 0098	RTIWDSTATUS	Watchdog Status. Reflects the status of Analog and Digital Watchdog.
0x4200 009C	RTIWDKEY	Watchdog Key. Correct written key values discharge the external capacitor.
0x4200 00A0	RTIDWDCNTR	Digital Watchdog Down-Counter

Figure 3-28 shows the bit layout of the CFGRTI register and Table 3-29 contains a description of the bits.

31	8
Reserved	

7	6	4	3	2	0
Reserved	CAPSEL1		Reserved	CAPSEL0	
	R/W, 0			R/W, 0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-28. CFGRTI Register Bit Layout (0x4000 0014)

Table 3-29. CFGRTI Register Bit Field Description (0x4000 0014)

BIT NO.	NAME	RESET VALUE	READ WRITE	DESCRIPTION
31:7,3	Reserved	N/A	N/A	Reads are indeterminate. Only 0s should be written to these bits.
6:4	CAPSEL1	0	R/W	CAPSEL0 selects the input to the RTI Input Capture 0 function. CAPSEL1 selects the input to the RTI Input Capture 1 function. The encoding is the same for both fields: 000 = Select McASP0 Transmit DMA Event 001 = Select McASP0 Receive DMA Event 010 = Select McASP1 Transmit DMA Event 011 = Select McASP1 Receive DMA Event 100 = Select McASP2 Transmit DMA Event 101 = Reserved Other values are reserved and their effect is not determined.
2:0	CAPSEL0	0	R/W	

3.16 External Clock Input From Oscillator or CLKIN Pin

The DA707/B/DA787B device includes two choices to provide an external clock input, which is fed to the on-chip PLL to generate high-frequency system clocks. These options are illustrated in Figure 3-29.

- Figure 3-29 (a) illustrates the option that uses an on-chip 1.2-V oscillator with external crystal circuit.
- Figure 3-29 (b) illustrates the option that uses an external 3.3-V LVCMOS-compatible clock input with the CLKIN pin .

Note that the two clock inputs are logically combined internally before the PLL so the clock input that is not used must be tied to ground.

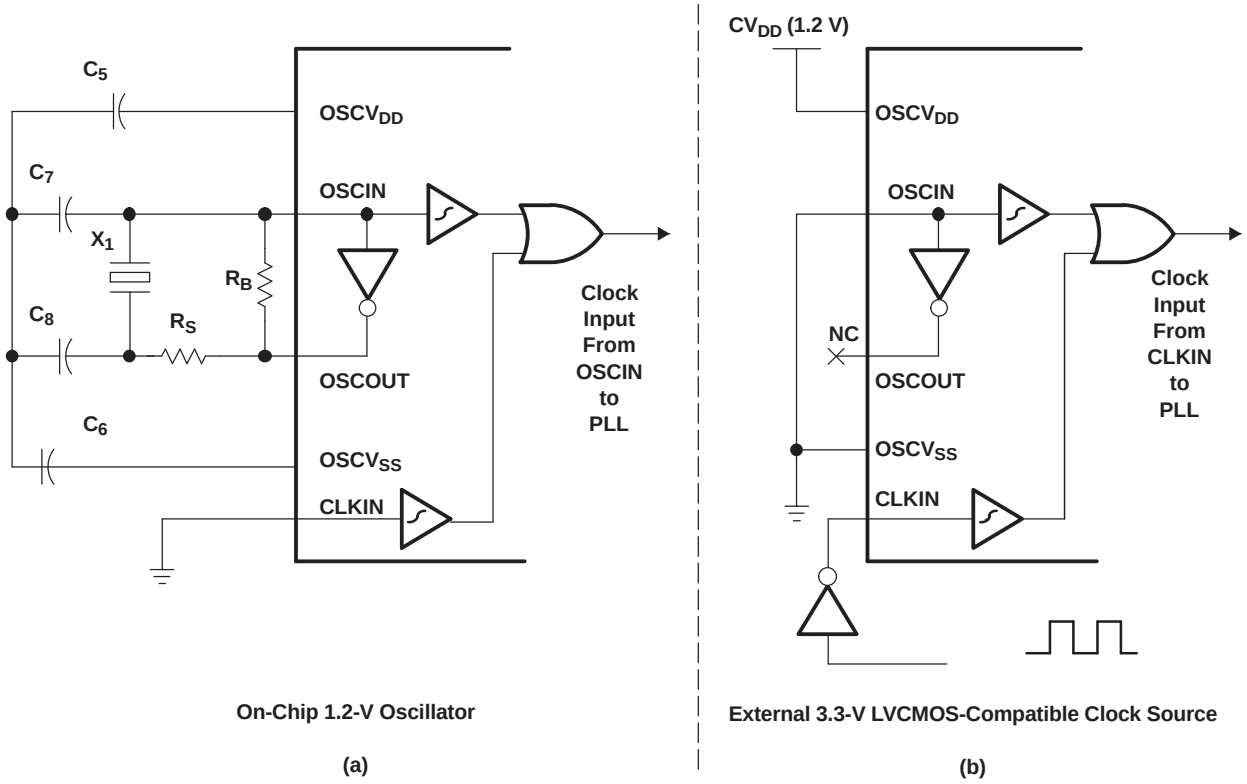


Figure 3-29. DA707/B/DA787B Clock Input Options

If the on-chip oscillator is chosen, then the recommended component values for Figure 3-29 (a) are listed in Table 3-30.

Table 3-30. Recommended On-Chip Oscillator Components

FREQUENCY	XTAL TYPE	X_1	C_5 (1)	C_6 (1)	C_7	C_8	R_B	R_S
22.579	AT-49	KDS 1AF225796A	470 pF	470 pF	8 pF	8 pF	1 MΩ	0 Ω
22.579	SMD-49	KDS 1AS225796AG	470 pF	470 pF	8 pF	8 pF	1 MΩ	0 Ω
24.576	AT-49	KDS 1AF245766AAA	470 pF	470 pF	8 pF	8 pF	1 MΩ	0 Ω
24.576	SMD-49	KDS 1AS245766AHA	470 pF	470 pF	8 pF	8 pF	1 MΩ	0 Ω

(1) Capacitors C_5 and C_6 are used to reduce oscillator jitter, but are optional. If C_5 and C_6 are not used, then the node connecting capacitors C_7 and C_8 should be tied to $OSCV_{SS}$ and $OSCV_{DD}$ should be tied to CV_{DD}.

3.16.1 Clock Electrical Data/Timing

Table 3-31 assumes testing over recommended operating conditions.

Table 3-31. CLKIN Timing Requirements

NO.			MIN	MAX	UNIT
1	f_{osc}	Oscillator frequency range (OSCIN/OSCOUT)	12	25	MHz
2	$t_{c(CLKIN)}$	Cycle time, external clock driven on CLKIN	20		ns
3	$t_{w(CLKINH)}$	Pulse width, CLKIN high	$0.4t_{c(CLKIN)}$		ns
4	$t_{w(CLKINL)}$	Pulse width, CLKIN low	$0.4t_{c(CLKIN)}$		ns
5	$t_{t(CLKIN)}$	Transition time, CLKIN		5	ns
6	f_{PLL}	Frequency range of PLL input	12	50	MHz

3.17 Phase-Locked Loop (PLL)

3.17.1 PLL Device-Specific Information

The DA707/B/DA787B DSP generates the high-frequency internal clocks it requires through an on-chip PLL.

The input to the PLL is either from the on-chip oscillator (OSCIN pin) or from an external clock on the CLKIN pin. The PLL outputs four clocks that have programmable divider options. Figure 3-30 illustrates the PLL Topology.

The PLL is disabled by default after a device reset. It must be configured by software according to the allowable operating conditions listed in Table 3-32 before enabling the DSP to run from the PLL by setting PLLEN = 1.

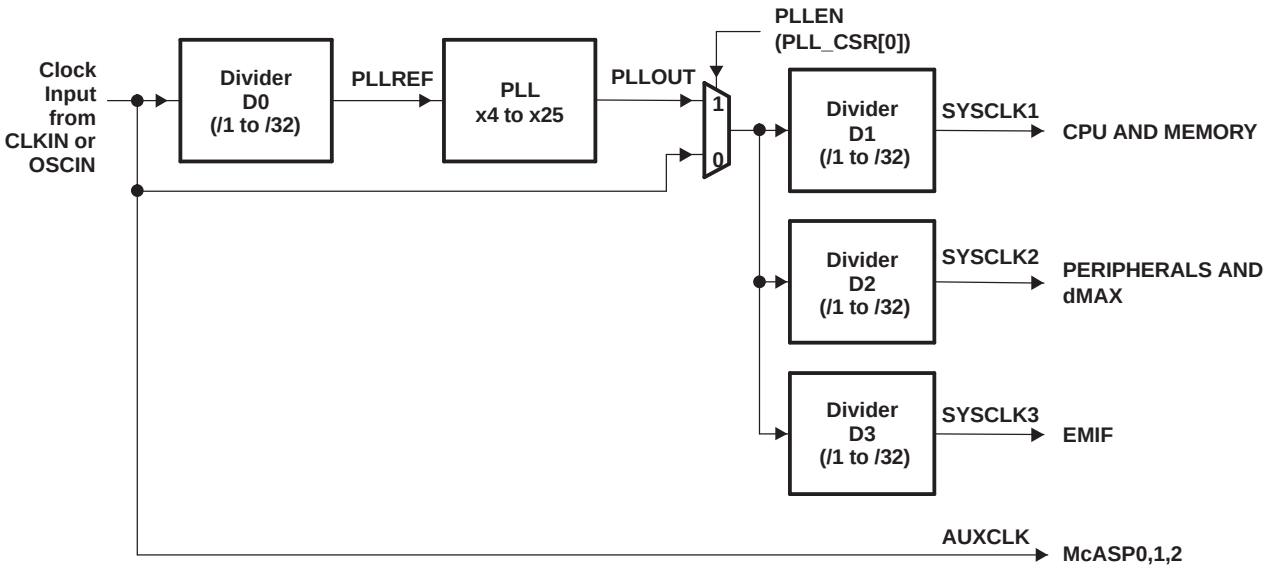


Figure 3-30. PLL Topology

Table 3-32. Allowed PLL Operating Conditions

	PARAMETER	DEFAULT VALUE	ALLOWED SETTING OR RANGE	
			MIN	MAX
1	PLLRST = 1 assertion time during initialization	N/A	125 ns	
2	Lock time before setting PLLEN = 1. After changing D0, PLLM, or input clock.	N/A	187.5 µs	
3	PLL input frequency (PLLREF after D0(1))		12 MHz	50 MHz
4	PLL multiplier values (PLLM)	x13	x4	x25
5	PLL output frequency (PLLOUT before dividers D1, D2, D3)(2)	N/A	140 MHz	600 MHz
6	SYSCLK1 frequency (set by PLLM and dividers D0, D1)	PLLOUT/1		Device Frequency Specification
7	SYSCLK2 frequency (set by PLLM and dividers D0, D2)	PLLOUT/2	/2, /3, or /4 of SYSCLK1	
8	SYSCLK3 frequency (set by PLLM and dividers D0, D3)	PLLOUT/3		EMIF Frequency Specification

(1) Some values for the D0 divider produce results outside of this range and should not be selected.
(2) In general, selecting the PLL output clock rate closest to the maximum frequency will decrease clock jitter.

CAUTION

SYSCLK1, SYSCLK2, SYSCLK3 must be configured as aligned by setting ALNCTL[2:0] to '1'; and the PLLCMD.GOSET bit must be written every time the dividers D1, D2, and D3 are changed in order to make sure the change takes effect and preserves alignment.

CAUTION

When changing the PLL parameters which affect the SYSCLK1, SYSCLK2, SYSCLK3 dividers, the bridge BR2 in Figure 2-6 must be reset by the CFGBRIDGE register. See Table 2-8.

The PLL is an analog circuit and is sensitive to power supply noise. Therefore it has a dedicated 3.3-V power pin (PLLHV) that should be connected to DV_{DD} at the board level through an external filter, as illustrated in Figure 3-31.

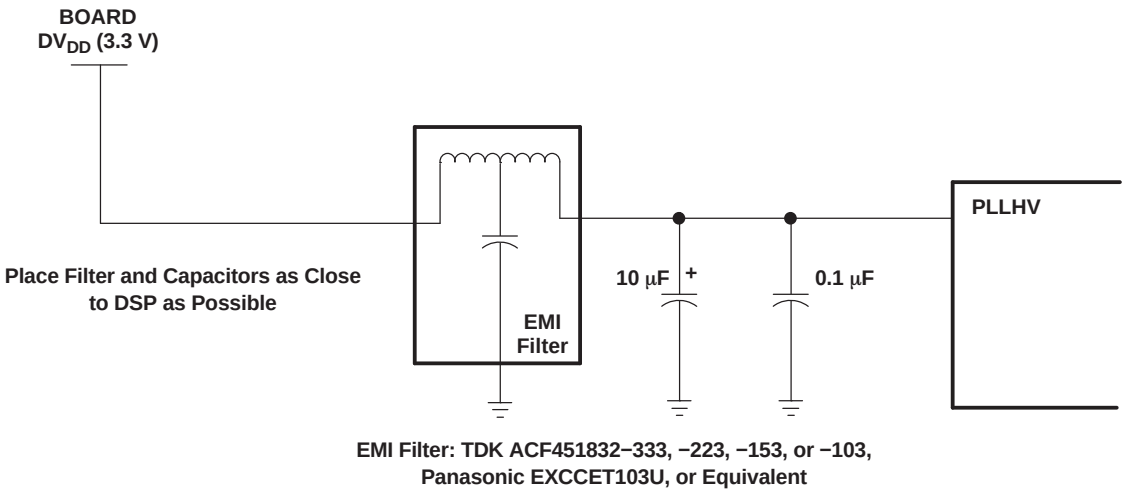


Figure 3-31. PLL Power Supply Filter

3.17.2 PLL Registers Description(s)

Table 3-33 is a list of the PLL registers. For more information about these registers, see the *TMS320C672x DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide* (literature number SPRU879).

Table 3-33. PLL Controller Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION
0x4100 0000	PLLPID	PLL controller peripheral identification register
0x4100 0100	PLLCSR	PLL control/status register
0x4100 0110	PLLM	PLL multiplier control register
0x4100 0114	PLLDIV0	PLL controller divider register 0
0x4100 0118	PLLDIV1	PLL controller divider register 1
0x4100 011C	PLLDIV2	PLL controller divider register 2
0x4100 0120	PLLDIV3	PLL controller divider register 3
0x4100 0138	PLLCMD	PLL controller command register
0x4100 013C	PLLSTAT	PLL controller status register
0x4100 0140	ALNCTL	PLL controller clock align control register
0x4100 0148	CKEN	Clock enable control register
0x4100 014C	CKSTAT	Clock status register
0x4100 0150	SYSTAT	SYSCLK status register

3.18 Device Configuration Registers

The DA707/B/DA787B DSP includes several device-level configuration registers, which are listed in Table 3-34. These registers need to be programmed as part of the device initialization procedure. See Section 3.20.

Table 3-34. Device-Level Configuration Registers

BYTE ADDRESS	REGISTER NAME	DESCRIPTION	DEFINED
0x4000 0000	CFGPIN0	Captures values of eight pins on rising edge of $\overline{\text{RESET}}$ pin.	Table 3-35
0x4000 0004	CFGPIN1	Captures values of eight pins on rising edge of $\overline{\text{RESET}}$ pin.	Table 3-36
0x4000 0008	Reserved	Do not write to these locations.	
0x4000 000C	Reserved		
0x4000 0010	Reserved		
0x4000 0014	CFGRTI	Selects the sources for the RTI Input Captures from among the six McASP DMA events.	Table 3-29
0x4000 0018	CFGMCASP0	Selects the peripheral pin to be used as AMUTEIN0.	Table 3-11
0x4000 001C	CFGMCASP1	Selects the peripheral pin to be used as AMUTEIN1.	Table 3-12
0x4000 0020	CFGMCASP2	Selects the peripheral pin to be used as AMUTEIN2.	Table 3-13
0x4000 0024	CFGBRIDGE	Controls reset of the bridge BR2 in Figure 2-6. This bridge must be reset explicitly after any change to the PLL controller affecting SYSCLK1 and SYSCLK2 and before the dMAX accesses the CPU Slave Port (CSP).	Table 2-8

3.19 Device Boot Modes

The DA707/B/DA787B DSP supports only one hardware bootmode option, this is to boot from the internal ROM starting at address 0x0000 0000. Other bootmode options are implemented by a software bootloader stored in ROM. The software bootloader can use CFGPIN0 and CFGPIN1 registers to determine which mode to enter. Note that in practice, only a few pins are used by the software.

CAUTION

Only an externally applied $\overline{\text{RESET}}$ causes the CFGPIN0 and CFGPIN1 registers to recapture their associated pin values. An emulator reset or an RTI reset does not cause these registers to update.

Typically, the ROM bootmodes will include:

- Asynchronous memory on $\overline{\text{EM\_CS}}$[2]
- SPI0 or I2C1 master mode from serial EEPROM
- SPI0 or I2C1 slave mode from external MCU

Refer to the *D710E001 Aureus TMS320DA7xx Floating-Point Digital Signal Processor ROM Data Manual* (literature number SPRS278) for details on supported bootmodes and their implementation.

Figure 3-32 shows the bit layout of the CFGPIN0 register and Table 3-35 contains a description of the bits.

31							8
Reserved							

7	6	5	4	3	2	1	0
PINCAP7	PINCAP6	PINCAP5	PINCAP4	PINCAP3	PINCAP2	PINCAP1	PINCAP0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-32. CFGPIN0 Register Bit Layout (0x4000 0000)

Table 3-35. CFGPIN0 Register Bit Field Description (0x4000 0000)

BIT NO.	NAME	DESCRIPTION
31:8	Reserved	Reads are indeterminate. Only 0s should be written to these bits.
7	PINCAP7	SPI0_SOMI/I2C0_SDA pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
6	PINCAP6	SPI0_SIMO pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
5	PINCAP5	SPI0_CLK/I2C0_SCL pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
4	PINCAP4	$\overline{\text{SPI0\_SCS}}$/I2C1_SCL pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
3	PINCAP3	$\overline{\text{SPI0\_ENA}}$/I2C1_SDA pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
2	PINCAP2	AXR0[8]/AXR1[5]/SPI1_SOMI pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
1	PINCAP1	AXR0[9]/AXR1[4]/SPI1_SIMO pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
0	PINCAP0	AXR0[7]/SPI1_CLK pin state captured on rising edge of $\overline{\text{RESET}}$ pin.

Figure 3-33 shows the bit layout of the CFGPIN1 register and Table 3-36 contains a description of the bits.

31							8
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PINCAP15	PINCAP14	Reserved	Reserved	Reserved	PINCAP10	PINCAP9	PINCAP8

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Figure 3-33. CFGPIN1 Register Bit Layout (0x4000 0004)

Table 3-36. CFGPIN1 Register Bit Field Description (0x4000 0004)

BIT NO.	NAME	DESCRIPTION
31:8	Reserved	Reads are indeterminate. Only 0s should be written to these bits.
7	PINCAP15	AXR0[5]/$\overline{\text{SPI1\_SCS}}$ pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
6	PINCAP14	AXR0[6]/$\overline{\text{SPI1\_ENA}}$ pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
5	Reserved	Reserved
4	Reserved	Reserved
3	Reserved	Reserved
2	PINCAP10	AFSX0 pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
1	PINCAP9	AFSR0 pin state captured on rising edge of $\overline{\text{RESET}}$ pin.
0	PINCAP8	AXR0[0] pin state captured on rising edge of $\overline{\text{RESET}}$ pin.

3.20 Peripheral Pin Multiplexing Options

This section describes the options for configuring peripherals which share pins on the DA707/B/DA787B DSP. See Section 3.21 for configuration examples.

Table 3-37 lists the options for configuring the SPI0, I2C0, and I2C1 peripheral pins.

Table 3-37. Options for Configuring SPI0, I2C0, and I2C1

		CONFIGURATION		
		OPTION 1	**OPTION 2**	**OPTION 3**
PERIPHERAL	SPI0	3-, 4-, or 5-pin mode	3-pin mode	disabled
	I2C0	disabled	disabled	enabled
	I2C1	disabled	enabled	enabled
PINS	SPI0_SOMI/I2C0_SDA	SPI0_SOMI	SPI0_SOMI	I2C0_SDA
	SPI0_SIMO	SPI0_SIMO	SPI0_SIMO	GPIO through SPI0_SIMO pin control
	SPI0_CLK/I2C0_SCL	SPI0_CLK	SPI0_CLK	I2C0_SCL
	$\overline{\text{SPI0\_SCS}}$/I2C1_SCL	$\overline{\text{SPI0\_SCS}}$	I2C1_SCL	I2C1_SCL
	$\overline{\text{SPI0\_ENA}}$/I2C1_SDA	$\overline{\text{SPI0\_ENA}}$	I2C1_SDA	I2C1_SDA

Table 3-38 lists the options for configuring the SPI1, McASP0, and McASP1 pins. Note that there are additional finer grain options when selecting which McASP controls the particular AXR serial data pins but these options are not listed here and can be made on a pin by pin basis.

Table 3-38. Options for Configuring SPI1, McASP0, and McASP1 Data Pins

		CONFIGURATION				
		OPTION 1	**OPTION 2**	**OPTION 3**	**OPTION 4**	**OPTION 5**
PERIPHERAL	SPI1	5-pin mode	4-pin mode	4-pin mode	3-pin mode	disabled
	McASP0 (max data pins)	11	12	12	13	16
	McASP1 (max data pins)	4	4	4	4	6
PINS	AXR0[5]/ $\overline{\text{SPI1\_SCS}}$	$\overline{\text{SPI1\_SCS}}$	$\overline{\text{SPI1\_SCS}}$	AXR0[5]	AXR0[5]	AXR0[5]
	AXR0[6]/ $\overline{\text{SPI1\_ENA}}$	$\overline{\text{SPI1\_ENA}}$	AXR0[6]	$\overline{\text{SPI1\_ENA}}$	AXR0[6]	AXR0[6]
	AXR0[7]/ SPI1_CLK	SPI1_CLK	SPI1_CLK	SPI1_CLK	SPI1_CLK	AXR0[7]
	AXR0[8]/AXR1[5]/ SPI1_SOMI	SPI1_SOMI	SPI1_SOMI	SPI1_SOMI	SPI1_SOMI	AXR0[8] ***or*** AXR1[5]
	AXR0[9]/AXR1[4]/ SPI1_SIMO	SPI1_SIMO	SPI1_SIMO	SPI1_SIMO	SPI1_SIMO	AXR0[9] ***or*** AXR1[4]

3.21 Configuration Examples

Figure 3-34 to Figure 3-36 show the different ways in which the DA707/B/DA787B device can be configured.

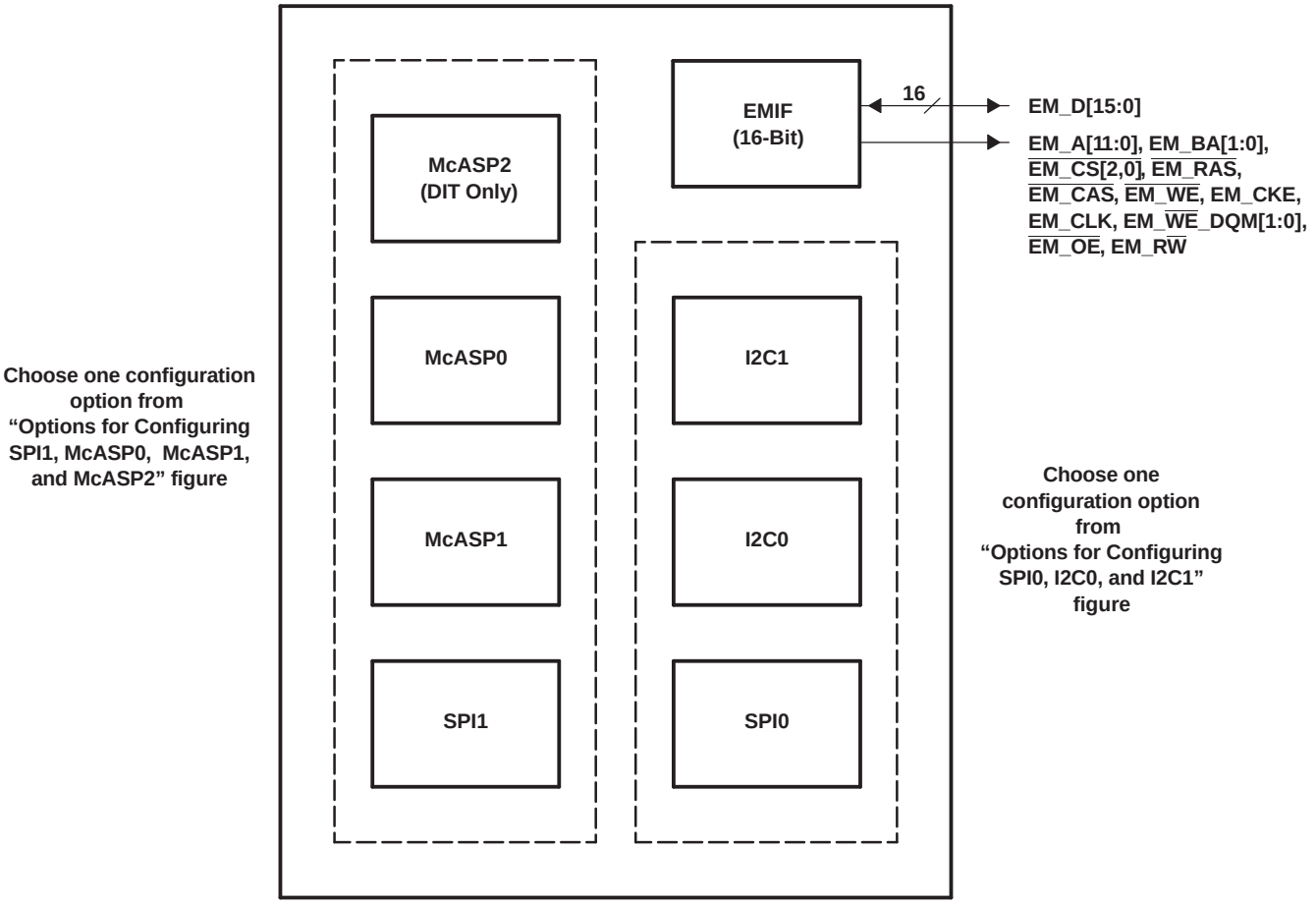


Figure 3-34. Configuration Example

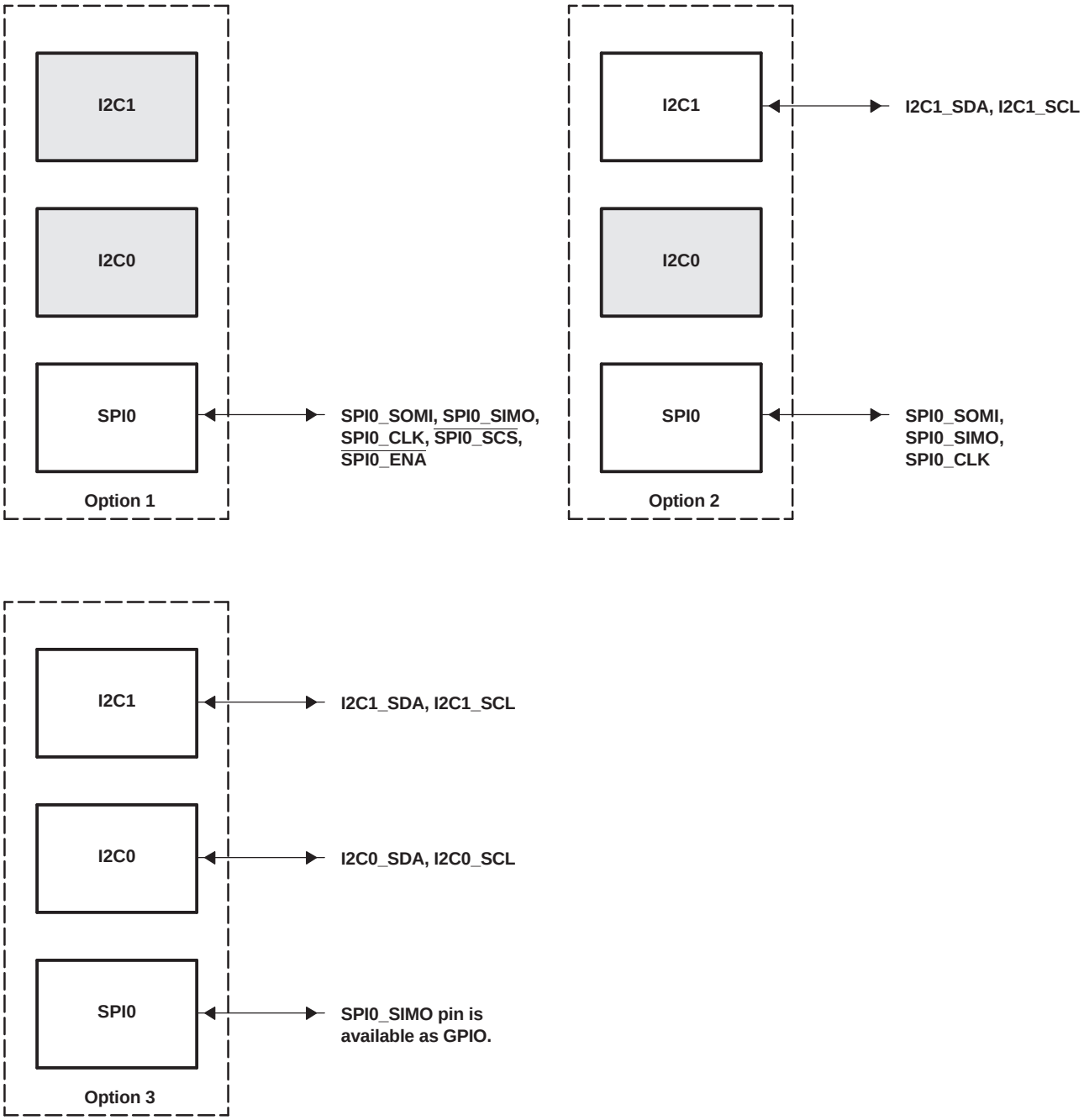
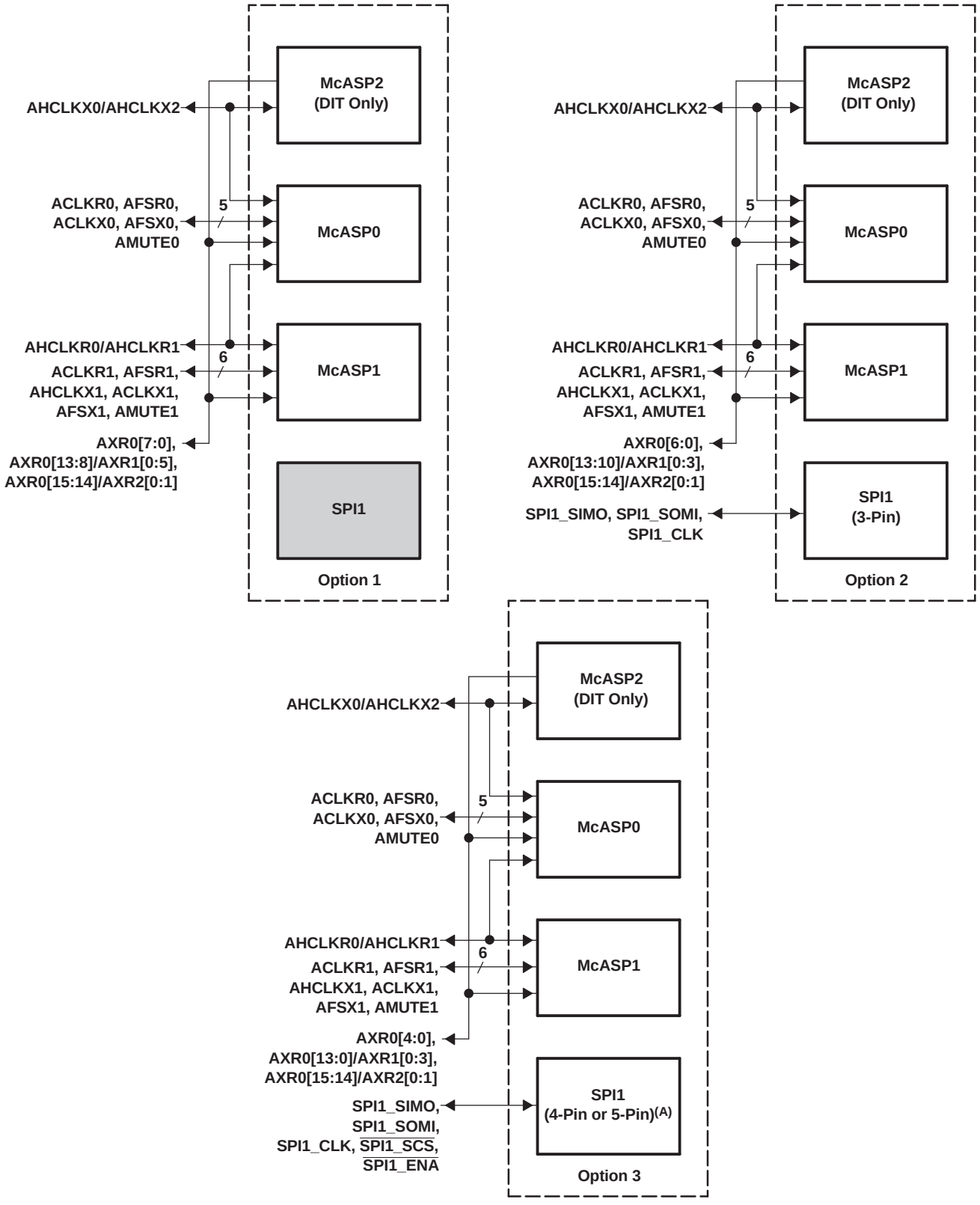


Figure 3-35. Options for Configuring SPI0, I2C0, and I2C1 (see Table 3-37)



NOTE A: For SPI1 in 4-pin chip-select mode, AXR0[6] is available as a McASP0 pin.
For SPI1 in 4-pin enable mode, AXR0[5] is available as a McASP0 pin. These are omitted from this diagram for simplicity.

Figure 3-36. Options for Configuring SPI1, McASP0, McASP1, and McASP2 (see Table 3-38)

3.22 Peripheral Pin Multiplexing Control

While Section 3.20 describes at a high level the most common pin multiplexing options, the control of pin multiplexing is largely determined on an individual pin-by-pin basis. Typically, each peripheral that shares a particular pin has internal control registers to determine the pin function and whether it is an input or an output.

The DA707/B/DA787B device determines whether a particular pin is an input or output based upon the following rules:

- The pin will be configured as an output if it is configured as an output in any of the peripherals sharing the pin.
- It is recommended that only one peripheral configure a given pin as an output. If more than one peripheral does configure a particular pin as an output, then the output value is controlled by the peripheral with highest priority for that pin. The priorities for each pin are given in Table 3-39.
- The value input on the pin is passed to all peripherals sharing the pin for input simultaneously.

Table 3-39. Priority of Control of Data Output on Multiplexed Pins

PIN	FIRST PRIORITY	SECOND PRIORITY	THIRD PRIORITY
SPI0_SOMI/I2C0_SDA	SPI0_SOMI	I2C0_SDA	
SPI0_CLK/I2C0_SCL	SPI0_CLK	I2C0_SCL	
$\overline{\text{SPI0\_SCS}}$/I2C1_SCL	$\overline{\text{SPI0\_SCS}}$	I2C1_SCL	
$\overline{\text{SPI0\_ENA}}$/I2C1_SDA	$\overline{\text{SPI0\_ENA}}$	I2C1_SDA	
AXR0[5]/$\overline{\text{SPI1\_SCS}}$	AXR0[5]	$\overline{\text{SPI1\_SCS}}$	
AXR0[6]/$\overline{\text{SPI1\_ENA}}$	AXR0[6]	$\overline{\text{SPI1\_ENA}}$	
AXR0[7]/SPI1_CLK	AXR0[7]	SPI1_CLK	
AXR0[8]/AXR1[5]/SPI1_SOMI	AXR0[8]	AXR1[5]	SPI1_SOMI
AXR0[9]/AXR1[4]/SPI1_SIMO	AXR0[9]	AXR1[4]	SPI1_SIMO
AXR0[10]/AXR1[3]	AXR0[10]	AXR1[3]	
AXR0[11]/AXR1[2]	AXR0[11]	AXR1[2]	
AXR0[12]/AXR1[1]	AXR0[12]	AXR1[1]	
AXR0[13]/AXR1[0]	AXR0[13]	AXR1[0]	
AXR0[14]/AXR2[1]	AXR0[14]	AXR2[1]	
AXR0[15]/AXR2[0]	AXR0[15]	AXR2[0]	
AHCLKR0/AHCLKR1	AHCLKR0	AHCLKR1	
AHCLKX0/AHCLKX2	AHCLKX0	AHCLKX2	

4 Development

4.1 Development Support

TI offers an extensive line of development tools for the TMS320C6000™ DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of C6000™ DSP-based applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator (supports C6000™ DSP multiprocessor system debug) EVM (Evaluation Module)

For a complete listing of development-support tools for the TMS320C6000™ DSP platform, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

4.2 Device Support

4.2.1 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320C6412GDK600). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX / TMDX) through fully qualified production devices/tools (TMS / TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully-qualified production device

Support tool development evolutionary flow:

TMDX Development support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

4.2.2 Documentation Support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data manuals, such as this document, with design specifications; complete user's reference guides for all devices and tools; technical briefs; development-support tools; on-line help; and hardware and software applications. The following is a brief, descriptive list of support documentation specific to the DA707/B/DA787B DSP devices:

SPRS278: D710E001 Aureus TMS320DA7xx Floating-Point Digital Signal Processor ROM Data Manual. This document describes the ROM of the TMS320DA7xx digital signal processor.

SPRZ237: TMS320DA707, TMS320DA707B Digital Signal Processors Silicon Errata. This document describes the known exceptions to the functional specifications for the TMS320DA707 and TMS320DA707B digital signal processors (DSPs).

SPRU877: TMS320C672x DSP Inter-Integrated Circuit (I2C) Module. This document describes the inter-integrated circuit (I2C) module in the TMS320C672x digital signal processors (DSPs) of the TMS320C6000™ DSP family.

SPRU795: TMS320C672x DSP Dual Data Movement Accelerator (dMAX). This document provides an overview and describes the common operation of the data movement accelerator (dMAX) controller in the digital signal processors (DSPs) of the TMS320C672x DSP family. This document also describes operations and registers unique to the dMAX controller.

SPRAA77: Migrating from TMS320DA6xx to TMS320DA7xx Aureus DSP. This document describes the issues related to migrating from the first generation TMS320DA6xx to the second generation TMS320DA7xx Aureus floating-point digital signal processors (DSPs).

SPRU733: TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide. Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C67x and TMS320C67x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C67x/C67x+ DSP generation comprises floating-point devices in the C6000 DSP platform. The C67x+ DSP is an enhancement of the C67x DSP with added functionality and an expanded instruction set.

SPRU711: TMS320C672x DSP External Memory Interface (EMIF) User's Guide. This document describes the operation of the external memory interface (EMIF) in the TMS320C672x™ digital signal processors (DSPs) of the TMS320C6000™ family.

SPRU718: TMS320C672x DSP Serial Peripheral Interface (SPI) Reference Guide. This reference guide provides the specifications for a 16-bit configurable, synchronous serial peripheral interface. The SPI is a programmable-length shift register, used for high speed communication between external peripherals or other DSPs.

SPRU719: TMS320C672x DSP Universal Host Port Interface (UHPI) Reference Guide. This document provides an overview and describes the common operation of the universal host port interface (UHPI).

SPRU878: TMS320C672x DSP Multichannel Audio Serial Port (McASP) Reference Guide. This document describes the multichannel audio serial port (McASP) in the TMS320C672x™ digital signal processors (DSPs) of the TMS320C6000™ DSP family.

SPRU879: TMS320C672x DSP Software-Programmable Phase-Locked Loop (PLL) Controller Reference Guide. This document describes the operation of the software-programmable phase-locked loop (PLL) controller in the TMS320C672x™ digital signal processors (DSPs) of the TMS320C6000™ DSP family.

SPRU301: TMS320C6000 Code Composer Studio Tutorial. This tutorial introduces you to some of the key features of Code Composer Studio. Code Composer Studio extends the capabilities of the Code Composer Integrated Development Environment (IDE) to include full awareness of the DSP target by the host and real-time analysis tools. This tutorial assumes that you have Code Composer Studio, which includes the TMS320C6000 code generation tools along with the APIs and plug-ins for both DSP/BIOS and RTDX. This manual also assumes that you have installed a target board in your PC containing the DSP device.

SPRU198: TMS320C6000 Programmer's Guide. Reference for programming the TMS320C6000 digital signal processors (DSPs). Before you use this manual, you should install your code generation and debugging tools. Includes a brief description of the C6000 DSP architecture and code development flow, includes C code examples and discusses optimization methods for the C code, describes the structure of assembly code and includes examples and discusses optimizations for the assembly code, and describes programming considerations for the C64x DSP.

SPRU186: TMS320C6000 Assembly Language Tools v6.0 Beta User's Guide. Describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C6000 platform of devices (including the C64x+ and C67x+ generations). **NOTE: The enhancements to tools release v5.3 to support the DA707 device are documented in the tools v6.0 documentation.**

SPRU187: TMS320C6000 Optimizing Compiler v6.0 Beta User's Guide. Describes the TMS320C6000 C compiler and the assembly optimizer. This C compiler accepts ANSI standard C source code and produces assembly language source code for the TMS320C6000 platform of devices (including the C64x+ and C67x+ generations). The assembly optimizer helps you optimize your assembly code. **NOTE: The enhancements to tools release v5.3 to support the DA707 device are documented in the tools v6.0 documentation.**

SPRA839: Using IBIS Models for Timing Analysis. Describes how to properly use IBIS models to attain accurate timing analysis for a given system.

The tools support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE). For a complete listing of C6000™ DSP latest documentation, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL).

5 Mechanical Data

5.1 Package Thermal Resistance Characteristics

Table 5-1 provides the thermal characteristics for the recommended package types used on the TMS320DA707/B/TMS320DA787B DSP.

Table 5-1. Thermal Characteristics for RFP Package

NO.			THERMAL PAD CONFIGURATION			°C/W	AIR FLOW (m/s)
			TOP	BOTTOM	VIA ARRAY		
Two-Signal, Two-Plane, 76.2 x 76.2 mm PCB(1)(2)(3)							
1	$R\theta_{JA}$	Thermal Resistance Junction to Ambient	10.6 x 10.6 mm	10.6 x 10.6 mm	6 x 6	20	0
			7.5 x 7.5 mm	7.5 x 7.5 mm	5 x 5	22	0
2	Ψ_{JP}	Thermal Metric Junction to Power Pad	10.6 x 10.6 mm	10.6 x 10.6 mm	6 x 6	0.39	0
Double-Sided 76.2 x 76.2 mm PCB(1)(2)(4)							
3	$R\theta_{JA}$	Thermal Resistance Junction to Ambient	10.6 x 10.6 mm	10.6 x 10.6 mm	6 x 6	49	0
			10.6 x 10.6 mm	38.1 x 38.1 mm	6 x 6	27	0
			10.6 x 10.6 mm	57.2 x 57 mm	6 x 6	22	0
			10.6 x 10.6 mm	76.2 x 76.2 mm	6 x 6	20	0
4	Ψ_{JP}	Thermal Metric Junction to Power Pad	10.6 x 10.6 mm	10.6 x 10.6 mm	6 x 6	0.39	0

(1) PCB modeled with 2 oz/ft^2 Top and Bottom Cu.
(2) Package thermal pad must be properly soldered to top layer PCB thermal pad for both thermal and electrical performance. Thermal pad is V_{SS}.
(3) Top layer thermal pad is connected through via array to both bottom layer thermal pad and internal V_{SS} plane.
(4) Top layer thermal pad is connected through via array to bottom layer thermal pad.

5.2 Packaging Information

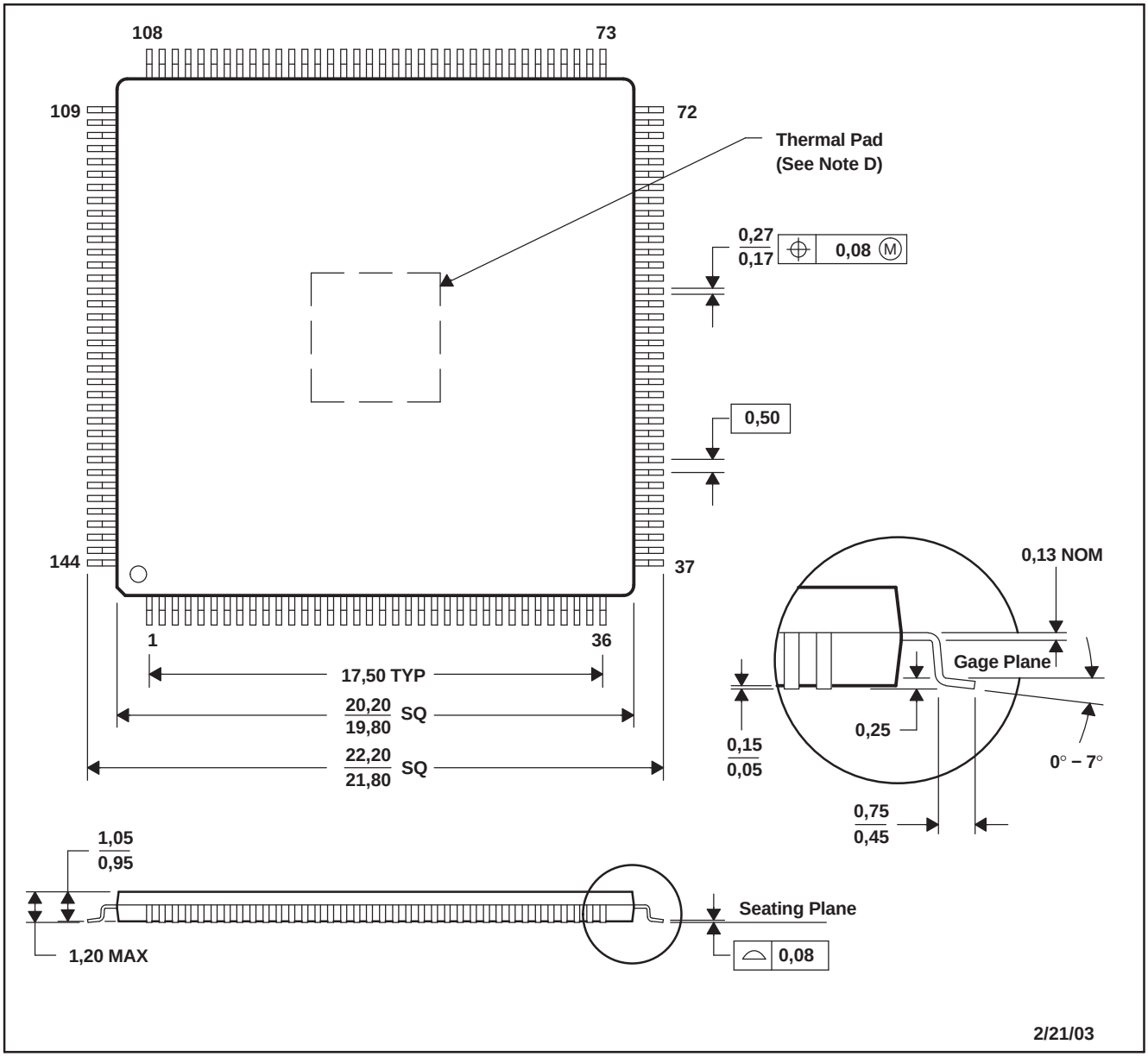
Table 5-2. Orderable Part Numbers

ORDERABLE PART NUMBER(1)	PACKAGE	CPU SPEED	SDRAM SPEED	CORE SUPPLY	I/O SUPPLY	OPERATING AMBIENT TEMPERATURE RANGE
D707yxxxRFP250	144 RFP	250 MHz	100 MHz	1.2 V	3.3 V	0°C to 70°C
D707yxxxRFPA250	144 RFP	250 MHz	100 MHz	1.2 V	3.3 V	–40°C to 85°C
D707yxxxBRFP250	144 RFP	250 MHz	100 MHz	1.2 V	3.3 V	0°C to 70°C
D707yxxxBRFPA250	144 RFP	250 MHz	100 MHz	1.2 V	3.3 V	–40°C to 85°C
D787yxxxBRFP250	144 RFP	250 MHz	100 MHz	1.2 V	3.3 V	0°C to 70°C
D787yxxxBRFPA250	144 RFP	250 MHz	100 MHz	1.2 V	3.3 V	–40°C to 85°C

(1) Part Number Nomenclature:
D707 = Base Part Number (DA707) [This device should ***not*** be used for applications with DTS IP]
D787 = Base Part Number (DA787B) [This device should be used for applications with DTS IP]
y = ROM image identifier
xxx = ROM image revision number
B = Silicon Revision 1.2 , blank = Silicon Revision 1.1
RFP = PowerPAD™ Package Designator
A = Automotive Temperature Range, blank = Commercial Temperature Range
250 = CPU Frequency (MHz)

5.3 PowerPAD™ Plastic Quad Flatpack Mechanical Data Drawing (RFP)

DA707/B/DA787B Device-Specific RFP (S-PQFP-G144) PowerPAD™ PLASTIC QUAD FLATPACK



A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion.

D. The package thermal performance may be enhanced by bonding the thermal pad to an external plane. This pad is electronically and thermally connected to the backside of the die and possibly selected leads. Actual size: 5.4 mm × 5.4 mm.

E. Falls within JEDEC MS-026.

5.3.1 Supplementary Information About the 144-Pin RFP PowerPAD™ Package

This section highlights a few important details about the 144-pin RFP PowerPAD™ package. Texas Instruments' PowerPAD Thermally Enhanced Package Technical Brief (literature number SLMA002) should be consulted before designing a PCB for this device.

5.3.1.1 Standoff Height

As illustrated in Figure 5-1, the standoff height specification for this device (between 0.050 mm and 0.150 mm) is measured from the seating plane established by the three lowest package pins to the **lowest** point on the package body. Due to warpage, the lowest point on the package body is located in the center of the package at the exposed thermal pad.

Using this definition of standoff height provides the correct result for determining the correct solder paste thickness. According to TI's PowerPAD Thermally Enhanced Package Technical Brief (literature number SLMA002), the recommended range of solder paste thickness for this package is between 0.152 mm and 0.178 mm.

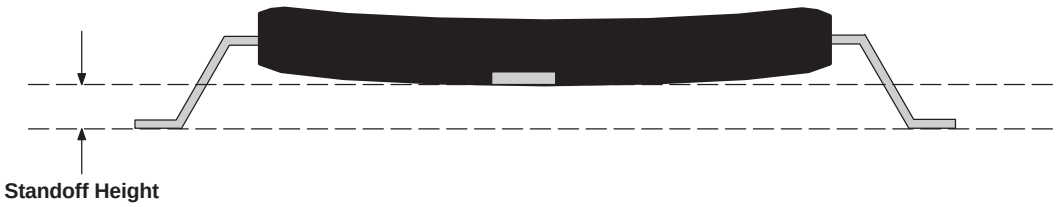


Figure 5-1. Standoff Height Measurement on 144-Pin RFP Package

5.3.1.2 PowerPAD™ PCB Footprint

In general, for proper thermal performance, the thermal pad under the package body should be as large as possible. However, the soldermask opening for the PowerPAD™ should be sized to match the pad size on the 144-pin RFP package; as illustrated in Figure 5-2.

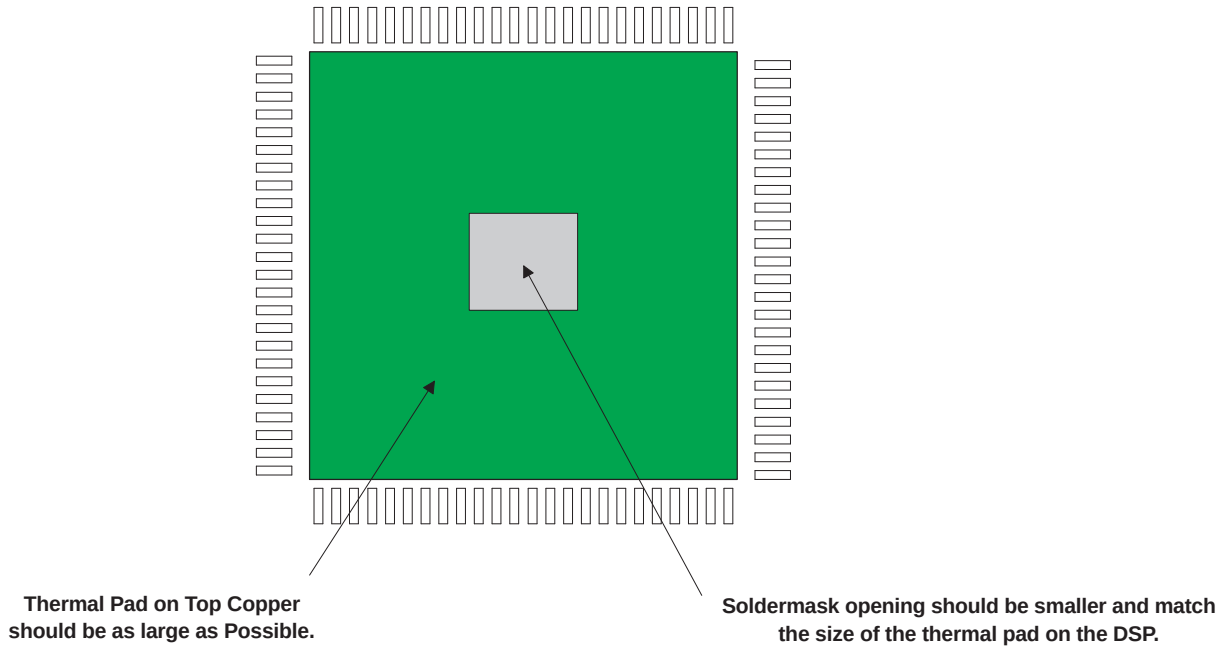


Figure 5-2. Soldermask Opening Should Match Size of DSP Thermal Pad

6 Revision History

This data sheet revision history highlights the technical changes made to the SPRS279D device-specific data sheet to make it an SPRS279E revision.

Scope: Added TMS320DA787B device which supports DTS® 5.1, DTS-ES™ 6.1, DTS Neo:6™, DTS 96/24™, and DTS-ES 96/24™.

ADDS/CHANGES/DELETES
Global: • Added information/data on the TMS320DA787B (DA787B) device throughout the document.
Section 1.1, Features: • Updated "Software Support" feature: – Added "(**DA787B only**)" to "DTS® 5.1, DTS-ES™ 6.1, DTS Neo:6™, DTS 96/24™, DTS-ES 96/24™" – Added "MPEG-4 AAC LC Encode/Decode" – Added "Neural-THX® Surround " to "THX® Select 2, THX® Ultra 2" – Deleted "WMA9 Pro Decode" – Added "2EQ®" to "Audyssey MultEQ XT®, MultEQ®, PrevEQ®"
Section 1.2, Trademarks: • Added "2EQ" to "Audyssey MultEQ XT, MultEQ, and PrevEQ are registered trademarks of Audyssey Laboratories."
Section 2, Device Overview: • Added **Note**
Table 5-2, Orderable Part Numbers: • Added part number D787yxxxBRFP250 • Added part number D787yxxxBRFPA250 • Added "[This device should ***not*** be used for applications with DTS IP]" statement to "D707 = Base Part Number (DA707)" • Added "D787 = Base Part Number (DA787B) [This device should be used for applications with DTS IP]"

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