DRA64x/DRA65x OMAP™ Automotive Applications Processors Technical Brief

1 High-Performance System-on-Chip (SoC)

1.1 Features

- High-Performance Automotive Media Applications Processors
  - Up to 1-GHz ARM® Cortex™-A8 RISC Core
  - Up to 600-MHz C674x™ VLIW DSP
  - Up to 4800/3600 C674x™ MIPS/MFLOPS
  - Fully Software-Compatible with C67x+™, C64x+™
- ARM® Cortex™-A8 Core
  - ARMv7 Architecture
    - In-Order, Dual-Issue, Superscalar Processor Core
    - NEON™ Multimedia Architecture
    - Supports Integer and Floating Point
    - Jazelle® RCT Execution Environment
- ARM® Cortex™-A8 Memory Architecture
  - 32K-Byte Instruction and Data Caches
  - 512K-Byte L2 Cache
  - 64K-Byte RAM, 48K-Byte Boot ROM
- TMS320C674x™ Floating-Point VLIW DSP
  - 64 General-Purpose Registers (32-Bit)
  - Six ALU (32-/40-Bit) Functional Units
    - Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit) and DP (IEEE Double Precision/64-Bit) Floating Point
    - Supports up to Four SP Adds Per Clock and Four DP Adds Every Two Clocks
    - Supports up to Two Floating-Point (SP or DP) Approximate Reciprocal or Square Root Operations Per Cycle
  - Two Multiply Functional Units
    - Mixed-Precision IEEE Floating-Point Multiply Supported up to:
      - 2 SP x SP → SP Per Clock
      - 2 SP x SP → DP Every Two Clocks
      - 2 SP x DP → DP Every Three Clocks
      - 2 DP x DP → DP Every Four Clocks
    - Fixed-Point Multiply Supports Two 32 x 32 Multiplies, Four 16 x 16-bit Multiplies including Complex Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle
- C674x™ Two-Level Memory Architecture
  - 32K-Byte L1P RAM/Cache With EDC
  - 32K-Byte L1D RAM/Cache
  - 256K-Byte L2 Unified Mapped RAM/Caches With ECC
- DSP/EDMA Memory Management Unit (DEMMU)
  - Maps C674x DSP and EDMA TC Memory Accesses to System Addresses
- 128K-Bytes On-Chip Memory Controller (OCMC) RAM
- General-Purpose M3 Subsystem
  - ARM® Cortex™ - M3 Processor
    - 128K-Byte Instruction/Data Memory
    - 16K-Byte Data Memory
  - General-Purpose DMA
  - Five General-Purpose Timers
- Programmable High-Definition Video Image Coprocessing (HDVICP v2) Engine
  - Encode, Decode, Transcode Operations
  - H.264, MPEG2, VC1, MPEG4, SP/ASP, JPEG/MJPEG
- Media Controller
  - Controls the HDVPSS and HDVICP2
- SGX530 3D Graphics Engine
  - Delivers up to 23 MPoly/sec
  - Universal Scalable Shader Engine
  - Direct3D Mobile, OpenGLES 1.1 and 2.0, OpenVG 1.0, OpenMax API Support
  - Advanced Geometry DMA Driven Operation
  - Programmable HQ Image Anti-Aliasing
- Viterbi Coprocessor (VCP2)
- Endianness
  - ARM/DSP Instructions/Data – Little Endian
- HD Video Processing Subsystem (HDVPSS)
  - Two 165 MHz HD Video Capture Inputs
    - One 16/24-bit Input, Splittable into Dual 8-bit SD Capture Ports
    - One 8/16/24-bit Input
    - One 8-bit Only Input
  - Two 165 MHz HD Video Display Output
    - One 16/24/30-bit and one 16/24-bit Output
  - Composite or S-Video Analog Output
  - MacroVision® Support Available
  - Digital HDMI 1.3 transmitter With Integrated PHY

- Advanced Video Processing Features Such as Scan/Format/Rate Conversion
- Three Graphics Layers and Compositors

- Dual 32-bit DDR2/DDR3 SDRAM Interfaces
  - Supports up to DDR2-800 and DDR3-800
  - Up to Eight x 8 Devices Total 2 GB Total Address Space
  - Dynamic Memory Manager (DMM)
    - Programmable Multi-Zone Memory Mapping and Interleaving
    - Enables Efficient 2D Block Accesses
    - Supports Tiled Objects in 0°, 90°, 180°, or 270° Orientation and Mirroring
    - Optimizes Interlaced Accesses
- General Purpose Memory Controller (GPMC)
  - 8-/16-bit Multiplexed Address/Data Bus
  - 512M-Byte Total Address Space Divided Among up to 8 Chip Selects
  - Glueless Interface to NOR Flash, NAND Flash (BCH/Hamming Error Code Detection), SRAM and Pseudo-SRAM
  - Error Locator Module (ELM) Outside of GPMC to Provide Upto 16-Bit/512-Bytes Hardware ECC for NAND
  - Flexible Asynchronous Protocol Control for Interface to FPGA, CPLD, ASICs, and so Forth
- Enhanced Direct-Memory-Access (EDMA) Controller
  - Four Transfer Controllers
  - 64/8 Independent DMA/QDMA Channels
- Dual Port Ethernet (10/100/1000 Mb/s) With Optional Switch
  - IEEE 802.3 Compliant (3.3V I/O Only)
  - MII/RMII/GMII/RGMII Media Independent I/Fs
  - Management Data I/O (MDIO) Module
  - Reset Isolation
  - IEEE-1588 Time-Stamping, AVB, and Industrial Ethernet Protocols
- Dual USB 2.0 Ports With Integrated PHYs
  - USB2.0 High-/Full-Speed Clients
  - USB2.0 High-/Full-/Low-Speed Hosts, or OTG
  - Supports End Points 0-15
- One PCI Express 2.0 Port With Integrated PHY
  - Single Port With 1 Lane at 5.0 GT/s
  - Configurable as Root Complex or Endpoint
- MLB Subsystem (MLBSS)
  - MLB 3-pin or 6-pin interfaces
  - Enables Connection to MOST Optical Rings
  - MOST25/50/150 (up to 100Mbps)
- Audio Tracking Logic (ATL)
  - Asyncronous SRC Assist
- Eight 32-bit General-Purpose Timers (Timer1–8)
- One System Watchdog Timer (WDT 0)
- Six Configurable UART/IrDA/CIR Modules
  - UART0 With Modem Control Signals
  - Supports up to 3.6864 Mbps UART0/1/2
  - Supports up to 12 Mbps UART3
  - SIR, MIR, FIR (4.0 MBAUD), and CIR
- Four Serial Peripheral Interfaces (SPIs) [up to 48-MHz]
  - Each With Four Chip-Selects
- Three MMC/SD/SDIO Serial Interfaces [up to 48-MHz]
  - Three Supporting up to 1-/4-/8-Bit Modes
- Dual Controller Area Network (DCAN) Modules
  - CAN Version 2 Part A, B
- Four Inter-Integrated Circuit (I2C Bus™) Ports
- Six Multi-Channel Audio Serial Ports (McASP)
  - Dual Ten Serializer Transmit/Receive Ports
  - Quad Four Serializer Transmit/Receive Ports
  - DIT-Capable For S/PDIF (All Ports)
- Multi-Channel Buffered Serial Port (McBSP)
  - Transmit/Receive Clocks up to 48 MHz
  - Two Clock Zones and Two Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
- Serial ATA (SATA) 3.0 Gbps Controller With Integrated PHY
  - Direct Interface to One Hard Disk Drive
  - Hardware-Assisted Native Command Queuing (NCQ) from up to 32 Entries
  - Supports Port Multiplier and Command-Based Switching
- Parallel ATA/ATAPI I/F (ATA/ATAPI-6 Specification)
  - PIO, Multiword DMA, and UDMA
- Real-Time Clock (RTC)
  - One-Time or Periodic Interrupt Generation
- Up to 128 General-Purpose I/O (GPIO) Pins
- One Spin Lock Module with up to 128 Hardware Semaphores
- One Mailbox Module with 12 Mailboxes
- On-Chip ARM ROM Bootloader (RBL)
- Power, Reset, and Clock Management
  - Multiple Independent Core Power Domains
  - Multiple Independent Core Voltage Domains
  - Support for Three Operating Points (OPP166/120/100) per Voltage Domain
  - Clock Enable/Disable Control for Subsystems and Peripherals
- 32KB Embedded Trace Buffer™ (ETB™) and 5-pin Trace Interface for Debug
- IEEE-1149.1 (JTAG) Compatible
- 684-Pin Pb-Free BGA Package (CYE Suffix), 0.8-mm Ball Pitch With Via Channel™ Technology to Reduce PCB Cost

- **45-nm CMOS Technology**
- **3.3-V Buffers for General I/O and 1.8V/3.3V Dual Voltage Buffers for MMC/SD/SDIO interface**

1.2 Applications

- **Automotive Navigation**
- **In Car Media/Radio/DTV Receiver**
- **Automotive Connectivity Box**
- **Automotive Vision**
- **Rear Seat Entertainment**

1.3 Description

DRA64x/DRA65x OMAP Automotive Applications Processors are a highly-integrated, programmable platform that leverages TI's technology to meet the processing needs of the following automotive applications: automotive navigation, Media/Radio/DTV reception, connectivity, automotive vision and rear seat entertainment.

The device enables Original-Equipment Manufacturers (OEMs) and Original-Design Manufacturers (ODMs) to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance through the maximum flexibility of a fully integrated mixed processor solution. The device also combines programmable processing with a highly integrated peripheral set.

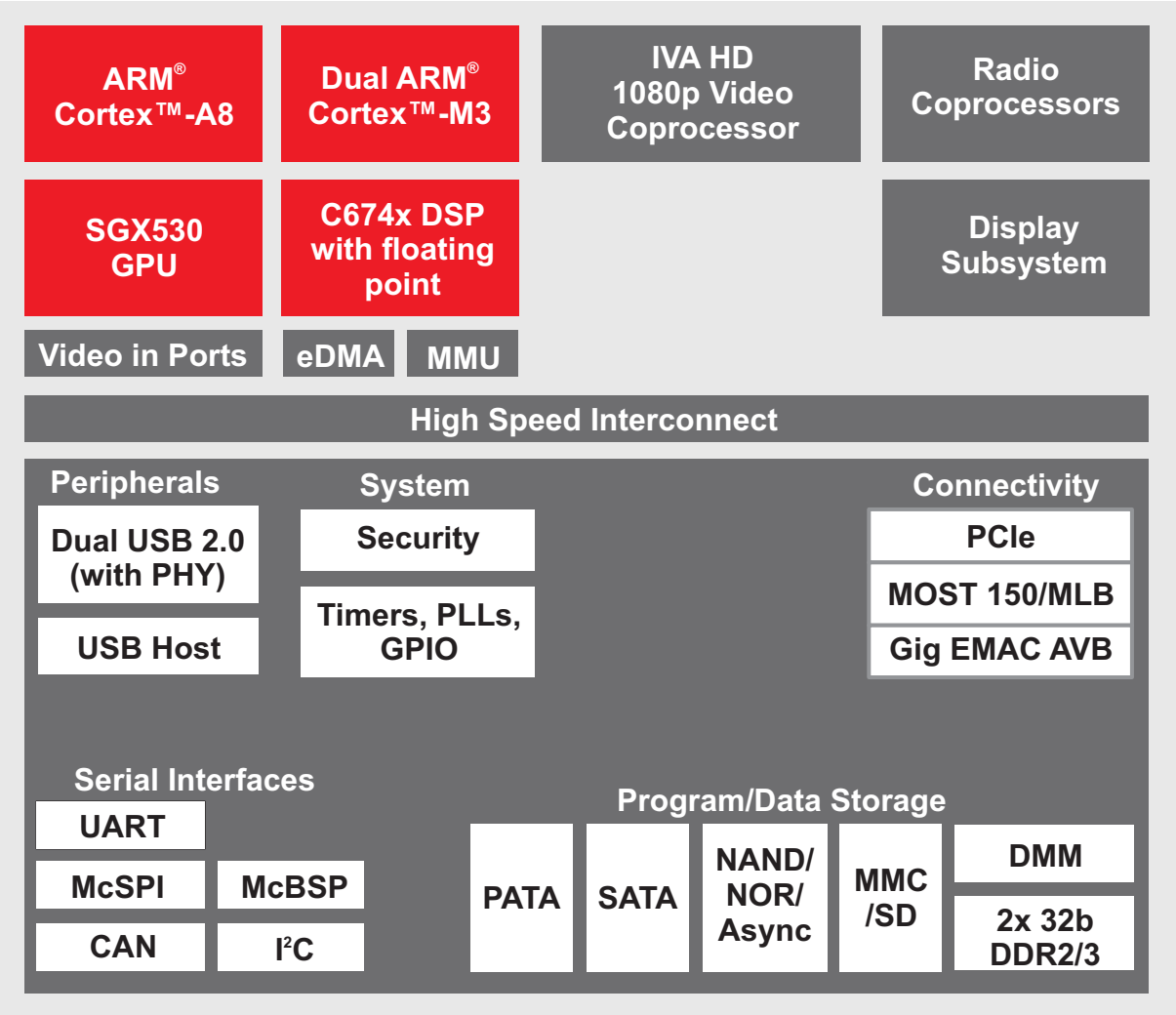
Programmability is provided by an ARM Cortex™-A8 RISC CPU with Neon™ extension, TI C674x VLIW floating-point DSP core, and high-definition video/imaging coprocessors. The ARM allows developers to keep control functions separate from algorithms programmed on the DSP and coprocessors, thus reducing the complexity of the system software. The ARM Cortex™-A8 32-bit RISC Core with Neon™ floating-point extension includes: 32 Kbytes (KB) of Instruction cache; 32KB of Data cache; 512KB of L2 Cache; 48KB of Boot ROM; and 64KB of RAM.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections in this document and the associated peripheral reference guides. The peripheral set includes: HD Video Processing Subsystem;General-Purpose M3 Subsystem; Transport Packet Processor Subsystem; Dual Port Gigabit Ethernet MACs (10/100/1000 Mbps) [Ethernet Switch] with MII/RMII/GMII/RGMII and MDIO interface supporting IEEE-1588 Time-Stamping, AVB, and Industrial Ethernet Protocols; two USB ports with integrated 2.0 PHY; PCIe x1 GEN2 Compliant interface; two 10-serializer McASP audio serial ports (with DIT mode); four quad-serilaizer McASP audio serial ports (with DIT mode); one McBSP multichannel buffered serial port; six UARTs with IrDA and CIR support; four SPI serial interfaces; three MMC/SD/SDIO serial interfaces; four I2C master/slave interfaces; a Parallel Camera Interface (CAM); up to 128 General-Purpose IOs (GPIOs); eight 32-bit general-purpose timers; System watchdog timer; Dual DDR2/DDR3 SDRAM interfaces; flexible 8/16-bit asynchronous memory interface; two Controller Area Network (DCAN) modules; a Spin Lock; Mailbox; Parallel Hard Disk Drive Interface (PATA/ATAPI); MLBSS 3-Pin and 6-Pin Interfaces; Audio Tracking Logic (ATL); and Parallel ATA.

DRA64x/DRA65x OMAP Automotive Applications Processors also include a high-definition video/imaging coprocessor 2 (HDVICP2), and an SGX530 3D graphics engine to off-load many video and imaging processing tasks from the DSP core, making more DSP MIPS available for common video and imaging algorithms. Additionally, it has a complete set of development tools for both the ARM and DSP which include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Microsoft® Windows™ debugger interface for visibility into source code execution.

The C674x DSP core is the high-performance floating-point DSP generation in the TMS320C6000™ DSP platform and is code-compatible with previous generation C64x Fixed-Point and C67x Floating-Point DSP generation. The C674x Floating-Point DSP processor uses 32KB of L1 program memory with EDC and 32KB of L1 data memory. Up to 32KB of L1P can be configured as program cache. The remaining is noncacheable no-wait-state program memory. Up to 32KB of L1D can be configured as data cache. The remaining is non-cacheable no-wait-state data memory. The DSP has 256KB of L2 RAM with ECC, which can be defined as SRAM, L2 cache, or a combination of both. All C674x L3 and off-chip memory accesses are routed through an MMU.

1.4 DRA64x/DRA65x Functional Block Diagram



Note: Not all peripherals are available at the same time due to pin multiplexing.

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