

SPRT659-January 2013-Revised June 2013

Introduction

This chapter introduces the features, subsystems, and architecture of the DRA74x (Jacinto 6) family of high-performance infotainment processors.

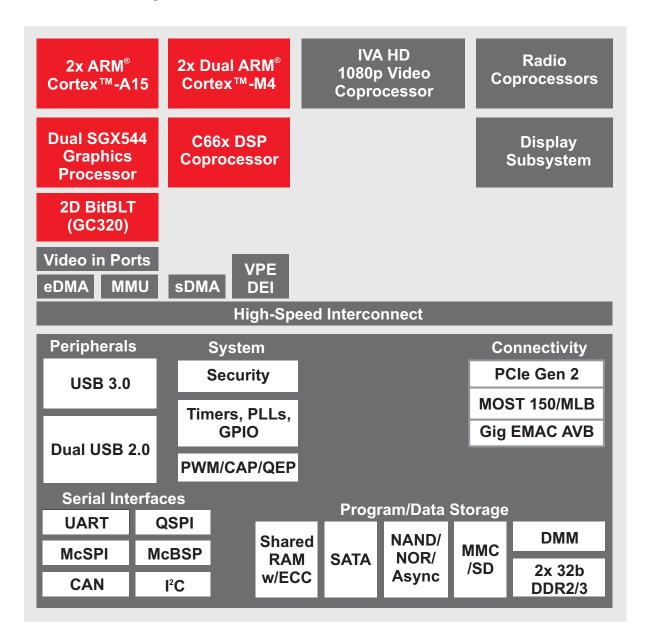
The DRA74x is a high-performance, infotainment application device family, based on enhanced OMAP™ architecture integrated on a 28-nm technology. Features

- The architecture is designed for advanced graphical HMI and Navigation, Digital and Analog Radio, Rear Seat Entertainment and Multimedia playback, providing best-in-class CPU performance, video, image, and graphics processing sufficient to support, among others:
 - Streaming video up to full high definition (Full-HD) (1920×1080p, 60 fps)
 - 2-dimensional (2D) and 3-dimensional (3D) graphics and composition
 - Decode of digital radio standards (DAB, HD Radio™), and analog AM/FM/RDS radio
 - Efficient web browsing
 - Support for multiple high-definition displays and video inputs
- The device is composed of the following subsystems:
 - Cortex[™]-A15 microprocessor unit (MPU) subsystem, including two ARM® Cortex-A15 cores
 - One digital signal processor (DSP) C66x subsystem
 - Image and video accelerator high-definition (IVA-HD) subsystem
 - Two CortexTM-M4 image processing unit (IPU) subsystems, each including two ARM Cortex-M4 microprocessors
 - Display subsystem (DSS)
 - Video Processing subsystem (VPE)
 - Video Input Capture (VIP)
 - 3D-graphics processing unit (GPU) subsystem, including POWERVR™ SGX544 dual-core
 - 2D-graphics accelerator (BB2D) subsystem, including Vivante™ GC320 core
 - Three pulse-width modulation (PWM) subsystems
 - Real-time clock (RTC) subsystem
 - Debug subsystem
- The device provides a rich set of connectivity peripherals, including:
 - One USB3.0 and two UBS2.0 subsystems
 - SATA 2 subsystem
 - PCI Express Gen2 subsystem
 - 3-port Gigabit Ethernet Switch subsystem
- The device includes state-of-the-art integrated power management techniques required for highperformance infotainment products.
- The device also integrates:
 - On-chip memory
 - External memory interfaces
 - Memory management
 - Level 3 (L3) and level 4 (L4) interconnects



- System peripherals
- Car, audio and media peripherals including CAN, MOST MLB, and Ethernet AVB
- Radio accelerators DRA74x Description

The DRA74x device is offered in a 760-ball, 23×23-mm, 0.8-mm ball pitch with Via Channel™ Array (VCA) technology, ball grid array (BGA) package. is the block diagram of the DRA74x device. DRA74x Functional Block Diagram



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