OMAP™

OMAP5432
Multimedia Device
Engineering Samples 2.0

Version E

Data Manual

Texas Instruments

Public Version

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Multimedia Device
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1 Introduction

This Data Manual describes the electrical and mechanical specifications of the OMAP5432 processor. It consists of the following sections:

- A description of the device terminals: ball assignments, electrical characteristics, multiplexing modes, and signal descriptions (Section 2)
- A description of the required electrical characteristics: absolute maximum ratings, operating conditions, dc characteristics, voltage decoupling capacitors, and device power-up and power-down sequences (Section 3)
- The clock specifications: characteristics of the input and output clocks, PLL and DLL specifications (Section 4)
- The timing requirements and switching characteristics (ac timings) of the interfaces (Section 5)
- The thermal management recommendations including the thermal resistance characteristics (Section 6)
- A description of the device nomenclature and mechanical data (Section 7)
- The OMAP5432 processor multimedia device PCB guidelines (Section 8)
- A glossary of the acronyms and abbreviations used in the data manual (Section 9)

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This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

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This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

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Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

2 Terminal Description

2.1 Terminal Assignment

Figure 2-1 shows the ball locations for the 754-ball plastic ball grid array (PBGA) package and are used in conjunction with Table 2-1 through Table 2-39 to locate signal names and ball grid numbers.

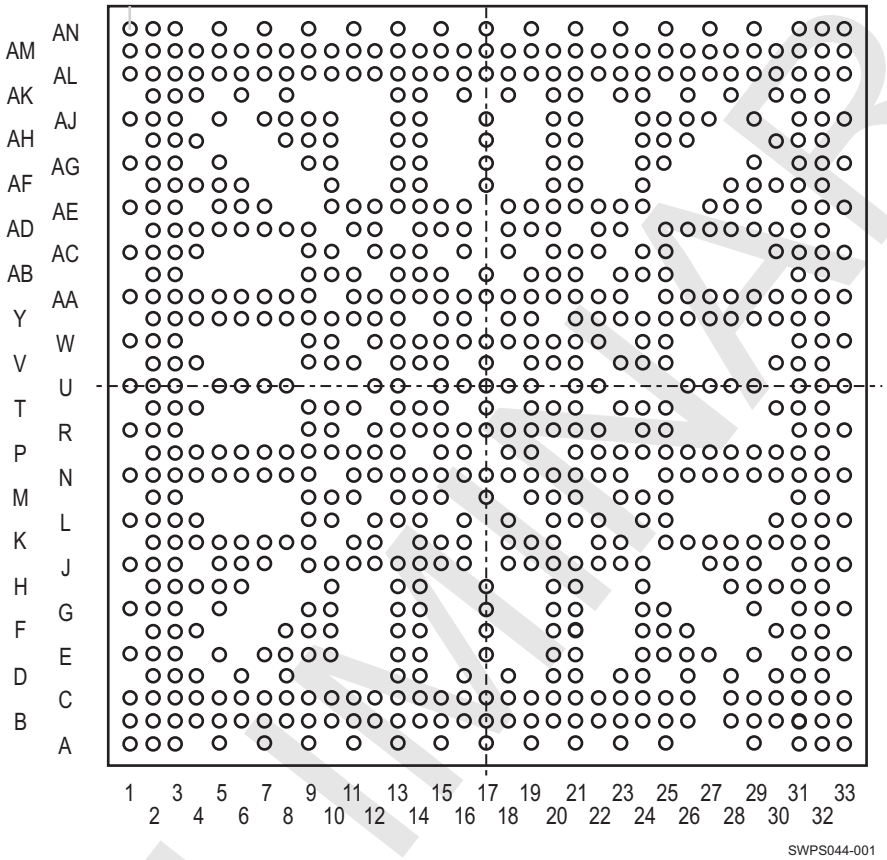


Figure 2-1. OMAP5432 AAN S-PBGA-N754 Package (Bottom View)

NOTE

The following bottom balls are not connected: A1 / A2 / AM33 / AN32 / AN33.

These balls can be connected to VSS if desired.

NOTE

The following bottom balls are reserved: AN2 / AD8 / K7 / AA8 / U7 / G10 / P27 / G17 / G25 / AN1 / B1 / AC33 / AG33 / AL22 / AM28 / AN27 / AM1 / AF14 / AG14 / AJ14 / AH14 / AG13 / AF13 / AH13 / AJ13.

These balls must be left unconnected.

NOTE

The following bottom balls are reserved: AJ17 / AK18 / AK16 / AF17 / H14.

These balls must be grounded.

2.2 Ball Characteristics

Table 2-1 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL BOTTOM:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in mode 0).

NOTE

Table 2-1 does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 2.4, *Signal Descriptions*.

NOTE

In the safe_mode, the buffer is configured in high-impedance.

3. **MODE:** Multiplexing mode number:
   (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the ball corresponds to the name of the ball. There is always a function mapped on the primary mode. The primary mode is not necessarily the default mode.

NOTE

The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.

   (b) Modes 1 through 7 are possible modes for alternate functions. On each ball, some modes are effectively used for alternate functions, while some modes are not used and correspond to a safe mode per design implementation.
4. **TYPE:** Signal type and direction:
   - I = Input
   - O = Output
   - IO = Input or Output
   - D = Open drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground
5. **BALL RESET STATE:** The state of the terminal at power-on reset:
   - 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   - 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H: High-impedance with an active pullup resistor
6. **BALL RESET REL. STATE:** The state of the terminal at the release of the system control module reset (PRCM CORE_PWRON_RET_RST reset signal).
   - 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   - 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H: High-impedance with an active pullup resistor

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the OMAP543x TRM.

7. **RESET REL. MODE:** This mode is automatically configured at the release of the system control module reset (PRCM CORE_PWRON_RET_RST reset signal).
8. **IO VOLTAGE VALUE**: This column describes the IO voltage value (VDDS supply).
9. **POWER NAME:** The voltage supply that powers the terminal IO buffers.
10. **SECOND POWER AVAIL.**: Some OMAP5432 IOs have a second power supply signal (vdds_1p8) to ensure the VDDS ramping.
11. **HYS:** Indicates if the input buffer is with hysteresis:
    - Yes: With high hysteresis
    - No: Without low hysteresis

NOTE

For more information, see the hysteresis values in Section 3.4, *DC Electrical Characteristics*.

12. **BUFFER STRENGTH:** Drive strength of the associated output buffer.

NOTE

For programmable buffer strength:
- The default value is given in Table 2-1.
- A note describes all possible values according to the selected mode.

13. **PULLUP/DOWN – TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

NOTE

The pullup/pulldown drive strength is equal to: minimum = 50 µA, typical = 100 µA, maximum = 250 µA, unless otherwise specified.

14. **IO CELL:** IO cell information:
    - LVCMOS: The IO buffer receives or drives a standard GPIO signal.
    - BK: This symbol underlines that this IO supports a bus keeper (or bus holder) function. It allows the output buffer to maintain the last state driven by using an internal pullup or pulldown resistor.
    - I^2C Open Drain: The IO buffer outputs an open drain signal. This IO is designed for I^2C function.
    - LVCMOS 3-State Open Drain: That indicates that the IO is a standard LVCMOS buffer that is used in the 3-state mode to have an open drain driver.
    - MPHY: This I/O supports MIPI M-PHY signals.
    - DPHY: This IO supports MIPI D-PHY signals.
    - Analog: For analog signals.
    - DDR: This IO can support LPDDR2 (for OMAP5430), DDR3 and DDR3L (used in OMAP5432), and HSUL_12 (HSIC) protocols.
    - SATAPHY: This IO supports SATA PHY signals.
    - USB3PHY: This IO supports USB3 PHY signals.
    - HDMIPHY: For IO buffer that supports HDMI PHY signals.

NOTE

Configuring two balls to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by ball multiplexing, this pad is actually set undriven (high impedance: Z) with potential pullup or pulldown resistors. Pulls need to be disabled to have a pure high impedance.

NOTE

All balls not described in Table 2-1 are not connected.

Table 2-1. Ball Characteristics(1)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] (2)	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
H20 / J23 / J22 / J14 / J13 / J12 / L9 / M9 / P26 / P25 / R25 / U27 / U26 / W25 / Y25 / Y9 / AA25 / AA9 / AB25 / AC25 / AC9 / AD25 / AE24 / AE21 / AE15 / AE14 / AE13 / AF21 / U28	vdds_1p8	0	PWR	-	-	-	-	-	-	-	-	-	Power
AB9	vdds_emmc	0	PWR	-	-	-	-	-	-	-	-	-	Power
AJ10	emmc_clk	0	O	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_46	6	IO										
	safe_mode	7											
AH10	emmc_cmd	0	IO	H	H	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_47	6	IO										
	safe_mode	7											
AG10	emmc_data0	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_48	6	IO										
	safe_mode	7											
AF10	emmc_data1	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_49	6	IO										
	safe_mode	7											
AH9	emmc_data2	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_50	6	IO										
	safe_mode	7											
AJ9	emmc_data3	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_51	6	IO										
	safe_mode	7											
AG9	emmc_data4	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_52	6	IO										
	safe_mode	7											
AJ8	emmc_data5	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_53	6	IO										
	safe_mode	7											
AH8	emmc_data6	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(8)	PU/PD	LVCMOS
	gpio2_54	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AJ7	emmc_data7	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio2_55	6	IO										
	safe_mode	7											
J21 / J20	vdds_c2c	0	PWR	-	-	-	-	-	-	-	-	-	Power
J27	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row0	3	I										
	gpmc_ad0	4	IO										
	gpio2_37	6	IO										
	safe_mode	7											
H28	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row1	3	I										
	gpmc_ad1	4	IO										
	gpio2_38	6	IO										
	safe_mode	7											
H29	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row2	3	I										
	gpmc_ad2	4	IO										
	gpio2_39	6	IO										
	safe_mode	7											
G29	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row3	3	I										
	gpmc_ad3	4	IO										
	gpio2_40	6	IO										
	safe_mode	7											
E29	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row4	3	I										
	gpmc_ad4	4	IO										
	gpio2_41	6	IO										
	safe_mode	7											
E27	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row5	3	I										
	gpmc_ad5	4	IO										
	gpio2_42	6	IO										
	safe_mode	7											
F26	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row6	3	I										
	gpmc_ad6	4	IO										
	gpio2_43	6	IO										
	safe_mode	7											
E26	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row7	3	I										
	gpmc_ad7	4	IO										
	gpio2_44	6	IO										
	safe_mode	7											
J28	Reserved	0	I	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_row8	3	I										
	gpmc_clk	4	O										
	gpio2_36	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
J29	Reserved	0	I	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_nwp	4	O										
	gpmc_nbe1	5	O										
	gpio2_35	6	IO										
	safe_mode	7											
E25	Reserved	0	O	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_NAdv_ale	4	O										
	gpio2_33	6	IO										
	safe_mode	7											
F25	Reserved	0	O	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col8	3	O										
	gpmc_nbe0_cle	4	O										
	gpio2_34	6	IO										
	safe_mode	7											
J32	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col0	3	O										
	gpmc_ad8	4	IO										
	hw_dbg16	5	O										
	gpio2_56	6	IO										
	safe_mode	7											
J33	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col1	3	O										
	gpmc_ad9	4	IO										
	hw_dbg17	5	O										
	gpio2_57	6	IO										
	safe_mode	7											
H32	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col2	3	O										
	gpmc_ad10	4	IO										
	hw_dbg18	5	O										
	gpio2_58	6	IO										
	safe_mode	7											
J31	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col3	3	O										
	gpmc_ad11	4	IO										
	hw_dbg19	5	O										
	gpio2_59	6	IO										
	safe_mode	7											
G31	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col4	3	O										
	gpmc_ad12	4	IO										
	hw_dbg20	5	O										
	gpio2_60	6	IO										
	safe_mode	7											
H31	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col5	3	O										
	gpmc_ad13	4	IO										
	hw_dbg21	5	O										
	gpio2_61	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
G32	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col6	3	O										
	gpmc_ad14	4	IO										
	hw_dbg22	5	O										
	gpio2_62	6	IO										
	safe_mode	7											
G33	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	kbd_col7	3	O										
	gpmc_ad15	4	IO										
	hw_dbg23	5	O										
	gpio2_63	6	IO										
	safe_mode	7											
G24	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a16	4	O										
	hw_dbg24	5	O										
	gpio4_113	6	IO										
	safe_mode	7											
H24	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a17	4	O										
	hw_dbg25	5	O										
	gpio4_114	6	IO										
	safe_mode	7											
E24	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a18	4	O										
	hw_dbg26	5	O										
	gpio4_115	6	IO										
	safe_mode	7											
F24	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a19	4	O										
	hw_dbg27	5	O										
	gpio4_116	6	IO										
	safe_mode	7											
G21	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a20	4	O										
	hw_dbg28	5	O										
	gpio4_117	6	IO										
	safe_mode	7											
H21	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a21	4	O										
	hw_dbg29	5	O										
	gpio4_118	6	IO										
	safe_mode	7											
E21	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a22	4	O										
	hw_dbg30	5	O										
	gpio4_119	6	IO										
	safe_mode	7											
F21	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_a23	4	O										
	hw_dbg31	5	O										
	gpio4_120	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
P32	reserved	0	O	H	1	4	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_ncs0	4	O										
	gpio2_32	6	IO										
	safe_mode	7											
N27	Reserved	0	O	H	H	4	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpmc_wait0	4	I										
	gpio2_45	6	IO										
	safe_mode	7											
N29	Reserved	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg13	5	O										
	gpio1_wk15	6	IO										
	safe_mode	7											
N28	Reserved	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg14	5	O										
	gpio1_wk14	6	IO										
	safe_mode	7											
G20	hsi2_caready	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_clk	3	I										
	gpmc_wait1	4	I										
	gpio3_76	6	IO										
	safe_mode	7											
F20	hsi2_acready	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_nxt	3	I										
	gpmc_ncs1[13]	4	O										
	gpio3_77	6	IO										
	safe_mode	7											
F17	hsi2_cawake	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_dir	3	I										
	gpmc_a24	4	O										
	gpio3_78	6	IO										
	safe_mode	7											
E20	hsi2_acwake	0	O	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_stp	3	O										
	gpmc_a25	4	O										
	gpio3_79	6	IO										
	safe_mode	7											
E14	hsi2_caflag	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_data0	3	IO										
	gpmc_wait2	4	I										
	gpio3_80	6	IO										
	safe_mode	7											
F14	hsi2_cadata	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_data1	3	IO										
	gpmc_ncs2[13]	4	O										
	gpio3_81	6	IO										
	safe_mode	7											
G14	hsi2_acflag	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_data2	3	IO										
	gpmc_ncs3[13]	4	O										
	gpio3_82	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
E17	hsi2_acdata	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbb1_ulpiphy_data3	3	IO										
	gpmc_ncs4[13]	4	O										
	gpio3_83	6	IO										
	safe_mode	7											
F13	uart2_rts	0	O	H	1	4	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi3_somi	1	IO										
	usbb1_ulpiphy_data4	3	IO										
	gpmc_nwe	4	O										
	hw_dbg16	5	O										
	gpio3_84	6	IO										
	safe_mode	7											
N9	uart2_cts	0	I	H	1	4	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi3_cs0	1	IO										
	usbb1_ulpiphy_data5	3	IO										
	gpmc_noe_nre	4	O										
	hw_dbg17	5	O										
	gpio3_85	6	IO										
	safe_mode	7											
G13	uart2_rx	0	I	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi3_simo	1	IO										
	usbb1_ulpiphy_data6	3	IO										
	gpmc_ncs5	4	O										
	hw_dbg18	5	O										
	gpio3_86	6	IO										
	safe_mode	7											
E13	uart2_tx	0	O	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi3_clk	1	IO										
	usbb1_ulpiphy_data7	3	IO										
	gpmc_ncs6	4	O										
	hw_dbg19	5	O										
	gpio3_87	6	IO										
	safe_mode	7											
N26	vdds_hsic	0	PWR	-	-	-	-	-	-	-	-	-	Power
K28	usbb2_hsic_strobe	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
	gpio3_94	6	IO										
	safe_mode	7											
K29	usbb2_hsic_data	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
	gpio3_95	6	IO										
	safe_mode	7											
W31	timer10_pwm_evt	0	IO	L	L	7	1.8 V or 1.2 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio6_188	6	IO										
	safe_mode	7											
W33	dsiporta_te0	0	I	L	L	7	1.8 V or 1.2 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio6_189	6	IO										
	safe_mode	7											
AA33	vdda_dsiporta	0	PWR	-	-	-	-	-	-	-	-	-	-
Y30	vssa_dsiporta	0	GND	-	-	-	-	-	-	-	-	-	-
AD31	dsiporta_lane0x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AD32	dsiporta_lane0y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AC31	dsiporta_lane1x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AC32	dsiporta_lane1y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AB32	dsiporta_lane2x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AB31	dsiporta_lane2y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AA32	dsiporta_lane3x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AA31	dsiporta_lane3y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
Y32	dsiporta_lane4x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
Y31	dsiporta_lane4y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiporta	No	No	See [15]	No	DPHY
AJ33	timer9_pwm_evt	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sync_sof_clk	1	O										
	sync_usof_itp_clk	2	O										
	gpio6_190	6	IO										
	safe_mode	7											
AK30	dsiportc_te0	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio6_191	6	IO										
	safe_mode	7											
AE33	vdda_dsiportc	0	PWR	-	-	-	-	-	-	-	-	-	Power
AD30	vssa_dsiportc	0	GND	-	-	-	-	-	-	-	-	-	Power
AJ31	dsiportc_lane0x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AJ32	dsiportc_lane0y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AH32	dsiportc_lane1x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AH31	dsiportc_lane1y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AG32	dsiportc_lane2x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AG31	dsiportc_lane2y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AF32	dsiportc_lane3x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AF31	dsiportc_lane3y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AE32	dsiportc_lane4x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AE31	dsiportc_lane4y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_ dsiportc	No	No	See [15]	No	DPHY
AN13	rfbi_hsync0	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data17	3	O										
	kbd_col5	4	O										
	gpio6_160	6	IO										
	safe_mode	7											
AM13	rfbi_te_vsync0	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data16	3	O										
	kbd_row5	4	I										
	jtag_sel	5	I										
	gpio6_161	6	IO										
	safe_mode	7											
AL18	rfbi_re	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_pclk	3	O										
	kbd_col4	4	O										
	gpio6_164	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AM18	rfbi_a0	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_de	3	O										
	kbd_row4	4	I										
	gpio6_165	6	IO										
	safe_mode	7											
AL14	rfbi_data8	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data8	3	O										
	kbd_col3	4	O										
	drm_emu12	5	O										
	gpio6_174	6	IO										
	safe_mode	7											
AM14	rfbi_data9	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data9	3	O										
	kbd_row3	4	I										
	drm_emu13	5	O										
	gpio6_175	6	IO										
	safe_mode	7											
AM12	rfbi_data10	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data10	3	O										
	kbd_row8	4	I										
	drm_emu14	5	O										
	gpio6_176	6	IO										
	safe_mode	7											
AL11	rfbi_data11	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data11	3	O										
	kbd_row7	4	I										
	drm_emu15	5	O										
	gpio6_177	6	IO										
	safe_mode	7											
AM11	rfbi_data12	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data12	3	O										
	kbd_row6	4	I										
	drm_emu16	5	O										
	gpio6_178	6	IO										
	safe_mode	7											
AN11	rfbi_data13	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data13	3	O										
	kbd_col8	4	O										
	drm_emu17	5	O										
	gpio6_179	6	IO										
	safe_mode	7											
AL10	rfbi_data14	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data14	3	O										
	kbd_col7	4	O										
	drm_emu18	5	O										
	gpio6_180	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AM10	rfbi_data15	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi2_cs1	1	O										
	dispc_data15	3	O										
	kbd_col6	4	O										
	drm_emu19	5	O										
	gpio6_181	6	IO										
	safe_mode	7											
AN9	gpio6_182[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data18	3	O										
	kbd_col0	4	O										
	gpio6_182[10]	6	IO										
	safe_mode	7											
AM9	gpio6_183[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data19	3	O										
	kbd_col1	4	O										
	gpio6_183[10]	6	IO										
	safe_mode	7											
AL9	gpio6_184[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data20	3	O										
	kbd_col2	4	O										
	hw_dbg22	5	O										
	gpio6_184[10]	6	IO										
	safe_mode	7											
AM8	gpio6_185[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data21	3	O										
	kbd_row0	4	I										
	hw_dbg23	5	O										
	gpio6_185[10]	6	IO										
	safe_mode	7											
AL8	gpio6_186[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data22	3	O										
	kbd_row1	4	I										
	hw_dbg24	5	O										
	gpio6_186[10]	6	IO										
	safe_mode	7											
AN7	gpio6_187[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data23	3	O										
	kbd_row2	4	I										
	hw_dbg25	5	O										
	gpio6_187[10]	6	IO										
	safe_mode	7											
AL17	rfbi_data0	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data0	3	O										
	jtagtapext_rtck	4	I										
	drm_emu4	5	O										
	gpio6_166	6	IO										
	safe_mode	7											
AM17	rfbi_data1	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data1	3	O										
	uart3_rx_irrx	4	I										
	drm_emu5	5	O										
	gpio6_167	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AN17	rfbi_data2	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data2	3	O										
	uart3_tx_irtx	4	O										
	drm_emu6	5	O										
	gpio6_168	6	IO										
	safe_mode	7											
AL16	rfbi_data3	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data3	3	O										
	jtagtapext_ntrst	4	O										
	drm_emu7	5	O										
	gpio6_169	6	IO										
	safe_mode	7											
AM16	rfbi_data4	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data4	3	O										
	jtagtapext_tck	4	O										
	drm_emu8	5	O										
	gpio6_170	6	IO										
	safe_mode	7											
AL15	rfbi_data5	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data5	3	O										
	jtagtapext_tmsc	4	O										
	drm_emu9	5	O										
	gpio6_171	6	IO										
	safe_mode	7											
AM15	rfbi_data6	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data6	3	O										
	jtagtapext_tdo	4	O										
	drm_emu10	5	O										
	gpio6_172	6	IO										
	safe_mode	7											
AN15	rfbi_data7	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_data7	3	O										
	jtagtapext_tdi	4	I										
	drm_emu11	5	O										
	gpio6_173	6	IO										
	safe_mode	7											
AL13	rfbi_cs0	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_hsync	3	O										
	drm_emu3	5	O										
	gpio6_163	6	IO										
	safe_mode	7											
AL12	rfbi_we	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	dispc_vsync	3	O										
	drm_emu2	5	O										
	gpio6_162	6	IO										
	safe_mode	7											
AF20	mcspi2_cs0	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	jtagtapext_ntrst	1	O										
	dispc_fid	3	O										
	gpio7_196	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AH17	mcspi2_clk	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	jtagtapext_tck	1	O										
	gpio7_197	6	IO										
	safe_mode	7											
AG20	mcspi2_simo	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	jtagtapext_tmsc	1	O										
	hw_dbg20	5	O										
	gpio7_198	6	IO										
	safe_mode	7											
AH20	mcspi2_somi	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	jtagtapext_tdo	1	O										
	hw_dbg21	5	O										
	gpio7_199	6	IO										
	safe_mode	7											
AJ21	i2c4_scl	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I²C Open Drain
	jtagtapext_tdi	1	I										
	gpio7_200	6	IO								4		
	safe_mode	7									4		
AJ20	i2c4_sda	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I²C Open Drain
	jtagtapext_rtck	1	I										
	gpio7_201	6	IO								4		
	safe_mode	7									4		
AE23	vdds_hdmi	0	PWR	-	-	-	-	-	-	-	-	-	Power
AN23	hdmi_cec	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_hdmi	Yes	Yes	4[8]	PU/PD	LVCMOS Tri-State Open Drain
	gpio7_192	6	IO										
	safe_mode	7											
AM23	hdmi_hpd	0	I	L	L	7	1.8 V or 1.2 V	vdds_hdmi	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio7_193	6	IO										
	safe_mode	7											
AM22	hdmi_ddc_scl	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_hdmi	Yes	No	3	PUx / PDy-OD[4]	LVCMOS I²C Open Drain
	gpio7_194	6	IO								4		
	safe_mode	7									4		
AL23	hdmi_ddc_sda	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_hdmi	Yes	No	3	PUx / PDy-OD[4]	LVCMOS I²C Open Drain
	gpio7_195	6	IO								4		
	safe_mode	7									4		
AN25	vdda_hdmi	0	PWR	-	-	-	-	-	-	-	-	-	Power
AK24	vssa_hdmi	0	GND	-	-	-	-	-	-	-	-	-	Power
AL24	hdmi_clkx	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AM24	hdmi_clky	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AL25	hdmi_data0x	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AM25	hdmi_data0y	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AL26	hdmi_data1x	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AM26	hdmi_data1y	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AL27	hdmi_data2x	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
AM27	hdmi_data2y	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi	No	No	10	PDy[5]	HDMIPHY
N3	vdda_csiporta	0	PWR	-	-	-	-	-	-	-	-	-	Power
P4	vssa_csiporta	0	GND	-	-	-	-	-	-	-	-	-	Power

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
U6	csiporta_lane0x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_pclk	3	I										
	gpio8_in236	6	I										
	safe_mode	7											
U5	csiporta_lane0y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_wen	3	I										
	gpio8_in237	6	I										
	safe_mode	7											
P5	csiporta_lane1y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data0	3	I										
	gpio8_in238	6	I										
	safe_mode	7											
P6	csiporta_lane1x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data1	3	I										
	gpio8_in239	6	I										
	safe_mode	7											
P8	csiporta_lane2y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data2	3	I										
	gpio8_in240	6	I										
	safe_mode	7											
P7	csiporta_lane2x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data3	3	I										
	gpio8_in241	6	I										
	safe_mode	7											
N5	csiporta_lane3x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data4	3	I										
	gpio8_in242	6	I										
	safe_mode	7											
N6	csiporta_lane3y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data5	3	I										
	gpio8_in243	6	I										
	safe_mode	7											
N7	csiporta_lane4x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data6	3	I										
	gpio8_in244	6	I										
	safe_mode	7											
N8	csiporta_lane4y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiporta	Yes	No	NA	PU/PD	DPHY
	cpi_data7	3	I										
	gpio8_in245	6	I										
	safe_mode	7											
AA7	vdda_csiportb	0	PWR	-	-	-	-	-	-	-	-	-	Power
Y4	vssa_csiportb	0	GND	-	-	-	-	-	-	-	-	-	Power
Y6	csiportb_lane0x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb	Yes	No	NA	PU/PD	DPHY
	cpi_data12	4	I										
	gpio8_in246	6	I										
	safe_mode	7											
Y5	csiportb_lane0y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb	Yes	No	NA	PU/PD	DPHY
	cpi_data13	4	I										
	gpio8_in247	6	I										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
Y7	csiportb_lane1y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb	Yes	No	NA	PU/PD	DPHY
	cpi_data14	4	I										
	gpio8_in248	6	I										
	safe_mode	7											
Y8	csiportb_lane1x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb	Yes	No	NA	PU/PD	DPHY
	cpi_data15	4	I										
	gpio8_in249	6	I										
	safe_mode	7											
AA5	csiportb_lane2y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb	Yes	No	NA	PU/PD	DPHY
	cpi_hsyncin	4	I										
	gpio8_in250	6	I										
	safe_mode	7											
AA6	csiportb_lane2x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb	Yes	No	NA	PU/PD	DPHY
	cpi_vsyncin	4	I										
	gpio8_in251	6	I										
	safe_mode	7											
J5	vdda_csiportc	0	PWR	-	-	-	-	-	-	-	-	-	Power
K4	vssa_csiportc	0	GND	-	-	-	-	-	-	-	-	-	Power
J6	csiportc_lane0y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc	Yes	No	NA	PU/PD	DPHY
	cpi_data8	3	I										
	gpio8_in252	6	I										
	safe_mode	7											
J7	csiportc_lane0x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc	Yes	No	NA	PU/PD	DPHY
	cpi_data9	3	I										
	gpio8_in253	6	I										
	safe_mode	7											
K6	csiportc_lane1y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc	Yes	No	NA	PU/PD	DPHY
	cpi_data10	3	I										
	gpio8_in254	6	I										
	safe_mode	7											
K5	csiportc_lane1x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc	Yes	No	NA	PU/PD	DPHY
	cpi_data11	3	I										
	gpio8_in255	6	I										
	safe_mode	7											
AE6	cam_shutter	0	O	Z	Z	5	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sys_nodeid0	5	I										
	gpio8_224	6	IO										
	safe_mode	7											
AE5	cam_strobe	0	O	Z	Z	5	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sys_nodeid1	5	I										
	gpio8_225	6	IO										
	safe_mode	7											
AF6	cam_globalreset	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	cam_shutter	1	O										
	cpi_fid	3	I										
	gpio8_226	6	IO										
	safe_mode	7											
AE7	timer11_pwm_evt	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	uart1_tx	2	O										
	cpi_data12	3	I										
	hw_dbg26	5	O										
	gpio8_227	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AD5	timer5_pwm_evt	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdcard_cd[14]	1	I										
	uart1_cts	2	I										
	cpi_data13	3	I										
	gpio8_228	6	IO										
	safe_mode	7											
AD6	timer6_pwm_evt	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdcard_wp[14]	1	I										
	uart1_rx	2	I										
	cpi_data14	3	I										
	gpio8_229	6	IO										
	safe_mode	7											
AD7	timer8_pwm_evt	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdcard_wp[14]	1	I										
	uart1_rts	2	O										
	cpi_data15	3	I										
	hw_dbg27	5	O										
	gpio8_230	6	IO										
	safe_mode	7											
AJ5	i2c3_scl	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I^2C Open Drain
	gpio8_231	6	IO								4		
	safe_mode	7									4		
AH4	i2c3_sda	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I^2C Open Drain
	gpio8_232	6	IO								4		
	safe_mode	7									4		
AG5	gpio8_233[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sys_secure_indicator	1	O										
	timer8_pwm_evt	2	IO										
	cpi_hsync	3	IO										
	gpio8_233[10]	6	IO										
	safe_mode	7											
AF5	gpio8_234[10]	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sys_drm_msecure	1	O										
	cpi_vsync	3	IO										
	gpio8_234[10]	6	IO										
	safe_mode	7											
W32	abe_clks	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_axr	3	IO										
	gpio4_96	6	IO										
	safe_mode	7											
AF28	abedmic_din1	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_ahclkr	3	IO										
	abemcbsp3_fsx	4	IO										
	gpio4_97	6	IO										
	safe_mode	7											
AE29	abedmic_din2	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_axr	3	IO										
	abemcbsp3_dx	4	O										
	gpio4_98	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AE28	abedmic_din3	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp3_dr	4	I										
	gpio4_99	6	IO										
	safe_mode	7											
AE27	abedmic_clk1	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp3_clkx	4	IO										
	gpio4_100	6	IO										
	safe_mode	7											
AD29	abedmic_clk2	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp1_fsx	1	IO										
	abemcasp_amutein	3	I										
	gpio4_101	6	IO										
	safe_mode	7											
AD28	abedmic_clk3	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp1_dx	1	O										
	abemcasp_aclkx	3	IO										
	gpio4_102	6	IO										
	safe_mode	7											
AF29	reserved	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp1_clkx	1	IO										
	abemcasp_afsr	3	IO										
	gpio4_103	6	IO										
	safe_mode	7											
AG29	reserved	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS BK
	abemcbsp1_dr	1	I										
	abemcasp_aclkr	3	IO										
	gpio4_104	6	IO										
	safe_mode	7											
AD26	abemcbsp2_dr	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_axr	3	IO										
	gpio4_105	6	IO										
	safe_mode	7											
AD27	abemcbsp2_dx	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_amuteout	3	O										
	gpio4_106	6	IO										
	safe_mode	7											
AA26	abemcbsp2_fsx	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_afsx	3	IO										
	gpio4_107	6	IO										
	safe_mode	7											
AA27	abemcbsp2_clkx	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcasp_ahclkx	3	IO										
	gpio4_108	6	IO										
	safe_mode	7											
AA28	abemcpdm_ul_data	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp3_dr	1	I										
	abemcasp_axr3	3	IO										
	gpio4_109	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AA29	abemcpdm_dl_data	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp3_dx	1	O										
	abemcasp_axr2	3	IO										
	gpio4_110	6	IO										
	safe_mode	7											
Y29	abemcpdm_frame	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp3_clkx	1	IO										
	abemcasp_axr1	3	IO										
	gpio4_111	6	IO										
	safe_mode	7											
Y28	abemcpdm_lb_clk	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	abemcbsp3_fsx	1	IO										
	gpio4_112	6	IO										
	safe_mode	7											
AH25	wlsdio_clk	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi4_clk	1	IO										
	gpio5_128	6	IO										
	safe_mode	7											
AG25	wlsdio_cmd	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio5_129	6	IO										
	safe_mode	7											
AJ26	wlsdio_data0	0	IO	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi4_simo	1	IO										
	gpio5_130	6	IO										
	safe_mode	7											
AH26	wlsdio_data1	0	IO	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi4_somi	1	IO										
	gpio5_131	6	IO										
	safe_mode	7											
AK28	wlsdio_data2	0	IO	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	mcspi4_cs0	1	IO										
	gpio5_132	6	IO										
	safe_mode	7											
AJ27	wlsdio_data3	0	IO	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio5_133	6	IO										
	safe_mode	7											
AL32	uart5_rx	0	I	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdio4_data1	4	IO										
	hw_dbg28	5	O										
	gpio5_134	6	IO										
	safe_mode	7											
AL31	uart5_tx	0	O	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdio4_data2	4	IO										
	hw_dbg29	5	O										
	gpio5_135	6	IO										
	safe_mode	7											
AK31	uart5_cts	0	I	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdio4_data0	4	IO										
	hw_dbg30	5	O										
	gpio5_136	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AK32	uart5_rts	0	O	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdio4_data3	4	IO										
	hw_dbg31	5	O										
	gpio5_137	6	IO										
	safe_mode	7											
AL33	i2c2_scl	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I²C Open Drain
	gpio5_138	6	IO								4		
	safe_mode	7									4		
AM32	i2c2_sda	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I²C Open Drain
	gpio5_139	6	IO								4		
	safe_mode	7									4		
AM30	mcspi1_clk	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio5_140	6	IO										
	safe_mode	7											
AL30	mcspi1_somi	0	I	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbd0_ulpiphy_nxt	5	I										
	gpio5_141	6	IO										
	safe_mode	7											
AL29	mcspi1_simo	0	IO	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbd0_ulpiphy_dir	5	I										
	gpio5_142	6	IO										
	safe_mode	7											
AN31	mcspi1_cs0	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbd0_ulpiphy_data0	5	IO										
	gpio5_143	6	IO										
	safe_mode	7											
AM31	mcspi1_cs1	0	O	L	L	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	usbd0_ulpiphy_data1	5	IO										
	gpio5_144	6	IO										
	safe_mode	7											
AL28	i2c5_scl	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I²C Open Drain
	uart4_rx	2	I								4		
	gpio5_147	6	IO								4		
	safe_mode	7									4		
AM29	i2c5_sda	0	IOD	H	H	7	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-GPIO[4]	LVCMOS I²C Open Drain
	uart4_tx	2	O								4		
	gpio5_148	6	IO								4		
	safe_mode	7									4		
AN29	uart6_rts	0	O	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sys_ndmareq0	1	I										
	sdio5_data0	3	IO										
	usbb2_mm_txse0	4	IO										
	usbd0_ulpiphy_stp	5	O										
	gpio5_152	6	IO										
	safe_mode	7											
AJ25	uart3_cts_rctx	0	IO	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sata_actled	1	O										
	sdio5_data7	3	IO										
	usbb2_mm_txen	4	IO										
	usbd0_ulpiphy_data4	5	IO										
	gpio5_153	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AJ24	uart3_rts_irsd	0	O	H	H	7	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS Tri-State Open Drain
	hdq_sio	1	IOD										
	sdio5_data6	3	IO										
	usbb2_mm_txdat	4	IO										
	usbd0_ulpiphy_data5	5	IO										
	gpio5_154	6	IO										
	safe_mode	7											
AG24	uart3_tx_irtx	0	O	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdio5_data5	3	IO										
	sdio4_clk	4	O										
	usbd0_ulpiphy_data6	5	IO										
	gpio5_155	6	IO										
	safe_mode	7											
AH24	uart3_rx_irrx	0	I	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	sdio5_data4	3	IO										
	sdio4_cmd	4	IO										
	usbd0_ulpiphy_data7	5	IO										
	gpio5_156	6	IO										
	safe_mode	7											
K26	usbb3_hsic_strobe	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
	gpio5_158	6	IO										
	safe_mode	7											
K27	usbb3_hsic_data	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
	gpio5_159	6	IO										
	safe_mode	7											
E9	vdda_sata	0	PWR	-	-	-	-	-	-	-	-	-	Power
D10	vssa_sata	0	GND	-	-	-	-	-	-	-	-	-	Power
G9	sata_tx	0	ODS	Z	Z	0	1.8 V	vdda_sata	No	No	3	No	SATAPHY
F9	sata_ty	0	ODS	Z	Z	0	1.8 V	vdda_sata	No	No	3	No	SATAPHY
E10	sata_rx	0	IDS	Z	Z	0	1.8 V	vdda_sata	No	No	NA	NA	SATAPHY
F10	sata_ry	0	IDS	Z	Z	0	1.8 V	vdda_sata	No	No	NA	NA	SATAPHY
E5	vdds_sdcard	0	PWR	-	-	-	-	-	-	-	-	-	Power
F8	sdcard_clk[14]	0	O	L	L	0	3.0 V or 1.8 V	vdds_ sdcard	Yes	See [9]	2[9]	PUx / PDy[6]	LVCMOS SDCARD
	jtag_rtck	3	O										
	n_clk	5	O										
	safe_mode	7											
E8	sdcard_cmd[14]	0	IO	L	L	0	3.0 V or 1.8 V	vdds_ sdcard	Yes	See [9]	2[9]	PUx / PDy[6]	LVCMOS SDCARD
	jtag_tdo	3	O										
	uart6_rx	4	I										
	n_d2	6	O										
	safe_mode	7											
H6	sdcard_data0[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_ sdcard	Yes	See [9]	2[9]	PUx / PDy[6]	LVCMOS SDCARD
	jtag_tdi	3	I										
	n_d0	5	O										
	safe_mode	7											
H5	sdcard_data1[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_ sdcard	Yes	See [9]	2[9]	PUx / PDy[6]	LVCMOS SDCARD
	jtag_ntrst	3	I										
	n_d1	5	O										
	safe_mode	7											
G5	sdcard_data2[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_ sdcard	Yes	See [9]	2[9]	PUx / PDy[6]	LVCMOS SDCARD
	jtag_tmsc	3	IO										
	n_d2	5	O										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
E7	sdcard_data3[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_ sdcard	Yes	See [9]	2[9]	PUx / PDy[6]	LVCMOS SDCARD
	jtag_tck	3	I										
	n_d3	5	O										
	safe_mode	7											
AE18	vdds_usbhs18	0	PWR	-	-	-	-	-	-	-	-	-	Power
AN21	vdda_usbhs33	0	PWR	-	-	-	-	-	-	-	-	-	Power
AK20	vssa_usbhs	0	GND	-	-	-	-	-	-	-	-	-	Power
AL19	usbd0_hs_dp	0	IODS	H	H	0	3.3 V	vdda_ usbhs33	No	No	See [16]	See [17]	USB2PHY
	uart3_rx_irrx	4	I										
	safe_mode	7											
AM19	usbd0_hs_dm	0	IODS	L	L	0	3.3 V	vdda_ usbhs33	No	No	See [16]	See [17]	USB2PHY
	uart3_tx_irtx	4	O										
	safe_mode	7											
AN19	usbphy_ce	0	O	0	Z	0	3.3 V	vdda_ usbhs33	No	No	See [16]	NA	USB2PHY
AE19	vdda_usbss18	0	PWR	-	-	-	-	-	-	-	-		Power
AK21	vssa_usbss	0	GND	-	-	-	-	-	-	-	-		Power
AL20	usbd0_ss_tx	0	ODS	Z	Z	0	1.8 V	vdda_ usbss18	No	No	5	No	USB3PHY
AM20	usbd0_ss_ty	0	ODS	Z	Z	0	1.8 V	vdda_ usbss18	No	No	5	No	USB3PHY
AL21	usbd0_ss_rx	0	IDS	Z	Z	0	1.8 V	vdda_ usbss18	No	No	NA	NA	USB3PHY
AM21	usbd0_ss_ry	0	IDS	Z	Z	0	1.8 V	vdda_ usbss18	No	No	NA	NA	USB3PHY
K32	drm_emu0	0	IO	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg6	5	O										
	gpio1_wk6	6	IO										
	safe_mode	7											
K31	drm_emu1	0	IO	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg7	5	O										
	gpio1_wk7	6	IO										
	safe_mode	7											
B32	jtag_ntrst	0	I	L	L	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	safe_mode	7											
C31	jtag_tck	0	I	L	L	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	safe_mode	7											
B33	jtag_rtck	0	O	L	L	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	safe_mode	7											
B31	jtag_tmsc	0	IO	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS BK
	safe_mode	7											
A32	jtag_tdi	0	I	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	safe_mode	7											
A33	jtag_tdo	0	O	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	safe_mode	7											
L31	sys_32k	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
J24	vdds_osc	0	PWR	-	-	-	-	-	-	-	-	-	Power
L30	vssa_xtal	0	GND	-	-	-	-	-	-	-	-	-	Power
L32	fref_xtal_in	0	I-AI	Z	Z	0	1.8 V	vdds_osc	Yes	No	NA	No	LVCMOS OSC
M32	fref_xtal_out	0	AO	Z	NA	0	1.8 V	vdds_osc	Yes	No	NA	No	OSC
L33	fref_xtal_clk	0	O-AO	0	Z	0	1.8 V	vdds_osc	Yes	No	NA	No	LVCMOS OSC
N31	fref_clk_ioreq	0	IO	L	L	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	gpio1_wk13	6	IO										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
M31	fref_clk0_out	0	O	L	0	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg9	5	O										
	gpio1_wk12	6	IO										
	safe_mode	7											
P31	fref_clk1_out	0	O	L	L	7	1.2 V or 1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg5	5	O										
	gpio1_wk11	6	IO										
	safe_mode	7											
N33	sys_nrespwron	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4	PUx / PDy[7]	LVCMOS
N32	sys_nreswarm	0	IOD	0	H	0	1.8 V	vdds_1p8	Yes	Yes	4	PUx / PDy[7]	LVCMOS Tri-State Open Drain
T31	sys_pwr_req	0	O	H	1	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	hw_wkdbg15	5	O										
	safe_mode	7											
R32	sr_pmic_scl	0	IOD	H	H	0	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy[4]	LVCMOS Open Drain
R31	sr_pmic_sda	0	IOD	H	H	0	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy[4]	LVCMOS Open Drain
R33	sys_nirq1	0	I	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PUx / PDy[4]	LVCMOS
	gpio1_wk16	6	IO										
T32	sys_nirq2	0	I	H	H	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PUx / PDy[4]	LVCMOS
	gpio1_wk17	6	IO										
P29	i2c1_pmic_scl	0	OD	H	H	0	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-OD[4]	I^2C Open Drain
P28	i2c1_pmic_sda	0	OD	H	H	0	1.8 V	vdds_1p8	Yes	No	3	PUx / PDy-OD[4]	I^2C Open Drain
U31	sys_boot0	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	drm_emu2	3	O										
	drm_emu15	4	O										
	hw_wkdbg0	5	O										
	gpio1_wkout0	6	O										
	safe_mode	7											
U32	sys_boot1	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	drm_emu3	3	O										
	drm_emu16	4	O										
	hw_wkdbg1	5	O										
	gpio1_wkout1	6	O										
	safe_mode	7											
U33	sys_boot2	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	drm_emu4	3	O										
	drm_emu17	4	O										
	hw_wkdbg2	5	O										
	gpio1_wkout2	6	O										
	safe_mode	7											
V31	sys_boot3	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	drm_emu5	3	O										
	drm_emu18	4	O										
	hw_wkdbg3	5	O										
	gpio1_wkout3	6	O										
	safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
V32	sys_boot4	0	I	Z	Z	0	1.8 V	vdds_1p8	Yes	Yes	4[8]	PU/PD	LVCMOS
	drm_emu6	3	O										
	drm_emu19	4	O										
	hw_wkdbg4	5	O										
	gpio1_wkout4	6	O										
	safe_mode	7											
A29	ddrch1_dm0	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B24	ddrch1_dm1	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C30	ddrch1_dm2	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B6	ddrch1_dm3	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C28	ddrch1_dq0	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
A31	ddrch1_dq1	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C29	ddrch1_dq2	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B30	ddrch1_dq3	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B29	ddrch1_dq4	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C26	ddrch1_dq5	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B28	ddrch1_dq6	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B26	ddrch1_dq7	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C23	ddrch1_dq8	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C22	ddrch1_dq9	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C21	ddrch1_dq10	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B22	ddrch1_dq11	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C24	ddrch1_dq12	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C25	ddrch1_dq13	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B25	ddrch1_dq14	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
A25	ddrch1_dq15	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
E31	ddrch1_dq16	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
E33	ddrch1_dq17	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
E32	ddrch1_dq18	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
F32	ddrch1_dq19	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C33	ddrch1_dq20	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
D30	ddrch1_dq21	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
F31	ddrch1_dq22	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C32	ddrch1_dq23	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C6	ddrch1_dq24	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
A5	ddrch1_dq25	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B5	ddrch1_dq26	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C5	ddrch1_dq27	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B2	ddrch1_dq28	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
B3	ddrch1_dq29	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C3	ddrch1_dq30	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
D4	ddrch1_dq31	0	IO	L	L	0	1.5 V	vdds_ ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C27	ddrch1_dqs0	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
B23	ddrch1_dqs1	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
D31	ddrch1_dqs2	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
C4	ddrch1_dqs3	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
B27	ddrch1_ndqs0	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
A23	ddrch1_ndqs1	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
D32	ddrch1_ndqs2	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
B4	ddrch1_ndqs3	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch1	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
A19	ddrch1_vref_dq	0	PWR	Z	NA	0	0.5 × vdds_ ddr_ch1	vdds_ ddr_ch1	Yes	No	-	NA	Analog
J16	vddq_vref_ddrch1	0	PWR	-	-	-	-	-	-	-	-	-	-
A27 / A11 / A3 / H30 / H10 / J19 / J18 / J10 / K30 / K25 / K23 / K15 / K14 / L25 / M25 / A21	vdds_ddr_ch1	0	PWR	-	-	-	-	-	-	-	-	-	Power
J1	ddrch2_dm0	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AJ3	ddrch2_dm1	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
G1	ddrch2_dm2	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AL4	ddrch2_dm3	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
K3	ddrch2_dq0	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
H2	ddrch2_dq1	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
H3	ddrch2_dq2	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
J3	ddrch2_dq3	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
J2	ddrch2_dq4	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
M3	ddrch2_dq5	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
L2	ddrch2_dq6	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
L1	ddrch2_dq7	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AK3	ddrch2_dq8	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AG1	ddrch2_dq9	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
AH3	ddrch2_dq10	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AJ2	ddrch2_dq11	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AH2	ddrch2_dq12	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AL1	ddrch2_dq13	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AL3	ddrch2_dq14	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AK4	ddrch2_dq15	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
G3	ddrch2_dq16	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
D3	ddrch2_dq17	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C2	ddrch2_dq18	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
C1	ddrch2_dq19	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
D2	ddrch2_dq20	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
F2	ddrch2_dq21	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
G2	ddrch2_dq22	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
F3	ddrch2_dq23	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AM3	ddrch2_dq24	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AL5	ddrch2_dq25	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AM4	ddrch2_dq26	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AN3	ddrch2_dq27	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AL7	ddrch2_dq28	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AL6	ddrch2_dq29	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AM7	ddrch2_dq30	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
AM6	ddrch2_dq31	0	IO	L	L	0	1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR
K2	ddrch2_dqs0	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
AK2	ddrch2_dqs1	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
E2	ddrch2_dqs2	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
AM5	ddrch2_dqs3	0	IODS	L	L	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
L3	ddrch2_ndqs0	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
AL2	ddrch2_ndqs1	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
E3	ddrch2_ndqs2	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
AN5	ddrch2_ndqs3	0	IODS	H	H	0	1.5 V	vdds_ ddr_ch2	NA	NA	See [3]	PUx / PDy[3]	LVCMOS DDR
U1	ddrch2_vref_dq	0	PWR	Z	NA	0	0.5 × vdds_ ddr_ch2	vdds_ ddr_ch2	Yes	No	-	NA	Analog
V10	vddq_vref_ddrch2	0	PWR	-	-	-	-	-	-	-	-	-	-

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
E1 / J9 / K8 / N1 / R9 / T9 / V9 / W9 / AA1 / AC10 / AE12 / AE11 / AE10 / AJ1 / AM2	vdds_ddr_ch2	0	PWR	-	-	-	-	-	-	-	-	-	-
A7	ddr3ch1_a0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B7	ddr3ch1_a1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C7	ddr3ch1_a2	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B8	ddr3ch1_a3	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C8	ddr3ch1_a4	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B9	ddr3ch1_a5	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C10	ddr3ch1_a6	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B12	ddr3ch1_a7	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C12	ddr3ch1_a8	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
A13	ddr3ch1_a9	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B13	ddr3ch1_a10_ap	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C13	ddr3ch1_a11	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B14	ddr3ch1_a12_nbc	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C14	ddr3ch1_a13	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
A15	ddr3ch1_a14	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B15	ddr3ch1_a15	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C11	ddr3ch1_cka	0	IODS	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C18	ddr3ch1_ckb	0	IODS	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
C9	ddr3ch1_cke0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
A17	ddr3ch1_cke1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B11	ddr3ch1_ncka	0	IODS	H	H	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
B18	ddr3ch1_nckb	0	IODS	H	H	0	1.35 V or 1.5 V	vdds_ddr_ch1	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L

Table 2-1. Ball Characteristics[(1)] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [(2)]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
B10	ddr3ch1_ncs0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
B17	ddr3ch1_ncs1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
C15	ddr3ch1_ba0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
B16	ddr3ch1_ba1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
C16	ddr3ch1_ba2	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
C17	ddr3ch1_ncas	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
B19	ddr3ch1_nras	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
C19	ddr3ch1_nreset	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
B20	ddr3ch1_nwe	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
C20	ddr3ch1_odt0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
B21	ddr3ch1_odt1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch1	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
A9	ddr3ch1_vref_ca	0	PWR	Z	NA	0	0.5 × vdds_ ddr_ch1	vdds_ ddr_ch1	Yes	No	-	NA	Analog
AG2	ddr3ch2_a0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AG3	ddr3ch2_a1	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AF2	ddr3ch2_a2	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AF3	ddr3ch2_a3	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AE2	ddr3ch2_a4	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AE3	ddr3ch2_a5	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AC3	ddr3ch2_a6	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AB2	ddr3ch2_a7	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AB3	ddr3ch2_a8	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AA2	ddr3ch2_a9	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
AA3	ddr3ch2_a10_ap	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L
Y2	ddr3ch2_a11	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [(3)]	PUx / PDy[(3)]	LVCMOS DDR3 DDR3L

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
Y3	ddr3ch2_a12_nbc	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
W1	ddr3ch2_a13	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
W2	ddr3ch2_a14	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
W3	ddr3ch2_a15	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
AC2	ddr3ch2_cka	0	IODS	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
R2	ddr3ch2_ckb	0	IODS	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
AD2	ddr3ch2_cke0	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
U3	ddr3ch2_cke1	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
AC1	ddr3ch2_ncka	0	IODS	H	H	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
R1	ddr3ch2_nckb	0	IODS	H	H	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
AD3	ddr3ch2_ncs0	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
T2	ddr3ch2_ncs1	0	IO	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
V2	ddr3ch2_ba0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
V3	ddr3ch2_ba1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
U2	ddr3ch2_ba2	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
T3	ddr3ch2_ncas	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
R3	ddr3ch2_nras	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
P2	ddr3ch2_nreset	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
P3	ddr3ch2_nwe	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
N2	ddr3ch2_odt0	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
M2	ddr3ch2_odt1	0	O	L	L	0	1.35 V or 1.5 V	vdds_ ddr_ch2	Yes	No	See [3]	PUx / PDy[3]	LVCMOS DDR3 DDR3L
AE1	ddr3ch2_vref_ca	0	AI	Z	NA	0	0.5 × vdds_ ddr_ch2	vdds_ ddr_ch2	Yes	No	-	NA	Analog

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
J11 / K22 / K12 / K11 / K9 / L14 / L13 / L12 / L10 / M14 / M13 / M11 / M10 / N15 / N14 / N11 / P11 / W24 / W22 / Y24 / Y23 / AA23 / AB24 / AB23 / AC24 / AC22 / AC21 / AD23 / AD22 / AD20 / AD16 / AD15 / AD14 / AD12	vdd_core	0	PWR	-	-	-	-	-	-	-	-	-	-
AH21	vdd_core_sense	0	PWR	-	-	-	-	-	-	-	-	-	-
T14 / T13 / T11 / T10 / W13 / W12 / W10 / Y19 / Y15 / Y11 / Y10 / AA19 / AA16 / AA15 / AA11 / AB19 / AB15 / AB13 / AB11 / AB10 / AC20 / AC16 / AC14 / AC13 / AC12 / AD19 / AD11	vdd_mm	0	PWR	-	-	-	-	-	-	-	-	-	-
AG21	vdd_mm_sense	0	PWR	-	-	-	-	-	-	-	-	-	-
K20 / K19 / K18 / L24 / L22 / L21 / L20 / L18 / M24 / M23 / M20 / M19 / N23 / N18 / P24 / P23 / P22 / P18 / R24 / T24 / T23 / T21 / T20	vdd_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
U29	vdd_mpu_sense	0	PWR	-	-	-	-	-	-	-	-	-	-
AJ29	vss_mpu_sense	0	GND	-	-	-	-	-	-	-	-	-	-
AD9	vpp1	0	PWR	-	-	-	-	-	-	-	-	-	-
D28 / D26 / D24 / D23 / D21 / D20 / D18 / D16 / D14 / D13 / D11 / D8 / D6 / F4 / H4 / L16 / L4 / M21 / M17 / M15 / N30 / N22 / N21 / N20 / N19 / N17 / N16 / N13 / N12 / N4 / P30 / P21 / P19 / P16 / P15 / P13 / P12 / P10 / P9 / R22 / R21 / R20 / R19 / R18 / R17 / R16 / R15 / R14 / R13 / R12 / R10 / T30 / T19 / T17 / T15 / T4 / U22 / U21 / U19 / U18 / U17 / U16 / U15 / U13 / U12 / V30 / V24 / V23 / V21 / V20 / V19 / V17 / V15 / V14 / V13 / V11 / V4 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W14 / Y22 / Y21 / Y18 / Y16 / Y13 / Y12 / AA30 / AA22 / AA21 / AA20 / AA18 / AA17 / AA14 / AA13 / AA12 / AA4 / AB21 / AB20 / AB17 / AB14 / AC30 / AC18 / AC4 / AD4 / AF30 / AF4 / AH30 / AK26 / AK23 / AK14 / AK13 / F30 / AK11 / AK10 / AK8 / AK6	vss	0	PWR	-	-	-	-	-	-	-	-	-	-
Y26	vdda_dpll_core_emu_abe	0	PWR	-	-	-	-	-	-	-	-	-	-
U8	vdda_dpll_mm_l4per	0	PWR	-	-	-	-	-	-	-	-	-	-
AF24	vdda_dpll_hdmi	0	PWR	-	-	-	-	-	-	-	-	-	-
Y27	vdda_dpll_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
AE22	vdda_ldo_core	0	PWR	-	-	-	-	-	-	-	-	-	-
AE20	vdda_ldo_mm	0	PWR	-	-	-	-	-	-	-	-	-	-
J15	vdda_ldo_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
N25	vdda_ldo_emu_wkup	0	PWR	-	-	-	-	-	-	-	-	-	-
AE16	vdda_vbgap_core	0	PWR	-	-	-	-	-	-	-	-	-	-

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	SIGNAL NAME [2]	MODE [3]	TYPE [4]	BALL RESET STATE [5]	BALL RESET REL. STATE [6]	RESET REL. MODE [7]	IO VOLTAGE VALUE [8] [2]	POWER NAME [9]	SECOND POWER AVAIL. [10]	HYS [11]	BUFFER STRENGTH (mA) [12]	PULLUP/ DOWN TYPE [13]	IO CELL [14]
T25	cap_vdda_ldo_sram_ core_array	0	PWR	-	-	-	-	-	-	-	-	-	-
AG17	cap_vdda_ldo_sram_ mm_array	0	PWR	-	-	-	-	-	-	-	-	-	-
H17	cap_vdda_ldo_sram_ mpu_array	0	PWR	-	-	-	-	-	-	-	-	-	-
V25	cap_vddldo_emu_wkup	0	PWR	-	-	-	-	-	-	-	-	-	-
AD18	cap_vbb_ldo_mm	0	PWR	-	-	-	-	-	-	-	-	-	-
H13	cap_vbb_ldo_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
K16	cap_vdda_ldo_sram_ mpu_array2	0	PWR	-	-	-	-	-	-	-	-	-	-

(1) NA in this table stands for not applicable.

(2) For more information on recommended operating conditions, see Table 3-3, *Recommended Operating Conditions*.

(3) In PUx / PDy, x and y = 60 to 200 µA
The output impedance settings (or drive strengths) of this IO are programmable (34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω or 11.75 mA, 10 mA, 8.33 mA, 6.67 mA) depending on the values of the I2, I1, I0 registers. The default value is I[2:0] = 010.

(4) The pullup or pulldown can be either the standard LVCMOS 100-µA drive strength or the configurable I^2C internal pullup resistor. Naming convention:

– PUx / PDy-OD is specified: the default buffer configuration is high-speed (HS) I^2C point-to-point mode using the internal pullup resistor.

NOTE

For balls P29 / P28, i2c1_pmic_scl and i2c1_pmic_sda functional modes are I^2C only.

– PUx / PDy-GPIO is specified: the default buffer configuration is standard LVCMOS mode (non-I^2C). The internal pullup resistance programming does not apply in this mode.

These IOs have a pullupresx register that configures the internal I^2C pullup or pulldown resistor of the IO, plus two load register bits [LB1:0] that configure the I^2C load.
By default, at the reset release time, the multiplexing mode is safe_mode (that means GPIO). The I^2C function must be selected to enable this I^2C function and by default:

– For HDMI DDC (balls AM22 / AL23):
HSMODE = fast-speed mode
PULLUPSPRESX = 0, this means that the internal I^2C pullup resistor is enabled.
LB[1:0] = 00: this means a 4-kΩ pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

– For SR (balls R32/ R31):
HSMODE = fast-speed mode
PULLUPSPRESX = 0, this means that the internal I^2C pullup resistor is enabled.
LB[1:0] = 01: this means a 4-kΩ pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

– For I2C1 (balls P29 / P28):
HSMODE = fast-speed mode
PULLUPSPRESX = 0, this means that the internal I^2C pullup resistor is enabled.
LB[1:0] = 01: this means a 2.1-kΩ pullup resistor, for a load = 15 pF to 50 pF, in fast-speed mode.

– For I2C2, I2C3, I2C4, I2C5 (balls AL33 / AM32 / AJ5 / AH4 / AJ21 / AJ20 / AL28 / AM29):
HSMODE = full-speed mode
PULLUPSPRESX = 1, external PU expected on the board.

NOTE

For I2C[5:2]: external pullup or pulldown resistors can be avoided if the I2C[5:2] interfaces are activated by boot. If the interface is activated then the interface is configured in driver mode and in this case pullup or pulldown resistors are not needed. For more information on boot modes, see the OMAP543x TRM.

In I^2C mode configuration, for a full description of the internal pullup resistance programming according to the load range, see the CONTROL_I2C_0 and the CONTROL_SMART3I/O_PADCONF_0 registers in the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the

OMAP543x TRM.
In standard LVCMOS mode configuration (non-I^2C mode), for a full description of the pullup or pulldown programming, see the CONTROL_CORE_PADX registers in the Control Module / Control Module Functional Description / Pad Functional Multiplexing and Configuration section of the OMAP543x TRM.

(5) In PDy, y = 200 kΩ

(6) In PUx / PDy, x and y = 10 kΩ to 100 kΩ.

(7) The pullup / pulldown block strength is equal to: minimum = 50 µA, typical = 100 µA, maximum = 250 µA.

(8) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω. For more information on DS[1:0] register configuration, see the OMAP543x TRM.

(9) The output impedance settings of this IO cell are programmable; by default, the register value is ic[1:0] = 00, this means 44 Ω. The hysteresis function is also programmable for this IO; by default, the register value is hyst_en = 1, this means hysteresis function is enabled. For more information see the OMAP543x TRM.

(10) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AN9 / AM9 / AL9 / AM8 / AL8 / AN7 / AG5 / AF5) can output the same GPIO in mode 0 or in mode 6.

(11) For the following balls: AF14 / AG14 / AH13 / AJ13, pulldown resistor is 20 kΩ. No pullup resistor is available.

(12) See the note below.

NOTE

For SATA and USB3 SS PHYs:

- If the serial PHY is enabled, the corresponding vdda_xxx voltage supply must be supplied by a dedicated, low-noise, voltage source.
- If the serial PHY is definitively disabled:
  - The PHY voltage supply (vdda_xxx and vssa_xxx) and the associated DPLL voltage supply (vdda_dpll_xxx) are grounded for power saving.
  - The associated interface balls are left unconnected.

For HDMI PHY:

- If the serial PHY is enabled, the corresponding vdda_hdmi voltage and vdda_dpll_hdmi supplies must be supplied by dedicated low-noise voltage sources.
- If the serial PHY is definitively disabled:
  - vdda_hdmi is supplied.
  - vdda_dpll_hdmi can be grounded only if the corresponding HDMI DPLL is never used to generate the functional clock to the DISPC.
  - The associated data/clock balls are left unconnected.
  - The PHY can be put in the off power state (even if the HDMI DPLL is used).

For HDMI control interface (CEC, HPD, DDC):

- If the HDMI control interface is enabled, vdds_hdmi must be supplied by a dedicated low-noise voltage source.
- If the HDMI is definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the HDMI and the multiplexed CMOS signals are definitively disabled:
  - The voltage supply (vdds_hdmi) is grounded for power saving.
  - The associated interface balls are left unconnected.

For DSI Port A and Port C PHYs:

- If the serial PHY is enabled, the corresponding vdda_dsiportx voltage supply must be supplied by a dedicated low-noise voltage source.
- If the PHY is definitively disabled:
  - The PHY voltage supply (vdda_dsiportx and vssa_dsiportx) is grounded for power saving only if the corresponding DSI DPLL is never used to generate the functional clock to the DISPC.
  - The associated interface balls are left unconnected.

For CSI-2 PHYs:

- If the CSI-2 serial PHY is enabled, vdda_csiportx must be supplied by a dedicated low-noise voltage source.
- If the CSI-2 serial PHY is definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the CSI-2 serial PHY and the multiplexed CMOS signals are definitively disabled:
  - The PHY voltage supply (vdda_csiportx and vssa_csiportx) is grounded for power saving.
  - The associated interface balls are left unconnected.

For USB2 HS PHY:

- If the USB2 HS PHY is enabled, vdda_usbhs33 and vdds_usbhs18 must be supplied by dedicated 3.3-V and 1.8-V low-noise voltage sources.
- If the USB2 HS PHY is definitively disabled, the other multiplexed 3.3-V CMOS signals (UART3) of the interface can be enabled, vdda_usbhs33 must be supplied by a dedicated 3.3-V voltage source and vdds_usbhs18 can be supplied by the same voltage source as vdds_1p8v.
- If the USB2 HS PHY and UART3 signals are definitively disabled:
  - vdda_usbhs33 and vdds_usbhs18 are supplied.
  - The power-down bit is set to 1 (USB2PHY_PWR_CNTL.MEM_PD bit) in order to put the USB2 PHY in power-down mode and lower the leakage current from other supplies.
  - The disable charger detect is set to 1 CONTROL_USB2PHYCORE.USB2PHY_DISCHGDET bit) to disable the charger detect.
  - There are forward-biased diodes from usbd0_hs_dp, usbd0_hs_dm, and usbphy_ce pins to the vdda_usbhs33 pin.

For SDCARD interface:

– If the SDCARD functional signals are enabled, vdds_sdcard must be supplied by a 1.8-V or 3.0-V voltage source.
– If the SDCARD functional signals are definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
– If the SDCARD functional balls and the multiplexed CMOS signals are definitively disabled:
  – The interface balls are left unconnected.
  – The SDCARD_PWRDNZ bit is kept at 0.

There are two options for the associated power supply:

– vdds_sdcard is grounded.
– vdds_sdcard is supplied by a 1.8-V or 3.0-V voltage supply. In this case, it is also recommended to keep default value of SDCARD_BIAS_VMODE bit (that is, 1).

For the corresponding setting of the SDCARD_PWRDNZ and SDCARD_BIAS_VMODE bits, see the Control Module / Control Module Functional Description / Extended-Drain IO and PBIAS Cell section and the Control Module / Control Module Programming Guide section of the OMAP543x TRM.

(13) See the Caution below.

CAUTION

Some GPMC chip-select pins have a pulldown resistor enabled by default after reset and all chip-select signals gpmc_ncs[6:0] are active low.

In case of an application with several memories connected to the GPMC, for the memories connected to a chip-select whose internal pulldown resistor is enabled by default after reset (ncs1, ncs2, ncs3, or ncs4), it is necessary to disable this pulldown resistor before performing the first access to any memory. Otherwise, contention will happen because several memories will be selected at the same time.

In the particular case of memory booting via the GPMC interface (memory device must be connected to the gpmc_ncs0 pin), it is not possible to disable any pulldown resistor before the first access. As a consequence, no memory device should be connected to a chip-select whose internal pulldown resistor is enabled by default (ncs1, ncs2, ncs3, or ncs4). Otherwise, contention will prevent OMAP from booting.

For more information, see the Initialization / Preinitialization / Boot Configuration / Boot Peripheral Pin Multiplexing section of the OMAP543x TRM.

(14) On the SDCARD IOs (supporting sdcard signals in muxmode0), the PU/PD range has been changed from [10 kΩ to 100 kΩ] for ES1.0 to [10 kΩ to 40 kΩ] for ES2.0.

(15) The maximum capacitive load for the DSI low-power mode is equal to 70 pF. For more information, see Chapter 9 of the MIPI D-PHY standard v1.1. No specific capacitive load is needed in DSI high-speed mode.

(16) IO drive strength for usbd0_hs_dp and usbd0_hs_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda_usba0otg_3p3v = 3.46 V). IO drive strength for usbphy_ce: minimum 100 µA, maximum 20 mA.

(17) Minimum PU = 900 Ω, maximum PU = 3.090 kΩ and minimum PD = 14.25 kΩ, maximum PD = 24.8 kΩ. For more information, see chapter 7 of the USB2 specification, in particular the Signaling / Device Speed Identification section.

2.3 Multiplexing Characteristics

Table 2-2 describes the device multiplexing (no characteristics are available in this table).

NOTE

This table does not take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 2.4, *Signal Descriptions*.

NOTE

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the OMAP543x TRM.

NOTE

Configuring two balls to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by ball multiplexing, this pad is actually set undriven (high impedance: Z) with a potential pullup or pulldown resistor. Pullup and pulldown resistors need to be disabled to have a pure high impedance.

NOTE

All balls not described in Table 2-1 and Table 2-2 are not connected.

Table 2-2. Multiplexing Characteristics[(1)]

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
H20 / J23 / J22 / J14 / J13 / J12 / L9 / M9 / P26 / P25 / R25 / U27 / U26 / W25 / Y25 / Y9 / AA25 / AA9 / AB25 / AC25 / AC9 / AD25 / AE24 / AE21 / AE15 / AE14 / AE13 / AF21 / U28	vdds_1p8	-	-	-	-	-	-	-
AB9	vdds_emmc	-	-	-	-	-	-	-
AJ10	emmc_clk	-	-	-	-	-	gpio2_46	safe_mode
AH10	emmc_cmd	-	-	-	-	-	gpio2_47	safe_mode
AG10	emmc_data0	-	-	-	-	-	gpio2_48	safe_mode
AF10	emmc_data1	-	-	-	-	-	gpio2_49	safe_mode
AH9	emmc_data2	-	-	-	-	-	gpio2_50	safe_mode
AJ9	emmc_data3	-	-	-	-	-	gpio2_51	safe_mode
AG9	emmc_data4	-	-	-	-	-	gpio2_52	safe_mode
AJ8	emmc_data5	-	-	-	-	-	gpio2_53	safe_mode
AH8	emmc_data6	-	-	-	-	-	gpio2_54	safe_mode
AJ7	emmc_data7	-	-	-	-	-	gpio2_55	safe_mode
J21 / J20	vdds_c2c	-	-	-	-	-	-	-
J27	Reserved	-	-	kbd_row0	gpmc_ad0	-	gpio2_37	safe_mode
H28	Reserved	-	-	kbd_row1	gpmc_ad1	-	gpio2_38	safe_mode
H29	Reserved	-	-	kbd_row2	gpmc_ad2	-	gpio2_39	safe_mode
G29	Reserved	-	-	kbd_row3	gpmc_ad3	-	gpio2_40	safe_mode
E29	Reserved	-	-	kbd_row4	gpmc_ad4	-	gpio2_41	safe_mode
E27	Reserved	-	-	kbd_row5	gpmc_ad5	-	gpio2_42	safe_mode
F26	Reserved	-	-	kbd_row6	gpmc_ad6	-	gpio2_43	safe_mode
E26	Reserved	-	-	kbd_row7	gpmc_ad7	-	gpio2_44	safe_mode
J28	Reserved	-	-	kbd_row8	gpmc_clk	-	gpio2_36	safe_mode
J29	Reserved	-	-	-	gpmc_nwp	gpmc_nbe1	gpio2_35	safe_mode
E25	Reserved	-	-	-	gpmc_nadv_ale	-	gpio2_33	safe_mode
F25	Reserved	-	-	kbd_col8	gpmc_nbe0_cle	-	gpio2_34	safe_mode
J32	Reserved	-	-	kbd_col0	gpmc_ad8	hw_dbg16	gpio2_56	safe_mode
J33	Reserved	-	-	kbd_col1	gpmc_ad9	hw_dbg17	gpio2_57	safe_mode
H32	Reserved	-	-	kbd_col2	gpmc_ad10	hw_dbg18	gpio2_58	safe_mode
J31	Reserved	-	-	kbd_col3	gpmc_ad11	hw_dbg19	gpio2_59	safe_mode
G31	Reserved	-	-	kbd_col4	gpmc_ad12	hw_dbg20	gpio2_60	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
H31	Reserved	-	-	kbd_col5	gpmc_ad13	hw_dbg21	gpio2_61	safe_mode
G32	Reserved	-	-	kbd_col6	gpmc_ad14	hw_dbg22	gpio2_62	safe_mode
G33	Reserved	-	-	kbd_col7	gpmc_ad15	hw_dbg23	gpio2_63	safe_mode
G24	Reserved	-	-	-	gpmc_a16	hw_dbg24	gpio4_113	safe_mode
H24	Reserved	-	-	-	gpmc_a17	hw_dbg25	gpio4_114	safe_mode
E24	Reserved	-	-	-	gpmc_a18	hw_dbg26	gpio4_115	safe_mode
F24	Reserved	-	-	-	gpmc_a19	hw_dbg27	gpio4_116	safe_mode
G21	Reserved	-	-	-	gpmc_a20	hw_dbg28	gpio4_117	safe_mode
H21	Reserved	-	-	-	gpmc_a21	hw_dbg29	gpio4_118	safe_mode
E21	Reserved	-	-	-	gpmc_a22	hw_dbg30	gpio4_119	safe_mode
F21	Reserved	-	-	-	gpmc_a23	hw_dbg31	gpio4_120	safe_mode
P32	Reserved	-	-	-	gpmc_ncs0	-	gpio2_32	safe_mode
N27	Reserved	-	-	-	gpmc_wait0	-	gpio2_45	safe_mode
N29	Reserved	-	-	-	-	hw_wkdbg13	gpio1_wk15	safe_mode
N28	Reserved	-	-	-	-	hw_wkdbg14	gpio1_wk14	safe_mode
G20	hsi2_caready	-	-	usbb1_ulpiphy_clk	gpmc_wait1	-	gpio3_76	safe_mode
F20	hsi2_acready	-	-	usbb1_ulpiphy_nxt	gpmc_ncs1	-	gpio3_77	safe_mode
F17	hsi2_cawake	-	-	usbb1_ulpiphy_dir	gpmc_a24	-	gpio3_78	safe_mode
E20	hsi2_acwake	-	-	usbb1_ulpiphy_stp	gpmc_a25	-	gpio3_79	safe_mode
E14	hsi2_caflag	-	-	usbb1_ulpiphy_data0	gpmc_wait2	-	gpio3_80	safe_mode
F14	hsi2_cadata	-	-	usbb1_ulpiphy_data1	gpmc_ncs2	-	gpio3_81	safe_mode
G14	hsi2_acflag	-	-	usbb1_ulpiphy_data2	gpmc_ncs3	-	gpio3_82	safe_mode
E17	hsi2_acdata	-	-	usbb1_ulpiphy_data3	gpmc_ncs4	-	gpio3_83	safe_mode
F13	uart2_rts	mcspi3_somi	-	usbb1_ulpiphy_data4	gpmc_nwe	hw_dbg16	gpio3_84	safe_mode
N9	uart2_cts	mcspi3_cs0	-	usbb1_ulpiphy_data5	gpmc_noe_nre	hw_dbg17	gpio3_85	safe_mode
G13	uart2_rx	mcspi3_simo	-	usbb1_ulpiphy_data6	gpmc_ncs5	hw_dbg18	gpio3_86	safe_mode
E13	uart2_tx	mcspi3_clk	-	usbb1_ulpiphy_data7	gpmc_ncs6	hw_dbg19	gpio3_87	safe_mode
N26	vdds_hsic	-	-	-	-	-	-	-
K28	usbb2_hsic_strobe	-	-	-	-	-	gpio3_94	safe_mode
K29	usbb2_hsic_data	-	-	-	-	-	gpio3_95	safe_mode
W31	timer10_pwm_evt	-	-	-	-	-	gpio6_188	safe_mode
W33	dsiporta_te0	-	-	-	-	-	gpio6_189	safe_mode
AA33	vdda_dsiporta	-	-	-	-	-	-	-
Y30	vssa_dsiporta	-	-	-	-	-	-	-
AD31	dsiporta_lane0x	-	-	-	-	-	-	-
AD32	dsiporta_lane0y	-	-	-	-	-	-	-
AC31	dsiporta_lane1x	-	-	-	-	-	-	-
AC32	dsiporta_lane1y	-	-	-	-	-	-	-
AB32	dsiporta_lane2x	-	-	-	-	-	-	-
AB31	dsiporta_lane2y	-	-	-	-	-	-	-
AA32	dsiporta_lane3x	-	-	-	-	-	-	-
AA31	dsiporta_lane3y	-	-	-	-	-	-	-
Y32	dsiporta_lane4x	-	-	-	-	-	-	-
Y31	dsiporta_lane4y	-	-	-	-	-	-	-
AJ33	timer9_pwm_evt	sync_sof_clk	sync_usof_itp_clk	-	-	-	gpio6_190	safe_mode
AK30	dsiportc_te0	-	-	-	-	-	gpio6_191	safe_mode
AE33	vdda_dsiportc	-	-	-	-	-	-	-
AD30	vssa_dsiportc	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AJ31	dsiportc_lane0x	-	-	-	-	-	-	-
AJ32	dsiportc_lane0y	-	-	-	-	-	-	-
AH32	dsiportc_lane1x	-	-	-	-	-	-	-
AH31	dsiportc_lane1y	-	-	-	-	-	-	-
AG32	dsiportc_lane2x	-	-	-	-	-	-	-
AG31	dsiportc_lane2y	-	-	-	-	-	-	-
AF32	dsiportc_lane3x	-	-	-	-	-	-	-
AF31	dsiportc_lane3y	-	-	-	-	-	-	-
AE32	dsiportc_lane4x	-	-	-	-	-	-	-
AE31	dsiportc_lane4y	-	-	-	-	-	-	-
AN13	rfbi_hsync0	-	-	dispc_data17	kbd_col5	-	gpio6_160	safe_mode
AM13	rfbi_te_vsync0	-	-	dispc_data16	kbd_row5	jtag_sel	gpio6_161	safe_mode
AL18	rfbi_re	-	-	dispc_pclk	kbd_col4	-	gpio6_164	safe_mode
AM18	rfbi_a0	-	-	dispc_de	kbd_row4	-	gpio6_165	safe_mode
AL14	rfbi_data8	-	-	dispc_data8	kbd_col3	drm_emu12	gpio6_174	safe_mode
AM14	rfbi_data9	-	-	dispc_data9	kbd_row3	drm_emu13	gpio6_175	safe_mode
AM12	rfbi_data10	-	-	dispc_data10	kbd_row8	drm_emu14	gpio6_176	safe_mode
AL11	rfbi_data11	-	-	dispc_data11	kbd_row7	drm_emu15	gpio6_177	safe_mode
AM11	rfbi_data12	-	-	dispc_data12	kbd_row6	drm_emu16	gpio6_178	safe_mode
AN11	rfbi_data13	-	-	dispc_data13	kbd_col8	drm_emu17	gpio6_179	safe_mode
AL10	rfbi_data14	-	-	dispc_data14	kbd_col7	drm_emu18	gpio6_180	safe_mode
AM10	rfbi_data15	mcspi2_cs1	-	dispc_data15	kbd_col6	drm_emu19	gpio6_181	safe_mode
AN9	gpio6_182[2]	-	-	dispc_data18	kbd_col0	-	gpio6_182[2]	safe_mode
AM9	gpio6_183[2]	-	-	dispc_data19	kbd_col1	-	gpio6_183[2]	safe_mode
AL9	gpio6_184[2]	-	-	dispc_data20	kbd_col2	hw_dbg22	gpio6_184[2]	safe_mode
AM8	gpio6_185[2]	-	-	dispc_data21	kbd_row0	hw_dbg23	gpio6_185[2]	safe_mode
AL8	gpio6_186[2]	-	-	dispc_data22	kbd_row1	hw_dbg24	gpio6_186[2]	safe_mode
AN7	gpio6_187[2]	-	-	dispc_data23	kbd_row2	hw_dbg25	gpio6_187[2]	safe_mode
AL17	rfbi_data0	-	-	dispc_data0	jtagtapext_rtck	drm_emu4	gpio6_166	safe_mode
AM17	rfbi_data1	-	-	dispc_data1	uart3_rx_irrx	drm_emu5	gpio6_167	safe_mode
AN17	rfbi_data2	-	-	dispc_data2	uart3_tx_irtx	drm_emu6	gpio6_168	safe_mode
AL16	rfbi_data3	-	-	dispc_data3	jtagtapext_ntrst	drm_emu7	gpio6_169	safe_mode
AM16	rfbi_data4	-	-	dispc_data4	jtagtapext_tck	drm_emu8	gpio6_170	safe_mode
AL15	rfbi_data5	-	-	dispc_data5	jtagtapext_tmsc	drm_emu9	gpio6_171	safe_mode
AM15	rfbi_data6	-	-	dispc_data6	jtagtapext_tdo	drm_emu10	gpio6_172	safe_mode
AN15	rfbi_data7	-	-	dispc_data7	jtagtapext_tdi	drm_emu11	gpio6_173	safe_mode
AL13	rfbi_cs0	-	-	dispc_hsync	-	drm_emu3	gpio6_163	safe_mode
AL12	rfbi_we	-	-	dispc_vsync	-	drm_emu2	gpio6_162	safe_mode
AF20	mcspi2_cs0	jtagtapext_ntrst	-	dispc_fid	-	-	gpio7_196	safe_mode
AH17	mcspi2_clk	jtagtapext_tck	-	-	-	-	gpio7_197	safe_mode
AG20	mcspi2_simo	jtagtapext_tmsc	-	-	-	hw_dbg20	gpio7_198	safe_mode
AH20	mcspi2_somi	jtagtapext_tdo	-	-	-	hw_dbg21	gpio7_199	safe_mode
AJ21	i2c4_scl	jtagtapext_tdi	-	-	-	-	gpio7_200	safe_mode
AJ20	i2c4_sda	jtagtapext_rtck	-	-	-	-	gpio7_201	safe_mode
AE23	vdds_hdmi	-	-	-	-	-	-	-
AN23	hdmi_cec	-	-	-	-	-	gpio7_192	safe_mode
AM23	hdmi_hpd	-	-	-	-	-	gpio7_193	safe_mode
AM22	hdmi_ddc_scl	-	-	-	-	-	gpio7_194	safe_mode
AL23	hdmi_ddc_sda	-	-	-	-	-	gpio7_195	safe_mode
AN25	vdda_hdmi	-	-	-	-	-	-	-
AK24	vssa_hdmi	-	-	-	-	-	-	-
AL24	hdmi_clkx	-	-	-	-	-	-	-
AM24	hdmi_clky	-	-	-	-	-	-	-
AL25	hdmi_data0x	-	-	-	-	-	-	-
AM25	hdmi_data0y	-	-	-	-	-	-	-
AL26	hdmi_data1x	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AM26	hdmi_data1y	-	-	-	-	-	-	-
AL27	hdmi_data2x	-	-	-	-	-	-	-
AM27	hdmi_data2y	-	-	-	-	-	-	-
N3	vdda_csiporta	-	-	-	-	-	-	-
P4	vssa_csiporta	-	-	-	-	-	-	-
U6	csiporta_lane0x	-	-	cpi_pclk	-	-	gpio8_in236	safe_mode
U5	csiporta_lane0y	-	-	cpi_wen	-	-	gpio8_in237	safe_mode
P5	csiporta_lane1y	-	-	cpi_data0	-	-	gpio8_in238	safe_mode
P6	csiporta_lane1x	-	-	cpi_data1	-	-	gpio8_in239	safe_mode
P8	csiporta_lane2y	-	-	cpi_data2	-	-	gpio8_in240	safe_mode
P7	csiporta_lane2x	-	-	cpi_data3	-	-	gpio8_in241	safe_mode
N5	csiporta_lane3x	-	-	cpi_data4	-	-	gpio8_in242	safe_mode
N6	csiporta_lane3y	-	-	cpi_data5	-	-	gpio8_in243	safe_mode
N7	csiporta_lane4x	-	-	cpi_data6	-	-	gpio8_in244	safe_mode
N8	csiporta_lane4y	-	-	cpi_data7	-	-	gpio8_in245	safe_mode
AA7	vdda_csiportb	-	-	-	-	-	-	-
Y4	vssa_csiportb	-	-	-	-	-	-	-
Y6	csiportb_lane0x	-	-	-	cpi_data12	-	gpio8_in246	safe_mode
Y5	csiportb_lane0y	-	-	-	cpi_data13	-	gpio8_in247	safe_mode
Y7	csiportb_lane1y	-	-	-	cpi_data14	-	gpio8_in248	safe_mode
Y8	csiportb_lane1x	-	-	-	cpi_data15	-	gpio8_in249	safe_mode
AA5	csiportb_lane2y	-	-	-	cpi_hsyncin	-	gpio8_in250	safe_mode
AA6	csiportb_lane2x	-	-	-	cpi_vsyncin	-	gpio8_in251	safe_mode
J5	vdda_csiportc	-	-	-	-	-	-	-
K4	vssa_csiportc	-	-	-	-	-	-	-
J6	csiportc_lane0y	-	-	cpi_data8	-	-	gpio8_in252	safe_mode
J7	csiportc_lane0x	-	-	cpi_data9	-	-	gpio8_in253	safe_mode
K6	csiportc_lane1y	-	-	cpi_data10	-	-	gpio8_in254	safe_mode
K5	csiportc_lane1x	-	-	cpi_data11	-	-	gpio8_in255	safe_mode
AE6	cam_shutter	-	-	-	-	sys_nodeid0	gpio8_224	safe_mode
AE5	cam_strobe	-	-	-	-	sys_nodeid1	gpio8_225	safe_mode
AF6	cam_globalreset	cam_shutter	-	cpi_fid	-	-	gpio8_226	safe_mode
AE7	timer11_pwm_evt	-	uart_tx	cpi_data12	-	hw_dbg26	gpio8_227	safe_mode
AD5	timer5_pwm_evt	sdcard_cd	uart_cts	cpi_data13	-	-	gpio8_228	safe_mode
AD6	timer6_pwm_evt	sdcard_wp	uart_rx	cpi_data14	-	-	gpio8_229	safe_mode
AD7	timer8_pwm_evt	sdcard_wp	uart_rts	cpi_data15	-	hw_dbg27	gpio8_230	safe_mode
AJ5	i2c3_scl	-	-	-	-	-	gpio8_231	safe_mode
AH4	i2c3_sda	-	-	-	-	-	gpio8_232	safe_mode
AG5	gpio8_233[2]	sys_secure_ indicator	timer8_pwm_ evt	cpi_hsync	-	-	gpio8_233[2]	safe_mode
AF5	gpio8_234[2]	sys_drm_msecure	-	cpi_vsync	-	-	gpio8_234[2]	safe_mode
W32	abe_clks	-	-	abemcasp_axr	-	-	gpio4_96	safe_mode
AF28	abedmic_din1	-	-	abemcasp_ahclkr	abemcbsp3_fsx	-	gpio4_97	safe_mode
AE29	abedmic_din2	-	-	abemcasp_axr	abemcbsp3_dx	-	gpio4_98	safe_mode
AE28	abedmic_din3	-	-	-	abemcbsp3_dr	-	gpio4_99	safe_mode
AE27	abedmic_clk1	-	-	-	abemcbsp3_clkx	-	gpio4_100	safe_mode
AD29	abedmic_clk2	abemcbsp1_fsx	-	abemcasp_ amutein	-	-	gpio4_101	safe_mode
AD28	abedmic_clk3	abemcbsp1_dx	-	abemcasp_aclkx	-	-	gpio4_102	safe_mode
AF29	reserved	abemcbsp1_clkx	-	abemcasp_afsr	-	-	gpio4_103	safe_mode
AG29	reserved	abemcbsp1_dr	-	abemcasp_aclkr	-	-	gpio4_104	safe_mode
AD26	abemcbsp2_dr	-	-	abemcasp_axr	-	-	gpio4_105	safe_mode
AD27	abemcbsp2_dx	-	-	abemcasp_ amuteout	-	-	gpio4_106	safe_mode
AA26	abemcbsp2_fsx	-	-	abemcasp_afsx	-	-	gpio4_107	safe_mode
AA27	abemcbsp2_clkx	-	-	abemcasp_ahclkx	-	-	gpio4_108	safe_mode
AA28	abemcpdm_ul_data	abemcbsp3_dr	-	abemcasp_axr3	-	-	gpio4_109	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AA29	abemcpdm_dl_data	abemcbsp3_dx	-	abemcasp_axr2	-	-	gpio4_110	safe_mode
Y29	abemcpdm_frame	abemcbsp3_clkx	-	abemcasp_axr1	-	-	gpio4_111	safe_mode
Y28	abemcpdm_lb_clk	abemcbsp3_fsx	-	-	-	-	gpio4_112	safe_mode
AH25	wlsdio_clk	mcspi4_clk	-	-	-	-	gpio5_128	safe_mode
AG25	wlsdio_cmd	-	-	-	-	-	gpio5_129	safe_mode
AJ26	wlsdio_data0	mcspi4_simo	-	-	-	-	gpio5_130	safe_mode
AH26	wlsdio_data1	mcspi4_somi	-	-	-	-	gpio5_131	safe_mode
AK28	wlsdio_data2	mcspi4_cs0	-	-	-	-	gpio5_132	safe_mode
AJ27	wlsdio_data3	-	-	-	-	-	gpio5_133	safe_mode
AL32	uart5_rx	-	-	-	sdio4_data1	hw_dbg28	gpio5_134	safe_mode
AL31	uart5_tx	-	-	-	sdio4_data2	hw_dbg29	gpio5_135	safe_mode
AK31	uart5_cts	-	-	-	sdio4_data0	hw_dbg30	gpio5_136	safe_mode
AK32	uart5_rts	-	-	-	sdio4_data3	hw_dbg31	gpio5_137	safe_mode
AL33	i2c2_scl	-	-	-	-	-	gpio5_138	safe_mode
AM32	i2c2_sda	-	-	-	-	-	gpio5_139	safe_mode
AM30	mcspi1_clk	-	-	-	-	usbd0_ulpiphy_clk	gpio5_140	safe_mode
AL30	mcspi1_somi	-	-	-	-	usbd0_ulpiphy_nxt	gpio5_141	safe_mode
AL29	mcspi1_simo	-	-	-	-	usbd0_ulpiphy_dir	gpio5_142	safe_mode
AN31	mcspi1_cs0	-	-	-	-	usbd0_ulpiphy_data0	gpio5_143	safe_mode
AM31	mcspi1_cs1	-	-	-	-	usbd0_ulpiphy_data1	gpio5_144	safe_mode
AL28	i2c5_scl	-	uart4_rx	-	-	-	gpio5_147	safe_mode
AM29	i2c5_sda	-	uart4_tx	-	-	-	gpio5_148	safe_mode
AN29	uart6_rts	sys_ndmareq0	-	sdio5_data0	usbb2_mm_txse0	usbd0_ulpiphy_stp	gpio5_152	safe_mode
AJ25	uart3_cts_rctx	sata_actled	-	sdio5_data7	usbb2_mm_txen	usbd0_ulpiphy_data4	gpio5_153	safe_mode
AJ24	uart3_rts_irsd	hdq_sio	-	sdio5_data6	usbb2_mm_txdat	usbd0_ulpiphy_data5	gpio5_154	safe_mode
AG24	uart3_tx_irtx	-	-	sdio5_data5	sdio4_clk	usbd0_ulpiphy_data6	gpio5_155	safe_mode
AH24	uart3_rx_irrx	-	-	sdio5_data4	sdio4_cmd	usbd0_ulpiphy_data7	gpio5_156	safe_mode
K26	usbb3_hsic_strobe	-	-	-	-	-	gpio5_158	safe_mode
K27	usbb3_hsic_data	-	-	-	-	-	gpio5_159	safe_mode
E9	vdda_sata	-	-	-	-	-	-	-
D10	vssa_sata	-	-	-	-	-	-	-
G9	sata_tx	-	-	-	-	-	-	-
F9	sata_ty	-	-	-	-	-	-	-
E10	sata_rx	-	-	-	-	-	-	-
F10	sata_ry	-	-	-	-	-	-	-
E5	vdds_sdcard	-	-	-	-	-	-	-
F8	sdcard_clk	-	-	jtag_rtck	-	n_clk	-	safe_mode
E8	sdcard_cmd	-	-	jtag_tdo	uart6_rx	-	n_d2	safe_mode
H6	sdcard_data0	-	-	jtag_tdi	-	n_d0	-	safe_mode
H5	sdcard_data1	-	-	jtag_ntrst	-	n_d1	-	safe_mode
G5	sdcard_data2	-	-	jtag_tmsc	-	n_d2	-	safe_mode
E7	sdcard_data3	-	-	jtag_tck	-	n_d3	-	safe_mode
AE18	vdds_usbhs18	-	-	-	-	-	-	-
AN21	vdda_usbhs33	-	-	-	-	-	-	-
AK20	vssa_usbhs	-	-	-	-	-	-	-
AL19	usbd0_hs_dp	-	-	-	uart3_rx_irrx	-	-	safe_mode
AM19	usbd0_hs_dm	-	-	-	uart3_tx_irtx	-	-	safe_mode
AN19	usbphy_ce	-	-	-	-	-	-	-
AE19	vdda_usbss18	-	-	-	-	-	-	-
AK21	vssa_usbss	-	-	-	-	-	-	-
AL20	usbd0_ss_tx	-	-	-	-	-	-	-
AM20	usbd0_ss_ty	-	-	-	-	-	-	-
AL21	usbd0_ss_rx	-	-	-	-	-	-	-
AM21	usbd0_ss_ry	-	-	-	-	-	-	-
K32	drm_emu0	-	-	-	-	hw_wkdbg6	gpio1_wk6	safe_mode
K31	drm_emu1	-	-	-	-	hw_wkdbg7	gpio1_wk7	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
B32	jtag_ntrst	-	-	-	-	-	-	safe_mode
C31	jtag_tck	-	-	-	-	-	-	safe_mode
B33	jtag_rtck	-	-	-	-	-	-	safe_mode
B31	jtag_tmsc	-	-	-	-	-	-	safe_mode
A32	jtag_tdi	-	-	-	-	-	-	safe_mode
A33	jtag_tdo	-	-	-	-	-	-	safe_mode
L31	sys_32k	-	-	-	-	-	-	-
J24	vdds_osc							
L30	vssa_xtal	-	-	-	-	-	-	-
L32	fref_xtal_in	-	-	-	-	-	-	-
M32	fref_xtal_out	-	-	-	-	-	-	-
L33	fref_xtal_clk	-	-	-	-	-	-	-
N31	fref_clk_ioreq	-	-	-	-	-	gpio1_wk13	safe_mode
M31	fref_clk0_out	-	-	-	-	hw_wkdbg9	gpio1_wk12	safe_mode
P31	fref_clk1_out	-	-	-	-	hw_wkdbg5	gpio1_wk11	safe_mode
N33	sys_nrespwron	-	-	-	-	-	-	-
N32	sys_nreswarm	-	-	-	-	-	-	-
T31	sys_pwr_req	-	-	-	-	hw_wkdbg15	-	safe_mode
R32	sr_pmic_scl	-	-	-	-	-	-	-
R31	sr_pmic_sda	-	-	-	-	-	-	-
R33	sys_nirq1	-	-	-	-	-	gpio1_wk16	-
T32	sys_nirq2	-	-	-	-	-	gpio1_wk17	-
P29	i2c1_pmic_scl	-	-	-	-	-	-	-
P28	i2c1_pmic_sda	-	-	-	-	-	-	-
U31	sys_boot0	-	-	drm_emu2	drm_emu15	hw_wkdbg0	gpio1_wkout0	safe_mode
U32	sys_boot1	-	-	drm_emu3	drm_emu16	hw_wkdbg1	gpio1_wkout1	safe_mode
U33	sys_boot2	-	-	drm_emu4	drm_emu17	hw_wkdbg2	gpio1_wkout2	safe_mode
V31	sys_boot3	-	-	drm_emu5	drm_emu18	hw_wkdbg3	gpio1_wkout3	safe_mode
V32	sys_boot4	-	-	drm_emu6	drm_emu19	hw_wkdbg4	gpio1_wkout4	safe_mode
A29	ddrch1_dm0	-	-	-	-	-	-	-
B24	ddrch1_dm1	-	-	-	-	-	-	-
C30	ddrch1_dm2	-	-	-	-	-	-	-
B6	ddrch1_dm3	-	-	-	-	-	-	-
C28	ddrch1_dq0	-	-	-	-	-	-	-
A31	ddrch1_dq1	-	-	-	-	-	-	-
C29	ddrch1_dq2	-	-	-	-	-	-	-
B30	ddrch1_dq3	-	-	-	-	-	-	-
B29	ddrch1_dq4	-	-	-	-	-	-	-
C26	ddrch1_dq5	-	-	-	-	-	-	-
B28	ddrch1_dq6	-	-	-	-	-	-	-
B26	ddrch1_dq7	-	-	-	-	-	-	-
C23	ddrch1_dq8	-	-	-	-	-	-	-
C22	ddrch1_dq9	-	-	-	-	-	-	-
C21	ddrch1_dq10	-	-	-	-	-	-	-
B22	ddrch1_dq11	-	-	-	-	-	-	-
C24	ddrch1_dq12	-	-	-	-	-	-	-
C25	ddrch1_dq13	-	-	-	-	-	-	-
B25	ddrch1_dq14	-	-	-	-	-	-	-
A25	ddrch1_dq15	-	-	-	-	-	-	-
E31	ddrch1_dq16	-	-	-	-	-	-	-
E33	ddrch1_dq17	-	-	-	-	-	-	-
E32	ddrch1_dq18	-	-	-	-	-	-	-
F32	ddrch1_dq19	-	-	-	-	-	-	-
C33	ddrch1_dq20	-	-	-	-	-	-	-
D30	ddrch1_dq21	-	-	-	-	-	-	-
F31	ddrch1_dq22	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
C32	ddrch1_dq23	-	-	-	-	-	-	-
C6	ddrch1_dq24	-	-	-	-	-	-	-
A5	ddrch1_dq25	-	-	-	-	-	-	-
B5	ddrch1_dq26	-	-	-	-	-	-	-
C5	ddrch1_dq27	-	-	-	-	-	-	-
B2	ddrch1_dq28	-	-	-	-	-	-	-
B3	ddrch1_dq29	-	-	-	-	-	-	-
C3	ddrch1_dq30	-	-	-	-	-	-	-
D4	ddrch1_dq31	-	-	-	-	-	-	-
C27	ddrch1_dqs0	-	-	-	-	-	-	-
B23	ddrch1_dqs1	-	-	-	-	-	-	-
D31	ddrch1_dqs2	-	-	-	-	-	-	-
C4	ddrch1_dqs3	-	-	-	-	-	-	-
B27	ddrch1_ndqs0	-	-	-	-	-	-	-
A23	ddrch1_ndqs1	-	-	-	-	-	-	-
D32	ddrch1_ndqs2	-	-	-	-	-	-	-
B4	ddrch1_ndqs3	-	-	-	-	-	-	-
A19	ddrch1_vref_dq	-	-	-	-	-	-	-
J16	vddq_vref_ddrch1	-	-	-	-	-	-	-
A27 / A11 / A3 / H30 / H10 / J19 / J18 / J10 / K30 / K25 / K23 / K15 / K14 / L25 / M25 / A21	vdds_ddr_ch1	-	-	-	-	-	-	-
J1	ddrch2_dm0	-	-	-	-	-	-	-
AJ3	ddrch2_dm1	-	-	-	-	-	-	-
G1	ddrch2_dm2	-	-	-	-	-	-	-
AL4	ddrch2_dm3	-	-	-	-	-	-	-
K3	ddrch2_dq0	-	-	-	-	-	-	-
H2	ddrch2_dq1	-	-	-	-	-	-	-
H3	ddrch2_dq2	-	-	-	-	-	-	-
J3	ddrch2_dq3	-	-	-	-	-	-	-
J2	ddrch2_dq4	-	-	-	-	-	-	-
M3	ddrch2_dq5	-	-	-	-	-	-	-
L2	ddrch2_dq6	-	-	-	-	-	-	-
L1	ddrch2_dq7	-	-	-	-	-	-	-
AK3	ddrch2_dq8	-	-	-	-	-	-	-
AG1	ddrch2_dq9	-	-	-	-	-	-	-
AH3	ddrch2_dq10	-	-	-	-	-	-	-
AJ2	ddrch2_dq11	-	-	-	-	-	-	-
AH2	ddrch2_dq12	-	-	-	-	-	-	-
AL1	ddrch2_dq13	-	-	-	-	-	-	-
AL3	ddrch2_dq14	-	-	-	-	-	-	-
AK4	ddrch2_dq15	-	-	-	-	-	-	-
G3	ddrch2_dq16	-	-	-	-	-	-	-
D3	ddrch2_dq17	-	-	-	-	-	-	-
C2	ddrch2_dq18	-	-	-	-	-	-	-
C1	ddrch2_dq19	-	-	-	-	-	-	-
D2	ddrch2_dq20	-	-	-	-	-	-	-
F2	ddrch2_dq21	-	-	-	-	-	-	-
G2	ddrch2_dq22	-	-	-	-	-	-	-
F3	ddrch2_dq23	-	-	-	-	-	-	-
AM3	ddrch2_dq24	-	-	-	-	-	-	-
AL5	ddrch2_dq25	-	-	-	-	-	-	-
AM4	ddrch2_dq26	-	-	-	-	-	-	-
AN3	ddrch2_dq27	-	-	-	-	-	-	-
AL7	ddrch2_dq28	-	-	-	-	-	-	-
AL6	ddrch2_dq29	-	-	-	-	-	-	-
AM7	ddrch2_dq30	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[(1)] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AM6	ddrch2_dq31	-	-	-	-	-	-	-
K2	ddrch2_dqs0	-	-	-	-	-	-	-
AK2	ddrch2_dqs1	-	-	-	-	-	-	-
E2	ddrch2_dqs2	-	-	-	-	-	-	-
AM5	ddrch2_dqs3	-	-	-	-	-	-	-
L3	ddrch2_ndqs0	-	-	-	-	-	-	-
AL2	ddrch2_ndqs1	-	-	-	-	-	-	-
E3	ddrch2_ndqs2	-	-	-	-	-	-	-
AN5	ddrch2_ndqs3	-	-	-	-	-	-	-
U1	ddrch2_vref_dq	-	-	-	-	-	-	-
V10	vddq_vref_ddrch2	-	-	-	-	-	-	-
E1 / J9 / K8 / N1 / R9 / T9 / V9 / W9 / AA1 / AC10 / AE12 / AE11 / AE10 / AJ1 / AM2	vdds_ddr_ch2	-	-	-	-	-	-	-
A7	ddr3ch1_a0	-	-	-	-	-	-	-
B7	ddr3ch1_a1	-	-	-	-	-	-	-
C7	ddr3ch1_a2	-	-	-	-	-	-	-
B8	ddr3ch1_a3	-	-	-	-	-	-	-
C8	ddr3ch1_a4	-	-	-	-	-	-	-
B9	ddr3ch1_a5	-	-	-	-	-	-	-
C10	ddr3ch1_a6	-	-	-	-	-	-	-
B12	ddr3ch1_a7	-	-	-	-	-	-	-
C12	ddr3ch1_a8	-	-	-	-	-	-	-
A13	ddr3ch1_a9	-	-	-	-	-	-	-
B13	ddr3ch1_a10_ap	-	-	-	-	-	-	-
C13	ddr3ch1_a11	-	-	-	-	-	-	-
B14	ddr3ch1_a12_nbc	-	-	-	-	-	-	-
C14	ddr3ch1_a13	-	-	-	-	-	-	-
A15	ddr3ch1_a14	-	-	-	-	-	-	-
B15	ddr3ch1_a15	-	-	-	-	-	-	-
C11	ddr3ch1_cka	-	-	-	-	-	-	-
C18	ddr3ch1_ckb	-	-	-	-	-	-	-
C9	ddr3ch1_cke0	-	-	-	-	-	-	-
A17	ddr3ch1_cke1	-	-	-	-	-	-	-
B11	ddr3ch1_ncka	-	-	-	-	-	-	-
B18	ddr3ch1_nckb	-	-	-	-	-	-	-
B10	ddr3ch1_ncs0	-	-	-	-	-	-	-
B17	ddr3ch1_ncs1	-	-	-	-	-	-	-
C15	ddr3ch1_ba0	-	-	-	-	-	-	-
B16	ddr3ch1_ba1	-	-	-	-	-	-	-
C16	ddr3ch1_ba2	-	-	-	-	-	-	-
C17	ddr3ch1_ncas	-	-	-	-	-	-	-
B19	ddr3ch1_nras	-	-	-	-	-	-	-
C19	ddr3ch1_nreset	-	-	-	-	-	-	-
B20	ddr3ch1_nwe	-	-	-	-	-	-	-
C20	ddr3ch1_odt0	-	-	-	-	-	-	-
B21	ddr3ch1_odt1	-	-	-	-	-	-	-
A9	ddr3ch1_vref_ca	-	-	-	-	-	-	-
AG2	ddr3ch2_a0	-	-	-	-	-	-	-
AG3	ddr3ch2_a1	-	-	-	-	-	-	-
AF2	ddr3ch2_a2	-	-	-	-	-	-	-
AF3	ddr3ch2_a3	-	-	-	-	-	-	-
AE2	ddr3ch2_a4	-	-	-	-	-	-	-
AE3	ddr3ch2_a5	-	-	-	-	-	-	-
AC3	ddr3ch2_a6	-	-	-	-	-	-	-
AB2	ddr3ch2_a7	-	-	-	-	-	-	-
AB3	ddr3ch2_a8	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AA2	ddr3ch2_a9	-	-	-	-	-	-	-
AA3	ddr3ch2_a10_ap	-	-	-	-	-	-	-
Y2	ddr3ch2_a11	-	-	-	-	-	-	-
Y3	ddr3ch2_a12_nbc	-	-	-	-	-	-	-
W1	ddr3ch2_a13	-	-	-	-	-	-	-
W2	ddr3ch2_a14	-	-	-	-	-	-	-
W3	ddr3ch2_a15	-	-	-	-	-	-	-
AC2	ddr3ch2_cka	-	-	-	-	-	-	-
R2	ddr3ch2_ckb	-	-	-	-	-	-	-
AD2	ddr3ch2_cke0	-	-	-	-	-	-	-
U3	ddr3ch2_cke1	-	-	-	-	-	-	-
AC1	ddr3ch2_ncka	-	-	-	-	-	-	-
R1	ddr3ch2_nckb	-	-	-	-	-	-	-
AD3	ddr3ch2_ncs0	-	-	-	-	-	-	-
T2	ddr3ch2_ncs1	-	-	-	-	-	-	-
V2	ddr3ch2_ba0	-	-	-	-	-	-	-
V3	ddr3ch2_ba1	-	-	-	-	-	-	-
U2	ddr3ch2_ba2	-	-	-	-	-	-	-
T3	ddr3ch2_ncas	-	-	-	-	-	-	-
R3	ddr3ch2_nras	-	-	-	-	-	-	-
P2	ddr3ch2_nreset	-	-	-	-	-	-	-
P3	ddr3ch2_nwe	-	-	-	-	-	-	-
N2	ddr3ch2_odt0	-	-	-	-	-	-	-
M2	ddr3ch2_odt1	-	-	-	-	-	-	-
AE1	ddr3ch2_vref_ca	-	-	-	-	-	-	-
J11 / K22 / K12 / K11 / K9 / L14 / L13 / L12 / L10 / M14 / M13 / M11 / M10 / N15 / N14 / N11 / P11 / W24 / W22 / Y24 / Y23 / AA23 / AB24 / AB23 / AC24 / AC22 / AC21 / AD23 / AD22 / AD20 / AD16 / AD15 / AD14 / AD12	vdd_core	-	-	-	-	-	-	-
AH21	vdd_core_sense	-	-	-	-	-	-	-
T14 / T13 / T11 / T10 / W13 / W12 / W10 / Y19 / Y15 / Y11 / Y10 / AA19 / AA16 / AA15 / AA11 / AB19 / AB15 / AB13 / AB11 / AB10 / AC20 / AC16 / AC14 / AC13 / AC12 / AD19 / AD11	vdd_mm	-	-	-	-	-	-	-
AG21	vdd_mm_sense	-	-	-	-	-	-	-
K20 / K19 / K18 / L24 / L22 / L21 / L20 / L18 / M24 / M23 / M20 / M19 / N23 / N18 / P24 / P23 / P22 / P18 / R24 / T24 / T23 / T21 / T20	vdd_mpu	-	-	-	-	-	-	-
U29	vdd_mpu_sense	-	-	-	-	-	-	-
AJ29	vss_mpu_sense	-	-	-	-	-	-	-
AD9	vpp1	-	-	-	-	-	-	-
D28 / D26 / D24 / D23 / D21 / D20 / D18 / D16 / D14 / D13 / D11 / D8 / D6 / F4 / H4 / L16 / L4 / M21 / M17 / M15 / N30 / N22 / N21 / N20 / N19 / N17 / N16 / N13 / N12 / N4 / P30 / P21 / P19 / P16 / P15 / P13 / P12 / P10 / P9 / R22 / R21 / R20 / R19 / R18 / R17 / R16 / R15 / R14 / R13 / R12 / R10 / T30 / T19 / T17 / T15 / T4 / U22 / U21 / U19 / U18 / U17 / U16 / U15 / U13 / U12 / V30 / V24 / V23 / V21 / V20 / V19 / V17 / V15 / V14 / V13 / V11 / V4 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W14 / Y22 / Y21 / Y18 / Y16 / Y13 / Y12 / AA30 / AA22 / AA21 / AA20 / AA18 / AA17 / AA14 / AA13 / AA12 / AA4 / AB21 / AB20 / AB17 / AB14 / AC30 / AC18 / AC4 / AD4 / AF30 / AF4 / AH30 / AK26 / AK23 / AK14 / AK13 / F30 / AK11 / AK10 / AK8 / AK6	vss	-	-	-	-	-	-	-
Y26	vdda_dpll_core_emu_abe	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
U8	vdda_dpll_mm_l4per	-	-	-	-	-	-	-
AF24	vdda_dpll_hdmi	-	-	-	-	-	-	-
Y27	vdda_dpll_mpu	-	-	-	-	-	-	-
AE22	vdda_ldo_core	-	-	-	-	-	-	-
AE20	vdda_ldo_mm	-	-	-	-	-	-	-
J15	vdda_ldo_mpu	-	-	-	-	-	-	-
N25	vdda_ldo_emu_wkup	-	-	-	-	-	-	-
AE16	vdda_vbgap_core	-	-	-	-	-	-	-
T25	cap_vdda_ldo_sram_core_array	-	-	-	-	-	-	-
AG17	cap_vdda_ldo_sram_mm_array	-	-	-	-	-	-	-
H17	cap_vdda_ldo_sram_mpu_array	-	-	-	-	-	-	-
V25	cap_vddldo_emu_wkup	-	-	-	-	-	-	-
AD18	cap_vbb_ldo_mm	-	-	-	-	-	-	-
H13	cap_vbb_ldo_mpu	-	-	-	-	-	-	-
K16	cap_vdda_ldo_sram_mpu_array2	-	-	-	-	-	-	-

(1) NA in table stands for not applicable.

(2) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AJ10 / AK10 / AJ11 / AK11 / AJ12 / AK12 / AC2 / AC3) can output the same GPIO in mode 0 or in mode 6.

2.4 Signal Descriptions

Many signals are available on multiple balls, according to the software configuration of the ball multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the ball.

NOTE

The subsystem multiplexing signals are not described in Table 2-1 and Table 2-2.

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input or output
   - D = Open Drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground
4. **BALL BOTTOM:** Associated ball(s) bottom
5. **PIN NAME:** This is the name of the ball the signal is passing through.

2.4.1 External Memory Interfaces

2.4.1.1 GPMC

NOTE

For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the OMAP543x TRM.

Table 2-3. GPMC Signal Descriptions

SIGNAL NAME [1]	PIN NAME [5]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Multiplexed GPMC Mode				
gpmc_a1 / gpmc_d0	gpmc_ad0	GPMC address bit 1 / data bit 0	IO	J27
gpmc_a2 / gpmc_d1	gpmc_ad1	GPMC address bit 2 / data bit 1	IO	H28
gpmc_a3 / gpmc_d2	gpmc_ad2	GPMC address bit 3 / data bit 2	IO	H29
gpmc_a4 / gpmc_d3	gpmc_ad3	GPMC address bit 4 / data bit 3	IO	G29
gpmc_a5 / gpmc_d4	gpmc_ad4	GPMC address bit 5 / data bit 4	IO	E29
gpmc_a6 / gpmc_d5	gpmc_ad5	GPMC address bit 6 / data bit 5	IO	E27
gpmc_a7 / gpmc_d6	gpmc_ad6	GPMC address bit 7 / data bit 6	IO	F26
gpmc_a8 / gpmc_d7	gpmc_ad7	GPMC address bit 8 / data bit 7	IO	E26
gpmc_a9 / gpmc_d8	gpmc_ad8	GPMC address bit 9 / data bit 8	IO	J32
gpmc_a10 / gpmc_d9	gpmc_ad9	GPMC address bit 10 / data bit 9	IO	J33
gpmc_a11 / gpmc_d10	gpmc_ad10	GPMC address bit 11 / data bit 10	IO	H32
gpmc_a12 / gpmc_d11	gpmc_ad11	GPMC address bit 12 / data bit 11	IO	J31
gpmc_a13 / gpmc_d12	gpmc_ad12	GPMC address bit 13 / data bit 12	IO	G31
gpmc_a14 / gpmc_d13	gpmc_ad13	GPMC address bit 14 / data bit 13	IO	H31
gpmc_a15 / gpmc_d14	gpmc_ad14	GPMC address bit 15 / data bit 14	IO	G32
gpmc_a16 / gpmc_d15	gpmc_ad15	GPMC address bit 16 / data bit 15	IO	G33
gpmc_a17	gpmc_a16	GPMC address bit 17	O	G24
gpmc_a18	gpmc_a17	GPMC address bit 18	O	H24
gpmc_a19	gpmc_a18	GPMC address bit 19	O	E24
gpmc_a20	gpmc_a19	GPMC address bit 20	O	F24
gpmc_a21	gpmc_a20	GPMC address bit 21	O	G21
gpmc_a22	gpmc_a21	GPMC address bit 22	O	H21
gpmc_a23	gpmc_a22	GPMC address bit 23	O	E21
gpmc_a24	gpmc_a23	GPMC address bit 24	O	F21
gpmc_a25	gpmc_a24	GPMC address bit 25	O	F17
gpmc_a26	gpmc_a25	GPMC address bit 26	O	E20
Nonmultiplexed GPMC Mode				
gpmc_d0	gpmc_ad0	GPMC data bit 0	IO	J27
gpmc_d1	gpmc_ad1	GPMC data bit 1	IO	H28
gpmc_d2	gpmc_ad2	GPMC data bit 2	IO	H29
gpmc_d3	gpmc_ad3	GPMC data bit 3	IO	G29
gpmc_d4	gpmc_ad4	GPMC data bit 4	IO	E29
gpmc_d5	gpmc_ad5	GPMC data bit 5	IO	E27
gpmc_d6	gpmc_ad6	GPMC data bit 6	IO	F26
gpmc_d7	gpmc_ad7	GPMC data bit 7	IO	E26
gpmc_d8	gpmc_ad8	GPMC data bit 8	IO	J32
gpmc_d9	gpmc_ad9	GPMC data bit 9	IO	J33
gpmc_d10	gpmc_ad10	GPMC data bit 10	IO	H32
gpmc_d11	gpmc_ad11	GPMC data bit 11	IO	J31
gpmc_d12	gpmc_ad12	GPMC data bit 12	IO	G31
gpmc_d13	gpmc_ad13	GPMC data bit 13	IO	H31
gpmc_d14	gpmc_ad14	GPMC data bit 14	IO	G32
gpmc_d15	gpmc_ad15	GPMC data bit 15	IO	G33
gpmc_a1	gpmc_a16	GPMC address bit 1	O	G24
gpmc_a2	gpmc_a17	GPMC address bit 2	O	H24
gpmc_a3	gpmc_a18	GPMC address bit 3	O	E24

Table 2-3. GPMC Signal Descriptions (continued)

SIGNAL NAME [1]	PIN NAME [5]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
gpmc_a4	gpmc_a19	GPMC address bit 4	O	F24
gpmc_a5	gpmc_a20	GPMC address bit 5	O	G21
gpmc_a6	gpmc_a21	GPMC address bit 6	O	H21
gpmc_a7	gpmc_a22	GPMC address bit 7	O	E21
gpmc_a8	gpmc_a23	GPMC address bit 8	O	F21
gpmc_a9	gpmc_a24	GPMC address bit 9	O	F17
gpmc_a10	gpmc_a25	GPMC address bit 10	O	E20
Common GPMC Signals				
gpmc_ncs0	gpmc_ncs0	GPMC chip select 0 invert	O	P32
gpmc_ncs1	gpmc_ncs1	GPMC chip select 1 invert	O	F20
gpmc_ncs2	gpmc_ncs2	GPMC chip select 2 invert	O	F14
gpmc_ncs3	gpmc_ncs3	GPMC chip select 3 invert	O	G14
gpmc_ncs4	gpmc_ncs4	GPMC chip select 4 invert	O	E17
gpmc_ncs5	gpmc_ncs5	GPMC chip select 5 invert	O	G13
gpmc_ncs6	gpmc_ncs6	GPMC chip select 6 invert	O	E13
gpmc_ncs7	gpmc_ncs7	GPMC chip select 7 invert	O	NA(1)
gpmc_nwp	gpmc_nwp	GPMC flash write protect invert	O	J29
gpmc_clk	gpmc_clk	GPMC clock	O	J28
gpmc_nadv_ale	gpmc_nadv_ale	GPMC address valid invert or address latch enable	O	E25
gpmc_noe_nre	gpmc_noe	GPMC output enable invert or read enable	O	N9
gpmc_nwe	gpmc_nwe	GPMC write enable invert	O	F13
gpmc_nbe0_cle	gpmc_nbe0_cle	GPMC lower-byte enable invert	O	F25
gpmc_nbe1	gpmc_nbe1	GPMC upper-byte enable invert	O	J29
gpmc_wait0	gpmc_wait0	GPMC external indication of wait 0	I	N27
gpmc_wait1	gpmc_wait1	GPMC external indication of wait 1	I	G20
gpmc_wait2	gpmc_wait2	GPMC external indication of wait 2	I	E14
gpmc_wait3	gpmc_wait3	GPMC external indication of wait 3	I	NA(1)

(1) NA in this table stands for not applicable for the OMAP5432 device.

2.4.1.2 DDR3 and DDR3L

NOTE

For more information, see the Memory Subsystem / EMIF Controller section of the OMAP543x TRM.

Table 2-4. DDR3 and DDR3L Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
DDR3 and DDR3L Channel 1			
DDR3 and DDR3L Channel 1 – Common Balls Between POP OMAP5430 LPDDR2 and Bottom OMAP5432 DDR3			
ddrch1_dm0	DDR3 and DDR3L channel 1 data mask 0	IO	A29
ddrch1_dm1	DDR3 and DDR3L channel 1 data mask 1	IO	B24
ddrch1_dm2	DDR3 and DDR3L channel 1 data mask 2	IO	C30
ddrch1_dm3	DDR3 and DDR3L channel 1 data mask 3	IO	B6
ddrch1_dq0	DDR3 and DDR3L channel 1 data bit 0	IO	C28
ddrch1_dq1	DDR3 and DDR3L channel 1 data bit 1	IO	A31
ddrch1_dq2	DDR3 and DDR3L channel 1 data bit 2	IO	C29
ddrch1_dq3	DDR3 and DDR3L channel 1 data bit 3	IO	B30
ddrch1_dq4	DDR3 and DDR3L channel 1 data bit 4	IO	B29
ddrch1_dq5	DDR3 and DDR3L channel 1 data bit 5	IO	C26
ddrch1_dq6	DDR3 and DDR3L channel 1 data bit 6	IO	B28
ddrch1_dq7	DDR3 and DDR3L channel 1 data bit 7	IO	B26
ddrch1_dq8	DDR3 and DDR3L channel 1 data bit 8	IO	C23
ddrch1_dq9	DDR3 and DDR3L channel 1 data bit 9	IO	C22
ddrch1_dq10	DDR3 and DDR3L channel 1 data bit 10	IO	C21
ddrch1_dq11	DDR3 and DDR3L channel 1 data bit 11	IO	B22
ddrch1_dq12	DDR3 and DDR3L channel 1 data bit 12	IO	C24
ddrch1_dq13	DDR3 and DDR3L channel 1 data bit 13	IO	C25
ddrch1_dq14	DDR3 and DDR3L channel 1 data bit 14	IO	B25
ddrch1_dq15	DDR3 and DDR3L channel 1 data bit 15	IO	A25
ddrch1_dq16	DDR3 and DDR3L channel 1 data bit 16	IO	E31
ddrch1_dq17	DDR3 and DDR3L channel 1 data bit 17	IO	E33
ddrch1_dq18	DDR3 and DDR3L channel 1 data bit 18	IO	E32
ddrch1_dq19	DDR3 and DDR3L channel 1 data bit 19	IO	F32
ddrch1_dq20	DDR3 and DDR3L channel 1 data bit 20	IO	C33
ddrch1_dq21	DDR3 and DDR3L channel 1 data bit 21	IO	D30
ddrch1_dq22	DDR3 and DDR3L channel 1 data bit 22	IO	F31
ddrch1_dq23	DDR3 and DDR3L channel 1 data bit 23	IO	C32
ddrch1_dq24	DDR3 and DDR3L channel 1 data bit 24	IO	C6
ddrch1_dq25	DDR3 and DDR3L channel 1 data bit 25	IO	A5
ddrch1_dq26	DDR3 and DDR3L channel 1 data bit 26	IO	B5
ddrch1_dq27	DDR3 and DDR3L channel 1 data bit 27	IO	C5
ddrch1_dq28	DDR3 and DDR3L channel 1 data bit 28	IO	B2
ddrch1_dq29	DDR3 and DDR3L channel 1 data bit 29	IO	B3
ddrch1_dq30	DDR3 and DDR3L channel 1 data bit 30	IO	C3
ddrch1_dq31	DDR3 and DDR3L channel 1 data bit 31	IO	D4
ddrch1_dqs0	DDR3 and DDR3L channel 1 data strobe 0	IO	C27
ddrch1_dqs1	DDR3 and DDR3L channel 1 data strobe 1	IO	B23
ddrch1_dqs2	DDR3 and DDR3L channel 1 data strobe 2	IO	D31

Table 2-4. DDR3 and DDR3L Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
ddrch1_dqs3	DDR3 and DDR3L channel 1 data strobe 3	IO	C4
ddrch1_ndqs0	DDR3 and DDR3L channel 1 negative data strobe 0	IO	B27
ddrch1_ndqs1	DDR3 and DDR3L channel 1 negative data strobe 1	IO	A23
ddrch1_ndqs2	DDR3 and DDR3L channel 1 negative data strobe 2	IO	D32
ddrch1_ndqs3	DDR3 and DDR3L channel 1 negative data strobe 3	IO	B4
DDR3 and DDR3L Channel 1 – Available on OMAP5432 DDR3 Only			
ddr3ch1_a0	DDR3 and DDR3L row, column address bit 0	O	A7
ddr3ch1_a1	DDR3 and DDR3L row, column address bit 1	O	B7
ddr3ch1_a2	DDR3 and DDR3L row, column address bit 2	O	C7
ddr3ch1_a3	DDR3 and DDR3L row, column address bit 3	O	B8
ddr3ch1_a4	DDR3 and DDR3L row, column address bit 4	O	C8
ddr3ch1_a5	DDR3 and DDR3L row, column address bit 5	O	B9
ddr3ch1_a6	DDR3 and DDR3L row, column address bit 6	O	C10
ddr3ch1_a7	DDR3 and DDR3L row, column address bit 7	O	B12
ddr3ch1_a8	DDR3 and DDR3L row, column address bit 8	O	C12
ddr3ch1_a9	DDR3 and DDR3L row, column address bit 9	O	A13
ddr3ch1_a10_ap	DDR3 and DDR3L row, column address bit 10 or DDR3 auto precharge sampling	O	B13
ddr3ch1_a11	DDR3 and DDR3L row, column address bit 11	O	C13
ddr3ch1_a12_nbc	DDR3 and DDR3L row, column address bit 12 or DDR3 bust chop on-the-fly sampling	O	B14
ddr3ch1_a13	DDR3 and DDR3L row, column address bit 13	O	C14
ddr3ch1_a14	DDR3 and DDR3L row, column address bit 14	O	A15
ddr3ch1_a15	DDR3 and DDR3L row, column address bit 15	O	B15
ddr3ch1_cka	DDR3 and DDR3L differential clock, set A	O	C11
ddr3ch1_ckb	DDR3 and DDR3L differential clock, set B	O	C18
ddr3ch1_cke0	DDR3 and DDR3L clock enable for rank 0	O	C9
ddr3ch1_cke1	DDR3 and DDR3L clock enable for rank 1	O	A17
ddr3ch1_ncka	DDR3 and DDR3L differential negative clock, set A	O	B11
ddr3ch1_nckb	DDR3 and DDR3L differential negative clock, set B	O	B18
ddr3ch1_ncs0	DDR3 and DDR3L rank select 0	O	B10
ddr3ch1_ncs1	DDR3 and DDR3L rank select 1	O	B17
ddr3ch1_ba0	DDR3 and DDR3L bank select bit 0	O	C15
ddr3ch1_ba1	DDR3 and DDR3L bank select bit 1	O	B16
ddr3ch1_ba2	DDR3 and DDR3L bank select bit 2	O	C16
ddr3ch1_ncas	DDR3 and DDR3L command	O	C17
ddr3ch1_nras	DDR3 and DDR3L command	O	B19
ddr3ch1_nreset	DDR3 and DDR3L command	O	C19
ddr3ch1_nwe	DDR3 and DDR3L asynchronous reset	O	B20
ddr3ch1_odt0	DDR3 and DDR3L on-die termination for rank 0	O	C20
ddr3ch1_odt1	DDR3 and DDR3L on-die termination for rank 1	O	B21
DDR3 and DDR3L Channel 2			
DDR3 and DDR3L Channel 2 – Common Balls Between POP OMAP5430 LPDDR2 and Bottom OMAP5432 DDR3			
ddrch2_dm0	DDR3 and DDR3L channel 2 data mask 0	IO	J1
ddrch2_dm1	DDR3 and DDR3L channel 2 data mask 1	IO	AJ3
ddrch2_dm2	DDR3 and DDR3L channel 2 data mask 2	IO	G1
ddrch2_dm3	DDR3 and DDR3L channel 2 data mask 3	IO	AL4
ddrch2_dq0	DDR3 and DDR3L channel 2 data bit 0	IO	K3

Table 2-4. DDR3 and DDR3L Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
ddrch2_dq1	DDR3 and DDR3L channel 2 data bit 1	IO	H2
ddrch2_dq2	DDR3 and DDR3L channel 2 data bit 2	IO	H3
ddrch2_dq3	DDR3 and DDR3L channel 2 data bit 3	IO	J3
ddrch2_dq4	DDR3 and DDR3L channel 2 data bit 4	IO	J2
ddrch2_dq5	DDR3 and DDR3L channel 2 data bit 5	IO	M3
ddrch2_dq6	DDR3 and DDR3L channel 2 data bit 6	IO	L2
ddrch2_dq7	DDR3 and DDR3L channel 2 data bit 7	IO	L1
ddrch2_dq8	DDR3 and DDR3L channel 2 data bit 8	IO	AK3
ddrch2_dq9	DDR3 and DDR3L channel 2 data bit 9	IO	AG1
ddrch2_dq10	DDR3 and DDR3L channel 2 data bit 10	IO	AH3
ddrch2_dq11	DDR3 and DDR3L channel 2 data bit 11	IO	AJ2
ddrch2_dq12	DDR3 and DDR3L channel 2 data bit 12	IO	AH2
ddrch2_dq13	DDR3 and DDR3L channel 2 data bit 13	IO	AL1
ddrch2_dq14	DDR3 and DDR3L channel 2 data bit 14	IO	AL3
ddrch2_dq15	DDR3 and DDR3L channel 2 data bit 15	IO	AK4
ddrch2_dq16	DDR3 and DDR3L channel 2 data bit 16	IO	G3
ddrch2_dq17	DDR3 and DDR3L channel 2 data bit 17	IO	D3
ddrch2_dq18	DDR3 and DDR3L channel 2 data bit 18	IO	C2
ddrch2_dq19	DDR3 and DDR3L channel 2 data bit 19	IO	C1
ddrch2_dq20	DDR3 and DDR3L channel 2 data bit 20	IO	D2
ddrch2_dq21	DDR3 and DDR3L channel 2 data bit 21	IO	F2
ddrch2_dq22	DDR3 and DDR3L channel 2 data bit 22	IO	G2
ddrch2_dq23	DDR3 and DDR3L channel 2 data bit 23	IO	F3
ddrch2_dq24	DDR3 and DDR3L channel 2 data bit 24	IO	AM3
ddrch2_dq25	DDR3 and DDR3L channel 2 data bit 25	IO	AL5
ddrch2_dq26	DDR3 and DDR3L channel 2 data bit 26	IO	AM4
ddrch2_dq27	DDR3 and DDR3L channel 2 data bit 27	IO	AN3
ddrch2_dq28	DDR3 and DDR3L channel 2 data bit 28	IO	AL7
ddrch2_dq29	DDR3 and DDR3L channel 2 data bit 29	IO	AL6
ddrch2_dq30	DDR3 and DDR3L channel 2 data bit 30	IO	AM7
ddrch2_dq31	DDR3 and DDR3L channel 2 data bit 31	IO	AM6
ddrch2_dqs0	DDR3 and DDR3L channel 2 data strobe 0	IO	K2
ddrch2_dqs1	DDR3 and DDR3L channel 2 data strobe 1	IO	AK2
ddrch2_dqs2	DDR3 and DDR3L channel 2 data strobe 2	IO	E2
ddrch2_dqs3	DDR3 and DDR3L channel 2 data strobe 3	IO	AM5
ddrch2_ndqs0	DDR3 and DDR3L channel 2 negative data strobe 0	IO	L3
ddrch2_ndqs1	DDR3 and DDR3L channel 2 negative data strobe 1	IO	AL2
ddrch2_ndqs2	DDR3 and DDR3L channel 2 negative data strobe 2	IO	E3
ddrch2_ndqs3	DDR3 and DDR3L channel 2 negative data strobe 3	IO	AN5
DDR3 and DDR3L Channel 2 – Available on OMAP5432 DDR3 Only			
ddr3ch2_a0	DDR3 and DDR3L row, column address bit 0	O	AG2
ddr3ch2_a1	DDR3 and DDR3L row, column address bit 1	O	AG3
ddr3ch2_a2	DDR3 and DDR3L row, column address bit 2	O	AF2
ddr3ch2_a3	DDR3 and DDR3L row, column address bit 3	O	AF3
ddr3ch2_a4	DDR3 and DDR3L row, column address bit 4	O	AE2
ddr3ch2_a5	DDR3 and DDR3L row, column address bit 5	O	AE3
ddr3ch2_a6	DDR3 and DDR3L row, column address bit 6	O	AC3

Table 2-4. DDR3 and DDR3L Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
ddr3ch2_a7	DDR3 and DDR3L row, column address bit 7	O	AB2
ddr3ch2_a8	DDR3 and DDR3L row, column address bit 8	O	AB3
ddr3ch2_a9	DDR3 and DDR3L row, column address bit 9	O	AA2
ddr3ch2_a10_ap	DDR3 and DDR3L row, column address bit 10 or DDR3 auto precharge sampling	O	AA3
ddr3ch2_a11	DDR3 and DDR3L row, column address bit 11	O	Y2
ddr3ch2_a12_nbc	DDR3 and DDR3L row, column address bit 12 or DDR3 bust chop on-the-fly sampling	O	Y3
ddr3ch2_a13	DDR3 and DDR3L row, column address bit 13	O	W1
ddr3ch2_a14	DDR3 and DDR3L row, column address bit 14	O	W2
ddr3ch2_a15	DDR3 and DDR3L row, column address bit 15	O	W3
ddr3ch2_cka	DDR3 and DDR3L differential clock, set A	O	AC2
ddr3ch2_ckb	DDR3 and DDR3L differential clock, set B	O	R2
ddr3ch2_cke0	DDR3 and DDR3L clock enable for rank 0	O	AD2
ddr3ch2_cke1	DDR3 and DDR3L clock enable for rank 1	O	U3
ddr3ch2_ncka	DDR3 and DDR3L differential negative clock, set A	O	AC1
ddr3ch2_nckb	DDR3 and DDR3L differential negative clock, set B	O	R1
ddr3ch2_ncs0	DDR3 and DDR3L rank select 0	O	AD3
ddr3ch2_ncs1	DDR3 and DDR3L rank select 1	O	T2
ddr3ch2_ba0	DDR3 and DDR3L bank select bit 0	O	V2
ddr3ch2_ba1	DDR3 and DDR3L bank select bit 1	O	V3
ddr3ch2_ba2	DDR3 and DDR3L bank select bit 2	O	U2
ddr3ch2_ncas	DDR3 and DDR3L command	O	T3
ddr3ch2_nras	DDR3 and DDR3L command	O	R3
ddr3ch2_nreset	DDR3 and DDR3L command	O	P2
ddr3ch2_nwe	DDR3 and DDR3L asynchronous reset	O	P3
ddr3ch2_odt0	DDR3 and DDR3L on-die termination for rank 0	O	N2
ddr3ch2_odt1	DDR3 and DDR3L on-die termination for rank 1	O	M2

2.4.2 Camera Interfaces

NOTE

For more information, see the Imaging Subsystem / ISS Interfaces section of the OMAP543x TRM.

2.4.2.1 Camera Control

Table 2-5. CAM Control Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
cam_shutter	Mechanical shutter	O	AE6 / AF6
cam_strobe	Flash trigger	O	AE5
cam_globalreset	Sensor reset	IO	AF6

2.4.2.2 CSI-2 MIPI D-PHY

Table 2-6. CSI-2 MIPI D-PHY Signal Descriptions

PIN NAME [5]	SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Main Camera—CSI-2 Port A				
csiporta_lane0x	CSI-2_lane0x	CSI-2 (Port A) camera lane 0 differential x	IDS	U6
csiporta_lane0y	CSI-2_lane0y	CSI-2 (Port A) camera lane 0 differential y	IDS	U5
csiporta_lane1x	CSI-2_lane1x	CSI-2 (Port A) camera lane 1 differential x	IDS	P6
csiporta_lane1y	CSI-2_lane1y	CSI-2 (Port A) camera lane 1 differential y	IDS	P5
csiporta_lane2x	CSI-2_lane2x	CSI-2 (Port A) camera lane 2 differential x	IDS	P7
csiporta_lane2y	CSI-2_lane2y	CSI-2 (Port A) camera lane 2 differential y	IDS	P8
csiporta_lane3x	CSI-2_lane3x	CSI-2 (Port A) camera lane 3 differential x	IDS	N5
csiporta_lane3y	CSI-2_lane3y	CSI-2 (Port A) camera lane 3 differential y	IDS	N6
csiporta_lane4x	CSI-2_lane4x	CSI-2 (Port A) camera lane 4 differential x	IDS	N7
csiporta_lane4y	CSI-2_lane4y	CSI-2 (Port A) camera lane 4 differential y	IDS	N8
Auxiliary Camera—CSI-2 Port B				
csiportb_lane0x	CSI-2_lane0x	CSI-2 (Port B) camera lane 0 differential x	IDS	Y6
csiportb_lane0y	CSI-2_lane0y	CSI-2 (Port B) camera lane 0 differential y	IDS	Y5
csiportb_lane1x	CSI-2_lane1x	CSI-2 (Port B) camera lane 1 differential x	IDS	Y8
csiportb_lane1y	CSI-2_lane1y	CSI-2 (Port B) camera lane 1 differential y	IDS	Y7
csiportb_lane2x	CSI-2_lane2x	CSI-2 (Port B) camera lane 2 differential x	IDS	AA6
csiportb_lane2y	CSI-2_lane2y	CSI-2 (Port B) camera lane 2 differential y	IDS	AA5
Second Camera—CSI-2 Port C				
csiportc_lane0x	CSI-2_lane0x	CSI-2 (Port C) camera lane 1 differential x	IDS	J7
csiportc_lane0y	CSI-2_lane0y	CSI-2 (Port C) camera lane 1 differential y	IDS	J6
csiportc_lane1x	CSI-2_lane1x	CSI-2 (Port C) camera lane 0 differential x	IDS	K5
csiportc_lane1y	CSI-2_lane1y	CSI-2 (Port C) camera lane 0 differential y	IDS	K6

2.4.2.3 CCP2 PHY

Table 2-7. CCP2 PHY Signal Descriptions

PIN NAME [5]	SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Auxiliary Camera—CCPV2 Port B				
csiportb_lane0x	ccpv2_lane0x	CCPV2 (Port B) camera lane 0 differential x	IDS	Y6
csiportb_lane0y	ccpv2_lane0y	CCPV2 (Port B) camera lane 0 differential y	IDS	Y5
csiportb_lane1x	ccpv2_lane1x	CCPV2 (Port B) camera lane 1 differential x	IDS	Y8
csiportb_lane1y	ccpv2_lane1y	CCPV2 (Port B) camera lane 1 differential y	IDS	Y7
csiportb_lane2x	ccpv2_lane2x	CCPV2 (Port B) camera lane 2 differential x	IDS	AA6
csiportb_lane2y	ccpv2_lane2y	CCPV2 (Port B) camera lane 2 differential y	IDS	AA5
Second Camera—CCPV2 Port C				
csiportc_lane1x	ccpv2_lane1x	CCPV2 (Port C) camera lane 0 differential x	IDS	J7
csiportc_lane1y	ccpv2_lane1y	CCPV2 (Port C) camera lane 0 differential y	IDS	J6
csiportc_lane0x	ccpv2_lane0x	CCPV2 (Port C) camera lane 1 differential x	IDS	K5
csiportc_lane0y	ccpv2_lane0y	CCPV2 (Port C) camera lane 1 differential y	IDS	K6

2.4.2.4 CPI

Table 2-8. CPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
cpi_pclk	CPI pixel clock	I	U6
cpi_hsync	CPI horizontal synchronization: line trigger	IO	AG5
cpi_vsync	CPI vertical synchronization: frame trigger	IO	AF5
cpi_hsyncin	CPI input-only version of cpi_hsynck	I	AA5
cpi_vsyncin	CPI input-only version of cpi_vsynck	I	AA6
cpi_data0	CPI data bit 0	I	P5
cpi_data1	CPI data bit 1	I	P6
cpi_data2	CPI data bit 2	I	P8
cpi_data3	CPI data bit 3	I	P7
cpi_data4	CPI data bit 4	I	N5
cpi_data5	CPI data bit 5	I	N6
cpi_data6	CPI data bit 6	I	N7
cpi_data7	CPI data bit 7	I	N8
cpi_data8	CPI data bit 8	I	J6
cpi_data9	CPI data bit 9	I	J7
cpi_data10	CPI data bit 10	I	K6
cpi_data11	CPI data bit 11	I	K5
cpi_data12	CPI data bit 12	I	Y6 / AE7
cpi_data13	CPI data bit 13	I	Y5 / AD5
cpi_data14	CPI data bit 14	I	Y7 / AD6
cpi_data15	CPI data bit 15	I	Y8 / AD7
cpi_wen	CPI external write enable	I	U5
cpi_fid	CPI field identification for interlaced sensors (I mode)	I	AF6

2.4.3 Display

NOTE

For more information, see the Display Subsystem / Display Subsystem Overview / DSS Environment section of the OMAP543x TRM.

2.4.3.1 DSI-1 MIPI D-PHY

Table 2-9. DSI-1 MIPI D-PHY Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
DSI Port A			
dsiporta_lane0x	DSI (Port A) lane 0 differential positive or negative	ODS	AD31
dsiporta_lane0y	DSI (Port A) lane 0 differential positive or negative	ODS	AD32
dsiporta_lane1x	DSI (Port A) lane 1 differential positive or negative	ODS	AC31
dsiporta_lane1y	DSI (Port A) lane 1 differential positive or negative	ODS	AC32
dsiporta_lane2x	DSI (Port A) lane 2 differential positive or negative	ODS	AB32
dsiporta_lane2y	DSI (Port A) lane 2 differential positive or negative	ODS	AB31
dsiporta_lane3x	DSI (Port A) lane 3 differential positive or negative	ODS	AA32
dsiporta_lane3y	DSI (Port A) lane 3 differential positive or negative	ODS	AA31
dsiporta_lane4x	DSI (Port A) lane 4 differential positive or negative	ODS	Y32
dsiporta_lane4y	DSI (Port A) lane 4 differential positive or negative	ODS	Y31
dsiporta_te0	DSI (Port A) tearing effect control input	I	W33
DSI Port C			
dsiportc_lane0x	DSI (Port C) lane 0 differential positive or negative	ODS	AJ31
dsiportc_lane0y	DSI (Port C) lane 0 differential positive or negative	ODS	AJ32
dsiportc_lane1x	DSI (Port C) lane 1 differential positive or negative	ODS	AH32
dsiportc_lane1y	DSI (Port C) lane 1 differential positive or negative	ODS	AH31
dsiportc_lane2x	DSI (Port C) lane 2 differential positive or negative	ODS	AG32
dsiportc_lane2y	DSI (Port C) lane 2 differential positive or negative	ODS	AG31
dsiportc_lane3x	DSI (Port C) lane 3 differential positive or negative	ODS	AF32
dsiportc_lane3y	DSI (Port C) lane 3 differential positive or negative	ODS	AF31
dsiportc_lane4x	DSI (Port A) lane 4 differential positive or negative	ODS	AE32
dsiportc_lane4y	DSI (Port A) lane 4 differential positive or negative	ODS	AE31
dsiportc_te0	DSI (Port C) tearing effect control input	I	AK30

2.4.3.2 HDMI PHY

Table 2-10. HDMI PHY Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
hdmi_cec	HDMI consumer electronic control	IOD	AN23
hdmi_hpd	HDMI display hot plug detect	I	AM23
hdmi_ddc_scl	HDMI display data channel clock	IOD	AM22
hdmi_ddc_sda	HDMI display data channel data	IOD	AL23
hdmi_clkx	HDMI clock differential positive or negative	ODS	AL24
hdmi_clky	HDMI clock differential positive or negative	ODS	AM24
hdmi_data0x	HDMI data 0 differential positive or negative	ODS	AL25
hdmi_data0y	HDMI data 0 differential positive or negative	ODS	AM25
hdmi_data1x	HDMI data 1 differential positive or negative	ODS	AL26
hdmi_data1y	HDMI data 1 differential positive or negative	ODS	AM26
hdmi_data2x	HDMI data 2 differential positive or negative	ODS	AL27
hdmi_data2y	HDMI data 2 differential positive or negative	ODS	AM27

2.4.3.3 RFBI

Table 2-11. RFBI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
rfbi_data0	RFBI data bit 0	IO	AL17
rfbi_data1	RFBI data bit 1	IO	AM17
rfbi_data2	RFBI data bit 2	IO	AN17
rfbi_data3	RFBI data bit 3	IO	AL16
rfbi_data4	RFBI data bit 4	IO	AM16
rfbi_data5	RFBI data bit 5	IO	AL15
rfbi_data6	RFBI data bit 6	IO	AM15
rfbi_data7	RFBI data bit 7	IO	AN15
rfbi_data8	RFBI data bit 8	IO	AL14
rfbi_data9	RFBI data bit 9	IO	AM14
rfbi_data10	RFBI data bit 10	IO	AM12
rfbi_data11	RFBI data bit 11	IO	AL11
rfbi_data12	RFBI data bit 12	IO	AM11
rfbi_data13	RFBI data bit 13	IO	AN11
rfbi_data14	RFBI data bit 14	IO	AL10
rfbi_data15	RFBI data bit 15	IO	AM10
rfbi_a0	RFBI data / control selection	O	AM18
rfbi_we	RFBI write enable	O	AL12
rfbi_re	RFBI read enable	O	AL18
rfbi_cs0	RFBI chip select	O	AL13
rfbi_te_vsync0	RFBI vertical synchronization / tearing effect control signal	I	AM13
rfbi_hsync0	RFBI horizontal synchronization / tearing effect control signal	I	AN13

2.4.3.4 DISPC

Table 2-12. DISPC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
dispc_data0	DISPC data to LCD2 panel—data bit 0	O	AL17
dispc_data1	DISPC data to LCD2 panel—data bit 1	O	AM17
dispc_data2	DISPC data to LCD2 panel—data bit 2	O	AN17
dispc_data3	DISPC data to LCD2 panel—data bit 3	O	AL16
dispc_data4	DISPC data to LCD2 panel—data bit 4	O	AM16
dispc_data5	DISPC data to LCD2 panel—data bit 5	O	AL15
dispc_data6	DISPC data to LCD2 panel—data bit 6	O	AM15
dispc_data7	DISPC data to LCD2 panel—data bit 7	O	AN15
dispc_data8	DISPC data to LCD2 panel—data bit 8	O	AL14
dispc_data9	DISPC data to LCD2 panel—data bit 9	O	AM14
dispc_data10	DISPC data to LCD2 panel—data bit 10	O	AM12
dispc_data11	DISPC data to LCD2 panel—data bit 11	O	AL11
dispc_data12	DISPC data to LCD2 panel—data bit 12	O	AM11
dispc_data13	DISPC data to LCD2 panel—data bit 13	O	AN11
dispc_data14	DISPC data to LCD2 panel—data bit 14	O	AL10
dispc_data15	DISPC data to LCD2 panel—data bit 15	O	AM10
dispc_data16	DISPC data to LCD2 panel—data bit 16	O	AN9

Table 2-12. DISPC Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
dispc_data17	DISPC data to LCD2 panel—data bit 17	O	AM9
dispc_data18	DISPC data to LCD2 panel—data bit 18	O	AL9
dispc_data19	DISPC data to LCD2 panel—data bit 19	O	AM8
dispc_data20	DISPC data to LCD2 panel—data bit 20	O	AL8
dispc_data21	DISPC data to LCD2 panel—data bit 21	O	AN7
dispc_data22	DISPC data to LCD2 panel—data bit 22	O	AL14
dispc_data23	DISPC data to LCD2 panel—data bit 23	O	AM14
dispc_hsync	DISPC horizontal synchronization from dispc to LCD2	O	AL13
dispc_vsync	DISPC vertical synchronization from dispc to LCD2	O	AL12
dispc_de	DISPC ac bias output enable or data enable to LCD2	O	AM18
dispc_pclk	DISPC LCD pixel clock to LCD2	O	AL18
dispc_fid	DISPC field ID to LCD2	O	AF20

2.4.4 Serial and Parallel Communication Interfaces

2.4.4.1 HDQ / 1-Wire

NOTE

For more information, see the Serial Communication Interface / HDQ/1-Wire section of the OMAP543x TRM.

Table 2-13. HDQ / 1-Wire Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
hdq_sio	HDQ 1-wire	IOD	AJ24

2.4.4.2 I^2C

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I^2C Controller / HS I^2C Environment / HS I^2C in I^2C Mode section of the OMAP543x TRM.

NOTE

For more information on SmartReflex™ AVS, see:

- The Power, Reset and Clock Management / Device Power Management Introduction / Device Power-Management Architecture Building Blocks / Voltage Management / AVS Overview section
- The Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section

of the OMAP543x TRM.

Table 2-14. I^2C Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Inter-Integrated Circuit Interface (I2C1)—Platform			
i2c1_pmic_scl	I2C1 master platform clock	IOD	P29
i2c1_pmic_sda	I2C1 master platform data	IOD	P28
Inter-Integrated Circuit Interface (I2C2)—Generic			

Table 2-14. I²C Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
i2c2_scl	I2C2 OMAP master or slave clock	IOD	AL33
i2c2_sda	I2C2 data	IOD	AM32
Inter-Integrated Circuit Interface (I2C3)—Generic			
i2c3_scl	I2C3 OMAP master clock	IOD	AJ5
i2c3_sda	I2C3 data	IOD	AH4
Inter-Integrated Circuit Interface (I2C4)—Generic			
i2c4_scl	I2C4 OMAP master clock	IOD	AJ21
i2c4_sda	I2C4 data	IOD	AJ20
Inter-Integrated Circuit Interface (I2C5)—Generic			
i2c5_scl	I2C5 OMAP master or slave clock	IOD	AL28
i2c5_sda	I2C5 data	IOD	AM29
Inter-Integrated Circuit Interface (SmartReflex™ AVS)—PMIC			
sr_pmic_scl	SmartReflex™ AVS clock	IOD	R32
sr_pmic_sda	SmartReflex™ AVS data	IOD	R31

2.4.4.3 McBSP

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) section of the OMAP543x TRM.

Table 2-15. McBSP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
abe_clks	ABE synchronization input clock	I	W32
Audio Back-end Multichannel Buffered Serial Port (ABE McBSP1)			
abemcbsp1_dr	ABE McBSP1 received serial data	I	AG29
abemcbsp1_dx	ABE McBSP1 transmitted serial data	O	AD28
abemcbsp1_fsx	ABE McBSP1 combined frame synchronization	IO	AD29
abemcbsp1_clkx	ABE McBSP1 combined serial clock	IO	AF29
Audio Back-end Multichannel Buffered Serial Port (ABE McBSP2)			
abemcbsp2_dr	ABE McBSP2 received serial data	I	AD26
abemcbsp2_dx	ABE McBSP2 transmitted serial data	O	AD27
abemcbsp2_fsx	ABE McBSP2 combined frame synchronization	IO	AA26
abemcbsp2_clkx	ABE McBSP2 combined serial clock	IO	AA27
Audio Back-end Multichannel Buffered Serial Port (ABE McBSP3)			
abemcbsp3_dr	ABE McBSP3 received serial data	I	AE28 / AA28
abemcbsp3_dx	ABE McBSP3 transmitted serial data	O	AE29 / AA29
abemcbsp3_fsx	ABE McBSP3 combined frame synchronization	IO	AF28 / Y28
abemcbsp3_clkx	ABE McBSP3 combined serial clock	IO	AE27 / Y29

2.4.4.4 McPDM

NOTE

For more information, see the Serial Communication Interface / Multichannel PDM Controller section of the OMAP543x TRM.

Table 2-16. McPDM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
abe_clks	ABE synchronization input clock	I	W32
Audio Back-end Multichannel PDM			
abemcpdm_ul_data	ABE PDM data stream from PMIC to OMAP5432	I	AA28
abemcpdm_dl_data	ABE PDM data stream from OMAP5432 to PMIC	O	AA29
abemcpdm_frame	ABE PDM frame synchronization	IO	Y29
abemcpdm_lb_clk	ABE PDM loop back clock	O	Y28

2.4.4.5 DMIC

NOTE

For more information, see the Serial Communication Interface / Digital Microphone Module section of the OMAP543x TRM.

Table 2-17. DMIC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
abe_clks	ABE synchronization input clock	I	W32
Audio Back-end Digital Microphone Module			
abedmic_clk1	ABE digital microphone clock output 1	O	AE27
abedmic_din1	ABE digital microphone data input 1	I	AF28
abedmic_clk2	ABE digital microphone clock output 2	O	AD29
abedmic_din2	ABE digital microphone data input 2	I	AE29
abedmic_clk3	ABE digital microphone clock output 3	O	AD28
abedmic_din3	ABE digital microphone data input 3	I	AE28

2.4.4.6 McASP

NOTE

For more information, see the Serial Communication Interface / Multichannel Audio Serial Port section of the OMAP543x TRM.

Table 2-18. McASP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
abe_clks	ABE synchronization input clock	I	W32
Audio Back-end Multichannel Audio Serial Port			
abemcasp_axr	ABE McASP serial data IO	IO	AD26 / W32 / AE29
abemcasp_axr1	ABE McASP serial data 1 IO	IO	Y29
abemcasp_axr2	ABE McASP serial data 2 IO	IO	AA29
abemcasp_axr3	ABE McASP serial data 3 IO	IO	AA28
abemcasp_aclkx	ABE McASP clock transmit	IO	AD28
abemcasp_afsx	ABE McASP frame synchronization transmit	IO	AA26
abemcasp_afsr	ABE McASP frame synchonization receive	IO	AF29
abemcasp_ahclkx	ABE McASP high frequency clock output	IO	AA27
abemcasp_aclkr	ABE McASP low frequency clock input	IO	AG29
abemcasp_amutein	ABE McASP auto mute input	I	AD29
abemcasp_amuteout	ABE McASP auto mute output	O	AD27

2.4.4.7 HSI

NOTE

For more information, see the Serial Communication Interface / MIPI-HSI section of the OMAP543x TRM.

NOTE

The HSI1 interface is not available in the OMAP5432 device. For more information, see the OMAP543x TRM.

Table 2-19. HSI2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
High-speed Synchronous Serial Interface (HSI2)			
hsi2_cawake	HSI2 cellular modem to APE wake signal	I	F17
hsi2_acready	HSI2 APE to cellular modem ready signal	O	F20
hsi2_cadata	HSI2 cellular modem to APE signal	I	F14
hsi2_caflag	HSI2 cellular modem to APE flag signal	I	E14
hsi2_acwake	HS2 APE to cellular modem wake signal	O	E20
hsi2_caready	HSI2 cellular modem to APE ready signal	I	G20
hsi2_acdata	HSI2 APE to cellular modem data signal	O	E17
hsi2_acflag	HSI2 APE to cellular modem ready signal	O	G14

2.4.4.8 McSPI

NOTE

For more information, see the Serial Communication Interface / Multichannel Serial Port Interface (MCSPI) section of the OMAP543x TRM.

Table 2-20. McSPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Multichannel Serial Port Interface (McSPI1)			
mcspi1_simo	McSPI1 data (slave input, master output, Z when not shifting)	IO	AL29
mcspi1_somi	McSPI1 data (slave output, master input, Z when not shifting)	I	AL30
mcspi1_clk	McSPI1 clock	IO	AM30
mcspi1_cs0	McSPI1 chip select 0	O	AN31
mcspi1_cs1	McSPI1 chip select 1	O	AM31
mcspi1_cs2	McSPI1 chip select 2	O	NA(1)
mcspi1_cs3	McSPI1 chip select 3	O	NA(1)
Multichannel Serial Port Interface (McSPI2)			
mcspi2_simo	McSPI2 data (slave input, master output, Z when not shifting)	IO	AG20
mcspi2_somi	McSPI2 data (slave output, master input, Z when not shifting)	I	AH20
mcspi2_clk	McSPI2 clock	IO	AH17
mcspi2_cs0	McSPI2 chip select 0	O	AF20
mcspi2_cs1	McSPI2 chip select 1	O	AM10
Multichannel Serial Port Interface (McSPI3)			
mcspi3_simo	McSPI3 data (slave input, master output, Z when not shifting)	IO	G13
mcspi3_somi	McSPI3 data (slave output, master input, Z when not shifting)	IO	F13

Table 2-20. McSPI Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
mcspi3_clk	McSPI3 clock	IO	E13
mcspi3_cs0	McSPI3 chip select 0	IO	N9
Multichannel Serial Port Interface (McSPI4)			
mcspi4_simo	McSPI4 data (slave input, master output, Z when not shifting)	IO	AJ26
mcspi4_somi	McSPI4 data (slave output, master input, Z when not shifting)	IO	AH26
mcspi4_clk	McSPI4 clock	IO	AH25
mcspi4_cs0	McSPI4 chip select 0	IO	AK28

(1) NA in this table stands for not applicable for the OMAP5432 device.

2.4.4.9 UART

NOTE

For more information, see the Serial Communication Interface / UART/IrDA/CIR section of the OMAP543x TRM.

NOTE

The UART4 and UART6 interfaces are not available in the OMAP5432 device. For more information, see the OMAP543x TRM.

Table 2-21. UART1, UART2, UART3, and UART5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Universal Asynchronous Receiver/Transmitter (UART1)			
uart1_tx	UART1 transmit data	O	AE7
uart1_rx	UART1 receive data	I	AD6
uart1_cts	UART1 clear to send	I	AD5
uart1_rts	UART1 request to send	O	AD7
Universal Asynchronous Receiver/Transmitter (UART2)			
uart2_tx	UART2 transmit data	O	E13
uart2_rx	UART2 receive data	I	G13
uart2_cts	UART2 clear to send	I	N9
uart2_rts	UART2 request to send	O	F13
Universal Asynchronous Receiver/Transmitter (UART3)			
uart3_tx_irtx	UART3 transmit data output or infrared data output	O	AN17 / AG24 / AM19
uart3_rx_irrx	UART3 receive data input or infrared data input	I	AM17 / AH24 / AL19
uart3_cts_rctx	UART3 clear to send or remote control data output	IO	AJ25
uart3_rts_irsd	UART3 request to send or infrared transceiver shutdown	O	AJ24
Universal Asynchronous Receiver/Transmitter (UART5)			
uart5_tx	UART5 transmit data	O	AL31
uart5_rx	UART5 receive data	I	AL32
uart5_cts	UART5 clear to send	I	AK31
uart5_rts	UART5 request to send	O	AK32

2.4.4.10 USB

NOTE

For more information, see:

- Serial Communication Interface / High-Speed Multiport USB Host Subsystem section, or
- Serial Communication Interface / High-Speed USB OTG Controller section, or
- Serial Communication Interface / Full-Speed USB Host Controller section, or
- Serial Communication Interface / Super-Speed USB OTG Subsystem section

of the OMAP543x TRM.

NOTE

The following interfaces are not available in the OMAP5432 device:

- USB (Port D0)—ULPI 8-bit
- USB (Port B1)—HSIC1
- USB (Port B2)—ULPI 8-bit
- USB (Port B2)—Full Speed / Low Speed

For more information, see the OMAP543x TRM.

Table 2-22. USB Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Universal Serial Bus (Port D0)—USB2PHY			
usbd0_hs_dp	USB2PHY (Port D0)—half-duplex positive lane	IODS	AL19
usbd0_hs_dm	USB2PHY (Port D0)—half-duplex negative lane	IODS	AM19
usbphy_ce	USB2PHY (Port D0)—charge enable	O	AN19
Universal Serial Bus (Port D0)—USB3PHY			
usbd0_ss_tx	USB3PHY (Port D0)—transmitter positive lane	ODS	AL20
usbd0_ss_ty	USB3PHY (Port D0)—transmitter negative lane	ODS	AM20
usbd0_ss_rx	USB3PHY (Port D0)—receiver positive lane	IDS	AL21
usbd0_ss_ry	USB3PHY (Port D0)—receiver negative lane	IDS	AM21
Universal Serial Bus (Port B1)—ULPI 8-bit			
usbb1_ulpiphy_clk	USB (Port B1)—ULPI functional clock	I	G20
usbb1_ulpiphy_stp	USB (Port B1)—ULPI stop	O	E20
usbb1_ulpiphy_dir	USB (Port B1)—ULPI bus direction	I	F17
usbb1_ulpiphy_nxt	USB (Port B1)—ULPI next	I	F20
usbb1_ulpiphy_data0	USB (Port B1)—ULPI 8-bit data bus	IO	E14
usbb1_ulpiphy_data1	USB (Port B1)—ULPI 8-bit data bus	IO	F14
usbb1_ulpiphy_data2	USB (Port B1)—ULPI 8-bit data bus	IO	G14
usbb1_ulpiphy_data3	USB (Port B1)—ULPI 8-bit data bus	IO	E17
usbb1_ulpiphy_data4	USB (Port B1)—ULPI 8-bit data bus	IO	F13
usbb1_ulpiphy_data5	USB (Port B1)—ULPI 8-bit data bus	IO	N9
usbb1_ulpiphy_data6	USB (Port B1)—ULPI 8-bit data bus	IO	G13
usbb1_ulpiphy_data7	USB (Port B1)—ULPI 8-bit data bus	IO	E13
Universal Serial Bus (Port B2)—HSIC			
usbb2_hsic_data	USB (Port B2)—interchip data	IO	K29
usbb2_hsic_strobe	USB (Port B2)—interchip strobe	IO	K28
Universal Serial Bus (Port B3)—HSIC			
usbb3_hsic_data	USB (Port B3)—interchip data	IO	K27

Table 2-22. USB Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
usbb3_hsic_strobe	USB (Port B3)—interchip strobe	IO	K26

2.4.4.11 SATA

NOTE

For more information, see the SATA section of the OMAP543x TRM.

Table 2-23. SATA Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
sata_tx	SATA differential positive or negative transmitter lane x	ODS	G9
sata_ty	SATA differential positive or negative transmitter lane y	ODS	F9
sata_rx	SATA differential positive or negative receiver lane x	IDS	E10
sata_ry	SATA differential positive or negative receiver lane y	IDS	F10
sata_actled	SATA channel activity indicator	O	AJ25

2.4.4.12 eMMC

NOTE

For more information, see the MMC / SD / SDIO section of the OMAP543x TRM.

Table 2-24. eMMC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
emmc_clk	eMMC clock	O	AJ10
emmc_cmd	eMMC command	IO	AH10
emmc_data0	eMMC data bit 0	IO	AG10
emmc_data1	eMMC data bit 1	IO	AF10
emmc_data2	eMMC data bit 2	IO	AH9
emmc_data3	eMMC data bit 3	IO	AJ9
emmc_data4	eMMC data bit 4	IO	AG9
emmc_data5	eMMC data bit 5	IO	AJ8
emmc_data6	eMMC data bit 6	IO	AH8
emmc_data7	eMMC data bit 7	IO	AJ7

2.4.4.13 WLSDIO3

Table 2-25. WLSDIO Signal Descriptions(1)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Wireless LAN SDIO (OMAP to Wireless LAN)			
wlsdio_clk	WLSDIO clock	O	AH25
wlsdio_cmd	WLSDIO command	IO	AG25
wlsdio_data0	WLSDIO data bit 0	IO	AJ26
wlsdio_data1	WLSDIO data bit 1	IO	AH26
wlsdio_data2	WLSDIO data bit 2	IO	AK28
wlsdio_data3	WLSDIO data bit 3	IO	AJ27

(1) This interface supports WLAN SDIO with inband interrupt.

2.4.4.14 SDIO4

Table 2-26. SDIO4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Generic SDIO			
sdio4_clk	SDIO4 clock	O	AG24
sdio4_cmd	SDIO4 command	IO	AH24
sdio4_data0	SDIO4 data bit 0	IO	AK31
sdio4_data1	SDIO4 data bit 1	IO	AL32
sdio4_data2	SDIO4 data bit 2	IO	AL31
sdio4_data3	SDIO4 data bit 3	IO	AK32

NOTE

The SDIO5 interface is not available in the OMAP5432 device. For more information, see the OMAP543x TRM.

2.4.5 Removable Cards

Table 2-27. SD Card Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
sdcard_clk	SD clock	O	F8
sdcard_cmd	SD command	IO	E8
sdcard_data0	SD data bit 0	IO	H6
sdcard_data1	SD data bit 1	IO	H5
sdcard_data2	SD data bit 2	IO	G5
sdcard_data3	SD data bit 3	IO	E7
sdcard_cd	SD card detect	I	AD5
sdcard_wp	SD write protect	I	AD6 / AD7

2.4.6 Debug and Trace Interfaces

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP543x TRM.

2.4.6.1 JTAG®

Table 2-28. JTAG Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
jtag_ntrst	JTAG test reset	I	H5 / B32
jtag_tck	JTAG test clock	I	E7 / C31
jtag_tmsc	JTAG test mode select (I for JTAG)	IO	B31 / G5
jtag_rtck	JTAG ARM ® clock emulation	O	F8 / B33
jtag_tdi	JTAG test data In	I	H6 / A32
jtag_tdo	JTAG test data out	O	E8 / A33
jtag_sel	JTAG override HW control for JTAG on SD card interface	I	AM13

2.4.6.2 cJTAG

Table 2-29. cJTAG Signal Descriptions

PIN NAME [5]	SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
cJTAG Muxed with JTAG				
jtag_tck	cjtag_tck	cJTAG test clock	I	E7 / C31
jtag_tmsc	cjtag_tmsc	cJTAG test mode control and data scan	IO	B31 / G5

2.4.6.3 JTAG Expansion Port

Table 2-30. JTAG Expansion Port Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Inverted JTAG interface to chain a modem (or other IC) with the OMAP JTAG			
jtagtapext_ntrst	Test reset for external modem or other IC	O	AL16 / AF20
jtagtapext_tck	Test clock for external modem or other IC	O	AM16 / AH17
jtagtapext_tmsc	Test mode select (0 for modem JTAG) for external modem or other IC	O	AL15 / AJ18
jtagtapext_rtck	ARM clock emulation for external modem or other IC	O	AL17 / AJ20
jtagtapext_tdi	Test data in for external modem or other IC	I	AN15 / AJ21
jtagtapext_tdo	Test data out for external modem or other IC	O	AM15 / AH20

2.4.6.4 Debug Resource Manager (DRM)

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP543x TRM.

Table 2-31 provides the DRM signal descriptions plus the debug modes available on the DRM signals.

Table 2-31. DRM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	DEBUG MODE		
				TRIGGER	TPIU PTM 16-BIT	TPIU STM 4-BIT
drm_emu19	Debug resource manager bit 19	O	AM10 / V32		atpiu_data15	stm_data[3:0] or stm_clk
drm_emu18	Debug resource manager bit 18	O	AL10 / V31		atpiu_data14	stm_data[3:0] or stm_clk
drm_emu17	Debug resource manager bit 17	O	AN11 / U33		atpiu_data13	stm_data[3:0] or stm_clk
drm_emu16	Debug resource manager bit 16	O	AM11 / U32		atpiu_data12	stm_data[3:0] or stm_clk
drm_emu15	Debug resource manager bit 15	O	AL11 / U31		atpiu_data11	stm_data[3:0] or stm_clk
drm_emu14	Debug resource manager bit 14	O	AM12		atpiu_data10	stm_data[3:0] or stm_clk
drm_emu13	Debug resource manager bit 13	O	AM14		atpiu_data9	stm_data[3:0] or stm_clk
drm_emu12	Debug resource manager bit 12	O	AL14		atpiu_data8	stm_data[3:0] or stm_clk
drm_emu11	Debug resource manager bit 11	O	AN15		atpiu_data7	stm_data[3:0] or stm_clk
drm_emu10	Debug resource manager bit 10	O	AM15		atpiu_data6	stm_data[3:0] or stm_clk

Table 2-31. DRM Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	DEBUG MODE		
				TRIGGER	TPIU PTM 16-BIT	TPIU STM 4-BIT
drm_emu9	Debug resource manager bit 9	O	AL15		atpiu_data5	stm_data[3:0] or stm_clk
drm_emu8	Debug resource manager bit 8	O	AM16		atpiu_data4	stm_data[3:0] or stm_clk
drm_emu7	Debug resource manager bit 7	O	AL16		atpiu_data3	stm_data[3:0] or stm_clk
drm_emu6	Debug resource manager bit 6	O	AN17 / V32		atpiu_data2	stm_data[3:0] or stm_clk
drm_emu5	Debug resource manager bit 5	O	AM17 / V31		atpiu_data1	stm_data[3:0] or stm_clk
drm_emu4	Debug resource manager bit 4	O	AL17 / U33		atpiu_data0	stm_data[3:0] or stm_clk
drm_emu3	Debug resource manager bit 3	O	AL13 / U32		atpiu_ctl	stm_data[3:0] or stm_clk
drm_emu2	Debug resource manager bit 2	O	AL12 / U31		atpiu_clk	stm_data[3:0] or stm_clk
drm_emu1	Debug resource manager bit 1	IO	K31	trigger_channel1		stm_data[3:0] or stm_clk
drm_emu0	Debug resource manager bit 0	IO	K32	trigger_channel0		stm_data[3:0] or stm_clk

The DRM interface supports:

- PTM: Processor Trace Module, specific to MPU trace.
- STM: System Trace Module, for HW and SW system events.

STM via the DRM interface is always supported while MPU trace (PTM) is not always possible. This limitation is induced by the DRM: while any drm_emu signals can be configured as the STM clock or one of the data lanes, the drm_emu signals have a fixed PTM assignment.

The concurrent debug use cases are:

- UC1: Either uses trigger channel 2 pins plus the TPIU PTM 16-bit data.
- UC2: Either the TPIU PTM 16-bit data plus the TPIU STM 1-bit data.
- UC3: Either the trigger channel 2 pins plus TPIU PTM 8-bit data plus TPIU STM 4-bit data.
- UC4: Or uses the trigger channel 2 pins plus TPIU PTM 11-bit data plus TPIU STM 4-bit data.

An STM 4-bit data always-on interface is available via the DRM interface on the sys_boot pins in order to use debug function in OFF mode (especially for PRCM or audio backend debug).

Table 2-32. Always-On STM 4-Bit Debug Port Configuration

DEBUG MODE STM 4-BIT	SIGNAL NAME (DEBUG PORT) [1]	PIN NAME [5]	TYPE [3]	BALL BOTTOM [4]
stm_data[3:0] or stm_clk	drm_emu15	sys_boot0	IO	U31
stm_data[3:0] or stm_clk	drm_emu16	sys_boot1	IO	U32
stm_data[3:0] or stm_clk	drm_emu17	sys_boot2	IO	U33
stm_data[3:0] or stm_clk	drm_emu18	sys_boot3	IO	V31
stm_data[3:0] or stm_clk	drm_emu19	sys_boot4	IO	V32

2.4.6.5 MIPI NIDnT (Narrow Interface for Debug and Test)

Typically, the device wide debug port is not available on a packaged end product phone due to connectivity and footprint constraints.

The OMAP5432 provides a narrow debug interface on SD Card connector compliant to the MIPI NIDnT specification. The MIPI NIDnT functionality is supported with full software control.

Table 2-33 provides the NIDnT signal descriptions.

Table 2-33. NIDnT Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Narrow Interface for Debug and Trace			
n_clk	NiDnT debug bus	O	F8
n_d0	NiDnT debug bus	O	H6
n_d1	NiDnT debug bus	O	H5
n_d2	NiDnT debug bus	O	E8 / G5
n_d3	NiDnT debug bus	O	E7

The NIDnT standard supports several overlay modes by software. For more information, see the On-Chip Debug Support / Debug Interfaces / NIDnT section of the OMAP543x TRM.

2.4.6.6 Hardware Debug

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP543x TRM.

Table 2-34. Hardware Debug Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
Observability Hardware Debug Bus: Wakeup Domain			
hw_wkdbg0	Hardware debug pin 0	O	U31
hw_wkdbg1	Hardware debug pin 1	O	U32
hw_wkdbg2	Hardware debug pin 2	O	U33
hw_wkdbg3	Hardware debug pin 3	O	V31
hw_wkdbg4	Hardware debug pin 4	O	V32
hw_wkdbg5	Hardware debug pin 5	O	P31
hw_wkdbg6	Hardware debug pin 6	O	K32
hw_wkdbg7	Hardware debug pin 7	O	K31
hw_wkdbg8	Hardware debug pin 8	O	NA(1)
hw_wkdbg9	Hardware debug pin 9	O	M31
hw_wkdbg10	Hardware debug pin 10	O	NA(1)
hw_wkdbg11	Hardware debug pin 11	O	NA(1)
hw_wkdbg12	Hardware debug pin 12	O	NA(1)
hw_wkdbg13	Hardware debug pin 13	O	N29
hw_wkdbg14	Hardware debug pin 14	O	N28
Observability Hardware Debug Bus: Core Domain			
hw_wkdbg15	Hardware debug pin 15	O	T31
hw_dbg16	Hardware debug pin 16	O	J32 / F13
hw_dbg17	Hardware debug pin 17	O	J33 / N9
hw_dbg18	Hardware debug pin 18	O	H32 / G13

Table 2-34. Hardware Debug Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
hw_dbg19	Hardware debug pin 19	O	J31 / E31
hw_dbg20	Hardware debug pin 20	O	G31 / AG20
hw_dbg21	Hardware debug pin 21	O	H31 / AH20
hw_dbg22	Hardware debug pin 22	O	G32 / AL9
hw_dbg23	Hardware debug pin 23	O	G33 / AM8
hw_dbg24	Hardware debug pin 24	O	G24 / AL8
hw_dbg25	Hardware debug pin 25	O	H24 / AN7
hw_dbg26	Hardware debug pin 26	O	E24 / AE7
hw_dbg27	Hardware debug pin 27	O	F24 / AD7
hw_dbg28	Hardware debug pin 28	O	G21 / AL32
hw_dbg29	Hardware debug pin 29	O	H21 / AL31
hw_dbg30	Hardware debug pin 30	O	E21 / AK31
hw_dbg31	Hardware debug pin 31	O	F21 / AK32

(1) NA in this table stands for not applicable for the OMAP5432 device.

2.4.7 General-Purpose IOs (GPIOs)

NOTE

For more information, see the General-Purpose Interface section of the OMAP543x TRM.

NOTE

Note that the following naming convention is used for the GPIO: gpio(N)_(wk)(In / Out)(Number)

With:

- N: bank name
- wk (for wakeable): the always-on GPIOs that have the capability to wake-up domains. If not specified, this means that the GPIO is not wakeable.
- In: Input only general-purpose signal
- Out: Output only general-purpose signal

Table 2-35. GPIO Signal Descriptions(2)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
gpio1_wk10	General-purpose IO, always on, wakeable	IO	NA(3)
gpio1_wk11	General-purpose IO, always on, wakeable	IO	P31
gpio1_wk12	General-purpose IO, always on, wakeable	IO	M31
gpio1_wk13	General-purpose IO, always on, wakeable	IO	N31
gpio1_wk14	General-purpose IO, always on, wakeable	IO	N28
gpio1_wk15	General-purpose IO, always on, wakeable	IO	N29
gpio1_wk16	General-purpose IO, always on, wakeable	IO	R33
gpio1_wk17	General-purpose IO, always on, wakeable	IO	T32
gpio1_wk6	General-purpose IO, always on, wakeable	IO	K32
gpio1_wk7	General-purpose IO, always on, wakeable	IO	K31
gpio1_wk8	General-purpose IO, always on, wakeable	IO	NA(3)
gpio1_wk9	General-purpose IO, always on, wakeable	IO	NA(3)
gpio1_wkout0	General-purpose output, always on, wakeable	O	U31
gpio1_wkout1	General-purpose output, always on, wakeable	O	U32
gpio1_wkout2	General-purpose output, always on, wakeable	O	U33
gpio1_wkout3	General-purpose output, always on, wakeable	O	V31
gpio1_wkout4	General-purpose output, always on, wakeable	O	V32
gpio1_wkout5	General-purpose output, always on, wakeable	O	NA(3)
gpio2_32	General-purpose IO	IO	P32
gpio2_33	General-purpose IO	IO	E25
gpio2_34	General-purpose IO	IO	F25
gpio2_35	General-purpose IO	IO	J29
gpio2_36	General-purpose IO	IO	J28
gpio2_37	General-purpose IO	IO	J27
gpio2_38	General-purpose IO	IO	H28
gpio2_39	General-purpose IO	IO	H29
gpio2_40	General-purpose IO	IO	G29
gpio2_41	General-purpose IO	IO	E29
gpio2_42	General-purpose IO	IO	E27
gpio2_43	General-purpose IO	IO	F26
gpio2_44	General-purpose IO	IO	E26

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
gpio2_45	General-purpose IO	IO	N27
gpio2_46	General-purpose IO	IO	AJ10
gpio2_47	General-purpose IO	IO	AH10
gpio2_48	General-purpose IO	IO	AG10
gpio2_49	General-purpose IO	IO	AF10
gpio2_50	General-purpose IO	IO	AH9
gpio2_51	General-purpose IO	IO	AJ9
gpio2_52	General-purpose IO	IO	AG9
gpio2_53	General-purpose IO	IO	AJ8
gpio2_54	General-purpose IO	IO	AH8
gpio2_55	General-purpose IO	IO	AJ7
gpio2_56	General-purpose IO	IO	J32
gpio2_57	General-purpose IO	IO	J33
gpio2_58	General-purpose IO	IO	H32
gpio2_59	General-purpose IO	IO	J31
gpio2_60	General-purpose IO	IO	G31
gpio2_61	General-purpose IO	IO	H31
gpio2_62	General-purpose IO	IO	G32
gpio2_63	General-purpose IO	IO	G33
gpio3_64	General-purpose IO	IO	NA[3]
gpio3_65	General-purpose IO	IO	NA[3]
gpio3_66	General-purpose IO	IO	NA[3]
gpio3_67	General-purpose IO	IO	NA[3]
gpio3_68	General-purpose IO	IO	NA[3]
gpio3_69	General-purpose IO	IO	NA[3]
gpio3_70	General-purpose IO	IO	NA[3]
gpio3_71	General-purpose IO	IO	NA[3]
gpio3_72	General-purpose IO	IO	NA[3]
gpio3_73	General-purpose IO	IO	NA[3]
gpio3_74	General-purpose IO	IO	NA[3]
gpio3_75	General-purpose IO	IO	NA[3]
gpio3_76	General-purpose IO	IO	G20
gpio3_77	General-purpose IO	IO	F20
gpio3_78	General-purpose IO	IO	F17
gpio3_79	General-purpose IO	IO	E20
gpio3_80	General-purpose IO	IO	E14
gpio3_81	General-purpose IO	IO	F14
gpio3_82	General-purpose IO	IO	G14
gpio3_83	General-purpose IO	IO	E17
gpio3_84	General-purpose IO	IO	F13
gpio3_85	General-purpose IO	IO	N9
gpio3_86	General-purpose IO	IO	G13
gpio3_87	General-purpose IO	IO	E13
gpio3_92	General-purpose IO	IO	NA[3]
gpio3_93	General-purpose IO	IO	NA[3]
gpio3_94	General-purpose IO	IO	K28
gpio3_95	General-purpose IO	IO	K29

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
gpio4_100	General-purpose IO	IO	AE27
gpio4_101	General-purpose IO	IO	AD29
gpio4_102	General-purpose IO	IO	AD28
gpio4_103	General-purpose IO	IO	AF29
gpio4_104	General-purpose IO	IO	AG29
gpio4_105	General-purpose IO	IO	AD26
gpio4_106	General-purpose IO	IO	AD27
gpio4_107	General-purpose IO	IO	AA26
gpio4_108	General-purpose IO	IO	AA27
gpio4_109	General-purpose IO	IO	AA28
gpio4_110	General-purpose IO	IO	AA29
gpio4_111	General-purpose IO	IO	Y29
gpio4_112	General-purpose IO	IO	Y28
gpio4_113	General-purpose IO	IO	G24
gpio4_114	General-purpose IO	IO	H24
gpio4_115	General-purpose IO	IO	E24
gpio4_116	General-purpose IO	IO	F24
gpio4_117	General-purpose IO	IO	G21
gpio4_118	General-purpose IO	IO	H21
gpio4_119	General-purpose IO	IO	E21
gpio4_120	General-purpose IO	IO	F21
gpio4_96	General-purpose IO	IO	W32
gpio4_97	General-purpose IO	IO	AF28
gpio4_98	General-purpose IO	IO	AE29
gpio4_99	General-purpose IO	IO	AE28
gpio5_128	General-purpose IO	IO	AH25
gpio5_129	General-purpose IO	IO	AG25
gpio5_130	General-purpose IO	IO	AJ26
gpio5_131	General-purpose IO	IO	AH26
gpio5_132	General-purpose IO	IO	AK28
gpio5_133	General-purpose IO	IO	AJ27
gpio5_134	General-purpose IO	IO	AL32
gpio5_135	General-purpose IO	IO	AL31
gpio5_136	General-purpose IO	IO	AK31
gpio5_137	General-purpose IO	IO	AK32
gpio5_138	General-purpose IO	IO	AL33
gpio5_139	General-purpose IO	IO	AM32
gpio5_140	General-purpose IO	IO	AM30
gpio5_141	General-purpose IO	IO	AL30
gpio5_142	General-purpose IO	IO	AL29
gpio5_143	General-purpose IO	IO	AN31
gpio5_144	General-purpose IO	IO	AM31
gpio5_145	General-purpose IO	IO	NA[3]
gpio5_146	General-purpose IO	IO	NA[3]
gpio5_147	General-purpose IO	IO	AL28
gpio5_148	General-purpose IO	IO	AL30
gpio5_149	General-purpose IO	IO	NA[3]

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
gpio5_150	General-purpose IO	IO	NA[3]
gpio5_151	General-purpose IO	IO	NA[3]
gpio5_152	General-purpose IO	IO	AN29
gpio5_153	General-purpose IO	IO	AJ25
gpio5_154	General-purpose IO	IO	AJ24
gpio5_155	General-purpose IO	IO	AG24
gpio5_156	General-purpose IO	IO	AH24
gpio5_158	General-purpose IO	IO	K26
gpio5_159	General-purpose IO	IO	K27
gpio6_160	General-purpose IO	IO	AN13
gpio6_161	General-purpose IO	IO	AM13
gpio6_162	General-purpose IO	IO	AL12
gpio6_163	General-purpose IO	IO	AL13
gpio6_164	General-purpose IO	IO	AL18
gpio6_165	General-purpose IO	IO	AM18
gpio6_166	General-purpose IO	IO	AL17
gpio6_167	General-purpose IO	IO	AM17
gpio6_168	General-purpose IO	IO	AN17
gpio6_169	General-purpose IO	IO	AL16
gpio6_170	General-purpose IO	IO	AM16
gpio6_171	General-purpose IO	IO	AL15
gpio6_172	General-purpose IO	IO	AM15
gpio6_173	General-purpose IO	IO	AN15
gpio6_174	General-purpose IO	IO	AL14
gpio6_175	General-purpose IO	IO	AM14
gpio6_176	General-purpose IO	IO	AM12
gpio6_177	General-purpose IO	IO	AL11
gpio6_178	General-purpose IO	IO	AM11
gpio6_179	General-purpose IO	IO	AN11
gpio6_180	General-purpose IO	IO	AL10
gpio6_181	General-purpose IO	IO	AM10
gpio6_182[1]	General-purpose IO	IO	AN9 / AN9 [1]
gpio6_183[1]	General-purpose IO	IO	AM9 / AM9 [1]
gpio6_184[1]	General-purpose IO	IO	AL9 / AL9 [1]
gpio6_185[1]	General-purpose IO	IO	AM8 / AM8 [1]
gpio6_186[1]	General-purpose IO	IO	AL8 / AL8 [1]
gpio6_187[1]	General-purpose IO	IO	AN7 / AN7 [1]
gpio6_188	General-purpose IO	IO	W31
gpio6_189	General-purpose IO	IO	W33
gpio6_190	General-purpose IO	IO	AJ33
gpio6_191	General-purpose IO	IO	AK30
gpio7_192	General-purpose IO	IO	AN23
gpio7_193	General-purpose IO	IO	AM23
gpio7_194	General-purpose IO	IO	AM22
gpio7_195	General-purpose IO	IO	AL23
gpio7_196	General-purpose IO	IO	AF20
gpio7_197	General-purpose IO	IO	AH17

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
gpio7_198	General-purpose IO	IO	AG20
gpio7_199	General-purpose IO	IO	AH20
gpio7_200	General-purpose IO	IO	AJ21
gpio7_201	General-purpose IO	IO	AJ20
gpio8_224	General-purpose IO	IO	AE6
gpio8_225	General-purpose IO	IO	AE5
gpio8_226	General-purpose IO	IO	AF6
gpio8_227	General-purpose IO	IO	AE7
gpio8_228	General-purpose IO	IO	AD5
gpio8_229	General-purpose IO	IO	AD6
gpio8_230	General-purpose IO	IO	AD7
gpio8_231	General-purpose IO	IO	AJ5
gpio8_232	General-purpose IO	IO	AH4
gpio8_233(1)	General-purpose IO	IO	AG5 / AG5 (1)
gpio8_234(1)	General-purpose IO	IO	AF5 / AF5 (1)
gpio8_in236	General-purpose input	I	U6
gpio8_in237	General-purpose input	I	U5
gpio8_in238	General-purpose input	I	P5
gpio8_in239	General-purpose input	I	P6
gpio8_in240	General-purpose input	I	P8
gpio8_in241	General-purpose input	I	P7
gpio8_in242	General-purpose input	I	N5
gpio8_in243	General-purpose input	I	N6
gpio8_in244	General-purpose input	I	N7
gpio8_in245	General-purpose input	I	N8
gpio8_in246	General-purpose input	I	Y6
gpio8_in247	General-purpose input	I	Y5
gpio8_in248	General-purpose input	I	Y7
gpio8_in249	General-purpose input	I	Y8
gpio8_in250	General-purpose input	I	AA5
gpio8_in251	General-purpose input	I	AA6
gpio8_in252	General-purpose input	I	J6
gpio8_in253	General-purpose input	I	J7
gpio8_in254	General-purpose input	I	K6
gpio8_in255	General-purpose input	I	K5

(1) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AN9 / AM9 / AL9 / AM8 / AL8 / AN7 / AG5 / AG5 / AF5) can output the same GPIO in mode 0 or in mode 6.

(2) The following naming convention is used for the GPIO: gpio(N)_(wk)(In / Out)(Number) with:

- N: bank name
- wk (for wakeable): the always-on GPIOs that have the capability to wake-up domains. If not specified, this means that the GPIO is not wakeable.
- In: Input only general-purpose signal
- Out: Output only general-purpose signal

(3) NA in this table stands for not applicable for the OMAP5432 device.

2.4.8 System and Miscellaneous

2.4.8.1 DM Timer

NOTE

For more information, see the Timers section of the OMAP543x TRM.

Table 2-36. DM Timer Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
timer5_pwm_evt	DM timer event input or PWM output	IO	AD5
timer6_pwm_evt	DM timer event input or PWM output	IO	AD6
timer8_pwm_evt	DM timer event input or PWM output	IO	AD7 / AG5
timer9_pwm_evt	DM timer event input or PWM output	IO	AJ33
timer10_pwm_evt	DM timer event input or PWM output	IO	W31
timer11_pwm_evt	DM timer event input or PWM output	IO	AE7

2.4.8.2 Keypad

NOTE

For more information, see Keyboard Controller / Keyboard Controller Environment section of the OMAP543x TRM.

Table 2-37. Keypad Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
kbd_row0	Keypad row 0	I	J27 / AM8
kbd_row1	Keypad row 1	I	H28 / AL8
kbd_row2	Keypad row 2	I	H29 / AN7
kbd_row3	Keypad row 3	I	G29 / AM14
kbd_row4	Keypad row 4	I	E29 / AM18
kbd_row5	Keypad row 5	I	E27 / AM13
kbd_row6	Keypad row 6	I	F26 / AM11
kbd_row7	Keypad row 7	I	E26 / AL11
kbd_row8	Keypad row 8	I	J28 / AM12
kbd_col0	Keypad column 0	O	J32 / AN9
kbd_col1	Keypad column 1	O	J33 / AM9
kbd_col2	Keypad column 2	O	H32 / AL9
kbd_col3	Keypad column 3	O	J31 / AL14
kbd_col4	Keypad column 4	O	G31 / AL18
kbd_col5	Keypad column 5	O	H31 / AN13
kbd_col6	Keypad column 6	O	G32 / AM10
kbd_col7	Keypad column 7	O	G33 / AL10
kbd_col8	Keypad column 8	O	F25 / AN11

2.4.8.3 System And Miscellaneous

NOTE

For more information, see:

- Power, Reset and Clock Management / PRCM Subsystem Environment / External Clock Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Reset Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section

of the OMAP543x TRM.

NOTE

Slicer functionality is not supported in the OMAP5432 device.

Table 2-38. System And Miscellaneous Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
fref_xtal_in	Crystal oscillator input	AI - I	L32
fref_xtal_out	Crystal oscillator output	AO	M32
fref_xtal_clk(1)	Crystal oscillator output – buffered directly from the input clock (dedicated for audio)	AO	L33
fref_slicer_in	Slicer positive input clock	AI	NA(2)
fref_clk_ioreq	FREF input clock request for main clock	IO	N31
fref_clk0_out	FREF clock 0 output: activated by default	O	M31
fref_clk1_out	FREF clock 1 output	O	P31
fref_clk2_out	FREF clock 2 output	O	NA(2)
fref_clk3_out	FREF clock 3 output	O	NA(2)
fref_clk1_req	FREF clock request 1	I	NA(2)
fref_clk2_req	FREF clock request 2	I	NA(2)
sys_32k	32-kHz clock input	I	L31
sys_nrespwron	OMAP power-on reset input	I	N33
sys_nreswarm	System warm reset output or input	IOD	N32
sys_pwr_req	Power request to exit off mode. Active high by default but configurable	O	T31
sys_nirq1	External interrupt 1 (aimed at PMIC power device connection)	I	R33
sys_nirq2	External interrupt 2 (aimed at PMIC power device connection)	I	T32
sys_drm_msecure	Secure transaction mode request (companion 0)	O	AF5
sys_aux_msecure	Secure transaction mode request (companion 1)	O	NA(2)
sys_secure_indicator	Secure transaction mode external indication	O	AG5
sys_boot0	Boot configuration: latched at power-on reset	I	U31
sys_boot1	Boot configuration: latched at power-on reset	I	U32
sys_boot2	Boot configuration: latched at power-on reset	I	U33
sys_boot3	Boot configuration: latched at power-on reset	I	V31
sys_boot4	Boot configuration: latched at power-on reset	I	V32
sys_boot5	Boot configuration: latched at power-on reset	I	NA(2)
sys_ndmareq0	External DMA request pipe 1	I	AN29
sys_ndmareq1	External DMA request pipe 2	I	NA(2)
sys_nodeid0	cJTAG node identifier bit 0 (up to 4 processors)	I	AE6
sys_nodeid1	cJTAG node identifier bit 1 (up to 4 processors)	I	AE5

(1) fref_xtal_clk is dedicated to audio purpose. A clean network is recommended.

(2) NA in this table stands for not applicable for the OMAP5432 device.

2.4.8.4 Power Supplies

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the OMAP543x TRM.

Table 2-39. Power Supply Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
vdds_1p8	Second IO power supply signal to ensure the VDDS ramping, and power supply for IO banks 2, 4, 5, 8-12, 14-16, 18, 19, 21, 23-26	PWR	H20 / J23 / J22 / J14 / J13 / J12 / L9 / M9 / P26 / P25 / R25 / U27 / U26 / W25 / Y25 / Y9 / AA25 / AA9 / AB25 / AC25 / AC9 / AD25 / AE24 / AE21 / AE15 / AE14 / AE13 / AF21 / U28
vdds_emmc	eMMC dual voltage IO power supply	PWR	AB9
vdds_c2c	Miscalenious IO power supply	PWR	J21 / J20
vdds_hsic	HS interchip data power supply	PWR	N26
vdda_dsiporta	DSI PHY (Port A) display primary port 1 – (main cut) power supply	PWR	AA33
vssa_dsiporta	DSI PHY (Port A) ground	GND	Y30
vdda_dsiportc	DSI PHY (Port C) display primary port 2 – main cut power supply	PWR	AE33
vssa_dsiportc	DSI PHY (Port C) ground	GND	AD30
vdds_hdmi	HDMI (digital part) power supply	PWR	AE23
vdda_hdmi	HDMI PHY (TMDS) power supply	PWR	AN25
vssa_hdmi	HDMI PHY ground	GND	AK24
vdda_csiporta	CSI (Port A) PHY camera (main cut) power supply	PWR	N3
vssa_csiporta	CSI (Port A) PHY camera (main cut) ground	GND	P4
vdda_csiportb	CSI (Port B) PHY camera (main cut) power supply	PWR	AA7
vssa_csiportb	CSI (Port B) PHY camera (main cut) ground	GND	Y4
vdda_csiportc	CSI (Port C) PHY camera (main cut) power supply	PWR	J5
vssa_csiportc	CSI (Port C) PHY camera (main cut) ground	GND	K4
vdda_sata	SATA PHY power supply	PWR	E9
vssa_sata	SATA PHY ground	GND	D10
vdds_sdcard	SD Card power supply	PWR	E5
vdds_usbhs18	USB HS (digital part) power supply	PWR	AE18
vdda_usbhs33	USB HS PHY power supply	PWR	AN21
vssa_usbhs	USB HS PHY ground	GND	AK20
vdda_usbss18	USB SS DRD PHY power supply	PWR	AE19
vssa_usbss	USB SS PHY ground	GND	AK21
vdds_osc	Crystal oscillator IO power supply	PWR	J24
vssa_xtal	Crystal oscillator IO Kelvin ground (same routing as OMAP3630 and OMAP4430)	GND	L30
vddq_vref_ddrch1	VREF cell power supply for DDR3 and DDR3L DQ channel 1 (or EMIF1)	PWR	J16
vddq_vref_ddrch2	VREF cell power supply for DDR3 and DDR3L DQ channel 2 (or EMIF2)	PWR	V10

Table 2-39. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
vdds_ddr_ch1	DDR3 and DDR3L (Channel 1) dm / dqs / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply	PWR	A27 / A11 / A3 / H30 / H10 / J19 / J18 / J10 / K30 / K25 / K23 / K15 / K14 / L25 / M25 / A21
vdds_ddr_ch2	DDR3 and DDR3L (Channel 2) dm / dqs / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply	PWR	E1 / J9 / K8 / N1 / R9 / T9 / V9 / W9 / AA1 / AC10 / AE12 / AE11 / AE10 / AJ1/ AM2
ddrch1_vref_dq	DDR3 and DDR3L, DQ Channel 1 VREF output power supply to memory	PWR	A19
ddrch2_vref_dq	DDR3 and DDR3L, DQ Channel 2 VREF output power supply to memory	PWR	U1
ddr3ch1_vref_ca	DDR3 and DDR3L addr / ba / ncas / nras / nreset / nwe / odt Channel 1 VREF output power supply to memory	PWR	A9
ddr3ch2_vref_ca	DDR3 and DDR3L addr / ba / ncas / nras / nreset / nwe / odt Channel 2 VREF output power supply to memory	PWR	AE1
vdd_core	Core and oscillator power supply	PWR	J11 / K22 / K12 / K11 / K9 / L14 / L13 / L12 / L10 / M14 / M13 / M11 / M10 / N15 / N14 / N11 / P11 / W24 / W22 / Y24 / Y23 / AA23 / AB24 / AB23 / AC24 / AC22 / AC21 / AD23 / AD22 / AD20 / AD16 / AD15 / AD14 / AD12
vdd_core_sense(1)	Core and oscillator output sensor feedback	PWR	AH21
vdd_mm	Multimedia power supply	PWR	T14 / T13 / T11 / T10 / W13 / W12 / W10 / Y19 / Y15 / Y11 / Y10 / AA19 / AA16 / AA15 / AA11 / AB19 / AB15 / AB13 / AB11 / AB10 / AC20 / AC16 / AC14 / AC13 / AC12 / AD19 / AD11
vdd_mm_sense(1)	Multimedia sensor output sensor feedback	PWR	AG21
vdd_mpu	MPU power supply	PWR	K20 / K19 / K18 / L24 / L22 / L21 / L20 / L18 / M24 / M23 / M20 / M19 / N23 / N18 / P24 / P23 / P22 / P18 / R24 / T24 / T23 / T21 / T20
vdd_mpu_sense(1)	MPU sensor output sensor feedback	PWR	U29
vss_mpu_sense(1)	MPU sensor output sensor feedback ground	GND	AJ29
vpp1	eFuse power supply	PWR	AD9
vss	Main ground	GND	D28 / D26 / D24 / D23 / D21 / D20 / D18 / D16 / D14 / D13 / D11 / D8 / D6 / F4 / H4 / L16 / L4 / M21 / M17 / M15 / N30 / N22 / N21 / N20 / N19 / N17 / N16 / N13 / N12 / N4 / P30 / P21 / P19 / P16 / P15 / P13 / P12 / P10 / P9 / R22 / R21 / R20 / R19 / R18 / R17 / R16 / R15 / R14 / R13 / R12 / R10 / T30 / T19 / T17 / T15 / T4 / U22 / U21 / U19 / U18 / U17 / U16 / U15 / U13 / U12 / V30 / V24 / V23 / V21 / V20 / V19 / V17 / V15 / V14 / V13 / V11 / V4 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W14 / Y22 / Y21 / Y18 / Y16 / Y13 / Y12 / AA30 / AA22 / AA21 / AA20 / AA18 / AA17 / AA14 / AA13 / AA12 / AA4 / AB21 / AB20 / AB17 / AB14 / AC30 / AC18 / AC4 / AD4 / AF30 / AF4 / AH30 / AK26 / AK23 / AK14 / AK13 / F30 / AK11 / AK10 / AK8 / AK6
vdda_dpll_core_emu_abe	Core, EMU, and ABE DPLL power supply	PWR	Y26
vdda_dpll_mm_l4per	MM and L4 interconnect DPLL power supply	PWR	U8
vdda_dpll_hdmi	HDMI PHY DPLL power supply	PWR	AF24
vdda_dpll_mpu	MPU DPLL power supply	PWR	Y27
vdda_ldo_core	Core SRAM LDO power supplu	PWR	AE22
vdda_ldo_mm	MM SRAM LDO power supply	PWR	AE20
vdda_ldo_mpu	MPU SRAM LDO power supply	PWR	J15
vdda_ldo_emu_wkup	Wake-up / emulation LDOs power supply	PWR	N25

Table 2-39. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]
vdda_vbgap_core	Bandgap, core LDOs power supply	PWR	AE16
cap_vdda_ldo_sram_core_array	Core SRAM array LDO output	PWR	T25
cap_vdda_ldo_sram_mm_array	MM SRAM array LDO output	PWR	AG17
cap_vdda_ldo_sram_mpu_array	MPU SRAM array LDO output	PWR	H17
cap_vdda_ldo_sram_mpu_array2	MPU SRAM array2 LDO output	PWR	K16
cap_vddldo_emu_wkup	MPU wake-up and EMU LDO output	PWR	V25
cap_vbb_ldo_mm	MPU MM LDO output	PWR	AD18
cap_vbb_ldo_mpu	MPU MPU LDO output	PWR	H13

(1) An optimized power distribution network is recommended for vdd_mpu_sense, vss_mpu_sense, vdd_mm_sense, and vdd_core_sense SMPS feedback sensors between the OMAP5432 and the power management IC (PMIC).

3 Electrical Characteristics

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the OMAP543x TRM.

3.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 3.3, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 3-1. Absolute Maximum Rating Over Junction Temperature Range

PARAMETER		Limits
Supply voltage ranges (steady state)	Core (vdd_mpu, vdd_mm, vdd_core, vdds_hsic, vddq_vref_ddrch1, vddq_vref_ddrch2, vdda_ldo_emu_wkup)	–0.4 V to 1.5 V
	I/O analog (vdds_1p8, vdda_dsiporta, vdda_dsiportc, vdda_hdmi, vdda_csiporta, vdda_csiportb, vdda_csiportc, vdda_sata, vdds_usbhs18, vdda_usbss18, vdda_dpll_core_emu_abe, vdda_dpll_mm_l4per, vdda_dpll_hdmi, vdda_dpll_mpu, vdda_ldo_mm, vdda_ldo_mpu, vdda_vbgap_core)	–0.5 V to 2.0 V
	I/O 1.8 V (vdds_c2c, vdds_hdmi, vdds_osc, vdda_ldo_core, vdds_emmc)	–0.5 V to 2.1 V
	I/O 3.3 V (vdds_sdcard, vdda_usbhs33)	–0.5 V to 3.8 V
Input and output voltage ranges (steady state)	Core I/Os	–0.4 V to 1.5 V
	Analog I/Os	–0.5 V to 2.0 V
	1.8-V I/Os	–0.5 V to 2.1 V
	3.3-V dual-voltage I/Os operating at 1.8 V	–0.5 V to 2.1 V
	3.3-V I/Os	–0.5 V to 3.8 V
T_J	Absolute junction temperature range (vpp turned off—floating)	–40°C to 125°C
Electrostatic Discharge (ESD) Performance(1)	ESD-HBM (Human Body Model)(2)	±1000 V
	ESD-CDM (Charged Device Model)(3)	±250 V
Latch-up I-test performance	Current-pulse injection on each I/O pin	±100 mA(5)
Latch-up overvoltage performance	Voltage injection on each supply	1.5 × Vddmax(6)
T_{STG}(4)	Storage temperature range after soldered onto PC board	–65°C to 150°C

(1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by electrostatic discharges into the device.

(2) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.

(3) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.

(4) For tape and reel the storage temperature range is [–10°C to 50°C] with a maximum relative humidity of 70%. It is recommended returning to ambient room temperature before usage.

(5) Pins stressed per JEDEC JESD78D at 120°C (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.

(6) Supplies stressed per JEDEC JESD78D at 120°C (Class II) and passed specified voltage injection.

3.2 Maximum Current Ratings at Ball Level

Table 3-2 summarizes the maximum estimated power consumption at the ball level.

Table 3-2. Maximum Current Ratings at Ball Level(1)

PARAMETER			MAX	UNIT
vdd_mpu(1)	Maximum current rating for MPU	MPU at OPPSPEEDBIN	6460	mA
		MPU at HIGH	4400	
vdd_mm(1)	Maximum current rating for multimedia		2145	mA
vdd_core(1)	Maximum current rating for core, DLL		890	mA
vdds_1p8	Maximum current rating for second IO signal to ensure the VDDS ramping		See(3)	mA
vdds_emmc	Maximum current rating for eMMC dual-voltage IO		See(3)	mA
vdds_c2c	Maximum current rating for Miscalenious IO		See(3)	mA
vdds_hsic	Maximum current rating for HS interchip data		See(3)	mA
vdda_dsiporta	Maximum current rating for DSI PHY (Port A) display primary port 1 (main cut), DSI1_A		19.3	mA
vdda_dsiportc	Maximum current rating for DSI PHY (Port C) display primary port 2 (main cut), DSI1_C		19.3	mA
vdds_hdmi	Maximum current rating for HDMI IOs (CEC, HPD, DDC)		See(3)	mA
vdda_hdmi	Maximum current rating for HDMI PHY (TMDS)		15.0	mA
vdda_csiporta	Maximum current rating for CSI (Port A) PHY camera (main cut)		4.6	mA
vdda_csiportb	Maximum current rating for CSI (Port B) PHY camera (main cut)		2.7	mA
vdda_csiportc	Maximum current rating for CSI (Port C) PHY camera (main cut)		1.75	mA
vdda_sata	Maximum current rating for SATA PHY		40.0	mA
vdds_sdcard	Maximum current rating for SD Card		See(3)	mA
vdds_usbhs18	Maximum current rating for USB HS (digital part)		26.0	mA
vdda_usbhs33	Maximum current rating for USB HS PHY		34.0	mA
vdda_usbss18	Maximum current rating for USB SS DRD PHY		45.0	mA
vdds_osc	Maximum current rating for crystal oscillator IO		2.0	mA
vdds_ddr_ch1	Maximum current rating for DDR3 and DDR3L (channel 1) dm / dqs / ndqs		400	mA
vdds_ddr_ch2	Maximum current rating for DDR3 and DDR3L (channel 2) dm / dqs / ndqs		400	mA
vddq_vref_ddrch1	Maximum current rating for VREF cell power supply for DDR3 and DDR3L DQ channel 1 (or EMIF1)		400	mA
vddq_vref_ddrch2	Maximum current rating for VREF cell power supply for DDR3 and DDR3L DQ channel 2 (or EMIF2)		400	mA
vpp1(2)	Maximum current rating for eFuse		50	mA
vdda_dpll_core_emu_abe	Maximum current rating for core, EMU, and ABE DPLL		9.0	mA
vdda_dpll_mm_l4per	Maximum current rating for MM and L4 interconnect DPLL		6.0	mA
vdda_dpll_hdmi	Maximum current rating for HDMI PHY DPLL		6.0	mA
vdda_dpll_mpu	Maximum current rating for MPU DPLL		3.0	mA
vdda_ldo_core	Maximum current rating for core SRAM LDO		60.0	mA
vdda_ldo_mm	Maximum current rating for MM SRAM LDO		85.0	mA
vdda_ldo_mpu	Maximum current rating for MPU SRAM LDO		145.0	mA
vdda_ldo_emu_wkup	Maximum current rating for wake-up / emulation LDOs		75.0	mA
vdda_vbgap_core	Maximum current rating for bandgap, core LDOs		5.0	mA

(1) With SmartReflex™ enabled

(2) VPP1 must not be connected.

(3) The sum of the maximum current consumption for these power supplies is 260 mA.

3.3 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 3-3.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 3-3. Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
Input Power Supply Voltage Range						
vdd_mpu	Supply voltage range for MPU domain			See(1)		V
	Maximum noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f ≥ 10 MHz		50		
vdd_mm	Supply voltage range for multimedia domain			See(1)		V
	Maximum noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f ≥ 10 MHz		50		
vdd_core	Supply voltage range for OMAP core and DLL domain			See(1)		V
	Maximum noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f ≥ 10 MHz		50		
vdda_dpll_mpu	Supply voltage for MPU DPLLs		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_core_emu_abe	Supply voltage for core, emulation, and audio DPLLs		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_mm_l4per	Supply voltage for multimedia and L4 interconnect DPLLs		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_hdmi	Supply voltage for HDMI DPLL		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_mpu	Supply voltage for MPU SRAM LDO		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_core	Supply voltage for core SRAM LDO		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_mm	Supply voltage for MM SRAM LDO		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_emu_wkup	Supply voltage for wake-up and emulation LDOs		1.14	1.20	1.26	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_vbgap_core	Supply voltage for bandgap, core LDOs power supply		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_csiporta	Supply voltage for CSI (Port A) PHY camera (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_csiportb	Supply voltage for CSI (Port B) PHY camera (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdda_csiportc	Supply voltage for CSI (Port C) PHY camera (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_dsiporta	Supply voltage for DSI PHY (Port A) display primary port 1—(main cut), DSI1_A	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_dsiportc	Supply voltage for DSI PHY (Port C) display primary port 2—main cut, DSI1_C	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_hdmi	Supply voltage for HDMI (analog part)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_hdmi	Supply voltage for HDMI IOs (CEC, HPD, DDC)	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_sata	Supply voltage for SATA PHY	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdda_usbhs33	Supply voltage for USB HS PHY	3.3-V Mode	3.14	3.30	3.46	V
	Maximum noise (peak-peak)	3.3-V Mode		50		mV_{PPmax}
vdds_usbhs18	Supply voltage for USB HS (digital part)	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdda_usbss18	Supply voltage for USB SS DRD PHY	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdds_c2c	Supply voltage for Miscalenious IO	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_emmc	Supply voltage for eMMC	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_hsic	Supply voltage for HS interchip data	1.2-V Mode	1.14	1.20	1.26	V
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
vdds_osc	Supply voltage for crystal oscillator	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdds_sdcard	Supply voltage for SD Card	1.8-V Mode	1.71	1.80	1.89	V
		3.0-V Mode	2.70	3.00	3.60	
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
		3.0-V Mode				
vdds_1p8v	Supply voltage for 1.8-V IO macros	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vpp1[2]	Supply voltage for eFuse			See [2]		V
vdds_ddr_ch1	DDR3, DDR3 (Channel 1) dm / dqs / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply		1.35	1.50	1.58	V
	DDR3L, DDR3L (Channel 1) dm / dqs / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply		1.28	1.35	1.42	
	Maximum noise (peak-peak)				75	mV_{PPmax}
vdds_ddr_ch2	DDR3, DDR3 (Channel 2) dm / dqs / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply		1.35	1.50	1.58	V
	DDR3L, DDR3L (Channel 2) dm / dqs / ndqs / addr / ba / ncas / nras / nreset / nwe / odt power supply		1.28	1.35	1.42	
	Maximum noise (peak-peak)				75	mV_{PPmax}
vddq_vref_ddrch1	VREF cell power supply for DDR3, DDR3L, DQ channel 1 (or EMIF1)			vdds_ddr_ch1[3]		V
	Maximum noise (peak-peak)				75	mV_{PPmax}
vddq_vref_ddrch2	VREF cell power supply for DDR3, DDR3L, DQ channel 2 (or EMIF2)			vdds_ddr_ch2[3]		V
	Maximum noise (peak-peak)				75	mV_{PPmax}
vss	Main ground			0		V
vssa_dsiporta	DSI PHY (Port A) DSI1_A ground			0		V
vssa_dsiportc	DSI PHY (Port C) DSI1_C ground			0		V
vssa_hdmi	HDMI PHY ground			0		V
vssa_csiporta	CSI (Port A) PHY camera (main cut) ground			0		V
vssa_csiportb	CSI (Port B) PHY camera (main cut) ground			0		V
vssa_csiportc	CSI (Port C) PHY camera (main cut) ground			0		V
vssa_sata	SATA PHY ground			0		V
vssa_usbhs	USB HS PHY ground			0		V
vssa_usbss	USB SS PHY ground			0		V
vssa_xtal	Crystal oscillator IO Kelvin ground (same routing as for OMAP3630 and OMAP4430)			0		V
vss_mpu_sense	MPU sensor ground			0		V
T_B[4]	Operating board (PCB) temperature range		–40		85	°C
T_J[4]	Operating junction temperature range (vpp turned off—floating)		–40		105[5]	°C
$T_{J\text{-}VPP}$[2]	Operating junction temperature range during eFuse programming (vpp turned on)		–10		65	°C
Output Power Supply Voltage Range						
ddrch1_vref_dq	DDR3, DDR3L DQ channel 1 VREF output power supply to memory		0.49 × vdds_ddr_ch1	0.5 × vdds_ddr_ch1	0.51 × vdds_ddr_ch1	V
	Maximum noise (peak-peak)		–0.01 × vdds_ddr_ch1		0.01 × vdds_ddr_ch1	mV_{PPmax}

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
ddrch2_vref_dq	DDR3, DDR3L DQ channel 2 VREF output power supply to memory	0.49 × vdds_ddr_ch2	0.5 × vdds_ddr_ch2	0.51 × vdds_ddr_ch2	V
	Maximum noise (peak-peak)	–0.01 × vdds_ddr_ch2		0.01 × vdds_ddr_ch2	mV_{PPmax}
ddr3ch1_vref_ca	DDR3, DDR3L addr / ba / ncas / nras / nreset / nwe / odt channel 1 VREF output power supply to memory	0.49 × vdds_ddr_ch1	0.5 × vdds_ddr_ch1	0.51 × vdds_ddr_ch1	V
	Maximum noise (peak-peak)	–0.01 × vdds_ddr_ch1		0.01 × vdds_ddr_ch1	mV_{PPmax}
ddr3ch2_vref_ca	DDR3, DDR3L addr / ba / ncas / nras / nreset / nwe / odt channel 2 VREF output power supply to memory	0.49 × vdds_ddr_ch2	0.5 × vdds_ddr_ch2	0.51 × vdds_ddr_ch2	V
	Maximum noise (peak-peak)	–0.01 × vdds_ddr_ch2		0.01 × vdds_ddr_ch2	mV_{PPmax}

(1) See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

(2) A pulse width of 1000 ns and an amplitude of 2 V is required to program each eFuse bit. Otherwise, VPP1 must not be supplied.

(3) vddq_vref_ddrch1 must be supplied from the same regulator as vdds_ddr_ch1. vddq_vref_ddrch2 must be supplied from the same regulator as vdds_ddr_ch2.

(4) The board temperature (T_B) and junction temperature (T_J) range is defined for 2S2P board types (reference JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

(5) Product can be run at 120°C T_J for 9000 power-on hours.

3.4 DC Electrical Characteristics

This section summarizes the dc electrical characteristics.

NOTE

The data specified in this section are subject to change.

NOTE

The interfaces or signals described in this section correspond to the interfaces or signals available in multiplexing mode 0.

All interfaces or signals multiplexed on the balls described in this section have the same dc electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different dc electrical characteristics are specified for the different multiplexing modes.

3.4.1 DDR3 and DDR3L DC Electrical Characteristics

Table 3-4 summarizes the DDR3 and DDR3L dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (i[2:0], sr[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.

Table 3-4. DDR3 and DDR3L DC Electrical Characteristics(3)

PARAMETER			MIN	NOM	MAX	UNIT
Signal Names in Mode 0 (Single-Ended Signals): ddrch1_dm[0-3], ddrch1_dq[0-31], ddr3ch1_a[0-9], ddr3ch1_a10_ap, ddr3ch1_a11, ddr3ch1_a12_nbc, ddr3ch1_a[13-15], ddr3ch1_cke[0-1], ddr3ch1_ncs[0-1], ddr3ch1_ba[0-2], ddr3ch1_ncas, ddr3ch1_nras, ddr3ch1_nreset, ddr3ch1_nwe, ddr3ch1_odt[0-1], ddrch2_dm[0-3], ddrch2_dq[0-31], ddrch2_dqs[0-3], ddrch2_ndqs[0-3], ddr3ch2_a[0-9], ddr3ch2_a10_ap, ddr3ch2_a11, ddr3ch2_a12_nbc, ddr3ch2_a[13-15], ddr3ch2_ck[a-b], ddr3ch2_cke[0-1], ddr3ch2_nck[a-b], ddr3ch2_ncs[0-1], ddr3ch2_ba[0-2], ddr3ch2_ncas, ddr3ch2_nras, ddr3ch2_nreset, ddr3ch2_nwe, ddr3ch2_odt[0-1]						
Bottom Balls: A29 / B24 / C30 / B6 / C28 / A31 / C29 / B30 / B29 / C26 / B28 / B26 / C23 / C22 / C21 / B22 / C24 / C25 / B25 / A25 / E31 / E33 / E32 / F32 / C33 / D30 / F31 / C32 / C6 / A5 / B5 / C5 / B2 / B3 / C3 / D4 / A7 / B7 / C7 / B8 / C8 / B9 / C10 / B12 / C12 / A13 / B13 / C13 / B14 / C14 / A15 / B15 / C9 / A17 / B10 / B17 / C15 / B16 / C16 / C17 / B19 / C19 / B20 / C20 / B21 / J1 / AJ3 / G1 / AL4 / K3 / H2 / H3 / J3 / J2 / M3 / L2 / L1 / AK3 / AG1 / AH3 / AJ2 / AH2 / AL1 / AL3 / AK4 / G3 / D3 / C2 / C1 / D2 / F2 / G2 / F3 / AM3 / AL5 / AM4 / AN3 / AL7 / AL6 / AM7 / AM6 / AG2 / AG3 / F2 / AF3 / AE2 / AE3 / AC3 / AB2 / AB3 / AA2 / AA3 / Y2 / Y3 / W1 / W2 / W3 / AD2 / U3 / AD3 / T2 / V2 / V3 / U2 / T3 / R3 / P2 / P3 / N2 / M2						
Driver mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 × vddx_ddr3(1)		vddx_ddr3(1) + 0.2	V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)		–0.2		0.1 × vddx_ddr3(1)	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)(5)	I[2:0] = 000 (Imp80)	68	80	92	Ω
		I[2:0] = 001 (Imp60)	51	60	69	
		I[2:0] = 010 (Imp48)	41	48	55	
		I[2:0] = 011 (Imp40)	34	40	46	
		I[2:0] = 100 (Imp34)	29	34	39	

Table 3-4. DDR3 and DDR3L DC Electrical Characteristics[3] (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}	Output transition time (rise time t_R or fall time t_F, evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 Ω and C_{LOAD} = 5 pF[3]	sr[2:0] = 000 (Fastest)	0.162		0.325	ns
		sr[2:0] = 001 (Faster)	0.162		0.33	
		sr[2:0] = 010 (Fast)	0.162		0.34	
		sr[2:0] = 011 (Slow)	0.168		0.35	
		sr[2:0] = 100 (Slower)	0.168		0.35	
		sr[2:0] = 101 (Slowest-1)	0.168		0.36	
		sr[2:0] = 110 (Slowest-2)	0.168		0.36	
		sr[2:0] = 111 (Slowest-3)	0.175		0.36	
Single-Ended Receiver mode						
V_{IH}	High-level input threshold		vddy_vref_ddr3[2] + 0.10		vddx_ddr3[1] + 0.2	V
V_{IL}	Low-level input threshold		–0.2		vddy_vref_ddr3[2] – 0.10	V
V_{CM}	Input common-mode voltage		vddy_vref_ddr3[2] – 0.1 × vddx_ddr3[1]		vddy_vref_ddr3[2] + 0.1 × vddx_ddr3[1]	V
Z_I	Input impedance	odt[1:0][4] = 00	Off	Off	Off	Ω
		odt[1:0][4] = 01	48	60	72	
		odt[1:0][4] = 10	64	80	96	
		odt[1:0][4] = 11	78	120	162	
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Signal Names in Mode 0 (Differential Signals): ddrch1_dqs[0-3], ddrch1_ndqs[0-3], ddr3ch1_ck[a-b], ddr3ch1_nck[a-b], ddrch2_dqs[0-3], ddrch2_ndqs[0-3], ddr3ch2_ck[a-b], ddr3ch2_nck[a-b], **Bottom Balls:** C27 / B23 / D31 / C4 / B27 / A23 / D32 / B4 / C11 / C18 / B11 / B18 / K2 / AK2 / E2 / AM5 / L3 / AL2 / E3 / AN5 / AC2 / R2 / AC1 / R1						
Driver mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 × vddx_ddr3[1]			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1 × vddx_ddr3[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)[5]	I[2:0] = 000 (Imp80)	68	80	92	Ω
		I[2:0] = 001 (Imp60)	51	60	69	
		I[2:0] = 010 (Imp48)	41	48	55	
		I[2:0] = 011 (Imp40)	34	40	46	
		I[2:0] = 100 (Imp34)	29	34	39	
t_{OT}	Output transition time (rise time t_R or fall time t_F, evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 Ω and C_{LOAD} = 5 pF[3]	sr[2:0] = 000 (Fastest)	0.162		0.325	ns
		sr[2:0] = 001 (Faster)	0.162		0.33	
		sr[2:0] = 010 (Fast)	0.162		0.34	
		sr[2:0] = 011 (Slow)	0.168		0.35	
		sr[2:0] = 100 (Slower)	0.168		0.35	
		sr[2:0] = 101 (Slowest-1)	0.168		0.36	
		sr[2:0] = 110 (Slowest-2)	0.168		0.36	
		sr[2:0] = 111 (Slowest-3)	0.175		0.36	
Single-Ended Receiver mode						
V_{IH}	High-level input threshold		0.5 × vddx_ddr3[1] + 0.13		vddx_ddr3[1] + 0.2	V
V_{IL}	Low-level input threshold		–0.2		0.5 × vddx_ddr3[1] – 0.13	V

ADVANCE INFORMATION

Table 3-4. DDR3 and DDR3L DC Electrical Characteristics[3] (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Z_I	Input impedance	odt[1:0][4] = 00	OFF	OFF	OFF	Ω
		odt[1:0][4] = 01	48	60	72	
		odt[1:0][4] = 10	64	80	96	
		odt[1:0][4] = 11	78	120	162	
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Differential Receiver mode						
V_{SWING}	Input voltage swing		0.20		vddx_ddr3[1] + 0.4	V
V_{CM}	Input common-mode voltage		0.4 × vddx_ddr3[1]		0.6 × vddx_ddr3[1]	V
Z_I	Input impedance	odt[1:0][4] = 00	OFF	OFF	OFF	Ω
		odt[1:0][4] = 01	48	60	72	
		odt[1:0][4] = 10	64	80	96	
		odt[1:0][4] = 11	78	120	162	
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Signal Names in Mode 0 (VREF Signals): ddrch1_vref_dq, ddrch2_vref_dq, ddr3ch1_vref_ca, ddr3ch2_vref_ca **Bottom Balls:** A19 / U1 / A9 / AE1						
V_{REF}	Reference internal generation dc voltage level	vref_tap[1:0] = 00, 2-µA current load	0.49 × vddq_vref_ddrchy[2]	0.50 × vddq_vref_ddrchy[2]	0.51 × vddq_vref_ddrchy[2]	V
		vref_tap[1:0] = 01, 4-µA current load	0.49 × vddq_vref_ddrchy[2]	0.50 × vddq_vref_ddrchy[2]	0.51 × vddq_vref_ddrchy[2]	
		vref_tap[1:0] = 10, 8-µA current load	0.49 × vddq_vref_ddrchy[2]	0.50 × vddq_vref_ddrchy[2]	0.51 × vddq_vref_ddrchy[2]	
		vref_tap[1:0] = 11, 32-µA current load	0.49 × vddq_vref_ddrchy[2]	0.50 × vddq_vref_ddrchy[2]	0.51 × vddq_vref_ddrchy[2]	
C_{CAP}	Decoupling capacitor	ccap[1:0] = 00	No capacitor connected			
		ccap[1:0] = 01	Capacitor between Bias2 and V_{SS}			
		ccap[1:0] = 10	Capacitor between Bias2 and V_{DDS}			
		ccap[1:0] = 11	Capacitor between Bias2 and V_{SS} and capacitor between Bias2 and V_{DDS}			

(1) vddx_ddr3 can have the value vdds_ddr_ch1, vdds_ddr_ch2, vddq_vref_ddrch1, or vddq_vref_ddrch2 depending on the ball used. For more information on the power supply name and the corresponding ball, see Table 2-1, POWER NAME [10] column.

(2) vddq_vref_ddrchy can have the value vddq_vref_ddrch1 or vddq_vref_ddrch2 depending on the ball used. For more information on the power supply name and the corresponding ball, see Table 2-1, POWER NAME [10] column.

(3) Output transition time or turn-on time is measured with the measurement setup (see Figure 3-1) with Z_O = 40 Ω and C_{LOAD} = 5 pF (lumped, no transmission line model).

(4) The ODT register can configure the on-die termination impedance. For more information, see the OMAP543x TRM.

(5) It is recommended to use 34 Ω and 40 Ω for actual use cases, for optimum performance.

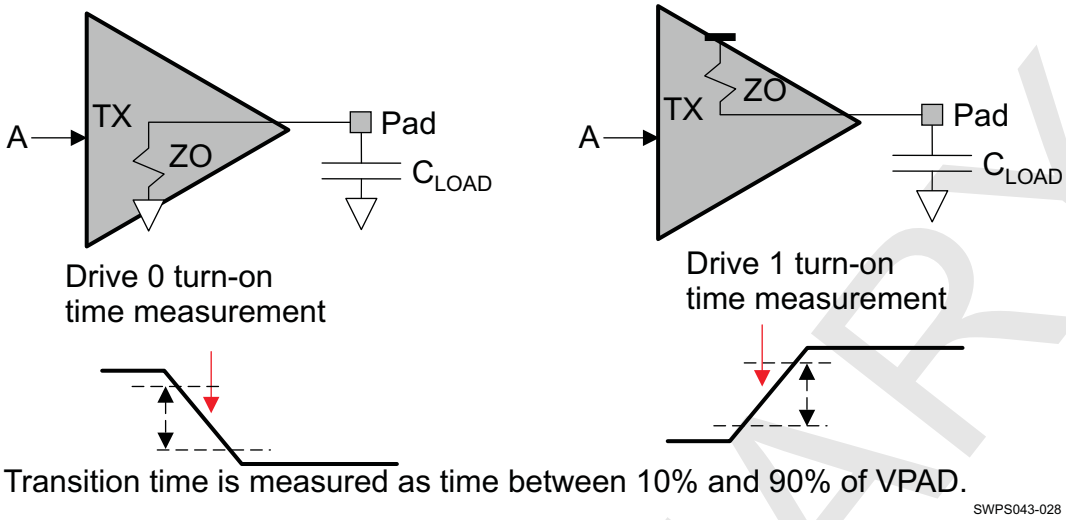


Figure 3-1. Output Transition Time Measurement

3.4.2 Camera DC Electrical Characteristics

3.4.2.1 CSI-2 MIPI D-PHY and CCPV2 DC Electrical Characteristics

NOTE

For more information on the CSI-2 IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.4.3 Display DC Electrical Characteristics

3.4.3.1 HDMI DC Electrical Characteristics

NOTE

For more information on HDMI, please contact your TI representative.

3.4.3.2 DSI-1 MIPI D-PHY (DSI1_A and DSI1_C) DC Electrical Characteristics

NOTE

For more information on the DSI-1 IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.4.4 I^2C DC Electrical Characteristics

NOTE

For more information on the I^2C IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.4.5 USB DC Electrical Characteristics

NOTE

The following interfaces are not available in the OMAP5432 device:

- USB (Port D0) – ULPI 8-bit
- USB (Port B1) – HSIC1
- USB (Port B2) – ULPI 8-bit
- USB (Port B2) – Full Speed / Low Speed

For more information, see the OMAP543x TRM.

3.4.5.1 USB2 PHY DC Electrical Characteristics

NOTE

For more information on the USB2 PHY IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.4.5.2 USB HSIC DC Electrical Characteristics

NOTE

For more information on the USB HSIC IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.4.5.3 USB3 PHY DC Electrical Characteristics

NOTE

The USB3 RX PHY module is compliant with the receiver electrical parameters specified in the *Universal Serial Bus 3.0 Specification*, Revision 1.0, November 12, 2008.

NOTE

The USB3 TX PHY module is compliant with the transmitter electrical parameters and LFPS electrical parameters specified in the *Universal Serial Bus 3.0 Specification*, Revision 1.0, November 12, 2008.

NOTE

For more information regarding the USB3 pin name (or ball name) and corresponding signal name, see Table 2-22, *USB Signal Descriptions*.

3.4.6 SD Card DC Electrical Characteristics

NOTE

For more information on the SD Card IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.4.7 SATA PHY DC Electrical Characteristics

NOTE

The SATA RX PHY module is compliant with the electrical specifications of SATA up to Gen2m.

NOTE

The SATA TX PHY module is compliant with the electrical specifications of SATA up to Gen2m.

NOTE

For more information regarding the SATA PHY pin name (or ball name) and corresponding signal name, see Table 2-23, *SATA Signal Descriptions*.

3.4.8 System DC Electrical Characteristics

NOTE

For more information on the System IO DC Electrical Characteristics, see the OMAP5430 data manual.

NOTE

Slicer functionality is not supported in the OMAP5432 device.

3.4.9 DC Electrical Characteristics for Other Balls

NOTE

For more information on the SMART IO DC Electrical Characteristics, see the OMAP5430 data manual.

3.5 External Capacitors

NOTE

For more information regarding the external capacitors, see the Power Integrity section of the OMAP5432 Multimedia Processor Device PCB Guidelines chapter.

3.6 Power-up and Power-down Sequences

NOTE

Slicer functionality is not supported in the OMAP5432 device.

3.6.1 Power-Up Sequence

NOTE

For more information, see Power, Reset and Clock Management / Reset Management Functional Description / Reset Sequences of the OMAP543x TRM.

Figure 3-2 shows the power-up sequence.

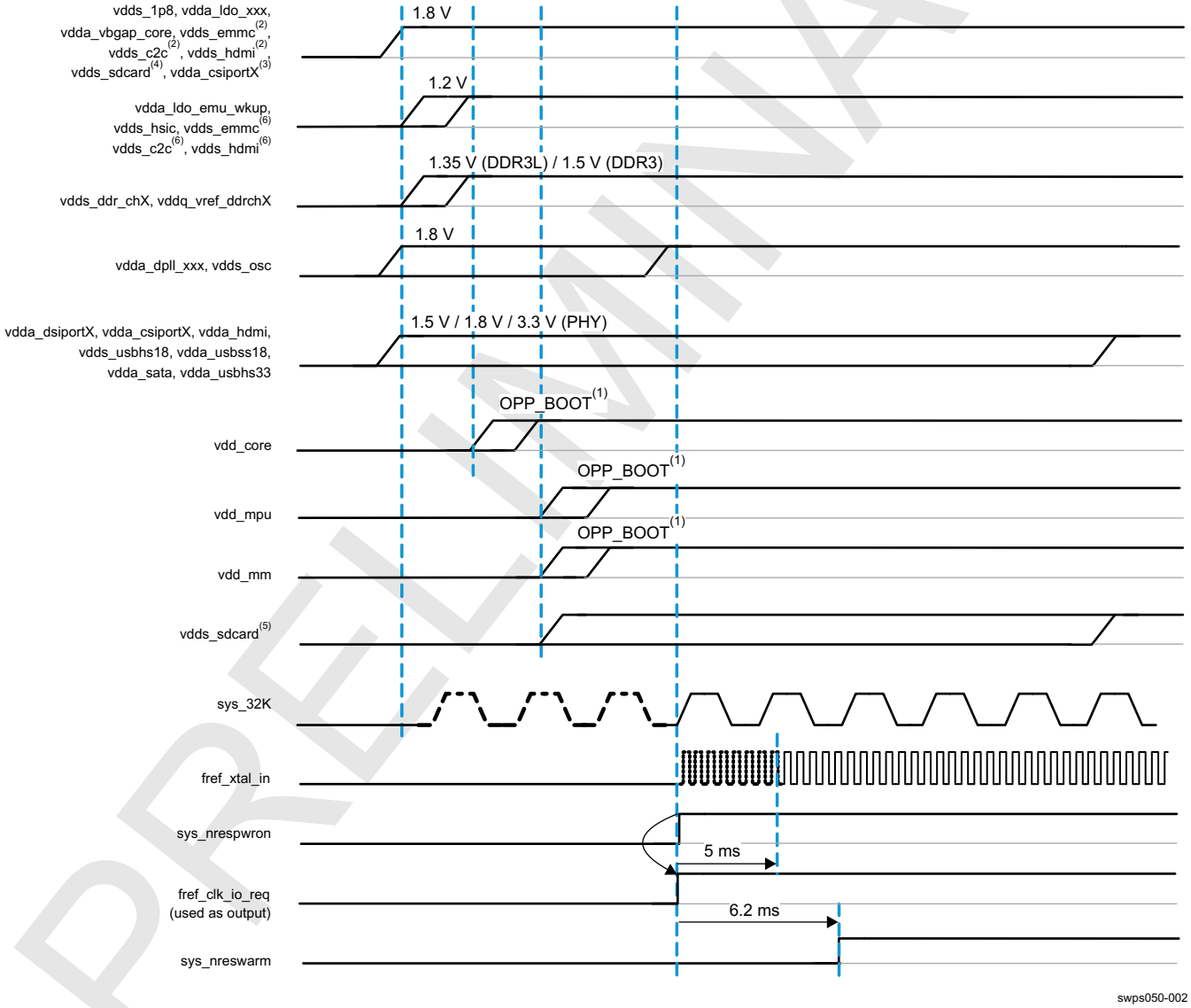


Figure 3-2. Power-Up Sequence

(1) The OMAP5432 ES2.0 device boots up with vdd_core, vdd_mpu, and vdd_mm @OPP_BOOT. See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

(2) In case the corresponding interfaces are used at 1.8 V.

(3) In case the MIPI CSI-2 interface is used as GPIO or CPI (function different from Muxmode 0).

(4) In case the SDCARD interface is used at 1.8 V only (function different from Muxmode 0).

(5) In case the SDCARD functional signals are used at 1.8 V or 3.0 V (Muxmode 0).

(6) In case the corresponding interfaces are used at 1.2 V.

NOTE

The DPLLs voltage supplies (vdda_dpll_xxx) and the system clock IOs voltage supplies (vdds_osc) can be turned on at the same time as the other 1.8-V voltage supplies or only before sys_nrespwron release.

The 1.5-V, 1.8-V, and 3.3-V PHY voltage supplies can be turned on at the same time as the other 1.8-V voltage supplies or only when the corresponding applications are needed.

Once vdda_ldo_emu_wkup is turned on, vdd_core can be turned on. Once vdd_core is turned on, vdd_mpu and vdd_mm can be turned on.

If the SDCARD functional signals are used at 1.8-V or 3.0-V, the vdds_sdcard voltage supply can be turned on any time after vdd_core ramp-up or only when the applications are needed.

sys_32k can be turned on any time after vdds_1p8 ramp-up and before sys_nrespwron release.

Once the sys_nrespwron is released, OMAP5432 activates the fref_clk_ioreq signal. Therefore, the fref_xtal_in clock can be turned on. (Nevertheless, the system can turn on the fref_xtal_in or clock before the fref_clk_ioreq activation provided the voltage supplies of the system clock IOs are turned on.)

5 ms after the sys_nrespwron release, the system clock is considered as stabilized on the OMAP5432 oscillator input. The clock may be supplied later provided it is perfectly stabilized when supplied.

1.2 ms (about 40 additional 32-kHz clock cycles) after the system clock is considered as stabilized, OMAP5432 releases its sys_nreswarm.

NOTE

Customer designs may optionally power-up only the boot interfaces (eMMC, uSD card, USB, and SATA) that their particular design needs to use. For example, if only eMMC is required then uSD card, USB, and SATA supplies do not need to be powered up. The TWL6037 PMIC is programmed to power up all the possible interfaces in order to be able to boot on any possible interface.

3.6.2 Power-Down Sequence

The following steps give two examples of power-down sequence supported by the OMAP5432 device:

1. Put the OMAP5432 device under reset (sys_nrespwron).
2. Stop all signals driven to its balls (sys_32k or fref_xtal_in).
3. Either:
   (a) Shutdown all voltage supplies at once. This sequence is described in black color in Figure 3-3.
   (b) Or, if the shutdown is sequenced, described in dashed blue color inFigure 3-3:
      (i) Turn off all PHY voltage supplies and SDCARD voltage supply.
      (ii) Turn off the multimedia (IVA, DSP, GPU) voltage domain supply (vdd_mm).
      (iii) Turn off the MPU voltage domain supply (vdd_mpu).
      (iv) Turn off the core voltage domain supply (vdd_core).
      (v) Turn off all DPLL and system clock IO voltage supplies.
      (vi) Turn off all 1.2-V IO voltage supplies.
      (vii) Turn off all remaining 1.8-V IO voltage supplies.

Figure 3-3 shows both power-down sequences: one of them is described in black color, and the other one in dashed blue color.

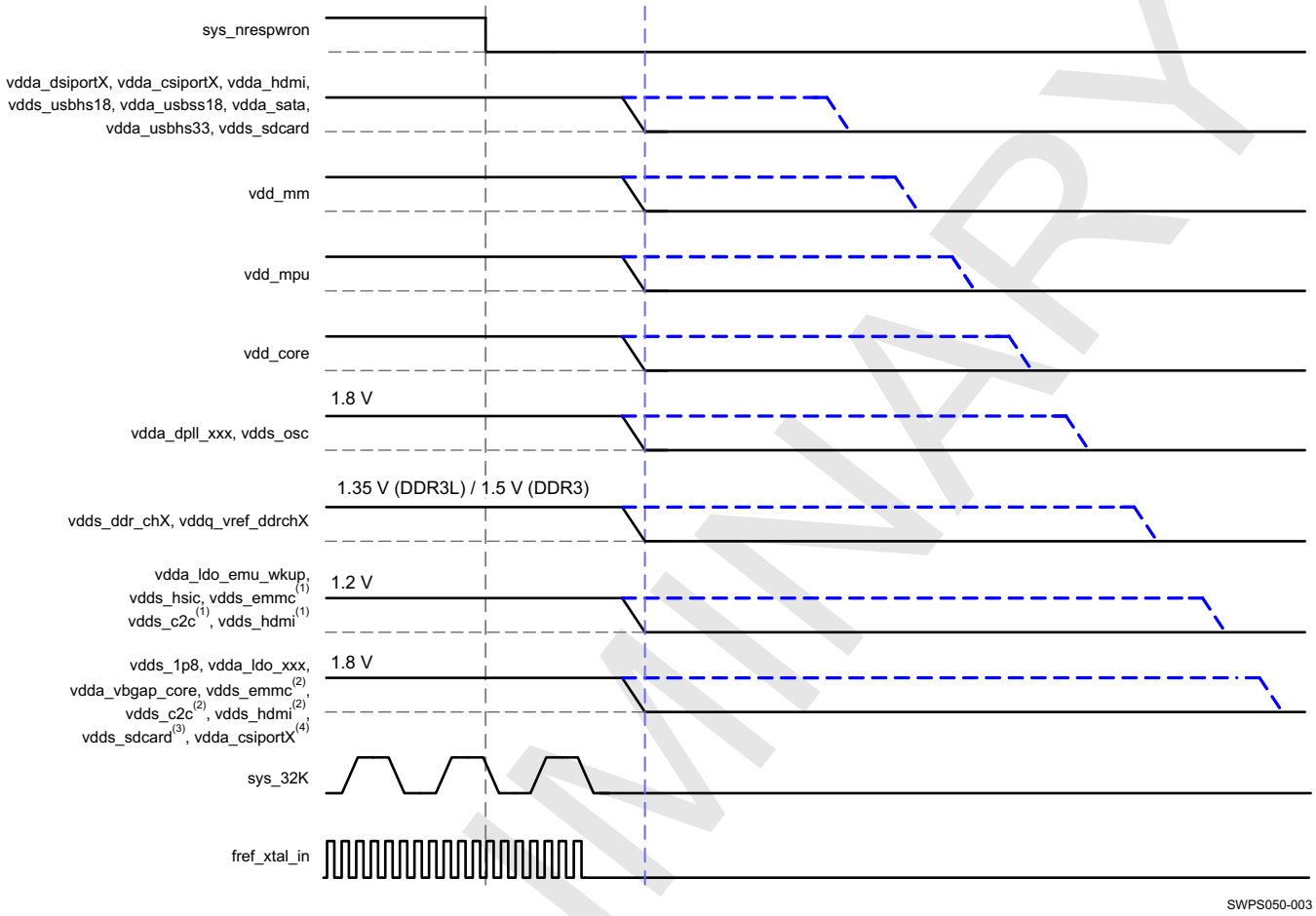


Figure 3-3. Power-Down Sequence

(1) In case the corresponding interfaces are used at 1.2 V.

(2) In case the corresponding interfaces are used at 1.8 V.

(3) In case the SDCARD interface is used at 1.8 V only (function different from Muxmode 0).

(4) In case the MIPI CSI-2 interface is used as GPIO or CPI (function different from Muxmode 0).

NOTE

sys_32k can be turned off any time after sys_nrespwron assertion and before vdds_1p8 shutdown.

The fref_xtal_in clock can be turned off any time after sys_nrespwron assertion and before the system clock IOs voltage supplies shutdown (vdds_osc).

4 Clock Specifications

The system clock specifications described in the OMAP5430 data manual are applied to the OMAP5432 with the following exceptions:

- The slicer input clock, the system clock request 1 and 2, and the output system clock 2 and 3 functionalities are not available in the OMAP5432 device.

NOTE

For more information on the Clock Specifications, see the OMAP5430 data manual.

5 Timing Requirements and Switching Characteristics

NOTE

The OPP (operating performance point) described in this chapter correspond to the OPP of the core domain. The operating point for MPU and multimedia are not described in this section. For more information, see the DM Operating Condition addendum.

5.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions, unless otherwise specified.

5.2 Interface Clock Specifications

5.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

5.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

5.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology will be used to identify this type of jitter.

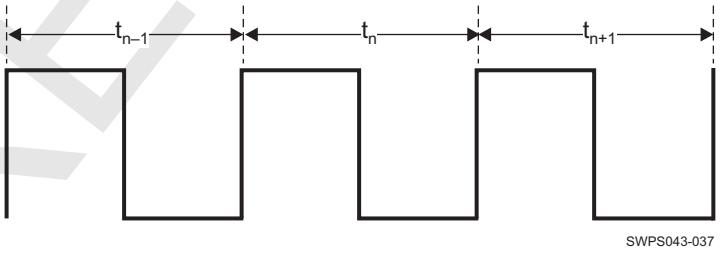


Figure 5-1. Cycle (or Period) Jitter

Jitter values are defined as follows:

- Ideal clock period = t_p
- Maximum Cycle/Period Jitter = Max ($|t_i - t_p|$), with i = n – 1, n, n + 1, …
- Minimum Cycle/Period Jitter = Min ($|t_i - t_p|$)
- Jitter Standard Deviation (or RMS Jitter) = Standard Deviation ($|t_i - t_p|$)

Unless otherwise specified, the jitter probability density can be approximated by a Gaussian function and peak-to-peak jitter is defined over a ±7 sigma distribution of this function.

5.2.4 Clock Duty Cycle Error

The maximum duty cycle error is the difference between the absolute value of the maximum high-level pulse duration or the maximum low-level pulse duration and the typical pulse duration value:

- Maximum pulse duration = typical pulse duration + maximum duty cycle error
- Minimum pulse duration = typical pulse duration – maximum duty cycle error

In this document, the clock duty cycle can be documented as maximum pulse duration or as maximum duty cycle error. In this case, you can consider:

- Maximum duty cycle error = maximum [(maximum pulse duration – typical pulse duration) or (typical pulse duration – minimum pulse duration)]

5.3 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

Table 5-1. Timing Parameters

SUBSCRIPTS	
SYMBOL	**PARAMETER**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or do not care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

NOTE

The OPP (operating performance point) described in this chapter correspond to the OPP of the core domain. The operating point for MPU and multimedia are not described in this section. For more information, see the DM Operating Condition addendum.

5.4 External Memory Interface

The OMAP5432 includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- External memory interface controller (EMIF)

5.4.1 General-Purpose Memory Controller (GPMC)

NOTE

For more information, see the OMAP5430 data manual.

5.4.2 External Memory Interface (EMIF)

NOTE

For more information, see the EMIF Controller section of the OMAP543x TRM.

The SDRAM controller subsystem module provides connectivity between the processor and external DRAM memory components.

The module includes support for double-data-rate SDRAM (mobile DDR).

DDR3 module embedded in the OMAP5432 is compliant with the JESD79-3D standard.

For more information on the DDR3 timing requirements and switching characteristics, see the JESD79-3D standard.

NOTE

EMIF I/O (DDR) does support 1.5 V.

5.5 Multimedia Interfaces

5.5.1 Camera Interface

NOTE

For more information, see the OMAP5430 data manual.

5.5.2 Display Interface

NOTE

For more information, see the OMAP5430 data manual.

5.6 Serial and Parallel Communication Interfaces

5.6.1 Multichannel Buffered Serial Port (McBSP)

NOTE

For more information, see the OMAP5430 data manual.

5.6.2 Multichannel Audio Serial Port (McASP)

NOTE

For more information, see the OMAP5430 data manual.

5.6.3 Multichannel Serial Port Interface (McSPI)

NOTE

For more information, see the OMAP5430 data manual.

5.6.4 Digital Microphone (DMIC)

NOTE

For more information, see the OMAP5430 data manual.

5.6.5 Multichannel Pulse Density Modulation (McPDM)

NOTE

For more information, see the OMAP5430 data manual.

5.6.6 High-Speed Synchronous Interface (HSI)

NOTE

The HSI1 interface is not available in the OMAP5432 device. For more information, see the OMAP543x TRM.

NOTE

For more information, see the OMAP5430 data manual.

5.6.7 Universal Serial Bus (USB)

NOTE

The following interfaces are not available in the OMAP5432 device:

- USB (Port D0) – ULPI 8-bit
- USB (Port B1) – HSIC1
- USB (Port B2) – ULPI 8-bit
- USB (Port B2) – Full Speed / Low Speed

For more information, see the OMAP543x TRM.

NOTE

For more information, see the OMAP5430 data manual.

5.6.8 Inter-Integrated Circuit Interface (I^2C)

NOTE

For more information, see the OMAP5430 data manual.

5.6.9 HDQ / 1-Wire Interface (HDQ/1-Wire)

NOTE

For more information, see the OMAP5430 data manual.

5.6.10 Universal Asynchronous Receiver Transmitter (UART)

NOTE

The UART4 and UART6 interfaces are not available in the OMAP5432 device. For more information, see the OMAP543x TRM.

NOTE

For more information, see the OMAP5430 data manual.

5.6.11 Serial Advanced Technology Attachment (SATA), 1.8 V

NOTE

For more information, see the OMAP5430 data manual.

5.6.12 MMC2—eMMC

NOTE

For more information, see the OMAP5430 data manual.

5.6.13 MMC3—WLAN Secure Digital Input / Output Interface (WLSDIO)

NOTE

For more information, see the OMAP5430 data manual.

5.6.14 MMC4 and MMC5—Secure Digital Input / Output Interface (SDIO)

NOTE

The SDIO5 interface is not available in the OMAP5432 device. For more information, see the OMAP543x TRM.

NOTE

For more information, see the OMAP5430 data manual.

5.7 Removable Media Interfaces

5.7.1 MMC1—SD Card Interface

NOTE

For more information, see the OMAP5430 data manual.

5.8 Test Interfaces

NOTE

For more information, see the OMAP5430 data manual.

6 Thermal Management

For reliability and operability concerns, the maximum junction temperature of OMAP5432 has to be at or below the T_J value identified in Table 3-3, *Recommended Operating Conditions*.

Depending on the thermal mechanical design and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level with the power worst use case.

Based on the results, if the temperature limits are exceeded, an OMAP level software thermal policy must be set up; for detailed information, see the *OMAP5432 Thermal Management* application note.

The OMAP level thermal policy relies on a PCB sensor. Therefore, it is recommended to have such sensors located on the PCB; for more information, see Section 6.2.1, *PCB Temperature Sensor*. In addition, it is recommended to avoid having another significant thermal source near the OMAP5432.

The risks of not managing this junction temperature are hazardous heating, power supply clamping, reliability issues, and malfunction.

6.1 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1. Thermal Resistance Characteristics

PACKAGE	POWER (W)	θ_{JA} (°C/W)(2)	Ψ_{JB} (°C/W)(3)	T_J (°C)(4)	BOARD TYPE
OMAP5432 ES2.0	4	16	5.5	107	2S2P(1)

(1) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

(2) Θ_{JA} (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W.

(3) Ψ_{JB} (Psi-JB) = Pseudo Resistance Junction-to-Board, °C/W derived from thermal simulation following JEDEC reference (JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

(4) $T_J = P \times \Psi_{JB} + T_B$, T_J is the junction temperature and T_B is the board temperature (85ºC).

CAUTION

Ψ_{JB} (Psi-JB) value could vary, depending on the board (PCB) and the device power distribution related to the power use case: 5.5ºC/W is given for a 4-W dissipated power.

6.2 Temperature Sensor Recommendation

6.2.1 PCB Temperature Sensor

To manage the OMAP5432 junction temperature, an external PCB temperature sensor is required in addition to the internal OMAP5432 thermal sensor. The accuracy of the temperature sensor is critical to optimize the OMAP performance; the minimum recommended accuracy is ±2ºC; see the TI TMP102 temperature sensor component. The temperature sensor can be located at one position to correctly monitor the OMAP5432 junction temperature:

- OMAP north side, 1 mm from package on same PCB side than OMAP.

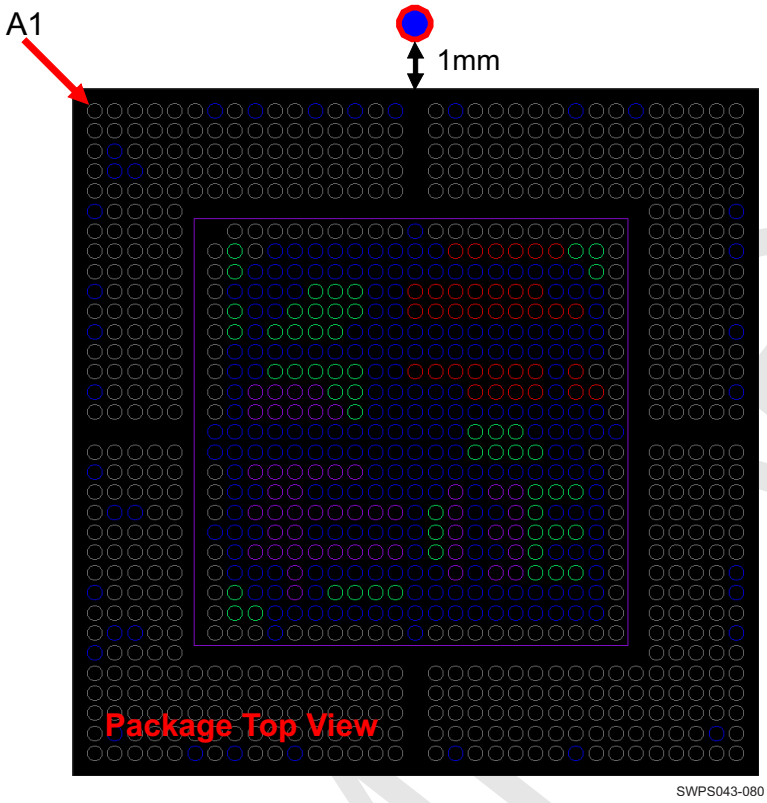


Figure 6-1. PCB Temperature Sensor Recommendation (Package Top View)

7 Package Characteristics

7.1 Device Nomenclature

7.1.1 Standard Package Symbolization

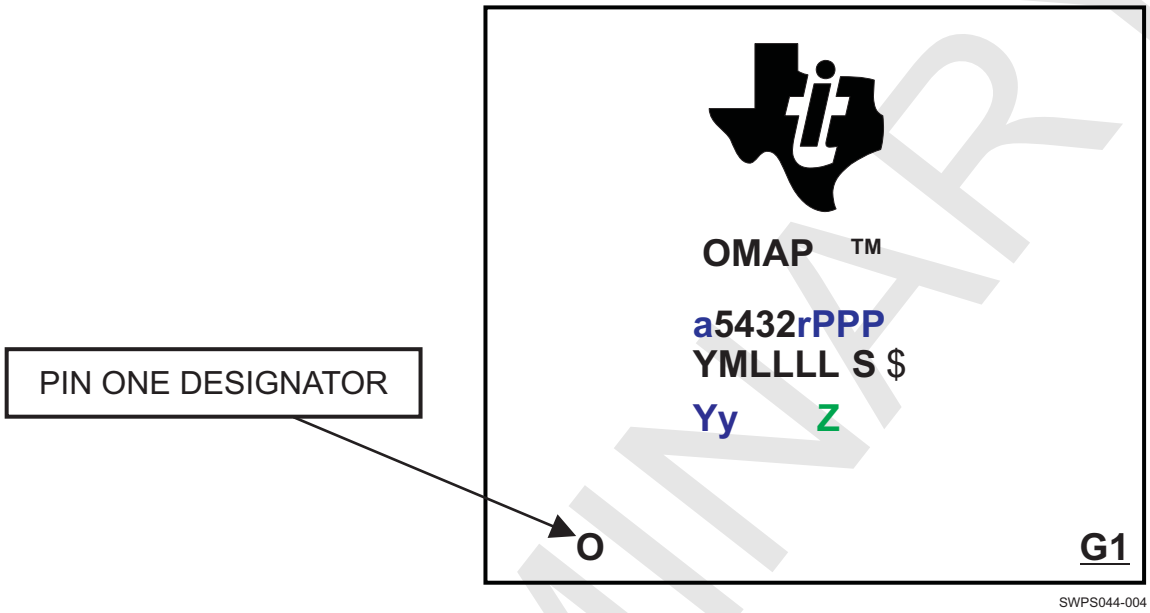


Figure 7-1. Printed Device Reference

NOTE

Black: Static field

Blue: Variable field coded with letters and/or numbers

Green: Variable fields coded with numbers

The letters and numbers fields are interleaved to facilitate the reading of the parameters.

During the prototyping phase, a generic symbolization can be applied for flexibility reasons (see Figure 7-2). TI will ensure the right fuse content and test program usage by part number.

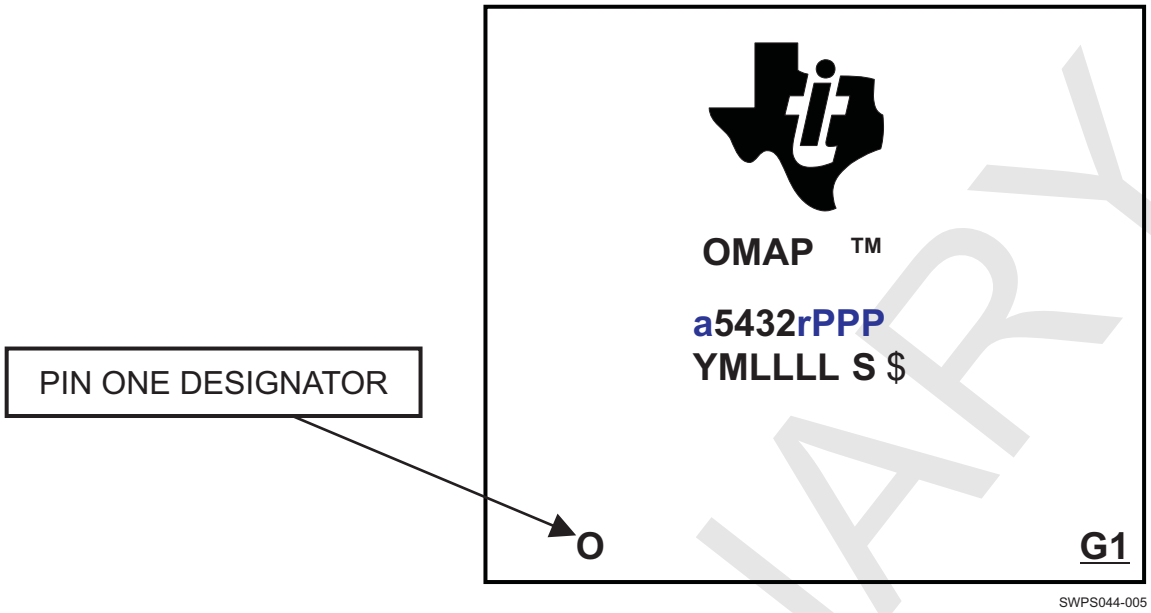


Figure 7-2. Prototype Device Reference

NOTE

Black: Static field

Blue: Variable field coded with letters and/or numbers

The letters and numbers fields are interleaved to facilitate the parameters reading.

7.1.2 SAP Part Number

The actual part number used in the system follows this syntax (SAP allows a maximum of 14 characters):

- SAP part number in Tray: a**5432**rZFYyPPP
- SAP part number in Tape and Reel: a**5430**rZFYyPPP**R**

7.1.3 Device Naming Convention

Table 7-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage(1)	X	X for TMX (prototypes)
		P	P for TMP (preproduction, production not yet qualified
		BLANK	blank for TMV (qualified production) blank when qualified
r	Device revision	BLANK	ES1.0
		A	ES2.0
PPP	Package designator	AAN	AAN S-PBGA-N754 (Prototype and Production)
F	Reserved	XX	Reserved
Yy	Device type	GP	General purpose (Prototype and Production)
		XX	Reserved
Z	Device Speed	BLANK or 0	OMAP5432 standard speed grade
		1, 2, …	OMAP5432 alternate speed grade
YM	Lot Trace Code (LTC): Y = Year, M = Month		
LLLL	Lot Trace Code (LTC): Assembly lot number		

Table 7-1. Nomenclature Description (continued)

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
S	Reserved		
$	Reserved		
O	Pin one designator		
G1	ECAT—Green package designator		

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Nonqualified / production devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

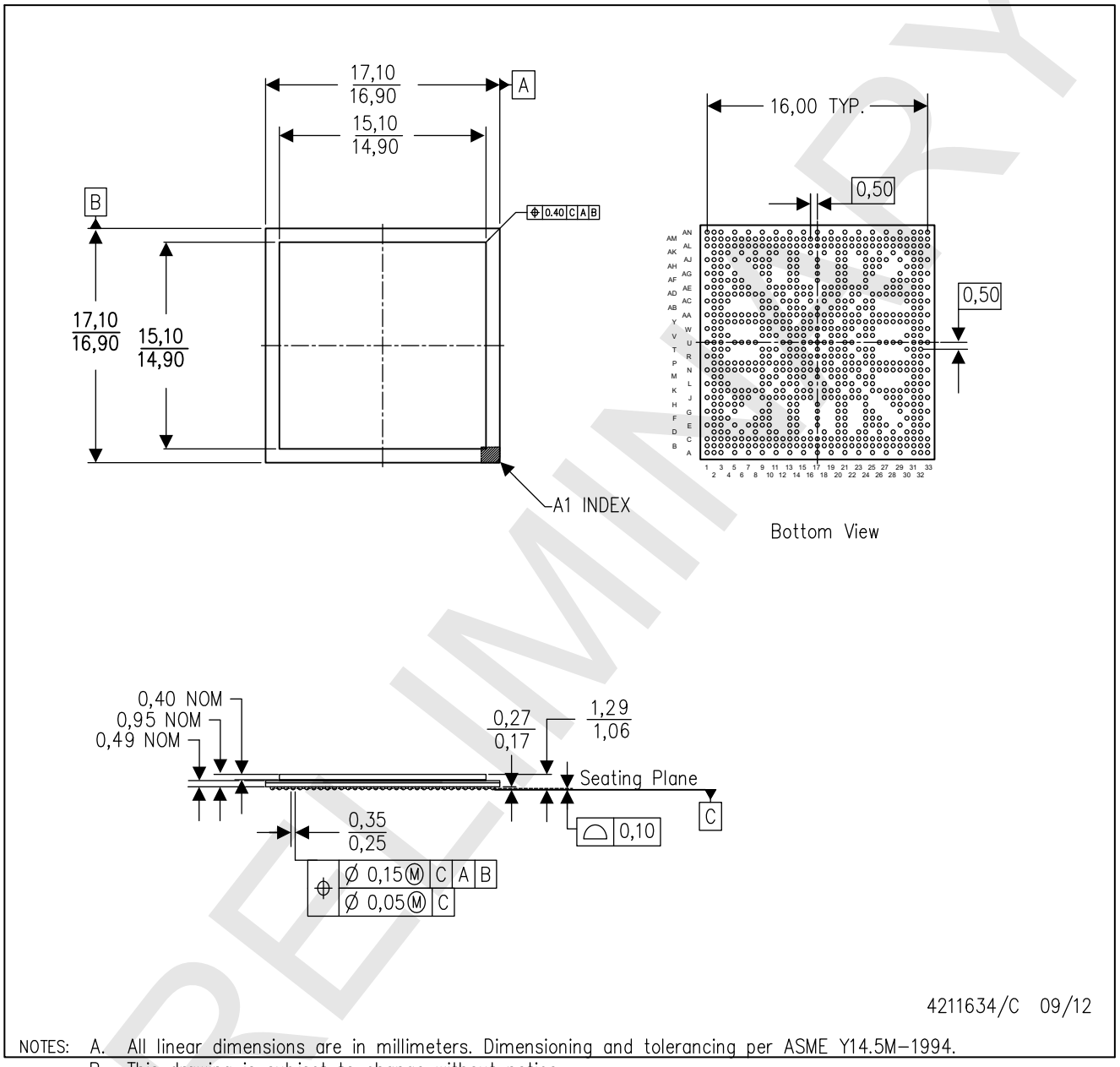
(2) The fabrication flow code will include the silicon fabrication site and / or assembly site and / or test site.

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

7.2 Mechanical Data

AAN (S–PBGA–N754) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

SWPS050-001

Figure 7-3. Mechanical Package

8 PCB Guidelines

NOTE

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this chapter are intended as guidelines only.

NOTE

These PCB guidelines are in a draft maturity and consequently, are subject to change depending on the verification steps during the IC development.

NOTE

Any references to OMAP5432 ballout or pin multiplexing are subject to change following the OMAP5432 ballout maturity.

8.1 Introduction

The OMAP5432 PCB guidelines chapter is to be considered with the *OMAP5430 Processor Multimedia Device PCB Guidelines* of the OMAP5430 data manual. Most of the guidelines needed to develop a platform based on the OMAP5432 device are embedded in the OMAP5430 PCB Guidelines chapter. The OMAP5432 PCB guidelines chapter has additional information that complements the OMAP5430 PCB Guidelines to cover the OMAP5432 device specifically.

The OMAP5432 PCB guidelines are presented through three main topics:

- PCB stackup proposal

  The OMAP5432 pitch and ballout enable implementing OMAP5432-based platform using PCB in plated through holes (PTH) technology. This permits minimizing costs associated to PCB but induces additional routing constraints.
- DDR3

  EMIF is addressed through DDR3 on the OMAP5432 device. This is main difference between the OMAP5430 and OMAP5432 devices. As a consequence, DDR3 will be the major topic addressed in this document.
- Power integrity

  Due to a different package, ballout, and possibly PCB stackup, the OMAP5432-based platform differs from the OMAP5430-based platform. Power integrity is greatly dependant on hardware implementation, which updates the power integrity analysis for the main supply domains: VDD_Core, VDDMPU, VDD_MM, and Vddq.

8.2 DDR3

8.2.1 Introduction

The OMAP5432 device has two 32-bit-wide DDR3 channels running at a clock frequency of 533 MHz. The device supports both 1.5-V (DDR3) and 1.35-V (DDR3L) voltage operation. Because the bus width is 32 bits, it is not compatible with DDR3 UB DIMM. Primarily, the OMAP5432 device is intended to use the on-board DDR3 memories. The DDR3 standard supports up to 1066 MHz, the operating frequency is limited to 533 MHz in the OMAP5432 context.

The OMAP5432 pitch and ballout have been defined to enable platform design with HDI and PTH PCB technologies. PTH technology permits minimizing costs associated to the PCB but induces additional routing constraints.

In this section, the principle of the DDR3 memory interface and the PCB design method are described for these two different PCB types (6L PTH and 1-4-1 HDI).

8.2.2 DDR3 Memory Configuration

According to the JEDEC Standard, DDR3 is specified as three different bus types: x4 (78-ball FBGA), x8 (78-ball FBGA), and x16 (96-ball FBGA). Because the OMAP5432 device does not support x4, either x8 or x16 are used. Different from LPDDR2, two or four DDR3 channels are used to build the 32-bit memory bus.

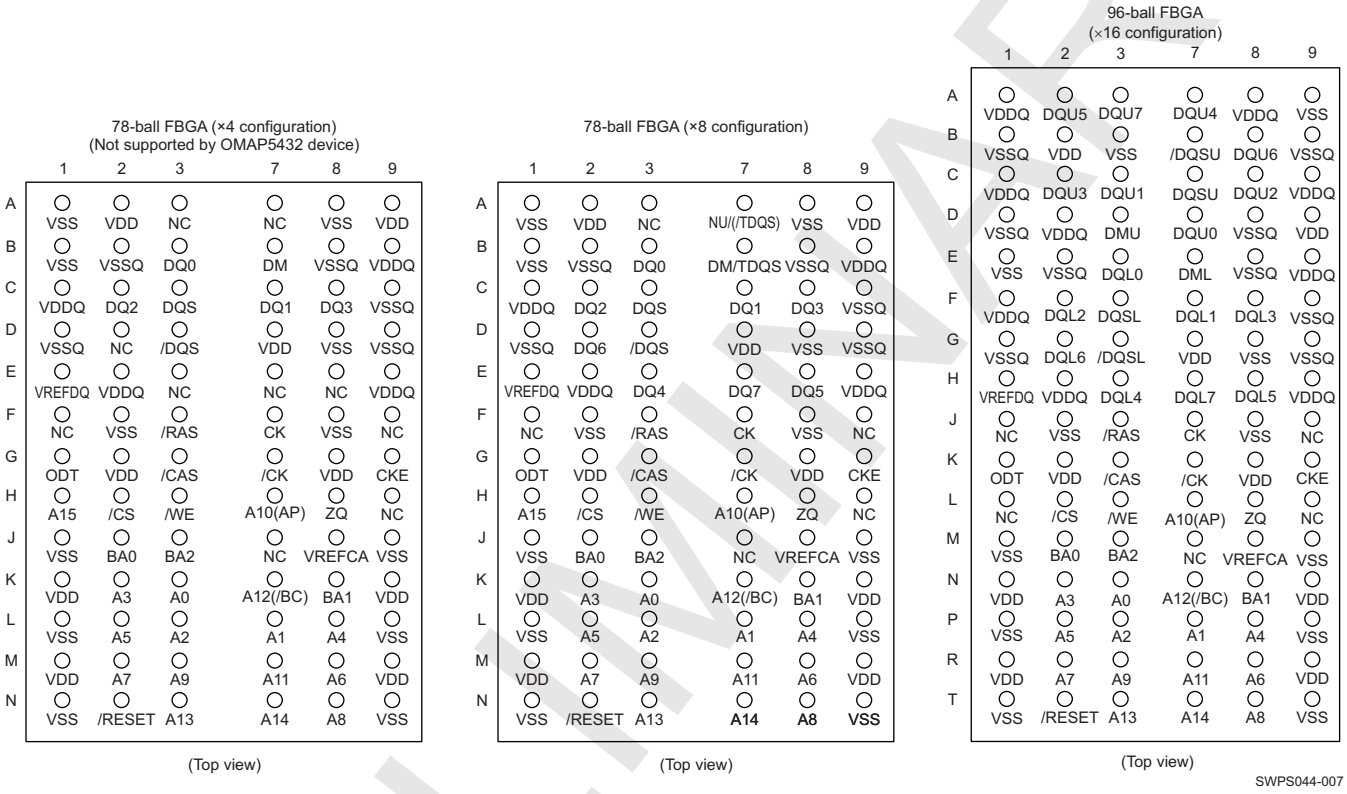


Figure 8-1. DDR3 Memory Ballout

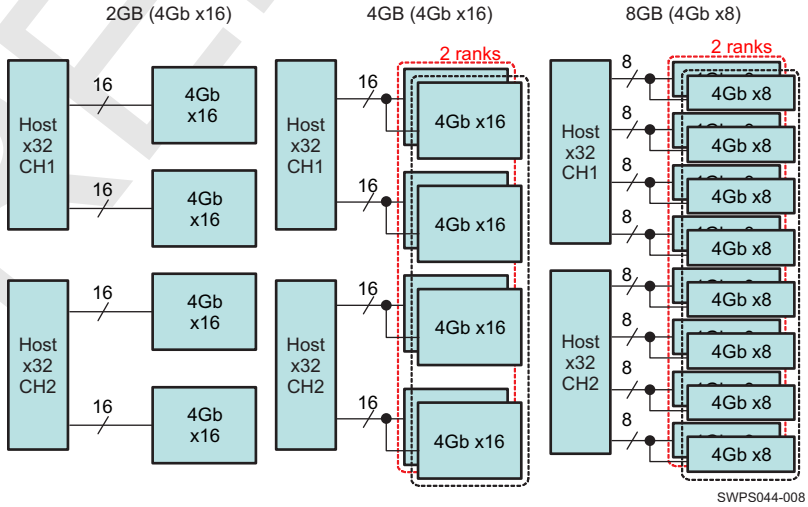


Figure 8-2. DDR3 Memory Configuration for 2GB, 4GB, and 8GB Memory Density

The OMAP5432 supports up to two chip selects by the EMIF channel/controller; therefore, the maximum system memory density is 8GB with a DDR3 die density of 4Gbit or 8Gbit (see Table 8-1). As shown in Figure 8-1, a CS line actually selects multiple memories; therefore, in the PC memory world, they are called ranks. Address and command lines are not written on Figure 8-2, they are connected in parallel to all memories.

Table 8-1. System Memory Density by Memory Type(1)

DDR3 DIE DENSITY	RANK	x16	x8
1 Gbit	1 rank	0.5GB	1GB
	2 rank	1GB	2GB
2 Gbit	1 rank	1GB	2GB
	2 rank	2GB	4GB
4 Gbit	1 rank	2GB	4GB
	2 rank	4GB	8GB
8 Gbit	1 rank	4GB	8GB
	2 rank	8GB	16GB

(1) 16GB is not supported by OMAP5432.

Table 8-1 shows a summary of system memory density (for two EMIF channels) that is configurable by each DDR3 type.

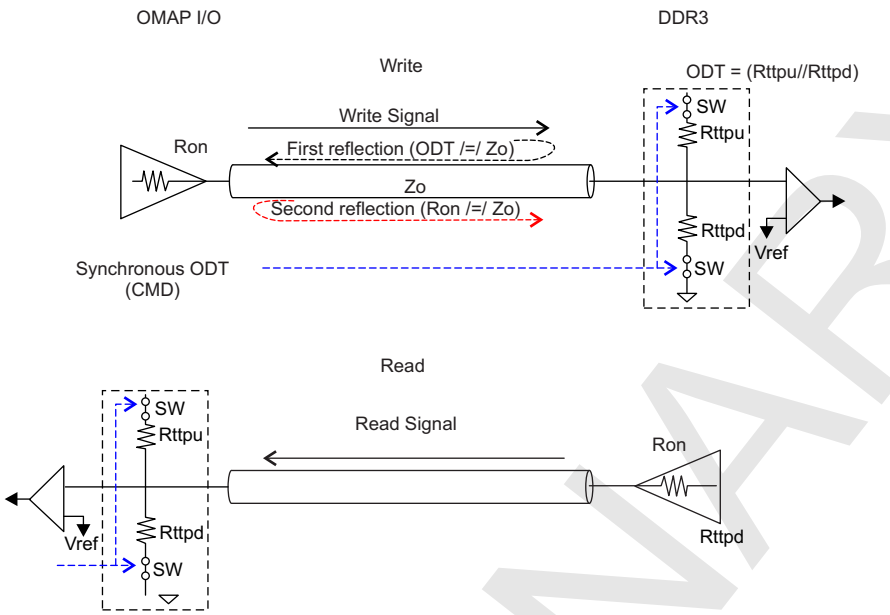
Note that 1Gbit and 2Gbit die memories are in production now, and memory vendors are sampling 4Gbit. 8Gbit die memory is not yet available.

It is possible to configure the same memory density with x16 two ranks or x8 one rank. However, 4* x8 power consumption is much higher than 2* x16; therefore, x16 two ranks are preferable. Also, the PCB foot-print is smaller.

To facilitate PCB routing, the second rank may be placed on the bottom side of the PCB.

In case the double side population is not possible (for example, by limitation of the PCB height) the DDP package may be used. The DDP package is the die-stacked package, called the dual-density package. Two die data and command addresses are connected in parallel in the package, it is useful to make two ranks memory system by the single side population.

8.2.2.1 DDR3 IO and Termination



OMAP5432 I/O	Drive strength (Ron) in Ω	I[2:0] = 000	80
		I[2:0] = 001	60
		I[2:0] = 010	48
		I[2:0] = 011	40
		I[2:0] = 100	34
	ODT in Ω	odt[1:0] = 00	OFF
		odt[1:0] = 01	60
		odt[1:0] = 10	80
		odt[1:0] = 11	120
DDR3 memory	Drive strength (Ron) in Ω	bit[1:0] = 00	40
		bit[1:0] = 01	34
	ODT in Ω	bit[2:0] = 001	60
		bit[2:0] = 010	120
		bit[2:0] = 011	40
		bit[2:0] = 100	20
		bit[2:0] = 101	30

ODT = Rttpu//pd

SWPS044-009

Figure 8-3. DDR3 Data Transmission Model

For high-speed data transmission, the PCB line impedance must be controlled, and the on-die termination may be applied. It depends on PCB stack-up, either Microstrip or strip-line is used. Usually a 40- to 50-Ω characteristic impedance (Z_O) is used.

As indicated on Figure 8-3, the drive impedance and the termination are programmable. To minimize the reflection, a termination equal to Z_O may be used. It may be adjusted to a higher value (for example, 60 Ω, 80 Ω, or 120 Ω) to reduce the power consumption.

8.2.2.2 Source Matching Concept

It is possible to choose the characteristic impedance equal to the drive impedance and to remove the termination. In this case, the signal is reflected at the receiver; however, the reflection signal is absorbed at the driver. It depends on the length and crosstalk of the lines; degradation of the signal may be acceptable.

To reduce the crosstalk and to make 34- to 40-Ω impedance, the HDI PCB may be used. Note that the drive impedance changes 15% and the PCB impedance changes 20%. It is important to verify the design at the corner.

8.2.2.3 Termination Power

When ODT is enabled, the power dissipation is increased. With the ODT control signal, termination is enabled only when the data burst occurs. Therefore, the termination power is proportional to the usage of bus. That is, it is proportional to the data rate.

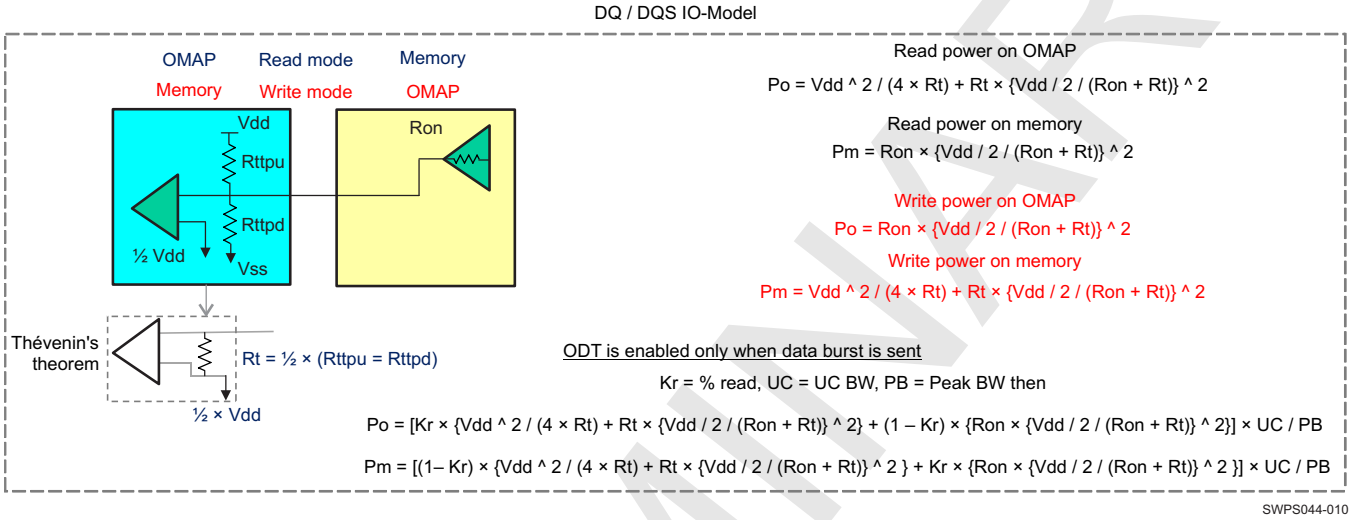


Figure 8-4. Data IO Model

Figure 8-4 shows how termination power is calculated. When OMAP writes to the memory, the termination occurs at the memory side, the direction is reversed by a read. Figure 8-4 shows power consumption per bit and it is necessary to multiply by the number of bits. One data byte is consisted by 11-bit line, so the termination power of the entire 8 bytes is 88 times the value.

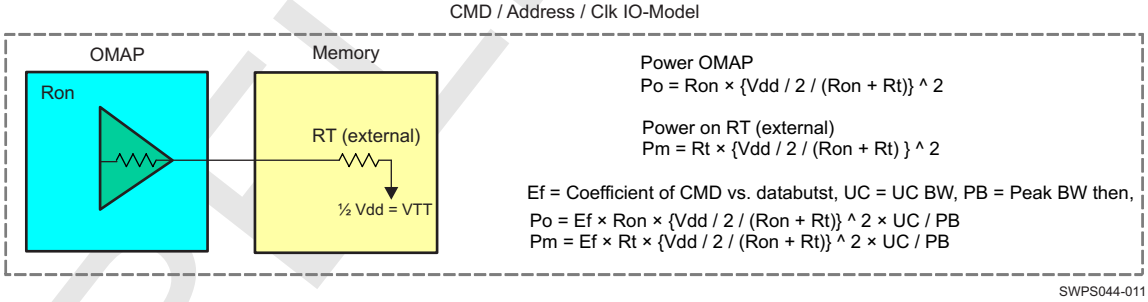


Figure 8-5. Termination Power on the Command-Address Bit

There is no ODT on the command-address (CA) bit. If a fly-by connection is selected, termination resisters are added to the PCB and the VTT (= Vref) regulator is used. If the T-branch connection is used, the CA termination could be eliminated.

8.2.2.4 T-Branch and Fly-by Topologies

As described in Table 8-1, multiple DDR3 memories are connected to construct the 32-bit data bus. The CA signals are common to all memories. It is possible to use the T-branch topology up to 2 x16 DDR3 (maximum of 4 memories with 2 ranks). The CA termination may be eliminated.

If the x8 DDR3 is used, a maximum of 8 memories are connected to a CA bus. In this case the fly-by topology must be used.

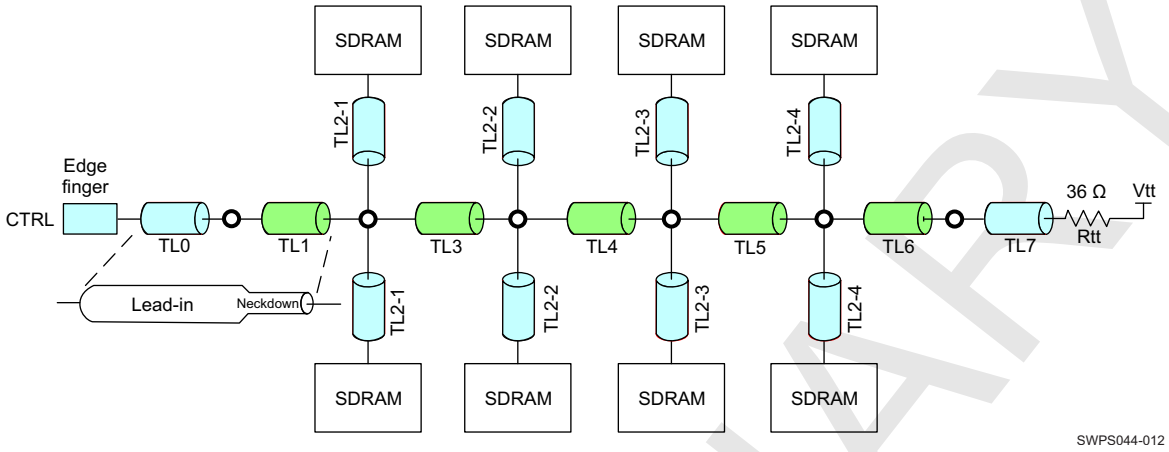


Figure 8-6. Fly-by Topology

With fly-by topology, multiple memories are connected to the single transmission line and the line is terminated at the end. Because each memory is driven by different timing, it is possible to reduce the impact of the capacitive loads.

The OMAP5432 memory controller supports write leveling, therefore we can use the fly-by topology. However, if the x16 device is used, only two memories are connected to the channel. In this case T-branch topology is recommended.

The OMAP5432 CA balls are located between the data bytes. The T-branch CA bus can be placed between the two memories.

The OMAP5432 ballout is optimized for x16 DDR3 device so that the data bits are connected straight in one layer.

Rank_0 memories are placed on the top of the PCB and the Rank_1 memories are placed on the bottom of the PCB.

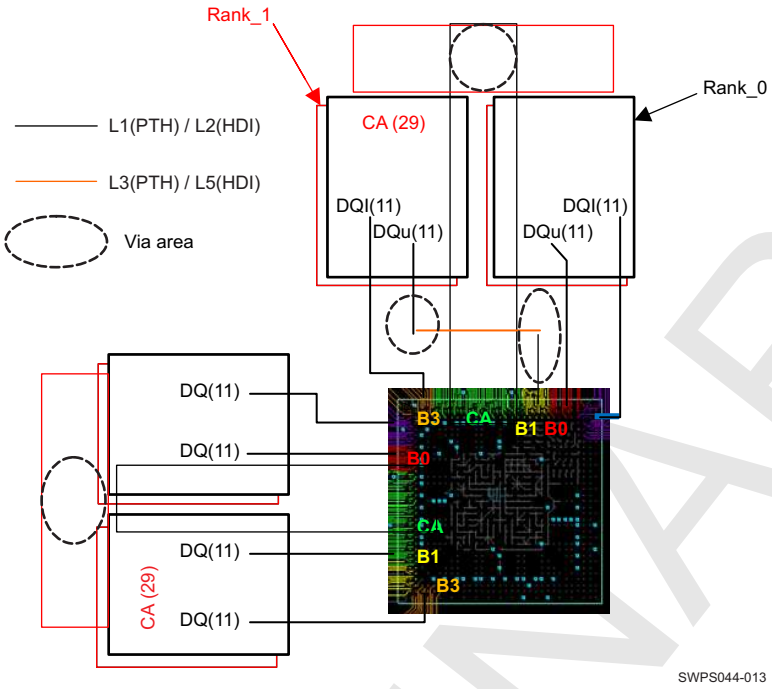


Figure 8-7. Floor Plan for the x16 DDR3 (T-Branch)

Figure 8-8 shows the floor plan for the x8 DDR3 using the fly-by topology. As the CA balls are located between the data bytes, it is necessary to cross the data lines. The 78BGA package is almost as large as the 96BGA package. A total of eight memories are connected per channel, the length of data lines becomes much longer than x16.

Considering the footprint of the memories, the x16 with T-branch topology has been selected for the reference board.

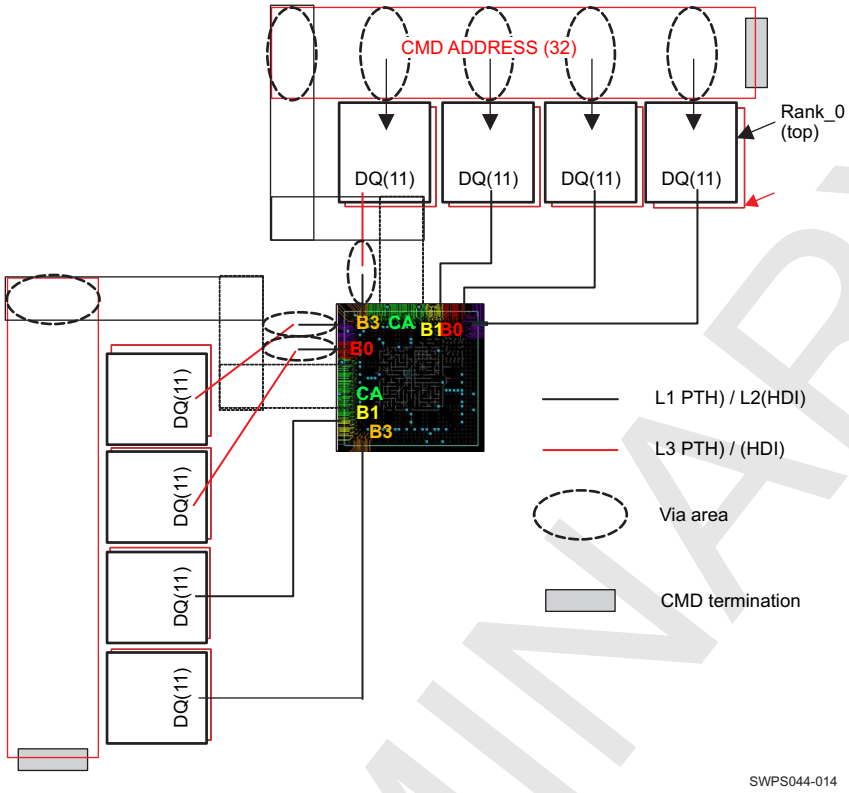


Figure 8-8. Floor Plan for x8 DDR3 (Fly-by Topology)

8.2.3 PCB Stack Up Options

The OMAP5432 ball assignment is optimized for the ×16 T-branch connection. The balls in the first row are partially depopulated so that the outer three rows can be routed by the single layer. All DDR3 signals are assigned there.

The balls in rows 4, 5, 6, 7, and 8 are routed through the vias located in the via channel array (VCA). Because of the VCA, we can use a conventional 6L PTH PCB for the OMAP5432 device.

It is also possible to use 1-4-1 HDI PCB. For the HDI PCB, L1 can be the GND plane. The DDR3 signals are routed by the L2 that works as a shielded strip-line. It is possible to attain the lower characteristic impedance and therefore source matching may be applied.

It is also possible to connect the power planes to the core balls through VCA. The power plane is not disconnected by the signal vias.

8.2.3.1 PTH PCB

Figure 8-9 shows the 6L PTH stack up. Via size can be up to 0.25 mm with a 0.45-mm annular ring. To escape 0.5 BGA, trace width and space must be 75/75 µm.

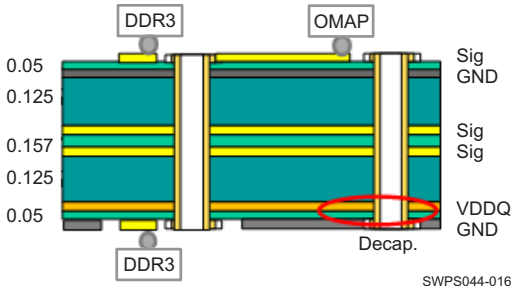


Figure 8-9. 6L PTH Stack up

If needed because of a manufacturing reason, we could use the 75/75 bottleneck and relax the rest of the design to 100/100 (see Figure 8-10).

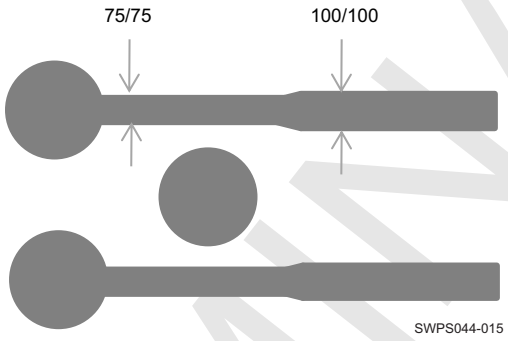


Figure 8-10. 75/75u Bottleneck

The signals are primarily in layer 1. Layer 6 is used for bit mirroring of the rank 1 memories. Layer 3 or 6 is used for crossing the signals. Layer 4 is reserved for other signals.

The GND plane and the 75-µm wide-line form a 51-Ω Microstrip line. Note that the GND plane is the return path of the signals. Therefore, the GND plane must always present under the signal line.

Layer 5 is used by the VDD plane. The line in layer 6 also works as Microstrip line. It is used for mirroring the rank 1 signals. Except the area of the L6 signal, it is recommended to cover layer 6 by GND as much as possible.

The L6 GND and the L5 VDD form a distributed decoupling capacitor.

8.2.3.2 1-4-1 HDI PCB

In the stack up, the DDR3 signals are primary routed on layer 2, and layer 6 is used for mirroring rank 1 signals. It is possible to use layer 4 for data crossing. Layer 3 is the VDD plane. A distributed decoupling capacitor is made between layer 3 and layer 5. Except around the IC, the components, and some critical nets, layer 1 and layer 6 must be the GND planes. It is useful to control EMC, and to reduce the cross-talk.

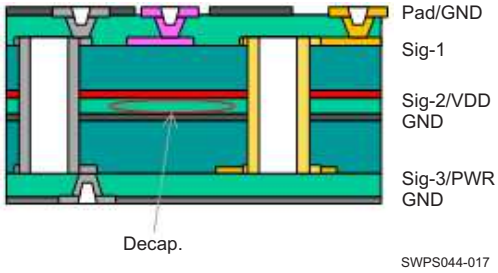


Figure 8-11. 1-4-1 HDI Stack up

8.2.4 PTH PCB Layout

8.2.4.1 Floor Plan

High-level floor plan based on the x16 DDR3 has been presented in Figure 8-7.

The CA bus is routed between the two DDR3 memories. Recommended trace/space is 75µ/150µ except for the BGA/decoupling capacitors escape area.

4 × 1.5-V decoupling capacitors and a 2x Vref decoupling capacitor must be placed as close as possible to the OMAP device.

The channel 2 floor plan is almost identical, except for the B1 byte. Because the CA is located within the two data bytes, CA and data are connected straightly.

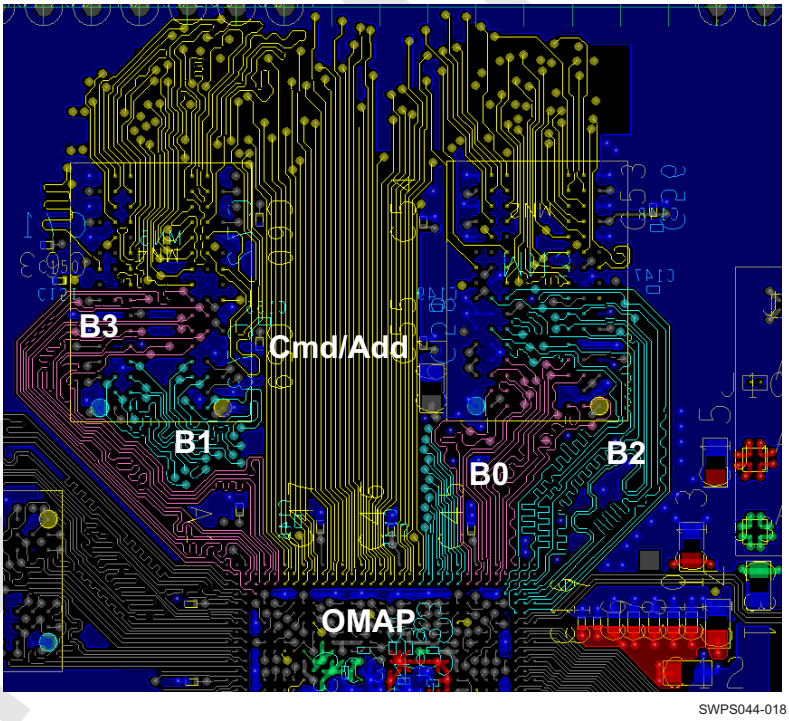


Figure 8-12. Channel 1 Test Layout (L1)

8.2.4.2 DQ Signal Routing

Minimum line spacing of 75 µm can be used for BGA escape and in the fan out area, as indicated on Figure 8-13. The total sum line length of 75 µm must be limited within 5 mm. Otherwise, line to line spacing must be greater than 2× the dielectric thickness (data to data) and 3× (data to strobe). In this stack up a 50-µm dielectric thickness is used.

DQS/nDQS to DQ/DM minimum spacing must be 150 µm. DQ/DM to DQ/DM minimum spacing must be 100 µm. The spacing between DQS and nDQS impacts the differential impedance; therefore, it must be kept constant at 100 µm.

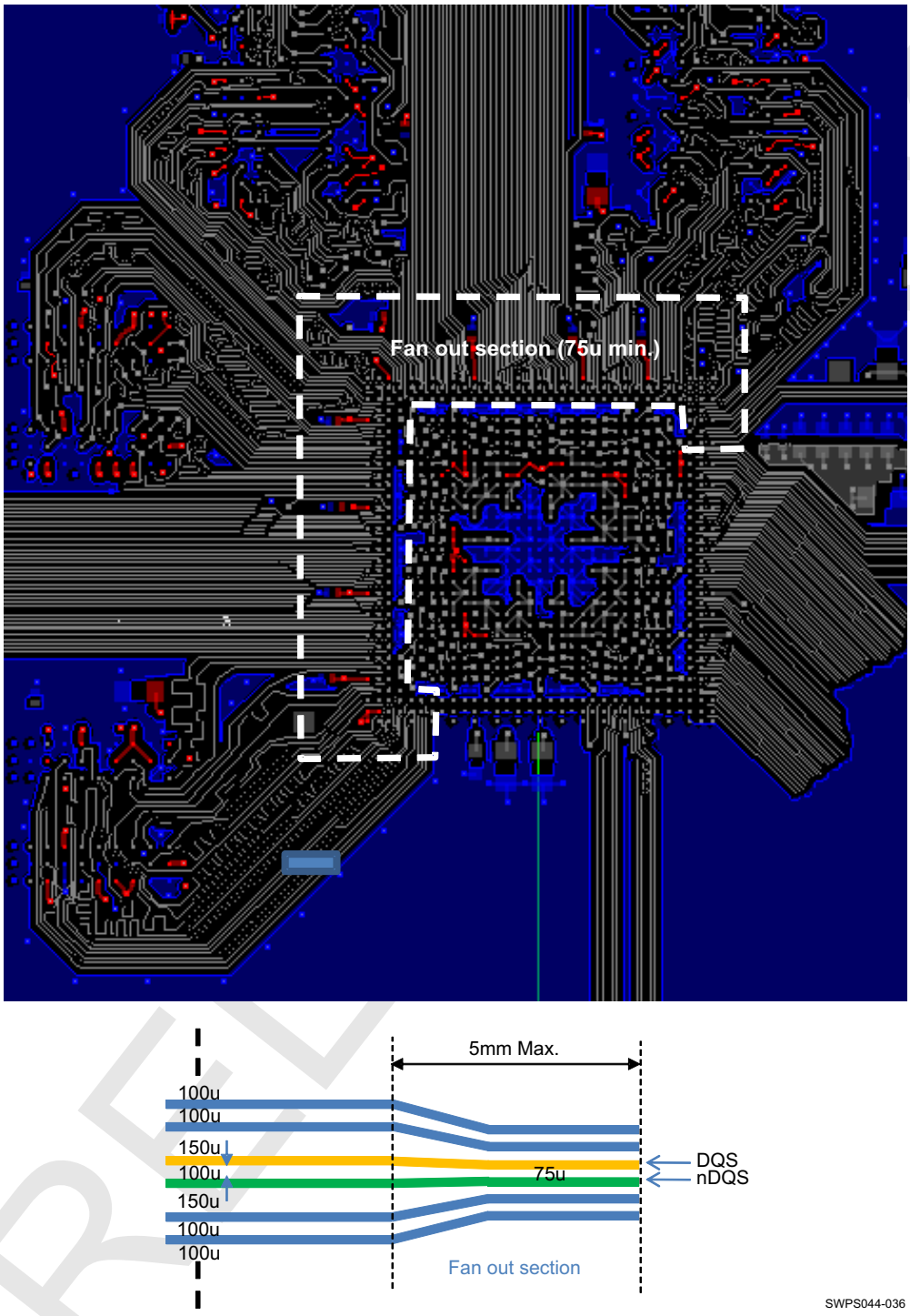


Figure 8-13. Line to Line Space (Edge to Edge)

Within the byte and the rank, the data signal length must be matched within ±0.5 mm. For routing to the rank 1 memories (bottom side) a PTH via is placed as close as possible to the DDR3 memory and routed to the bottom memories by L6. Signals are mirrored by the L6 traces. To facilitate layout of the bottom memories, DQ bits could be swapped as listed in Table 8-2. The DQS, nDQS, DM, and DQ0, 8, 16, and 24 must not be swapped

Table 8-2. DQ Bit-swap

Rank0	Rank1	Rank0	Rank1
DQU0	DQU0	DQL0	DQL0
DQU1	DQU1	DQL1	DQL1
DQU2	DQU3	DQL2	DQL3
DQU3	DQU2	DQL3	DQL2
DQU4	DQU7	DQL4	DQL7
DQU5	DQU6	DQL5	DQL6
DQU6	DQU5	DQL6	DQL5
DQU7	DQU4	DQL7	DQL4
DQSU	DQSU	DQSL	DQSL
nDQSU	nDQSU	nDQSL	nDQSL
DMU	DMU	DML	DML

In case the multiple layers are used within the same byte, it must be considered that the signal velocity is different from layer to layer. In this case static skew of data signals must be controlled within ±10 ps from the strove (DQS/nDQS).

8.2.4.3 Byte 1 (DQ08-15) Crossing

The channel 1 byte 1 signals need to cross the CA bus, if possible layer 6 should be used. Note that signal velocity of layer 1 and layer 6 is same. If other layers are used, careful skew control is needed. The vias must be located within 5 mm from the nearest decoupling capacitor. This is to connect the layer 5 plane and layer 2 plane to provide return paths. If both layers 2 and 5 are assigned to GND, the decoupling capacitor can be replaced by the vias connecting the both planes. The signal vias must be placed in distance so that the plane is connected in between the vias.

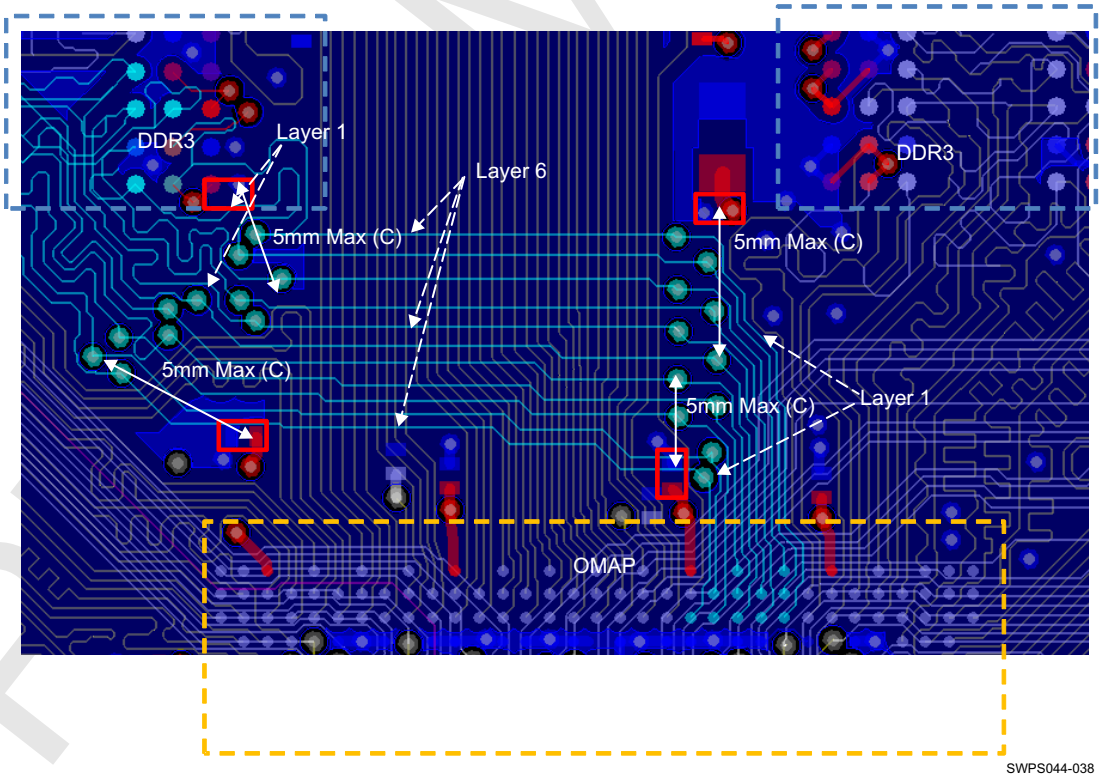


Figure 8-14. Byte 1 Crossing CA Bus

It is also important to secure the return path in the GND plane. As indicated on Figure 8-15 vias must have enough distance, not to make a big hole in the GND plane.

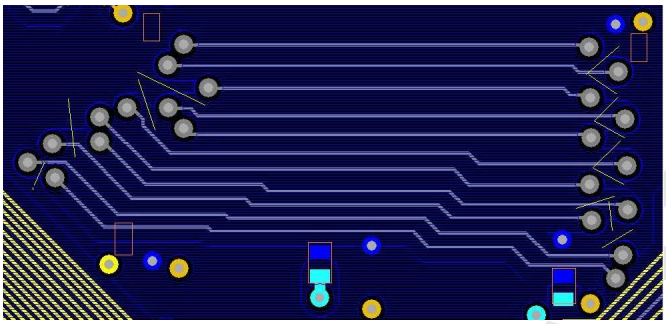


Figure 8-15. Layer2 GND Return Path (Yellow) and Decoupling Capacitors

8.2.4.4 Command Signal Routing

To obtain the best signal integrity, the T-branch CA line must be laid out as shown in Figure 8-16. The left and right arms of large-T (L1 = L2) must be balanced to within ±2 mm. It is ideal that small T (L3 = L4, L5 = L6) are also balanced to within ±2 mm, but it may be difficult.

Therefore, small T must be as short as possible. The unbalanced-T causes the signal degradation.

It is possible to route this way by 1-4-1 HDI.

The vias may be placed outside of the memory BGA area, it is important to match the left and right branches to within ±2 mm.

To route the CA bus by the 6L PTH, the small T could be long; therefore, it will be necessary to balance the small T. See Figure 8-17.

For the test layout, layer 1 is used for the blue line, layer 3 for the green, and layer 6 for the orange.

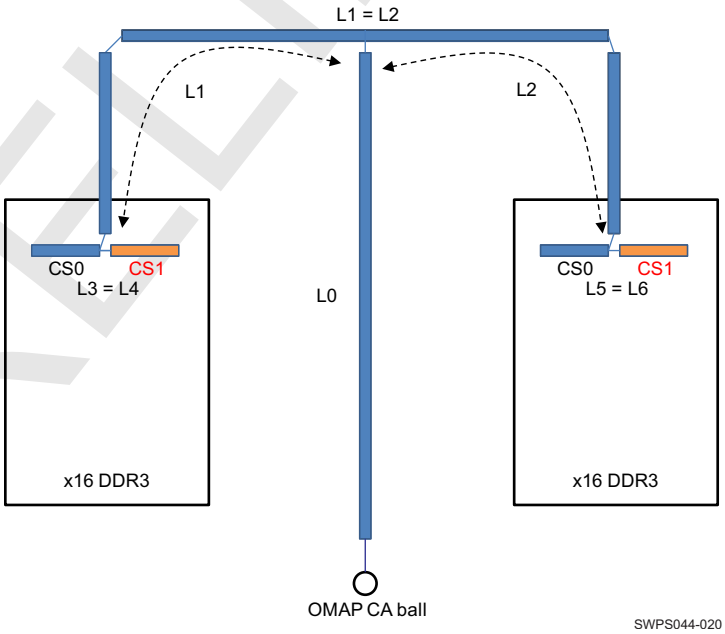


Figure 8-16. Goal of CA Layout

Hints for line balancing:

- The trombone loops may be added to balance L1 and L2. For example, if A0 is located at left, L1 needs to be extended. If ODT_0 is located at right, L2 needs to be extended. It is desirable to balance them within a few mm.
- The order of the horizontal bus must align to the order of the DDR3 balls. For example, RAS and CAS must be located next to the memory, A13 and A14 must be far from the memory. Reset must be at the end (reset is asynchronous).
- clk and nclk are close to the middle of the bus.

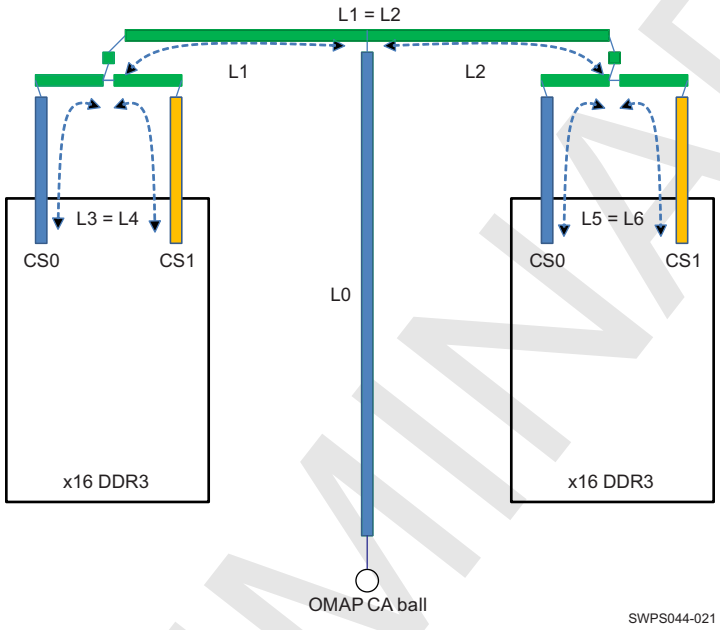


Figure 8-17. CA Topology of 6L PTH

In this way, total line length can be balanced < ±10 mm, from the clk lines. Static skew around 70 ps is acceptable.

8.2.4.5 Clock to Data Strobe Relationship

The OMAP5432 device supports write and read leveling. For the OMAP controller to work properly, the clock and the data-strobe must meet the following (DDR3-1066). The OMAP memory controller can delay the strobe to align to the clock at the memory. Therefore, the clock delay must be same or longer than the strobe.

Clock to strobe delay (clk – dqs = D1):

Default setting (invert clock): –470 ps < D1 < 470 ps

Approximate physical length: –67 mm < D1 < 67 mm

If D1 is not in this range, a noninvert clock can be used: 470 ps < D1 < 1410 ps

Approximate physical length: 67 mm < D1 < 201 mm

See the OMAP543x TRM to change invert clock setting.

Maximum round trip delay (ckl + dqs + 0.5 × t_{CK} = D2)

D2 < 2231 ps

If you use the floor plan described in this chapter, these conditions will be met with good margin.

8.2.4.6 Power Plane

Layer 2 and layer 5 are planes. They are assigned to GND and VDD-IO/DDR3 supply (1.35 V). The OMAP5432 GND and VDD-IO BGA must be connected to the plane. As illustrated in Figure 8-18, BGAs are depopulated so that critical via can be placed. GND/VDD-IO vias must be placed as mentioned in Figure 8-18. VDD-IO BGA must be connected to the decoupling capacitor by 0.25-mm width line at maximum length of 2 mm (A). The GND/VDD-IO vias must be located next to the decoupling capacitor. The maximum pad-to-pad spacing must be less than 0.5 mm (B). The 7 bottom decoupling capacitors must be connected between VDD-IO vias and GND vias. The maximum VDD-GND loop must be less than 2.5 mm.

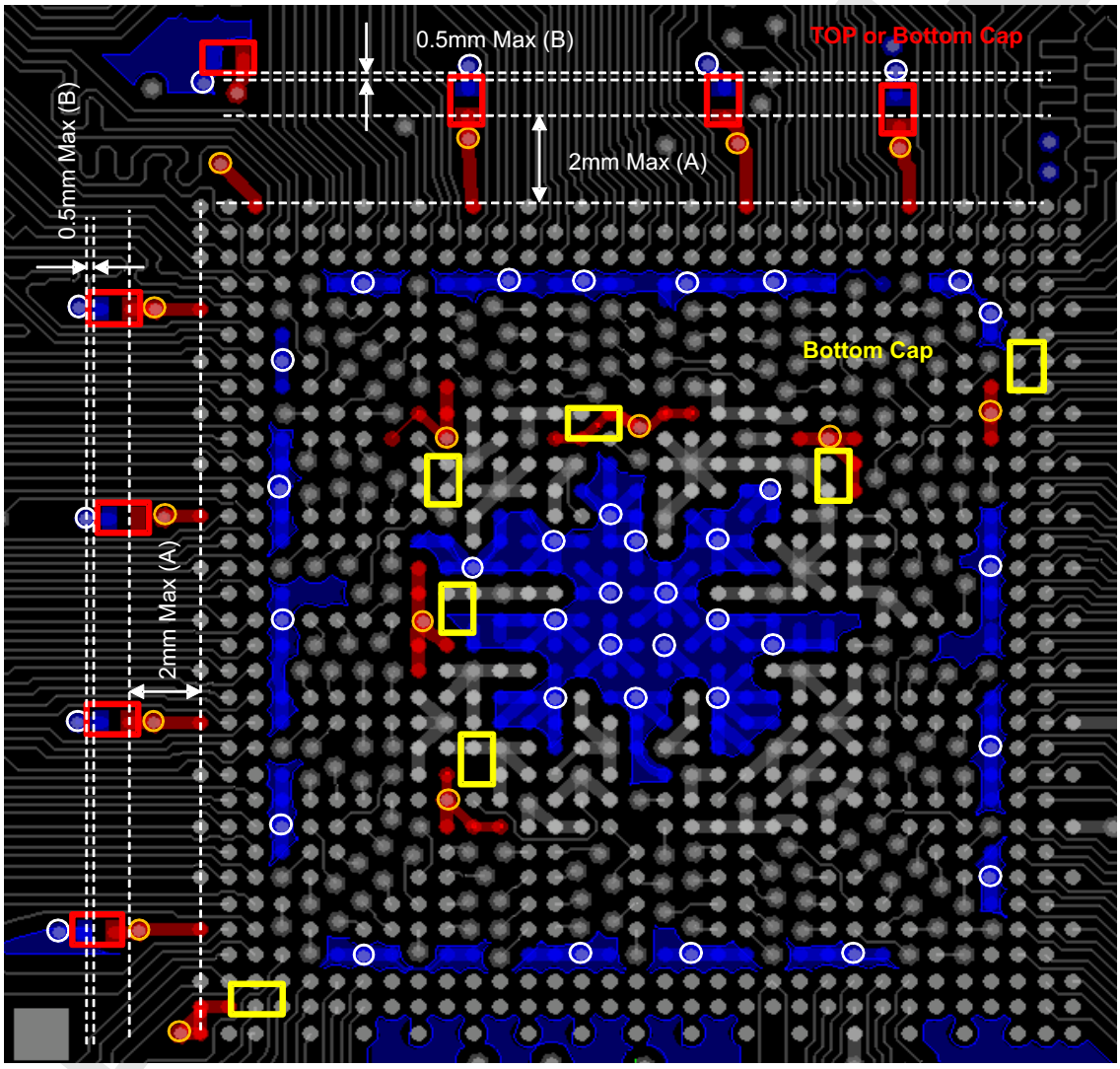


Figure 8-18. Critical Via and Decoupling Capacitor Connection

The layer 2 and layer 5 planes must be secured in the area as indicated in Figure 8-19. Basically the layer 2 plane must be placed anywhere the layer 1 signal line is present and the layer 5 plane for layer 6 signals. No other signal line is present in the plane secure area.

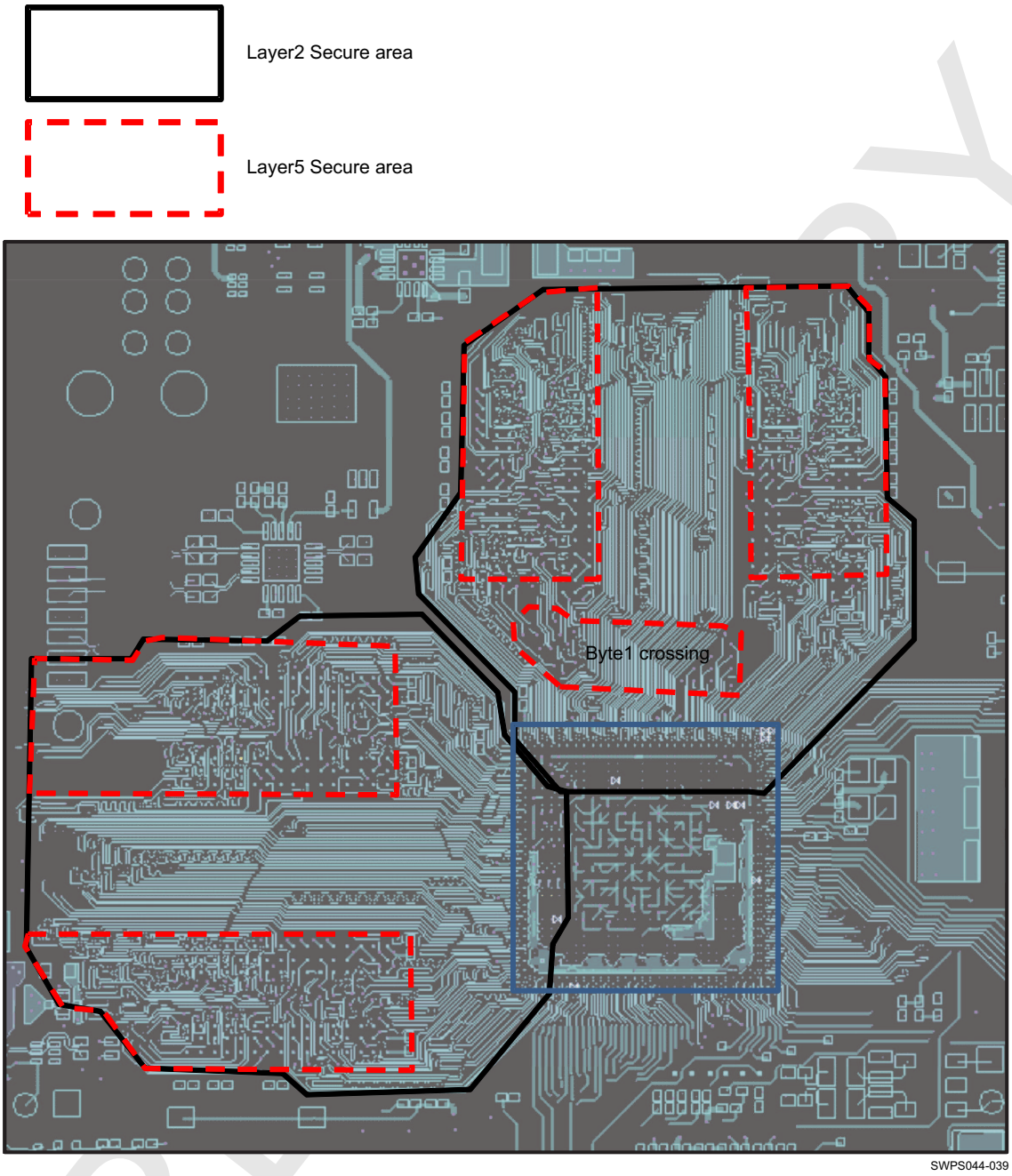


Figure 8-19. Layer 2/Layer 5 Plane Secure Area

8.2.4.7 Vref Routing

There are two Vref balls per channel. They are routed to DDR3 VREFDQ and VREFCA along with the CA bus. A greater than or equal to 500-µm wide trace must be used with a minimum 150-µm space from other signals. A 0.1-µF decoupling capacitor must be connected at both ends.

8.2.5 HDI PCB

8.2.5.1 Floor Plan

The high-level floor plan is almost identical to the PTH PCB. As already shown in Figure 8-11, layer 1 is GND and the signals are routed by layer 2. Layer 3 is the VDD plane. With this sandwich structure, layer 2 works as a strip-line.

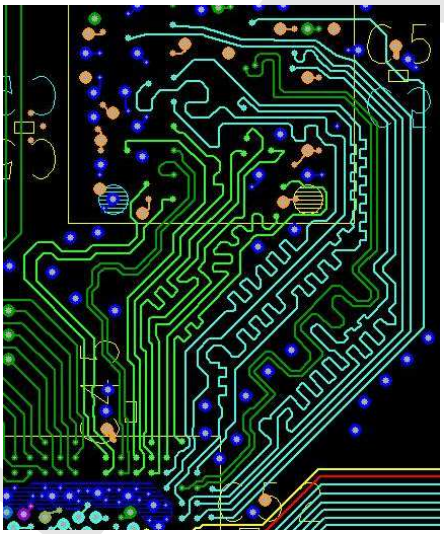
The impedance of layer 2 (75 µm) is 39 to 42 Ω and that is matched to the drive impedance of the IO (Ron = 40 Ω). Crosstalk to or from the adjacent lines is smaller than the microstrip structure.

The DQ bit swap is applied as PTH PCB, it helps to simplify the routing (see Table 8-2).

As described in Section 8.2.5.3, the crossing of address signals to the bottom memories can be done at the memory ball. Therefore, command routing topology shown in Figure 8-16 must be used. L1 and L6 are used to cross address lines to the bottom memory.

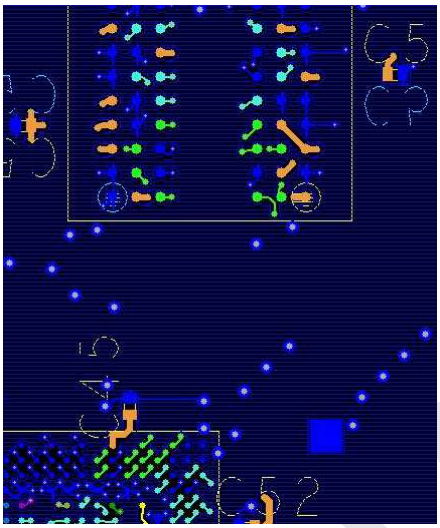
8.2.5.2 DQ Signal Routing

Figure 8-20 and Figure 8-21 show the test layout by 1-4-1 HDI PCB. Layer 1 is covered by the GND plane, and layer 2 is used for connecting data signal to memory. Layer 5 is used to cross the data signals to the bottom memories.



SWPS044-022

Figure 8-20. Routing DQ0/2 (L2)

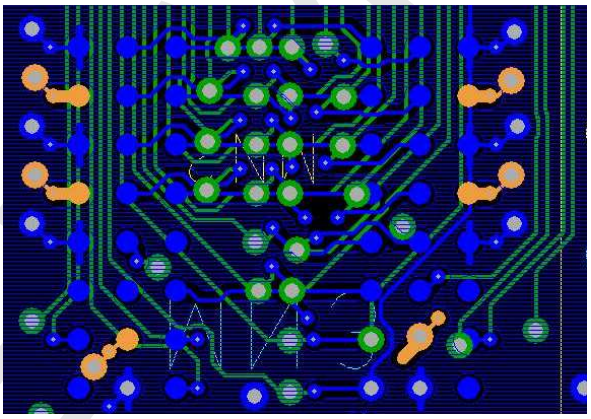


SWPS044-023

Figure 8-21. Routing DQ0/2 (L1)

8.2.5.3 Command-Address Routing

Figure 8-22 and Figure 8-23 show how CA signals are routed by HDI PCB. It is possible to cross the signal for the bottom memory at the memory balls. The vias are placed at the middle of the memory to balance the small-T as much as possible. L1 is used to cross inner balls (rows 3 and 7) and L6 for outer balls (rows 2 and 8).



SWPS044-024

Figure 8-22. Command-Address Routing L1/L2

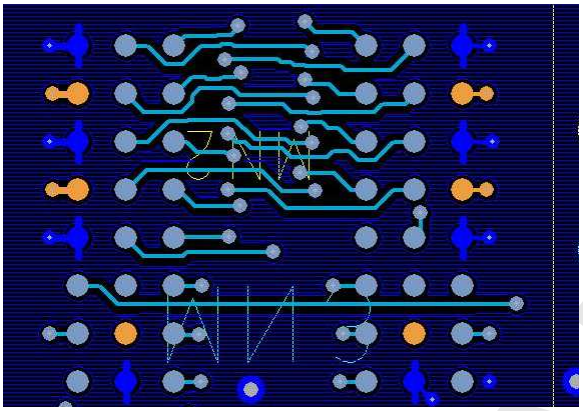


Figure 8-23. Command-Address Routing L6

8.2.6 DDR3 Timing Budget

8.2.6.1 Data Read Timing Budget

Figure 8-24 shows the timing diagram of the DDR3 memory specified by JESD79-3. Depending on the speed grade, t_{DQSQ} (150 ps for DDR3-1066) for setup and t_{QH} (76% UI) for data hold time are specified. Figure 8-24 (red lines) shows the memory data valid window.

The parameters are set assuming no clock jitter. When the memory is operated with jitter, they must be de-rated according to TJITper (see JESD79-3 section 13.3 jitter note g). 72 ps are counted on the budget sheet. Data interval is further reduced by the interconnect (PCB) (PCB + Pkg + IO). This is the setup and hold skew of the interconnect, see Figure 8-24 (blue lines).

The OMAP5432 device delays DQS or nDQS crossing time by $t_{CK}/4$ and samples the data. The delay time is automatically adjusted during the read data training. Therefore, at any unbalanced setup hold times are re-centered.

As a result, minimum setup time (247.9 ps) and hold time (104.2 ps) are needed for proper operation.

Entire PCB skew must be less than 40 ps.

It is recommended to simulate the entire interconnect chain; for example, IO + Pkg + PCB as described above. TI will provide encrypted spice model for IO and package. Total of 88-ps skew is acceptable.

When the memory spice model is used for a read simulation, the skew or jitter caused by the memory model must be removed from the simulation. The memory model skew can be estimated by terminating with a 25-Ω resistor.

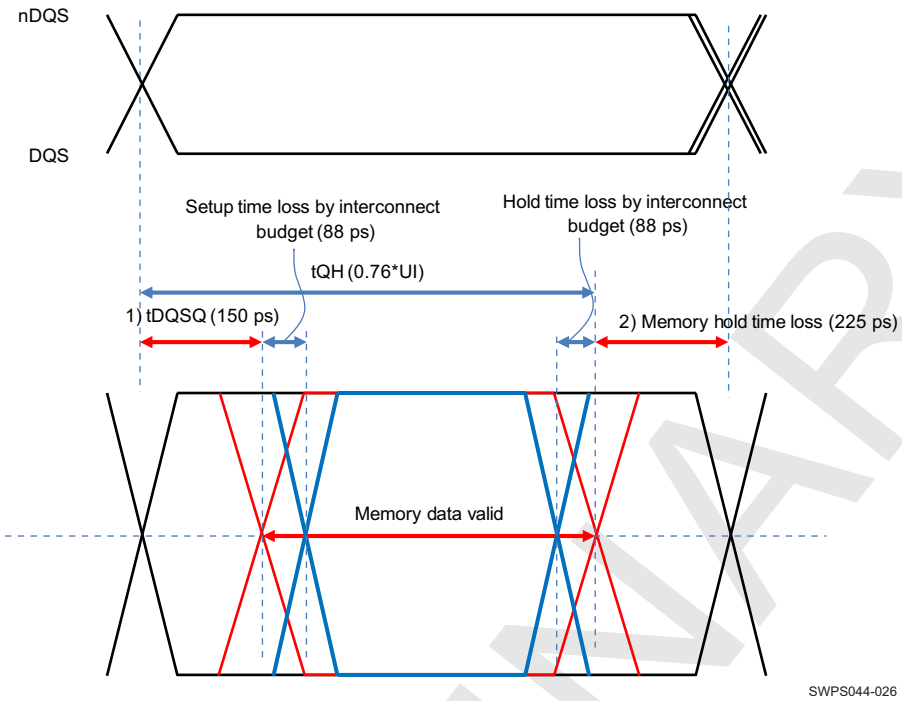


Figure 8-24. Data Read Timing

Table 8-3. DDR3 Data Read Timing Budget

	DDR3-1066		UNIT
DDR Clock Frequency	533		MHz
Maximum Interval (UI)	938		ps
Time Available (UI/2)	469.0	469.0	ps
Skew Components	**Setup**	**Hold**	
Transmitter			
t_{DQSQ} (1)	150.0		ps
Memory hold time loss (UI-t_{DH}) (2)		225.1	ps
t_{Jitter}/Duty		72.0	ps
Total Transmitter	**150.0**	**297.1**	ps
Interconnect (PCB)			
Static Skew (3)	10.0	20.0	ps
Crosstalk/SSO	30.0	20.0	ps
PCB total	40.0	40.0	ps
Others			
Total Interconnect (PCB)	**40.0**	**40.0**	ps
OMAP Setup and Hold Time			
IO + Package skew (4)	48.0	48.0	ps
OMAP Controller	199.9	56.2	ps
OMAP Total	**247.9**	**104.2**	ps
Margin	31.1	27.7	ps

(1) JEDEC DDR3-1066 t_{DQSQ}

(2) t_{DH} derated by jitter

(3) DQ/DQS/DM trace is balanced < ±0.5 mm. This is counting possibility of a delay matching error.

(4) Poor interconnect may degrade package skew. It is recommended to simulate PCB with IC model (H-spice).

8.2.6.2 Data Write Timing Budget

According to JESD79-3, the DDR3 memory timings are specified at V_{IH} and V_{IL}. The setup and hold times are also affected by the slew rate of the signal.

Figure 8-25 shows a relationship between each threshold and timing. t_{DS} and t_{DH} are specified at the nominal slew rate 1 (V/ns), it must be de-rated if the SR is changed.

Assuming that the SR > 1 (V/ns), we recalculate t_{DS} and t_{DH} for the Vref crossing. t_{DS}/t_{DH} is independent to SR at the Vref crossing point.

It must be verified by the simulation that t_{DS} (AC, DC) and t_{DH} (DC) meet the specification after de-rating with a measured SR.

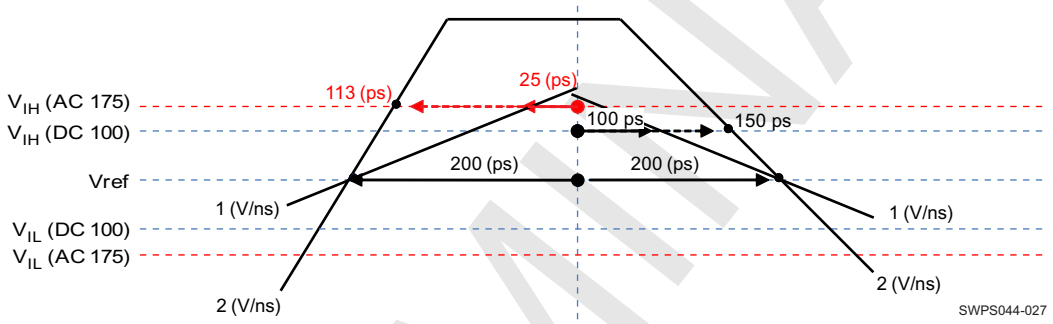


Figure 8-25. DDR3-1066 Setup/Hold Time vs Slew Rate

Table 8-4 shows the data write timing budget of DDR3-1066, the memory setup and hold times at Vref (200 ps) are used. PCB skew must be controlled below 40 ps. Vref crossing point gives unique setup and hold time requirements independent from SR.

Table 8-4. De-rated t_{DS}/t_{DH} AC/DC and t_{DS}/t_{DH} at Vref

DDR3-1066			
Slew Rate (V/ns)	1.0	1.5	2.0
t_{DS} (AC175) (ps)	25.0	84.0	113.0
t_{DS} (AC150) (ps)	75.0	125.0	150.0
t_{DH} (DC100) (ps)	100.0	134.0	150.0
t_{DS} (Vref) (ps)	200.0	200.7	200.5
t_{DH} (Vref) (ps)	200.0	200.7	200.0
DDR3-1333			
Slew Rate (V/ns)	1.0	1.5	2.0
t_{DS} (AC175) (ps)			
t_{DS} (AC150) (ps)	30.0	80.0	105.0
t_{DH} (DC100) (ps)	65.0	99.0	115.0
t_{DS} (Vref) (ps)	180.0	180.0	180.0
t_{DH} (Vref) (ps)	165.0	165.7	165.0
DDR3-1600			
Slew Rate (V/ns)	1.0	1.5	2.0
t_{DS} (AC175) (ps)			

Table 8-4. De-rated t_{DS}/t_{DH} AC/DC and t_{DS}/t_{DH} at Vref (continued)

t_{DS} (AC150) (ps)	10.0	60.0	85.0
t_{DH} (DC100) (ps)	45.0	79.0	95.0
t_{DS} (Vref) (ps)	160.0	160.0	160.0
t_{DH} (Vref) (ps)	145.0	145.7	145.0

Table 8-5. OMAP5432 DDR3 Write Timing Budget

	DDR3-1066		UNIT
DDR clock frequency	533		MHz
Maximum Interval (UI)	938		ps
Time Available (UI/2)	469.0	469.0	ps
Skew Components	**Setup**	**Hold**	
Transmitter			
Clock jitter		76.59	ps
OMAP controller skew	169.3	97.5	ps
IO + package(1)	55.0	55.0	ps
Transmitter Total	**224.3**	**229.1**	ps
Interconnect			
PCB Static Skew(2)	10.0	20.0	ps
PCB Crosstalk/jitter	30.0	20.0	ps
PCB total	**40.0**	**40.0**	ps
Others			
Total Interconnect	**40.0**	**40.0**	ps
Receiver			
Memory t_{DS} at Vref(3)	200.0		ps
Memory t_{DH} at Vref(4)		200.0	ps
Total Receiver	**200.0**	**200.0**	ps
Margin	4.8	0.0	ps

(1) Poor interconnect may degrade package skew. It is recommended to simulate PCB with IC model (H-spice).

(2) DQ/DQS/DM trace must be balanced < ±0.5 mm. This is counting possibility of delay matching error.

(3) Measured from crossing $V_{IH(ac)min}$ or $V_{IL(ac)max}$. DDR3: Referenced to AC175 level. Converted to Vref reference to be independent of slew rate.

(4) Measured from crossing $V_{IH(dc)min}$ or $V_{IL(dc)max}$. DDR3: Referenced to DC100 level. Converted to Vref reference to be independent of slew rate.

8.2.6.3 Command-Address Timing Budget

Table 8-6 shows the timing budget of the CA bits. In the table package and IO skew are included in the controller skew. DDR3 CA is SDR, therefore we could allocate larger skew for the CA bits. To facilitate the T-Branch routing, considerably large skew (300 ps) is allocated to the PCB. Therefore, path length mismatch is relaxed to ±10 mm that gives about 70 ps of static skew.

As described in Section 8.2.4.4, it is recommended to balance the large and small-T. Unbalanced T and fast slew-rate may cause signal integrity degradation.

Table 8-6. Command-Address Timing Budget

	DDR3-1066		UNIT
DDR Clock Frequency	533		MHz
Maximum Interval (UI)	1876		ps
Time Available (UI/2)	938.0	938.0	ps
Skew Components	**Setup**	**Hold**	

Table 8-6. Command-Address Timing Budget (continued)

	DDR3-1066		UNIT
Transmitter			
Full cycle clock jitter		41.52	ps
OMAP Controller Skew	277.7	232.7	ps
Transmitter Total	**277.7**	**274.2**	ps
Interconnect			
PCB Static Skew	70.0	70.0	ps
PCB Crosstalk/jitter	230.0	230.0	ps
PCB total	**300.0**	**300.0**	ps
Others			ps
Total Interconnect	**300.0**	**300.0**	ps
Receiver			
Memory t_{IS} at Vref(1)	300.0		ps
Memory t_{IH} at Vref(2)		300.0	ps
Total Receiver	**300.0**	**300.0**	ps
Margin	60.3	63.8	ps

(1) Based on JESD79-3D spec with respect to AC175 level. Converting then to Vref base to be independent of slew rate.

(2) Based on JESD79-3D spec with respect to DC100 level. Converting then to Vref base to be independent of slew rate.

8.3 External Capacitors

8.3.1 Core, MPU, MM and VIO_DDR3 Voltage Decoupling

8.3.1.1 Core, MPU, MM and VIO_DDR3 Voltage Decoupling Values

The following are some core, MPU, MM (multimedia), and VIO_1V5 (Vddq) voltage decoupling PCB recommendations.

The PCB guidelines between the power IC (PMIC) balls and the OMAP balls are:

- For core, MPU, and MM:

  Maximum recommended inductance by power supply rail is less than 2 nH (VDD + VSS)

  Maximum recommended static IR-drop by power supply rail is less than 1.5% (with rise on ground accounted for).
- For VIO_1V5 (vddq):

  Maximum recommended static IR-drop by power supply rail is less than 1% (with rise on ground accounted for).

  The capacitor value is defined at ±50% of the value in order to take in account the aging effects, and the voltage impact.

  Maximum ESR = 0.3 Ω at 1 GHz and maximum ESL = 0.45 nH.
- Main characteristics of the decoupling bypass capacitors are listed in Table 8-7:

Table 8-7. Decoupling Bypass Capacitors Main Characteristics(1)(2)

CAPACITOR	PACKAGE	VERSION	TOLERANCE	VOLTAGE	REFERENCE
22 µF	0603	X5R	±20%	6.3 V	GRM188R60J226MEA
4.7 µF	0402	X5R	±20%	6.3 V	GRM155R60J475ME87
2.2 µF	0402	X5R	±20%	6.3 V	GRM155R60J225ME95
1 µF	0201	X5R	±20%	6.3 V	GRM033R60J105MEA2
470 nF	0201	X5R	±20%	6.3 V	GRM033R60J474ME90
220 nF	0201	X5R	±20%	4.0 V	GRM033R60G224ME15
100 nF	0201	X5R	±20%	6.3 V	GRM033R60J104ME19

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

Table 8-8. Core, MPU, MM Decoupling Characteristics[6]

PARAMETER	PDN IMPEDANCE CHARACTERISTICS[4]		PCB RESISTANCE BETWEEN SPMS AND OMAP (mΩ)[5]	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WITHOUT ESL)[2]	DECOUPLING CAPACITOR VALUES[3]						
	IMPEDANCE TARGET (mΩ)	FREQUENCY OF INTEREST (MHz)			100 nF	220 nF	470 nF	1 µF	2.2 µF	4.7 µF	22 µF
C_{vdd_core}	82	77	20	0.6	3	1	0	1	0	1	0
C_{vdd_mpu}	28	16	5	0.4	5	0	3	4	1	0	1
C_{vdd_mm}	41	30	10	0.5	3	1	0	1	0	1	0

(1) For more information on peak-to-peak noise values, see Table 3-3, *Recommended Operating Conditions*.

(2) ESL must be as low as possible and must not exceed 0.5 nH.

(3) To take into account the aging effects and voltage impact on capacitance, their values, as described in Table 8-7, are specified at ±50%.

(4) The PDN (Power Delivery Network) impedance characteristics are defined versus the device activity (that runs at different frequency) based on Table 3-3, *Recommended Operating Conditions*.

(5) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the OMAP5 power balls.

(6) Assuming that the external SMPS (power IC) feedback sense is taken close to OMAP5432 power balls.

Table 8-9. VIO_DDR3 Decoupling Characteristics[1][2]

PARAMETER	VOLTAGE (V)	PDN IMPEDANCE CHARACTERISTICS		DECOUPLING CAPACITOR VALUES			
		Impedence Target (mΩ)	Frequency of Interest (MHz)	100nF	470nF	1µF	2.2µF
$C_{vdds\_ddr\_ch1}$ / $C_{vdds\_ddr\_ch2}$ $C_{vddq\_vref\_ddrch1}$ / $C_{vddq\_vref\_ddrch2}$	1.35	135	202	8	2	1	1

(1) The data in this table are given with an assumption of 500 mA for 1.35- and 1.5-V voltages. This current value can vary depending on the memory vendor.

(2) The worst case is at 1.35 V. The 1.5 V case is covered by the worst case.

Table 8-10. VIO_1V5 Decoupling Characteristics

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR (pF)				MAXIMUM FREQUENCY BANDWIDTH (MHz)
					100 nF	470 nF	1 µF	2.2 µF	
VIO_V5 (vddq)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

8.3.1.2 Core, MPU, MM and VIO_DDR3 Voltage Decoupling PCB Examples

8.3.1.2.1 MPU Voltage Decoupling PCB Examples

Figure 8-26 and Figure 8-27 show an example of PCB layout of vdd_mpu with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-26 and Figure 8-27 describe a working board. They do not show an optimized board.

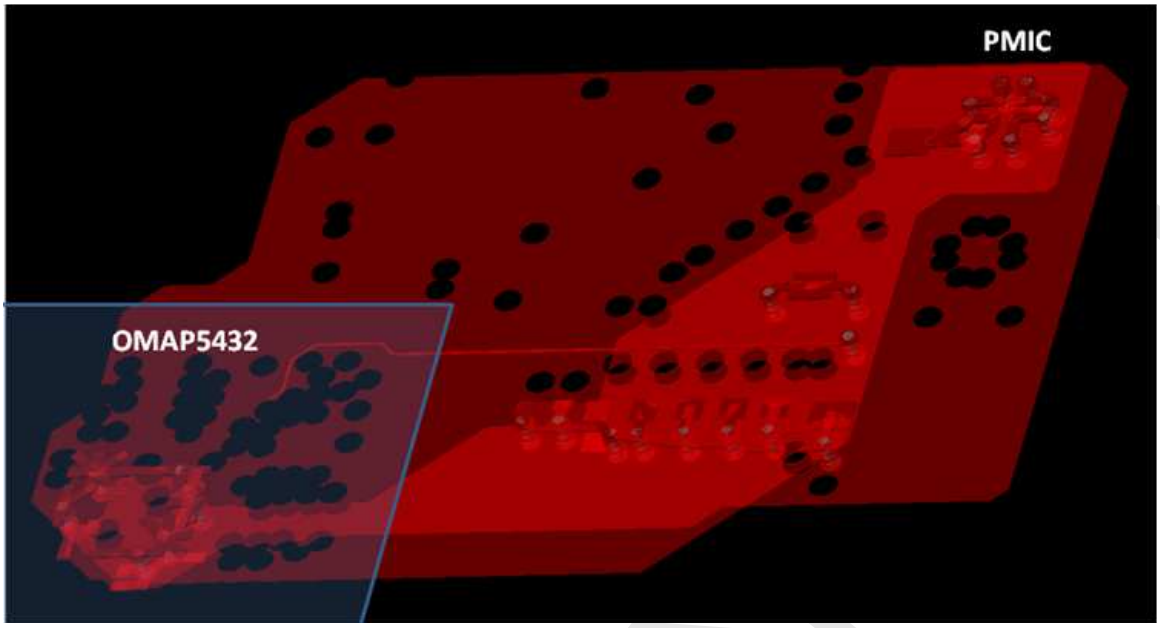


Figure 8-26. vdd_mpu PCB Requirements(1)

(1) Figure 8-26 shows an example of vdd_mpu PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 8-27 describes the vdd_mpu PDN analysis versus frequency.

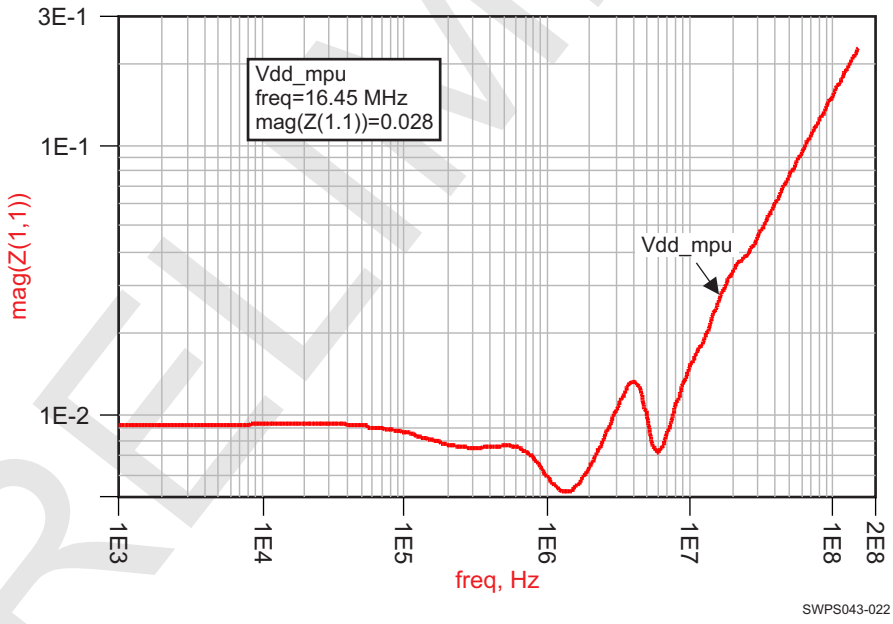


Figure 8-27. vdd_mpu PDN Analysis

8.3.1.2.2 MM Voltage Decoupling PCB Examples

Figure 8-28 and Figure 8-29 show an example of PCB layout of vdd_mm with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-28 and Figure 8-29 describe a working board. They do not show an optimized board.

Figure 8-28. vdd_mm PCB Routing(1)

(1) Figure 8-28 shows an example of vdd_mpu PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 8-29 shows the vdd_mm PDN analysis versus frequency:

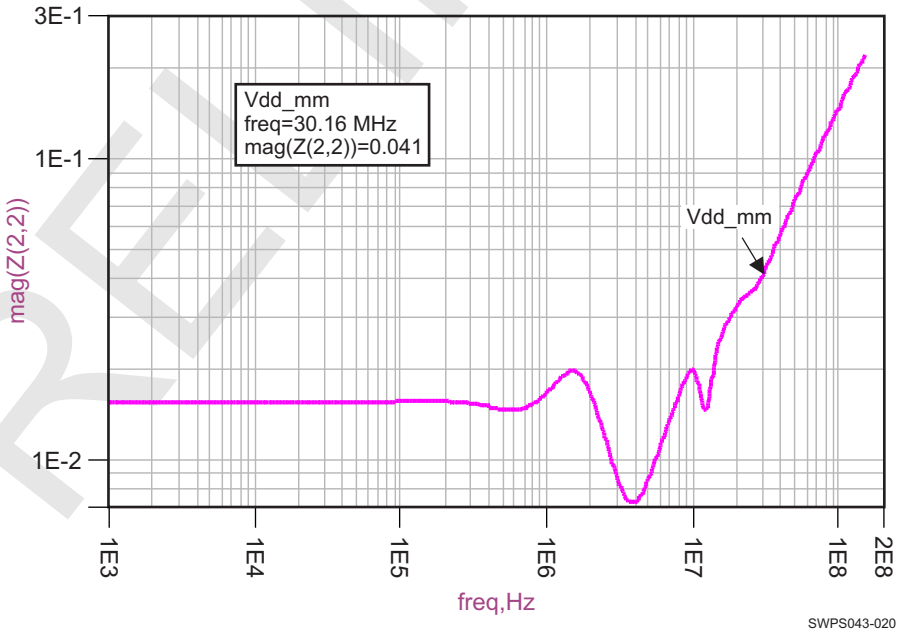


Figure 8-29. vdd_mm PDN Analysis

8.3.1.2.3 Core Voltage Decoupling PCB Examples

Figure 8-30 and Figure 8-31 show an example of PCB layout of vdd_core with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-30 and Figure 8-31 show describe a working board. They do not show an optimized board.

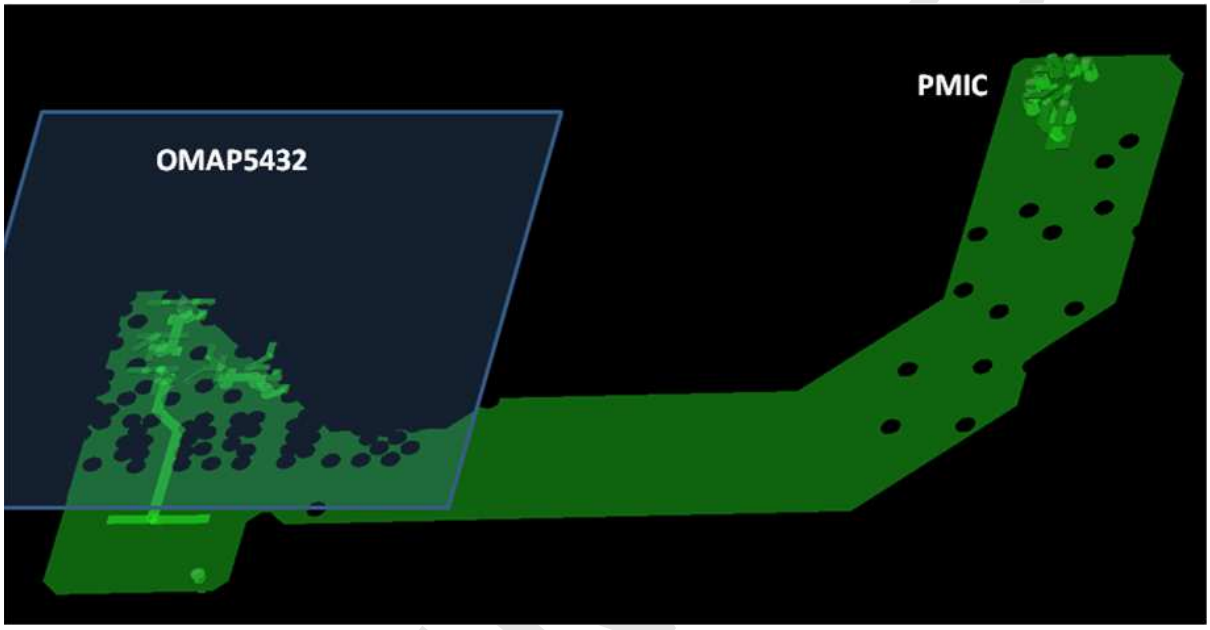


Figure 8-30. vdd_core PCB Routing(1)

(1) Figure 8-30 describes an example of vdd_core PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 8-31 shows the vdd_core PDN analysis versus frequency:

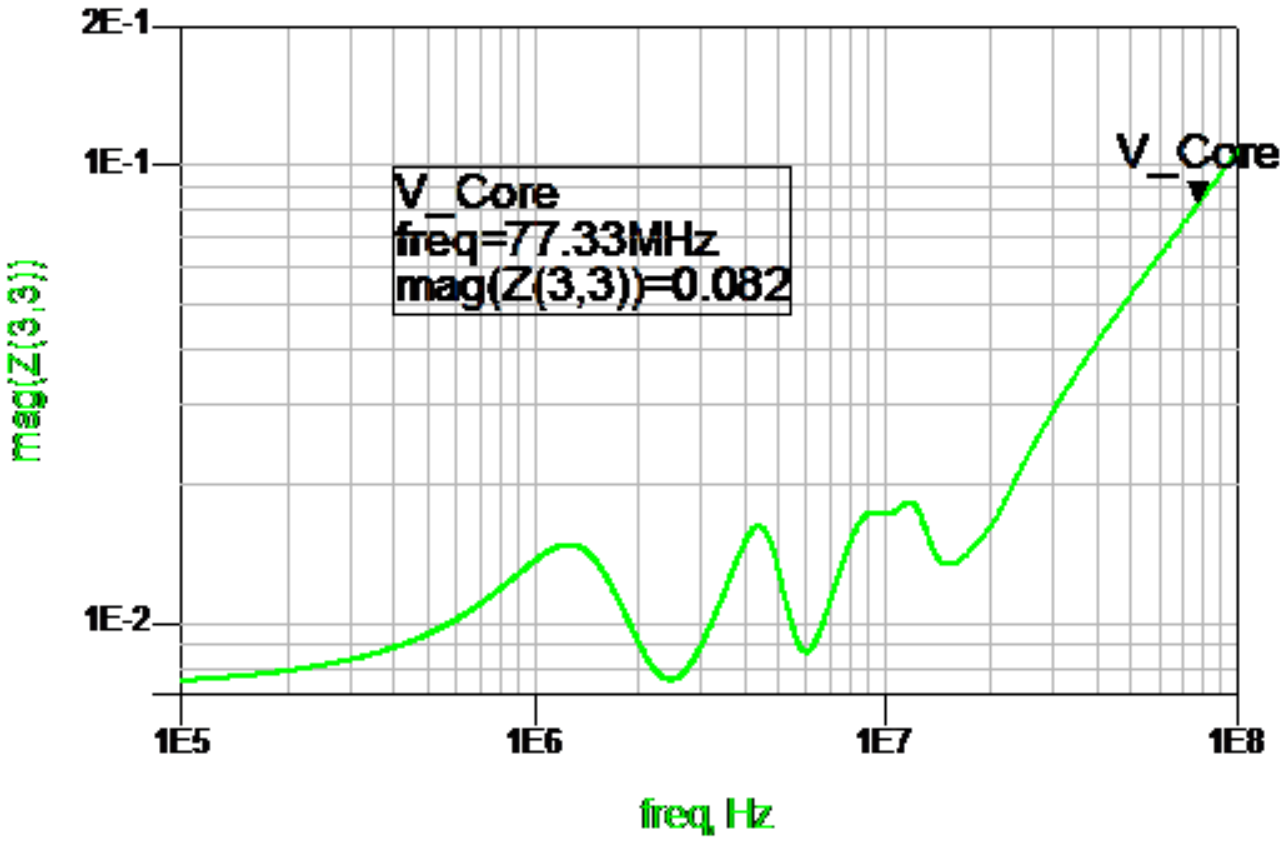


Figure 8-31. vdd_core PDN Analysis

8.3.1.2.4 VIO_DDR3 Decoupling PCB Examples

Figure 8-32 and Figure 8-33 show an example of PCB layout of VIO_1V5 with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-32 and Figure 8-33 describe a working board. They do not show an optimized board.

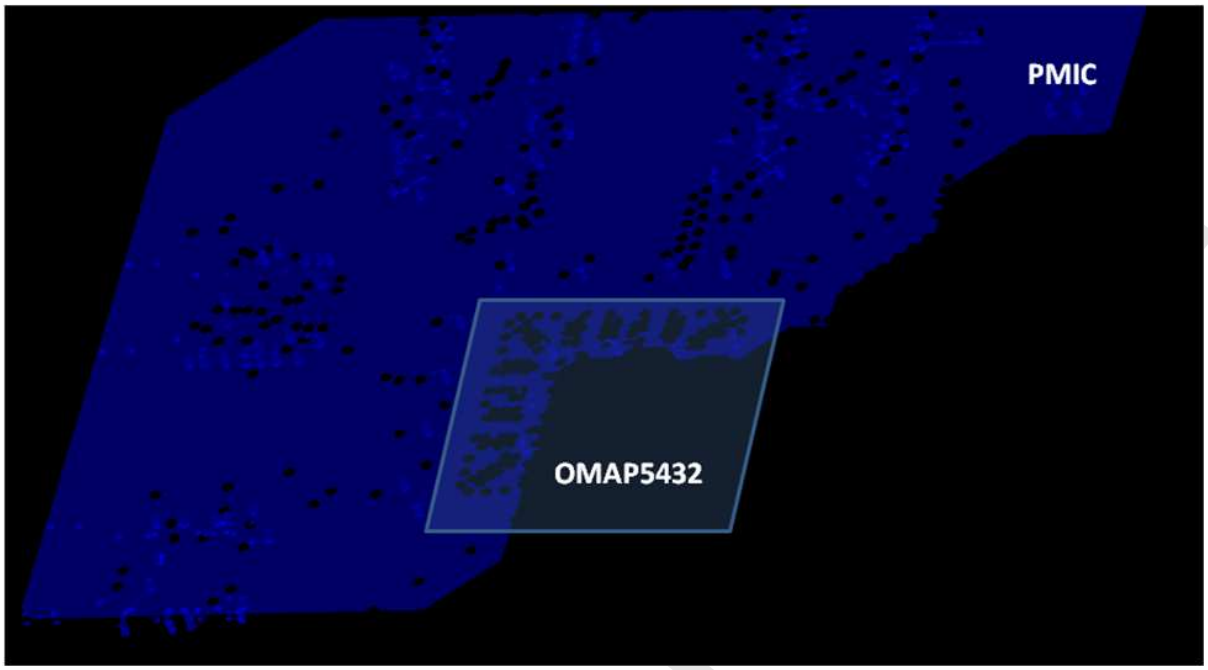


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Figure 8-32. vdd_core PCB Routing(1)

(1) Figure 8-32 describes an example of VIO_1V5 PCB layout that meets the IR drop and capacitance-inductance loop requirements.

Figure 8-33 shows the VIO_1V5 PDN analysis versus frequency:

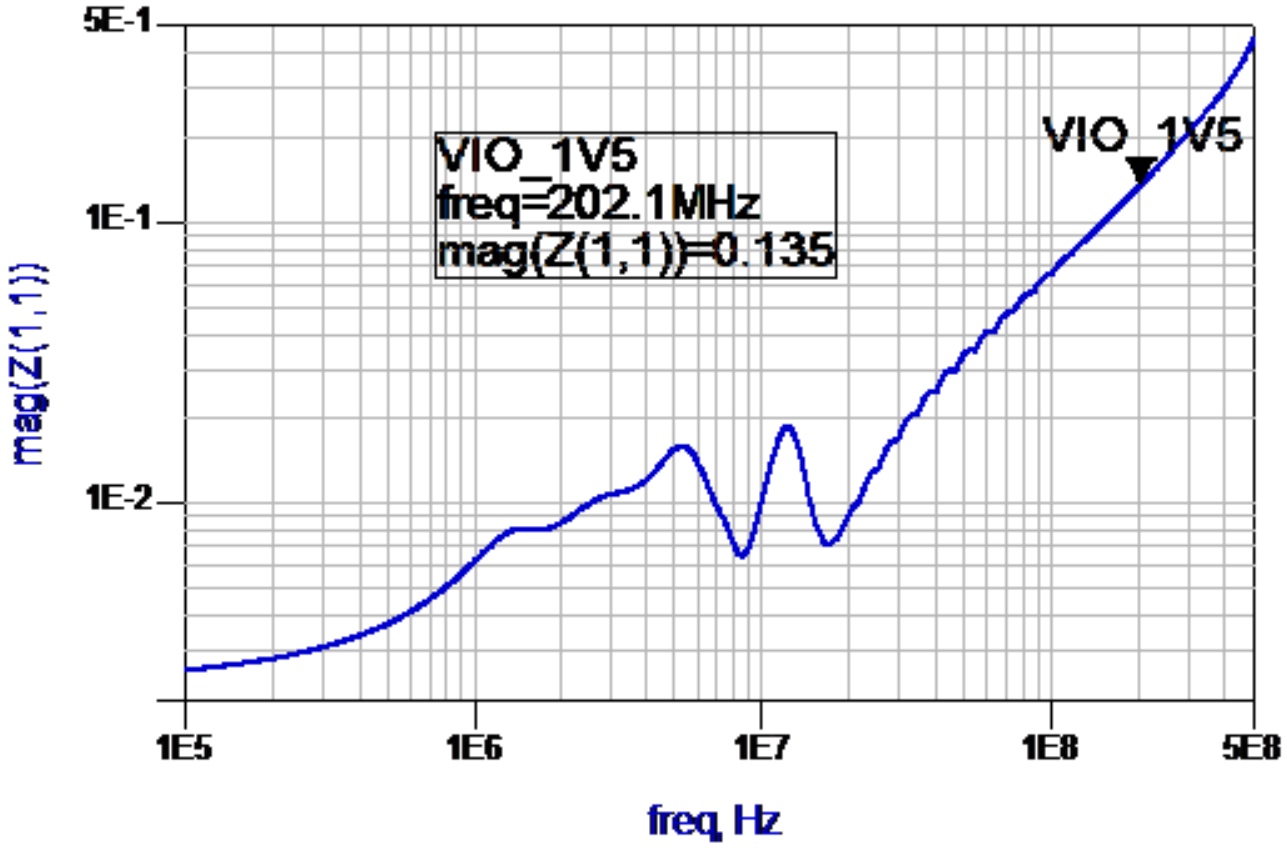

Figure 8-33. VIO_DDR3 PDN Analysis

9 Glossary

9.1 GLOSSARY

ABE	Audio Back End
AC or ac	Alternating Current
APLL	Analog Phase Locked Loop
ARM	Advanced RISC Machine
ASIC	Application-Specific Integrated Circuit
BG	Bandgap
CAM	Parallel Camera Interface
CCP	Compact Camera Port
CDM	Charged Device Modem
CJTAG	Component Joint Test Action Group, IEEE 1149.1 Standard
CM	Clock Manager
CMOS	Complementary Metal Oxide Silicon
CSI	Camera Serial Interface
DAC	Digital-to-Analog Converter
DC or dc	Direct Current
DDR	Double Data Rate
DISPC	Display Controller
DLL	Delay Locked Loop
DMA	Direct Memory Access
DMIC	Digital Microphone
DPLL	Digital Phase-Locked Loop
DSI	Display Serial Interface
DSS	Display Subsystem
eFuse	Electrical Fuse
EMIF	External Memory Inferface
eMMC	embedded MultiMedia Card
EMU	Emulation
ESD	Electrostatic Discharge
ESR	Equivalent series resistance
ETK	Embedded Trace kit
ETM	Embedded Trace Macrocell
FIR	Fast Infrared
FSR	Full-Scale Range
FSUSB	Full-Speed Universal Serial Bus
GP	General-Purpose
GPIN	General-Purpose Input
GPIO	General-Purpose Input Output
GPMC	General-Purpose Memory Controller
HBM	Human Body Model
HDMI	High Definition Multimedia Interface
HDQ	High-Speed Data Queue
HDTV	High-Definition Television
HS	High speed or high security
HSI	High-speed Synchronous Interface
HSUSB	High-Speed Universal Serial Bus
HWDBG	Hardware Debug

HYS	Hysteresis
I^2C	Inter-Integrated Circuit
I2S	Inter IC Sound
IC	Integrated Circuit
ICE	In-Circuit Emulator
IEEE	Institute of Electrical and Electronics Engineers
IO	Input or Output
IR	Infrared
IrDA	Infrared Data Association
ISP	Image Sensing Product
ITU	International Telecommunications Union
IVA	Image and Video Accelerator
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group (Image format)
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LCD	Liquid-Crystal Display
LDO	Low Dropout
LJF	Left-Justified Format
LP	Low Power
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signaling
McBSP	Multichannel Buffered Serial Port
McSPI	Multichannel Serial Port Interface
MIPI®	Mobile Industry Processor Interface (MIPI ® is a registered trademark of Mobile Industry Processor (MIPI) Alliance.)
MIR	Medium Infrared
MMC	MultiMedia Card
MPU	Microprocessor Unit
MS-PRO	Memory Stick PRO
NA	Not Applicable
NAND	Not AND (Boolean Logic)
NOR	Not OR (Boolean Logic)
OMAP	Open Multimedia Applications Platform
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PDN	Power Delivery Network
PD	Pull Down
PHY	Physical Layer Controller
PLL	Phase-Locked Loop
POP	Package On Package
PU	Pull Up
QXGA	Quad eXtended Graphics Array
RAW	Raw (Image format)
RFBI	Remote Frame Buffer Interface
RGB	Red Green Blue (Image format)
RMS	Root Mean Square
RX	Receiver / Receive
SAP	TBD

SCL	Serial Clock: programmable serial clock used in the I^2C interface (can be called also SCLK)
SDA	Serial Data: serial data bus in the I^2C interface
SDI	Serial Display Interface
SDIO	Secure Digital Input Output
SDMMC	Secure Digital MultiMedia Card
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SDRC	SDRAM Controller
SDTI	System Debug Trace Interface
SIM	Subscriber Identity Module
SIR	Slow Infrared
SPI	Serial Port Interface
SRAM	Synchronous Random Access Memory
SSI	Synchronous Serial Interface
STN	Super Twist Nematic (LCD Panel)
SYNC	Synchronous
SYS	System
TAP	Test Access Point
TBD	To Be Defined
TDM	Time Division Multiplexing
TFT	Thin Film Transistor (LCD Panel)
TLL	Transistor-Transistor Logic
TX	Transmitter / Transmit
UART	Universal Asynchronous Receiver Transmitter
ULPI	UTMI Low Pin Interface
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
UTMI	USB2.0 Transceiver Macrocell Interface
WKUP	Wake-Up
YUV	Luminance + 2 Chrominance Difference Signals (PAL Y, Cr, Cb) Color Encoding

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