OMAP™

OMAP5430
Multimedia Device
Engineering Samples 2.0

Version F

Data Manual

Texas Instruments

Public Version

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Multimedia Device
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1 Introduction

This Data Manual describes the electrical and mechanical specifications of the OMAP5430 processor. It consists of the following sections:

- A description of the device terminals: ball assignments, electrical characteristics, multiplexing modes, and signal descriptions (Section 2)
- A description of the required electrical characteristics: absolute maximum ratings, operating conditions, dc characteristics, voltage decoupling capacitors, and device power-up and power-down sequences (Section 3)
- The clock specifications: characteristics of the input and output clocks, PLL and DLL specifications (Section 4)
- The timing requirements and switching characteristics (ac timings) of the interfaces (Section 5)
- The thermal management recommendations including the thermal resistance characteristics (Section 6)
- A description of the device nomenclature, and mechanical data (Section 7)
- The OMAP5430 processor multimedia device PCB guidelines (Section 8)
- A glossary of the acronyms and abbreviations used in the data manual (Section 9)

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This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

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This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

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2 Terminal Description

2.1 Terminal Assignment

Figure 2-1 and Figure 2-2 show the ball locations for the 980-ball plastic ball grid array (PBGA) package and are used in conjunction with Table 2-1 through Table 2-40 to locate signal names and ball grid numbers.

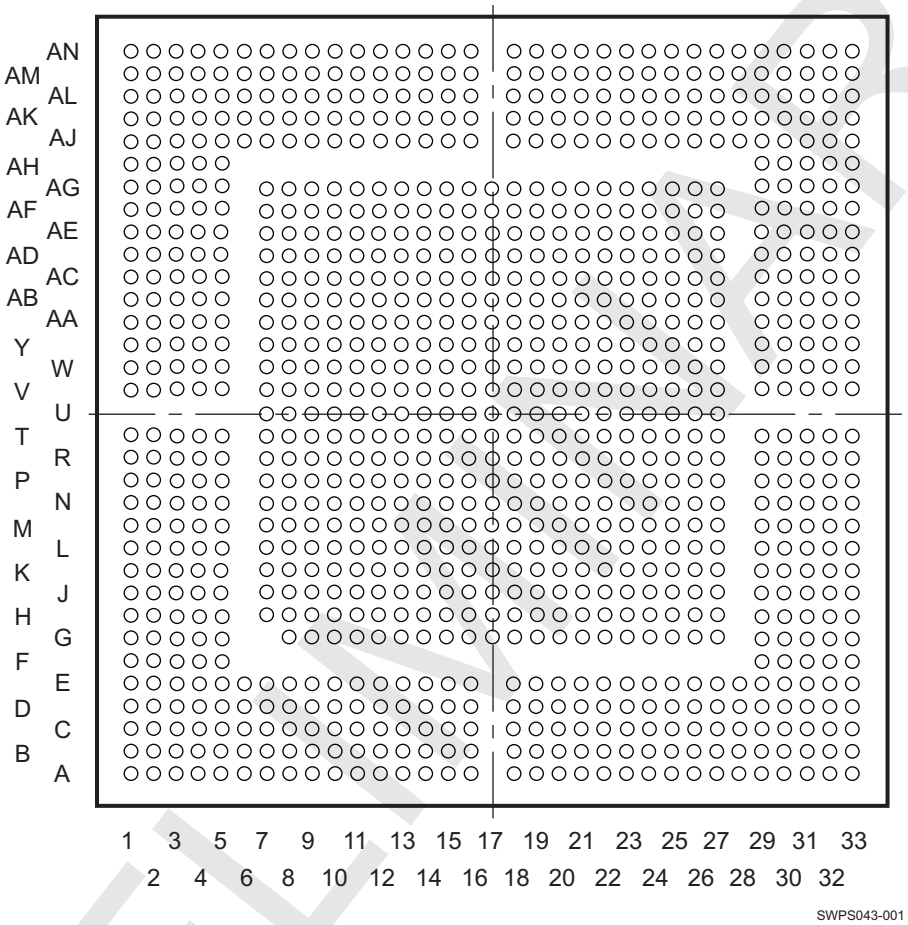


Figure 2-1. OMAP5430 CBU S-PBGA-N980 Package (Bottom View)

NOTE

The following bottom balls are not connected: A1 / A11 / A23 / A4 / AF1 / AJ1 / AK33 / AL33 / AM1 / AM33 / AN23 / AN24 / AN30 / AN31 / AN32 / AN33 / AN4 / AN9 / D1 / E33 / G1 / J1 / J33 / P1 / V33.

These balls can be connected to VSS if desired.

NOTE

The following bottom balls are reserved: AA29 / AA30 / AA4 / AA5 / AB30 / AB4 / AB5 / AC30 / AC4 / AC5 / AF4 / AF5 / AG30 / AG4 / AJ14 / AJ15 / AJ19 / AL27 / AL29 / AL3 / AL30 / AL4 / AM29 / AM3 / AM30 / AM31 / AM4 / B23 / B24 / B29 / B3 / B4 / C23 / C24 / C28 / C3 / C4 / D28 / D4 / D5 / E4 / E5 / F4 / G4 / G5 / H4 / H5 / J4 / J5 / K4 / K5 / L4 / L5 / M4 / M5 / P4 / P5 / R4 / T4 / W4 / Y29 / Y30 / Y4 / Y5 / A2 / AN2 / AE4 / AK19 / AN1 / V5 / AJ13 / D16 / N5 / E28 / E27 / K33 / A5 / R5 / AD5 / F5 / AH5 / AM16 / AL16 / AM14 / AL14 / AM12 / AL12 / AM15 / AL15 / AM13 / AL13 / AM11 / AL11 / C15 / B15 / C13 / B13 / C16 / B16 / C14 / B14 / C12 / B12.

These balls must be left unconnected.

NOTE

The following bottom balls are reserved: AN16 / AK16 / AN15 / AK15 / AK13 / AK14 / AG13 / D11 / B11 / E11 / C11 / G11

These balls must be grounded.

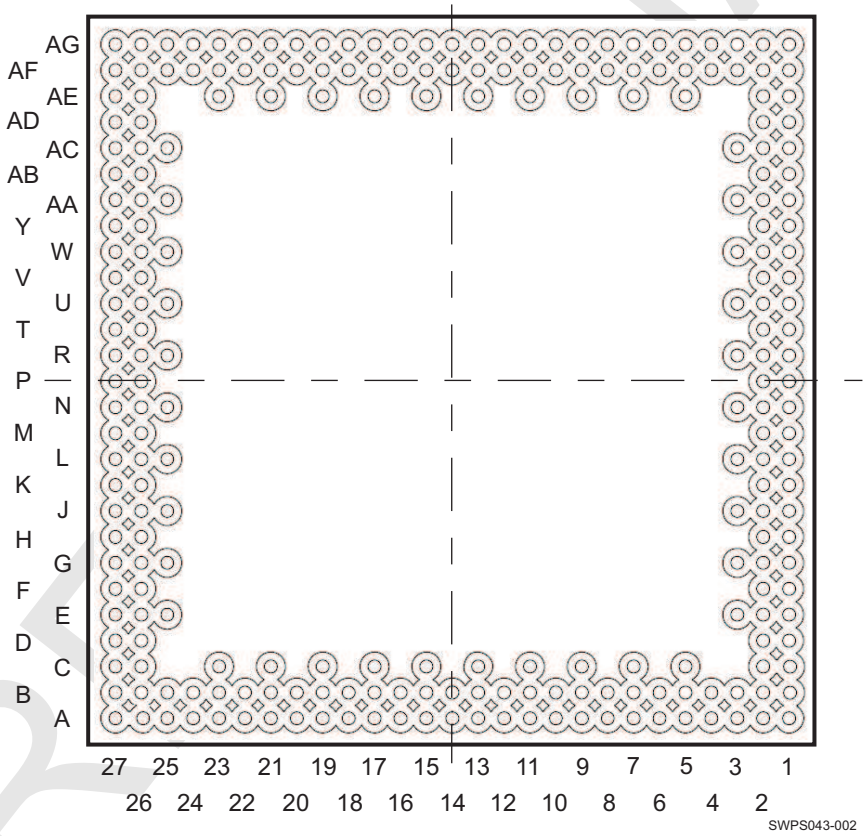


Figure 2-2. OMAP5430 CBU S-PBGA-N980 Package (Top View)

NOTE

The following top balls are not connected: A27 / A1 / AC26 / AC25 / AD27 / AD26 /AE27 / AE26 / AE23 / AF27 / AF26 / AF25 / AF24 / AG27 / AG26 / AG25 / AG24 / AG1.

2.2 Ball Characteristics

Table 2-1 describes the terminal characteristics and the signals multiplexed on each ball. The following list describes the table column headers:

1. **BALL BOTTOM:** Ball number(s) on the bottom side associated with each signal on the bottom.
2. **BALL TOP:** Ball number(s) on the top side associated with each signal on the top.
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in mode 0).

NOTE

Table 2-1 does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 2.4, *Signal Descriptions*.

NOTE

In the safe_mode, the buffer is configured in high-impedance.

4. **MODE:** Multiplexing mode number:
   (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. The primary mode is not necessarily the default mode.

NOTE

The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.

   (b) Modes 1 through 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and correspond to a safe mode per design implementation.
5. **TYPE:** Signal type and direction:
   – I = Input
   – O = Output
   – IO = Input or Output
   – D = Open drain
   – DS = Differential
   – A = Analog
   – PWR = Power
   – GND = Ground
6. **BALL RESET STATE:** The state of the terminal at power-on reset:
   – 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   – 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   – Z: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H: High-impedance with an active pullup resistor
7. **BALL RESET REL. STATE:** The state of the terminal at the release of the system control module reset (PRCM CORE_PWRON_RET_RST reset signal).
   – 0: The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   – 1: The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   – Z: High-impedance
   – L: High-impedance with an active pulldown resistor
   – H: High-impedance with an active pullup resistor

NOTE

For more information on the CORE_PWRON_RET_RST reset signal and its reset sources, see the Power Reset and Clock Management / PRCM Reset Management Functional Description section of the OMAP543x TRM.

8. **RESET REL. MODE:** This mode is automatically configured at the release of the system control module reset (PRCM CORE_PWRON_RET_RST reset signal).
9. **IO VOLTAGE VALUE**: This column describes the IO voltage value (VDDS supply).
10. **POWER NAME:** The voltage supply that powers the terminal IO buffers.
11. **SECOND POWER AVAIL.**: Some OMAP5430 IOs have a second power supply signal (vdds_1p8) to ensure the VDDS ramping.
12. **HYS:** Indicates if the input buffer is with hysteresis:
    - Yes: With high hysteresis
    - No: Without low hysteresis

NOTE

For more information, see the hysteresis values in Section 3.4, *DC Electrical Characteristics*.

13. **BUFFER STRENGTH:** Drive strength of the associated output buffer.

NOTE

For programmable buffer strength:
- The default value is given in .
- A note describes all possible values according to the selected mode.

14. **PULLUP/DOWN—TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

NOTE

The pullup/pulldown drive strength is equal to: minimum = 50 µA, typical = 100 µA, maximum = 250 µA, unless otherwise specified.

15. **IO CELL:** IO cell information:
    - LVCMOS: The IO buffer receives or drives a standard GPIO signal.
    - BK: This symbol underlines that this IO supports a bus keeper (or bus holder) function. It allows the output buffer to maintain the last state driven by using an internal pullup or pulldown resistor.
    - I^2C Open Drain: The IO buffer outputs an open drain signal. This IO is designed for I^2C function.
    - LVCMOS 3-State Open Drain: That indicates that the IO is a standard LVCMOS buffer that is used in 3-state mode to have an open drain driver.
    - MPHY: This IO supports MIPI M-PHY signals.
    - DPHY: This IO supports MIPI D-PHY signals.
    - Analog: For analog signals.
    - DDR: This IO can support LPDDR2 (for the OMAP5430 device), DDR3 (used in the OMAP5432 device) and HSUL_12 (HSIC) protocols.
    - SATAPHY: This IO supports SATA PHY signals.
    - USB3PHY: This IO supports USB3 PHY signals.
    - HDMIPHY: For IO buffer that supports HDMI PHY signals.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, this pad is actually set undriven (high impedance: Z) with potential pullup/pulldown. Pulls need to be disabled to have a pure high impedance.

NOTE

All balls not described in Table 2-1 are not connected.

Table 2-1. Ball Characteristics(1)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] (2)	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
G26 / G15 / G13 / G8 / H27 / L7 / M7 / W27 / AA27 / AA7 / AC7 / AE27 / AG22 / AG21 / AG14 / AG12 / AG8	-	vdds_1p8	0	PWR	-	-	-	-	-	-	-	-	-	Power
AF7	-	vdds_emmc	0	PWR	-	-	-	-	-	-	-	-	-	Power
AL2	-	emmc_clk	0	O	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_46	6	IO										
		safe_mode	7											
AK4	-	emmc_cmd	0	IO	H	H	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_47	6	IO										
		safe_mode	7											
AK3	-	emmc_data0	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_48	6	IO										
		safe_mode	7											
AJ4	-	emmc_data1	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_49	6	IO										
		safe_mode	7											
AK2	-	emmc_data2	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_50	6	IO										
		safe_mode	7											
AJ3	-	emmc_data3	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_51	6	IO										
		safe_mode	7											
AH2	-	emmc_data4	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_52	6	IO										
		safe_mode	7											
AJ2	-	emmc_data5	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_53	6	IO										
		safe_mode	7											
AH3	-	emmc_data6	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_54	6	IO										
		safe_mode	7											
AH4	-	emmc_data7	0	IO	H	0	0	1.8 V or 1.2 V	vdds_emmc	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpio2_55	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
G21 / G22	-	vdds_c2c	0	PWR	-	-	-	-	-	-	-	-	-	Power
B21	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row0	3	I										
		gpmc_ad0	4	IO										
		gpio2_37	6	IO										
		safe_mode	7											
C21	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row1	3	I										
		gpmc_ad1	4	IO										
		gpio2_38	6	IO										
		safe_mode	7											
B20	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row2	3	I										
		gpmc_ad2	4	IO										
		gpio2_39	6	IO										
		safe_mode	7											
C20	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row3	3	I										
		gpmc_ad3	4	IO										
		gpio2_40	6	IO										
		safe_mode	7											
B19	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row4	3	I										
		gpmc_ad4	4	IO										
		gpio2_41	6	IO										
		safe_mode	7											
C19	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row5	3	I										
		gpmc_ad5	4	IO										
		gpio2_42	6	IO										
		safe_mode	7											
B18	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row6	3	I										
		gpmc_ad6	4	IO										
		gpio2_43	6	IO										
		safe_mode	7											
C18	-	Reserved	0	I	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row7	3	I										
		gpmc_ad7	4	IO										
		gpio2_44	6	IO										
		safe_mode	7											
C22	-	Reserved	0	I	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_row8	3	I										
		gpmc_clk	4	O										
		gpio2_36	6	IO										
		safe_mode	7											
B22	-	Reserved	0	I	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpmc_nwp	4	O										
		gpmc_nbe1	5	O										
		gpio2_35	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
E22	-	Reserved	0	O	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpmc_NAdv_ale	4	O										
		gpio2_33	6	IO										
		safe_mode	7											
D22	-	Reserved	0	O	L	0	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col8	3	O										
		gpmc_nbe0_cle	4	O										
		gpio2_34	6	IO										
		safe_mode	7											
E26	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col0	3	O										
		gpmc_ad8	4	IO										
		hw_dbg16	5	O										
		gpio2_56	6	IO										
		safe_mode	7											
D26	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col1	3	O										
		gpmc_ad9	4	IO										
		hw_dbg17	5	O										
		gpio2_57	6	IO										
		safe_mode	7											
E25	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col2	3	O										
		gpmc_ad10	4	IO										
		hw_dbg18	5	O										
		gpio2_58	6	IO										
		safe_mode	7											
D25	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col3	3	O										
		gpmc_ad11	4	IO										
		hw_dbg19	5	O										
		gpio2_59	6	IO										
		safe_mode	7											
E24	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col4	3	O										
		gpmc_ad12	4	IO										
		hw_dbg20	5	O										
		gpio2_60	6	IO										
		safe_mode	7											
D24	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col5	3	O										
		gpmc_ad13	4	IO										
		hw_dbg21	5	O										
		gpio2_61	6	IO										
		safe_mode	7											
E23	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4[9]	PU/PD	LVCMOS
		kbd_col6	3	O										
		gpmc_ad14	4	IO										
		hw_dbg22	5	O										
		gpio2_62	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] (2)	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
D23	-	Reserved	0	O	L	L	4	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		kbd_col7	3	O										
		gpmc_ad15	4	IO										
		hw_dbg23	5	O										
		gpio2_63	6	IO										
		safe_mode	7											
E21	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a16	4	O										
		hw_dbg24	5	O										
		gpio4_113	6	IO										
		safe_mode	7											
D21	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a17	4	O										
		hw_dbg25	5	O										
		gpio4_114	6	IO										
		safe_mode	7											
E20	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a18	4	O										
		hw_dbg26	5	O										
		gpio4_115	6	IO										
		safe_mode	7											
D20	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a19	4	O										
		hw_dbg27	5	O										
		gpio4_116	6	IO										
		safe_mode	7											
E19	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a20	4	O										
		hw_dbg28	5	O										
		gpio4_117	6	IO										
		safe_mode	7											
D19	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a21	4	O										
		hw_dbg29	5	O										
		gpio4_118	6	IO										
		safe_mode	7											
E18	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a22	4	O										
		hw_dbg30	5	O										
		gpio4_119	6	IO										
		safe_mode	7											
D18	-	Reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_c2c	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_a23	4	O										
		hw_dbg31	5	O										
		gpio4_120	6	IO										
		safe_mode	7											
E29	-	Reserved	0	O	H	1	4	1.8 V or 1.2 V	vdds_ bank25	Yes	Yes	4(9)	PU/PD	LVCMOS
		gpmc_ncs0	4	O										
		gpio2_32	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
C29	-	Reserved	0	O	H	H	4	1.8 V or 1.2 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpmc_wait0	4	I										
		gpio2_45	6	IO										
		safe_mode	7											
E30	-	Reserved	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg13	5	O										
		gpio1_wk15	6	IO										
		safe_mode	7											
C30	-	Reserved	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg14	5	O										
		gpio1_wk14	6	IO										
		safe_mode	7											
G12	-	vdds_bank2	0	PWR	-	-	-	-	-	-	-	-	-	Power
E13	-	hsi1_acready	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		cam_strobe	1	O										
		usbb2_ulpitll_clk	3	O										
		gpio3_64	6	IO										
		safe_mode	7											
E14	-	hsi1_caready	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_nxt	3	O										
		gpio3_65	6	IO										
		safe_mode	7											
D13	-	hsi1_acwake	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_dir	3	O										
		gpio3_66	6	IO										
		safe_mode	7											
E15	-	hsi1_cawake	0	I	H	H	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_stp	3	I										
		gpio3_67	6	IO										
		safe_mode	7											
D15	-	hsi1_acflag	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data0	3	IO										
		gpio3_68	6	IO										
		safe_mode	7											
D14	-	hsi1_acdata	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data1	3	IO										
		gpio3_69	6	IO										
		safe_mode	7											
D12	-	hsi1_caflag	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data2	3	IO										
		gpio3_70	6	IO										
		safe_mode	7											
E12	-	hsi1_cadata	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data3	3	IO										
		gpio3_71	6	IO										
		safe_mode	7											
D10	-	uart1_tx	0	O	H	H	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data4	3	IO										
		gpio3_72	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
E9	-	uart1_cts	0	I	H	H	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data5	3	IO										
		gpmc_wait3	4	I										
		gpio3_73	6	IO										
		safe_mode	7											
D9	-	uart1_rx	0	I	H	H	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data6	3	IO										
		gpio3_74	6	IO										
		safe_mode	7											
E10	-	uart1_rts	0	O	H	H	7	1.8 V or 1.2 V	vdds_bank2	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb2_ulpitll_data7	3	IO										
		gpmc_ncs7	4	O										
		gpio3_75	6	IO										
		safe_mode	7											
G10	-	vdds_bank4	0	PWR	-	-	-	-	-	-	-	-	-	Power
C7	-	hsi2_caready	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_clk	3	I										
		gpmc_wait1	4	I										
		gpio3_76	6	IO										
		safe_mode	7											
C10	-	hsi2_acready	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_nxt	3	I										
		gpmc_ncs1[14]	4	O										
		gpio3_77	6	IO										
		safe_mode	7											
B8	-	hsi2_cawake	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_dir	3	I										
		gpmc_a24	4	O										
		gpio3_78	6	IO										
		safe_mode	7											
C8	-	hsi2_acwake	0	O	H	H	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_stp	3	O										
		gpmc_a25	4	O										
		gpio3_79	6	IO										
		safe_mode	7											
B7	-	hsi2_caflag	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_ data0	3	IO										
		gpmc_wait2	4	I										
		gpio3_80	6	IO										
		safe_mode	7											
B10	-	hsi2_cadata	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_ data1	3	IO										
		gpmc_ncs2[14]	4	O										
		gpio3_81	6	IO										
		safe_mode	7											
B9	-	hsi2_acflag	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_ data2	3	IO										
		gpmc_ncs3[14]	4	O										
		gpio3_82	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
C9	-	hsi2_acdata	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbb1_ulpiphy_data3	3	IO										
		gpmc_ncs4[14]	4	O										
		gpio3_83	6	IO										
		safe_mode	7											
C5	-	uart2_rts	0	O	H	1	4	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi3_somi	1	IO										
		usbb1_ulpiphy_data4	3	IO										
		gpmc_nwe	4	O										
		hw_dbg16	5	O										
		gpio3_84	6	IO										
		safe_mode	7											
B5	-	uart2_cts	0	I	H	1	4	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi3_cs0	1	IO										
		usbb1_ulpiphy_data5	3	IO										
		gpmc_noe_nre	4	O										
		hw_dbg17	5	O										
		gpio3_85	6	IO										
		safe_mode	7											
C6	-	uart2_rx	0	I	H	H	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi3_simo	1	IO										
		usbb1_ulpiphy_data6	3	IO										
		gpmc_ncs5	4	O										
		hw_dbg18	5	O										
		gpio3_86	6	IO										
		safe_mode	7											
B6	-	uart2_tx	0	O	H	H	7	1.8 V or 1.2 V	vdds_bank4	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi3_clk	1	IO										
		usbb1_ulpiphy_data7	3	IO										
		gpmc_ncs6	4	O										
		hw_dbg19	5	O										
		gpio3_87	6	IO										
		safe_mode	7											
G23	-	vdds_hsic	0	PWR	-	-	-	-	-	-	-	-	-	Power
B26	-	usbb1_hsic_strobe	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
		gpio3_92	6	IO										
		safe_mode	7											
C26	-	usbb1_hsic_data	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
		gpio3_93	6	IO										
		safe_mode	7											
B25	-	usbb2_hsic_strobe	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
		gpio3_94	6	IO										
		safe_mode	7											
C25	-	usbb2_hsic_data	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
		gpio3_95	6	IO										
		safe_mode	7											
Y27	-	vdds_bank5	0	PWR	-	-	-	-	-	-	-	-	-	-
V30	-	timer10_pwm_evt	0	IO	L	L	7	1.8 V or 1.5 V	vdds_bank5	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio6_188	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
W30	-	dsiporta_te0	0	I	L	L	7	1.8 V or 1.5 V	vdds_bank5	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio6_189	6	IO										
		safe_mode	7											
AA32	-	vdda_dsiporta[13]	0	PWR	-	-	-	-	-	-	-	-	-	-
W33	-	vssa_dsiporta	0	GND	-	-	-	-	-	-	-	-	-	-
Y32	-	dsiporta_lane0x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
Y31	-	dsiporta_lane0y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
W32	-	dsiporta_lane1x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
W31	-	dsiporta_lane1y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
V32	-	dsiporta_lane2x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
V31	-	dsiporta_lane2y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
T32	-	dsiporta_lane3x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
T31	-	dsiporta_lane3y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
R32	-	dsiporta_lane4x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
R31	-	dsiporta_lane4y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiporta[13]	No	No	See [16]	No	DPHY
AC29	-	timer9_pwm_evt	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank5	Yes	Yes	4[9]	PU/PD	LVCMOS
		sync_sof_clk	1	O										
		sync_usof_itp_clk	2	O										
		gpio6_190	6	IO										
		safe_mode	7											
AB29	-	dsiportc_te0	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank5	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio6_191	6	IO										
		safe_mode	7											
AA31	-	vdda_dsiportc[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
AB33	-	vssa_dsiportc	0	GND	-	-	-	-	-	-	-	-	-	Power
AF32	-	dsiportc_lane0x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AF31	-	dsiportc_lane0y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AE32	-	dsiportc_lane1x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AE31	-	dsiportc_lane1y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AD32	-	dsiportc_lane2x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AD31	-	dsiportc_lane2y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AC32	-	dsiportc_lane3x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AC31	-	dsiportc_lane3y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AB32	-	dsiportc_lane4x	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AB31	-	dsiportc_lane4y	0	ODS	0	L	0	1.8 V or 1.5 V	vdda_dsiportc[13]	No	No	See [16]	No	DPHY
AG9 / AG11	-	vdds_bank9	0	PWR	-	-	-	-	-	-	-	-	-	Power
AK7	-	rfbi_hsync0	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data17	3	O										
		kbd_col5	4	O										
		gpio6_160	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AJ7	-	rfbi_te_vsync0	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data16	3	O										
		kbd_row5	4	I										
		jtag_sel	5	I										
		gpio6_161	6	IO										
		safe_mode	7											
AK9	-	rfbi_re	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_pclk	3	O										
		kbd_col4	4	O										
		gpio6_164	6	IO										
		safe_mode	7											
AM5	-	rfbi_a0	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_de	3	O										
		kbd_row4	4	I										
		gpio6_165	6	IO										
		safe_mode	7											
AK5	-	rfbi_data8	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data8	3	O										
		kbd_col3	4	O										
		drm_emu12	5	O										
		gpio6_174	6	IO										
		safe_mode	7											
AJ5	-	rfbi_data9	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data9	3	O										
		kbd_row3	4	I										
		drm_emu13	5	O										
		gpio6_175	6	IO										
		safe_mode	7											
AL5	-	rfbi_data10	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data10	3	O										
		kbd_row8	4	I										
		drm_emu14	5	O										
		gpio6_176	6	IO										
		safe_mode	7											
AL6	-	rfbi_data11	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data11	3	O										
		kbd_row7	4	I										
		drm_emu15	5	O										
		gpio6_177	6	IO										
		safe_mode	7											
AJ8	-	rfbi_data12	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data12	3	O										
		kbd_row6	4	I										
		drm_emu16	5	O										
		gpio6_178	6	IO										
		safe_mode	7											
AM9	-	rfbi_data13	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data13	3	O										
		kbd_col8	4	O										
		drm_emu17	5	O										
		gpio6_179	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AL9	-	rfbi_data14	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data14	3	O										
		kbd_col7	4	O										
		drm_emu18	5	O										
		gpio6_180	6	IO										
		safe_mode	7											
AJ9	-	rfbi_data15	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi2_cs1	1	O										
		dispc_data15	3	O										
		kbd_col6	4	O										
		drm_emu19	5	O										
		gpio6_181	6	IO										
		safe_mode	7											
AJ10	-	gpio6_182[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data18	3	O										
		kbd_col0	4	O										
		gpio6_182[11]	6	IO										
		safe_mode	7											
AK10	-	gpio6_183[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data19	3	O										
		kbd_col1	4	O										
		gpio6_183[11]	6	IO										
		safe_mode	7											
AJ11	-	gpio6_184[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data20	3	O										
		kbd_col2	4	O										
		hw_dbg22	5	O										
		gpio6_184[11]	6	IO										
		safe_mode	7											
AK11	-	gpio6_185[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data21	3	O										
		kbd_row0	4	I										
		hw_dbg23	5	O										
		gpio6_185[11]	6	IO										
		safe_mode	7											
AJ12	-	gpio6_186[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data22	3	O										
		kbd_row1	4	I										
		hw_dbg24	5	O										
		gpio6_186[11]	6	IO										
		safe_mode	7											
AK12	-	gpio6_187[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data23	3	O										
		kbd_row2	4	I										
		hw_dbg25	5	O										
		gpio6_187[11]	6	IO										
		safe_mode	7											
AM6	-	rfbi_data0	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data0	3	O										
		jtagtapext_rtck	4	I										
		drm_emu4	5	O										
		gpio6_166	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AL7	-	rfbi_data1	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data1	3	O										
		uart3_rx_irrx	4	I										
		drm_emu5	5	O										
		gpio6_167	6	IO										
		safe_mode	7											
AJ6	-	rfbi_data2	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data2	3	O										
		uart3_tx_irtx	4	O										
		drm_emu6	5	O										
		gpio6_168	6	IO										
		safe_mode	7											
AM7	-	rfbi_data3	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data3	3	O										
		jtagtapext_ntrst	4	O										
		drm_emu7	5	O										
		gpio6_169	6	IO										
		safe_mode	7											
AM8	-	rfbi_data4	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data4	3	O										
		jtagtapext_tck	4	O										
		drm_emu8	5	O										
		gpio6_170	6	IO										
		safe_mode	7											
AL8	-	rfbi_data5	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data5	3	O										
		jtagtapext_tmsc	4	O										
		drm_emu9	5	O										
		gpio6_171	6	IO										
		safe_mode	7											
AM10	-	rfbi_data6	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data6	3	O										
		jtagtapext_tdo	4	O										
		drm_emu10	5	O										
		gpio6_172	6	IO										
		safe_mode	7											
AL10	-	rfbi_data7	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_data7	3	O										
		jtagtapext_tdi	4	I										
		drm_emu11	5	O										
		gpio6_173	6	IO										
		safe_mode	7											
AK6	-	rfbi_cs0	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_hsync	3	O										
		drm_emu3	5	O										
		gpio6_163	6	IO										
		safe_mode	7											
AK8	-	rfbi_we	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank9	Yes	Yes	4[9]	PU/PD	LVCMOS
		dispc_vsync	3	O										
		drm_emu2	5	O										
		gpio6_162	6	IO										
		safe_mode	7											
AG20	-	vdds_bank8	0	PWR	-	-	-	-	-	-	-	-	-	Power

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AK20	-	mcspi2_cs0	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank8	Yes	Yes	4[9]	PU/PD	LVCMOS
		jtagtapext_ntrst	1	O										
		dispc_fid	3	O										
		gpio7_196	6	IO										
		safe_mode	7											
AK21	-	mcspi2_clk	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank8	Yes	Yes	4[9]	PU/PD	LVCMOS
		jtagtapext_tck	1	O										
		gpio7_197	6	IO										
		safe_mode	7											
AJ18	-	mcspi2_simo	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank8	Yes	Yes	4[9]	PU/PD	LVCMOS
		jtagtapext_tmsc	1	O										
		hw_dbg20	5	O										
		gpio7_198	6	IO										
		safe_mode	7											
AK23	-	mcspi2_somi	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank8	Yes	Yes	4[9]	PU/PD	LVCMOS
		jtagtapext_tdo	1	O										
		hw_dbg21	5	O										
		gpio7_199	6	IO										
		safe_mode	7											
AK22	-	i2c4_scl	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_bank8	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I²C Open Drain
		jtagtapext_tdi	1	I										
		gpio7_200	6	IO								4		
		safe_mode	7									4		
AJ20	-	i2c4_sda	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_bank8	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I²C Open Drain
		jtagtapext_rtck	1	I										
		gpio7_201	6	IO								4		
		safe_mode	7									4		
AG24	-	vdds_hdmi	0	PWR	-	-	-	-	-	-	-	-	-	Power
AK25	-	hdmi_cec	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_hdmi	Yes	Yes	4[9]	PU/PD	LVCMOS Tri-State Open Drain
		gpio7_192	6	IO										
		safe_mode	7											
AJ25	-	hdmi_hpd	0	I	L	L	7	1.8 V or 1.2 V	vdds_hdmi	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio7_193	6	IO										
		safe_mode	7											
AK24	-	hdmi_ddc_scl	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_hdmi	Yes	No	3	PUx/ PDy-OD[4]	LVCMOS I²C Open Drain
		gpio7_194	6	IO								4		
		safe_mode	7									4		
AJ24	-	hdmi_ddc_sda	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_hdmi	Yes	No	3	PUx/ PDy-OD[4]	LVCMOS I²C Open Drain
		gpio7_195	6	IO								4		
		safe_mode	7									4		
AM27	-	vdda_hdmi[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
AN27	-	vssa_hdmi	0	GND	-	-	-	-	-	-	-	-	-	Power
AM23	-	hdmi_clkx	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY
AL23	-	hdmi_clky	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY
AM24	-	hdmi_data0x	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY
AL24	-	hdmi_data0y	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY
AM25	-	hdmi_data1x	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY
AL25	-	hdmi_data1y	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY
AM26	-	hdmi_data2x	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi [13]	No	No	10	PDy[5]	HDMIPHY

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] (2)	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AL26	-	hdmi_data2y	0	ODS	Z	Z	0	1.8 V or 1.5 V	vdda_hdmi (13)	No	No	10	PDy(5)	HDMIPHY
T2	-	vdda_csiporta(13)	0	PWR	-	-	-	-	-	-	-	-	-	Power
N4	-	vssa_csiporta	0	GND	-	-	-	-	-	-	-	-	-	Power
R2	-	csiporta_lane0x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_pclk	3	I										
		gpio8_in236	6	I										
		safe_mode	7											
R3	-	csiporta_lane0y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_wen	3	I										
		gpio8_in237	6	I										
		safe_mode	7											
P3	-	csiporta_lane1y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data0	3	I										
		gpio8_in238	6	I										
		safe_mode	7											
P2	-	csiporta_lane1x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data1	3	I										
		gpio8_in239	6	I										
		safe_mode	7											
N3	-	csiporta_lane2y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data2	3	I										
		gpio8_in240	6	I										
		safe_mode	7											
N2	-	csiporta_lane2x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data3	3	I										
		gpio8_in241	6	I										
		safe_mode	7											
M2	-	csiporta_lane3x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data4	3	I										
		gpio8_in242	6	I										
		safe_mode	7											
M3	-	csiporta_lane3y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data5	3	I										
		gpio8_in243	6	I										
		safe_mode	7											
L2	-	csiporta_lane4x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data6	3	I										
		gpio8_in244	6	I										
		safe_mode	7											
L3	-	csiporta_lane4y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiporta(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data7	3	I										
		gpio8_in245	6	I										
		safe_mode	7											
T3	-	vdda_csiportb(13)	0	PWR	-	-	-	-	-	-	-	-	-	Power
V4	-	vssa_csiportb	0	GND	-	-	-	-	-	-	-	-	-	Power
V3	-	csiportb_lane0x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiportb(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data12	4	I										
		gpio8_in246	6	I										
		safe_mode	7											
V2	-	csiportb_lane0y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_csiportb(13)	Yes	No	NA	PU/PD	DPHY
		cpi_data13	4	I										
		gpio8_in247	6	I										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
W2	-	csiportb_lane1y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb[13]	Yes	No	NA	PU/PD	DPHY
		cpi_data14	4	I										
		gpio8_in248	6	I										
		safe_mode	7											
W3	-	csiportb_lane1x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb[13]	Yes	No	NA	PU/PD	DPHY
		cpi_data15	4	I										
		gpio8_in249	6	I										
		safe_mode	7											
Y2	-	csiportb_lane2y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb[13]	Yes	No	NA	PU/PD	DPHY
		cpi_hsyncin	4	I										
		gpio8_in250	6	I										
		safe_mode	7											
Y3	-	csiportb_lane2x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportb[13]	Yes	No	NA	PU/PD	DPHY
		cpi_vsyncin	4	I										
		gpio8_in251	6	I										
		safe_mode	7											
H3	-	vdda_csiportc[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
H2	-	vssa_csiportc	0	GND	-	-	-	-	-	-	-	-	-	Power
K3	-	csiportc_lane0y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc[13]	Yes	No	NA	PU/PD	DPHY
		cpi_data8	3	I										
		gpio8_in252	6	I										
		safe_mode	7											
K2	-	csiportc_lane0x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc[13]	Yes	No	NA	PU/PD	DPHY
		cpi_data9	3	I										
		gpio8_in253	6	I										
		safe_mode	7											
J3	-	csiportc_lane1y	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc[13]	Yes	No	NA	PU/PD	DPHY
		cpi_data10	3	I										
		gpio8_in254	6	I										
		safe_mode	7											
J2	-	csiportc_lane1x	0	IDS	L	L	7	1.8 V or 1.5 V	vdda_ csiportc[13]	Yes	No	NA	PU/PD	DPHY
		cpi_data11	3	I										
		gpio8_in255	6	I										
		safe_mode	7											
W5	-	vdds_bank10	0	PWR	-	-	-	-	-	-	-	-	-	Power
AD3	-	cam_shutter	0	IO	Z	Z	5	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_nodeid0	5	I										
		gpio8_224	6	IO										
		safe_mode	7											
AD4	-	cam_strobe	0	O	Z	Z	5	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_nodeid1	5	I										
		gpio8_225	6	IO										
		safe_mode	7											
AD2	-	cam_globalreset	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		cam_shutter	1	O										
		cpi_fid	3	I										
		gpio8_226	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AF3	-	timer11_pwm_evt	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		uart1_tx	2	O										
		cpi_data12	3	I										
		hw_dbg26	5	O										
		gpio8_227	6	IO										
		safe_mode	7											
AF2	-	timer5_pwm_evt	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdcard_cd	1	I										
		uart1_cts	2	I										
		cpi_data13	3	I										
		gpio8_228	6	IO										
		safe_mode	7											
AE3	-	timer6_pwm_evt	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdcard_wp	1	I										
		uart1_rx	2	I										
		cpi_data14	3	I										
		gpio8_229	6	IO										
		safe_mode	7											
AE2	-	timer8_pwm_evt	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdcard_wp	1	I										
		uart1_rts	2	O										
		cpi_data15	3	I										
		hw_dbg27	5	O										
		gpio8_230	6	IO										
		safe_mode	7											
AB3	-	i2c3_scl	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_ bank10	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I^2C Open Drain
		gpio8_231	6	IO								4		
		safe_mode	7									4		
AB2	-	i2c3_sda	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_ bank10	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I^2C Open Drain
		gpio8_232	6	IO								4		
		safe_mode	7									4		
AC2	-	gpio8_233[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_secure_ indicator	1	O										
		timer8_pwm_evt	2	IO										
		cpi_hsync	3	IO										
		gpio8_233[11]	6	IO										
		safe_mode	7											
AC3	-	gpio8_234[11]	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank10	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_drm_msecure	1	O										
		cpi_vsync	3	IO										
		gpio8_234[11]	6	IO										
		safe_mode	7											
P27	-	vdds_bank11	0	PWR	-	-	-	-	-	-	-	-	-	Power
N30	-	abe_clks	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank11	Yes	Yes	4[9]	PU/PD	LVCMOS
		abemcasp_axr	3	IO										
		gpio4_96	6	IO										
		safe_mode	7											
R30	-	abedmic_din1	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank11	Yes	Yes	4[9]	PU/PD	LVCMOS
		abemcasp_ahclkr	3	IO										
		abemcbsp3_fsx	4	IO										
		gpio4_97	6	IO										
		safe_mode	7											
R27	-	vdds_bank12	0	PWR	-	-	-	-	-	-	-	-	-	Power

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] (2)	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
P32	-	abedmic_din2	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank12	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcasp_axr	3	IO										
		abemcbsp3_dx	4	O										
		gpio4_98	6	IO										
		safe_mode	7											
P31	-	abedmic_din3	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank12	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcbsp3_dr	4	I										
		gpio4_99	6	IO										
		safe_mode	7											
P29	-	abedmic_clk1	0	O	L	L	7	1.8 V or 1.2 V	vdds_ bank12	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcbsp3_clkx	4	IO										
		gpio4_100	6	IO										
		safe_mode	7											
P30	-	abedmic_clk2	0	O	L	L	7	1.8 V or 1.2 V	vdds_ bank12	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcbsp1_fsx	1	IO										
		abemcasp_amutein	3	I										
		gpio4_101	6	IO										
		safe_mode	7											
N29	-	abedmic_clk3	0	O	L	L	7	1.8 V or 1.2 V	vdds_ bank12	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcbsp1_dx	1	O										
		abemcasp_aclkx	3	IO										
		gpio4_102	6	IO										
		safe_mode	7											
R29	-	vdds_bank14	0	PWR	-	-	-	-	-	-	-	-	-	Power
T30	-	reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank14	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcbsp1_clkx	1	IO										
		abemcasp_afsr	3	IO										
		gpio4_103	6	IO										
		safe_mode	7											
T29	-	reserved	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank14	Yes	Yes	4(9)	PU/PD	LVCMOS BK
		abemcbsp1_dr	1	I										
		abemcasp_aclkr	3	IO										
		gpio4_104	6	IO										
		safe_mode	7											
N31	-	abemcbsp2_dr	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank11	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcasp_axr	3	IO										
		gpio4_105	6	IO										
		safe_mode	7											
N32	-	abemcbsp2_dx	0	O	L	L	7	1.8 V or 1.2 V	vdds_ bank11	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcasp_ amuteout	3	O										
		gpio4_106	6	IO										
		safe_mode	7											
M31	-	abemcbsp2_fsx	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank11	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcasp_afsx	3	IO										
		gpio4_107	6	IO										
		safe_mode	7											
M32	-	abemcbsp2_clkx	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank11	Yes	Yes	4(9)	PU/PD	LVCMOS
		abemcasp_ahclkx	3	IO										
		gpio4_108	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
M29	-	abemcpdm_ul_data	0	I	L	L	7	1.8 V or 1.2 V	vdds_bank11	Yes	Yes	4[9]	PU/PD	LVCMOS
		abemcbsp3_dr	1	I										
		abemcasp_axr3	3	IO										
		gpio4_109	6	IO										
		safe_mode	7											
M30	-	abemcpdm_dl_data	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank11	Yes	Yes	4[9]	PU/PD	LVCMOS
		abemcbsp3_dx	1	O										
		abemcasp_axr2	3	IO										
		gpio4_110	6	IO										
		safe_mode	7											
L30	-	abemcpdm_frame	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank11	Yes	Yes	4[9]	PU/PD	LVCMOS
		abemcbsp3_clkx	1	IO										
		abemcasp_axr1	3	IO										
		gpio4_111	6	IO										
		safe_mode	7											
L29	-	abemcpdm_lb_clk	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank11	Yes	Yes	4[9]	PU/PD	LVCMOS
		abemcbsp3_fsx	1	IO										
		gpio4_112	6	IO										
		safe_mode	7											
AG25	-	vdds_bank15	0	PWR	-	-	-	-	-	-	-	-	-	Power
AK29	-	wlsdio_clk	0	O	L	L	7	1.8 V or 1.2 V	vdds_bank15	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi4_clk	1	IO										
		gpio5_128	6	IO										
		safe_mode	7											
AJ29	-	wlsdio_cmd	0	IO	L	L	7	1.8 V or 1.2 V	vdds_bank15	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio5_129	6	IO										
		safe_mode	7											
AJ30	-	wlsdio_data0	0	IO	H	H	7	1.8 V or 1.2 V	vdds_bank15	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi4_simo	1	IO										
		gpio5_130	6	IO										
		safe_mode	7											
AK30	-	wlsdio_data1	0	IO	H	H	7	1.8 V or 1.2 V	vdds_bank15	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi4_somi	1	IO										
		gpio5_131	6	IO										
		safe_mode	7											
AJ31	-	wlsdio_data2	0	IO	H	H	7	1.8 V or 1.2 V	vdds_bank15	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi4_cs0	1	IO										
		gpio5_132	6	IO										
		safe_mode	7											
AK31	-	wlsdio_data3	0	IO	H	H	7	1.8 V or 1.2 V	vdds_bank15	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio5_133	6	IO										
		safe_mode	7											
AD27	-	vdds_bank16	0	PWR	-	-	-	-	-	-	-	-	-	Power
AD30	-	uart5_rx	0	I	H	H	7	1.8 V or 1.2 V	vdds_bank16	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio4_data1	4	IO										
		hw_dbg28	5	O										
		gpio5_134	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AE29	-	uart5_tx	0	O	H	H	7	1.8 V or 1.2 V	vdds_ bank16	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio4_data2	4	IO										
		hw_dbg29	5	O										
		gpio5_135	6	IO										
		safe_mode	7											
AE30	-	uart5_cts	0	I	H	H	7	1.8 V or 1.2 V	vdds_ bank16	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio4_data0	4	IO										
		hw_dbg30	5	O										
		gpio5_136	6	IO										
		safe_mode	7											
AD29	-	uart5_rts	0	O	H	H	7	1.8 V or 1.2 V	vdds_ bank16	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio4_data3	4	IO										
		hw_dbg31	5	O										
		gpio5_137	6	IO										
		safe_mode	7											
AF30	-	i2c2_scl	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_ bank16	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I^2C Open Drain
		gpio5_138	6	IO								4		
		safe_mode	7									4		
AF29	-	i2c2_sda	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_ bank16	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I^2C Open Drain
		gpio5_139	6	IO								4		
		safe_mode	7									4		
AF27	-	vdds_bank18	0	PWR	-	-	-	-	-	-	-	-	-	Power
AH32	-	mcspi1_clk	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank18	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbd0_ulpiphy_clk	5	I										
		gpio5_140	6	IO										
		safe_mode	7											
AG32	-	mcspi1_somi	0	I	L	L	7	1.8 V or 1.2 V	vdds_ bank18	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbd0_ulpiphy_nxt	5	I										
		gpio5_141	6	IO										
		safe_mode	7											
AH31	-	mcspi1_simo	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank18	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbd0_ulpiphy_dir	5	I										
		gpio5_142	6	IO										
		safe_mode	7											
AG31	-	mcspi1_cs0	0	O	L	L	7	1.8 V or 1.2 V	vdds_ bank18	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbd0_ulpiphy_ data0	5	IO										
		gpio5_143	6	IO										
		safe_mode	7											
AH30	-	mcspi1_cs1	0	O	L	L	7	1.8 V or 1.2 V	vdds_ bank18	Yes	Yes	4[9]	PU/PD	LVCMOS
		usbd0_ulpiphy_ data1	5	IO										
		gpio5_144	6	IO										
		safe_mode	7											
AL32	-	i2c5_scl	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_ bank18	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I^2C Open Drain
		uart4_rx	2	I								4		
		gpio5_147	6	IO								4		
		safe_mode	7									4		
AL31	-	i2c5_sda	0	IOD	H	H	7	1.8 V or 1.2 V	vdds_ bank18	Yes	No	3	PUx/ PDy-GPIO[4]	LVCMOS I^2C Open Drain
		uart4_tx	2	O								4		
		gpio5_148	6	IO								4		
		safe_mode	7									4		
AG27	-	vdds_bank19	0	PWR	-	-	-	-	-	-	-	-	-	Power

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AJ32	-	gpio5_145	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank19	Yes	Yes	4[9]	PU/PD	LVCMOS
		mcspi1_cs2	1	O										
		uart4_cts	2	I										
		sdio5_clk	3	O										
		usbd0_ulpiphy_ data2	5	IO										
		gpio5_145	6	IO										
		safe_mode	7											
AK32	-	gpio5_146	0	IO	L	L	7	1.8 V or 1.2 V	vdds_ bank19	Yes	Yes	4[9]	PU/PD	LVCMOS BK
		mcspi1_cs3	1	O										
		uart4_rts	2	O										
		sdio5_cmd	3	IO										
		usbd0_ulpiphy_ data3	5	IO										
		gpio5_146	6	IO										
		safe_mode	7											
AG26	-	vdds_bank21	0	PWR	-	-	-	-	-	-	-	-	-	Power
AJ27	-	uart6_tx	0	O	H	H	7	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio5_data3	3	IO										
		usbb2_mm_rxdp	4	IO										
		gpio5_149	6	IO										
		safe_mode	7											
AJ26	-	uart6_rx	0	I	H	H	7	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio5_data2	3	IO										
		usbb2_mm_rxdm	4	IO										
		gpio5_150	6	IO										
		safe_mode	7											
AK26	-	uart6_cts	0	I	H	H	7	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_ndmareq1	1	I										
		sdio5_data1	3	IO										
		usbb2_mm_rxrcv	4	IO										
		gpio5_151	6	IO										
		safe_mode	7											
AK27	-	uart6_rts	0	O	H	H	7	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_ndmareq0	1	I										
		sdio5_data0	3	IO										
		usbb2_mm_txse0	4	IO										
		usbd0_ulpiphy_stp	5	O										
		gpio5_152	6	IO										
		safe_mode	7											
AJ28	-	uart3_cts_rctx	0	IO	H	H	7	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sata_actled	1	O										
		sdio5_data7	3	IO										
		usbb2_mm_txen	4	IO										
		usbd0_ulpiphy_ data4	5	IO										
		gpio5_153	6	IO										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
AK28	-	uart3_rts_irsd	0	O	H	H	7	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS Tri-State Open Drain
		hdq_sio	1	IOD										
		sdio5_data6	3	IO										
		usbb2_mm_txdat	4	IO										
		usbd0_ulpiphy_ data5	5	IO										
		gpio5_154	6	IO										
		safe_mode	7											
AL28	-	uart3_tx_irtx	0	O	H	H	0	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio5_data5	3	IO										
		sdio4_clk	4	O										
		usbd0_ulpiphy_ data6	5	IO										
		gpio5_155	6	IO										
		safe_mode	7											
AM28	-	uart3_rx_irrx	0	I	H	H	0	1.8 V or 1.2 V	vdds_ bank21	Yes	Yes	4[9]	PU/PD	LVCMOS
		sdio5_data4	3	IO										
		sdio4_cmd	4	IO										
		usbd0_ulpiphy_ data7	5	IO										
		gpio5_156	6	IO										
		safe_mode	7											
D29	-	usbb3_hsic_strobe	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
		gpio5_158	6	IO										
		safe_mode	7											
D30	-	usbb3_hsic_data	0	IO	L	L	7	1.2 V	vdds_hsic	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
		gpio5_159	6	IO										
		safe_mode	7											
E8	-	vdda_sata[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
D8	-	vssa_sata	0	GND	-	-	-	-	-	-	-	-	-	Power
E6	-	sata_tx	0	ODS	Z	Z	0	1.8 V	vdda_sata [13]	No	No	3	No	SATAPHY
D6	-	sata_ty	0	ODS	Z	Z	0	1.8 V	vdda_sata [13]	No	No	3	No	SATAPHY
E7	-	sata_rx	0	IDS	Z	Z	0	1.8 V	vdda_sata [13]	No	No	NA	NA	SATAPHY
D7	-	sata_ry	0	IDS	Z	Z	0	1.8 V	vdda_sata [13]	No	No	NA	NA	SATAPHY
K7	-	vdds_sdcard[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
E3	-	sdcard_clk[14]	0	O	L	L	0	3.0 V or 1.8 V	vdds_ sdcard[13]	Yes	See [10]	2[10]	PUx/ PDy[6]	LVCMOS SDCARD
		jtag_rtck	3	O										
		n_clk	5	O										
		safe_mode	7											
E2	-	sdcard_cmd[14]	0	IO	L	L	0	3.0 V or 1.8 V	vdds_ sdcard[13]	Yes	See [10]	2[10]	PUx/ PDy[6]	LVCMOS SDCARD
		jtag_tdo	3	O										
		uart6_rx	4	I										
		drm_emu4	5	O										
		n_d2	6	O										
		safe_mode	7											
G3	-	sdcard_data0[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_ sdcard[13]	Yes	See [10]	2[10]	PUx/ PDy[6]	LVCMOS SDCARD
		jtag_tdi	3	I										
		n_d0	5	O										
		safe_mode	7											

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
G2	-	sdcard_data1[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_sdcard[13]	Yes	See [10]	2[10]	PUx/ PDy[6]	LVCMOS SDCARD
		jtag_ntrst	3	I										
		n_d1	5	O										
		safe_mode	7											
F2	-	sdcard_data2[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_sdcard[13]	Yes	See [10]	2[10]	PUx/ PDy[6]	LVCMOS SDCARD
		jtag_tmsc	3	IO										
		n_d2	5	O										
		safe_mode	7											
F3	-	sdcard_data3[14]	0	IO	L	0	0	3.0 V or 1.8 V	vdds_sdcard[13]	Yes	See [10]	2[10]	PUx/ PDy[6]	LVCMOS SDCARD
		jtag_tck	3	I										
		n_d3	5	O										
		safe_mode	7											
AK18	-	vdds_usbhs18[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
AN22	-	vdda_usbhs33[13]	0	PWR	-	-	-	-	-	-	-	-	-	Power
AM19	-	vssa_usbhs	0	GND	-	-	-	-	-	-	-	-	-	Power
AM20	-	usbd0_hs_dp	0	IODS	H	H	0	3.3 V	vdda_usbhs33[13]	No	No	See [17]	See [18]	USB2PHY
		uart3_rx_irrx	4	I										
		safe_mode	7											
AL20	-	usbd0_hs_dm	0	IODS	L	L	0	3.3 V	vdda_usbhs33[13]	No	No	See [17]	See [18]	USB2PHY
		uart3_tx_irtx	4	O										
		safe_mode	7											
AL19	-	usbphy_ce	0	O	0	Z	0	3.3 V	vdda_usbhs33[13]	No	No	See [17]	NA	USB2PHY
AL18	-	vdda_usbss18[13]	0	PWR	-	-	-	-	-	-	-	-		Power
AM18	-	vssa_usbss	0	GND	-	-	-	-	-	-	-	-		Power
AM21	-	usbd0_ss_tx	0	ODS	Z	Z	0	1.8 V	vdda_usbss18[13]	No	No	5	No	USB3PHY
AL21	-	usbd0_ss_ty	0	ODS	Z	Z	0	1.8 V	vdda_usbss18[13]	No	No	5	No	USB3PHY
AM22	-	usbd0_ss_rx	0	IDS	Z	Z	0	1.8 V	vdda_usbss18[13]	No	No	NA	NA	USB3PHY
AL22	-	usbd0_ss_ry	0	IDS	Z	Z	0	1.8 V	vdda_usbss18[13]	No	No	NA	NA	USB3PHY
G27	-	vdds_bank23	0	PWR	-	-	-	-	-	-	-	-	-	Power
B30	-	drm_emu0	0	IO	H	H	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg6	5	O										
		gpio1_wk6	6	IO										
		safe_mode	7											
B31	-	drm_emu1	0	IO	H	H	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg7	5	O										
		gpio1_wk7	6	IO										
		safe_mode	7											
C32	-	jtag_ntrst	0	I	L	L	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		safe_mode	7											
C31	-	jtag_tck	0	I	L	L	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		safe_mode	7											
A33	-	jtag_rtck	0	O	L	L	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		safe_mode	7											
B32	-	jtag_tmsc	0	IO	H	H	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS BK
		safe_mode	7											
A32	-	jtag_tdi	0	I	H	H	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		safe_mode	7											
B33	-	jtag_tdo	0	O	H	H	0	1.8 V	vdds_bank23	Yes	Yes	4[9]	PU/PD	LVCMOS
		safe_mode	7											
J27	-	vdds_bank24	0	PWR	-	-	-	-	-	-	-	-	-	Power

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
F32	-	sys_32k	0	I	Z	Z	0	1.8 V	vdds_ bank24	Yes	Yes	4[9]	PU/PD	LVCMOS
C27	-	vdds_osc	0	PWR	-	-	-	-	-	-	-	-	-	Power
E31	-	vssa_xtal	0	GND	-	-	-	-	-	-	-	-	-	Power
E32	-	fref_xtal_in	0	AI	Z	Z	0	1.8 V	vdds_osc	Yes	No	NA	No	LVCMOS OSC
D32	-	fref_xtal_out	0	AO	Z	NA	0	1.8 V	vdds_osc	Yes	No	NA	No	OSC
D31	-	fref_xtal_clk	0	AO	0	Z	0	1.8 V	vdds_osc	Yes	No	NA	No	LVCMOS OSC
B27	-	vdda_slicer	0	PWR	-	-	-	-	-	-	-	-	-	Power
A27	-	vssa_slicer	0	GND	-	-	-	-	-	-	-	-	-	Power
B28	-	fref_slicer_in	0	AI	Z	Z	0	No	vdda_slicer	No	No	NA	No	LVCMOS SLICER
H32	-	fref_clk_ioreq	0	IO	L	L	0	1.8 V	vdds_ bank24	Yes	Yes	4[9]	PU/PD	LVCMOS
		gpio1_wk13	6	IO										
		safe_mode	7											
F30	-	fref_clk0_out	0	O	L	0	0	1.8 V	vdds_ bank24	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg9	5	O										
		gpio1_wk12	6	IO										
		safe_mode	7											
K27	-	vdds_bank25	0	PWR	-	-	-	-	-	-	-	-	-	Power
G32	-	fref_clk1_out	0	O	L	L	7	1.2 V or 1.8 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg5	5	O										
		gpio1_wk11	6	IO										
		safe_mode	7											
G31	-	fref_clk2_out	0	O	L	L	7	1.2 V or 1.8 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg10	5	O										
		gpio1_wk10	6	IO										
		safe_mode	7											
G29	-	fref_clk2_req	0	I	L	L	7	1.2 V or 1.8 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		fref_clk3_out	1	O										
		sys_ndmareq0	3	I										
		hw_wkdbg11	5	O										
		gpio1_wk9	6	IO										
		safe_mode	7											
G30	-	fref_clk1_req	0	I	L	L	7	1.2 V or 1.8 V	vdds_ bank25	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_ndmareq1	3	I										
		hw_wkdbg12	5	O										
		gpio1_wk8	6	IO										
		safe_mode	7											
F31	-	sys_nrespwron	0	I	Z	Z	0	1.8 V	vdds_ bank24	Yes	Yes	4	PUx/ PDy[7]	LVCMOS
F29	-	sys_nreswarm	0	IOD	0	H	0	1.8 V	vdds_ bank24	Yes	Yes	4	PUx/ PDy[7]	LVCMOS Tri-State Open Drain
N27	-	vdds_bank26	0	PWR	-	-	-	-	-	-	-	-	-	Power
L31	-	sys_pwr_req	0	O	H	1	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		hw_wkdbg15	5	O										
		safe_mode	7											
H29	-	sr_pmic_scl	0	IOD	H	H	0	1.2 V or 1.8 V	vdds_ bank26	Yes	No	3	PUx/ PDy[4]	LVCMOS Open Drain
J29	-	sr_pmic_sda	0	IOD	H	H	0	1.2 V or 1.8 V	vdds_ bank26	Yes	No	3	PUx/ PDy[4]	LVCMOS Open Drain
K30	-	sys_nirq1	0	I	H	H	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PUx/ PDy[4]	LVCMOS
		gpio1_wk16	6	IO										
J30	-	sys_nirq2	0	I	H	H	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PUx/ PDy[4]	LVCMOS
		gpio1_wk17	6	IO										

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
K29	-	i2c1_pmic_scl	0	IOD	H	H	0	1.2 V or 1.8 V	vdds_ bank26	Yes	No	3	PUx/ PDy-OD[4]	I^2C Open Drain
H30	-	i2c1_pmic_sda	0	IOD	H	H	0	1.2 V or 1.8 V	vdds_ bank26	Yes	No	3	PUx/ PDy-OD[4]	I^2C Open Drain
J31	-	sys_boot0	0	I	Z	Z	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		drm_emu2	3	O										
		drm_emu15	4	O										
		hw_wkdbg0	5	O										
		gpio1_wkout0	6	O										
		safe_mode	7											
K31	-	sys_boot1	0	I	Z	Z	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		drm_emu3	3	O										
		drm_emu16	4	O										
		hw_wkdbg1	5	O										
		gpio1_wkout1	6	O										
		safe_mode	7											
L32	-	sys_boot2	0	I	Z	Z	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		drm_emu4	3	O										
		drm_emu17	4	O										
		hw_wkdbg2	5	O										
		gpio1_wkout2	6	O										
		safe_mode	7											
K32	-	sys_boot3	0	I	Z	Z	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		drm_emu5	3	O										
		drm_emu18	4	O										
		hw_wkdbg3	5	O										
		gpio1_wkout3	6	O										
		safe_mode	7											
J32	-	sys_boot4	0	I	Z	Z	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		drm_emu6	3	O										
		drm_emu19	4	O										
		hw_wkdbg4	5	O										
		gpio1_wkout4	6	O										
		safe_mode	7											
H31	-	sys_boot5	0	I	Z	Z	0	1.2 V or 1.8 V	vdds_ bank26	Yes	Yes	4[9]	PU/PD	LVCMOS
		sys_aux_msecure	1	O										
		hw_wkdbg8	5	O										
		gpio1_wkout5	6	O										
		safe_mode	7											
-	B20	ddrch1_dm0	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C17	ddrch1_dm1	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C26	ddrch1_dm2	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A10	ddrch1_dm3	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B25	ddrch1_dq0	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B24	ddrch1_dq1	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C23	ddrch1_dq2	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B23	ddrch1_dq3	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B22	ddrch1_dq4	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
-	A22	ddrch1_dq5	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B21	ddrch1_dq6	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A21	ddrch1_dq7	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A15	ddrch1_dq8	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B14	ddrch1_dq9	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C13	ddrch1_dq10	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B13	ddrch1_dq11	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B12	ddrch1_dq12	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A12	ddrch1_dq13	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B11	ddrch1_dq14	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A11	ddrch1_dq15	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	J27	ddrch1_dq16	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	J26	ddrch1_dq17	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	H27	ddrch1_dq18	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	H26	ddrch1_dq19	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	G26	ddrch1_dq20	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	G25	ddrch1_dq21	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	F26	ddrch1_dq22	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	E27	ddrch1_dq23	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A8	ddrch1_dq24	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C7	ddrch1_dq25	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A7	ddrch1_dq26	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B6	ddrch1_dq27	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C5	ddrch1_dq28	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B5	ddrch1_dq29	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B4	ddrch1_dq30	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A4	ddrch1_dq31	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C19	ddrch1_dqs0	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C15	ddrch1_dqs1	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	E26	ddrch1_dqs2	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A9	ddrch1_dqs3	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B19	ddrch1_ndqs0	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B15	ddrch1_ndqs1	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
-	D27	ddrch1_ndqs2	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	B9	ddrch1_ndqs3	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	A17	ddrch1_vref_dq	0	PWR	Z	NA	0	1.2 V	vddq_ddr_ch1	Yes	No	-	NA	Analog
G18	-	vddq_vref_ddrch1	0	PWR	-	-	-	-	-	-	-	-	-	-
A29 / A26 / A24 / A20 / A18 / A15 / A13 / A10 / A8 / A6 / D33 / G33 / G25 / G24 / G20 / G19 / G9 / H9 / L33 / L27 / M27	A24 / A19 / A14 / A5 / B16 / B7 / C21 / C11 / C9 / D26 / F27 / J25	vddq_ddr_ch1	0	PWR	-	-	-	-	-	-	-	-	-	Power
-	U3	ddrch2_dm0	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	W1	ddrch2_dm1	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	J3	ddrch2_dm2	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG4	ddrch2_dm3	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	K2	ddrch2_dq0	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	L1	ddrch2_dq1	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	L3	ddrch2_dq2	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	M1	ddrch2_dq3	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	N1	ddrch2_dq4	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	N2	ddrch2_dq5	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	P1	ddrch2_dq6	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	P2	ddrch2_dq7	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AA3	ddrch2_dq8	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AB2	ddrch2_dq9	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AC1	ddrch2_dq10	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AC2	ddrch2_dq11	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AD2	ddrch2_dq12	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AD1	ddrch2_dq13	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AE2	ddrch2_dq14	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF3	ddrch2_dq15	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	C2	ddrch2_dq16	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	D1	ddrch2_dq17	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	E1	ddrch2_dq18	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	E2	ddrch2_dq19	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	F1	ddrch2_dq20	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	F2	ddrch2_dq21	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
-	G2	ddrch2_dq22	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	G3	ddrch2_dq23	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG6	ddrch2_dq24	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF6	ddrch2_dq25	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF7	ddrch2_dq26	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AE7	ddrch2_dq27	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF8	ddrch2_dq28	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG9	ddrch2_dq29	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AE9	ddrch2_dq30	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG10	ddrch2_dq31	0	IO	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	R2	ddrch2_dqs0	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AA2	ddrch2_dqs1	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	H2	ddrch2_dqs2	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF5	ddrch2_dqs3	0	IODS	L	L	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	R3	ddrch2_ndqs0	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AA1	ddrch2_ndqs1	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	J1	ddrch2_ndqs2	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG5	ddrch2_ndqs3	0	IODS	H	H	0	1.2 V or 1.3 V or 1.5 V	vddq_ddr_ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	U1	ddrch2_vref_dq	0	PWR	Z	NA	0	1.2 V	vddq_ddr_ch2	Yes	No	-	NA	Analog
W7	-	vddq_vref_ddrch2	0	PWR	-	-	-	-	-	-	-	-	-	-
E1 / H7 / H1 / J7 / L1 / N1 / P7 / R7 / T1 / V1 / AD7 / AD1 / AE7 / AG7 / AG5 / AG1 / AK1 / AN10 / AN7 / AN5	D2 / G1 / J2 / L2 / N3 / R1 / Y1 / AB1 / AF9 / AF4 / AF2 / AG7	vddq_ddr_ch2	0	PWR	-	-	-	-	-	-	-	-	-	-
-	AF22	lpddr2ch1_ca0	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG22	lpddr2ch1_ca1	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF20	lpddr2ch1_ca2	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG20	lpddr2ch1_ca3	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AE19	lpddr2ch1_ca4	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AE15	lpddr2ch1_ca5	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AE13	lpddr2ch1_ca6	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF13	lpddr2ch1_ca7	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG13	lpddr2ch1_ca8	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF12	lpddr2ch1_ca9	0	O	L	L	0	1.2 V	vddca_lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF17	lpddr2ch1_ck	0	IODS	L	L	0	1.2 V	vddca_lpddr2ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
-	AF18	lpddr2ch1_cke0	0	O	L	L	0	1.2 V	vddca_ lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG18	lpddr2ch1_cke1	0	O	L	L	0	1.2 V	vddca_ lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG17	lpddr2ch1_nck	0	IODS	H	H	0	1.2 V	vddca_ lpddr2ch1	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AF19	lpddr2ch1_ncs0	0	O	L	L	0	1.2 V	vddca_ lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG19	lpddr2ch1_ncs1	0	O	L	L	0	1.2 V	vddca_ lpddr2ch1	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AG15	lpddr2ch1_vref_ ca_out	0	PWR	Z	NA	0	1.2 V	vddq_ddr_ ch1	Yes	No	-	NA	Analog
AG18	-	vddca_vref_ lpddr2ch1	0	PWR	-	-	-	-	-	-	-	-	-	Power
AJ23 / AJ22 / AN26 / AN20 / AN18	AF16 / AF14 / AG21	vddca_lpddr2ch1	0	PWR	-	-	-	-	-	-	-	-	-	Power
-	L25	lpddr2ch2_ca0	0	O	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	M26	lpddr2ch2_ca1	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	N26	lpddr2ch2_ca2	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	N25	lpddr2ch2_ca3	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	P26	lpddr2ch2_ca4	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	W25	lpddr2ch2_ca5	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	Y27	lpddr2ch2_ca6	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	Y26	lpddr2ch2_ca7	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AA27	lpddr2ch2_ca8	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	AA26	lpddr2ch2_ca9	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	T27	lpddr2ch2_ck	0	IODS	L	L	0	1.2 V	vddca_ lpddr2ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	R25	lpddr2ch2_cke0	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	R27	lpddr2ch2_cke1	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	T26	lpddr2ch2_nck	0	IODS	H	H	0	1.2 V	vddca_ lpddr2ch2	NA	NA	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	R26	lpddr2ch2_ncs0	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	P27	lpddr2ch2_ncs1	0	IO	L	L	0	1.2 V	vddca_ lpddr2ch2	Yes	No	See[3]	PUx/ PDy[3]	LVCMOS DDR
-	V27	lpddr2ch2_vref_ ca_out	0	AI	Z	NA	0	1.2 V	vddq_ddr_ ch2	Yes	No	-	NA	Analog
AB27	-	vddca_vref_ lpddr2ch2	0	PWR	-	-	-	-	-	-	-	-	-	Power
T33 / AA33 / AC33 / AG29 / AH29	N27 / U26 / W26	vddca_lpddr2ch2	0	PWR	-	-	-	-	-	-	-	-	-	Power
AN14	AG12	pop_lpddr2ch1_zq	0	FEED	-	-	-	-	-	-	-	-	-	FEED
AH33	AB27	pop_lpddr2ch2_zq	0	FEED	-	-	-	-	-	-	-	-	-	FEED
B2 / A31	B2 / B26	pop_vacc_lpddr2[15]	0	PWR	-	-	-	-	-	-	-	-	-	FEED
A21 / A30 / AJ33 / AL1 / AN12 / AN29 / C1 / P33 / Y1 / AA1	A18 / A25 / AC27 / AE1 / AG11 / AG23 / C1 / L26 / V1 / V2	pop_vdd1_lpddr2_ shared	0	PWR	-	-	-	-	-	-	-	-	-	FEED

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
A3 / AF33 / AN13 / AN21 / AN28 / AN3 / A22 / C33 / N33 / Y33 / AB1 / AC1	A3 / AA25 / AE11 / AE17 / AF23 / AG3 / B18 / C27 / K27 / U25 / W2 / W3	pop_vdd2_lpddr2_shared	0	PWR	-	-	-	-	-	-	-	-	-	FEED
H26 / H25 / H8 / J26 / J8 / K14 / K13 / K12 / L14 / L13 / L12 / L11 / L8 / M13 / M12 / M11 / M10 / M8 / P14 / P13 / P12 / P11 / P10 / R14 / R13 / T14 / U22 / U21 / U20 / V23 / V22 / V21 / V20 / Y25 / Y24 / Y23 / AA23 / AA18 / AB25 / AB24 / AB23 / AB18 / AC23 / AC18 / AD25 / AD24 / AD23 / AE16 / AE15 / AE14 / AE13 / AE8 / AF9 / AF8	-	vdd_core	0	PWR	-	-	-	-	-	-	-	-	-	-
AC27	-	vdd_core_sense	0	PWR	-	-	-	-	-	-	-	-	-	-
R12 / R11 / R10 / R9/ T13 / T12 / T11 / T10 / T9 / W14 / W13 / W12 / W11 / W10 / W9 / Y22 / Y21 / Y19 / Y11 / Y10 / AA22 / AA19 / AA16 / AA15 / AA14 / AA13 / AA12 / AA11 / AA10 / AA9 / AB22 / AB21 / AB19 / AB11 / AB10 / AC22 / AC19 / AC16 / AC15 / AC14 / AC13 / AC12 / AC11 / AC10 / AC9 / AD22 / AD21 / AD19 / AD11 / AE11	-	vdd_mm	0	PWR	-	-	-	-	-	-	-	-	-	-
AJ21	-	vdd_mm_sense	0	PWR	-	-	-	-	-	-	-	-	-	-
H24 / H23 / H22 / H21 / H20 / H19 / K23 / K22 / K21 / K20 / K19 / K18 / K17 / L25 / L24 / L23 / L22 / L21 / L20 / L19 / L18 / L17 / P25 / P23 / P22 / P21 / P20 / P19 / P18 / P17 / R26 / R25 / R23 / R22 / R21 / R20	-	vdd_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
P26	-	vdd_mpu_sense	0	PWR	-	-	-	-	-	-	-	-	-	-
D27	-	vss_mpu_sense	0	GND	-	-	-	-	-	-	-	-	-	-
AE5	-	vpp1	0	PWR	-	-	-	-	-	-	-	-	-	-

Table 2-1. Ball Characteristics[1] (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] [2]	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
A28 / A25 / A19 / A16 / A14 / A12 / A9 / A7 / C2 / D3 / D2 / F33 / F1 / G17 / H33 / H18 / H17 / H16 / H15 / H14 / H13 / H12 / H11 / H10 / J25 / J24 / J23 / J22 / J21 / J20 / J19 / J18/ J17 / J16 / J15 / J14 / J13 / J12 / J11 / J10 / J9 / K26 / K25 / K24 / K16 / K15 / K11 / K10 / K9 / K8 / K1 / L26 / L16 / L15 / L10 / L9 / M33 / M26 / M25 / M24 / M23 / M22 / M21 / M20 / M19 / M18 / M17 / M16 /	A26 / A23 / A20 / A16 / A13 / A6 / A2 / B27 / B17 / B10 / B8 / B3 / B1 / E25 / E3 / G27 / H1 / K26 / K1 / L27 / M27 / M2 / T2 / T1 / U27 / U2 / V26 / W27 / Y2 / AB26 / AC3 / AE21 / AE5 / AF21 / AF15 / AF11 / AF10 / AF1 / AG16 /	vss	0	PWR	-	-	-	-	-	-	-	-	-	-
M15 / M14 / M9 / M1 / N26 / N25 / N24 / N23 / N22 / N21 / N20 / N19 / N18 / N17 / N16 / N15 / N14 / N13 / N12 / N11 / N10 / N9 / N8 / P24 / P16 / P15 / P9 / P8 / R33 / R24 / R19 / R18 / R17 / R16 / R15 / R8 / R1 / T26 / T25 / T24 / T23 / T22 / T21 / T20 / T19 / T18 / T17 / T16 / T15 / T8 / U27 / U26 / U25 / U24 / U23 / U19 / U18 / U17 / U16 / U15 / U14 / U13 / U12 / U11 / U10 / U9 / U8 / U7 / V25 / V24 / V19 / V18 / V17 / V16 / V15 / V14 / V13 / V12 / V11 / V10 / V9 / V8 / W26 / W25 / W24 / W23 / W22 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W8 / W1 / Y26 / Y20 / Y18 / Y17 / Y16 / Y15 / Y14 / Y13 / Y12 / Y9 / Y8 / AA26 / AA25 / AA24 / AA21 / AA20 / AA17 / AA8 / AA3 / AA2 / AE33 / AB26 / AB20 / AB17 / AB16 / AB15 / AB14 / AB13 / AB12 / AB9 / AB8 / AB7 / AC26 / AC25 / AC24 / AC21 / AC20 / AC17 / AC8 / AD33 / AD26 / AD20 / AD18 / AD17 / AD16 / AD15 / AD14 / AD13 / AD12 / AD10 / AD9 / AD8 / AE26 / AE25 / AE24 / AE23 / AE22 / AE21 / AE20 / AE19 / AE18 / AE17 / AE12 / AE10 / AE9 / AE1 / AF26 / AF25 / AF24 / AF23 / AF22 / AF21 / AF20 / AF19 / AF18 / AF17 / AF16 / AF15 / AF14 / AF13 / AF12 / AF11 / AF10 / AG33 / AG17 / AG10 / AG3 / AG2 / AH1 / AM32 / AM2 / AN25 / AN19 / AN11 / AN8 / AN6 / V7 / AE33	AG14 / AG8 / AG2	vss	0	PWR	-	-	-	-	-	-	-	-	-	-

Table 2-1. Ball Characteristics(1) (continued)

BALL BOTTOM [1]	BALL TOP [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	IO VOLTAGE VALUE [9] (2)	POWER NAME [10]	SECOND POWER AVAIL. [11]	HYS [12]	BUFFER STRENGTH (mA) [13]	PULLUP/ DOWN TYPE [14]	IO CELL [15]
V26	-	vdda_dpll_core_emu_abe	0	PWR	-	-	-	-	-	-	-	-	-	-
T7	-	vdda_dpll_mm_l4per	0	PWR	-	-	-	-	-	-	-	-	-	-
AG23	-	vdda_dpll_hdmi	0	PWR	-	-	-	-	-	-	-	-	-	-
V27	-	vdda_dpll_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
T5	-	vdda_ldo_core	0	PWR	-	-	-	-	-	-	-	-	-	-
AG15	-	vdda_ldo_mm	0	PWR	-	-	-	-	-	-	-	-	-	-
G14	-	vdda_ldo_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
V29	-	vdda_ldo_emu_wkup(8)	0	PWR	-	-	-	-	-	-	-	-	-	-
W29	-	vnwa_emu_wkup(8)	0	PWR	-	-	-	-	-	-	-	-	-	-
Y7	-	vdda_vbgap_core	0	PWR	-	-	-	-	-	-	-	-	-	-
AG19	-	cap_vdda_ldo_sram_core_array	0	PWR	-	-	-	-	-	-	-	-	-	-
AG16	-	cap_vdda_ldo_sram_mm_array	0	PWR	-	-	-	-	-	-	-	-	-	-
G16	-	cap_vdda_ldo_sram_mpu_array	0	PWR	-	-	-	-	-	-	-	-	-	-
T27	-	cap_vddldo_emu_wkup	0	PWR	-	-	-	-	-	-	-	-	-	-
AJ16	-	cap_vbb_ldo_mm	0	PWR	-	-	-	-	-	-	-	-	-	-
e16	-	cap_vbb_ldo_mpu	0	PWR	-	-	-	-	-	-	-	-	-	-
N7	-	cap_vdda_ldo_sram_mpu_array2	0	PWR	-	-	-	-	-	-	-	-	-	-

(1) NA in this table stands for Not Applicable.

(2) For more information on recommended operating conditions, see Table 3-3, *Recommended Operating Conditions*.

(3) In PUx / PDy, x and y = 60 to 200 µA
The output impedance settings (or drive strengths) of this IO are programmable (34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω or 11.75 mA, 10 mA, 8.33 mA, 6.67 mA) depending on the values of the I2, I1, I0 registers. The default value is I[2:0] = 010.

(4) The pullup or pulldown resistor can be either the standard LVCMOS 100-µA drive strength or the configurable I^2C internal pullup resistance.
Naming convention:

– PUx / PDy-OD is specified: the default buffer configuration is high-speed (HS) I^2C point-to-point mode using the internal pullup resistance.

NOTE

For balls K29 / H30, i2c1_pmic_scl and i2c1_pmic_sda functional modes are I^2C only.

– PUx / PDy-GPIO is specified: the default buffer configuration is standard LVCMOS mode (non-I^2C). The internal pullup resistance programming does not apply in this mode.

These IOs have a pullupresx register that configures the internal I^2C pullup or pulldown resistor of the IO, plus two load register bits [LB1:0] that configure the I^2C load.
By default, at the reset release time, the multiplexing mode is safe_mode. The I^2C function must be selected to enable this I^2C function and by default:

– For HDMI DDC (balls AK24 / AJ24):
HSMODE = fast-speed mode
PULLUPSPRESX = 0, this means that the internal I^2C pullup resistor is enabled.
LB[1:0] = 00: this means a 4-kΩ pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

– For SR (balls H29 / J29):
HSMODE = fast-speed mode
PULLUPSPRESX = 0, this means that the internal I^2C pullup resistor is enabled.
LB[1:0] = 01: this means a 4-kΩ pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

– For I2C1 (balls K29 / H30):
HSMODE = fast-speed mode
PULLUPSPRESX = 0, this means that the internal I^2C pullup resistor is enabled.
LB[1:0] = 01: this means a 2.1-kΩ pullup resistor, for a load = 5 pF to 15 pF, in fast-speed mode.

– For I2C2, I2C3, I2C4, I2C5 (balls AK22 / AJ20 / AB3 / AB2 / AF30 / AF29 / AL32 / AL31):
HSMODE = full-speed mode
PULLUPSPRESX = 1, external PU expected on the board.

NOTE

For I2C[5:2]: external pullup or pulldown resistors can be avoided if the I2C[5:2] interfaces are activated by boot. Indeed, if the interface is activated then the interface is configured in driver mode and in this case pullup or pulldown resistors are not needed. For more information on boot modes, see the OMAP543x TRM.

In I^2C mode configuration, for a full description of the internal pullup resistance programming according to the load range, see the CONTROL_I2C_0 and the CONTROL_SMART3I/O_PADCONF_0 registers in the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.
In standard LVCMOS mode configuration (non-I^2C mode), for a full description of the pullup or pulldown programming, see the CONTROL_CORE_PADX registers in the Control Module / Control Module Functional Description / Pad Functional Multiplexing and Configuration section of the OMAP543x TRM.

(5) In PDy, y = 200 kΩ

(6) On the SDCARD IOs, PUx/PDy = 10 kO to 40 kΩ.

(7) The pullup or pulldown block strength is equal to: minimum = 50 µA, typical = 100 µA, maximum = 250 µA.

(8) **CAUTION**: vnwa_emu_wkup and vdda_ldo_emu_wkup must be connected on the board.

(9) The output impedance settings of this IO cell are programmable; by default, the value is DS[1:0] = 10, this means 40 Ω. For more information on DS[1:0] register configuration, see the OMAP543x TRM.

(10) The output impedance settings of this IO cell are programmable; by default, the register value is ic[1:0] = 00, this means 44 Ω.
The hysteresis function is also programmable for this IO; by default, the register value is hyst_en = 1, this means hysteresis function is enabled. For more information see the OMAP543x TRM.

(11) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AJ10 / AK10 / AJ11 / AK11 / AJ12 / AK12 / AC2 / AC3) can output the same GPIO in mode 0 or in mode 5.

(12) For the following balls: AL15 / AM15 / AL13 / AM13 / AL11 / AM11 / B16 / C16 / B14 / C14 / B12 / C12, pulldown resistor is 20 kΩ. No pullup resistor is available.

(13) See the Note below.

(14) See the Caution below.

(15) pop_vacc_lpddr2 must be left unconnected.

(16) The maximum capacitive load for the DSI Low-Power mode is equal to 70 pF.
For more information, see Chapter 9 of the MIPI D-PHY standard v1.1.
No specific capacitive load is needed in DSI High-Speed mode.

(17) IO drive strength for usbd0_hs_dp and usbd0_hs_dm: minimum 18.3 mA, maximum 89 mA (for a power supply vdda_usba0otg_3p3v = 3.46 V).
IO drive strength for usbphy_ce: minimum 100 µA, maximum 20 mA.

(18) Minimum PU = 900 O, maximum PU = 3.090 kO and minimum PD = 14.25 kO, maximum PD = 24.8 kO.
For more information, see chapter 7 of the USB2 specification, in particular section Signaling / Device Speed Identification.

NOTE

For SATA and USB3 SS PHYs:

- If the serial PHY is enabled, the corresponding vdda_xxx voltage supply must be supplied by a dedicated, low-noise, voltage source.
- If the serial PHY is definitively disabled:
  - The PHY voltage supply (vdda_xxx/vssa_xxx) and the associated DPLL voltage supply (vdda_dpll_xxx) are grounded for power saving.
  - The associated interface balls are left unconnected.

For HDMI PHY:

- If the serial PHY is enabled, the corresponding vdda_hdmi voltage and vdda_dpll_hdmi supplies must be supplied by dedicated low-noise voltage sources.
- If the serial PHY is definitively disabled:
  - vdda_hdmi is supplied.
  - vdda_dpll_hdmi can be grounded only if the corresponding HDMI DPLL is never used to generate the functional clock to the DISPC.
  - The associated data/clock balls are left unconnected.
  - The PHY can be put in OFF power state (even if the HDMI DPLL is used).

For HDMI control interface (CEC, HPD, DDC):

- If the HDMI control interface is enabled, vdds_hdmi must be supplied by a dedicated low-noise voltage source.
- If the HDMI is definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the HDMI and the multiplexed CMOS signals are definitively disabled:
  - The voltage supply (vdds_hdmi) is grounded for power saving.
  - The associated interface balls are left unconnected.

For DSI PortA/PortC PHYs:

- If the serial PHY is enabled, the corresponding vdda_dsiportx voltage supply must be supplied by a dedicated low-noise voltage source.
- If the PHY is definitively disabled:
  - The PHY voltage supply (vdda_dsiportx/vssa_dsiportx) is grounded for power saving only if the corresponding DSI DPLL is never used to generate the functional clock to the DISPC.
  - The associated interface balls are left unconnected.

For CSI-2 PHYs:

- If the CSI-2 serial PHY is enabled, vdda_csiportx must be supplied by a dedicated low-noise voltage source.
- If the CSI-2 serial PHY is definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
- If the CSI-2 serial PHY and the multiplexed CMOS signals are definitively disabled:
  - The PHY voltage supply (vdda_csiportx/vssa_csiportx) is grounded for power saving.
  - The associated interface balls are left unconnected.

For USB2 HS PHY:

- If the USB2 HS PHY is enabled, vdda_usbhs33 and vdds_usbhs18 must be supplied by dedicated 3.3-V and 1.8-V low-noise voltage sources.
- If the USB2 HS PHY is definitively disabled, the other multiplexed 3.3-V CMOS signals (UART3) of the interface can be enabled, vdda_usbhs33 must be supplied by a dedicated 3.3-V voltage source and vdds_usbhs18 can be supplied by the same voltage source as vdds_1p8v.
- If the USB2 HS PHY and UART3 signals are definitively disabled:
  - vdda_usbhs33 and vdds_usbhs18 are supplied.
  - The power-down bit is set to 1 (USB2PHY_PWR_CNTL.MEM_PD bit) to put the USB2 PHY in power-down mode and lower the leakage current from other supplies.
  - The disable charger detect is set to 1 CONTROL_USB2PHYCORE.USB2PHY_DISCHGDET bit) to disable the charger detect.
  - There is a forward-biased diode from usbd0_hs_dp, usbd0_hs_dm, usbphy_ce pins to vdda_usbhs33 pin.

For SDCARD interface:

– If the SDCARD functional signals are enabled, vdds_sdcard must be supplied by a 1.8-V / 3.0-V voltage source.
– If the SDCARD functional signals are definitively disabled, the other multiplexed CMOS signals of the interface can be enabled, the interface can be supplied by the same voltage source as vdds_1p8v.
– If the SDCARD functional balls and the multiplexed CMOS signals are definitively disabled:
  – The interface balls are left unconnected.
  – The SDCARD_PWRDNZ bit is kept at 0.

There are two options for the associated power supply:

– vdds_sdcard is grounded.
– vdds_sdcard is supplied by a 1.8-V or 3.0-V voltage supply. In this case, it is also recommended to keep default value of SDCARD_BIAS_VMODE bit (that is, 1).

For the corresponding setting of the SDCARD_PWRDNZ, and SDCARD_BIAS_VMODE bits, see the Control Module / Control Module Functional Description / Extended-Drain I/O and PBIAS Cell section and the Control Module / Control Module Programming Guide section of the OMAP543x TRM.

CAUTION

Some GPMC chip-select pins have a pulldown resistor enabled by default after reset and all chip-select signals gpmc_ncs[7:0] are active low.

In case of an application with several memories connected to the GPMC, for the memories connected to a chip-select whose internal pulldown resistor is enabled by default after reset (ncs1, ncs2, ncs3, or ncs4), it is necessary to disable this pulldown resistor before performing the first access to any memory. Otherwise, contention will happen because several memories will be selected at the same time.

In the particular case of memory booting via the GPMC interface (memory device must be connected to the gpmc_ncs0 pin), it is not possible to disable any pulldown resistor before the first access. As a consequence, no memory device should be connected to a chip-select whose internal pulldown resistor is enabled by default (ncs1, ncs2, ncs3, or ncs4). Otherwise, contention will prevent the OMAP5430 device from booting.

For more information, see the Initialization / Preinitialization / Boot Configuration / Boot Peripheral Pin Multiplexing section of the OMAP543x TRM.

ADVANCE INFORMATION

2.3 Multiplexing Characteristics

Table 2-2 describes the device multiplexing (no characteristics are available in this table).

NOTE

This table doesn't take into account subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 2.4, *Signal Descriptions*.

NOTE

For more information, see the Control Module / Control Module Functional Description / PAD Functional Multiplexing and Configuration section of the OMAP543x TRM.

NOTE

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration. (safe_mode is not an input signal.)

NOTE

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, this pad is actually set undriven (high impedance: Z) with a potential pullup or pulldown resistor. Pullup and pulldown resistors need to be disabled to have a pure high impedance.

NOTE

All balls not described in Table 2-1 and Table 2-2 are not connected.

Table 2-2. Multiplexing Characteristics(1)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
G26 / G15 / G13 / G8 / H27 / L7 / M7 / W27 / AA27 / AA7 / AC7 / AE27 / AG22 / AG21 / AG14 / AG12 / AG8	-	vdds_1p8	-	-	-	-	-	-	-
AF7	-	vdds_emmc	-	-	-	-	-	-	-
AL2	-	emmc_clk	-	-	-	-	-	gpio2_46	safe_mode
AK4	-	emmc_cmd	-	-	-	-	-	gpio2_47	safe_mode
AK3	-	emmc_data0	-	-	-	-	-	gpio2_48	safe_mode
AJ4	-	emmc_data1	-	-	-	-	-	gpio2_49	safe_mode
AK2	-	emmc_data2	-	-	-	-	-	gpio2_50	safe_mode
AJ3	-	emmc_data3	-	-	-	-	-	gpio2_51	safe_mode
AH2	-	emmc_data4	-	-	-	-	-	gpio2_52	safe_mode
AJ2	-	emmc_data5	-	-	-	-	-	gpio2_53	safe_mode
AH3	-	emmc_data6	-	-	-	-	-	gpio2_54	safe_mode
AH4	-	emmc_data7	-	-	-	-	-	gpio2_55	safe_mode
G21 / G22	-	vdds_c2c	-	-	-	-	-	-	-
B21	-	Reserved	-	-	kbd_row0	gpmc_ad0	-	gpio2_37	safe_mode
C21	-	Reserved	-	-	kbd_row1	gpmc_ad1	-	gpio2_38	safe_mode
B20	-	Reserved	-	-	kbd_row2	gpmc_ad2	-	gpio2_39	safe_mode
C20	-	Reserved	-	-	kbd_row3	gpmc_ad3	-	gpio2_40	safe_mode
B19	-	Reserved	-	-	kbd_row4	gpmc_ad4	-	gpio2_41	safe_mode
C19	-	Reserved	-	-	kbd_row5	gpmc_ad5	-	gpio2_42	safe_mode
B18	-	Reserved	-	-	kbd_row6	gpmc_ad6	-	gpio2_43	safe_mode
C18	-	Reserved	-	-	kbd_row7	gpmc_ad7	-	gpio2_44	safe_mode
C22	-	Reserved	-	-	kbd_row8	gpmc_clk	-	gpio2_36	safe_mode
B22	-	Reserved	-	-	-	gpmc_nwp	gpmc_nbe1	gpio2_35	safe_mode
E22	-	Reserved	-	-	-	gpmc_nadv_ale	-	gpio2_33	safe_mode
D22	-	Reserved	-	-	kbd_col8	gpmc_nbe0_cle	-	gpio2_34	safe_mode
E26	-	Reserved	-	-	kbd_col0	gpmc_ad8	hw_dbg16	gpio2_56	safe_mode
D26	-	Reserved	-	-	kbd_col1	gpmc_ad9	hw_dbg17	gpio2_57	safe_mode
E25	-	Reserved	-	-	kbd_col2	gpmc_ad10	hw_dbg18	gpio2_58	safe_mode
D25	-	Reserved	-	-	kbd_col3	gpmc_ad11	hw_dbg19	gpio2_59	safe_mode
E24	-	Reserved	-	-	kbd_col4	gpmc_ad12	hw_dbg20	gpio2_60	safe_mode
D24	-	Reserved	-	-	kbd_col5	gpmc_ad13	hw_dbg21	gpio2_61	safe_mode
E23	-	Reserved	-	-	kbd_col6	gpmc_ad14	hw_dbg22	gpio2_62	safe_mode
D23	-	Reserved	-	-	kbd_col7	gpmc_ad15	hw_dbg23	gpio2_63	safe_mode
E21	-	Reserved	-	-	-	gpmc_a16	hw_dbg24	gpio4_113	safe_mode
D21	-	Reserved	-	-	-	gpmc_a17	hw_dbg25	gpio4_114	safe_mode
E20	-	Reserved	-	-	-	gpmc_a18	hw_dbg26	gpio4_115	safe_mode
D20	-	Reserved	-	-	-	gpmc_a19	hw_dbg27	gpio4_116	safe_mode
E19	-	Reserved	-	-	-	gpmc_a20	hw_dbg28	gpio4_117	safe_mode
D19	-	Reserved	-	-	-	gpmc_a21	hw_dbg29	gpio4_118	safe_mode
E18	-	Reserved	-	-	-	gpmc_a22	hw_dbg30	gpio4_119	safe_mode
D18	-	Reserved	-	-	-	gpmc_a23	hw_dbg31	gpio4_120	safe_mode
E29	-	Reserved	-	-	-	gpmc_ncs0	-	gpio2_32	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
C29	-	Reserved	-	-	-	gpmc_wait0	-	gpio2_45	safe_mode
E30	-	Reserved	-	-	-	-	hw_wkdbg13	gpio1_wk15	safe_mode
C30	-	Reserved	-	-	-	-	hw_wkdbg14	gpio1_wk14	safe_mode
G12	-	vdds_bank2	-	-	-	-	-	-	-
E13	-	hsi1_acready	cam_strobe	-	usbb2_ulpitll_clk	-	-	gpio3_64	safe_mode
E14	-	hsi1_caready	-	-	usbb2_ulpitll_nxt	-	-	gpio3_65	safe_mode
D13	-	hsi1_acwake	-	-	usbb2_ulpitll_dir	-	-	gpio3_66	safe_mode
E15	-	hsi1_cawake	-	-	usbb2_ulpitll_stp	-	-	gpio3_67	safe_mode
D15	-	hsi1_acflag	-	-	usbb2_ulpitll_ data0	-	-	gpio3_68	safe_mode
D14	-	hsi1_acdata	-	-	usbb2_ulpitll_ data1	-	-	gpio3_69	safe_mode
D12	-	hsi1_caflag	-	-	usbb2_ulpitll_ data2	-	-	gpio3_70	safe_mode
E12	-	hsi1_cadata	-	-	usbb2_ulpitll_ data3	-	-	gpio3_71	safe_mode
D10	-	uart1_tx	-	-	usbb2_ulpitll_ data4	-	-	gpio3_72	safe_mode
E9	-	uart1_cts	-	-	usbb2_ulpitll_ data5	gpmc_wait3	-	gpio3_73	safe_mode
D9	-	uart1_rx	-	-	usbb2_ulpitll_ data6	-	-	gpio3_74	safe_mode
E10	-	uart1_rts	-	-	usbb2_ulpitll_ data7	gpmc_ncs7	-	gpio3_75	safe_mode
G10	-	vdds_bank4	-	-	-	-	-	-	-
C7	-	hsi2_caready	-	-	usbb1_ulpiphy_ clk	gpmc_wait1	-	gpio3_76	safe_mode
C10	-	hsi2_acready	-	-	usbb1_ulpiphy_ nxt	gpmc_ncs1	-	gpio3_77	safe_mode
B8	-	hsi2_cawake	-	-	usbb1_ulpiphy_ dir	gpmc_a24	-	gpio3_78	safe_mode
C8	-	hsi2_acwake	-	-	usbb1_ulpiphy_ stp	gpmc_a25	-	gpio3_79	safe_mode
B7	-	hsi2_caflag	-	-	usbb1_ulpiphy_ data0	gpmc_wait2	-	gpio3_80	safe_mode
B10	-	hsi2_cadata	-	-	usbb1_ulpiphy_ data1	gpmc_ncs2	-	gpio3_81	safe_mode
B9	-	hsi2_acflag	-	-	usbb1_ulpiphy_ data2	gpmc_ncs3	-	gpio3_82	safe_mode
C9	-	hsi2_acdata	-	-	usbb1_ulpiphy_ data3	gpmc_ncs4	-	gpio3_83	safe_mode
C5	-	uart2_rts	mcspi3_somi	-	usbb1_ulpiphy_ data4	gpmc_nwe	hw_dbg16	gpio3_84	safe_mode
B5	-	uart2_cts	mcspi3_cs0	-	usbb1_ulpiphy_ data5	gpmc_noe_nre	hw_dbg17	gpio3_85	safe_mode
C6	-	uart2_rx	mcspi3_simo	-	usbb1_ulpiphy_ data6	gpmc_ncs5	hw_dbg18	gpio3_86	safe_mode
B6	-	uart2_tx	mcspi3_clk	-	usbb1_ulpiphy_ data7	gpmc_ncs6	hw_dbg19	gpio3_87	safe_mode
G23	-	vdds_hsic	-	-	-	-	-	-	-
B26	-	usbb1_hsic_strobe	-	-	-	-	-	gpio3_92	safe_mode
C26	-	usbb1_hsic_data	-	-	-	-	-	gpio3_93	safe_mode
B25	-	usbb2_hsic_strobe	-	-	-	-	-	gpio3_94	safe_mode
C25	-	usbb2_hsic_data	-	-	-	-	-	gpio3_95	safe_mode
Y27	-	vdds_bank5	-	-	-	-	-	-	-
V30	-	timer10_pwm_evt	-	-	-	-	-	gpio6_188	safe_mode
W30	-	dsiporta_te0	-	-	-	-	-	gpio6_189	safe_mode
AA32	-	vdda_dsiporta	-	-	-	-	-	-	-
W33	-	vssa_dsiporta	-	-	-	-	-	-	-
Y32	-	dsiporta_lane0x	-	-	-	-	-	-	-
Y31	-	dsiporta_lane0y	-	-	-	-	-	-	-
W32	-	dsiporta_lane1x	-	-	-	-	-	-	-
W31	-	dsiporta_lane1y	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
V32	-	dsiporta_lane2x	-	-	-	-	-	-	-
V31	-	dsiporta_lane2y	-	-	-	-	-	-	-
T32	-	dsiporta_lane3x	-	-	-	-	-	-	-
T31	-	dsiporta_lane3y	-	-	-	-	-	-	-
R32	-	dsiporta_lane4x	-	-	-	-	-	-	-
R31	-	dsiporta_lane4y	-	-	-	-	-	-	-
AC29	-	timer9_pwm_evt	sync_sof_clk	sync_usof _itp_clk	-	-	-	gpio6_190	safe_mode
AB29	-	dsiportc_te0	-	-	-	-	-	gpio6_191	safe_mode
AA31	-	vdda_dsiportc	-	-	-	-	-	-	-
AB33	-	vssa_dsiportc	-	-	-	-	-	-	-
AF32	-	dsiportc_lane0x	-	-	-	-	-	-	-
AF31	-	dsiportc_lane0y	-	-	-	-	-	-	-
AE32	-	dsiportc_lane1x	-	-	-	-	-	-	-
AE31	-	dsiportc_lane1y	-	-	-	-	-	-	-
AD32	-	dsiportc_lane2x	-	-	-	-	-	-	-
AD31	-	dsiportc_lane2y	-	-	-	-	-	-	-
AC32	-	dsiportc_lane3x	-	-	-	-	-	-	-
AC31	-	dsiportc_lane3y	-	-	-	-	-	-	-
AB32	-	dsiportc_lane4x	-	-	-	-	-	-	-
AB31	-	dsiportc_lane4y	-	-	-	-	-	-	-
AG9 / AG11	-	vdds_bank9	-	-	-	-	-	-	-
AK7	-	rfbi_hsync0	-	-	dispc_data17	kbd_col5	-	gpio6_160	safe_mode
AJ7	-	rfbi_te_vsync0	-	-	dispc_data16	kbd_row5	jtag_sel	gpio6_161	safe_mode
AK9	-	rfbi_re	-	-	dispc_pclk	kbd_col4	-	gpio6_164	safe_mode
AM5	-	rfbi_a0	-	-	dispc_de	kbd_row4	-	gpio6_165	safe_mode
AK5	-	rfbi_data8	-	-	dispc_data8	kbd_col3	drm_emu12	gpio6_174	safe_mode
AJ5	-	rfbi_data9	-	-	dispc_data9	kbd_row3	drm_emu13	gpio6_175	safe_mode
AL5	-	rfbi_data10	-	-	dispc_data10	kbd_row8	drm_emu14	gpio6_176	safe_mode
AL6	-	rfbi_data11	-	-	dispc_data11	kbd_row7	drm_emu15	gpio6_177	safe_mode
AJ8	-	rfbi_data12	-	-	dispc_data12	kbd_row6	drm_emu16	gpio6_178	safe_mode
AM9	-	rfbi_data13	-	-	dispc_data13	kbd_col8	drm_emu17	gpio6_179	safe_mode
AL9	-	rfbi_data14	-	-	dispc_data14	kbd_col7	drm_emu18	gpio6_180	safe_mode
AJ9	-	rfbi_data15	mcspi2_cs1	-	dispc_data15	kbd_col6	drm_emu19	gpio6_181	safe_mode
AJ10	-	gpio6_182[3]	-	-	dispc_data18	kbd_col0	-	gpio6_182[3]	safe_mode
AK10	-	gpio6_183[3]	-	-	dispc_data19	kbd_col1	-	gpio6_183[3]	safe_mode
AJ11	-	gpio6_184[3]	-	-	dispc_data20	kbd_col2	hw_dbg22	gpio6_184[3]	safe_mode
AK11	-	gpio6_185[3]	-	-	dispc_data21	kbd_row0	hw_dbg23	gpio6_185[3]	safe_mode
AJ12	-	gpio6_186[3]	-	-	dispc_data22	kbd_row1	hw_dbg24	gpio6_186[3]	safe_mode
AK12	-	gpio6_187[3]	-	-	dispc_data23	kbd_row2	hw_dbg25	gpio6_187[3]	safe_mode
AM6	-	rfbi_data0	-	-	dispc_data0	jtagtapext_rtck	drm_emu4	gpio6_166	safe_mode
AL7	-	rfbi_data1	-	-	dispc_data1	uart3_rx_irrx	drm_emu5	gpio6_167	safe_mode
AJ6	-	rfbi_data2	-	-	dispc_data2	uart3_tx_irtx	drm_emu6	gpio6_168	safe_mode
AM7	-	rfbi_data3	-	-	dispc_data3	jtagtapext_ntrst	drm_emu7	gpio6_169	safe_mode
AM8	-	rfbi_data4	-	-	dispc_data4	jtagtapext_tck	drm_emu8	gpio6_170	safe_mode
AL8	-	rfbi_data5	-	-	dispc_data5	jtagtapext_tmsc	drm_emu9	gpio6_171	safe_mode
AM10	-	rfbi_data6	-	-	dispc_data6	jtagtapext_tdo	drm_emu10	gpio6_172	safe_mode
AL10	-	rfbi_data7	-	-	dispc_data7	jtagtapext_tdi	drm_emu11	gpio6_173	safe_mode
AK6	-	rfbi_cs0	-	-	dispc_hsync	-	drm_emu3	gpio6_163	safe_mode
AK8	-	rfbi_we	-	-	dispc_vsync	-	drm_emu2	gpio6_162	safe_mode
AG20	-	vdds_bank8	-	-	-	-	-	-	-
AK20	-	mcspi2_cs0	jtagtapext_ntrst	-	dispc_fid	-	-	gpio7_196	safe_mode
AK21	-	mcspi2_clk	jtagtapext_tck	-	-	-	-	gpio7_197	safe_mode
AJ18	-	mcspi2_simo	jtagtapext_tmsc	-	-	-	hw_dbg20	gpio7_198	safe_mode
AK23	-	mcspi2_somi	jtagtapext_tdo	-	-	-	hw_dbg21	gpio7_199	safe_mode
AK22	-	i2c4_scl	jtagtapext_tdi	-	-	-	-	gpio7_200	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AJ20	-	i2c4_sda	jtagtapext_rtck	-	-	-	-	gpio7_201	safe_mode
AG24	-	vdds_hdmi	-	-	-	-	-	-	-
AK25	-	hdmi_cec	-	-	-	-	-	gpio7_192	safe_mode
AJ25	-	hdmi_hpd	-	-	-	-	-	gpio7_193	safe_mode
AK24	-	hdmi_ddc_scl	-	-	-	-	-	gpio7_194	safe_mode
AJ24	-	hdmi_ddc_sda	-	-	-	-	-	gpio7_195	safe_mode
AM27	-	vdda_hdmi	-	-	-	-	-	-	-
AN27	-	vssa_hdmi	-	-	-	-	-	-	-
AM23	-	hdmi_clkx	-	-	-	-	-	-	-
AL23	-	hdmi_clky	-	-	-	-	-	-	-
AM24	-	hdmi_data0x	-	-	-	-	-	-	-
AL24	-	hdmi_data0y	-	-	-	-	-	-	-
AM25	-	hdmi_data1x	-	-	-	-	-	-	-
AL25	-	hdmi_data1y	-	-	-	-	-	-	-
AM26	-	hdmi_data2x	-	-	-	-	-	-	-
AL26	-	hdmi_data2y	-	-	-	-	-	-	-
T2	-	vdda_csiporta	-	-	-	-	-	-	-
N4	-	vssa_csiporta	-	-	-	-	-	-	-
R2	-	csiporta_lane0x	-	-	cpi_pclk	-	-	gpio8_in236	safe_mode
R3	-	csiporta_lane0y	-	-	cpi_wen	-	-	gpio8_in237	safe_mode
P3	-	csiporta_lane1y	-	-	cpi_data0	-	-	gpio8_in238	safe_mode
P2	-	csiporta_lane1x	-	-	cpi_data1	-	-	gpio8_in239	safe_mode
N3	-	csiporta_lane2y	-	-	cpi_data2	-	-	gpio8_in240	safe_mode
N2	-	csiporta_lane2x	-	-	cpi_data3	-	-	gpio8_in241	safe_mode
M2	-	csiporta_lane3x	-	-	cpi_data4	-	-	gpio8_in242	safe_mode
M3	-	csiporta_lane3y	-	-	cpi_data5	-	-	gpio8_in243	safe_mode
L2	-	csiporta_lane4x	-	-	cpi_data6	-	-	gpio8_in244	safe_mode
L3	-	csiporta_lane4y	-	-	cpi_data7	-	-	gpio8_in245	safe_mode
T3	-	vdda_csiportb	-	-	-	-	-	-	-
V4	-	vssa_csiportb	-	-	-	-	-	-	-
V3	-	csiportb_lane0x	-	-	-	cpi_data12	-	gpio8_in246	safe_mode
V2	-	csiportb_lane0y	-	-	-	cpi_data13	-	gpio8_in247	safe_mode
W2	-	csiportb_lane1y	-	-	-	cpi_data14	-	gpio8_in248	safe_mode
W3	-	csiportb_lane1x	-	-	-	cpi_data15	-	gpio8_in249	safe_mode
Y2	-	csiportb_lane2y	-	-	-	cpi_hsyncin	-	gpio8_in250	safe_mode
Y3	-	csiportb_lane2x	-	-	-	cpi_vsyncin	-	gpio8_in251	safe_mode
H3	-	vdda_csiportc	-	-	-	-	-	-	-
H2	-	vssa_csiportc	-	-	-	-	-	-	-
K3	-	csiportc_lane0y	-	-	cpi_data8	-	-	gpio8_in252	safe_mode
K2	-	csiportc_lane0x	-	-	cpi_data9	-	-	gpio8_in253	safe_mode
J3	-	csiportc_lane1y	-	-	cpi_data10	-	-	gpio8_in254	safe_mode
J2	-	csiportc_lane1x	-	-	cpi_data11	-	-	gpio8_in255	safe_mode
W5	-	vdds_bank10	-	-	-	-	-	-	-
AD3	-	cam_shutter	-	-	-	-	sys_nodeid0	gpio8_224	safe_mode
AD4	-	cam_strobe	-	-	-	-	sys_nodeid1	gpio8_225	safe_mode
AD2	-	cam_globalreset	cam_shutter	-	cpi_fid	-	-	gpio8_226	safe_mode
AF3	-	timer11_pwm_evt	-	uart_tx	cpi_data12	-	hw_dbg26	gpio8_227	safe_mode
AF2	-	timer5_pwm_evt	sdcard_cd	uart_cts	cpi_data13	-	-	gpio8_228	safe_mode
AE3	-	timer6_pwm_evt	sdcard_wp	uart_rx	cpi_data14	-	-	gpio8_229	safe_mode
AE2	-	timer8_pwm_evt	sdcard_wp	uart_rts	cpi_data15	-	hw_dbg27	gpio8_230	safe_mode
AB3	-	i2c3_scl	-	-	-	-	-	gpio8_231	safe_mode
AB2	-	i2c3_sda	-	-	-	-	-	gpio8_232	safe_mode
AC2	-	gpio8_233[3]	sys_secure_ indicator	timer8_pwm_ evt	cpi_hsync	-	-	gpio8_233[3]	safe_mode
AC3	-	gpio8_234[3]	sys_drm_ msecure	-	cpi_vsync	-	-	gpio8_234[3]	safe_mode
P27	-	vdds_bank11	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
N30	-	abe_clks	-	-	abemcasp_axr	-	-	gpio4_96	safe_mode
R30	-	abedmic_din1	-	-	abemcasp_ahclkr	abemcbsp3_fsx	-	gpio4_97	safe_mode
R27	-	vdds_bank12	-	-	-	-	-	-	-
P32	-	abedmic_din2	-	-	abemcasp_axr	abemcbsp3_dx	-	gpio4_98	safe_mode
P31	-	abedmic_din3	-	-	-	abemcbsp3_dr	-	gpio4_99	safe_mode
P29	-	abedmic_clk1	-	-	-	abemcbsp3_clkx	-	gpio4_100	safe_mode
P30	-	abedmic_clk2	abemcbsp1_fsx	-	abemcasp_amutein	-	-	gpio4_101	safe_mode
N29	-	abedmic_clk3	abemcbsp1_dx	-	abemcasp_aclkx	-	-	gpio4_102	safe_mode
R29	-	vdds_bank14	-	-	-	-	-	-	-
T30	-	reserved	abemcbsp1_clkx	-	abemcasp_afsr	-	-	gpio4_103	safe_mode
T29	-	reserved	abemcbsp1_dr	-	abemcasp_aclkr	-	-	gpio4_104	safe_mode
N31	-	abemcbsp2_dr	-	-	abemcasp_axr	-	-	gpio4_105	safe_mode
N32	-	abemcbsp2_dx	-	-	abemcasp_amuteout	-	-	gpio4_106	safe_mode
M31	-	abemcbsp2_fsx	-	-	abemcasp_afsx	-	-	gpio4_107	safe_mode
M32	-	abemcbsp2_clkx	-	-	abemcasp_ahclkx	-	-	gpio4_108	safe_mode
M29	-	abemcpdm_ul_data	abemcbsp3_dr	-	abemcasp_axr3	-	-	gpio4_109	safe_mode
M30	-	abemcpdm_dl_data	abemcbsp3_dx	-	abemcasp_axr2	-	-	gpio4_110	safe_mode
L30	-	abemcpdm_frame	abemcbsp3_clkx	-	abemcasp_axr1	-	-	gpio4_111	safe_mode
L29	-	abemcpdm_lb_clk	abemcbsp3_fsx	-	-	-	-	gpio4_112	safe_mode
AG25	-	vdds_bank15	-	-	-	-	-	-	-
AK29	-	wlsdio_clk	mcspi4_clk	-	-	-	-	gpio5_128	safe_mode
AJ29	-	wlsdio_cmd	-	-	-	-	-	gpio5_129	safe_mode
AJ30	-	wlsdio_data0	mcspi4_simo	-	-	-	-	gpio5_130	safe_mode
AK30	-	wlsdio_data1	mcspi4_somi	-	-	-	-	gpio5_131	safe_mode
AJ31	-	wlsdio_data2	mcspi4_cs0	-	-	-	-	gpio5_132	safe_mode
AK31	-	wlsdio_data3	-	-	-	-	-	gpio5_133	safe_mode
AD27	-	vdds_bank16	-	-	-	-	-	-	-
AD30	-	uart5_rx	-	-	-	sdio4_data1	hw_dbg28	gpio5_134	safe_mode
AE29	-	uart5_tx	-	-	-	sdio4_data2	hw_dbg29	gpio5_135	safe_mode
AE30	-	uart5_cts	-	-	-	sdio4_data0	hw_dbg30	gpio5_136	safe_mode
AD29	-	uart5_rts	-	-	-	sdio4_data3	hw_dbg31	gpio5_137	safe_mode
AF30	-	i2c2_scl	-	-	-	-	-	gpio5_138	safe_mode
AF29	-	i2c2_sda	-	-	-	-	-	gpio5_139	safe_mode
AF27	-	vdds_bank18	-	-	-	-	-	-	-
AH32	-	mcspi1_clk	-	-	-	-	usbd0_ulpiphy_clk	gpio5_140	safe_mode
AG32	-	mcspi1_somi	-	-	-	-	usbd0_ulpiphy_nxt	gpio5_141	safe_mode
AH31	-	mcspi1_simo	-	-	-	-	usbd0_ulpiphy_dir	gpio5_142	safe_mode
AG31	-	mcspi1_cs0	-	-	-	-	usbd0_ulpiphy_data0	gpio5_143	safe_mode
AH30	-	mcspi1_cs1	-	-	-	-	usbd0_ulpiphy_data1	gpio5_144	safe_mode
AL32	-	i2c5_scl	-	uart4_rx	-	-	-	gpio5_147	safe_mode
AL31	-	i2c5_sda	-	uart4_tx	-	-	-	gpio5_148	safe_mode
AG27	-	vdds_bank19	-	-	-	-	-	-	-
AJ32	-	gpio5_145	mcspi1_cs2	uart4_cts	sdio5_clk	-	usbd0_ulpiphy_data2	gpio5_145	safe_mode
AK32	-	gpio5_146	mcspi1_cs3	uart4_rts	sdio5_cmd	-	usbd0_ulpiphy_data3	gpio5_146	safe_mode
AG26	-	vdds_bank21	-	-	-	-	-	-	-
AJ27	-	uart6_tx	-	-	sdio5_data3	usbb2_mm_rxdp	-	gpio5_149	safe_mode
AJ26	-	uart6_rx	-	-	sdio5_data2	usbb2_mm_rxdm	-	gpio5_150	safe_mode
AK26	-	uart6_cts	sys_ndmareq1	-	sdio5_data1	usbb2_mm_rxrcv	-	gpio5_151	safe_mode
AK27	-	uart6_rts	sys_ndmareq0	-	sdio5_data0	usbb2_mm_txse0	usbd0_ulpiphy_stp	gpio5_152	safe_mode
AJ28	-	uart3_cts_rctx	sata_actled	-	sdio5_data7	usbb2_mm_txen	usbd0_ulpiphy_data4	gpio5_153	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
AK28	-	uart3_rts_irsd	hdq_sio	-	sdio5_data6	usbb2_mm_txdat	usbd0_ulpiphy_data5	gpio5_154	safe_mode
AL28	-	uart3_tx_irtx	-	-	sdio5_data5	sdio4_clk	usbd0_ulpiphy_data6	gpio5_155	safe_mode
AM28	-	uart3_rx_irrx	-	-	sdio5_data4	sdio4_cmd	usbd0_ulpiphy_data7	gpio5_156	safe_mode
D29	-	usbb3_hsic_strobe	-	-	-	-	-	gpio5_158	safe_mode
D30	-	usbb3_hsic_data	-	-	-	-	-	gpio5_159	safe_mode
E8	-	vdda_sata	-	-	-	-	-	-	-
D8	-	vssa_sata	-	-	-	-	-	-	-
E6	-	sata_tx	-	-	-	-	-	-	-
D6	-	sata_ty	-	-	-	-	-	-	-
E7	-	sata_rx	-	-	-	-	-	-	-
D7	-	sata_ry	-	-	-	-	-	-	-
K7	-	vdds_sdcard	-	-	-	-	-	-	-
E3	-	sdcard_clk	-	-	jtag_rtck	-	n_clk	-	safe_mode
E2	-	sdcard_cmd	-	-	jtag_tdo	uart6_rx	-	n_d2	safe_mode
G3	-	sdcard_data0	-	-	jtag_tdi	-	n_d0	-	safe_mode
G2	-	sdcard_data1	-	-	jtag_ntrst	-	n_d1	-	safe_mode
F2	-	sdcard_data2	-	-	jtag_tmsc	-	n_d2	-	safe_mode
F3	-	sdcard_data3	-	-	jtag_tck	-	n_d3	-	safe_mode
AK18	-	vdds_usbhs18	-	-	-	-	-	-	-
AN22	-	vdda_usbhs33	-	-	-	-	-	-	-
AM19	-	vssa_usbhs	-	-	-	-	-	-	-
AM20	-	usbd0_hs_dp	-	-	-	uart3_rx_irrx	-	-	safe_mode
AL20	-	usbd0_hs_dm	-	-	-	uart3_tx_irtx	-	-	safe_mode
AL19	-	usbphy_ce	-	-	-	-	-	-	-
AL18	-	vdda_usbss18	-	-	-	-	-	-	-
AM18	-	vssa_usbss	-	-	-	-	-	-	-
AM21	-	usbd0_ss_tx	-	-	-	-	-	-	-
AL21	-	usbd0_ss_ty	-	-	-	-	-	-	-
AM22	-	usbd0_ss_rx	-	-	-	-	-	-	-
AL22	-	usbd0_ss_ry	-	-	-	-	-	-	-
G27	-	vdds_bank23	-	-	-	-	-	-	-
B30	-	drm_emu0	-	-	-	-	hw_wkdbg6	gpio1_wk6	safe_mode
B31	-	drm_emu1	-	-	-	-	hw_wkdbg7	gpio1_wk7	safe_mode
C32	-	jtag_ntrst	-	-	-	-	-	-	safe_mode
C31	-	jtag_tck	-	-	-	-	-	-	safe_mode
A33	-	jtag_rtck	-	-	-	-	-	-	safe_mode
B32	-	jtag_tmsc	-	-	-	-	-	-	safe_mode
A32	-	jtag_tdi	-	-	-	-	-	-	safe_mode
B33	-	jtag_tdo	-	-	-	-	-	-	safe_mode
J27	-	vdds_bank24	-	-	-	-	-	-	-
F32	-	sys_32k	-	-	-	-	-	-	-
E31	-	vssa_xtal	-	-	-	-	-	-	-
E32	-	fref_xtal_in	-	-	-	-	-	-	-
D32	-	fref_xtal_out	-	-	-	-	-	-	-
D31	-	fref_xtal_clk	-	-	-	-	-	-	-
B27	-	vdda_slicer	-	-	-	-	-	-	-
A27	-	vssa_slicer	-	-	-	-	-	-	-
B28	-	fref_slicer_in	-	-	-	-	-	-	-
H32	-	fref_clk_ioreq	-	-	-	-	-	gpio1_wk13	safe_mode
F30	-	fref_clk0_out	-	-	-	-	hw_wkdbg9	gpio1_wk12	safe_mode
K27	-	vdds_bank25	-	-	-	-	-	-	-
G32	-	fref_clk1_out	-	-	-	-	hw_wkdbg5	gpio1_wk11	safe_mode
G31	-	fref_clk2_out	-	-	-	-	hw_wkdbg10	gpio1_wk10	safe_mode
G29	-	fref_clk2_req	fref_clk3_out	-	sys_ndmareq0	-	hw_wkdbg11	gpio1_wk9	safe_mode

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
G30	-	fref_clk1_req	-	-	sys_ndmareq1	-	hw_wkdbg12	gpio1_wk8	safe_mode
F31	-	sys_nrespwron	-	-	-	-	-	-	-
F29	-	sys_nreswarm	-	-	-	-	-	-	-
N27	-	vdds_bank26	-	-	-	-	-	-	-
L31	-	sys_pwr_req	-	-	-	-	hw_wkdbg15	-	safe_mode
H29	-	sr_pmic_scl	-	-	-	-	-	-	-
J29	-	sr_pmic_sda	-	-	-	-	-	-	-
K30	-	sys_nirq1	-	-	-	-	-	gpio1_wk16	-
J30	-	sys_nirq2	-	-	-	-	-	gpio1_wk17	-
K29	-	i2c1_pmic_scl	-	-	-	-	-	-	-
H30	-	i2c1_pmic_sda	-	-	-	-	-	-	-
J31	-	sys_boot0	-	-	drm_emu2	drm_emu15	hw_wkdbg0	gpio1_wkout0	safe_mode
K31	-	sys_boot1	-	-	drm_emu3	drm_emu16	hw_wkdbg1	gpio1_wkout1	safe_mode
L32	-	sys_boot2	-	-	drm_emu4	drm_emu17	hw_wkdbg2	gpio1_wkout2	safe_mode
K32	-	sys_boot3	-	-	drm_emu5	drm_emu18	hw_wkdbg3	gpio1_wkout3	safe_mode
J32	-	sys_boot4	-	-	drm_emu6	drm_emu19	hw_wkdbg4	gpio1_wkout4	safe_mode
H31	-	sys_boot5	sys_aux_msecure	-	-	-	hw_wkdbg8	gpio1_wkout5	safe_mode
-	B20	ddrch1_dm0	-	-	-	-	-	-	-
-	C17	ddrch1_dm1	-	-	-	-	-	-	-
-	C26	ddrch1_dm2	-	-	-	-	-	-	-
-	A10	ddrch1_dm3	-	-	-	-	-	-	-
-	B25	ddrch1_dq0	-	-	-	-	-	-	-
-	B24	ddrch1_dq1	-	-	-	-	-	-	-
-	C23	ddrch1_dq2	-	-	-	-	-	-	-
-	B23	ddrch1_dq3	-	-	-	-	-	-	-
-	B22	ddrch1_dq4	-	-	-	-	-	-	-
-	A22	ddrch1_dq5	-	-	-	-	-	-	-
-	B21	ddrch1_dq6	-	-	-	-	-	-	-
-	A21	ddrch1_dq7	-	-	-	-	-	-	-
-	A15	ddrch1_dq8	-	-	-	-	-	-	-
-	B14	ddrch1_dq9	-	-	-	-	-	-	-
-	C13	ddrch1_dq10	-	-	-	-	-	-	-
-	B13	ddrch1_dq11	-	-	-	-	-	-	-
-	B12	ddrch1_dq12	-	-	-	-	-	-	-
-	A12	ddrch1_dq13	-	-	-	-	-	-	-
-	B11	ddrch1_dq14	-	-	-	-	-	-	-
-	A11	ddrch1_dq15	-	-	-	-	-	-	-
-	J27	ddrch1_dq16	-	-	-	-	-	-	-
-	J26	ddrch1_dq17	-	-	-	-	-	-	-
-	H27	ddrch1_dq18	-	-	-	-	-	-	-
-	H26	ddrch1_dq19	-	-	-	-	-	-	-
-	G26	ddrch1_dq20	-	-	-	-	-	-	-
-	G25	ddrch1_dq21	-	-	-	-	-	-	-
-	F26	ddrch1_dq22	-	-	-	-	-	-	-
-	E27	ddrch1_dq23	-	-	-	-	-	-	-
-	A8	ddrch1_dq24	-	-	-	-	-	-	-
-	C7	ddrch1_dq25	-	-	-	-	-	-	-
-	A7	ddrch1_dq26	-	-	-	-	-	-	-
-	B6	ddrch1_dq27	-	-	-	-	-	-	-
-	C5	ddrch1_dq28	-	-	-	-	-	-	-
-	B5	ddrch1_dq29	-	-	-	-	-	-	-
-	B4	ddrch1_dq30	-	-	-	-	-	-	-
-	A4	ddrch1_dq31	-	-	-	-	-	-	-
-	C19	ddrch1_dqs0	-	-	-	-	-	-	-
-	C15	ddrch1_dqs1	-	-	-	-	-	-	-
-	E26	ddrch1_dqs2	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[(1)] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
-	A9	ddrch1_dqs3	-	-	-	-	-	-	-
-	B19	ddrch1_ndqs0	-	-	-	-	-	-	-
-	B15	ddrch1_ndqs1	-	-	-	-	-	-	-
-	D27	ddrch1_ndqs2	-	-	-	-	-	-	-
-	B9	ddrch1_ndqs3	-	-	-	-	-	-	-
-	A17	ddrch1_vref_dq	-	-	-	-	-	-	-
A29 / A26 / A24 / A20 / A18 / A15 / A13 / A10 / A8 / A6 / D33 / G33 / G25 / G24 / G20 / G19 / G9 / H9 / L33 / L27 / M27	A24 / A19 / A14 / A5 / B16 / B7 / C21 / C11 / C9 / D26 / F27 / J25	vddq_ddr_ch1	-	-	-	-	-	-	-
-	U3	ddrch2_dm0	-	-	-	-	-	-	-
-	W1	ddrch2_dm1	-	-	-	-	-	-	-
-	J3	ddrch2_dm2	-	-	-	-	-	-	-
-	AG4	ddrch2_dm3	-	-	-	-	-	-	-
-	K2	ddrch2_dq0	-	-	-	-	-	-	-
-	L1	ddrch2_dq1	-	-	-	-	-	-	-
-	L3	ddrch2_dq2	-	-	-	-	-	-	-
-	M1	ddrch2_dq3	-	-	-	-	-	-	-
-	N1	ddrch2_dq4	-	-	-	-	-	-	-
-	N2	ddrch2_dq5	-	-	-	-	-	-	-
-	P1	ddrch2_dq6	-	-	-	-	-	-	-
-	P2	ddrch2_dq7	-	-	-	-	-	-	-
-	AA3	ddrch2_dq8	-	-	-	-	-	-	-
-	AB2	ddrch2_dq9	-	-	-	-	-	-	-
-	AC1	ddrch2_dq10	-	-	-	-	-	-	-
-	AC2	ddrch2_dq11	-	-	-	-	-	-	-
-	AD2	ddrch2_dq12	-	-	-	-	-	-	-
-	AD1	ddrch2_dq13	-	-	-	-	-	-	-
-	AE2	ddrch2_dq14	-	-	-	-	-	-	-
-	AF3	ddrch2_dq15	-	-	-	-	-	-	-
-	C2	ddrch2_dq16	-	-	-	-	-	-	-
-	D1	ddrch2_dq17	-	-	-	-	-	-	-
-	E1	ddrch2_dq18	-	-	-	-	-	-	-
-	E2	ddrch2_dq19	-	-	-	-	-	-	-
-	F1	ddrch2_dq20	-	-	-	-	-	-	-
-	F2	ddrch2_dq21	-	-	-	-	-	-	-
-	G2	ddrch2_dq22	-	-	-	-	-	-	-
-	G3	ddrch2_dq23	-	-	-	-	-	-	-
-	AG6	ddrch2_dq24	-	-	-	-	-	-	-
-	AF6	ddrch2_dq25	-	-	-	-	-	-	-
-	AF7	ddrch2_dq26	-	-	-	-	-	-	-
-	AE7	ddrch2_dq27	-	-	-	-	-	-	-
-	AF8	ddrch2_dq28	-	-	-	-	-	-	-
-	AG9	ddrch2_dq29	-	-	-	-	-	-	-
-	AE9	ddrch2_dq30	-	-	-	-	-	-	-
-	AG10	ddrch2_dq31	-	-	-	-	-	-	-
-	R2	ddrch2_dqs0	-	-	-	-	-	-	-
-	AA2	ddrch2_dqs1	-	-	-	-	-	-	-
-	H2	ddrch2_dqs2	-	-	-	-	-	-	-
-	AF5	ddrch2_dqs3	-	-	-	-	-	-	-
-	R3	ddrch2_ndqs0	-	-	-	-	-	-	-
-	AA1	ddrch2_ndqs1	-	-	-	-	-	-	-
-	J1	ddrch2_ndqs2	-	-	-	-	-	-	-
-	AG5	ddrch2_ndqs3	-	-	-	-	-	-	-
-	U1	ddrch2_vref_dq	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
E1 / H7 / H1 / J7 / L1 / N1 / P7 / R7 / T1 / V1 / AD7 / AD1 / AE7 / AG7 / AG5 / AG1 / AK1 / AN10 / AN7 / AN5	D2 / G1 / J2 / L2 / N3 / R1 / Y1 / AB1 / AF9 / AF4 / AF2 / AG7	vddq_ddr_ch2	-	-	-	-	-	-	-
-	AF22	lpddr2ch1_ca0	-	-	-	-	-	-	-
-	AG22	lpddr2ch1_ca1	-	-	-	-	-	-	-
-	AF20	lpddr2ch1_ca2	-	-	-	-	-	-	-
-	AG20	lpddr2ch1_ca3	-	-	-	-	-	-	-
-	AE19	lpddr2ch1_ca4	-	-	-	-	-	-	-
-	AE15	lpddr2ch1_ca5	-	-	-	-	-	-	-
-	AE13	lpddr2ch1_ca6	-	-	-	-	-	-	-
-	AF13	lpddr2ch1_ca7	-	-	-	-	-	-	-
-	AG13	lpddr2ch1_ca8	-	-	-	-	-	-	-
-	AF12	lpddr2ch1_ca9	-	-	-	-	-	-	-
-	AF17	lpddr2ch1_ck	-	-	-	-	-	-	-
-	AF18	lpddr2ch1_cke0	-	-	-	-	-	-	-
-	AG18	lpddr2ch1_cke1	-	-	-	-	-	-	-
-	AG17	lpddr2ch1_nck	-	-	-	-	-	-	-
-	AF19	lpddr2ch1_ncs0	-	-	-	-	-	-	-
-	AG19	lpddr2ch1_ncs1	-	-	-	-	-	-	-
-	AG15	lpddr2ch1_vref_ca_out	-	-	-	-	-	-	-
AG18	-	vddca_vref_lpddr2ch1	-	-	-	-	-	-	-
AJ23 / AJ22 / AN26 / AN20 / AN18	AF16 / AF14 / AG21	vddca_lpddr2ch1	-	-	-	-	-	-	-
-	L25	lpddr2ch2_ca0	-	-	-	-	-	-	-
-	M26	lpddr2ch2_ca1	-	-	-	-	-	-	-
-	N26	lpddr2ch2_ca2	-	-	-	-	-	-	-
-	N25	lpddr2ch2_ca3	-	-	-	-	-	-	-
-	P26	lpddr2ch2_ca4	-	-	-	-	-	-	-
-	W25	lpddr2ch2_ca5	-	-	-	-	-	-	-
-	Y27	lpddr2ch2_ca6	-	-	-	-	-	-	-
-	Y26	lpddr2ch2_ca7	-	-	-	-	-	-	-
-	AA27	lpddr2ch2_ca8	-	-	-	-	-	-	-
-	AA26	lpddr2ch2_ca9	-	-	-	-	-	-	-
-	T27	lpddr2ch2_ck	-	-	-	-	-	-	-
-	R25	lpddr2ch2_cke0	-	-	-	-	-	-	-
-	R27	lpddr2ch2_cke1	-	-	-	-	-	-	-
-	T26	lpddr2ch2_nck	-	-	-	-	-	-	-
-	R26	lpddr2ch2_ncs0	-	-	-	-	-	-	-
-	P27	lpddr2ch2_ncs1	-	-	-	-	-	-	-
-	V27	lpddr2ch2_vref_ca_out	-	-	-	-	-	-	-
AB27	-	vddca_vref_lpddr2ch2	-	-	-	-	-	-	-
T33 / AA33 / AC33 / AG29 / AH29	N27 / U26 / W26	vddca_lpddr2ch2	-	-	-	-	-	-	-
AN14	AG12	pop_lpddr2ch1_zq	-	-	-	-	-	-	-
AH33	AB27	pop_lpddr2ch2_zq	-	-	-	-	-	-	-
B2 / A31	B2 / B26	pop_vacc_lpddr2[4]	-	-	-	-	-	-	-
A21 / A30 / AJ33 / AL1 / AN12 / AN29 / C1 / P33 / Y1 / AA1	A18 / A25 / AC27 / AE1 / AG11 / AG23 / C1 / L26 / V1 / V2	pop_vdd1_lpddr2_shared	-	-	-	-	-	-	-
A3 / AF33 / AN13 / AN21 / AN28 / AN3 / A22 / C33 / N33 / Y33 / AB1 / AC1	A3 / AA25 / AE11 / AE17 / AF23 / AG3 / B18 / C27 / K27 / U25 / W2 / W3	pop_vdd2_lpddr2_shared	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[(1)] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
H26 / H25 / H8 / J26 / J8 / K14 / K13 / K12 / L14 / L13 / L12 / L11 / L8 / M13 / M12 / M11 / M10 / M8 / P14 / P13 / P12 / P11 / P10 / R14 / R13 / T14 / U22 / U21 / U20 / V23 / V22 / V21 / V20 / Y25 / Y24 / Y23 / AA23 / AA18 / AB25 / AB24 / AB23 / AB18 / AC23 / AC18 / AD25 / AD24 / AD23 / AE16 / AE15 / AE14 / AE13 / AE8 / AF9 / AF8	-	vdd_core	-	-	-	-	-	-	-
AC27	-	vdd_core_sense	-	-	-	-	-	-	-
R12 / R11 / R10 / R9 / T13 / T12 / T11 / T10 / T9 / W14 / W13 / W12 / W11 / W10 / W9 / Y22 / Y21 / Y19 / Y11 / Y10 / AA22 / AA19 / AA16 / AA15 / AA14 / AA13 / AA12 / AA11 / AA10 / AA9 / AB22 / AB21 / AB19 / AB11 / AB10 / AC22 / AC19 / AC16 / AC15 / AC14 / AC13 / AC12 / AC11 / AC10 / AC9 / AD22 / AD21 / AD19 / AD11 / AE11	-	vdd_mm	-	-	-	-	-	-	-
AJ21	-	vdd_mm_sense	-	-	-	-	-	-	-
H24 / H23 / H22 / H21 / H20 / H19 / K23 / K22 / K21 / K20 / K19 / K18 / K17 / L25 / L24 / L23 / L22 / L21 / L20 / L19 / L18 / L17 / P25 / P23 / P22 / P21 / P20 / P19 / P18 / P17 / R26 / R25 / R23 / R22 / R21 / R20	-	vdd_mpu	-	-	-	-	-	-	-
P26	-	vdd_mpu_sense	-	-	-	-	-	-	-
P26	-	vss_mpu_sense	-	-	-	-	-	-	-
AE5	-	vpp1	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics[1] (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
A28 / A25 / A19 / A16 / A14 / A12 / A9 / A7 / C2 / D3 / D2 / F33 / F1 / G17 / H33 / H18 / H17 / H16 / H15 / H14 / H13 / H12 / H11 / H10 / J25 / J24 / J23 / J22 / J21 / J20 / J19 / J18/ J17 / J16 / J15 / J14 / J13 / J12 / J11 / J10 / J9 / K26 / K25 / K24 / K16 / K15 / K11 / K10 / K9 / K8 / K1 / L26 / L16 / L15 / L10 / L9 / M33 / M26 / M25 / M24 / M23 / M22 / M21 / M20 / M19 / M18 / M17 / M16 / M15 / M14 / M9 / M1 / N26 / N25 / N24 / N23 / N22 / N21 / N20 / N19 / N18 / N17 / N16 / N15 / N14 / N13 / N12 / N11 / N10 / N9 / N8 / P24 / P16 / P15 / P9 / P8 / R33 / R24 / R19 / R18 / R17 / R16 / R15 / R8 / R1 / T26 / T25 / T24 / T23 / T22 / T21 / T20 / T19 / T18 / T17 / T16 / T15 / T8 / U27 / U26 / U25 / U24 / U23 / U19 / U18 / U17 / U16 / U15 / U14 / U13 / U12 / U11 / U10 / U9 / U8 / U7 / V25 / V24 / V19 / V18 / V17 / V16 / V15 / V14 / V13 / V12 / V11 / V10 / V9 / V8 / W26 / W25 / W24 / W23 / W22 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W8 / W1 / Y26 / Y20 / Y18 / Y17 / Y16 / Y15 / Y14 / Y13 / Y12 / Y9 / Y8 / AA26 / AA25 / AA24 / AA21 / AA20 / AA17 / AA8 / AA3 / AA2 / AE33 / AB26 / AB20 / AB17 / AB16 / AB15 / AB14 / AB13 / AB12 / AB9 / AB8 / AB7 / AC26 / AC25 / AC24 / AC21 / AC20 / AC17 / AC8 / AD33 / AD26 / AD20 / AD18 / AD17 / AD16 / AD15 / AD14 / AD13/ AD12 / AD10 / AD9 / AD8 / AE26 / AE25 / AE24 / AE23 / AE22 / AE21 / AE20 / AE19 / AE18 / AE17 / AE12 / AE10 / AE9 / AE1 / AF26 / AF25 / AF24 / AF23 / AF22 / AF21 / AF20 / AF19 / AF18 / AF17 / AF16 / AF15 / AF14 / AF13 / AF12 / AF11 / AF10 / AG33 / AG17 / AG10 / AG3 / AG2 / AH1 / AM32 / AM2 / AN25 / AN19 / AN11 / AN8 / AN6 / V7	A26 / A23 / A20 / A16 / A13 / A6 / A2 / B27 / B17 / B10 / B8 / B3 / B1 / E25 / E3 / G27 / H1 / K26 / K1 / L27 / M27 / M2 / T2 / T1 / U27 / U2 / V26 / W27 / Y2 / AB26 / AC3 / AE21 / AE5 / AF21 / AF15 / AF11 / AF10 / AF1 / AG16 / AG14 / AG8 / AG2	vss	-	-	-	-	-	-	-
V26	-	vdda_dpll_core_emu_abe	-	-	-	-	-	-	-
T7	-	vdda_dpll_mm_l4per	-	-	-	-	-	-	-
AG23	-	vdda_dpll_hdmi	-	-	-	-	-	-	-
V27	-	vdda_dpll_mpu	-	-	-	-	-	-	-
T5	-	vdda_ldo_core	-	-	-	-	-	-	-
AG15	-	vdda_ldo_mm	-	-	-	-	-	-	-
G14	-	vdda_ldo_mpu	-	-	-	-	-	-	-
V29	-	vdda_ldo_emu_wkup[2]	-	-	-	-	-	-	-

Table 2-2. Multiplexing Characteristics(1) (continued)

BOTTOM BALLS	TOP BALLS	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	MODE 7
W29	-	vnwa_emu_wkup(2)	-	-	-	-	-	-	-
Y7	-	vdda_vbgap_core	-	-	-	-	-	-	-
AG19	-	cap_vdda_ldo_ sram_core_array	-	-	-	-	-	-	-
AG16	-	cap_vdda_ldo_ sram_mm_array	-	-	-	-	-	-	-
G16	-	cap_vdda_ldo_ sram_mpu_array	-	-	-	-	-	-	-
T27	-	cap_vddldo_emu_ wkup	-	-	-	-	-	-	-
AJ16	-	cap_vbb_ldo_mm	-	-	-	-	-	-	-
E16	-	cap_vbb_ldo_mpu	-	-	-	-	-	-	-
N7	-	cap_vdda_ldo_ sram_mpu_array2	-	-	-	-	-	-	-

(1) NA in table stands for Not Applicable.

(2) **CAUTION**: vnwa_emu_wkup and vdda_ldo_emu_wlup must be connected on the board.

(3) gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AJ10 / AK10 / AJ11 / AK11 / AJ12 / AK12 / AC2 / AC3) can output the same GPIO in mode 0 or in mode 5.

(4) pop_vacc_lpddr2 must be left unconnected.

2.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The name of the signal passing through the pin.

NOTE

The subsystem multiplexing signals are not described in Table 2-1 and Table 2-2.

2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input or output
   - D = Open Drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground
4. **BALL BOTTOM:** Associated ball(s) bottom
5. **BALL TOP:** Associated ball(s) top
6. **PIN NAME:** This is the name of the pin the signal is passing through.

2.4.1 External Memory Interfaces

2.4.1.1 GPMC

NOTE

For more information, see the Memory Subsystem / General-Purpose Memory Controller section of the OMAP543x TRM.

Table 2-3. GPMC Signal Descriptions

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Multiplexed GPMC Mode					
gpmc_a1 / gpmc_d0	gpmc_ad0	GPMC address bit 1 / data bit 0	IO	B21	-
gpmc_a2 / gpmc_d1	gpmc_ad1	GPMC address bit 2 / data bit 1	IO	C21	-
gpmc_a3 / gpmc_d2	gpmc_ad2	GPMC address bit 3 / data bit 2	IO	B20	-
gpmc_a4 / gpmc_d3	gpmc_ad3	GPMC address bit 4 / data bit 3	IO	C20	-
gpmc_a5 / gpmc_d4	gpmc_ad4	GPMC address bit 5 / data bit 4	IO	B19	-
gpmc_a6 / gpmc_d5	gpmc_ad5	GPMC address bit 6 / data bit 5	IO	C19	-
gpmc_a7 / gpmc_d6	gpmc_ad6	GPMC address bit 7 / data bit 6	IO	B18	-
gpmc_a8 / gpmc_d7	gpmc_ad7	GPMC address bit 8 / data bit 7	IO	C18	-
gpmc_a9 / gpmc_d8	gpmc_ad8	GPMC address bit 9 / data bit 8	IO	E26	-
gpmc_a10 / gpmc_d9	gpmc_ad9	GPMC address bit 10 / data bit 9	IO	D26	-
gpmc_a11 / gpmc_d10	gpmc_ad10	GPMC address bit 11 / data bit 10	IO	E25	-
gpmc_a12 / gpmc_d11	gpmc_ad11	GPMC address bit 12 / data bit 11	IO	D25	-
gpmc_a13 / gpmc_d12	gpmc_ad12	GPMC address bit 13 / data bit 12	IO	E24	-
gpmc_a14 / gpmc_d13	gpmc_ad13	GPMC address bit 14 / data bit 13	IO	D24	-
gpmc_a15 / gpmc_d14	gpmc_ad14	GPMC address bit 15 / data bit 14	IO	E23	-
gpmc_a16 / gpmc_d15	gpmc_ad15	GPMC address bit 16 / data bit 15	IO	D23	-
gpmc_a17	gpmc_a16	GPMC address bit 17	O	E21	-
gpmc_a18	gpmc_a17	GPMC address bit 18	O	D21	-
gpmc_a19	gpmc_a18	GPMC address bit 19	O	E20	-
gpmc_a20	gpmc_a19	GPMC address bit 20	O	D20	-
gpmc_a21	gpmc_a20	GPMC address bit 21	O	E19	-
gpmc_a22	gpmc_a21	GPMC address bit 22	O	D19	-
gpmc_a23	gpmc_a22	GPMC address bit 23	O	E18	-
gpmc_a24	gpmc_a23	GPMC address bit 24	O	D18	-
gpmc_a25	gpmc_a24	GPMC address bit 25	O	B8	-
gpmc_a26	gpmc_a25	GPMC address bit 26	O	C8	-
Nonmultiplexed GPMC Mode					
gpmc_d0	gpmc_ad0	GPMC data bit 0	IO	B21	-
gpmc_d1	gpmc_ad1	GPMC data bit 1	IO	C21	-
gpmc_d2	gpmc_ad2	GPMC data bit 2	IO	B20	-
gpmc_d3	gpmc_ad3	GPMC data bit 3	IO	C20	-
gpmc_d4	gpmc_ad4	GPMC data bit 4	IO	B19	-
gpmc_d5	gpmc_ad5	GPMC data bit 5	IO	C19	-
gpmc_d6	gpmc_ad6	GPMC data bit 6	IO	B18	-
gpmc_d7	gpmc_ad7	GPMC data bit 7	IO	C18	-
gpmc_d8	gpmc_ad8	GPMC data bit 8	IO	E26	-
gpmc_d9	gpmc_ad9	GPMC data bit 9	IO	D26	-
gpmc_d10	gpmc_ad10	GPMC data bit 10	IO	E25	-
gpmc_d11	gpmc_ad11	GPMC data bit 11	IO	D25	-
gpmc_d12	gpmc_ad12	GPMC data bit 12	IO	E24	-
gpmc_d13	gpmc_ad13	GPMC data bit 13	IO	D24	-

Table 2-3. GPMC Signal Descriptions (continued)

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpmc_d14	gpmc_ad14	GPMC data bit 14	IO	E23	-
gpmc_d15	gpmc_ad15	GPMC data bit 15	IO	D23	-
gpmc_a1	gpmc_a16	GPMC address bit 1	O	E21	-
gpmc_a2	gpmc_a17	GPMC address bit 2	O	D21	-
gpmc_a3	gpmc_a18	GPMC address bit 3	O	E20	-
gpmc_a4	gpmc_a19	GPMC address bit 4	O	D20	-
gpmc_a5	gpmc_a20	GPMC address bit 5	O	E19	-
gpmc_a6	gpmc_a21	GPMC address bit 6	O	D19	-
gpmc_a7	gpmc_a22	GPMC address bit 7	O	E18	-
gpmc_a8	gpmc_a23	GPMC address bit 8	O	D18	-
gpmc_a9	gpmc_a24	GPMC address bit 9	O	B8	-
gpmc_a10	gpmc_a25	GPMC address bit 10	O	C8	-
Common GPMC Signals					
gpmc_ncs0	gpmc_ncs0	GPMC chip select 0 invert	O	E29	-
gpmc_ncs1	gpmc_ncs1	GPMC chip select 1 invert	O	C10	-
gpmc_ncs2	gpmc_ncs2	GPMC chip select 2 invert	O	B10	-
gpmc_ncs3	gpmc_ncs3	GPMC chip select 3 invert	O	B9	-
gpmc_ncs4	gpmc_ncs4	GPMC chip select 4 invert	O	C9	-
gpmc_ncs5	gpmc_ncs5	GPMC chip select 5 invert	O	C6	-
gpmc_ncs6	gpmc_ncs6	GPMC chip select 6 invert	O	B6	-
gpmc_ncs7	gpmc_ncs7	GPMC chip select 7 invert	O	E10	-
gpmc_nwp	gpmc_nwp	GPMC flash write protect invert	O	B22	-
gpmc_clk	gpmc_clk	GPMC clock	O	C22	-
gpmc_nadv_ale	gpmc_nadv_ale	GPMC address valid invert (or address latch enable for NAND protocol memories)	O	E22	-
gpmc_noe_nre	gpmc_noe	GPMC output enable invert (or read enable invert for NAND protocol memories)	O	B5	-
gpmc_nwe	gpmc_nwe	GPMC write enable invert	O	C5	-
gpmc_nbe0_cle	gpmc_nbe0_cle	GPMC lower-byte enable invert (or command latch enable for NAND protocol memories)	O	D22	-
gpmc_nbe1	gpmc_nbe1	GPMC upper-byte enable invert	O	B22	-
gpmc_wait0	gpmc_wait0	GPMC external indication of wait 0	I	C29	-
gpmc_wait1	gpmc_wait1	GPMC external indication of wait 1	I	C7	-
gpmc_wait2	gpmc_wait2	GPMC external indication of wait 2	I	B7	-
gpmc_wait3	gpmc_wait3	GPMC external indication of wait 3	I	E9	-

2.4.1.2 LPDDR2

NOTE

For more information, see the Memory Subsystem / EMIF Controller section of the OMAP543x TRM.

Table 2-4. LPDDR2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
LPDDR2 Channel 1				
LPDDR2 Channel 1—Common Balls Between POP OMAP5430 LPDDR2 and Bottom OMAP5432 DDR3				
ddrch1_dm0	LPDDR2 Channel 1 data mask 0	IO	-	B20
ddrch1_dm1	LPDDR2 Channel 1 data mask 1	IO	-	C17
ddrch1_dm2	LPDDR2 Channel 1 data mask 2	IO	-	C26
ddrch1_dm3	LPDDR2 Channel 1 data mask 3	IO	-	A10
ddrch1_dq0	LPDDR2 Channel 1 data bit 0	IO	-	B25
ddrch1_dq1	LPDDR2 Channel 1 data bit 1	IO	-	B24
ddrch1_dq2	LPDDR2 Channel 1 data bit 2	IO	-	C23
ddrch1_dq3	LPDDR2 Channel 1 data bit 3	IO	-	B23
ddrch1_dq4	LPDDR2 Channel 1 data bit 4	IO	-	B22
ddrch1_dq5	LPDDR2 Channel 1 data bit 5	IO	-	A22
ddrch1_dq6	LPDDR2 Channel 1 data bit 6	IO	-	B21
ddrch1_dq7	LPDDR2 Channel 1 data bit 7	IO	-	A21
ddrch1_dq8	LPDDR2 Channel 1 data bit 8	IO	-	A15
ddrch1_dq9	LPDDR2 Channel 1 data bit 9	IO	-	B14
ddrch1_dq10	LPDDR2 Channel 1 data bit 10	IO	-	C13
ddrch1_dq11	LPDDR2 Channel 1 data bit 11	IO	-	B13
ddrch1_dq12	LPDDR2 Channel 1 data bit 12	IO	-	B12
ddrch1_dq13	LPDDR2 Channel 1 data bit 13	IO	-	A12
ddrch1_dq14	LPDDR2 Channel 1 data bit 14	IO	-	B11
ddrch1_dq15	LPDDR2 Channel 1 data bit 15	IO	-	A11
ddrch1_dq16	LPDDR2 Channel 1 data bit 16	IO	-	J27
ddrch1_dq17	LPDDR2 Channel 1 data bit 17	IO	-	J26
ddrch1_dq18	LPDDR2 Channel 1 data bit 18	IO	-	H27
ddrch1_dq19	LPDDR2 Channel 1 data bit 19	IO	-	H26
ddrch1_dq20	LPDDR2 Channel 1 data bit 20	IO	-	G26
ddrch1_dq21	LPDDR2 Channel 1 data bit 21	IO	-	G25
ddrch1_dq22	LPDDR2 Channel 1 data bit 22	IO	-	F26
ddrch1_dq23	LPDDR2 Channel 1 data bit 23	IO	-	E27
ddrch1_dq24	LPDDR2 Channel 1 data bit 24	IO	-	A8
ddrch1_dq25	LPDDR2 Channel 1 data bit 25	IO	-	C7
ddrch1_dq26	LPDDR2 Channel 1 data bit 26	IO	-	A7
ddrch1_dq27	LPDDR2 Channel 1 data bit 27	IO	-	B6
ddrch1_dq28	LPDDR2 Channel 1 data bit 28	IO	-	C5
ddrch1_dq29	LPDDR2 Channel 1 data bit 29	IO	-	B5
ddrch1_dq30	LPDDR2 Channel 1 data bit 30	IO	-	B4
ddrch1_dq31	LPDDR2 Channel 1 data bit 31	IO	-	A4
ddrch1_dqs0	LPDDR2 Channel 1 data strobe 0	IO	-	C19
ddrch1_dqs1	LPDDR2 Channel 1 data strobe 1	IO	-	C15
ddrch1_dqs2	LPDDR2 Channel 1 data strobe 2	IO	-	E26

Table 2-4. LPDDR2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
ddrch1_dqs3	LPDDR2 Channel 1 data strobe 3	IO	-	A9
ddrch1_ndqs0	LPDDR2 Channel 1 negative data strobe 0	IO	-	B19
ddrch1_ndqs1	LPDDR2 Channel 1 negative data strobe 1	IO	-	B15
ddrch1_ndqs2	LPDDR2 Channel 1 negative data strobe 2	IO	-	D27
ddrch1_ndqs3	LPDDR2 Channel 1 negative data strobe 3	IO	-	B9
ddrch1_vref_dq	LPDDR2 Channel 1 DQ reference voltage	AO	-	A17
LPDDR2 Channel 1—Available on OMAP5430 POP LPDDR2 Only				
lpddr2ch1_ca0	LPDDR2 Channel 1—LPDDR2 command / address bit 0	O	-	AF22
lpddr2ch1_ca1	LPDDR2 Channel 1—LPDDR2 command / address bit 1	O	-	AG22
lpddr2ch1_ca2	LPDDR2 Channel 1—LPDDR2 command / address bit 2	O	-	AF20
lpddr2ch1_ca3	LPDDR2 Channel 1—LPDDR2 command / address bit 3	O	-	AG20
lpddr2ch1_ca4	LPDDR2 Channel 1—LPDDR2 command / address bit 4	O	-	AE19
lpddr2ch1_ca5	LPDDR2 Channel 1—LPDDR2 command / address bit 5	O	-	AE15
lpddr2ch1_ca6	LPDDR2 Channel 1—LPDDR2 command / address bit 6	O	-	AE13
lpddr2ch1_ca7	LPDDR2 Channel 1—LPDDR2 command / address bit 7	O	-	AF13
lpddr2ch1_ca8	LPDDR2 Channel 1—LPDDR2 command / address bit 8	O	-	AG13
lpddr2ch1_ca9	LPDDR2 Channel 1—LPDDR2 command / address bit 9	O	-	AF12
lpddr2ch1_ck	LPDDR2 Channel 1—LPDDR2 differential clock	O	-	AF17
lpddr2ch1_cke0	LPDDR2 Channel 1—LPDDR2 Clock enable for die 0	O	-	AF18
lpddr2ch1_cke1	LPDDR2 Channel 1—LPDDR2 Clock enable for die 1	O	-	AG18
lpddr2ch1_nck	LPDDR2 Channel 1—LPDDR2 negative differential clock	O	-	AG17
lpddr2ch1_ncs0	LPDDR2 Channel 1—LPDDR2 die select 0	O	-	AF19
lpddr2ch1_ncs1	LPDDR2 Channel 1—LPDDR2 die select 1	O	-	AG19
lpddr2ch1_vref_ca_out	LPDDR2 Channel 1—LPDDR2 CA reference voltage	AO	-	AG15
LPDDR2 Channel 2				
LPDDR2 Channel 2—Common Balls Between POP OMAP5430 LPDDR2 and Bottom OMAP5432 DDR3				
ddrch2_dm0	LPDDR2 Channel 2 data mask 0	IO	-	U3
ddrch2_dm1	LPDDR2 Channel 2 data mask 1	IO	-	W1
ddrch2_dm2	LPDDR2 Channel 2 data mask 2	IO	-	J3
ddrch2_dm3	LPDDR2 Channel 2 data mask 3	IO	-	AG4
ddrch2_dq0	LPDDR2 Channel 2 data bit 0	IO	-	K2
ddrch2_dq1	LPDDR2 Channel 2 data bit 1	IO	-	L1
ddrch2_dq2	LPDDR2 Channel 2 data bit 2	IO	-	L3
ddrch2_dq3	LPDDR2 Channel 2 data bit 3	IO	-	M1
ddrch2_dq4	LPDDR2 Channel 2 data bit 4	IO	-	N1
ddrch2_dq5	LPDDR2 Channel 2 data bit 5	IO	-	N2
ddrch2_dq6	LPDDR2 Channel 2 data bit 6	IO	-	P1
ddrch2_dq7	LPDDR2 Channel 2 data bit 7	IO	-	P2

Table 2-4. LPDDR2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
ddrch2_dq8	LPDDR2 Channel 2 data bit 8	IO	-	AA3
ddrch2_dq9	LPDDR2 Channel 2 data bit 9	IO	-	AB2
ddrch2_dq10	LPDDR2 Channel 2 data bit 10	IO	-	AC1
ddrch2_dq11	LPDDR2 Channel 2 data bit 11	IO	-	AC2
ddrch2_dq12	LPDDR2 Channel 2 data bit 12	IO	-	AD2
ddrch2_dq13	LPDDR2 Channel 2 data bit 13	IO	-	AD1
ddrch2_dq14	LPDDR2 Channel 2 data bit 14	IO	-	AE2
ddrch2_dq15	LPDDR2 Channel 2 data bit 15	IO	-	AF3
ddrch2_dq16	LPDDR2 Channel 2 data bit 16	IO	-	C2
ddrch2_dq17	LPDDR2 Channel 2 data bit 17	IO	-	D1
ddrch2_dq18	LPDDR2 Channel 2 data bit 18	IO	-	E1
ddrch2_dq19	LPDDR2 Channel 2 data bit 19	IO	-	E2
ddrch2_dq20	LPDDR2 Channel 2 data bit 20	IO	-	F1
ddrch2_dq21	LPDDR2 Channel 2 data bit 21	IO	-	F2
ddrch2_dq22	LPDDR2 Channel 2 data bit 22	IO	-	G2
ddrch2_dq23	LPDDR2 Channel 2 data bit 23	IO	-	G3
ddrch2_dq24	LPDDR2 Channel 2 data bit 24	IO	-	AG6
ddrch2_dq25	LPDDR2 Channel 2 data bit 25	IO	-	AF6
ddrch2_dq26	LPDDR2 Channel 2 data bit 26	IO	-	AF7
ddrch2_dq27	LPDDR2 Channel 2 data bit 27	IO	-	AE7
ddrch2_dq28	LPDDR2 Channel 2 data bit 28	IO	-	AF8
ddrch2_dq29	LPDDR2 Channel 2 data bit 29	IO	-	AG9
ddrch2_dq30	LPDDR2 Channel 2 data bit 30	IO	-	AE9
ddrch2_dq31	LPDDR2 Channel 2 data bit 31	IO	-	AG10
ddrch2_dqs0	LPDDR2 Channel 2 data strobe 0	IO	-	R2
ddrch2_dqs1	LPDDR2 Channel 2 data strobe 1	IO	-	AA2
ddrch2_dqs2	LPDDR2 Channel 2 data strobe 2	IO	-	H2
ddrch2_dqs3	LPDDR2 Channel 2 data strobe 3	IO	-	AF5
ddrch2_ndqs0	LPDDR2 Channel 2 negative data strobe 0	IO	-	R3
ddrch2_ndqs1	LPDDR2 Channel 2 negative data strobe 1	IO	-	AA1
ddrch2_ndqs2	LPDDR2 Channel 2 negative data strobe 2	IO	-	J1
ddrch2_ndqs3	LPDDR2 Channel 2 negative data strobe 3	IO	-	AG5
ddrch2_vref_dq	LPDDR2 Channel 2 DQ reference voltage	AO	-	U1
LPDDR2—Channel 2 —Available on OMAP5430 POP LPDDR2 Only				
lpddr2ch2_ca0	LPDDR2 Channel 2—LPDDR2 command / address bit 0	O	-	L25
lpddr2ch2_ca1	LPDDR2 Channel 2—LPDDR2 command / address bit 1	O	-	M26
lpddr2ch2_ca2	LPDDR2 Channel 2—LPDDR2 command / address bit 2	O	-	N26
lpddr2ch2_ca3	LPDDR2 Channel 2—LPDDR2 command / address bit 3	O	-	N25
lpddr2ch2_ca4	LPDDR2 Channel 2—LPDDR2 command / address bit 4	O	-	P26
lpddr2ch2_ca5	LPDDR2 Channel 2—LPDDR2 command / address bit 5	O	-	W25
lpddr2ch2_ca6	LPDDR2 Channel 2—LPDDR2 command / address bit 6	O	-	Y27
lpddr2ch2_ca7	LPDDR2 Channel 2—LPDDR2 command / address bit 7	O	-	Y26

Table 2-4. LPDDR2 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
lpddr2ch2_ca8	LPDDR2 Channel 2—LPDDR2 command / address bit 8	O	-	AA27
lpddr2ch2_ca9	LPDDR2 Channel 2—LPDDR2 command / address bit 9	O	-	AA26
lpddr2ch2_ck	LPDDR2 Channel 2—LPDDR2 differential clock	O	-	T27
lpddr2ch2_cke0	LPDDR2 Channel 2—LPDDR2 Clock enable for die 0	O	-	R25
lpddr2ch2_cke1	LPDDR2 Channel 2—LPDDR2 Clock enable for die 1	O	-	R27
lpddr2ch2_nck	LPDDR2 Channel 2—LPDDR2 negative differential clock	O	-	T26
lpddr2ch2_ncs0	LPDDR2 Channel 2—LPDDR2 die select 0	O	-	R26
lpddr2ch2_ncs1	LPDDR2 Channel 2—LPDDR2 die select 1	O	-	P27
lpddr2ch2_vref_ca_out	LPDDR2 Channel 2—LPDDR2 CA reference voltage	AO	-	V27
POP LPDDR2 Feedthrough				
pop_lpddr2ch1_zq	LPDDR2 Channel 1—LPDDR2 Feedthrough to top lpddr2 ZQ pin	FEED	-	AG12
pop_lpddr2ch2_zq	LPDDR2 Channel 2—LPDDR2 Feedthrough to top lpddr2 ZQ pin	FEED	-	AB27

2.4.2 Camera Interfaces

NOTE

For more information, see the Imaging Subsystem / ISS Interfaces section of the OMAP543x TRM.

2.4.2.1 Camera Control

Table 2-5. CAM Control Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
cam_shutter	Mechanical shutter	O	AD3 / AD2	-
cam_strobe	Flash trigger	O	AD4 / E13	-
cam_globalreset	Sensor reset	IO	AD2	-

2.4.2.2 CSI-2 MIPI D-PHY

Table 2-6. CSI-2 MIPI D-PHY Signal Descriptions

PIN NAME [6]	SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Main Camera—MIPI CSI-2 Port A					
csiporta_lane0x	MIPI CSI-2_lane0x	MIPI CSI-2 (Port A) camera lane 0 differential x	IDS	R2	-
csiporta_lane0y	MIPI CSI-2_lane0y	MIPI CSI-2 (Port A) camera lane 0 differential y	IDS	R3	-
csiporta_lane1x	MIPI CSI-2_lane1x	MIPI CSI-2 (Port A) camera lane 1 differential x	IDS	P2	-
csiporta_lane1y	MIPI CSI-2_lane1y	MIPI CSI-2 (Port A) camera lane 1 differential y	IDS	P3	-
csiporta_lane2x	MIPI CSI-2_lane2x	MIPI CSI-2 (Port A) camera lane 2 differential x	IDS	N2	-

Table 2-6. CSI-2 MIPI D-PHY Signal Descriptions (continued)

PIN NAME [6]	SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
csiporta_lane2y	MIPI CSI-2_lane2y	MIPI CSI-2 (Port A) camera lane 2 differential y	IDS	N3	-
csiporta_lane3x	MIPI CSI-2_lane3x	MIPI CSI-2 (Port A) camera lane 3 differential x	IDS	M2	-
csiporta_lane3y	MIPI CSI-2_lane3y	MIPI CSI-2 (Port A) camera lane 3 differential y	IDS	M3	-
csiporta_lane4x	MIPI CSI-2_lane4x	MIPI CSI-2 (Port A) camera lane 4 differential x	IDS	L2	-
csiporta_lane4y	MIPI CSI-2_lane4y	MIPI CSI-2 (Port A) camera lane 4 differential y	IDS	L3	-
Auxiliary Camera—MIPI CSI-2 Port B					
csiportb_lane0x	MIPI CSI-2_lane0x	MIPI CSI-2 (Port B) camera lane 0 differential x	IDS	V3	-
csiportb_lane0y	MIPI CSI-2_lane0y	MIPI CSI-2 (Port B) camera lane 0 differential y	IDS	V2	-
csiportb_lane1x	MIPI CSI-2_lane1x	MIPI CSI-2 (Port B) camera lane 1 differential x	IDS	W3	-
csiportb_lane1y	MIPI CSI-2_lane1y	MIPI CSI-2 (Port B) camera lane 1 differential y	IDS	W2	-
csiportb_lane2x	MIPI CSI-2_lane2x	MIPI CSI-2 (Port B) camera lane 2 differential x	IDS	Y3	-
csiportb_lane2y	MIPI CSI-2_lane2y	MIPI CSI-2 (Port B) camera lane 2 differential y	IDS	Y2	-
Second Camera—MIPI CSI-2 Port C					
csiportc_lane0x	MIPI CSI-2_lane0x	MIPI CSI-2 (Port C) camera lane 1 differential x	IDS	K2	-
csiportc_lane0y	MIPI CSI-2_lane0y	MIPI CSI-2 (Port C) camera lane 1 differential y	IDS	K3	-
csiportc_lane1x	MIPI CSI-2_lane1x	MIPI CSI-2 (Port C) camera lane 0 differential x	IDS	J2	-
csiportc_lane1y	MIPI CSI-2_lane1y	MIPI CSI-2 (Port C) camera lane 0 differential y	IDS	J3	-

2.4.2.3 CCP2 PHY

Table 2-7. CCP2 PHY Signal Descriptions

PIN NAME [6]	SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Auxiliary Camera—CCPV2 Port B					
csiportb_lane1x	ccpv2_lane1x	CCPV2 (Port B) camera lane 1 differential x	IDS	W3	-
csiportb_lane1y	ccpv2_lane1y	CCPV2 (Port B) camera lane 1 differential y	IDS	W2	-
csiportb_lane2x	ccpv2_lane2x	CCPV2 (Port B) camera lane 2 differential x	IDS	Y3	-
csiportb_lane2y	ccpv2_lane2y	CCPV2 (Port B) camera lane 2 differential y	IDS	Y2	-
Second Camera—CCPV2 Port C					
csiportc_lane1x	ccpv2_lane1x	CCPV2 (Port C) camera lane 0 differential x	IDS	J2	-
csiportc_lane1y	ccpv2_lane1y	CCPV2 (Port C) camera lane 0 differential y	IDS	J3	-
csiportc_lane0x	ccpv2_lane0x	CCPV2 (Port C) camera lane 1 differential x	IDS	K2	-
csiportc_lane0y	ccpv2_lane0y	CCPV2 (Port C) camera lane 1 differential y	IDS	K3	-

2.4.2.4 CPI

Table 2-8. CPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
cpi_pclk	CPI pixel clock	I	R2	-
cpi_hsync	CPI horizontal synchronization: line trigger	IO	AC2	-
cpi_vsync	CPI vertical synchronization: frame trigger	IO	AC3	-
cpi_hsyncin	CPI input-only version of cpi_hsynck	I	Y2	-
cpi_vsyncin	CPI input-only version of cpi_vsynck	I	Y3	-
cpi_data0	CPI data bit 0	I	P3	-
cpi_data1	CPI data bit 1	I	P2	-
cpi_data2	CPI data bit 2	I	N3	-
cpi_data3	CPI data bit 3	I	N2	-
cpi_data4	CPI data bit 4	I	M2	-
cpi_data5	CPI data bit 5	I	M3	-
cpi_data6	CPI data bit 6	I	L2	-
cpi_data7	CPI data bit 7	I	L3	-
cpi_data8	CPI data bit 8	I	K3	-
cpi_data9	CPI data bit 9	I	K2	-
cpi_data10	CPI data bit 10	I	J3	-
cpi_data11	CPI data bit 11	I	J2	-
cpi_data12	CPI data bit 12	I	V3 / AF3	- / -
cpi_data13	CPI data bit 13	I	V2 / AF2	- / -
cpi_data14	CPI data bit 14	I	W2 / AE3	- / -
cpi_data15	CPI data bit 15	I	W3 / AE2	- / -
cpi_wen	CPI external write enable	I	R3	-
cpi_fid	CPI field identification, for interlaced sensors (I mode)	I	AD2	-

2.4.3 Display

NOTE

For more information, see the Display Subsystem / Display Subsystem Overview / DSS Environment section of the OMAP543x TRM.

2.4.3.1 DSI-1 MIPI D-PHY

Table 2-9. DSI-1 MIPI D-PHY Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
DSI Port A				
dsiporta_lane0x	DSI (Port A) lane 0 differential positive or negative	ODS	Y32	-
dsiporta_lane0y	DSI (Port A) lane 0 differential positive or negative	ODS	Y31	-
dsiporta_lane1x	DSI (Port A) lane 1 differential positive or negative	ODS	W32	-
dsiporta_lane1y	DSI (Port A) lane 1 differential positive or negative	ODS	W31	-
dsiporta_lane2x	DSI (Port A) lane 2 differential positive or negative	ODS	V32	-
dsiporta_lane2y	DSI (Port A) lane 2 differential positive or negative	ODS	V31	-
dsiporta_lane3x	DSI (Port A) lane 3 differential positive or negative	ODS	T32	-
dsiporta_lane3y	DSI (Port A) lane 3 differential positive or negative	ODS	T31	-

Table 2-9. DSI-1 MIPI D-PHY Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dsiporta_lane4x	DSI (Port A) lane 4 differential positive or negative	ODS	R32	-
dsiporta_lane4y	DSI (Port A) lane 4 differential positive or negative	ODS	R31	-
dsiporta_te0	DSI (Port A) tearing effect control input	I	W30	-
DSI Port C				
dsiportc_lane0x	DSI (Port C) lane 0 differential positive or negative	ODS	AF32	-
dsiportc_lane0y	DSI (Port C) lane 0 differential positive or negative	ODS	AF31	-
dsiportc_lane1x	DSI (Port C) lane 1 differential positive or negative	ODS	AE32	-
dsiportc_lane1y	DSI (Port C) lane 1 differential positive or negative	ODS	AE31	-
dsiportc_lane2x	DSI (Port C) lane 2 differential positive or negative	ODS	AD32	-
dsiportc_lane2y	DSI (Port C) lane 2 differential positive or negative	ODS	AD31	-
dsiportc_lane3x	DSI (Port C) lane 3 differential positive or negative	ODS	AC32	-
dsiportc_lane3y	DSI (Port C) lane 3 differential positive or negative	ODS	AC31	-
dsiportc_lane4x	DSI (Port A) lane 4 differential positive or negative	ODS	AB32	-
dsiportc_lane4y	DSI (Port A) lane 4 differential positive or negative	ODS	AB31	-
dsiportc_te0	DSI (Port C) tearing effect control input	I	AB29	-

2.4.3.2 HDMI PHY

Table 2-10. HDMI PHY Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
hdmi_cec	HDMI consumer electronic control	IOD	AK25	-
hdmi_hpd	HDMI display hot plug detect	I	AJ25	-
hdmi_ddc_scl	HDMI display data channel clock	IOD	AK24	-
hdmi_ddc_sda	HDMI display data channel data	IOD	AJ24	-
hdmi_clkx	HDMI clock differential positive or negative	ODS	AM23	-
hdmi_clky	HDMI clock differential positive or negative	ODS	AL23	-
hdmi_data0x	HDMI data 0 differential positive or negative	ODS	AM24	-
hdmi_data0y	HDMI data 0 differential positive or negative	ODS	AL24	-
hdmi_data1x	HDMI data 1 differential positive or negative	ODS	AM25	-
hdmi_data1y	HDMI data 1 differential positive or negative	ODS	AL25	-
hdmi_data2x	HDMI data 2 differential positive or negative	ODS	AM26	-
hdmi_data2y	HDMI data 2 differential positive or negative	ODS	AL26	-

2.4.3.3 RFBI

Table 2-11. RFBI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
rfbi_data0	RFBI data bit 0	IO	AM6	-
rfbi_data1	RFBI data bit 1	IO	AL7	-
rfbi_data2	RFBI data bit 2	IO	AJ6	-
rfbi_data3	RFBI data bit 3	IO	AM7	-
rfbi_data4	RFBI data bit 4	IO	AM8	-
rfbi_data5	RFBI data bit 5	IO	AL8	-
rfbi_data6	RFBI data bit 6	IO	AM10	-
rfbi_data7	RFBI data bit 7	IO	AL10	-
rfbi_data8	RFBI data bit 8	IO	AK5	-
rfbi_data9	RFBI data bit 9	IO	AJ5	-
rfbi_data10	RFBI data bit 10	IO	AL5	-
rfbi_data11	RFBI data bit 11	IO	AL6	-
rfbi_data12	RFBI data bit 12	IO	AJ8	-
rfbi_data13	RFBI data bit 13	IO	AM9	-
rfbi_data14	RFBI data bit 14	IO	AL9	-
rfbi_data15	RFBI data bit 15	IO	AJ9	-
rfbi_a0	RFBI data / control selection	O	AM5	-
rfbi_we	RFBI write enable	O	AK8	-
rfbi_re	RFBI read enable	O	AK9	-
rfbi_cs0	RFBI chip select	O	AK6	-
rfbi_te_vsync0	RFBI vertical synchronization / tearing effect control signal	I	AJ7	-
rfbi_hsync0	RFBI horizontal synchronization / tearing effect control signal	I	AK7	-

2.4.3.4 DISPC

Table 2-12. DISPC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
dispc_data0	DISPC data to LCD2 panel—data bit 0	O	AM6	-
dispc_data1	DISPC data to LCD2 panel—data bit 1	O	AL7	-
dispc_data2	DISPC data to LCD2 panel—data bit 2	O	AJ6	-
dispc_data3	DISPC data to LCD2 panel—data bit 3	O	AM7	-
dispc_data4	DISPC data to LCD2 panel—data bit 4	O	AM8	-
dispc_data5	DISPC data to LCD2 panel—data bit 5	O	AL8	-
dispc_data6	DISPC data to LCD2 panel—data bit 6	O	AM10	-
dispc_data7	DISPC data to LCD2 panel—data bit 7	O	AL10	-
dispc_data8	DISPC data to LCD2 panel—data bit 8	O	AK5	-
dispc_data9	DISPC data to LCD2 panel—data bit 9	O	AJ5	-
dispc_data10	DISPC data to LCD2 panel—data bit 10	O	AL5	-
dispc_data11	DISPC data to LCD2 panel—data bit 11	O	AL6	-
dispc_data12	DISPC data to LCD2 panel—data bit 12	O	AJ8	-
dispc_data13	DISPC data to LCD2 panel—data bit 13	O	AM9	-
dispc_data14	DISPC data to LCD2 panel—data bit 14	O	AL9	-
dispc_data15	DISPC data to LCD2 panel—data bit 15	O	AJ9	-
dispc_data16	DISPC data to LCD2 panel—data bit 16	O	AJ7	-
dispc_data17	DISPC data to LCD2 panel—data bit 17	O	AK7	-
dispc_data18	DISPC data to LCD2 panel—data bit 18	O	AJ10	-
dispc_data19	DISPC data to LCD2 panel—data bit 19	O	AK10	-
dispc_data20	DISPC data to LCD2 panel—data bit 20	O	AJ11	-
dispc_data21	DISPC data to LCD2 panel—data bit 21	O	AK11	-
dispc_data22	DISPC data to LCD2 panel—data bit 22	O	AJ12	-
dispc_data23	DISPC data to LCD2 panel—data bit 23	O	AK12	-
dispc_hsync	DISPC horizontal synchronization from dispc to LCD2	O	AK6	-
dispc_vsync	DISPC vertical synchronization from dispc to LCD2	O	AK8	-
dispc_de	DISPC ac bias output enable or data enable to LCD2	O	AM5	-
dispc_pclk	DISPC LCD pixel clock to LCD2	O	AK9	-
dispc_fid	DISPC field ID to LCD2	O	AK20	-

2.4.4 Serial and Parallel Communication Interfaces

2.4.4.1 HDQ / 1-Wire

NOTE

For more information, see the Serial Communication Interface / HDQ/1-Wire section of the OMAP543x TRM.

Table 2-13. HDQ / 1-Wire Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
hdq_sio	HDQ 1-wire	IOD	AK28	-

2.4.4.2 I²C

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I²C Controller / HS I²C Environment / HS I²C in I²C Mode section of the OMAP543x TRM.

NOTE

For more information on SmartReflex™, see:

- The Power, Reset and Clock Management / Device Power Management Introduction / Device Power-Management Architecture Building Blocks / Voltage Management / AVS Overview section
- The Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section

of the OMAP543x TRM.

Table 2-14. I²C Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Inter-Integrated Circuit Interface (I2C1)—Platform				
i2c1_pmic_scl	I2C1 master platform clock	IOD	K29	-
i2c1_pmic_sda	I2C1 master platform data	IOD	H30	-
Inter-Integrated Circuit Interface (I2C2)—Generic				
i2c2_scl	I2C2 OMAP master or slave clock	IOD	AF30	-
i2c2_sda	I2C2 data	IOD	AF29	-
Inter-Integrated Circuit Interface (I2C3)—Generic				
i2c3_scl	I2C3 OMAP master clock	IOD	AB3	-
i2c3_sda	I2C3 data	IOD	AB2	-
Inter-Integrated Circuit Interface (I2C4)—Generic				
i2c4_scl	I2C4 OMAP master clock	IOD	AK22	-
i2c4_sda	I2C4 data	IOD	AJ20	-
Inter-Integrated Circuit Interface (I2C5)—Generic				
i2c5_scl	I2C5 OMAP master or slave clock	IOD	AL32	-
i2c5_sda	I2C5 data	IOD	AL31	-
Inter-Integrated Circuit Interface (SmartReflex™)—PMIC				
sr_pmic_scl	SmartReflex™ clock	IOD	H29	-
sr_pmic_sda	SmartReflex™ data	IOD	J29	-

2.4.4.3 McBSP

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) section of the OMAP543x TRM.

Table 2-15. McBSP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE synchronization input clock	I	N30	-
Audio Backend Multichannel Buffered Serial Port (ABE McBSP1)				
abemcbsp1_dr	ABE McBSP1 received serial data	I	T29	-
abemcbsp1_dx	ABE McBSP1 transmitted serial data	O	N29	-

Table 2-15. McBSP Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abemcbsp1_fsx	ABE McBSP1 combined frame synchronization	IO	P30	-
abemcbsp1_clkx	ABE McBSP1 combined serial clock	IO	T30	-
Audio Backend Multichannel Buffered Serial Port (ABE McBSP2)				
abemcbsp2_dr	ABE McBSP2 received serial data	I	N31	-
abemcbsp2_dx	ABE McBSP2 transmitted serial data	O	N32	-
abemcbsp2_fsx	ABE McBSP2 combined frame synchronization	IO	M31	-
abemcbsp2_clkx	ABE McBSP2 combined serial clock	IO	M32	-
Audio Backend Multichannel Buffered Serial Port (ABE McBSP3)				
abemcbsp3_dr	ABE McBSP3 received serial data	I	P31 / M29	- / -
abemcbsp3_dx	ABE McBSP3 transmitted serial data	O	P32 / M30	- / -
abemcbsp3_fsx	ABE McBSP3 combined frame synchronization	IO	R30 / L29	- / -
abemcbsp3_clkx	ABE McBSP3 combined serial clock	IO	P29 / L30	- / -

2.4.4.4 McPDM

NOTE

For more information, see the Serial Communication Interface / Multichannel PDM Controller section of the OMAP543x TRM.

Table 2-16. McPDM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE synchronization input clock	I	N30	-
Audio Backend Multichannel PDM				
abemcpdm_ul_data	ABE PDM data stream from PMIC to the OMAP5430 device	I	M29	-
abemcpdm_dl_data	ABE PDM data stream from the OMAP5430 device to PMIC	O	M30	-
abemcpdm_frame	ABE PDM frame synchronization	IO	L30	-
abemcpdm_lb_clk	ABE PDM loop back clock	O	L29	-

2.4.4.5 DMIC

NOTE

For more information, see the Serial Communication Interface / Digital Microphone Module section of the OMAP543x TRM.

Table 2-17. DMIC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE synchronization input clock	I	N30	-
Audio Backend Digital Microphone Module				
abedmic_clk1	ABE digital microphone clock output 1	O	P29	-
abedmic_din1	ABE digital microphone data input 1	I	R30	-
abedmic_clk2	ABE digital microphone clock output 2	O	P30	-
abedmic_din2	ABE digital microphone data input 2	I	P32	-
abedmic_clk3	ABE digital microphone clock output 3	O	N29	-
abedmic_din3	ABE digital microphone data input 3	I	P31	-

2.4.4.6 McASP

NOTE

For more information, see the Serial Communication Interface / Multichannel Audio Serial Port section of the OMAP543x TRM.

Table 2-18. McASP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
abe_clks	ABE synchronization input clock	I	N30	-
Audio Backend Multichannel Audio Serial Port				
abemcasp_axr	ABE McASP serial data IO	IO	N31 / N30 / P32	-
abemcasp_axr1	ABE McASP serial data 1 IO	IO	L30	-
abemcasp_axr2	ABE McASP serial data 2 IO	IO	M30	-
abemcasp_axr3	ABE McASP serial data 3 IO	IO	M29	-
abemcasp_aclkx	ABE McASP clock transmit	IO	N29	-
abemcasp_afsx	ABE McASP frame synchronization transmit	IO	M31	-
abemcasp_afsr	ABE McASP frame synchonization receive	IO	T30	-
abemcasp_ahclkx	ABE McASP high frequency clock output	IO	M32	-
abemcasp_aclkr	ABE McASP low frequency clock input	IO	T29	-
abemcasp_amutein	ABE McASP auto mute input	I	P30	-
abemcasp_amuteout	ABE McASP auto mute output	O	N32	-

2.4.4.7 HSI

NOTE

For more information, see the Serial Communication Interface / MIPI-HSI section of the OMAP543x TRM.

Table 2-19. HSI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
High-speed Synchronous Serial Interface (HSI1)				
hsi1_cawake	HSI1 cellular modem to APE wake signal	I	E15	-
hsi1_acready	HSI1 APE to cellular modem ready signal	O	E13	-
hsi1_cadata	HSI1 cellular modem to APE signal	I	E12	-
hsi1_caflag	HSI1 cellular modem to APE flag signal	I	D12	-
hsi1_acwake	HS1 APE to cellular modem wake signal	O	D13	-
hsi1_caready	HSI1 cellular modem to APE ready signal	I	E14	-
hsi1_acdata	HSI1 APE to cellular modem data signal	O	D14	-
hsi1_acflag	HSI1 APE to cellular modem ready signal	O	D15	-
High-speed Synchronous Serial Interface (HSI2)				
hsi2_cawake	HSI2 cellular modem to APE wake signal	I	B8	-
hsi2_acready	HSI2 APE to cellular modem ready signal	O	C10	-
hsi2_cadata	HSI2 cellular modem to APE signal	I	B10	-
hsi2_caflag	HSI2 cellular modem to APE flag signal	I	B7	-
hsi2_acwake	HS2 APE to cellular modem wake signal	O	C8	-
hsi2_caready	HSI2 cellular modem to APE ready signal	I	C7	-
hsi2_acdata	HSI2 APE to cellular modem data signal	O	C9	-
hsi2_acflag	HSI2 APE to cellular modem ready signal	O	B9	-

2.4.4.8 McSPI

NOTE

For more information, see the Serial Communication Interface / Multichannel Serial Port Interface (MCSPI) section of the OMAP543x TRM.

Table 2-20. McSPI Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Multichannel Serial Port Interface (McSPI1)				
mcspi1_simo	McSPI1 data (slave input, master input, Z when not shifting)	IO	AH31	-
mcspi1_somi	McSPI1 data (slave output, master input, Z when not shifting)	I	AG32	-
mcspi1_clk	McSPI1 clock (slave input, master output)	IO	AH32	-
mcspi1_cs0	McSPI1 chip select 0 (slave input, master output)	O	AG31	-
mcspi1_cs1	McSPI1 chip select 1	O	AH30	-
mcspi1_cs2	McSPI1 chip select 2	O	AJ32	-
mcspi1_cs3	McSPI1 chip select 3	O	AK32	-
Multichannel Serial Port Interface (McSPI2)				
mcspi2_simo	McSPI2 data (slave input, master input, Z when not shifting)	IO	AJ18	-
mcspi2_somi	McSPI2 data (slave output, master input, Z when not shifting)	I	AK23	-
mcspi2_clk	McSPI2 clock (slave input, master output)	IO	AK21	-
mcspi2_cs0	McSPI2 chip select 0 (slave input, master output)	O	AK20	-

Table 2-20. McSPI Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
mcspi2_cs1	McSPI2 chip select 1	O	AJ9	-
Multichannel Serial Port Interface (McSPI3)				
mcspi3_simo	McSPI3 data (slave input, master input, Z when not shifting)	IO	C6	-
mcspi3_somi	McSPI3 data (slave output, master input, Z when not shifting)	IO	C5	-
mcspi3_clk	McSPI3 clock (slave input, master output)	IO	B6	-
mcspi3_cs0	McSPI3 chip select 0 (slave input, master output)	IO	B5	-
Multichannel Serial Port Interface (McSPI4)				
mcspi4_simo	McSPI4 data (slave input, master input, Z when not shifting)	IO	AJ30	-
mcspi4_somi	McSPI4 data (slave output, master input, Z when not shifting)	IO	AK30	-
mcspi4_clk	McSPI4 clock (slave input, master output)	IO	AK29	-
mcspi4_cs0	McSPI4 chip select 0 (slave input, master output)	IO	AJ31	-

2.4.4.9 UART

NOTE

For more information, see the Serial Communication Interface / UART/IrDA/CIR section of the OMAP543x TRM.

Table 2-21. UART Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Universal Asynchronous Receiver/Transmitter (UART1)				
uart1_tx	UART1 transmit data	O	D10 / AF3	-
uart1_rx	UART1 receive data	I	D9 / AE3	-
uart1_cts	UART1 clear to send	I	E9 / AF2	-
uart1_rts	UART1 request to send	O	E10 / AE2	-
Universal Asynchronous Receiver/Transmitter (UART2)				
uart2_tx	UART2 transmit data	O	B6	-
uart2_rx	UART2 receive data	I	C6	-
uart2_cts	UART2 clear to send	I	B5	-
uart2_rts	UART2 request to send	O	C5	-
Universal Asynchronous Receiver/Transmitter (UART3)				
uart3_tx_irtx	UART3 transmit data output or infrared data output	O	AJ6 / AL28 / AL20	- / - / -
uart3_rx_irrx	UART3 receive data input or infrared data input	I	AL7 / AM28 / AM20	- / - / -
uart3_cts_rctx	UART3 clear to send or remote control data output	IO	AJ28	-
uart3_rts_irsd	UART3 request to send or infrared transceiver shutdown	O	AK28	-
Universal Asynchronous Receiver/Transmitter (UART4)				
uart4_tx	UART4 transmit data	O	AL31	-
uart4_rx	UART4 receive data	I	AL32	-
uart4_cts	UART4 clear to send	I	AJ32	-
uart4_rts	UART4 request to send	O	AK32	-
Universal Asynchronous Receiver/Transmitter (UART5)				
uart5_tx	UART5 transmit data	O	AE29	-
uart5_rx	UART5 receive data	I	AD30	-
uart5_cts	UART5 clear to send	I	AE30	-
uart5_rts	UART5 request to send	O	AD29	-
Universal Asynchronous Receiver/Transmitter (UART6)				

Table 2-21. UART Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
uart6_tx	UART6 transmit data	O	AJ27	-
uart6_rx	UART6 receive data	I	AJ26 / E2	- / -
uart6_cts	UART6 clear to send	I	AK26	-
uart6_rts	UART6 request to send	O	AK27	-

2.4.4.10 USB

NOTE

For more information, see:

- Serial Communication Interface / High-Speed Multiport USB Host Subsystem section, or
- Serial Communication Interface / High-Speed USB OTG Controller section, or
- Serial Communication Interface / Full-Speed USB Host Controller section

of the OMAP543x TRM.

Table 2-22. USB Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Universal Serial Bus (Port D0)—USB2PHY				
usbd0_hs_dp	USB2PHY (Port D0)—half-duplex positive lane	IODS	AM20	-
usbd0_hs_dm	USB2PHY (Port D0)—half-duplex negative lane	IODS	AL20	-
usbphy_ce	USB2PHY (Port D0)—charge enable	O	AL19	-
Universal Serial Bus (Port D0)—ULPI 8-bit				
usbd0_ulpiphy_clk	USB Port D0—ULPI functional clock	I	AH32	-
usbd0_ulpiphy_stp	USB Port D0—ULPI stop	O	AK27	-
usbd0_ulpiphy_dir	USB Port D0—ULPI bus direction	I	AH31	-
usbd0_ulpiphy_nxt	USB Port D0—ULPI next	I	AG32	-
usbd0_ulpiphy_data0	USB Port D0—ULPI 8-bit data bus	IO	AG31	-
usbd0_ulpiphy_data1	USB Port D0—ULPI 8-bit data bus	IO	AH30	-
usbd0_ulpiphy_data2	USB Port D0—ULPI 8-bit data bus	IO	AJ32	-
usbd0_ulpiphy_data3	USB Port D0—ULPI 8-bit data bus	IO	AK32	-
usbd0_ulpiphy_data4	USB Port D0—ULPI 8-bit data bus	IO	AJ28	-
usbd0_ulpiphy_data5	USB Port D0—ULPI 8-bit data bus	IO	AK28	-
usbd0_ulpiphy_data6	USB Port D0—ULPI 8-bit data bus	IO	AL28	-
usbd0_ulpiphy_data7	USB Port D0—ULPI 8-bit data bus	IO	AM28	-
Universal Serial Bus (Port D0)—USB3PHY				
usbd0_ss_tx	USB3PHY (Port D0)—transmitter positive lane	ODS	AM21	-
usbd0_ss_ty	USB3PHY (Port D0)—transmitter negative lane	ODS	AL21	-
usbd0_ss_rx	USB3PHY (Port D0)—receiver positive lane	IDS	AM22	-
usbd0_ss_ry	USB3PHY (Port D0)—receiver negative lane	IDS	AL22	-
Universal Serial Bus (Port D0)—USB frame sync output				
sync_sof_clk	0.5-kHz clock output, each edge locked to SOF synchronous packets of FS USB	O	AC29	
sync_usof_itp_clk	4-kHz clock output, each edge locked to ITP/uSOF synchronous packets of SS/HS USB	O	AC29	
Universal Serial Bus (Port B1)—HSIC				
usbb1_hsic_data	USB (Port B1)—interchip data	IO	C26	-
usbb1_hsic_strobe	USB (Port B1)—interchip strobe	IO	B26	-
Universal Serial Bus (Port B1)—ULPI 8-bit				

Table 2-22. USB Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
usbb1_ulpiphy_clk	USB (Port B1)—ULPI functional clock	I	C7	-
usbb1_ulpiphy_stp	USB (Port B1)—ULPI stop	O	C8	-
usbb1_ulpiphy_dir	USB (Port B1)—ULPI bus direction	I	B8	-
usbb1_ulpiphy_nxt	USB (Port B1)—ULPI next	I	C10	-
usbb1_ulpiphy_data0	USB (Port B1)—ULPI 8-bit data bus	IO	B7	-
usbb1_ulpiphy_data1	USB (Port B1)—ULPI 8-bit data bus	IO	B10	-
usbb1_ulpiphy_data2	USB (Port B1)—ULPI 8-bit data bus	IO	B9	-
usbb1_ulpiphy_data3	USB (Port B1)—ULPI 8-bit data bus	IO	C9	-
usbb1_ulpiphy_data4	USB (Port B1)—ULPI 8-bit data bus	IO	C5	-
usbb1_ulpiphy_data5	USB (Port B1)—ULPI 8-bit data bus	IO	B5	-
usbb1_ulpiphy_data6	USB (Port B1)—ULPI 8-bit data bus	IO	C6	-
usbb1_ulpiphy_data7	USB (Port B1)—ULPI 8-bit data bus	IO	B6	-
Universal Serial Bus (Port B2)—HSIC				
usbb2_hsic_data	USB (Port B2)—interchip data	IO	C25	-
usbb2_hsic_strobe	USB (Port B2)—interchip strobe	IO	B25	-
Universal Serial Bus (Port B2)—ULPI 8-bit				
usbb2_ulpitll_clk	USB (Port B2)—ULPI functional clock	O	E13	-
usbb2_ulpitll_stp	USB (Port B2)—ULPI stop	I	E15	-
usbb2_ulpitll_dir	USB (Port B2)—ULPI bus direction	O	D13	-
usbb2_ulpitll_nxt	USB (Port B2)—ULPI next	O	E14	-
usbb2_ulpitll_data0	USB (Port B2)—ULPI 8-bit data bus	IO	D15	-
usbb2_ulpitll_data1	USB (Port B2)—ULPI 8-bit data bus	IO	D14	-
usbb2_ulpitll_data2	USB (Port B2)—ULPI 8-bit data bus	IO	D12	-
usbb2_ulpitll_data3	USB (Port B2)—ULPI 8-bit data bus	IO	E12	-
usbb2_ulpitll_data4	USB (Port B2)—ULPI 8-bit data bus	IO	D10	-
usbb2_ulpitll_data5	USB (Port B2)—ULPI 8-bit data bus	IO	E9	-
usbb2_ulpitll_data6	USB (Port B2)—ULPI 8-bit data bus	IO	D9	-
usbb2_ulpitll_data7	USB (Port B2)—ULPI 8-bit data bus	IO	E10	-
Universal Serial Bus (Port B2)—Full Speed / Low Speed				
usbb2_mm_rxdm	USB (Port B2)—Full- / Low-speed multimode interface	IO	AJ26	-
usbb2_mm_rxdp	USB (Port B2)—Full- / Low-speed multimode interface	IO	AJ27	-
usbb2_mm_rxrcv	USB (Port B2)—Full- / Low-speed multimode interface	IO	AK26	-
usbb2_mm_txse0	USB (Port B2)—Full- / Low-speed multimode interface	IO	AK27	-
usbb2_mm_txdat	USB (Port B2)—Full- / Low-speed multimode interface	IO	AK28	-
usbb2_mm_txen	USB (Port B2)—Full- / Low-speed multimode interface	IO	AJ28	-
Universal Serial Bus (Port B3)—HSIC				
usbb3_hsic_data	USB (Port B3)—interchip data	IO	D30	-
usbb3_hsic_strobe	USB (Port B3)—interchip strobe	IO	D29	-

2.4.4.11 SATA

NOTE

For more information, see the SATA section of the OMAP543x TRM.

Table 2-23. SATA Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sata_tx	SATA differential positive or negative transmitter lane x	ODS	E6	-
sata_ty	SATA differential positive or negative transmitter lane y	ODS	D6	-
sata_rx	SATA differential positive or negative receiver lane x	IDS	E7	-
sata_ry	SATA differential positive or negative receiver lane y	IDS	D7	-
sata_actled	SATA channel activity indicator	O	AJ28	-

2.4.4.12 MMC2–eMMC

NOTE

For more information, see the MMC / SD / SDIO section of the OMAP543x TRM.

Table 2-24. MMC2–eMMC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
emmc_clk	eMMC clock	O	AL2	-
emmc_cmd	eMMC command	IO	AK4	-
emmc_data0	eMMC data bit 0	IO	AK3	-
emmc_data1	eMMC data bit 1	IO	AJ4	-
emmc_data2	eMMC data bit 2	IO	AK2	-
emmc_data3	eMMC data bit 3	IO	AJ3	-
emmc_data4	eMMC data bit 4	IO	AH2	-
emmc_data5	eMMC data bit 5	IO	AJ2	-
emmc_data6	eMMC data bit 6	IO	AH3	-
emmc_data7	eMMC data bit 7	IO	AH4	-

2.4.4.13 MMC3 WLSDIO3

Table 2-25. MMC3 WLSDIO Signal Descriptions(1)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Wireless LAN SDIO (OMAP to Wireless LAN)				
wlsdio_clk	WLSDIO clock	O	AK29	-
wlsdio_cmd	WLSDIO command	IO	AJ29	-
wlsdio_data0	WLSDIO data bit 0	IO	AJ30	-
wlsdio_data1	WLSDIO data bit 1	IO	AK30	-
wlsdio_data2	WLSDIO data bit 2	IO	AJ31	-
wlsdio_data3	WLSDIO data bit 3	IO	AK31	-

(1) This interface supports WLAN SDIO with inband interrupt.

2.4.4.14 MMC4 SDIO4 and MMC5 SDIO5

Table 2-26. MMC4 SDIO4 and MMC5 SDIO5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Generic SDIO				
sdio4_clk	SDIO4 clock	O	AL28	-
sdio4_cmd	SDIO4 command	IO	AM28	-
sdio4_data0	SDIO4 data bit 0	IO	AE30	-
sdio4_data1	SDIO4 data bit 1	IO	AD30	-
sdio4_data2	SDIO4 data bit 2	IO	AE29	-
sdio4_data3	SDIO4 data bit 3	IO	AD29	-
sdio5_clk	SDIO5 clock	O	AJ32	-
sdio5_cmd	SDIO5 command	IO	AK32	-
sdio5_data0	SDIO5 data bit 0	IO	AK27	-
sdio5_data1	SDIO5 data bit 1	IO	AK26	-
sdio5_data2	SDIO5 data bit 2	IO	AJ26	-
sdio5_data3	SDIO5 data bit 3	IO	AJ27	-

Table 2-26. MMC4 SDIO4 and MMC5 SDIO5 Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sdio5_data4	SDIO5 data bit 4	IO	AM28	-
sdio5_data5	SDIO5 data bit 5	IO	AL28	-
sdio5_data6	SDIO5 data bit 6	IO	AK28	-
sdio5_data7	SDIO5 data bit 7	IO	AJ28	-

2.4.5 Removable Cards

2.4.5.1 MMC1—SD Card

Table 2-27. MMC1 SD Card Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sdcard_clk	SD clock	O	E3	-
sdcard_cmd	SD command	IO	E2	-
sdcard_data0	SD data bit 0	IO	G3	-
sdcard_data1	SD data bit 1	IO	G2	-
sdcard_data2	SD data bit 2	IO	F2	-
sdcard_data3	SD data bit 3	IO	F3	-
sdcard_cd	SD card detect	I	AF2	-
sdcard_wp	SD write protect	I	AE3 / AE2	-

2.4.6 Debug and Trace Interfaces

NOTE

For more information, see the On-Chip Debug Support / Debug Ports section of the OMAP543x TRM.

2.4.6.1 JTAG®

Table 2-28. JTAG Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
jtag_ntrst	JTAG test reset	I	G2 / C32	- / -
jtag_tck	JTAG test clock	I	F3 / C31	- / -
jtag_tmsc	JTAG test mode select (I for JTAG)	IO	F2 / B32	- / -
jtag_rtck	JTAG return test clock	O	E3 / A33	- / -
jtag_tdi	JTAG test data in	I	G3 / A32	- / -
jtag_tdo	JTAG test data out	O	E2 / B33	- / -
jtag_sel	JTAG override HW control for JTAG on SD card interface	I	AJ7	-

2.4.6.2 cJTAG

Table 2-29. cJTAG Signal Descriptions

SIGNAL NAME [1]	PIN NAME [6]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
cJTAG Muxed with JTAG					
cjtag_tck	jtag_tck	cJTAG test clock	I	F3 / C31	- / -
cjtag_tmsc	jtag_tmsc	cJTAG test mode control and data scan	IO	F2 / B32	- / -

2.4.6.3 JTAG Expansion Port

Table 2-30. JTAG Expansion Port Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Inverted JTAG interface to chain a modem (or other IC) with the OMAP JTAG				
jtagtapext_ntrst	Test reset for external modem or other IC	O	AM7 / AK20	- / -
jtagtapext_tck	Test clock for external modem or other IC	O	AM8 / AK21	- / -
jtagtapext_tmsc	Test Mode Select (O for Modem JTAG) for external modem or other IC	O	AL8 / AJ18	- / -
jtagtapext_rtck	ARM clock emulation for external modem or other IC	O	AM6 / AJ20	- / -
jtagtapext_tdi	Test data in for external modem or other IC	I	AL10 / AK22	- / -
jtagtapext_tdo	Test data out for external modem or other IC	O	AM10 / AK23	- / -

2.4.6.4 Debug Resource Manager (DRM)

Table 2-31 provides the DRM signal descriptions plus the debug modes available on the DRM signals.

Table 2-31. DRM Signal Descriptions and Debug Modes

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]	DEBUG MODE		
					TRIGGER	TPIU PTM 16-BIT	TPIU STM 4-BIT
drm_emu19	Debug resource manager bit 19	O	AJ9 / J32	- / -		atpiu_data15	stm_data[3:0] or stm_clk
drm_emu18	Debug resource manager bit 18	O	AL9 / K32	- / -		atpiu_data14	
drm_emu17	Debug resource manager bit 17	O	AM9 / L32	- / -		atpiu_data13	
drm_emu16	Debug resource manager bit 16	O	AJ8 / K31	- / -		atpiu_data12	
drm_emu15	Debug resource manager bit 15	O	AL6 / J31	- / -		atpiu_data11	
drm_emu14	Debug resource manager bit 14	O	AL5	-		atpiu_data10	
drm_emu13	Debug resource manager bit 13	O	AJ5	-		atpiu_data9	
drm_emu12	Debug resource manager bit 12	O	AK5	-		atpiu_data8	
drm_emu11	Debug resource manager bit 11	O	AL10	-		atpiu_data7	
drm_emu10	Debug resource manager bit 10	O	AM10	-		atpiu_data6	
drm_emu9	Debug resource manager bit 9	O	AL8	-		atpiu_data5	
drm_emu8	Debug resource manager bit 8	O	AM8	-		atpiu_data4	
drm_emu7	Debug resource manager bit 7	O	AM7	-		atpiu_data3	
drm_emu6	Debug resource manager bit 6	O	AJ6 / J32	-		atpiu_data2	
drm_emu5	Debug resource manager bit 5	O	AL7 / K32	- / -		atpiu_data1	
drm_emu4	Debug resource manager bit 4	O	AM6 / E2 / L32	- / -		atpiu_data0	
drm_emu3	Debug resource manager bit 3	O	AK6 / K31	- / -		atpiu_ctl	
drm_emu2	Debug resource manager bit 2	O	AK8 / J31	- / -		atpiu_clk	
drm_emu1	Debug resource manager bit 1	IO	B31	- / -	trigger_channel1		
drm_emu0	Debug resource manager bit 0	IO	B30	- / -	trigger_channel0		

The DRM interface supports:

- Processor trace module (PTM) specific to MPU trace.
- System trace module (STM) for HW and SW system events.

STM via the DRM interface is always supported while MPU trace (PTM) is not always possible. This limitation is induced by the DRM: while any drm_emu signals can be configured as the STM clock or one of the data lanes, the drm_emu signals have a fixed PTM assignment.

The concurrent debug use cases are:

- UC1: Either uses trigger channel 2-pin plus the TPIU PTM 16-bit data.
- UC2: Either the TPIU PTM 16-bit data plus the TPIU STM 1-bit data.
- UC3: Either the trigger channel 2-pin plus TPIU PTM 8-bit data plus TPIU STM 4-bit data.
- UC4: Or uses the trigger channel 2-pin plus TPIU PTM 11-bit data plus TPIU STM 4-bit data.

A STM 4-bit data always-on interface is available via the DRM interface on the sys_boot pins in order to use debug function in the off mode (especially for PRCM or audio back-end debug).

Table 2-32. Always-On STM 4-Bit Signal Mapping

DEBUG MODE STM 4-BIT	SIGNAL NAME [1]	PIN NAME [6]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
stm_data[3:0] or stm_clk	drm_emu15	sys_boot0	IO	J31	-
stm_data[3:0] or stm_clk	drm_emu16	sys_boot1	IO	K31	-
stm_data[3:0] or stm_clk	drm_emu17	sys_boot2	IO	L32	-
stm_data[3:0] or stm_clk	drm_emu18	sys_boot3	IO	K32	-
stm_data[3:0] or stm_clk	drm_emu19	sys_boot4	IO	J32	-

2.4.6.5 MIPI NIDnT (Narrow Interface for Debug and Test)

Typically, the device wide debug port is not available on a packaged, end product phone due to connectivity and footprint constraints. The OMAP5430 provides a narrow debug interface on SD Card connector compliant to the MIPI NIDnT specification. The MIPI NIDnT functionality is supported with full software control. Table 2-33 provides the NIDnT signal descriptions.

Table 2-33. NIDnT Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
n_clk	NIDnT clock	O	E3	-
n_d0	NIDnT data 0	O	G3	-
n_d1	NIDnT data 1	O	G2	-
n_d2	NIDnT data 2	O	E2 / F2	- / -
n_d3	NIDnT data 3	O	F3	-

The NIDnT standard supports several overlay modes by software. For more information, see the On-Chip Debug Support / Debug Interfaces / NIDnT section of the OMAP543x TRM.

2.4.6.6 Hardware Debug

Table 2-34. Hardware Debug Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
Observability Hardware Debug Bus: Wakeup Domain				
hw_wkdbg0	Hardware debug pin 0	O	J31	-
hw_wkdbg1	Hardware debug pin 1	O	K31	-
hw_wkdbg2	Hardware debug pin 2	O	L32	-
hw_wkdbg3	Hardware debug pin 3	O	K32	-
hw_wkdbg4	Hardware debug pin 4	O	J32	-
hw_wkdbg5	Hardware debug pin 5	O	G32	-
hw_wkdbg6	Hardware debug pin 6	O	B30	-
hw_wkdbg7	Hardware debug pin 7	O	B31	-
hw_wkdbg8	Hardware debug pin 8	O	H31	-
hw_wkdbg9	Hardware debug pin 9	O	F30	-
hw_wkdbg10	Hardware debug pin 10	O	G31	-
hw_wkdbg11	Hardware debug pin 11	O	G29	-
hw_wkdbg12	Hardware debug pin 12	O	G30	-
hw_wkdbg13	Hardware debug pin 13	O	E30	-
hw_wkdbg14	Hardware debug pin 14	O	C30	-
Observability Hardware Debug Bus: Core Domain				
hw_wkdbg15	Hardware debug pin 15	O	L31	-
hw_dbg16	Hardware debug pin 16	O	E26 / C5	- / -
hw_dbg17	Hardware debug pin 17	O	D26 / B5	- / -
hw_dbg18	Hardware debug pin 18	O	E25 / C6	- / -
hw_dbg19	Hardware debug pin 19	O	D25 / B6	- / -
hw_dbg20	Hardware debug pin 20	O	E24 / AJ18	- / -
hw_dbg21	Hardware debug pin 21	O	D24 / AK23	- / -
hw_dbg22	Hardware debug pin 22	O	E23 / AJ11	- / -
hw_dbg23	Hardware debug pin 23	O	D23 / AK11	- / -
hw_dbg24	Hardware debug pin 24	O	E21 / AJ12	- / -
hw_dbg25	Hardware debug pin 25	O	D21 / AK12	- / -
hw_dbg26	Hardware debug pin 26	O	E20 / AF3	- / -
hw_dbg27	Hardware debug pin 27	O	D20 / AE2	- / -
hw_dbg28	Hardware debug pin 28	O	E19 / AD30	- / -
hw_dbg29	Hardware debug pin 29	O	D19 / AE29	- / -
hw_dbg30	Hardware debug pin 30	O	E18 / AE30	- / -
hw_dbg31	Hardware debug pin 31	O	D18 / AD29	- / -

2.4.7 General-Purpose IOs (GPIOs)

NOTE

For more information, see the General-Purpose Interface section of the OMAP543x TRM.

NOTE

Note that the following naming convention is used for the GPIO: gpio(N)_(wk)(In / Out)(Number)

With:

- N: bank name
- wk (for wakeable): the always-on GPIOs that have the capability to wake-up domains. If not specified, this means that the GPIO is not wakeable.
- In: Input only general-purpose signal
- Out: Output only general-purpose signal

Table 2-35. GPIO Signal Descriptions(2)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio1_wk10	General-purpose IO, always on, wakeable	IO	G31	-
gpio1_wk11	General-purpose IO, always on, wakeable	IO	G32	-
gpio1_wk12	General-purpose IO, always on, wakeable	IO	F30	-
gpio1_wk13	General-purpose IO, always on, wakeable	IO	H32	-
gpio1_wk14	General-purpose IO, always on, wakeable	IO	C30	-
gpio1_wk15	General-purpose IO, always on, wakeable	IO	E30	-
gpio1_wk16	General-purpose IO, always on, wakeable	IO	K30	
gpio1_wk17	General-purpose IO, always on, wakeable	IO	J30	
gpio1_wk6	General-purpose IO, always on, wakeable	IO	B30	-
gpio1_wk7	General-purpose IO, always on, wakeable	IO	B31	-
gpio1_wk8	General-purpose IO, always on, wakeable	IO	G30	-
gpio1_wk9	General-purpose IO, always on, wakeable	IO	G29	-
gpio1_wkout0	General-purpose output, always on, wakeable	O	J31	-
gpio1_wkout1	General-purpose output, always on, wakeable	O	K31	-
gpio1_wkout2	General-purpose output, always on, wakeable	O	L32	-
gpio1_wkout3	General-purpose output, always on, wakeable	O	K32	-
gpio1_wkout4	General-purpose output, always on, wakeable	O	J32	-
gpio1_wkout5	General-purpose output, always on, wakeable	O	H31	-
gpio2_32	General-purpose IO	IO	E29	-
gpio2_33	General-purpose IO	IO	E22	-
gpio2_34	General-purpose IO	IO	D22	-
gpio2_35	General-purpose IO	IO	B22	-
gpio2_36	General-purpose IO	IO	C22	-
gpio2_37	General-purpose IO	IO	B21	-
gpio2_38	General-purpose IO	IO	C21	-
gpio2_39	General-purpose IO	IO	B20	-
gpio2_40	General-purpose IO	IO	C20	-
gpio2_41	General-purpose IO	IO	B19	-
gpio2_42	General-purpose IO	IO	C19	-
gpio2_43	General-purpose IO	IO	B18	-
gpio2_44	General-purpose IO	IO	C18	-

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio2_45	General-purpose IO	IO	C29	-
gpio2_46	General-purpose IO	IO	AL2	-
gpio2_47	General-purpose IO	IO	AK4	-
gpio2_48	General-purpose IO	IO	AK3	-
gpio2_49	General-purpose IO	IO	AJ4	-
gpio2_50	General-purpose IO	IO	AK2	-
gpio2_51	General-purpose IO	IO	AJ3	-
gpio2_52	General-purpose IO	IO	AH2	-
gpio2_53	General-purpose IO	IO	AJ2	-
gpio2_54	General-purpose IO	IO	AH3	-
gpio2_55	General-purpose IO	IO	AH4	-
gpio2_56	General-purpose IO	IO	E26	-
gpio2_57	General-purpose IO	IO	D26	-
gpio2_58	General-purpose IO	IO	E25	-
gpio2_59	General-purpose IO	IO	D25	-
gpio2_60	General-purpose IO	IO	E24	-
gpio2_61	General-purpose IO	IO	D24	-
gpio2_62	General-purpose IO	IO	E23	-
gpio2_63	General-purpose IO	IO	D23	-
gpio3_64	General-purpose IO	IO	E13	-
gpio3_65	General-purpose IO	IO	E14	-
gpio3_66	General-purpose IO	IO	D13	-
gpio3_67	General-purpose IO	IO	E15	-
gpio3_68	General-purpose IO	IO	D15	-
gpio3_69	General-purpose IO	IO	D14	-
gpio3_70	General-purpose IO	IO	D12	-
gpio3_71	General-purpose IO	IO	E12	-
gpio3_72	General-purpose IO	IO	D10	-
gpio3_73	General-purpose IO	IO	E9	-
gpio3_74	General-purpose IO	IO	D9	-
gpio3_75	General-purpose IO	IO	E10	-
gpio3_76	General-purpose IO	IO	C7	-
gpio3_77	General-purpose IO	IO	C10	-
gpio3_78	General-purpose IO	IO	B8	-
gpio3_79	General-purpose IO	IO	C8	-
gpio3_80	General-purpose IO	IO	B7	-
gpio3_81	General-purpose IO	IO	B10	-
gpio3_82	General-purpose IO	IO	B9	-
gpio3_83	General-purpose IO	IO	C9	-
gpio3_84	General-purpose IO	IO	C5	-
gpio3_85	General-purpose IO	IO	B5	-
gpio3_86	General-purpose IO	IO	C6	-
gpio3_87	General-purpose IO	IO	B6	-
gpio3_92	General-purpose IO	IO	B26	-
gpio3_93	General-purpose IO	IO	C26	-
gpio3_94	General-purpose IO	IO	B25	-
gpio3_95	General-purpose IO	IO	C25	-

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio4_100	General-purpose IO	IO	P29	-
gpio4_101	General-purpose IO	IO	P30	-
gpio4_102	General-purpose IO	IO	N29	-
gpio4_103	General-purpose IO	IO	T30	-
gpio4_104	General-purpose IO	IO	T29	-
gpio4_105	General-purpose IO	IO	N31	-
gpio4_106	General-purpose IO	IO	N32	-
gpio4_107	General-purpose IO	IO	M31	-
gpio4_108	General-purpose IO	IO	M32	-
gpio4_109	General-purpose IO	IO	M29	-
gpio4_110	General-purpose IO	IO	M30	-
gpio4_111	General-purpose IO	IO	L30	-
gpio4_112	General-purpose IO	IO	L29	-
gpio4_113	General-purpose IO	IO	E21	-
gpio4_114	General-purpose IO	IO	D21	-
gpio4_115	General-purpose IO	IO	E20	-
gpio4_116	General-purpose IO	IO	D20	-
gpio4_117	General-purpose IO	IO	E19	-
gpio4_118	General-purpose IO	IO	D19	-
gpio4_119	General-purpose IO	IO	E18	-
gpio4_120	General-purpose IO	IO	D18	-
gpio4_96	General-purpose IO	IO	N30	-
gpio4_97	General-purpose IO	IO	R30	-
gpio4_98	General-purpose IO	IO	P32	-
gpio4_99	General-purpose IO	IO	P31	-
gpio5_128	General-purpose IO	IO	AK29	-
gpio5_129	General-purpose IO	IO	AJ29	-
gpio5_130	General-purpose IO	IO	AJ30	-
gpio5_131	General-purpose IO	IO	AK30	-
gpio5_132	General-purpose IO	IO	AJ31	-
gpio5_133	General-purpose IO	IO	AK31	-
gpio5_134	General-purpose IO	IO	AD30	-
gpio5_135	General-purpose IO	IO	AE29	-
gpio5_136	General-purpose IO	IO	AE30	-
gpio5_137	General-purpose IO	IO	AD29	-
gpio5_138	General-purpose IO	IO	AF30	-
gpio5_139	General-purpose IO	IO	AF29	-
gpio5_140	General-purpose IO	IO	AH32	-
gpio5_141	General-purpose IO	IO	AG32	-
gpio5_142	General-purpose IO	IO	AH31	-
gpio5_143	General-purpose IO	IO	AG31	-
gpio5_144	General-purpose IO	IO	AH30	-
gpio5_145[1]	General-purpose IO	IO	AJ32	-
gpio5_146[1]	General-purpose IO	IO	AK32	-
gpio5_147	General-purpose IO	IO	AL32	-
gpio5_148	General-purpose IO	IO	AL31	-
gpio5_149	General-purpose IO	IO	AJ27	-

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio5_150	General-purpose IO	IO	AJ26	-
gpio5_151	General-purpose IO	IO	AK26	-
gpio5_152	General-purpose IO	IO	AK27	-
gpio5_153	General-purpose IO	IO	AJ28	-
gpio5_154	General-purpose IO	IO	AK28	-
gpio5_155	General-purpose IO	IO	AL28	-
gpio5_156	General-purpose IO	IO	AM28	-
gpio5_158	General-purpose IO	IO	D29	-
gpio5_159	General-purpose IO	IO	D30	-
gpio6_160	General-purpose IO	IO	AK7	-
gpio6_161	General-purpose IO	IO	AJ7	-
gpio6_162	General-purpose IO	IO	AK8	-
gpio6_163	General-purpose IO	IO	AK6	-
gpio6_164	General-purpose IO	IO	AK9	-
gpio6_165	General-purpose IO	IO	AM5	-
gpio6_166	General-purpose IO	IO	AM6	-
gpio6_167	General-purpose IO	IO	AL7	-
gpio6_168	General-purpose IO	IO	AJ6	-
gpio6_169	General-purpose IO	IO	AM7	-
gpio6_170	General-purpose IO	IO	AM8	-
gpio6_171	General-purpose IO	IO	AL8	-
gpio6_172	General-purpose IO	IO	AM10	-
gpio6_173	General-purpose IO	IO	AL10	-
gpio6_174	General-purpose IO	IO	AK5	-
gpio6_175	General-purpose IO	IO	AJ5	-
gpio6_176	General-purpose IO	IO	AL5	-
gpio6_177	General-purpose IO	IO	AL6	-
gpio6_178	General-purpose IO	IO	AJ8	-
gpio6_179	General-purpose IO	IO	AM9	-
gpio6_180	General-purpose IO	IO	AL9	-
gpio6_181	General-purpose IO	IO	AJ9	-
gpio6_182[1]	General-purpose IO	IO	AJ10 / AJ10[1]	-
gpio6_183[1]	General-purpose IO	IO	AK10 / AK10[1]	-
gpio6_184[1]	General-purpose IO	IO	AJ11 / AJ11[1]	-
gpio6_185[1]	General-purpose IO	IO	AK11 / AK11[1]	-
gpio6_186[1]	General-purpose IO	IO	AJ12 / AJ12[1]	-
gpio6_187[1]	General-purpose IO	IO	AK12 / AK12[1]	-
gpio6_188	General-purpose IO	IO	V30	-
gpio6_189	General-purpose IO	IO	W30	-
gpio6_190	General-purpose IO	IO	AC29	-
gpio6_191	General-purpose IO	IO	AB29	-
gpio7_192	General-purpose IO	IO	AK25	-
gpio7_193	General-purpose IO	IO	AJ25	-
gpio7_194	General-purpose IO	IO	AK24	-
gpio7_195	General-purpose IO	IO	AJ24	-
gpio7_196	General-purpose IO	IO	AK20	-
gpio7_197	General-purpose IO	IO	AK21	-

Table 2-35. GPIO Signal Descriptions[2] (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
gpio7_198	General-purpose IO	IO	AJ18	-
gpio7_199	General-purpose IO	IO	AK23	-
gpio7_200	General-purpose IO	IO	AK22	-
gpio7_201	General-purpose IO	IO	AJ20	-
gpio8_224	General-purpose IO	IO	AD3	-
gpio8_225	General-purpose IO	IO	AD4	-
gpio8_226	General-purpose IO	IO	AD2	-
gpio8_227	General-purpose IO	IO	AF3	-
gpio8_228	General-purpose IO	IO	AF2	-
gpio8_229	General-purpose IO	IO	AE3	-
gpio8_230	General-purpose IO	IO	AE2	-
gpio8_231	General-purpose IO	IO	AB3	-
gpio8_232	General-purpose IO	IO	AB2	-
gpio8_233[1]	General-purpose IO	IO	AC2 / AC2[1]	-
gpio8_234[1]	General-purpose IO	IO	AC3 / AC3[1]	-
gpio8_in236	General-purpose input	I	R2	-
gpio8_in237	General-purpose input	I	R3	-
gpio8_in238	General-purpose input	I	P3	-
gpio8_in239	General-purpose input	I	P2	-
gpio8_in240	General-purpose input	I	N3	-
gpio8_in241	General-purpose input	I	N2	-
gpio8_in242	General-purpose input	I	M2	-
gpio8_in243	General-purpose input	I	M3	-
gpio8_in244	General-purpose input	I	L2	-
gpio8_in245	General-purpose input	I	L3	-
gpio8_in246	General-purpose input	I	V3	-
gpio8_in247	General-purpose input	I	V2	-
gpio8_in248	General-purpose input	I	W2	-
gpio8_in249	General-purpose input	I	W3	-
gpio8_in250	General-purpose input	I	Y2	-
gpio8_in251	General-purpose input	I	Y3	-
gpio8_in252	General-purpose input	I	K3	-
gpio8_in253	General-purpose input	I	K2	-
gpio8_in254	General-purpose input	I	J3	-
gpio8_in255	General-purpose input	I	J2	-

(1) gpio5_145, gpio5_146, gpio6_182, gpio6_183, gpio6_184, gpio6_185, gpio6_186, gpio6_187, gpio8_233, gpio8_234 GPIOs (balls AJ32 / AK32 / AJ10 / AK10 / AJ11 / AK11 / AJ12 / AK12 / AC2 / AC3) can output the same GPIO in mode 0 or in mode 6.

(2) The following naming convention is used for the GPIO: gpio(N)_(wk)(In / Out)(Number) with:

- N: bank name
- wk (for wakeable): the always-on GPIOs that have the capability to wake-up domains. If not specified, this means that the GPIO is not wakeable.
- In: Input only general-purpose signal
- Out: Output only general-purpose signal

2.4.8 System and Miscellaneous

2.4.8.1 DM Timer

NOTE

For more information, see the Timers section of the OMAP543x TRM.

Table 2-36. DM Timer Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
timer5_pwm_evt	DM timer event input or PWM output	IO	AF2	-
timer6_pwm_evt	DM timer event input or PWM output	IO	AE3	-
timer8_pwm_evt	DM timer event input or PWM output	IO	AE2 / AC2	- / -
timer9_pwm_evt	DM timer event input or PWM output	IO	AC29	-
timer10_pwm_evt	DM timer event input or PWM output	IO	V30	-
timer11_pwm_evt	DM timer event input or PWM output	IO	AF3	-

2.4.8.2 KeyPad

NOTE

For more information, see Keyboard Controller / Keyboard Controller Environment section of the OMAP543x TRM.

Table 2-37. KeyPad Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
kbd_row0	Keypad row 0	I	B21 / AK11	- / -
kbd_row1	Keypad row 1	I	C21 / AJ12	- / -
kbd_row2	Keypad row 2	I	B20 / AK12	- / -
kbd_row3	Keypad row 3	I	C20 / AJ5	- / -
kbd_row4	Keypad row 4	I	B19 / AM5	- / -
kbd_row5	Keypad row 5	I	C19 / AJ7	- / -
kbd_row6	Keypad row 6	I	B18 / AJ8	- / -
kbd_row7	Keypad row 7	I	C18 / AL6	- / -
kbd_row8	Keypad row 8	I	C22 / AL5	- / -
kbd_col0	Keypad column 0	O	E26 / AJ10	- / -
kbd_col1	Keypad column 1	O	D26 / AK10	- / -
kbd_col2	Keypad column 2	O	E25 / AJ11	- / -
kbd_col3	Keypad column 3	O	D25 / AK5	- / -
kbd_col4	Keypad column 4	O	E24 / AK9	- / -
kbd_col5	Keypad column 5	O	D24 / AK7	- / -
kbd_col6	Keypad column 6	O	E23 / AJ9	- / -
kbd_col7	Keypad column 7	O	D23 / AL9	- / -
kbd_col8	Keypad column 8	O	D22 / AM9	- / -

2.4.8.3 POP

NOTE

For more information, see Package-On-Package Concept section of the OMAP543x TRM.

Table 2-38. POP Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
pop_lpddr2ch1_zq	Feedthrough to top lpddr2 channel 1 ZQ pin	FEED	AN14	AG12
pop_lpddr2ch2_zq	Feedthrough to top lpddr2 channel 2 ZQ pin	FEED	AH33	AB27
pop_vacc_lpddr2(1)	Feedthrough to top lpddr2 channel 1 and channel 2 vacc power supply	FEED	B2 / A31	B2 / B26
pop_vdd1_lpddr2_shared	Feedthrough to shared top lpddr2 channel 1 and channel 2 vdd1 power supply	FEED	A21 / A30 / AJ33 / AL1 / AN12 / AN29 / C1 / P33 / Y1 / AA1	A18 / A25 / AC27 / AE1 / AG11 / AG23 / C1 / L26 / V1 / V2
pop_vdd2_lpddr2_shared	Feedthrough to shared top lpddr2 channel 1 and channel 2 vdd2 power supply	FEED	A3 / AF33 / AN13 / AN21 / AN28 / AN3 / A22 / C33 / N33 / Y33 / AB1 / AC1	A3 / AA25 / AE11 / AE17 / AF23 / AG3 / B18 / C27 / K27 / U25 / W2 / W3

(1) pop_vacc_lpddr2 must be left unconnected.

2.4.8.4 System And Miscellaneous

NOTE

For more information, see:

- Power, Reset and Clock Management / PRCM Subsystem Environment / External Clock Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Reset Signals section, or
- Power, Reset and Clock Management / PRCM Subsystem Environment / External Power Control Signals section

of the OMAP543x TRM.

Table 2-39. System And Miscellaneous Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
fref_xtal_in	Crystal oscillator input	AI	E32	-
fref_xtal_out	Crystal oscillator output	AO	D32	-
fref_xtal_clk(1)	Crystal oscillator output—buffered directly from the input clock (dedicated for audio)	AO	D31	-
fref_slicer_in	Slicer positive input clock	AI	B28	-
fref_clk_ioreq	FREF input clock request for main clock	IO	H32	-
fref_clk0_out	FREF clock 0 output: activated by default	O	F30	-
fref_clk1_out	FREF clock 1 output	O	G32	-
fref_clk2_out	FREF clock 2 output	O	G31	-
fref_clk3_out	FREF clock 3 output	O	G29	-
fref_clk1_req	FREF clock request 1	I	G30	-
fref_clk2_req	FREF clock request 2	I	G29	-
sys_32k	32-kHz clock input	I	F32	-
sys_nrespwron	OMAP power-on-reset input	I	F31	-
sys_nreswarm	System warm reset output or input	IOD	F29	-
sys_pwr_req	Power request to exit off mode. Active high by default but configurable	O	L31	-

Table 2-39. System And Miscellaneous Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
sys_nirq1	External interrupt 1 (aimed at PMIC power device connection)	I	K30	-
sys_nirq2	External interrupt 2 (aimed at PMIC power device connection)	I	J30	-
sys_drm_msecure	Secure transaction mode request (companion 0)	O	AC3	-
sys_aux_msecure	Secure transaction mode request (companion 1)	O	H31	-
sys_secure_indicator	Secure transaction mode external indication	O	AC2	-
sys_boot0	Boot configuration: latched at power-on reset	I	J31	-
sys_boot1	Boot configuration: latched at power-on reset	I	K31	-
sys_boot2	Boot configuration: latched at power-on reset	I	L32	-
sys_boot3	Boot configuration: latched at power-on reset	I	K32	-
sys_boot4	Boot configuration: latched at power-on reset	I	J32	-
sys_boot5	Boot configuration: latched at power-on reset	I	H31	-
sys_ndmareq0	External DMA request pipe 1	I	G29 / AK27	-
sys_ndmareq1	External DMA request pipe 2	I	G30 / AK26	-
sys_nodeid0	cJTAG node identifier bit 0 (up to 4 processors)	I	AD3	-
sys_nodeid1	cJTAG node identifier bit 1 (up to 4 processors)	I	AD4	-

(1) fref_xtal_clk is dedicated to audio purpose. A clean network is recommended.

2.4.8.5 Power Supplies

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs section of the OMAP543x TRM.

Table 2-40. Power Supply Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vdds_1p8	Second IO power supply signal to ensure the VDDS ramping.	PWR	G26 / G15 / G13 / G8 / H27 / L7 / M7 / W27 / AA27 / AA7 / AC7 / AE27 / AG22 / AG21 / AG14 / AG12 / AG8	-
vdds_emmc	eMMC dual voltage IO power supply	PWR	AF7	-
vdds_c2c	Miscalenious IO power supply	PWR	G21 / G22	-
vdds_hsic	HS interchip data power supply	PWR	G23	-
vdda_dsiporta	DSI PHY (Port A) display primary port 1 (main cut) power supply	PWR	AA32	-
vssa_dsiporta	DSI PHY (Port A) ground	GND	W33	-
vdda_dsiportc	DSI PHY (Port C) display primary port 2 (main cut) power supply	PWR	AA31	-
vssa_dsiportc	DSI PHY (Port C) ground	GND	AB33	-
vdds_hdmi	HDMI IOs (digital part) power supply	PWR	AG24	-
vdda_hdmi	HDMI PHY (TMDS) power supply	PWR	AM27	-
vssa_hdmi	HDMI PHY ground	GND	AN27	-
vdda_csiporta	CSI (Port A) PHY camera (main cut) power supply	PWR	T2	-
vssa_csiporta	CSI (Port A) PHY camera (main cut) ground	GND	N4	-
vdda_csiportb	CSI (Port B) PHY camera (main cut) power supply	PWR	T3	-
vssa_csiportb	CSI (Port B) PHY camera (main cut) ground	GND	V4	-

Table 2-40. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vdda_csiportc	CSI (Port C) PHY camera (main cut) power supply	PWR	H3	-
vssa_csiportc	CSI (Port C) PHY camera (main cut) ground	GND	H2	-
vdds_bank2	Serial bank 2 IO power supply	PWR	G12	-
vdds_bank4	Serial bank 4 IO power supply	PWR	G10	-
vdds_bank5	Serial bank 5 IO power supply	PWR	Y27	-
vdds_bank8	Serial bank 8 IO power supply	PWR	AG20	-
vdds_bank9	Serial bank 9 IO power supply	PWR	AG9 / AG11	-
vdds_bank10	Serial bank 10 IO power supply	PWR	W5	-
vdds_bank11	Serial bank 11 IO power supply	PWR	P27	-
vdds_bank12	Serial bank 12 IO power supply	PWR	R27	-
vdds_bank14	Serial bank 14 IO power supply	PWR	R29	-
vdds_bank15	Serial bank 15 IO power supply	PWR	AG25	-
vdds_bank16	Serial bank 16 IO power supply	PWR	AD27	-
vdds_bank18	Serial bank 18 IO power supply	PWR	AF27	-
vdds_bank19	Serial bank 19 IO power supply	PWR	AG27	-
vdds_bank21	Serial bank 21 IO power supply	PWR	AG26	-
vdds_bank23	Serial bank 23 IO power supply	PWR	G27	-
vdds_bank24	Serial bank 24 IO power supply	PWR	J27	-
vdds_bank25	Serial bank 25 IO power supply	PWR	K27	-
vdds_bank26	Serial bank 26 IO power supply	PWR	N27	-
vdda_sata	SATA PHY power supply	PWR	E8	-
vssa_sata	SATA PHY ground	GND	D8	-
vdds_sdcard	SD Card power supply	PWR	K7	-
vdds_usbhs18	USB HS (digital part) power supply	PWR	AK18	-
vdda_usbhs33	USB HS PHY power supply	PWR	AN22	-
vssa_usbhs	USB HS PHY ground	GND	AM19	-
vdda_usbss18	USB SS DRD PHY power supply	PWR	AL18	-
vssa_usbss	USB SS DRD PHY ground	GND	AM18	-
vdds_osc	Crystal oscillator IO power supply	PWR	C27	-
vssa_xtal	Crystal oscillator IO Kelvin ground (same routing as OMAP3630 and OMAP4430)	GND	E31	-
vdda_slicer	Slicer IO power supply	PWR	B27	-
vssa_slicer	Slicer IO ground	GND	A27	-
vddq_vref_ddrch1	VREF cell power supply for LPDDR2, DDR3 DQ channel 1 (or EMIF1)	PWR	G18	-
vddq_vref_ddrch2	VREF cell power supply for LPDDR2, DDR3 DQ channel 2 (or EMIF2)	PWR	W7	-
vddq_ddr_ch1	LPDDR2 (Channel 1) dm / dqs / ndqs power supply	PWR	A29 / A26 / A24 / A20 / A18 / A15 / A13 / A10 / A8 / A6 / D33 / G33 / G25 / G24 / G20 / G19 / G9 / H9 / L33 / L27 / M27	A24 / A19 / A14 / A5 / B16 / B7 / C21 / C11 / C9 / D26 / F27 / J25
vddq_ddr_ch2	LPDDR2 (Channel 2) dm / dqs / ndqs power supply	PWR	E1 / H7 / H1 / J7 / L1 / N1 / P7 / R7 / T1 / V1 / AD7 / AD1 / AE7 / AG7 / AG5 / AG1 / AK1 / AN10 / AN7 / AN5	D2 / G1 / J2 / L2 / N3 / R1 / Y1 / AB1 / AF9 / AF4 / AF2 / AG7
ddrch1_vref_dq	LPDDR2, DDR3 DQ VREF output power supply to memory for channel 1	PWR	-	A17
ddrch2_vref_dq	LPDDR2, DDR3 DQ VREF output power supply to memory for channel 2	PWR	-	U1

Table 2-40. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vddca_vref_lpddr2ch1	LPDDR2 CA VREF (Channel 1) power supply	PWR	AG18	-
vddca_vref_lpddr2ch2	LPDDR2 CA VREF (Channel 2) power supply	PWR	AB27	-
lpddr2ch1_vref_ca_out	LPDDR2 CA VREF output power supply to memory for channel 1	PWR	-	AG15
lpddr2ch2_vref_ca_out	LPDDR2 CA VREF output power supply to memory for channel 2	PWR	-	V27
vddca_lpddr2ch1	LPDDR2 CA / clk / clk enable / chip select (Channel 1) power supply	PWR	AJ23 / AJ22 / AN26 / AN20 / AN18	AF16 / AF14 / AG21
vddca_lpddr2ch2	LPDDR2 CA / clk / clk enable / chip select (Channel 2) power supply	PWR	T33 / AA33 / AC33 / AG29 / AH29	N27 / U26 / W26
vdd_core	Core and oscillator power supply	PWR	H26 / H25 / H8 / J26 / J8 / K14 / K13 / K12 / L14 / L13 / L12 / L11 / L8 / M13 / M12 / M11 / M10 / M8 / P14 / P13 / P12 / P11 / P10 / R14 / R13 / T14 / U22 / U21 / U20 / V23 / V22 / V21 / V20 / Y25 / Y24 / Y23 / AA23 / AA18 / AB25 / AB24 / AB23 / AB18 / AC23 / AC18 / AD25 / AD24 / AD23 / AE16 / AE15 / AE14 / AE13 / AE8 / AF9 / AF8	-
vdd_core_sense[2]	Core and oscillator output sensor feedback	PWR	AC27	-
vdd_mm	MultiMedia power supply	PWR	R12 / R11 / R10 / R9 / T13 / T12 / T11 / T10 / T9 / W14 / W13 / W12 / W11 / W10 / W9 / Y22 / Y21 / Y19 / Y11 / Y10 / AA22 / AA19 / AA16 / AA15 / AA14 / AA13 / AA12 / AA11 / AA10 / AA9 / AB22 / AB21 / AB19 / AB11 / AB10 / AC22 / AC19 / AC16 / AC15 / AC14 / AC13 / AC12 / AC11 / AC10 / AC9 / AD22 / AD21 / AD19 / AD11 / AE11	-
vdd_mm_sense[2]	MultiMedia sensor output sensor feedback	PWR	AJ21	-
vdd_mpu	MPU power supply	PWR	H24 / H23 / H22 / H21 / H20 / H19 / K23 / K22 / K21 / K20 / K19 / K18 / K17 / L25 / L24 / L23 / L22 / L21 / L20 / L19 / L18 / L17 / P25 / P23 / P22 / P21 / P20 / P19 / P18 / P17 / R26 / R25 / R23 / R22 / R21 / R20	-
vdd_mpu_sense[2]	MPU sensor output sensor feedback	PWR	P26	-
vss_mpu_sense[2]	MPU sensor output sensor feedback ground	GND	D27	-
vpp1	eFuse power supply	PWR	AE5	-

Table 2-40. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vss	Main ground	GND	A28 / A25 / A19 / A16 / A14 / A12 / A9 / A7 / C2 / D3 / D2 / F33 / F1 / G17 / H33 / H18 / H17 / H16 / H15 / H14 / H13 / H12 / H11 / H10 / J25 / J24 / J23 / J22 / J21 / J20 / J19 / J18 / J17 / J16 / J15 / J14 / J13 / J12 / J11 / J10 / J9 / K26 / K25 / K24 / K16 / K15 / K11 / K10 / K9 / K8 / K1 / L26 / L16 / L15 / L10 / L9 / M33 / M26 / M25 / M24 / M23 / M22 / M21 / M20 / M19 / M18 / M17 / M16 / M15 / M14 / M9 / M1 / N26 / N25 / N24 / N23 / N22 / N21 / N20 / N19 / N18 / N17 / N16 / N15 / N14 / N13 / N12 / N11 / N10 / N9 / N8 / P24 / P16 / P15 / P9 / P8 / R33 / R24 / R19 / R18 / R17 / R16 / R15 / R8 / R1 / T26 / T25 / T24 / T23 / T22 / T21 / T20 / T19 / T18 / T17 / T16 / T15 / T8 / U27 / U26 / U25 / U24 / U23 / U19 / U18 / U17 / U16 / U15 / U14 / U13 / U12 / U11 / U10 / U9 / U8 / U7 / V25 / V24 / V19 / V18 / V17 / V16 / V15 / V14 / V13 / V12 / V11 / V10 / V9 / V8 / W26 / W25 / W24 / W23 / W22 / W21 / W20 / W19 / W18 / W17 / W16 / W15 / W8 / W1 / Y26 / Y20 / Y18 / Y17 / Y16 / Y15 / Y14 / Y13 / Y12 / Y9 / Y8 / AA26 / AA25 / AA24 / AA21 / AA20 / AA17 / AA8 / AA3 / AA2 / AE33 / AB26 / AB20 / AB17 / AB16 / AB15 / AB14 / AB13 / AB12 / AB9 / AB8 / AB7 / AC26 / AC25 / AC24 / AC21 / AC20 / AC17 / AC8 / AD33 / AD26 / AD20 / AD18 / AD17 / AD16 / AD15 / AD14 / AD13 / AD12 / AD10 / AD9 / AD8 / AE26 / AE25 / AE24 / AE23 / AE22 / AE21 / AE20 / AE19 / AE18 / AE17 / AE12 / AE10 / AE9 / AE1 / AF26 / AF25 / AF24 / AF23 / AF22 / AF21 / AF20 / AF19 / AF18 / AF17 / AF16 /	A26 / A23 / A20 / A16 / A13 / A6 / A2 / B27 / B17 / B10 / B8 / B3 / B1 / E25 / E3 / G27 / H1 / K26 / K1 / L27 / M27 / M2 / T2 / T1 / U27 / U2 / V26 / W27 / Y2 / AB26 / AC3 / AE21 / AE5 / AF21 / AF15 / AF11 / AF10 / AF1 / AG16 / AG14 / AG8 / AG2
vss	Main ground	GND	AF15 / AF14 / AF13 / AF12 / AF11 / AF10 / AG33 / AG17 / AG10 / AG3 / AG2 / AH1 / AM32 / AM2 / AN25 / AN19 / AN11 / AN8 / AN6 / V7	
vdda_dpll_core_emu_abe	Core, EMU, and ABE DPLL power supply	PWR	V26	-
vdda_dpll_mm_l4per	MM and L4 interconnect DPLL power supply	PWR	T7	-
vdda_dpll_hdmi	HDMI PHY DPLL power supply	PWR	AG23	-
vdda_dpll_mpu	MPU DPLL power supply	PWR	V27	-
vdda_ldo_core	Core SRAM LDO power supplu	PWR	T5	-
vdda_ldo_mm	MM SRAM LDO power supply	PWR	AG15	-

Table 2-40. Power Supply Signal Descriptions (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	BALL BOTTOM [4]	BALL TOP [5]
vdda_ldo_mpu	MPU SRAM LDO power supply	PWR	G14	-
vdda_ldo_emu_wkup(1)	Wake-up / emulation LDOs power supply	PWR	V29	-
vnwa_emu_wkup(1)	Internal EMU wake-up power signal to be connected to vdda_ldo_emu_wkup on board	PWR	W29	-
vdda_vbgap_core	Bandgap, core LDOs power supply	PWR	Y7	-
cap_vdda_ldo_sram_core_array	CORE SRAM array LDO output	PWR	AG19	-
cap_vdda_ldo_sram_mm_array	MM SRAM array LDO output	PWR	AG16	-
cap_vdda_ldo_sram_mpu_array	MPU SRAM array LDO output	PWR	G16	-
cap_vdda_ldo_sram_mpu_array2	MPU SRAM array2 LDO output	PWR	N7	-
cap_vddldo_emu_wkup	MPU wake-up and EMU LDO output	PWR	T27	-
cap_vbb_ldo_mm	MPU MM LDO output	PWR	AJ16	-
cap_vbb_ldo_mpu	MPU MPU LDO output	PWR	E16	-

(1) vnwa_emu_wkup and vdda_ldo_emu_wlup must be connected on the board.

(2) An optimized power distribution network is recommended for vdd_mpu_sense, vss_mpu_sense, vdd_mm_sense, and vdd_core_sense SMPS feedback sensors between the OMAP5430 device and the power management IC (PMIC).

3 Electrical Characteristics

NOTE

For more information, see Power, Reset and Clock Management / PRCM Subsystem Environment / External Voltage Inputs or Initialization / Preinitialization / Power Requirements section of the OMAP543x TRM.

3.1 Absolute Maximum Ratings

Stresses beyond those listed as absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Section 3.3, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 3-1. Absolute Maximum Rating Over Junction Temperature Range

PARAMETER		LIMITS
Supply voltage ranges (steady state)	Core (vdd_mpu, vdd_mm, vdd_core, vdds_hsic, vddq_ddr_ch1, vddq_vref_ddrch1, vddq_ddr_ch2, vddq_vref_ddrch2, vddca_lpddr2ch1, vddca_vref_lpddr2ch1, vddca_lpddr2ch2, vddca_vref_lpddr2ch2, vdda_ldo_emu_wkup(7), vnwa_emu_wkup(7))	–0.4 V to 1.5 V
	IO analog (vdds_1p8, vdda_dsiporta, vdda_dsiportc, vdda_hdmi, vdda_csiporta, vdda_csiportb, vdda_csiportc, vdda_sata, vdds_usbhs18, vdda_usbss18, vdda_dpll_core_emu_abe, vdda_dpll_mm_l4per, vdda_dpll_hdmi, vdda_dpll_mpu, vdda_ldo_mm, vdda_ldo_mpu, vdda_vbgap_core)	–0.5 V to 2 V
	IO 1.8 V (vdds_c2c, vdds_hdmi, vdds_bank2, vdds_bank4, vdds_bank5, vdds_bank8, vdds_bank9, vdds_bank10, vdds_bank11, vdds_bank12, vdds_bank14, vdds_bank15, vdds_bank16, vdds_bank18, vdds_bank19, vdds_bank21, vdds_bank23, vdds_bank24, vdds_bank25, vdds_bank26, vdds_osc, vdda_slicer, vdda_ldo_core, vdds_emmc)	–0.5 V to 2.1 V
	IO 3.3 V (vdds_sdcard, vdda_usbhs33)	–0.5 V to 3.8 V
Input and output voltage ranges (steady state)	Core IOs	–0.4 V to 1.5 V
	Analog IOs	–0.5 V to 2 V
	1.8-V IOs	–0.5 V to 2.1 V
	3.3-V Dual-voltage IOs operating at 1.8 V	–0.5 V to 2.1 V
	3.3-V IOs	–0.5 V to 3.8 V
T_J	Absolute junction temperature range (vpp turned off—floating)	-40°C to 125°C
Electrostatic discharge (ESD) performance(1)	ESD-HBM (Human Body Model)(2)	±1000 V
	ESD-CDM (Charged Device Model)(3)	±250 V
Latch-up I-test performance	Current-pulse injection on each IO pin	±100 mA(5)
Latch-up overvoltage performance	Voltage injection on each supply	1.5 × Vddmax(6)
T_{STG}(4)	Storage temperature range after soldered onto PC Board	–65°C to 150°C

(1) Electrostatic discharge (ESD) to measure device sensitivity or immunity to damage caused by electrostatic discharges into the device.

(2) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.

(3) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible if necessary precautions are taken. Pins listed as 250 V may actually have higher performance.

(4) For tape and reel the storage temperature range is [–10°C to 50°C] with a maximum relative humidity of 70%. It is recommended returning to ambient room temperature before usage.

(5) Pins stressed per JEDEC JESD78D at 120°C (Class II) and passed with specified IO pin injection current and clamp voltage of 1.5 times maximum recommended IO voltage and negative 0.5 times maximum recommended IO voltage.

(6) Supplies stressed per JEDEC JESD78D at 120°C (Class II) and passed specified voltage injection.

(7) **CAUTION**: vnwa_emu_wkup and vdda_ldo_emu_wkup must be connected together on the board.

3.2 Maximum Current Ratings at Ball Level

Table 3-2 summarizes the maximum estimated power consumption at the ball level.

Table 3-2. Maximum Current Ratings at Ball Level[1]

PARAMETER			MAX	UNIT
vdd_mpu[1]	Maximum current rating for MPU	MPU at OPPSPEEDBIN	6460	mA
		MPU at HIGH	4400	
vdd_mm[1]	Maximum current rating for multimedia		2145	mA
vdd_core[1]	Maximum current rating for core, DLL		890	mA
vdds_1p8	Maximum current rating for second IO signal to ensure the VDDS ramping		See[4]	mA
vdds_bankX[5]	Maximum current rating for serial bank X IO		See[4]	mA
vdds_emmc	Maximum current rating for eMMC dual-voltage IO		See[4]	mA
vdds_c2c	Maximum current rating for Miscallenious IO		See[4]	mA
vdds_hsic	Maximum current rating for HS interchip data		See[4]	mA
vdds_sdcard	Maximum current rating for SD Card		See[4]	mA
vdds_hdmi	Maximum current rating for HDMI IOs (CEC, HPD, DDC)		See[4]	mA
vdda_dsiporta	Maximum current rating for DSI PHY (Port A) display primary port 1 (main cut), DSI1_A		19.3	mA
vdda_dsiportc	Maximum current rating for DSI PHY (Port C) display primary port 2 (main cut), DSI1_C		19.3	mA
vdda_hdmi	Maximum current rating for HDMI PHY (TMDS)		15	mA
vdda_csiporta	Maximum current rating for CSI (Port A) PHY camera (main cut)		4.6	mA
vdda_csiportb	Maximum current rating for CSI (Port B) PHY camera (main cut)		2.7	mA
vdda_csiportc	Maximum current rating for CSI (Port C) PHY camera (main cut)		1.75	mA
vdda_sata	Maximum current rating for SATA PHY		40	mA
vdds_usbhs18	Maximum current rating for USB HS (digital part)		26	mA
vdda_usbhs33	Maximum current rating for USB HS PHY		34	mA
vdda_usbss18	Maximum current rating for USB SS DRD PHY		45	mA
vdds_osc	Maximum current rating for crystal oscillator IO		2	mA
vdda_slicer	Maximum current rating for slicer IO		1.1	mA
vddq_ddr_ch1	Maximum current rating for LPDDR2 (channel 1) dm / dqs / ndqs		400	mA
vddq_vref_ddrch1	Maximum current rating for VREF cell power supply for LPDDR2, DDR3 DQ channel 1 (or EMIF1)		400	mA
vddq_ddr_ch2	Maximum current rating for LPDDR2 (channel 2) dm / dqs / ndqs		400	mA
vddq_vref_ddrch2	Maximum current rating for VREF cell power supply for LPDDR2, DDR3 DQ channel 2 (or EMIF2)		400	mA
vddca_lpddr2ch1	Maximum current rating for LPDDR2 CA / clk / clk enable / chip select (channel 1)		400	mA
vddca_vref_lpddr2ch1	Maximum current rating for VREF cell power supply for LPDDR2 CA channel 1 (or EMIF1)		400	mA
vddca_lpddr2ch2	Maximum current rating for LPDDR2 CA / clk / clk enable / chip select (channel 2)		400	mA
vddca_vref_lpddr2ch2	Maximum current rating for VREF cell power supply for LPDDR2 CA channel 2 (or EMIF2)		400	mA
vpp1[3]	Maximum current rating for eFuse		50	mA
vdda_dpll_core_emu_abe	Maximum current rating for core, EMU, and ABE DPLL		9	mA
vdda_dpll_mm_l4per	Maximum current rating for MM and L4 interconnect DPLL		6	mA
vdda_dpll_hdmi	Maximum current rating for HDMI PHY DPLL		6	mA
vdda_dpll_mpu	Maximum current rating for MPU DPLL		3	mA
vdda_ldo_core	Maximum current rating for core SRAM LDO		60	mA
vdda_ldo_mm	Maximum current rating for MM SRAM LDO		85	mA

Table 3-2. Maximum Current Ratings at Ball Level(1) (continued)

PARAMETER		MAX	UNIT
vdda_ldo_mpu	Maximum current rating for MPU SRAM LDO	145	mA
vdda_ldo_emu_wkup(2)	Maximum current rating for wake-up / emulation LDOs	75	mA
vnwa_emu_wkup(2)	Maximum current rating for internal EMU wake-up power signal to be connected to vdda_ldo_emu_wkup on board	30	mA
vdda_vbgap_core	Maximum current rating for bandgap, core LDOs	5	mA

(1) With SmartReflex™ enabled

(2) **CAUTION**: vnwa_emu_wkup and vdda_ldo_emu_wkup must be connected together on the board.

(3) A pulse width of 1000 ns and an amplitude of 2 V is required to program each eFuse bit. Otherwise, VPP1 must not be supplied.

(4) The sum of the maximum current consumption for these power supplies is 260 mA.

(5) The vdds_bankX described in this table are applicable for X = 2, 4, 5, 8, 9, 10, 11, 12, 14, 15, 16, 18, 19, 21, 23, 24, 25, and 26.

3.3 Recommended Operating Conditions

The device is used under the recommended operating conditions described in Table 3-3.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 3-3. Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
Input Power Supply Voltage Range						
vdd_mpu	Supply voltage range for MPU domain			See(1)		V
	Maximum noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f = 10 MHz		50		
vdd_mm	Supply voltage range for multimedia domain			See(1)		V
	Maximum noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f = 10 MHz		50		
vdd_core	Supply voltage range for OMAP core and DLL domain			See(1)		V
	Maximum noise (peak-peak)	f < 10 MHz		80		mV_{PPmax}
		f = 10 MHz		50		
vdda_dpll_mpu	Supply voltage for MPU DPLLs		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_core_emu_abe	Supply voltage for core, emulation, and audio DPLLs		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_mm_l4per	Supply voltage for multimedia and L4 interconnect DPLLs		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_dpll_hdmi	Supply voltage for HDMI DPLL		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_mpu	Supply voltage for MPU LDO		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_core	Supply voltage for SRAM LDO		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_mm	Supply voltage for MM SRAM LDO		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_ldo_emu_wkup(2)	Supply voltage for wake-up and emulation LDOs		1.14	1.20	1.26	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vnwa_emu_wkup(2)	Supply voltage for internal EMU wake-up		1.14	1.20	1.26	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_vbgap_core	Supply voltage for bandgap, core LDOs power supply		1.71	1.80	1.89	V
	Maximum noise (peak-peak)			50		mV_{PPmax}
vdda_csiporta	Supply voltage for CSI (Port A) PHY camera (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdda_csiportb	Supply voltage for CSI (Port B) PHY camera (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_csiportc	Supply voltage for CSI (Port C) PHY camera (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_dsiporta	Supply voltage for DSI PHY (Port A) display primary port 1 (main cut)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_dsiportc	Supply voltage for DSI PHY (Port A) display primary port 2—main cut	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_hdmi	Supply voltage for HDMI (analog part)	1.5-V Mode	1.43	1.50	1.57	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.5-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_hdmi	Supply voltage for HDMI (digital part)	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdda_sata	Supply voltage for SATA PHY	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdda_usbhs33	Supply voltage for USB HS PHY	3.3-V Mode	3.14	3.30	3.46	V
	Maximum noise (peak-peak)	3.3-V Mode		50		mV_{PPmax}
vdds_usbhs18	Supply voltage for USB HS (digital part)	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdda_usbss18	Supply voltage for USB SS DRD PHY	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdds_bankX[(3)]	Supply voltage for serial bank 2	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_c2c	Supply voltage for Miscallenious IO	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				
vdds_emmc	Supply voltage for eMMC	1.2-V Mode	1.14	1.20	1.26	V
		1.8-V Mode	1.71	1.80	1.89	
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
		1.8-V Mode				

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
vdds_hsic	Supply voltage for HS interchip data	1.2-V Mode	1.14	1.20	1.26	V
	Maximum noise (peak-peak)	1.2-V Mode		50		mV_{PPmax}
vdds_osc	Supply voltage for crystal oscillator	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vdda_slicer	Supply voltage for slicer IO	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode	50	50		mV_{PPmax}
vdds_sdcard	Supply voltage for SD Card	1.8-V Mode	1.71	1.80	1.89	V
		3.0-V Mode	2.7	3.0	3.6	
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
		3.0-V Mode				
vdds_1p8v	Supply voltage for 1.8-V IO macros	1.8-V Mode	1.71	1.80	1.89	V
	Maximum noise (peak-peak)	1.8-V Mode		50		mV_{PPmax}
vddq_ddr_ch1	Supply voltage for LPDDR2 channel 1		1.14	1.20	1.30	V
	Maximum noise (peak-peak)				60	mV_{PPmax}
vddq_ddr_ch2	Supply voltage for LPDDR2 channel 2		1.14	1.20	1.30	V
	Maximum noise (peak-peak)				60	mV_{PPmax}
vddq_vref_ddrch1	Supply voltage for embedded LPDDR2, DDR3 DQ VREF voltage generator channel 1		vddq_ddr_ch1[5]			V
	Maximum noise (peak-peak)				60	mV_{PPmax}
vddq_vref_ddrch2	Supply voltage for embedded LPDDR2, DDR3 DQ VREF voltage generator channel 2		vddq_ddr_ch2[5]			V
	Maximum noise (peak-peak)				60	mV_{PPmax}
vddca_lpddr2ch1	Supply voltage for LPDDR2 CA, clock, clock enable, and chip select channel 1		1.14	1.20	1.30	V
	Maximum noise (peak-peak)				60	mV_{PPmax}
vddca_lpddr2ch2	Supply voltage for LPDDR2 CA, clock, clock enable, and chip select channel 2		1.14	1.20	1.30	V
	Maximum noise (peak-peak)				60	mV_{PPmax}
vddca_vref_lpddr2ch1	Supply voltage for embedded LPDDR2 CA VREF voltage generator channel 1		vddca_lpddr2ch1[5]			V
	Maximum noise (peak-peak)				12	mV_{PPmax}
vddca_vref_lpddr2ch2	Supply voltage for embedded LPDDR2 CA VREF voltage generator channel 1		vddca_lpddr2ch2[5]			V
	Maximum noise (peak-peak)				12	mV_{PPmax}
vpp1[4]	Supply voltage for eFuse		See[4]			V
vss	Main ground		0			V
vssa_dsiporta	DSI PHY (Port A) ground		0			V
vssa_dsiportc	DSI PHY (Port C) ground		0			V
vssa_hdmi	HDMI PHY ground		0			V
vssa_csiporta	CSI (Port A) PHY camera (main cut) ground		0			V
vssa_csiportb	CSI (Port B) PHY camera (main cut) ground		0			V
vssa_csiportc	CSI (Port C) PHY camera (main cut) ground		0			V
vssa_sata	SATA PHY ground		0			V
vssa_usbhs	USB HS PHY ground		0			V
vssa_usbss	USB SS DRD PHY ground		0			V

Table 3-3. Recommended Operating Conditions (continued)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
vssa_xtal	Crystal oscillator IO Kelvin ground (same routing as for OMAP3630 and OMAP4430)		0		V
vssa_slicer	Slicer IO ground		0		V
vss_mpu_sense	MPU sensor ground		0		V
T_B (6)	Operating board (PCB) temperature range	–40		85	°C
T_J (6)	Operating junction temperature range (vpp turned off—floating)	–40		105 (7)	°C
$T_{J\text{-}VPP}$ (4)	Operating junction temperature range during eFuse programming (vpp turned on)	–10		65	°C
Output Power Supply Voltage Range					
ddrch1_vref_dq	LPDDR2, DDR3 DQ VREF output channel 1	0.49 × vddq_vref_ddrch1	0.50 × vddq_vref_ddrch1	0.51 × vddq_vref_ddrch1	V
ddrch2_vref_dq	LPDDR2, DDR3 DQ VREF output channel 2	0.49 × vddq_vref_ddrch2	0.50 × vddq_vref_ddrch2	0.51 × vddq_vref_ddrch2	V
lpddr2ch1_vref_ca_out	LPDDR2 CA VREF output channel 1	0.49 × vddca_vref_lpddr2ch1	0.50 × vddca_vref_lpddr2ch1	0.51 × vddca_vref_lpddr2ch1	V
lpddr2ch2_vref_ca_out	LPDDR2 CA VREF output channel 2	0.49 × vddca_vref_lpddr2ch2	0.50 × vddca_vref_lpddr2ch2	0.51 × vddca_vref_lpddr2ch2	V

(1) See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

(2) **CAUTION**: vnwa_emu_wkup and vdda_ldo_emu_wkup must be connected together on the board.

(3) The vdds_bankX recommended voltage ranges described in this table are applicable for X = 2, 4, 5, 8, 9, 10, 11, 12, 14, 15, 16, 18, 19, 21, 23, 24, 25, and 26.

(4) A pulse width of 1000 ns and an amplitude of 2 V is required to program each eFuse bit. Otherwise, VPP1 must not be supplied.

(5) vddq_vref_ddrch1 must be supplied from the same regulator as vddq_ddr_ch1.
vddq_vref_ddrch2 must be supplied from the same regulator as vddq_ddr_ch2.
vddca_vref_lpddr2ch1 must be supplied from the same regulator as vddca_lpddr2ch1.
vddca_vref_lpddr2ch2 must be supplied from the same regulator as vddca_lpddr2ch2.

(6) The board temperature (T_B) and junction temperature (T_J) range is defined for 2S2P board types (reference JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

(7) Product can be run at 120°C T_J for 9000 power-on hours.

3.4 DC Electrical Characteristics

Table 3-4 through Table 3-12 summarize the dc electrical characteristics.

NOTE

The data specified in Table 3-4 through Table 3-12 are subject to change.

NOTE

The interfaces or signals described in Table 3-4 through Table 3-12 correspond to the interfaces or signals available in multiplexing mode 0.

All interfaces or signals multiplexed on the balls described in these tables have the same dc electrical characteristics, unless multiplexing involves a PHY/GPIO combination in which case different dc electrical characteristics are specified for the different multiplexing modes.

NOTE

In the following tables, the V_{OL} and V_{OH} are JEDEC (JESD8-7A) compliant. This means:

- Normal range of V_{OH} / V_{OL} = [VDDS—0.45 V] / 0.45 V respectively, for I_{OH} / I_{OL} = 2 mA
- Wide range of V_{OH} / V_{OL} = [VDDS—0.2 V] / 0.2 V respectively, for I_{OH} / I_{OL} = 100 µA, except for the following signals: HDMI, I^2C interfaces in I^2C mode, MIPI CSI-2, CCPV2 D-PHY RX, DSI D-PHY TX, HDMI PHY, USB2 PHY, SATA PHY, MMC/SDIO (SD Card), USB HSIC, USB3 PHY RX, USB3 PHY TX, HDQ-1-Wire, sys_nreswarm, fref_xtal_out, kpd_col[7:0], and usbd0_hs_dp-dm.

3.4.1 LPDDR2 DC Electrical Characteristics

Table 3-4 summarizes the LPDDR2 dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (i[2:0], sr[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.

Table 3-4. LPDDR2 DC Electrical Characteristics[3]

PARAMETER			MIN	NOM	MAX	UNIT
Signal Names in Mode 0 (Single-Ended Signals): ddrch1_dq[31:0], lpddr2ch1_ca[9:0], ddrch1_dm[3:0], lpddr2ch1_ncs[1:0], lpddr2ch1_cke[1:0], ddrch2_dq[31:0], lpddr2ch2_ca[9:0], ddrch2_dm[3:0], lpddr2ch2_ncs[1:0], lpddr2ch2_cke[1:0] **Top Balls:** A4 / B4 / B5 / C5 / B6 / A7 / C7 / A8 / E27 / F26 / G25 / G26 / H26 / H27 / J26 / J27 / A11 / B11 / A12 / B12 / B13 / C13 / B14 / A15 / A21 / B21 / A22 / B22 / B23 / C23 / B24 / B25 / AF12 / AG13 / AF13 / AE13 / AE15 / AE19 / AG20 / AF20 / AG22 / AF22 / A10 / C26 / C17 / B20 / AG19 / AF19 / AG18 / AF18 / AG10 / AE9 / AG9 / AF8 / AE7 / AF7 / AF6 / AG6 / G3 / G2 / F2 / F1 / E2 / E1 / D1 / C2 / AF3 / AE2 / AD1 / AD2 / AC2 / AC1 / AB2 / AA3 / P2 / P1 / N2 / N1 / M1 / L3 / L1 / K2 / AA26 / AA27 / Y26 / Y27 / W25 / P26 / N25 / N26 / M26 / L25 / AG4 / J3 / W1 / U3 / P27 / R26 / R27 / R25						
Driver Mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 × vddx_lpddr2[1]			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1 × vddx_lpddr2[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)	68	80	92	Ω
		I[2:0] = 001 (Imp60)	51	60	69	
		I[2:0] = 010 (Imp48)	41	48	55	
		I[2:0] = 011 (Imp40)	34	40	46	
		I[2:0] = 100 (Imp34)	29	34	39	
t_{OT}	Output transition time (rise time, t_R, or fall time, t_F, evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 O and C_{LOAD} = 5 pF[3]	sr[2:0] = 000 (Fastest)	0.162		0.325	ns
		sr[2:0] = 001 (Faster)	0.162		0.33	
		sr[2:0] = 010 (Fast)	0.162		0.34	
		sr[2:0] = 011 (Slow)	0.168		0.35	
		sr[2:0] = 100 (Slower)	0.168		0.35	
		sr[2:0] = 101 (Slowest-1)	0.168		0.36	
		sr[2:0] = 110 (Slowest-2)	0.168		0.36	
		sr[2:0] = 111 (Slowest-3)	0.175		0.36	
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold		vddy_vref_lpddr2[2] + 0.13		vddx_lpddr2[1] + 0.2	V
V_{IL}	Low-level input threshold		–0.2		vddy_vref_lpddr2[2] —0.13	V
V_{CM}	Input common-mode voltage		vddy_vref_lpddr2[2] —0.1 × vddx_lpddr2[1]		vddy_vref_lpddr2[2] + 0.1 × vddx_lpddr2[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Signal Names in Mode 0 (Differential Signals): ddrch1_dqs[3:0], ddrch1_ndqs[3:0], lpddr2ch1_ck, lpddr2ch1_nck, ddrch2_dqs[3:0], ddrch2_ndqs[3:0], lpddr2ch2_ck, lpddr2ch2_nck **Top Balls:** A9 / E26 / C15 / C19 / B9 / D27 / B15 / B19 / AF17 / AG17 / AG5 / J1 / AA1 / R3 / AF5 / H2 / AA2 / R2 / T27 / T26						
Driver Mode						
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)		0.9 × vddx_lpddr2[1]			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)				0.1 × vddx_lpddr2[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)	68	80	92	Ω
		I[2:0] = 001 (Imp60)	51	60	69	
		I[2:0] = 010 (Imp48)	41	48	55	
		I[2:0] = 011 (Imp40)	34	40	46	
		I[2:0] = 100 (Imp34)	29	34	39	

Table 3-4. LPDDR2 DC Electrical Characteristics[3] (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 O and C_{LOAD} = 5 pF[3]	sr[2:0] = 000 (Fastest)	0.162		0.325	ns
		sr[2:0] = 001 (Faster)	0.162		0.33	
		sr[2:0] = 010 (Fast)	0.162		0.34	
		sr[2:0] = 011 (Slow)	0.168		0.35	
		sr[2:0] = 100 (Slower)	0.168		0.35	
		sr[2:0] = 101 (Slowest-1)	0.168		0.36	
		sr[2:0] = 110 (Slowest-2)	0.168		0.36	
		sr[2:0] = 111 (Slowest-3)	0.175		0.36	
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold		0.5 × vddx_lpddr2[1] + 0.13		vddx_lpddr2[1] + 0.2	V
V_{IL}	Low-level input threshold		–0.2		0.5 × vddx_lpddr2[1]—0.13	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Differential Receiver Mode						
V_{SWING}	Input voltage swing		0.26		vddx_lpddr2[1] + 0.4	V
V_{CM}	Input common-mode voltage		0.4 × vddx_lpddr2[1]		0.6 × vddx_lpddr2[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Signal Names in Mode 0 (VREF Signals): ddrch1_vref_dq, lpddr2ch1_vref_ca_out, ddrch2_vref_dq, lpddr2ch2_vref_ca_out **Top Balls:** A17 / AG15 / U1 / V27						
V_{REF}	Reference internal generation dc voltage level	vref_tap[1:0] = 00, 2-µA current load	0.49 × vddy_vref_lpddr2[2]	0.50 × vddy_vref_lpddr2[2]	0.51 × vddy_vref_lpddr2[2]	V
		vref_tap[1:0] = 01, 4-µA current load	0.49 × vddy_vref_lpddr2[2]	0.50 × vddy_vref_lpddr2[2]	0.51 × vddy_vref_lpddr2[2]	
		vref_tap[1:0] = 10, 8-µA current load	0.49 × vddy_vref_lpddr2[2]	0.50 × vddy_vref_lpddr2[2]	0.51 × vddy_vref_lpddr2[2]	
		vref_tap[1:0] = 11, 32-µA current load	0.49 × vddy_vref_lpddr2[2]	0.50 × vddy_vref_lpddr2[2]	0.51 × vddy_vref_lpddr2[2]	
C_{CAP}	Decoupling capacitor	ccap[1:0] = 00	No capacitor connected			
		ccap[1:0] = 01	Capacitor between Bias2 and Vss			
		ccap[1:0] = 10	Capacitor between Bias2 and Vdds			
		ccap[1:0] = 11	Capacitor between Bias2 and Vss and capacitor between Bias2 and Vdds			

(1) vddx_lpddr2 can have the value vddq_ddr_ch1, vddq_ddr_ch2, vddca_lpddr2ch1, or vddca_lpddr2ch2 depending on the ball used. For more information on the power supply name and the corresponding ball, see Table 2-1, POWER NAME [10] column.

(2) vddy_vref_lpddr2 can have the value vddca_vref_lpddr2ch1, vddca_vref_lpddr2ch2, vddq_vref_ddrch1, or vddq_vref_ddrch2 depending on the ball used. For more information on the power supply name and the corresponding ball, see Table 2-1, POWER NAME [10] column.

(3) Output transition time/turn on time is measured with the measurement setup (see Figure 3-1) with Z_O = 40 Ω and C_{LOAD} = 5 pF (lumped, no transmission line model).

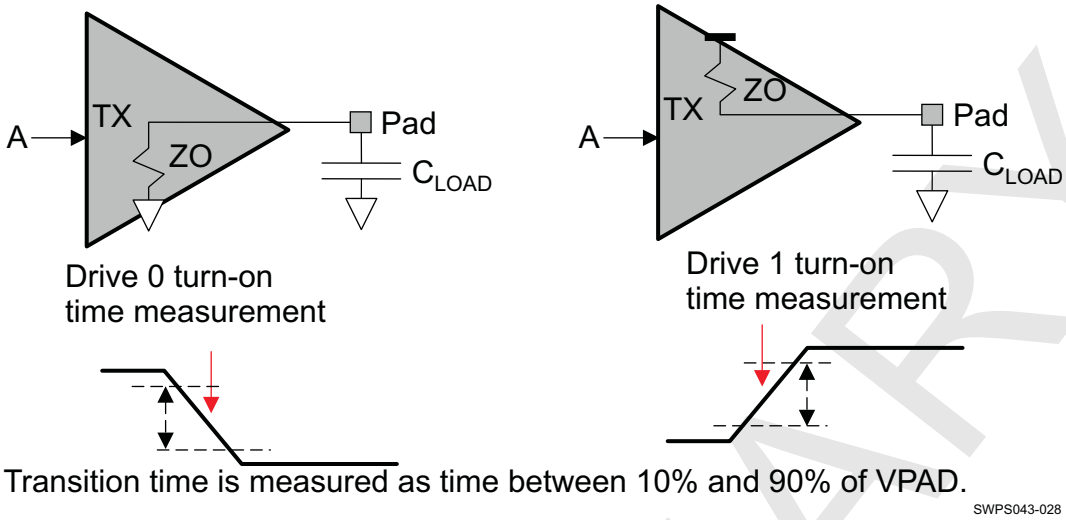


Figure 3-1. Output Transition Time Measurement

3.4.2 Camera DC Electrical Characteristics

3.4.2.1 CSI-2 MIPI D-PHY and CCPV2 DC Electrical Characteristics

Table 3-5 summarizes the CSI-2 MIPI D-PHY and CCPV2 dc electrical characteristics in multiplexing mode 0.

Table 3-5. CSI-2 MIPI D-PHY and CCPV2 RX DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0[11]**:** csiportc_lane[1:0]x, csiportc_lane[1:0]y, csiportb_lane[2:0]x, csiportb_lane[2:0]y, csiporta_lane[4:0]x, csiporta_lane[4:0]y **Bottom Balls:** J2 / K2 / J3 / K3 / Y3 / W3 / V3 / Y2 / W2 / V2 / L2 / M2 / N2 / P2 / R2 / L3 / M3 / N3 / P3 / R3					
MIPI D-PHY Mode Low-Power Receiver (LP-RX)					
V_{IH}	Input high-level voltage	880		1350	mV
V_{IL}	Input low-level voltage			550	mV
V_{ITH}	Input high-level threshold[1]			880	mV
V_{ITL}	Input low-level threshold[2]	550			mV
V_{HYS}	Input hysteresis[3]	25			mV
MIPI D-PHY Mode Ultralow Power Receiver (ULP-RX)					
V_{IH}	Input high-level voltage	880			mV
V_{IL}	Input low-level voltage			300	mV
V_{ITH}	Input high-level threshold[1]			880	mV
V_{ITL}	Input low-level threshold[4]	300			mV
V_{HYS}	Input hysteresis[3]	25			mV
MIPI D-PHY Mode High-Speed Receiver (HS-RX)					
V_{IDTH}	Differential input high-level threshold	70			mV
V_{IDTL}	Differential input low-level threshold			–70	mV
V_{IDMAX}	Maximum differential input voltage[7]			270	mV
V_{IHHS}	Single-ended input high voltage[5]			460	mV
V_{ILHS}	Single-ended input low voltage[5]	–40			mV
V_{CMRXDC}	Differential input common-mode voltage[5][6][8]	70		330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω

Table 3-5. CSI-2 MIPI D-PHY and CCPV2 RX DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
CCP2 Mode (only on MIPI CSI-2 port B and MIPI CSI-2 port C) Signal Names: csiportc_lane[1:0]x, csiportc_lane[1:0]y, csiportb_lane[2:1]x, csiportb_lane[2:1]y **Bottom Balls:** J2 / K2 / J3 / K3 / Y3 / W3 / Y2 / W2					
V_{CM}	Input common-mode voltage range(8)	0.6	0.9	1.2	V
V_{OS}	Receiver input dc offset	–20		20	mV
V_{ID}	Receiver input differential amplitude	140	200	400	mV_{PP}
ΔV_{ID} / V_{ID}	Amplitude mismatch between lane modules	–10%		10%	
ΔV_{CMRX}	Common-mode mismatch between lane modules	–100		100	mV
ΔV_{CMn}	Common-mode noise ripple(9)	–15		15	mV
Z_{ID}	Differential input impedance	80	100	120	Ω
GPI Mode(10) Signal Names(11): csiportc_lane[1:0]x, csiportc_lane[1:0]y, csiportb_lane[2:0]x, csiportb_lane[2:0]y, csiporta_lane[4:0]x, csiporta_lane[4:0]y **Bottom Balls:** J2 / K2 / J3 / K3 / Y3 / W3 / V3 / Y2 / W2 / V2 / L2 / M2 / N2 / P2 / R2 / L3 / M3 / N3 / P3 / R3					
V_{ITH}	Input high-level threshold	0.65 × Vdd		Vdd + 0.3	V
V_{ITL}	Input low-level threshold	–0.3		0.35 × Vdd	V
V_{HYS}	Input hysteresis voltage	150			mV
C_{IN}	Input capacitance			1.3	pF
t_{TIN}	Input transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}), minimum at minimum load and maximum at maximum load			10	ns

(1) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.

(2) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both low-power (LP) receivers will detect low during HS signaling.

(3) To reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST}. V_{HYST} is the difference between the V_{ITH} threshold and the V_{ITL} threshold.

(4) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during ultralow power (ULP) state. The LP receiver is not required to detect HS single-ended voltage as 0 in this state.

(5) Excluding possible additional RF interference of 200 mV_{PP} beyond 450 MHz.

(6) This value includes a ground difference of 50 mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.

(7) This number corresponds to the V_{ODMAX} transmitter.

(8) Common mode is defined as the average voltage level of X and Y: $V_{CMRX} = (V_X + V_Y) / 2$.

(9) Common mode ripple may be due to t_R or t_F and transmission line impairments in the PCB.

(10) The GPI mode is only available through multiplexing modes 3, 4, and 6. For more information, see Table 2-1. The GPI mode is only supported in 1.8-V mode.

(11) For more information regarding the pin name (or ball name) and corresponding signal name, see Table 2-6, *MIPI CSI-2 Signal Descriptions*, or Table 2-7, *CCPV2 Signal Descriptions*.

3.4.3 Display DC Electrical Characteristics

3.4.3.1 HDMI DC Electrical Characteristics

NOTE

For more information on HDMI, please contact your TI representative.

3.4.3.2 DSI-1 MIPI D-PHY (DSI1_A and DSI1_C) DC Electrical Characteristics

Table 3-6 summarizes the DSI-1 MIPI D-PHY dc electrical characteristics in multiplexing mode 0.

Table 3-6. DSI-1 MIPI D-PHY (DSI1_A and DSI1_C) TX DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0: dsiporta_lane[4:0]x, dsiporta_lane[4:0]y, dsiportc_lane[4:0]x, dsiportc_lane[4:0]y **Bottom Balls:** R32 / T32 / V32 / W32 / Y32 / R31 / T31 / V31 / W31 / Y31 / AB32 / AC32 / AD32 / AE32 / AF32 / AB31 / AC31 / AD31 / AE31 / AF31					
MIPI D-PHY Mode High-Speed Transmitter (HS-TX)					
V_{CMTX}	HS transmit static common-mode voltage(1)(2)	150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV
$\lvert V_{OD}\rvert$	HS transmit differential output voltage(1)(3)	140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is Differential-1 or Differential-0			14	mV
V_{OHHS}	HS output high voltage(1)			360	mV
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch			10%	
$\Delta V_{CMTX(HF)}$	Common-level variation above 450 MHz			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variation between 50 MHz and 450 MHz	–50		50	mV_{PEAK}
t_{TOUT}	Output transition time (t_R or t_F evaluated between 20% and 80% of V_{PAD})	0.10(11)			ns
				0.3(8)(9)	$UI_{INST,MIN}$
				0.35(8)(10)	$UI_{INST,MIN}$
MIPI D-PHY Mode Low-Power Transmitter (LP-TX)					
V_{OL}	Thevenin output low level	–50		50	mV
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V
Z_{OLP}	Output impedance of LP transmitter	110			Ω
t_{TOUT}	Output transition time (t_R or t_F evaluated between 20% and 80% of V_{PAD})			25	ns
MIPI D-PHY Mode Low-Power Receiver (LP-RX)					
V_{IH}	Input high-level voltage	880		1350	mV
V_{IL}	Input low-level voltage			550	mV
V_{ITH}	Input high-level threshold(4)			880	mV
V_{ITL}	Input low-level threshold(5)	550			mV
V_{HYS}	Input hysteresis(6)	25			mV
MIPI D-PHY Mode Ultralow Power Receiver (ULP-RX)					
V_{IH}	Input high-level voltage	880			mV
V_{IL}	Input low-level voltage			300	mV
V_{ITH}	Input high-level threshold(4)			880	mV
V_{ITL}	Input low-level threshold(7)	300			mV
V_{HYS}	Input hysteresis(6)	25			mV
MIPI D-PHY mode Low-Power Contention Detector (LP-CD)					
V_{IHCD}	Input high-level contention voltage	450			mV
V_{ILCD}	Input low-level contention voltage			200	mV

(1) Value when driving into a differential load impedance anywhere in the range of 80 to 125 Ω.

(2) Common mode is defined as the average voltage level of X and Y: $V_{CMTX} = (V_X + V_Y) / 2$.

(3) $V_{OD} = V_X — V_Y$

(4) V_{ITH} is the voltage at which the receiver is required to detect a high state in the input signal.

(5) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. V_{ITL} is larger than the maximum single-ended line high voltage during HS transmission. Therefore, both LP receivers will detect low during HS signaling.

(6) To reduce noise sensitivity on the received signal, the LP receiver is required to incorporate a hysteresis, V_{HYST}. V_{HYST} is the difference between the V_{ITH} threshold and the V_{ITL} threshold.

(7) V_{ITL} is the voltage at which the receiver is required to detect a low state in the input signal. Specification is relaxed for detecting 0 during ultralow power (ULP) state. The LP receiver is not required to detect HS single-ended voltage as 0 in this state.

(8) $UI_{INST,MIN} = 1/(2 \times f_{max})$, where f_{max} is the highest fundamental frequency of the HS data transmission.

(9) Applicable when operating at HS bit rates = 1 Gbps (UI = 1 ns).

(10) Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

(11) Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates = 1 Gbps (UI = 1 ns) must not use values below 0.15 ns.

3.4.4 I^2C DC Electrical Characteristics

Table 3-7 summarizes the I^2C dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (LB0[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.

NOTE

I^2C in 1.2 V is not supported in the OMAP5430 ES2.0 device.

Table 3-7. I^2C DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0: i2c[5:2]_scl, i2c[5:2]_sda, i2c1_pmic_scl, i2c1_pmic_sda, sr_pmic_scl, sr_pmic_sda					
Bottom Balls: AL32 / AK22 / AB3 / AF30 / AL31 / AJ20 / AB2 / AF29 / K29 / H30 / H29 / J29					
I^2C Standard Mode—1.2 V and 1.8 V(3)					
V_{IH}(5)	Input high-level threshold	0.7 × vddsx(1)		vddsx(1) + 0.5	V
V_{IL}(5)	Input low-level threshold	–0.5		0.3 × vddsx(1)	V
I_I	Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd	–10		10	µA
C_I	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current	NA(2)		NA(2)	V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 5 pF to 400 pF			250	ns
t_{OR}	Output rise time from V_{ILmax} to V_{IHmin} with a capacitive load from 5 pF to 150 pF with internal pullup resistor enabled	20 + 0.1 × C_B		250	ns
I^2C Fast Mode—1.2 V and 1.8 V					
V_{IH}(5)	Input high-level threshold	0.7 × vddsx(1)		vddsx(1) + 0.5	V
V_{IL}(5)	Input low-level threshold	–0.5		0.3 × vddsx(1)	V
I_I	Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd	–10		10	µA
C_I	Input capacitance			10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current	0		0.2 × vddsx(1)	V

Table 3-7. I²C DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance C_B from 5 pF to 400 pF		20 + 0.1 × C_B		250	ns
t_{OR}	Output rise time from V_{ILmax} to V_{IHmin} with a capacitive load from 5 pF to 150 pF with internal pullup resistor enabled		20 + 0.1 × C_B		250	ns
R_{INPU}	Internal I²C pullup resistance for a given load range	LB[1:0] = 00	3	4 (5 to 15 pF)	6	kΩ
		LB[1:0] = 01	1.6	2.1 (15 to 50 pF)	3.17	
		LB[1:0] = 10	0.64	0.84 (50 to 150 pF)	1.27	
		LB[1:0] = 11		NA		
I²C High-Speed Mode—1.2 V and 1.8 V						
V_{IH}[5]	Input high-level threshold		0.7 × vddsx[1]		vddsx[1] + 0.5	V
V_{IL}[5]	Input low-level threshold		–0.5		0.3 × vddsx[1]	V
I_I	Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd		–10		10	µA
C_I	Input capacitance				10	pF
V_{OL3}	Output low-level threshold open-drain at 3-mA sink current		0		0.2 × vddsx[1]	V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a capacitive load from 5 pF to 100 pF at 3-mA sink current		10		40	ns
	Output fall time from V_{IHmin} to V_{ILmax} with a capacitive load of 400 pF at 3-mA sink current		20		80	ns
t_{OR}	Output rise time from V_{ILmax} to V_{IHmin} with a capacitive load from 5 pF to 80 pF with internal pullup resistor enabled		10		40	ns
R_{INPU}	Internal I²C pullup resistance for a given load range	LB[1:0] = 00	1.37	1.8 (5 to 12 pF)	2.72	kΩ
		LB[1:0] = 01	0.76	1.0 (12 to 25 pF)	1.51	
		LB[1:0] = 10	0.4	0.525 (25 to 50 pF)	0.79	
		LB[1:0] = 11	0.23	0.3 (50 to 80 pF)	0.45	
Non-I²C Mode (Normal Mode)[4]						
1.2-V Mode						
V_{IH}[5]	Input high-level threshold		0.7 × vddsx[1]		vddsx[1] + 0.5	V
V_{IL}[5]	Input low-level threshold		–0.5		0.3 × Vdd	V
V_{HYS}	Input hysteresis voltage		50			mV
I_I	Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd		–10		10	µA
C_I	Input capacitance				10	pF
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		0.75 × vddsx[1]			
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.25 × vddsx[1]	V
t_{OT}	Output transition time (t_R or t_F) at 40-pF load, evaluated between 10% to 90% V_{PAD}				10	ns
1.8-V Mode						
V_{IH}[5]	Input high-level threshold		0.7 × vddsx[1]		vddsx[1] + 0.5	V
V_{IL}[5]	Input low-level threshold		–0.5		0.3 × vddsx[1]	V
V_{HYS}	Input hysteresis voltage		130			mV
I_I	Input current at each IO pin with an input voltage between 0.1 × vdd to 0.9 × vdd		–10		10	µA
C_I	Input capacitance				10	pF
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)		vddsx[1]—0.45			
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)				0.45	V
t_{OT}	Output transition time (t_R or t_F) at 40-pF load, evaluated between 10% to 90% of V_{PAD}				6	ns

(1) Depending on the I^2C ball, vddsx can have the value: vdds_bank8, vdds_bank10, vdds_bank16, vdds_bank18, vdds_bank26, or vdds_hdmi. For more information, see Table 2-1, POWER NAME [10] column.

(2) V_{OL} specification is not applicable in the standard mode.

(3) The pullup versus load settings of I^2C fast mode also apply to I^2C standard mode.

(4) This mode is only available through multiplexing modes 2 through 6. For more information, see Table 2-1 or Table 2-2. In the normal mode (non-I^2C mode), the pullup or pulldown nominal strength is 100 µA.

(5) Input voltage level could be in an undefined state (between V_{IL} and V_{IH}) for a maximum of 1 second without causing any damage.

3.4.5 USB DC Electrical Characteristics

3.4.5.1 USB2 PHY DC Electrical Characteristics

Table 3-8 summarizes the USB2 PHY dc electrical characteristics in multiplexing mode 0.

Table 3-8. USB2 PHY DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0: usbd0_hs_dp, usbd0_hs_dm **Bottom Balls:** AM20 / AL20					
USB2 PHY in USB LS / FS Single-Ended Receiver					
V_{IH}	Input high-level threshold	2			V
V_{IL}	Input low-level threshold			0.8	V
Z_{INP}	Input impedance exclusive of a pullup or pulldown resistor (pullup and pulldown resistors are disabled, DP and DM are in Hi-Z state).	300			kΩ
USB2 PHY in USB GPI LS / FS Receiver(1)					
V_{IH}	Input high-level threshold	2			V
V_{IL}	Input low-level threshold			0.8	V
USB2 PHY in USB LS / FS Differential Receiver					
V_{CM}	Differential common-mode range(2)	0.8		2.5	V
V_{DI}	Differential Input sensitivity	0.2			V
V_{HYS}	Differential receiver hysteresis	0		0	mV
USB2 PHY in USB HS Differential Receiver					
V_{HSSQ}	HS squelch detection threshold (differential signal amplitude)	100	125	150	mV
V_{HSDISC}	HS disconnect detection threshold (differential signal amplitude)	525	600	625	mV
V_{HSCM}	HS data signaling common mode voltage range(2)	–50	200	500	mV
Z_{HSDRCV}	Input impedance in HS receive mode (or termination impedance)	40.5		49.5	Ω
USB2 PHY in USB LS / FS Differential Transmitter					
V_{OH}	Output high-level threshold (pulldown R = 15 kΩ on both DP and DM)	2.8	3.3	3.6	V
V_{OL}	Output low-level threshold (pullup R = 1.5 kΩ at 3.6 V on both DP and DM)	0	0.1	0.3	V
V_{CRS}	Output signal crossover voltage (pulldown R = 15 kΩ on both DP and DM, pullup R = 1.5 kΩ at 3.6 V on DM only)	1.3		2	Ω
Z_{DRV}	Driver output resistance	28	45	49.5	Ω
t_{LSOT}	Output transition time (t_R or t_F), evaluated between 10% to 90% of V_{PAD}, C_L = [200 to 600] pF on both DP and DM, pullup R = 1.5 kΩ at 3.6 V for DM only	75		300	ns
t_{FSOT}	Output transition time (t_R or t_F), evaluated between 10% to 90% of V_{PAD}, C_L = 50 pF on both DP and DM	4		20	ns
USB2 PHY in GPO LS / FS Driver(1)					
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)	2.8	3.3	3.6	V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)	0	0.1	0.4	V
USB2 PHY in USB HS Differential Transmitter					
V_{HSOI}	HS output idle level	–10.0	0.0	10.0	mV
V_{HSOH}	HS output data signaling high	360	400	440	mV
V_{HSOL}	HS output data signaling low	–10.0	0.0	10.0	mV

Table 3-8. USB2 PHY DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CHIRPJ}	Chirp J level	700	900	1100	mV
V_{CHIRPK}	Chirp K level	–900	–700	–500	mV
t_{OT}	Output transition time (t_R or t_F) evaluated between 10% to 90% of V_{PAD}	500			ps
Z_{HSDRV}	Driver output resistance	40.5	45	49.5	Ω
Signal Name: usbphy_ce **Bottom Ball:** AL19					
USB2 PHY in USB LS / FS Differential Transmitter					
V_{OH}	Output high-level threshold (pulldown R = 15 kΩ on both DP and DM)	2.8	3.3	3.6	V
V_{OL}	Output low-level threshold (pullup R = 1.5 kΩ at 3.6 V on both DP and DM)	0	0.1	0.3	V
V_{CRS}	Output signal crossover voltage (pulldown R = 15 kΩ on both DP and DM, pullup R = 1.5 kΩ at 3.6 V on DM only)	1.3		2	Ω
Z_{DRV}	Driver output resistance	28	45	49.5	Ω
t_{LSOT}	Output transition time (t_R or t_F), evaluated between 10% to 90% of V_{PAD}, C_L = [200 to 600] pF on both DP and DM, pullup R = 1.5 kΩ at 3.6 V for DM only	75		300	ns
t_{FSOT}	Output transition time (t_R or t_F), evaluated between 10% to 90% of V_{PAD}, C_L = 50 pF on both DP and DM	4		20	ns
USB2 PHY in GPO LS / FS Driver(1)					
V_{OH}	Output high-level threshold (I_{OH} = 4 mA)	2.8	3.3	3.6	V
V_{OL}	Output low-level threshold (I_{OL} = 4 mA)	0	0.1	0.4	V
USB2 PHY in USB HS Differential Transmitter					
V_{HSOI}	HS output idle level	–10.0	0.0	10.0	mV
V_{HSOH}	HS output data signaling high	360	400	440	mV
V_{HSOL}	HS output data signaling low	–10.0	0.0	10.0	mV
V_{CHIRPJ}	Chirp J level	700	900	1100	mV
V_{CHIRPK}	Chirp K level	–900	–700	–500	mV
t_{OT}	Output transition time (t_R or t_F) evaluated between 10% to 90% of V_{PAD}	500			ps
Z_{HSDRV}	Driver output resistance	40.5	45	49.5	Ω

(1) The GPIO modes are only available through multiplexing mode 4. For more information, see Table 2-1 or Table 2-2.

(2) Common mode is defined as the average voltage level of DP and DM: $V_{CM} = (V_{DP} + V_{DM}) / 2$.

3.4.5.2 USB HSIC DC Electrical Characteristics

Table 3-9 summarizes the USB HSIC dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (i[2:0], sr[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.

Table 3-9. USB HSIC DC Electrical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Signal Names in Mode 0 (Single-Ended Signals): usbb1_hsic_strobe, usbb1_hsic_data, usbb2_hsic_strobe, usbb2_hsic_data, usbb3_hsic_strobe, usbb3_hsic_data **Top Balls:** B26 / C26 / B25 / C25 / D29 / D30					
Driver Mode					
V_{OH}	High-level output threshold (I_{OH} = 0.1 mA)	0.9 × vdds_hsic			V
V_{OL}	Low-level output threshold (I_{OL} = 0.1 mA)			0.1 × vdds_hsic	V
C_{PAD}	Pad capacitance			3	pF

Table 3-9. USB HSIC DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
Z_O	Output impedance (drive strength)	I[2:0] = 000 (Imp80)		80		Ω
		I[2:0] = 001 (Imp60)		60		
		I[2:0] = 010 (Imp48)		48		
		I[2:0] = 011 (Imp40)		40		
		I[2:0] = 100 (Imp34)		34		
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 O and C_{LOAD} = 5 pF(2)	sr[2:0] = 000 (Fastest)	0.162		0.325	ns
		sr[2:0] = 001 (Faster)	0.162		0.33	
		sr[2:0] = 010 (Fast)	0.162		0.34	
		sr[2:0] = 011 (Slow)	0.168		0.35	
		sr[2:0] = 100 (Slower)	0.168		0.35	
		sr[2:0] = 101 (Slowest-1)	0.168		0.36	
		sr[2:0] = 110 (Slowest-2)	0.168		0.36	
		sr[2:0] = 111 (Slowest-3)	0.175		0.36	
Single-Ended Receiver Mode						
V_{IH}	High-level input threshold		vddy_vref_lpddr2(1) + 0.13		vdds_hsic + 0.2	V
V_{IL}	Low-level input threshold		–0.2		vddy_vref_lpddr2(1)— 0.13	V
V_{CM}	Input common-mode voltage		vddy_vref_lpddr2(1)— 0.1 × vdds_hsic		vddy_vref_lpddr2(1) + 0.1 × vdds_hsic	V

(1) vddy_vref_lpddr2 can have the value vddca_vref_lpddr2ch1, vddca_vref_lpddr2ch2, vddq_vref_ddrch1, or vddq_vref_ddrch2 depending on the ball used. For more information of the power supply name and the corresponding pin, ball, see Table 2-1, POWER NAME [10] column.

(2) Output transition time/turn on time is measured with the measurement setup (see Figure 3-1) with Z_O = 40 Ω and C_{LOAD} = 5 pF (lumped, no transmission line model).

3.4.5.3 USB3 PHY DC Electrical Characteristics

NOTE

The USB3 RX PHY module is compliant with the receiver electrical parameters specified in the *Universal Serial Bus 3.0 Specification*, Revision 1.0, November 12, 2008.

NOTE

The USB3 TX PHY module is compliant with the transmitter electrical parameters and LFPS electrical parameters specified in the *Universal Serial Bus 3.0 Specification*, Revision 1.0, November 12, 2008.

NOTE

For more information regarding the USB3 pin name (or ball name) and corresponding signal name, see Table 2-22, *USB Signal Descriptions*.

3.4.6 SD Card DC Electrical Characteristics

Table 3-10 summarizes the SD Card dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (IC[1:0), UHS104 or UHS50 modes) see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.

Table 3-10. SD Card DC Electrical Characteristics

PARAMETER				MIN	NOM	MAX	UNIT
Signal Names in Mode 0: sdcard_clk, sdcard_cmd, sdcard_data[3:0] **Bottom Balls:** E3 / E2 / F3 / F2 / G2 / G3							
1.8-V Mode							
V_{IH} (3)	Input high-level threshold			1.27			V
V_{IL} (3)	Input low-level threshold					0.58	V
V_{HYS}	Input hysteresis voltage (1)			50			mV
C_{PAD}	Pad capacitance (including package capacitance)					5	pF
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)			1.4			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)					0.45	V
Z_O	Output impedance (drive strength)		IC[1:0] = 00 (driver type B)		44		Ω
			IC[1:0] = 01 (driver type A)		33		
			IC[1:0] = 10 (driver type C)		58		
			IC[1:0] = 11 (driver type D)		100		
t_{OT}	Output transition time (t_R or t_F evaluated between V_{OL} and V_{OH}) for driver type B		UHS104 mode (104 MB/s maximum)	0.4		1.32	ns
			UHS50 mode (50 MB/s maximum)	0.7		2.75	
C_{LOAD}	Load capacitance (at which the t_{OT} are measured)	IC[1:0] = 00 (driver type B)	UHS104 mode (104 MB/s maximum)			15	pF
			UHS50 mode (50 MB/s maximum)			30	
		IC[1:0] = 01 (driver type A)	UHS104 mode (104 MB/s maximum)			21	
			UHS50 mode (50 MB/s maximum)			43	
		IC[1:0] = 10 (driver type C)	UHS104 mode (104 MB/s maximum)			11	
			UHS50 mode (50 MB/s maximum)			23	
		IC[1:0] = 11 (driver type D) (2)	UHS104 mode (104 MB/s maximum)			-	
			UHS50 mode (50 MB/s maximum)			-	
R_{RF}	t_R / t_F ratio			0.7	1.00	1.4	-
3.3-V Mode							
V_{IH} (3)	Input high-level threshold			0.625 × vdds_sdcard			V
V_{IL} (3)	Input low-level threshold					0.25 × vdds_sdcard	V
V_{HYS}	Input hysteresis voltage			40			mV
C_{PAD}	Pad capacitance (including package capacitance)					5	pF
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)			0.75 × vdds_sdcard			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)					0.125 × vdds_sdcard	V
Z_O	Output impedance (drive strength)		IC[1:0] = 01 (driver type A)		33		Ω
			IC[1:0] = 10 (driver type C)		58		

Table 3-10. SD Card DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}	Output transition time (t_R or t_F evaluated between V_{IHmin} and V_{ILmax})	HS mode (25 MB/s maximum)			3	ns
		Default speed mode (12 MB/s maximum)			10	
C_{LOAD}	Load capacitance (at which the t_{OT} are measured)	HS mode (25 MB/s maximum)			40	pF
		Default speed mode (12 MB/s maximum)			40	

(1) The hysteresis of the input buffer is programmable with the hyst_en register bit. For more information, see the OMAP543x TRM.

(2) The load capacitance specification does not exist for driver type D. It will be the maximum load that the host can support.

(3) Input voltage level could be in an undefined state (between V_{IL} and V_{IH}) for a maximum of 1 second without causing any damage.

3.4.7 SATA PHY DC Electrical Characteristics

NOTE

The SATA RX PHY module is compliant with the electrical specifications of SATA up to Gen2m.

NOTE

The SATA TX PHY module is compliant with the electrical specifications of SATA up to Gen2m.

NOTE

For more information regarding the SATA PHY pin name (or ball name) and corresponding signal name, see Table 2-23, *SATA Signal Descriptions*.

3.4.8 System DC Electrical Characteristics

Table 3-11 summarizes the System dc electrical characteristics in multiplexing mode 0.

NOTE

For more information on the IO cell configurations (DS[1:0], SC[1:0]), see the Control Module / Control Module Functional Description / Functional Register Description / Signal Integrity Parameter Control Registers With Pad Group Assignment section of the OMAP543x TRM.

NOTE

1.2-V mode for System signals is not supported in the OMAP5430 ES2.0 device.

Table 3-11. System DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
Signal Names in Mode 0: sys_nrespwron, sys_nreswarm **Bottom Balls:** F31 / F29						
1.8-V Mode						
V_{IH}	Input high-level threshold		0.65 × vdds_bank24			V
V_{IL}	Input low-level threshold				0.35 × vdds_bank24	V
V_{HYS}	Input hysteresis voltage		135			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)		vdds_bank24—0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)				0.45	V
Z_O	Output impedance (drive strength)	DS[1:0] = 00		120		Ω
		DS[1:0] = 01		60		
		DS[1:0] = 10		40		
		DS[1:0] = 11		30		
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 O and C_{LOAD} = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
		SC[1:0] = 01 (slow)	0.9		2	
		SC[1:0] = 10 (fast)	0.6		1.1	
		SC[1:0] = 11 (fastest)(1)	NA(1)		NA(1)	
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 60 O and C_{LOAD} = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.8	ns
		SC[1:0] = 01 (slow)	1		2.2	
		SC[1:0] = 10 (fast)	0.7		1.4	
		SC[1:0] = 11 (fastest)(1)	NA(1)		NA(1)	
Signal Names in Mode 0: fref_xtal_in, fref_xtal_out **Bottom Balls:** E32 / D32						
V_{IH}	Input high-level threshold		0.65 × vdds_osc			V
V_{IL}	Input low-level threshold				0.35 × vdds_osc	V
V_{HYS}	Input hysteresis voltage		150			mV
C_{IN}	Input capacitance		1.25	1.4	1.55	pF
t_{IT}	Input transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD})				5	ns
C_{OUT}	Load capacitance (C_{L1} = C_{L2})		12		24	pF
Signal Name in Mode 0: fref_xtal_clk **Bottom Ball:** D31						
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)		0.7 × vdds_osc			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)				0.3 × vdds_osc	V

Table 3-11. System DC Electrical Characteristics (continued)

PARAMETER		MIN	NOM	MAX	UNIT
f_{OUT}	Output frequency, fref_xtal_clk			100	MHz
t_{WOUT}	Output pulse duration, fref_xtal_clk low or high	0.45 × 1/f_{OUT}		0.55 × 1/f_{OUT}	ns
t_{OT}	Output transition time (t_R or t_F evaluated between 20% and 80% of V_{PAD}), fref_xtal_clk			0.5	ns
C_{OUT}	Load capacitance			5	pF
Signal Name in Mode 0: fref_slicer_in **Bottom Ball:** B28					
Single-ended Application Mode					
V_{SWING}	Input voltage swing(2)	500		1600	mV
R_{IN}	Input resistance		18.3		kΩ
C_{IN}	Input capacitance			2.5	pF
Single–ended High-Voltage CMOS Application Mode					
V_{IH}	Input high-level voltage	0.65 × vdda_slicer		2	V
V_{IL}	Input low-level voltage	–0.2		0.35 × vdda_slicer	V
R_{IN}	Input resistance		18.3		kΩ
C_{IN}	Input capacitance			2.5	pF
t_{IT}	Input transition time (t_R or t_F) evaluated between 10% to 90% of V_{PAD}	1.5		10	ns

(1) The SC[1:0] = 11 is the fastest bit setting. It is not supported.

(2) The input voltage swing is the peak-peak input voltage.

Minimum input common mode voltage—input voltage swing / 2 > 0 V

Maximum input common mode voltage + input voltage swing / 2 < 1.6 V

3.4.9 Other Balls DC Electrical Characteristics

Table 3-12 summarizes the dc electrical characteristics in multiplexing mode 0 for balls (using the SMART IO) other than the ones described in Section 3.4.1 through Section 3.4.8.

Table 3-12. Other Balls(4) DC Electrical Characteristics

PARAMETER			MIN	NOM	MAX	UNIT
1.8-V Mode						
V_{IH}(3)	Input high-level threshold		0.65 × vddsx(1)			V
V_{IL}(3)	Input low-level threshold				0.35 × vddsx(1)	V
V_{HYS}	Input hysteresis voltage		130			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)		vddsx(1)—0.45			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)				0.45	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	DS[1:0] = 00		120		Ω
		DS[1:0] = 01		60		
		DS[1:0] = 10		40		
		DS[1:0] = 11		30		
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 O and C_{LOAD} = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
		SC[1:0] = 01 (slow)	0.9		2.0	
		SC[1:0] = 10 (fast)	0.6		1.1	
		SC[1:0] = 11 (fastest)(2)	NA(2)		NA(2)	

Table 3-12. Other Balls[4] DC Electrical Characteristics (continued)

PARAMETER			MIN	NOM	MAX	UNIT
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 60 O and C_{LOAD} = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.75	ns
		SC[1:0] = 01 (slow)	1.0		2.25	
		SC[1:0] = 10 (fast)	0.7		1.4	
		SC[1:0] = 11 (fastest)[2]	NA[2]		NA[2]	
1.2-V Mode						
V_{IH}	Input high-level threshold		0.65 × vddsx[1]			V
V_{IL}	Input low-level threshold				0.35 × vddsx[1]	V
V_{HYS}	Input hysteresis voltage		60			mV
V_{OH}	Output high-level threshold (I_{OH} = 2 mA)		0.75 × vddsx[1]			V
V_{OL}	Output low-level threshold (I_{OL} = 2 mA)				0.25 × vddsx[1]	V
C_{PAD}	Pad capacitance (including package capacitance)				3	pF
Z_O	Output impedance (drive strength)	DS[1:0] = 00		120		Ω
		DS[1:0] = 01		60		
		DS[1:0] = 10		40		
		DS[1:0] = 11		30		
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 40 O and C_{LOAD} = 10 pF	SC[1:0] = 00 (slowest)	2.0		2.7	ns
		SC[1:0] = 01 (slow)	1.0		1.45	
		SC[1:0] = 10 (fast)	0.7		1.0	
		SC[1:0] = 11 (fastest)[2]	NA[2]		NA[2]	
t_{OT}	Output transition time (t_R or t_F evaluated between 10% and 90% of V_{PAD}) for drive strength = 60 O and C_{LOAD} = 10 pF	SC[1:0] = 00 (slowest)	2.0		2.75	ns
		SC[1:0] = 01 (slow)	1.15		1.65	
		SC[1:0] = 10 (fast)	0.9		1.3	
		SC[1:0] = 11 (fastest)[2]	NA[2]		NA[2]	

(1) For more information regarding the corresponding power supply (vddsx) for each ball described in the section, see Table 2-1, POWER NAME [10] column.

(2) The SC[1:0] = 11 is the fastest bit setting. It is not supported.

(3) Input voltage level could be in an undefined state (between V_{IL} and V_{IH}) for a maximum of 1 second without causing any damage.

(4) Other balls using the SMART IO.

3.5 External Capacitors

NOTE

For more information regarding the external capacitors, see Section 8.6, *External Capacitors* of the OMAP5430 DM PCB Guidelines.

3.6 Power-up and Power-down Sequences

3.6.1 Power-Up Sequence

NOTE

For more information, see Power, Reset and Clock Management / Reset Management Functional Description / Reset Sequences of OMAP543x TRM.

Figure 3-2 shows the power-up sequence.

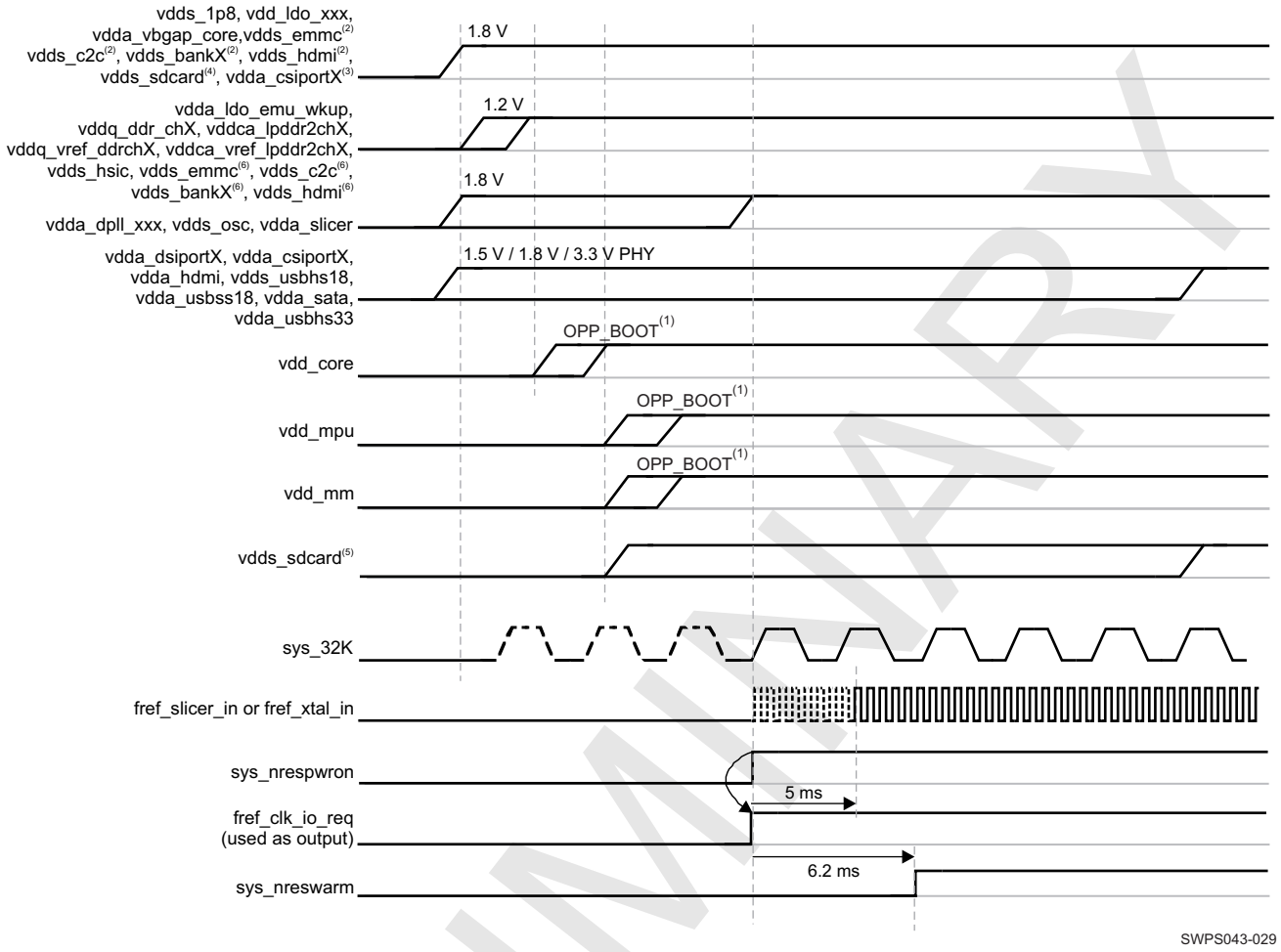


Figure 3-2. Power-Up Sequence

(1) The OMAP5430 ES2.0 device boots up with vdd_core, vdd_mpu, and vdd_mm at OPP_BOOT. See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

(2) In case the corresponding interfaces are used at 1.8 V.

(3) In case the MIPI CSI-2 interface is used as GPIO or CPI (function different from Muxmode 0).

(4) In case the SD Card interface is used at 1.8 V only (function different from Muxmode 0).

(5) In case the SD Card functional signals are used at 1.8 V or 3.0 V (Muxmode 0).

(6) In case the corresponding interfaces are used at 1.2 V.

NOTE

The DPLLs voltage supplies (vdda_dpll_xxx) and the system clock IO voltage supplies (vdds_osc and vdda_slicer) can be turned on at the same time as the other 1.8-V voltage supplies or only before sys_nrespwron release.

The 1.5-V, 1.8-V, and 3.3-V PHY voltage supplies can be turned on at the same time as the other 1.8-V voltage supplies or only when the corresponding applications are needed.

Once vdda_ldo_emu_wkup is turned on, vdd_core can be turned on. Once vdd_core is turned on, vdd_mpu and vdd_mm can be turned on.

If the SD Card functional signals are used at 1.8 V or 3.0 V, the vdds_sdcard voltage supply can be turned on any time after vdd_core ramp-up or only when the applications are needed.

sys_32k can be turned on any time after vdds_bankX ramp-up and before sys_nrespwron release.

Once the sys_nrespwron is released, the OMAP5430 device activates the fref_clk_ioreq signal.

Therefore, the fref_xtal_in or fref_slicer_in clock can be turned on. (Nevertheless, the system can turn on the fref_xtal_in or the fref_slicer_in clock before the fref_clk_ioreq activation provided the system clock IO voltage supplies are turned on.)

5 ms after the sys_nrespwron release, the system clock is considered as stabilized on the OMAP5430 oscillator input or slicer input. The clock may be supplied later provided it is perfectly stabilized when supplied.

1.2 ms (about 40 additional 32-kHz clock cycles) after the system clock is considered as stabilized, the OMAP5430 device releases its sys_nreswarm.

NOTE

Customer designs may optionally power-up only the boot interfaces (eMMC, uSD card, USB, and SATA) which their particular design needs to use. For example, if only eMMC is required then uSD card, USB, and SATA supplies do not need to be powered up. The TWL6035 PMIC is programmed to power up all the possible interfaces to be able to boot on any possible interface.

3.6.2 Power-Down Sequence

The following steps give two examples of power-down sequence supported by the OMAP5430 device:

1. Put the OMAP5430 device under reset (sys_nrespwron).
2. Stop all signals driven to its balls (sys_32k, fref_slicer_in, or fref_xtal_in).
3. Either:
   (a) Shutdown all voltage supplies at once. This sequence is described in black color in Figure 3-3.
   (b) Or, if the shutdown is sequenced, described in dashed blue color in Figure 3-3:
      (i) Turn off all PHY voltage supplies and SD Card voltage supply.
      (ii) Turn off the multimedia (IVA, DSP, and GPU) voltage domain supply (vdd_mm).
      (iii) Turn off the MPU voltage domain supply (vdd_mpu).
      (iv) Turn off the core voltage domain supply (vdd_core).
      (v) Turn off all DPLL and system clock IO voltage supplies.
      (vi) Turn off all 1.2-V IO voltage supplies.
      (vii) Turn off all remaining 1.8-V IO voltage supplies.

Figure 3-3 shows both power-down sequences: one of them is described in black color, and the other one in dashed blue color.

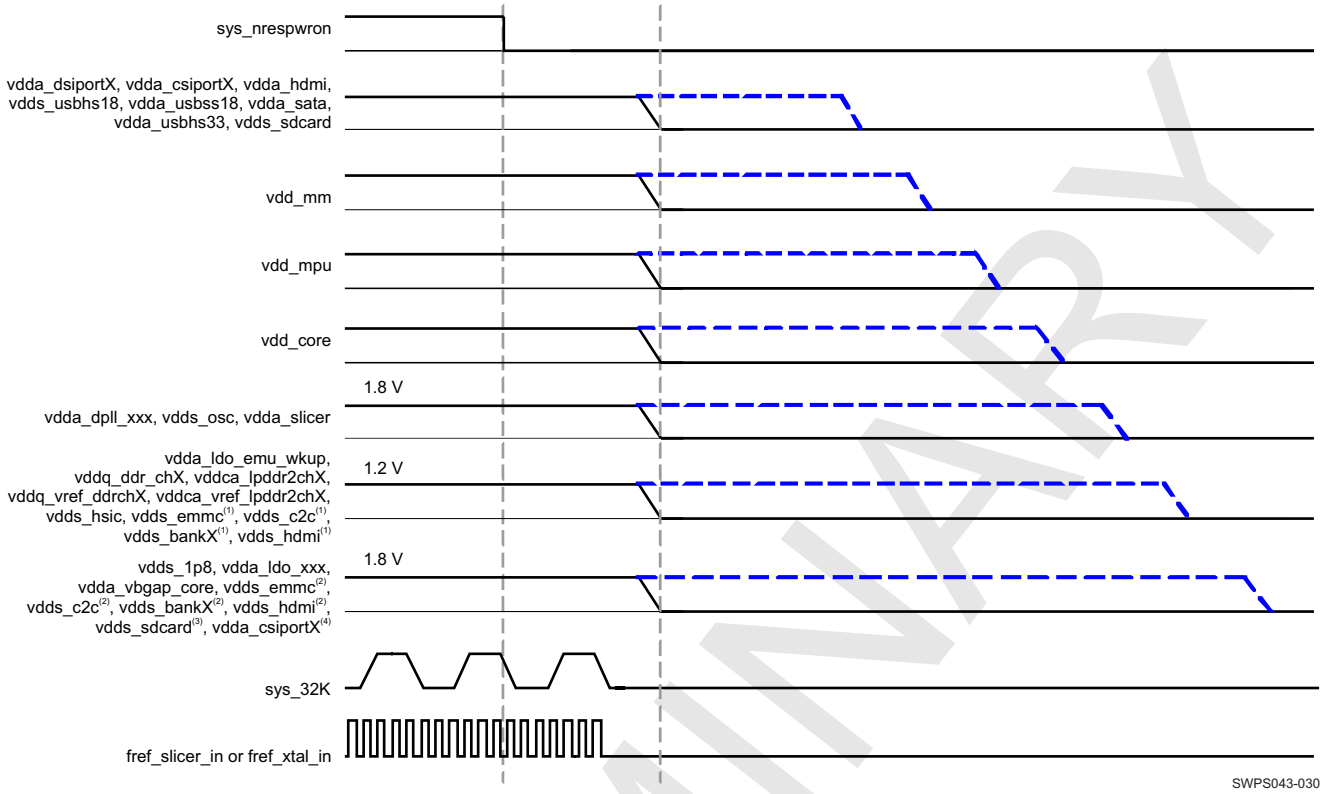


Figure 3-3. Power-Down Sequence(1)(2)(3)(4)

(1) In case the corresponding interfaces are used at 1.2 V.

(2) In case the corresponding interfaces are used at 1.8 V.

(3) In case the SD Card interface is used at 1.8 V only (function different from Muxmode 0).

(4) In case the MIPI CSI-2 interface is used as GPIO or CPI (function different from Muxmode 0).

NOTE

sys_32k can be turned off any time after sys_nrespwron assertion and before vdds_bankX shutdown.

The fref_xtal_in or fref_slicer_in clock can be turned off any time after sys_nrespwron assertion and before the system clock IO voltage supplies shutdown (vdds_osc, vdda_slicer).

4 Clock Specifications

NOTE

For more information, see Power Reset and Clock Management / PRCM Environment / External Clock Signal and Power Reset / PRCM Functional Description / PRCM Clock Manager Functional Description section of the OMAP543x TRM.

The OMAP5430 device operation requires the following clocks:

- The 32-kHz frequency clock is used for low frequency operation. It supplies the wake-up (WKUP) domain for operation in the lowest power mode, the clock source for the DPLL of the audio back-end module.
- The system clock (from either the fref_xtal_in or fref_slicer_in signal with the following possible frequencies: 12, 16.8, 19.2, 26, or 38.4 MHz) is the main source clock of the OMAP5430 device. It supplies the reference clock to the DPLLs as well as the functional clock to several OMAP modules.

The system clock source could be either:

- A CMOS square clock that enters on the fref_xtal_in pin (signal is IO voltage level) with fref_xtal_out left unconnected.
- A crystal oscillator clock managed by fref_xtal_in and fref_xtal_out. In this situation, the crystal clock frequency must be between 12 and 19.2 MHz (other values must be checked case by case). The crystal is oscillating on the fundamental frequency (oscillation on third harmonic is not supported).
- A sine wave (single-ended) clock that enters on the fref_slicer_in ball.
- A CMOS square clock that enters on the fref_slicer_in ball.

NOTE

It is recommended to not use the slicer bypass mode. Even in case of square clock used, it is better to use the slicer active mode.

The system clock source are configurable on sys_boot[5:4]. For more information, see the OMAP543x TRM.

The OMAP5430 device delivers four clock signals (fref_clk[3:0]_out) to external devices:

- The clocks are configurable and can be managed by software or by hardware thanks to the fref_clk[2:1]_req and fref_clk_ioreq (when in input direction) pins.
- When fref_clk_ioreq is configured as output, the signal is used to request an external clock source for the OMAP5430 device. When configured as input (oscillator enabled), this fref_clk_ioreq pin can be used as an additional clock request fref_clk0_req to the existing fref_clk[2:1]_req signals.
- Output fref_clk[3:0]_out clocks come from:
  - Either the input system clock and alternate clock (fref_xtalin or fref_slicer_in)
  - Or, a core clock (from DPLL_CORE output)
  - Or, a 192-MHz clock (from PER DPLL output)

  Each of this clock can be divided and independantly controlled by software. For more information, see the OMAP543x TRM.
- Each of the output clocks can be gated or enabled independently by activation of the associated clock request signals, fref_clk[2:1]_req or fref_clk_ioreq pins.

  The fref_clk_ioreq pin can be used as fref_clk0_req signal when configured as input pin (oscillator enabled).

  By default:
  - The fref_clk0_req auxiliary clock request (fref_clk_ioreq as input pin) is mapped on the fref_clk0_out auxiliary clock.
  - The fref_clk1_req auxiliary clock request is mapped on the fref_clk1_out auxiliary clock.

  - The fref_clk2_req auxiliary clock request is mapped on the fref_clk2_out auxiliary clock.
  - No auxiliary clock request is mapped on the fref_clk3_out auxiliary clock.

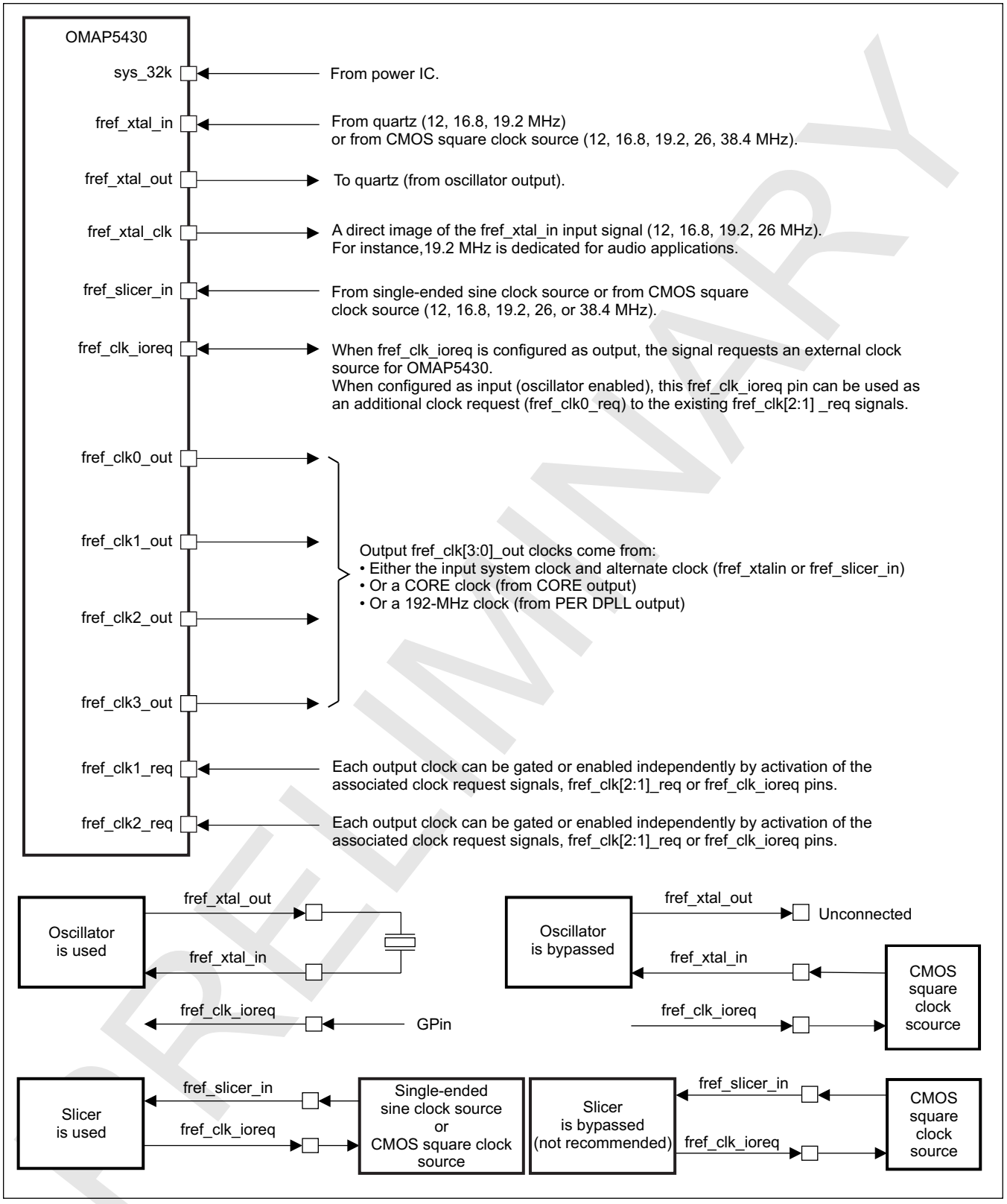
  A re-mapping is possible to map the fref_clkx_req clock request (x = [2:0]) on the fref_clky_out clock (y = [3:0]).

  The polarity of fref_clk[2:1]_req and fref_clk_ioreq pins is programmable (active High by default after reset).

- Input fref_clk_req2 and output fref_clk3_out signals are multiplexed on the same ball (see Table 2-2). Hence, fref_clk_req2 and fref_clk3_out are.
- fref_clk_ioreq is an open-drain output (driving a low-level when requesting clock, else output driver is in Hi-Z and line must have a pullup to maintain it inactive) or open-source (driving a high-level when requesting clock, else output driver is in Hi-Z and line must have a pulldown to maintain it inactive) for requesting the clock to an external clock source device when the SYS.CLK clock is not provided by the crystal oscillator (that is, when SYS_BOOT[5:4] ≠ 2b'00).

The OMAP5430 device also embeds an internal free-running 32-kHz oscillator that is always active as long as the the wake-up (WKUP) domain is supplied.

Figure 4-1 shows the external input clock sources and the output clocks to peripherals.



SWPS043-031

Figure 4-1. Clock Interface

4.1 Input Clock Specifications

4.1.1 Input Clock Requirements

The source of the internal system clock (SYS.CLK) could be either:

- A CMOS square clock that enters on the fref_xtal_in ball (with fref_xtal_out left unconnected on the CMOS square clock case).
- A crystal oscillator clock managed by fref_xtal_in and fref_xtal_out (oscillating in the fundamental 10-MHz to 20-MHz frequency range).
- A sine wave and single-ended clock that comes in the fref_slicer_in ball
- A CMOS square clock that enters on the fref_slicer_in ball.

Table 4-1 illustrates the requirements to supply an input clock to the device.

Table 4-1. Input Clock Requirements(4)

PAD	CLOCK FREQUENCY			STABILITY	DUTY CYCLE	JITTER	TRANSITION
sys_32k	32.768 kHz			± 200 ppm	-	-	< 30 ns
fref_xtal_in fref_xtal_out	12, 16.8, or 19.2 MHz		Crystal clock	± 50 (±5) ppm(3)	NA	NA	NA
	12, 16.8, 19.2, 26, or 38.4 MHz		Square clock	± 50 (±5) ppm(3)	45% to 55%	1% × $t_{c(XTALIN)}$(2) (ps) × X_{DIV}(1) — 390 (ps)	< 5 ns
fref_slicer_in fref_clk0_out	12, 16.8, 19.2, 26, or 38.4 MHz	Active mode	Single-ended sine clock	± 50 (±5) ppm(3)	38.5% to 61.5%	1% × $t_{c(SLICER)}$(2) (ps) × X_{DIV}(1) — 340 ps	NA
			Square clock	± 50 (±5) ppm(3)	45% to 55%	1% × $t_{c(SLICER)}$(2) (ps) × X_{DIV}(1) — 340 (ps)	< 10 ns

(1) In X_{DIV}, X_{DIV} represents the internal DSS DPLLs dividers. [$t_{c(XTALIN)}$ (ps) × X_{DIV}] or [$t_{c(SLICER)}$ (ps) × X_{DIV}] represents the input clock cycle coming to the DSS DPLLs (this means after dividing). For the other internal DPLLs, the X_{DIV} value is equal to 1. This input jitter limitation comes from the DPLL constraints shifted at ball level. To clarify this formula, please consider a maximum jitter of 1% of the clock period coming to the internal DPLL (input DPLL). For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP543x TRM.

(2) $t_{c(SLICER)}$ is the fref_slicer_in cycle time of the clock coming to fref_slicer_in ball.

$t_{c(XTALIN)}$ is the fref_xtal_in cycle time of the clock coming to fref_xtalin_in ball.

(3) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(4) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

4.1.1.1 sys_32k CMOS Input Clock

Table 4-2 summarizes the electrical characteristics of the sys_32k input clock.

Table 4-2. sys_32k Input Clock Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, sys_32k		32.768		kHz
C_I	Input capacitance			3	pF
R_I	Input resistance	3		10	GΩ

Table 4-3 details the input requirements of the sys_32k input clock.

Table 4-3. sys_32k Input Clock Timing Requirements(1)(2)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
CK0	1 / $t_{c(32k)}$	Frequency, sys_32k		32.768		kHz
	$t_{R(32k)}$	Rise time, sys_32k			30	ns
	$t_{F(32k)}$	Fall time, sys_32k			30	ns
	$t_{j(32k)}$	Frequency stability, sys_32k			200	ppm

(1) See Section 3.4.8, *System DC Electrical Characteristics*, SYS (clk32k …) part for sys_32k V_{IH} /V_{IL} parameters.

(2) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

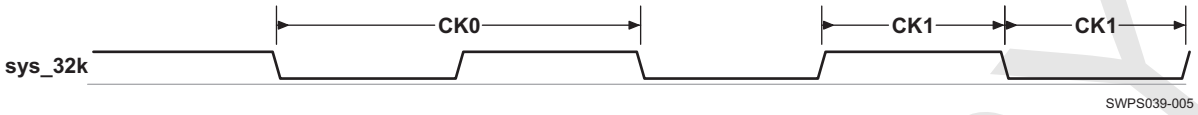


Figure 4-2. sys_32k Input Clock

4.1.1.2 fref_xtalin CMOS Input Clock

4.1.1.2.1 fref_xtal_in / fref_xtal_out External Crystal

An external crystal is connected to the device pins. Figure 4-3 describes the crystal implementation.

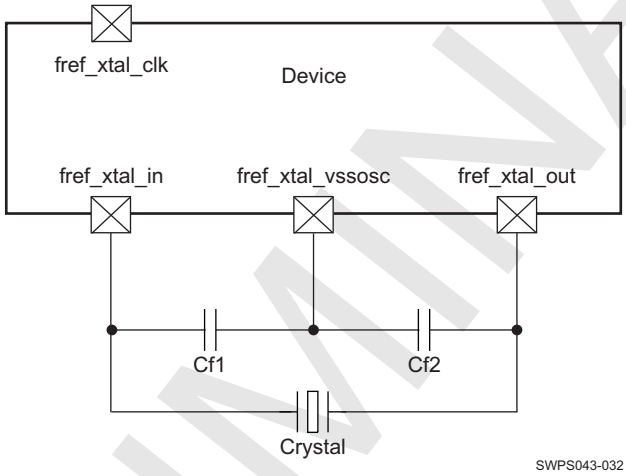


Figure 4-3. Crystal Implementation(1)

(1) When the oscillator is bypassed, the fref_xtal_in ball is connected to a square clock source, the fref_xtal_out ball is not connected and the fref_xtal_vssosc ball is connected to the ground.

When the oscillator is not used, the fref_xtal_in and fref_xtal_out balls can be connected to the ground, or not connected and the fref_xtal_vssosc ball is connected to the ground.

The crystal must be in the fundamental mode of operation and parallel resonant. Table 4-4 summarizes the required electrical constraints.

Table 4-4. Crystal Electrical Characteristics(2)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency		12, 16.8, or 19.2		MHz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$	12		24	pF
ESR(C_{f1},C_{f2}) (1)	Frequency 12 MHz, Negative resistor at nominal 500 Ω, Negative resistor at worst case 300 Ω			100	Ω
	Frequency 16.8 MHz and 19.2 MHz, Negative resistor at nominal 300 Ω, Negative resistor at worst case 180 Ω			60	
C_O	Crystal shunt capacitance			4.5	pF
L_M	Crystal motional inductance for f_p = 12 MHz		16		mH
C_M	Crystal motional capacitance		10.87		fF
D_L	Crystal drive level			0.5	mW

(1) Measured with the load capacitance specified by the crystal manufacturer. This load is defined by the foot capacitances tied in series. If C_L = 20 pF, then both foot capacitors will be $C_{f1} = C_{f2}$ = 40 pF. Parasitic capacitance from package and board must also be taken in account.

(2) The crystal motional resistance R_M is related to the equivalent series resistance (ESR) by the following formula:

$ESR = R_M \times (1 + (C_O \times C_{f1} \times C_{f2} / (C_{f1} + C_{f2})))$ 2.

When selecting a crystal, the system design must take into account the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 4-5 details the switching characteristics of the oscillator and the requirements of the input clock.

Table 4-5. Oscillator Switching Characteristics—Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_p	Oscillation frequency		12, 16.8, or 19.2		MHz
t_{sX}	Start-up time(1)(2)			1.2	ms

(1) Start-up time is defined as the time the oscillator takes to gain fref_xtal_in amplitude enough to have 45% to 55% duty cycle at the core input from the time power down (PWRDN) is released. Start-up time is a strong function of crystal parameters. At power-on reset, the time is adjustable using the pin itself. The reset must be released when the oscillator or clock source is stable. To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in the t_{sX} parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 µs.

4.1.1.2.2 fref_xtal_in Squarer Input Clock

Table 4-6 summarizes the fref_xtal_in input square clock electrical characteristics.

Table 4-6. fref_xtal_in Input Square Clock Electrical Characteristics—Bypass Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency		12, 16.8, 19.2, 26, or 38.4		MHz
C_I	Input capacitance	1.00	1.15	1.35	pF
R_I	Input resistance	3.1	132	1100	MΩ
t_{sX}	Start-up time(1)		See(2)		ms

(1) To switch from bypass mode to crystal or from crystal mode to bypass mode, there is a waiting time about 100 µs; however, if the chip comes from bypass mode to crystal mode the crystal will start-up after time mentioned in Table 4-5, t_{sX} parameter.

(2) Before the processor boots up and the oscillator is set to bypass mode, there is a waiting time when the internal oscillator is in application mode and receives a square wave. The switching time in this case is about 100 µs.

Table 4-7 details the fref_xtal_in input square clock timing requirements.

Table 4-7. fref_xtal_in Input Square Clock Timing Requirements—Bypass Mode(3)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
OCS0	$1 / t_{c(xtalin)}$	Frequency, fref_xtal_in	12, 16.8, 19.2, 26, or 38.4			MHz
OCS1	$t_{w(xtalin)}$	Pulse duration, fref_xtal_in low or high	$0.45 \times t_{c(XTALIN)}$		$0.55 \times t_{c(XTALIN)}$	ns
	$t_{j(xtalin)}$	Peak-to-peak jitter(1), fref_xtal_in			$1\% \times t_{c(XTALIN)}$(5) (ps) × X_{DIV}(4) — 390 (ps)	ps
	$t_{R(xtalin)}$	Rise time, fref_xtal_in			5	ns
	$t_{F(xtalin)}$	Fall time, fref_xtal_in			5	ns
	$t_{j(xtalin)}$	Frequency stability, fref_xtal_in			50 (±5)(2)	ppm

(1) Peak-to-peak jitter is meant here as follows:

—The maximum value is the difference between the longest measured clock period and the expected clock period

—The minimum value is the difference between the shortest measured clock period and the expected clock period

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(2) ±50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.

(3) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

(4) In X_{DIV}, X_{DIV} represents the internal DSS DPLLs dividers. [$t_{c(XTALIN)}$ (ps) × X_{DIV}] represents the input clock cycle coming to the DSS DPLLs (this means after dividing). For the other internal DPLLs, the X_{DIV} value is equal to 1. For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP543x TRM.

(5) $t_{c(XTALIN)}$ is the fref_xtal_in cycle time of the clock coming to fref_xtalin_in ball.

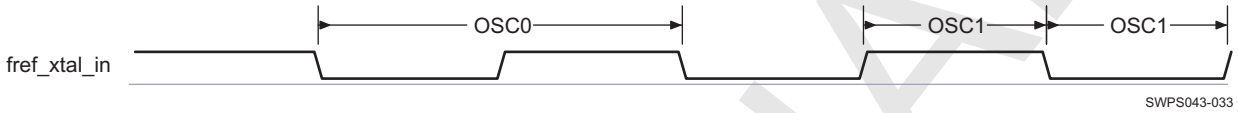


Figure 4-4. fref_xtal_in Input Square Clock

4.1.1.2.3 fref_xtal_clk Output Clock

The signal on the fref_xtal_clk output pad is a direct image of the signal on the fref_xtal_in input pad. It is available when oscillator is active or bypassed.

Table 4-8 summarizes the fref_xtal_clk output clock electrical characteristics.

Table 4-8. fref_xtal_clk Output Clock Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, fref_xtal_clk	12, 16.8, 19.2, or 26			MHz
C_L	Load capacitance (Transmission line load + Far-end load)			5	pF

Table 4-9 details the fref_xtal_clk output switching characteristics.

Table 4-9. fref_xtal_clk Output Switching Characteristics(3)

NAME		DESCRIPTION	MIN	TYP	MAX	UNIT
OCS0	1 / $t_{c(xtalclk)}$	Frequency, fref_xtal_clk	12, 16.8, 19.2, or 26			MHz
OCS1	$t_{w(xtalclk)}$	Pulse duration, fref_xtal_clk low or high	0.45 × $t_{c(XTALCLK)}$		0.55 × $t_{c(XTALCLK)}$	ns
	$t_{j(xtalclk)}$	Peak-to-peak jitter(1), fref_xtal_clk			$t_{J(XTALIN)}$(4) + 150 (ps)	ps
	$t_{R(xtalclk)}$	Rise time, fref_xtal_clk			0.5	ns
	$t_{F(xtalclk)}$	Fall time, fref_xtal_clk			0.5	ns
	$t_{j(xtalclk)}$	Frequency stability, fref_xtal_clk			50 (±5)(2)	ppm

(1) Peak-to-peak jitter is meant as follows:

—The maximum value is the difference between the longest measured clock period and the expected clock period.

—The minimum value is the difference between the shortest measured clock period and the expected clock period.

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(2) ±50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.

(3) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

(4) $t_{J(fxtal\_in)}$ corresponds to the external jitter coming to the fref_xtal_in input PAD.

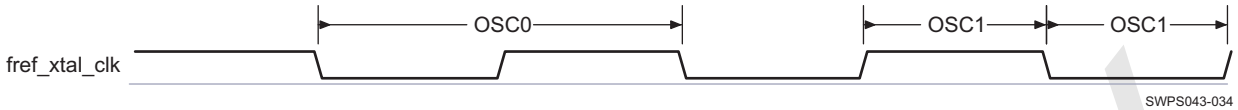


Figure 4-5. fref_xtal_clk Squarer Input Clock

4.1.1.3 fref_slicer_in Input Clock

NOTE

It is recommended to not use the slicer bypass mode. Even in case of square clock used, it is better to use the slicer active mode.

Table 4-10 summarizes the electrical characteristics of the fref_slicer_in input clock.

Table 4-10. fref_slicer_in Input Clock Electrical Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, fref_slicer_in	12, 16.8, 19.2, 26, and 38.4			MHz
C_I	Input capacitance			2.5	pF
R_I	Input resistance	14		29	kΩ

Table 4-11 details the input requirements of the fref_slicer_in input clock.

Table 4-11. fref_slicer_in Input Square Clock Timing Requirements(1)(6)

NAME	DESCRIPTION			MIN	TYP	MAX	UNIT
SLC0	$1 / t_{c(fref\_slicer\_in)}$	Frequency, fref_slicer_in		12, 16.8, 19.2, 26, and 38.4			MHz
SLC1	$t_{w(fref\_slicer\_in)}$	Pulse duration, fref_slicer_in low or high	Active mode square clock	0.45 × $t_{c(SLICER)}$		0.55 × $t_{c(SLICER)}$	ns
	$t_{j(fref\_slicer\_in)}$	Peak-to-peak jitter(2), fref_slicer_in	Active mode square clock			1% × $t_{c(SLICER)}$(4) (ps) × X_{DIV}(3)— 340 (ps)	ps
	$t_{R(fref\_slicer\_in)}$	Rise time, fref_slicer_in		1.5		10	ns
	$t_{F(fref\_slicer\_in)}$	Fall time, fref_slicer_in		1.5		10	ns
	$t_{j(fref\_slicer\_in)}$	Frequency stability, fref_slicer_in				50 (±5)(5)	ppm

(1) See Section 3.4.8, *System DC Electrical Characteristics*, SYS (clk_slicer_in) part for fref_slicer_in V_{IH} /V_{IL} parameters.

(2) Peak-to-peak jitter is meant here as follows:

—The maximum value is the difference between the longest measured clock period and the expected clock period

—The minimum value is the difference between the shortest measured clock period and the expected clock period

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(3) In X_{DIV}, X_{DIV} represents the internal DSS DPLLs dividers. [$t_{c(SLICER)}$ (ps) × X_{DIV}] represents the input clock cycle coming to the DSS DPLLs (this means after dividing). For the other internal DPLLs, the X_{DIV} value is equal to 1. For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP543x TRM.

(4) $t_{c(SLICER)}$ is the fref_slicer_in cycle time of the clock coming to fref_slicer_in ball.

(5) ±50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.

(6) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

Table 4-12. fref_slicer_in Input Single-ended Sine Clock Timing Requirements(1)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
SLC0	$1 / t_{c(fref\_slicer\_in)}$	Frequency, fref_slicer_in	12, 16.8, 19.2, 26, and 38.4			MHz

Table 4-12. fref_slicer_in Input Single-ended Sine Clock Timing Requirements(1) (continued)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
SLC1	$t_{w(fref\_slicer\_in)}$	Pulse duration, fref_slicer_in low or high	0.385 × $t_{c(SLICER)}$		0.615 × $t_{c(SLICER)}$	ns
	$t_{j(fref\_slicer\_in)}$	Peak-to-peak jitter(2), fref_slicer_in			1% × $t_{c(SLICER)}$(4) (ps) × X_{DIV}(3)— 340 (ps)	ps
	$t_{j(fref\_slicer\_in)}$	Frequency stability, fref_slicer_in			50 (±5)(5)	ppm

(1) See Section 3.4.8, *System DC Electrical Characteristics*, SYS (clk_slicer_in) part for fref_slicer_in V_{IH} /V_{IL} parameters.

(2) Peak-to-peak jitter is meant here as follows:

—The maximum value is the difference between the longest measured clock period and the expected clock period

—The minimum value is the difference between the shortest measured clock period and the expected clock period

Maximum and minimum are obtained on a statistical population of 300 period samples and expressed relative to the expected clock period.

(3) In X_{DIV}, X_{DIV} represents the internal DSS DPLLs dividers. [$t_{c(SLICER)}$ (ps) × X_{DIV}] represents the input clock cycle coming to the DSS DPLLs (this means after dividing). For the other internal DPLLs, the X_{DIV} value is equal to 1.

For more information, see the Power, Reset and Clock Management / Clock Management Functional Description / Internal Clock Sources/Generators / PRM Clock Source section of the OMAP543x TRM.

(4) $t_{c(SLICER)}$ is the fref_slicer_in cycle time of the clock coming to fref_slicer_in ball.

(5) ±50 ppm is the clock frequency stability/accuracy and ± 5 ppm takes into account the aging effects.

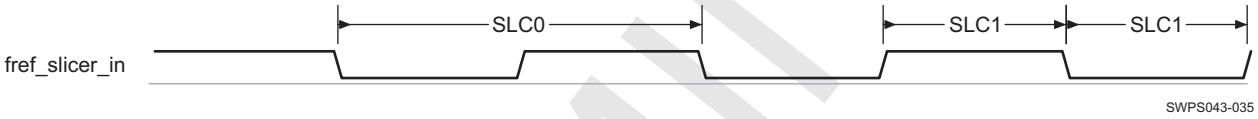


Figure 4-6. fref_slicer_in Input Clock

4.2 Output Clock Specifications

4.2.1 FREF Output Clocks

Four configurable clock output signals are available on fref_clk[3:0]_out (x = 0…3) pins. The clocks are configurable and can be managed by software and/or by hardware with the fref_clk_req[2:1] and fref_clk_ioreq (when in input direction) pins.

When fref_clk_ioreq is configured as output, the signal is used to request an external clock source for the OMAP5430 device. When configured as input (oscillator enabled), this fref_clk_ioreq pin can be used as an additional clock request fref_clk0_req to the existing fref_clk_req[2:1] signals.

Each of the output clocks can be gated or enabled independently by activation of the associated clock request signals, fref_clk[2:1]_req or fref_clk_ioreq pins.

The fref_clk_ioreq pin can be used as the fref_clk0_req signal when configured as input pin (oscillator enabled).

By default:

- The fref_clk0_req auxiliary clock request (fref_clk_ioreq as input pin) is mapped on the fref_clk0_out auxiliary clock.
- The fref_clk1_req auxiliary clock request is mapped on the fref_clk1_out auxiliary clock.
- The fref_clk2_req auxiliary clock request is mapped on the fref_clk2_out auxiliary clock.
- No auxiliary clock request is mapped on the fref_clk3_out auxiliary clock.

A re-mapping is possible to map the fref_clkx_req clock request (x = [2:0]) on the fref_clky_out clock (y = [3:0])

The polarity of fref_clk[2:1]_req and fref_clk_ioreq pins is programmable (active high by default after reset).

Input fref_clk_req2 and output fref_clk3_out signals are multiplexed on the same ball (see Table 2-2). Hence, fref_clk_req2 and fref_clk3_out are.

Output fref_clk[3:0]_out clocks come from either:

- The input system clock and alternate clock (fref_xtalin or fref_slicer_in)
- Or, a CORE clock (from DPLL_CORE output)
- Or, a 192-MHz clock (from PER DPLL output)

Each of these clocks can be divided and independently controlled by software. For more information, see the OMAP543x TRM.

fref_clk_ioreq is an open-drain output (driving a low-level when requesting clock, else output driver is in Hi-Z and line must have a pullup to maintain it inactive) or open-source (driving a high-level when requesting clock, else output driver is in Hi-Z and line must have a pulldown to maintain it inactive) for requesting the clock to an external clock source device when the system clock is not provided by the crystal oscillator

For more information, see the System Clock and Reset Manager section of the OMAP543x TRM.

Table 4-13 summarizes the electrical characteristics of the fref_clk1_out output clock (especially targeted for the primary camera sensor functional input clock), fref_clk2_out output clock (targeted for the secondary camera sensor functional input clock), and fref_clk0_out, fref_clk3_out, fref_clk4_out, and fref_clk5_out output clocks (input clocks for the other peripherals).

Table 4-13. fref_clkx_out Output Clock Electrical Characteristics(1)(2)

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f	Frequency, fref_clkx_out	fref_xtal_in(3) clock frequency, or fref_slicer_in(3) clock frequency, or DPLL_CORE(3), or DPLL_PER(3)			MHz
Drive Strength, output impedance: DS[1:0] = 01 for Z_O = 51 to 65 Ω					
Drive Strength, output impedance: DS[1:0] = 10 for Z_O = 41 to 50 Ω					
Drive Strength, output impedance: DS[1:0] = 11 for Z_O = 30 to 40 Ω					
Slew-rate Control: SC[1:0] = 10					
C_L	Load capacitance (Transmission line load + Far-end load)	5		25	pF
Z_T	Transmission line impedance	30		65	Ω
L_T	Transmission line length	1		10	cm
D_T	Transmission line delay time		67		ps

(1) In fref_clkx_out, x = 0, 1, 2, or 3.

(2) The modes are configured by 4 bits, DS[1:0] and SC[1:0], of the IO cell. For more details, see the OMAP543x TRM.

(3) A divide factor from 1 to 16 can be applied on this clock frequency.
For more information, see the SCRM.AUXCLK[0:3] register, CLKDIV bitfield in the OMAP543x TRM.

Table 4-14 details the fref_clk0_out, fref_clk1_out, fref_clk2_out, and fref_clk3_out output clock switching characteristics.

Table 4-14. fref_clkx_out Output Clock Switching Characteristics(1)(5)(7)(9)

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
	f	Frequency, fref_clkx_out	fref_xtal_in clock frequency(6), or fref_slicer_in clock frequency(6), or DPLL_CORE clock frequency(6), or DPLL_PER clock frequency(6)			MHz
FREF0	$t_{c(clkx\_out)}$	Period, fref_clkx_out	1/ f			ns

Table 4-14. fref_clkx_out Output Clock Switching Characteristics[1][5][7][9] (continued)

NAME	DESCRIPTION				MIN	TYP	MAX	UNIT
	$t_{J(clkx\_out)}$	Peak-to-peak jitter, fref_clkx_out	From fref_xtal_in CORE DPLL or PER DPLL bypassed				$t_{J(fref\_xtal\_in)} \times (1 + CLKDIV^{(6)}) + 0.400$	ns
			From fref_xtal_in CORE DPLL or PER DPLL used				$2.5\% \times t_{(dpll\_out)} \times (1 + CLKDIV^{(6)}) + 0.125$	
			From fref_slicer_in CORE DPLL or PER DPLL bypassed				$t_{J(fref\_slicer\_in)} \times (1 + CLKDIV^{(6)}) + 0.440$	
			From fref_slicer_in CORE DPLL or PER DPLL used				$2.5\% \times t_{(dpll\_out)} \times (1 + CLKDIV^{(6)}) + 0.125$	
	Stability, fref_clkx_out					50[8]		ppm
FREF1	$t_{w(clkx\_out)}$	Pulse duration, fref_clkx_out low or high	CLKDIV[6] value is even	From fref_xtal_in CORE DPLL or PER DPLL bypassed			$[0.50 \times t_{c(clkx\_out)}] + t_{J(clkx\_out)}$	ns
				From fref_xtal_in CORE DPLL or PER DPLL used			$[0.50 \times t_{c(clkx\_out)}] + t_{J(clkx\_out)}$	
				From fref_slicer_in CORE DPLL or PER DPLL bypassed			$[0.50 \times t_{c(clkx\_out)}] + t_{J(clkx\_out)}$	
				From fref_slicer_in CORE DPLL or PER DPLL used			$[0.50 \times t_{c(clkx\_out)}] + t_{J(clkx\_out)}$	
			CLKDIV[6] value is odd	From fref_xtal_in CORE DPLL or PER DPLL bypassed			$[(CLKDIV) / (2 \times CLKDIV + 2)] \times t_{c(clkx\_out)} + t_{J(clkx\_out)}$	
				From fref_xtal_in CORE DPLL or PER DPLL used			$[(CLKDIV) / (2 \times CLKDIV + 2)] \times t_{c(clkx\_out)} + t_{J(clkx\_out)}$	
				From fref_slicer_in CORE DPLL or PER DPLL bypassed			$[(CLKDIV) / (2 \times CLKDIV + 2)] \times t_{c(clkx\_out)} + t_{J(clkx\_out)}$	
				From fref_slicer_in CORE DPLL or PER DPLL used			$[(CLKDIV) / (2 \times CLKDIV + 2)] \times t_{c(clkx\_out)} + t_{J(clkx\_out)}$	
Drive Strength, output impedance: DS[1:0] = 01 for Z_O = 51 to 65 Ω								
Drive Strength, output impedance: DS[1:0] = 10 for Z_O = 41 to 50 Ω								
Drive Strength, output impedance: DS[1:0] = 11 for Z_O = 30 to 40 Ω								
Slew-rate Control: SC[1:0] = 10								
	$t_{R(clkx\_out)}$	Rise time, fref_clkx_out			0.907[2][4]		1.931[3]	ns
	$t_{F(clkx\_out)}$	Fall time, fref_clkx_out			0.910[2][4]		2.225[3]	ns

(1) In fref_clkx_out, x = 0, 1, 2, or 3

(2) At minimum load

(3) At maximum load

(4) **Caution**: this creates EMI parasitics up to 1.2 ns.

(5) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

(6) A divide factor from 1 to 16 can be applied on this clock frequency.
For more information, see the SCRM.AUXCLK[0:3] register, CLKDIV bitfield in the OMAP543x TRM.

(7) clkx_out is the external clock signal at the fref_clkx_out output pin.
dpll_out is the internal clock signal at the dpll output, before the clock divider controlled by CLKDIV.

(8) ±50 ppm is the clock frequency stability/accuracy and ±5 ppm takes into account the aging effects.

(9) $t_{J(fref\_xtal\_in)}$ or $t_{J(fref\_slicer\_in)}$ corresponds to the external jitter coming to the fref_xtal_in or fref_slicer_in input PAD.

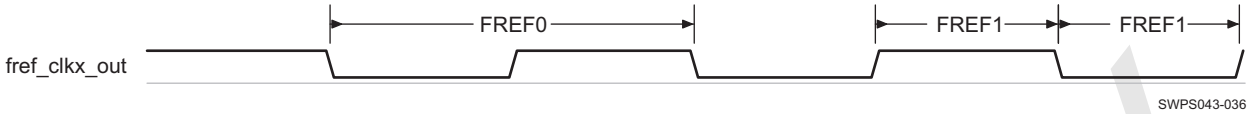


Figure 4-7. fref_clkx_out Output Clocks(1)

(1) In fref_clkx_out, x = 0, 1, 2, or 3.

4.2.2 DPLLs, DLLs Specifications

NOTE

For more information, see:

- Power, Reset and Clock Management / Clock Management Functional / Internal Clock Sources / Generators / Generic DPLL Overview Section

  and

- Display Subsystem / Display Subsystem Overview section of the OMAP543x TRM.

To generate high frequency clocks, the OMAP5430 device embeds 14 DPLLs. They all have the following common features:

- They have their own independent power domain (each one embeds its own switch and can be controlled as an independent functional power domain)
- They are fed with ALWAYS ON system clock, with independent control per DPLL
- Their analog part is supplied through dedicated power supply (1.8 V) and an embedded LDO.

The different DPLLs managed by the PRCM are listed below:

- DPLL_MPU: It supplies the MPU subsystem clocking internally.
- DPLL_IVA: It feeds the IVA and DSP subsystem clocking.
- DPLL_CORE: It supplies all interface clocks and also few module functional clocks. It generates clocks for EMIF and LPDDR2 PHYs. It can be also direct source of fref_clk[3:0]_out and emulation trace clock.
- DPLL_PER: It supplies several clock sources: a 192-MHz clock for the display functional clock and the ISS functional clock, a 96-MHz functional clock to subsystems and peripherals, fref_clk[3:0]_out and emulation trace clock.
- DPLL_ABE: This is the DPLL for the interface clock of Audio Back-End, the functional clock of ABE peripherals (McBSP1-3, and so on) and MPU, plus IVA subsystem bypass clock (this allows to clock these subsystems at ULP consumption, as only DPLL_ABE is active, DPLL_MPU and DPLL_IVA can be inactive). DPLL_ABE is optimized to produce up to 100-MHz clock from 32.768-kHz clock with a very low-power consumption.
- DPLL_USB: The USB_PHY contains one DPLL that feeds the USB_HOST_HS link, the USB_TLL_HS, and the USB2PHY module.

NOTE

The following DPLLs are controlled by the clock manager located in the always-on Core power domain (CM_CORE_AON):

- DPLL_MPU, DPLL_IVA, DPLL_CORE, and DPLL_ABE.

And the following DPLLs are managed by the clock manager in the Core power domain (CM_CORE):

- DPLL_PER and DPLL_USB.

For more information on CM_CORE_AON and CM_CORE or PRCM DPLLs, see the Power Reset Controller Manager (PRCM) chapter of the OMAP543x TRM.

The following DPLLs are not managed by the PRCM:

- DPLL_USB_OTG_SS: The USB SS DRD controller manages this DPLL. It supplies the functional clock of the USB SS DRD and associated PHYs.
- DPLL_SATA: The SATA PHY controller manages this DPLL. It supplies the functional clock of the SATA module and the PHYs.
- DPLL_DSI1_A, DPLL_DSI1_C and DPLL_HDMI: The display subsystem contains three DPLLs, which are directly managed by this subsystem. For more information, see the DSS (DSI, HDMI) section of the OMAP543x TRM.
- DPLL_DEBUGSS: The DEBUGSS manages this DPLL. It supplies the functional clock of the debug subsystem.

4.2.2.1 DPLL Characteristics

The DPLL has three relevant input clocks. One of them is the reference clock (CLKINP) used to generated the synthesized clock but can also be used as the bypass clock whenever the DPLL enters a bypass mode. It is therefore mandatory. The second one is a fast bypass clock (CLKINPULOW) used when selected as the bypass clock and is optional. The third clock (CLKINPHIF) is explained in the next paragraph.

The DPLL has three output clocks (namely CLKOUT, CLKOUTX2, and CLKOUTHIF). CLKOUT and CLKOUTX2 run at the bypass frequency whenever the DPLL enters a bypass mode. Both of them are generated from the lock frequency divided by a post-divider (namely M2 post-divider). The third clock, CLKOUTHIF, has no automatic bypass capability. It is an output of a post-divider (M3 post-divider) with the input clock selectable between the internal lock clock (Fdpll) and CLKINPHIF input of the PLL through an asynchronous multplexing.

For more information, see the Power Reset Controller Management chapter of the OMAP543x TRM.

Table 4-15 summarizes DPLL type described in Section 4.2.2, *DPLLs, DLLs Specifications* introduction.

Table 4-15. DPLL Control Type

DPLL NAME	TYPE	CONTROLLED BY PRCM
DPLL_ABE	Table 4-16 (Type A)	Yes(1)
DPLL_CORE	Table 4-16 (Type A)	Yes(1)
DPLL_DSI1_A	Table 4-16 (Type A)	No(2)
DPLL_DSI1_C	Table 4-16 (Type A)	No(2)
DPLL_HDMI	Table 4-17 (Type B)	No(2)
DPLL_PER	Table 4-16 (Type A)	Yes(1)
DPLL_SATA	Table 4-17 (Type B)	No(2)
DPLL_USB	Table 4-17 (Type B)	Yes
DPLL_USB_OTG_SS	Table 4-17 (Type B)	No(2)
DPLL_DEBUGSS	Table 4-16 (Type A)	No(2)
DPLL_IVA	Table 4-16 (Type A)	Yes(1)
DPLL_MPU	Table 4-16 (Type A)	Yes(1)

(1) DPLL is in the always-on domain.

(2) DPLL is not controlled by the PRCM.

Table 4-16 and Table 4-17 summarize the DPLL characteristics and assume testing over recommended operating conditions.

Table 4-16. DPLL_CORE / DPLL_PER / DPLL_MPU / DPLL_IVA / DPLL_ABE / DPLL_DEBUGSS / DPLL_DSI1_A / DPLL_DSI1_C Characteristics—Type A

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
vdda_dpll_mpu	Supply voltage for DPLL MPU	1.71	1.80	1.89	V	
vdda_dpll_mm_l4per	Supply voltage for DPLL IVA	1.71	1.80	1.89	V	
vdda_dpll_core_emu_abe	Supply voltage for DPLL CORE	1.71	1.80	1.89	V	
vdda_dpll_mm_l4per	Supply voltage for DPLL PER	1.71	1.80	1.89	V	
vdda_dpll_core_emu_abe	Supply voltage for DPLL ABE	1.71	1.80	1.89	V	
vdda_dsiportA	Supply voltage for DPLL DSI Port A , DSI1_A	1.71	1.80	1.89	V	
vdda_dsiportC	Supply voltage for DPLL DSI Port C, DSI1_C	1.71	1.80	1.89	V	
vdda_dpll_core_emu_abe	Supply voltage for DPLL DEBUGSS	1.71	1.80	1.89	V	
f_{input}	CLKINP input frequency	0.032		52	MHz	F_{INP}
$f_{internal}$	Internal reference frequency	0.032		52	MHz	REFCLK
$f_{CLKINPHIF}$	CLKINPHIF input frequency	20		1400	MHz	F_{INPHIF}
$f_{CLKINPULOW}$	CLKINPULOW input frequency	0.001		600	MHz	Bypass mode: f_{CLKOUT} = $f_{CLKINPULOW}$ / (M1 + 1) if ulowclken = 1[6]
f_{CLKOUT}	CLKOUT output frequency	20[1]		1400[2]	MHz	[M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKOUTx2}$	CLKOUTx2 output frequency	40[1]		2800[2]	MHz	2 × [M / (N + 1)] × F_{INP} × [1 / M2] (in locked condition)
$f_{CLKOUTHIF}$	CLKOUTHIF output frequency	20[3]		1400[4]	MHz	F_{INPHIF} / M3 if clkinphifsel = 1
		40[3]		2800[4]		2 × [M / (N + 1)] × F_{INP} × [1 / M3] if if clkinphifsel = 0
$f_{CLKDCOLDO}$	DCOCLKLDO output frequency	40		2400	MHz	2 × [M / (N + 1)] × F_{INP} (in locked condition)
t_{lock}	Frequency lock time			5 + 350 × REFCLK	µs	
p_{lock}	Phase lock time			5 + 500 × REFCLK	µs	
$t_{relock-L}$	Relock time—Frequency lock[5] (LP relock time from bypass)			5 + 70 × REFCLK	µs	DPLL in LP relock time: lowcurrstdby = 1
$p_{relock-L}$	Relock time—Phase lock[5] (LP relock time from bypass)			5 + 120 × REFCLK	µs	DPLL in LP relock time: lowcurrstdby = 1
$t_{relock-F}$	Relock time—Frequency lock[5] (fast relock time from bypass)			2.55 + 70 × REFCLK	µs	DPLL in fast relock time: lowcurrstdby = 0
$p_{relock-F}$	Relock time—Phase lock[5] (fast relock time from bypass)			2.55 + 120 × REFCLK	µs	DPLL in fast relock time: lowcurrstdby = 0

(1) The minimum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

For M2 > 1, the minimum frequency on these clocks will further scale down by factor of M2.

(2) The maximum frequencies on CLKOUT and CLKOUTX2 are assuming M2 = 1.

(3) The minimum frequency on CLKOUTHIF is assuming M3 = 1. For M3 > 1, the minimum frequency on this clock will further scale down by factor of M3.

(4) The maximum frequency on CLKOUTHIF is assuming M3 = 1.

(5) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(6) Bypass mode: f_{CLKOUT} = F_{INP} if ulowclken = 0. For more information, see the OMAP543x TRM.

Table 4-17. DPLL_USB / DPLL_USB_OTG_SS / DPLL_SATA / DPLL_HDMI Characteristics—Type B

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT	COMMENTS
vdds_usbhs18	Supply voltage for DPLL USB	1.71	1.80	1.89	V	
vdda_dpll_hdmi	Supply voltage for DPLL HDMI	1.71	1.80	1.89	V	
vdda_usbss18	Supply voltage for DPLL USB SS	1.71	1.80	1.89	V	
vdda_sata	Supply voltage for DPLL SATA	1.71	1.80	1.89	V	
f_{input}	CLKINP input clock frequency	0.62		60	MHz	F_{INP}
$f_{internal}$	REFCLK internal reference clock frequency	0.62		2.5	MHz	$[1 / (N + 1)] \times F_{INP}$
$f_{CLKINPULOW}$	CLKINPULOW bypass input clock frequency	0.001		600	MHz	Bypass mode: $f_{CLKOUT} = f_{CLKINPULOW} / (M1 + 1)$ If ulowclken = 1(4)
$f_{CLKLDOOUT}$	CLKOUTLDO output clock frequency	750(1)(5)		1500(2)(5)	MHz	$M / (N + 1)] \times F_{INP} \times [1 / M2]$ (in locked condition)
		1250(1)(5)		2500(2)(5)	MHz	
f_{CLKOUT}	CLKOUT output clock frequency	750(1)(5)	15	00(2)(5)	MHz	$[M / (N + 1)] \times F_{INP} \times [1 / M2]$ (in locked condition)
		1250(1)(5)		2500(2)(5)	MHz	
$f_{CLKDCOLDO}$	Internal oscillator (DCO) output clock frequency	750(5)		1500(5)	MHz	$[M / (N + 1)] \times F_{INP}$ (in locked condition)
		1250(5)		2500(5)		
t_J	CLKOUTLDO period jitter	–2.5%		2.5%		The period jitter at the output clocks is ± 2.5% peak to peak
	CLKOUT period jitter					
	CLKDCOLDO period jitter					
t_{lock}	Frequency lock time			350 × REFCLKs	µs	
p_{lock}	Phase lock time			500 × REFCLKs	µs	
$t_{relock-L}$	Relock time—Frequency lock(3) (LP relock time from bypass)			9 + 30 × REFCLKs	µs	
$p_{relock-L}$	Relock time—Phase lock(3) (LP relock time from bypass)			9 + 125 × REFCLKs	µs	

(1) The minimum frequency on CLKOUT is assuming M2 = 1.

For M2 > 1, the minimum frequency on this clock will further scale down by factor of M2.

(2) The maximum frequency on CLKOUT is assuming M2 = 1.

(3) Relock time assumes typical operating conditions, 10°C maximum temperature drift.

(4) Bypass mode: $f_{CLKOUT} = F_{INP}$ if ULOWCLKEN = 0. For more information, see the OMAP543x TRM.

(5) For output clocks, there are two frequency ranges according to the SELFREQDCO setting. For more information, see the OMAP543x TRM.

4.2.2.2 DLL Characteristics

Table 4-18 summarizes the DLL characteristics and assumes testing over recommended operating conditions.

Table 4-18. DLL Characteristics

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
vdd_core	LPDDR21 power supply providing clocks to bytes 0 and 2		See (1)		V
vdd_core	LPDDR21 power supply providing clocks to bytes 1 and 3		See (1)		V
vdd_core	LPDDR22 power supply providing clocks to bytes 0 and 2		See (1)		V
vdd_core	LPDDR22 power supply providing clocks to bytes 1 and 3		See (1)		V
f_{input}	Input clock frequency			266	MHz
t_{lock}	Lock time			TBD	cycles
t_{relock}	Relock time (a change of the DLL frequency implies that DLL must relock)			TBD	cycles

(1) See the operating condition addendum for values. OPP voltage values may change following the silicon characterization result.

4.2.2.3 DPLL and DLL Noise Isolation

NOTE

For more information on DPLL and DLL decoupling capacitor requirements, see the External Capacitors / Voltage Decoupling Capacitors / I/O and Analog Voltage Decoupling / VDDA Power Domain section.

4.2.3 Internal 32-kHz Oscillator

An internal 32-kHz oscillator is implemented in the wake-up domain. Table 4-19 gives the internal 32-kHz oscillator characteristics.

Table 4-19. Internal 32-kHz Oscillator Characteristic

PARAMETER	MIN	TYP	MAX	UNIT
Internal 32-kHz oscillator frequency	16	32	60	kHz

5 Timing Requirements and Switching Characteristics

NOTE

The OPP (operating performance point) described in this chapter correspond to the OPP of the core domain. The operating point for MPU and multimedia are not described in this section. For more information, see the DM Operating Condition addendum.

5.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions unless otherwise specified.

5.2 Interface Clock Specifications

5.2.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and/or to control transfers accordingly with the interface protocol.

5.2.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the device IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and the device IC timing characteristics as well to define properly the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

5.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology will be used to identify this type of jitter.

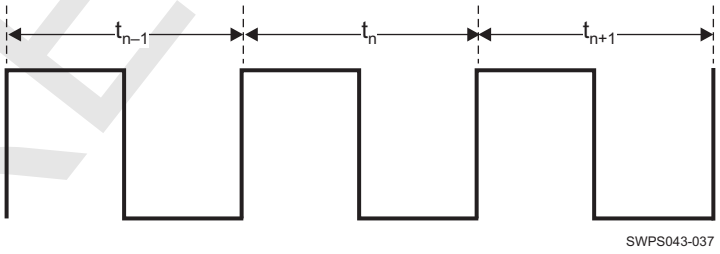


Figure 5-1. Cycle (or Period) Jitter

Jitter values are defined as follows:

- Ideal clock period = t_p
- Maximum Cycle or Period Jitter = Max ($|t_i — t_p|$), with i = n—1, n, n + 1, …
- Minimum Cycle or Period Jitter = Min ($|t_i — t_p|$)
- Jitter Standard Deviation (or RMS Jitter) = Standard Deviation ($|t_i — t_p|$)

Unless otherwise specified, the jitter probability density can be approximated by a Gaussian function and peak-to-peak jitter is defined over a ±7 sigma distribution of this function.

5.2.4 Clock Duty Cycle Error

The maximum duty cycle error is the difference between the absolute value of the maximum high-level pulse duration or the maximum low-level pulse duration and the typical pulse duration value:

- Maximum pulse duration = typical pulse duration + maximum duty cycle error
- Minimum pulse duration = typical pulse duration—maximum duty cycle error

In this document, the clock duty cycle can be documented as maximum pulse duration or as maximum duty cycle error. In this case, you can consider:

- Maximum duty cycle error = maximum [(maximum pulse duration—typical pulse duration) or (typical pulse duration —minimum pulse duration)]

5.3 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of pin names and other related terminologies have been abbreviated as follows:

Table 5-1. Timing Parameters

SUBSCRIPTS	
SYMBOL	**PARAMETER**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

NOTE

The OPP (operating performance point) described in this chapter correspond to the OPP of the core domain. The operating point for MPU and multimedia are not described in this section. For more information, see the DM Operating Condition addendum.

5.4 External Memory Interface

The OMAP5430 device includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- External memory interface controller (EMIF)

5.4.1 General-Purpose Memory Controller (GPMC), 1.8 V

NOTE

For more information, see the Memory Subsystem and General-Purpose Memory Controller sections of the OMAP543x TRM.

The GPMC is the OMAP-unified memory controller that interfaces the following types of external memory devices:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous, synchronous burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

5.4.1.1 NOR Flash, 1.8 V

5.4.1.1.1 NOR Flash, Read synchronous mode, 88.6 MHz

Table 5-2. NOR Flash Timing Conditions — Read Synchronous Mode

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.30	1.79	ns
t_F	Input signal fall time	0.33	1.84	ps
PCB Conditions(1)				

(1) See Table 8-2.

Table 5-3 and Table 5-4 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-3. NOR Flash Timing Requirements — Read Synchronous Mode(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
F12	$t_{SU(dV-clkH)}$	Setup time, input data gpmc_ad[15:0] valid before output gpmc_clk high	2.4		ns
F13	$t_{H(clkH-dV)}$	Hold time, input data gpmc_ad[15:0] valid after output gpmc_clk high	1.1		ns
F21	$t_{SU(waitV-clkH)}$	Setup time, input wait gpmc_waitx(1) valid before output gpmc_clk high	2.4		ns
F22	$t_{H(clkH-waitV)}$	Hold time, input wait gpmc_waitx(1) valid after output gpmc_clk high	1.1		ns

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-4. NOR Flash Switching Characteristics — Read Synchronous Mode(15)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
F0	1 / $t_{C(CLK)}$	Frequency(12), output gpmc_clk		88.6	MHz
F1	$t_{W(CLKH)}$	Typical Pulse duration, output gpmc_clk high	0.5 P(10)		ns
F1	$t_{W(CLKL)}$	Typical Pulse duration, output gpmc_clk low	0.5 P(10)		ns

Table 5-4. NOR Flash Switching Characteristics — Read Synchronous Mode[15] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$t_{DC(CLK)}$	Duty cycle error, output gpmc_clk		565	ps
	$t_{J(CLK)}$	Jitter standard deviation[13], output gpmc_clk		73.1	ps
	$t_{R(CLK)}$	Rise time, output gpmc_clk	0.5	1.1	ns
	$t_{F(CLK)}$	Fall time, output gpmc_clk	0.5	1.1	ns
	$t_{R(DO)}$	Rise time, output data gpmc_ad[15:0]	0.5	1.4	ns
	$t_{F(DO)}$	Fall time, output data gpmc_ad[15:0]	0.5	1.4	ns
F2	$t_{D(CLKH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx[9] valid	F[6] – 0.8	F[6] + 3.1	ns
F3	$t_{D(CLKH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx[9] invalid	E[5] – 0.8	E[5] + 3.1	ns
F4	$t_{D(ADDV-CLK)}$	Delay time, gpmc_a[25:16] address bus valid to gpmc_clk first edge	B[2] – 3.1	B[2] + 0.8	ns
F5	$t_{D(CLKH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[25:16] gpmc address bus invalid	-0.8		ns
F8	$t_{D(CLKH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale valid	G[7] – 0.8	G[7] + 3.1	ns
F9	$t_{D(CLKH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid	D[4] – 0.8	D[4] + 3.1	ns
F10	$t_{D(CLKH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe valid	H[8] – 0.8	H[8] + 2.1	ns
F11	$t_{D(CLKH-nOEIV)}$	Delay time, gpmc rising edge to gpmc_noe invalid	E[5] – 0.8	E[5] + 2.1	ns
F18	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx[9] low	A[1]		ns
F19	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	C[3]		ns
F20	$t_{W(nADVV)}$	Pulse duration, gpmc_nadv_ale low	K[11]		ns
F23	$t_{D(CLKH-IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)	H[8] – 0.8	H[8] + 2.1	ns
F24	$t_{D(CLKH-IODIRIV)}$	Delay time, gpmc rising edge to gpmc_io_dir low (OUT direction)	M[14] – 0.8	M[14] + 2.1	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK period.
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period with n the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK with n the page burst access number.

(4) For single read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(5) For single read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0:
F = 0.5 × CSExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
F = 0.5 × CSExtraDelay × GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
F = 0.5 × CSExtraDelay × GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV desactivated) in Reading mode:
Case GpmcFCLKDivider = 0:

G = 0.5 × ADVExtraDelay × GPMC_FCLK Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
Case GpmcFCLKDivider = 0:
H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
For OE rising edge (OE desactivated):
Case GpmcFCLKDivider = 0:
H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(9) In “gpmc_ncsx”, x is equal to 0, 1, 2, 3, 4, 5, 6, 7. In “gpmc_waitx”, x is equal to 0, 1, 2, or 3

(10) P = gpmc_clk period

(11) For read: K = (ADVRdOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(12) Related to the gpmc_clk output clock Maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(13) The jitter probability density can be approximated by a Gaussian function.

(14) M = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK Above M parameter expression is given as one example of GPMC programmation. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automactically handled by GPMC controller

(15) See the Data Manual Operating Condition Addendum for CORE OPP voltages.

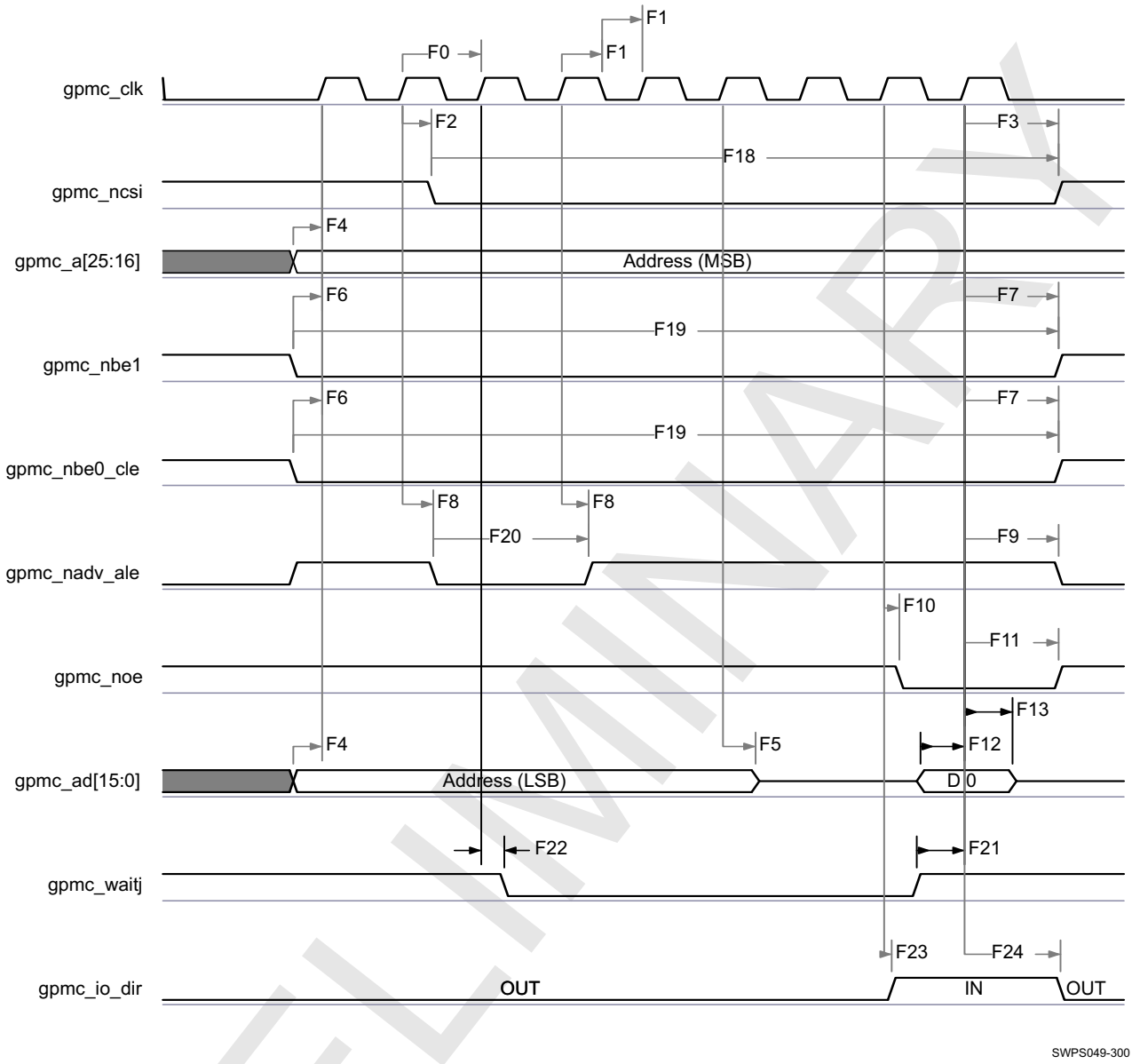


Figure 5-2. GPMC / Multiplexed 16bits NOR Flash – Synchronous Single Read(1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

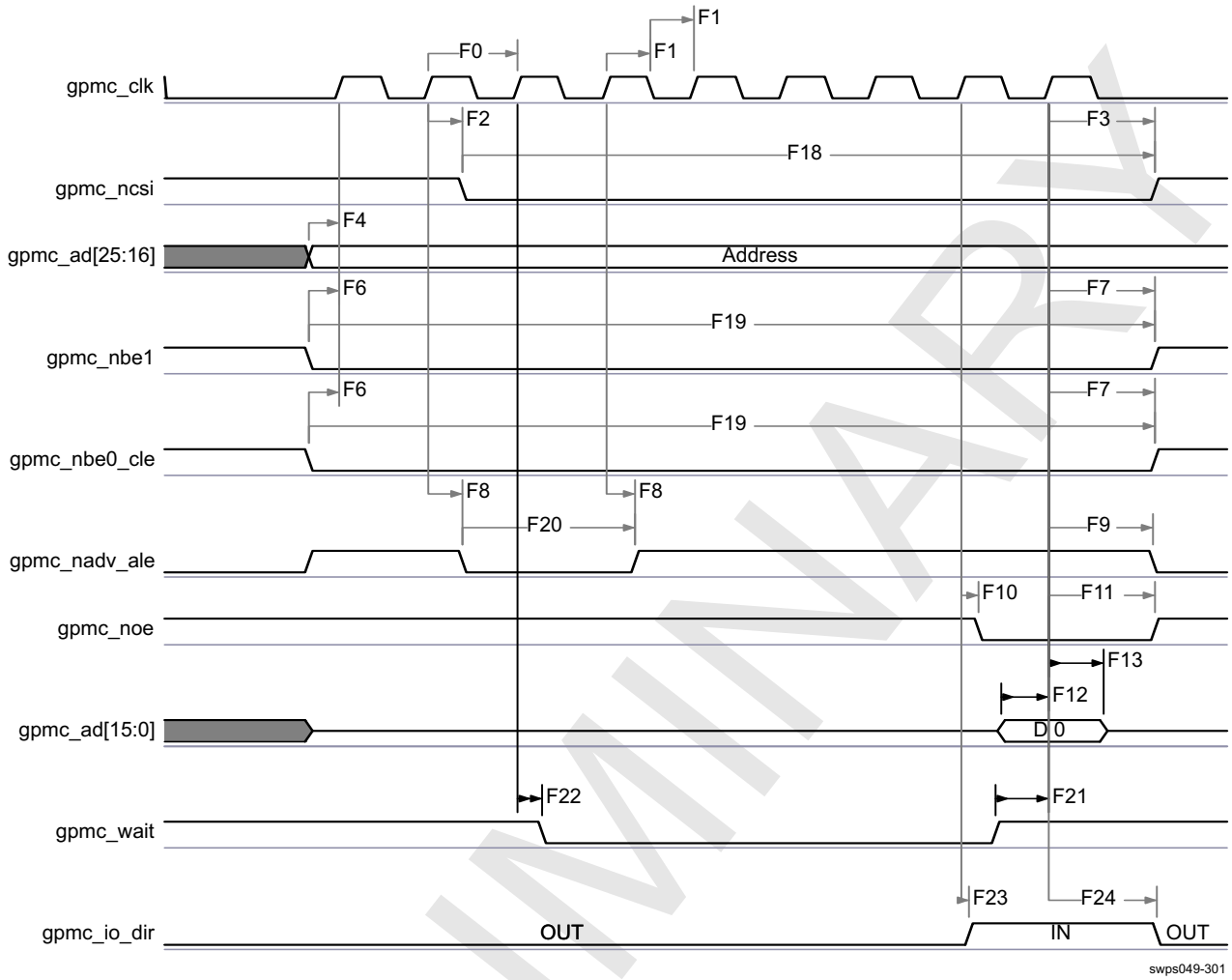


Figure 5-3. GPMC / Non-Multiplexed 16bits NOR Flash – Synchronous Single Read(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

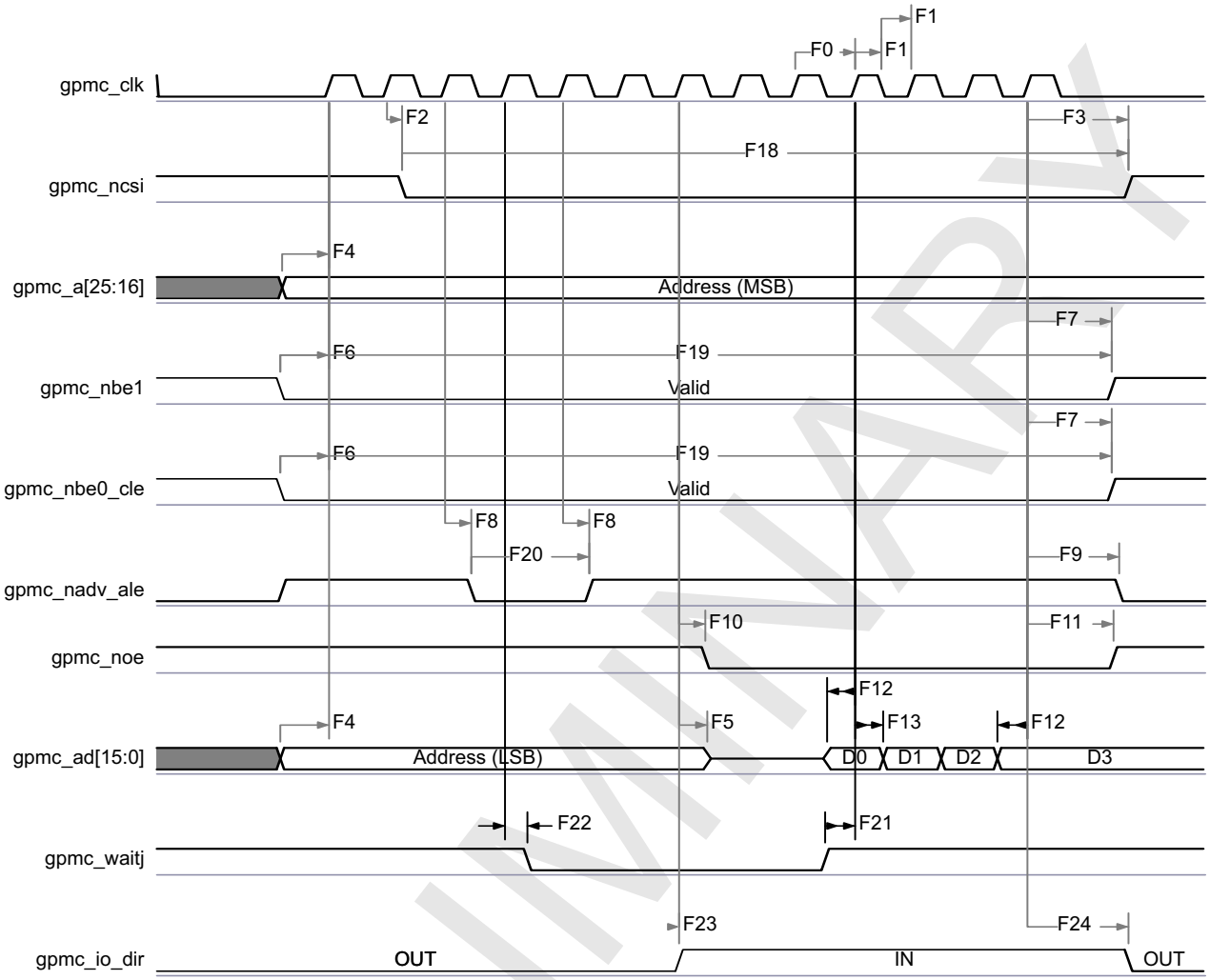


Figure 5-4. GPMC / Multiplexed 16bits NOR Flash – Synchronous Burst Read 4×16 Bits[(1)(2)]

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

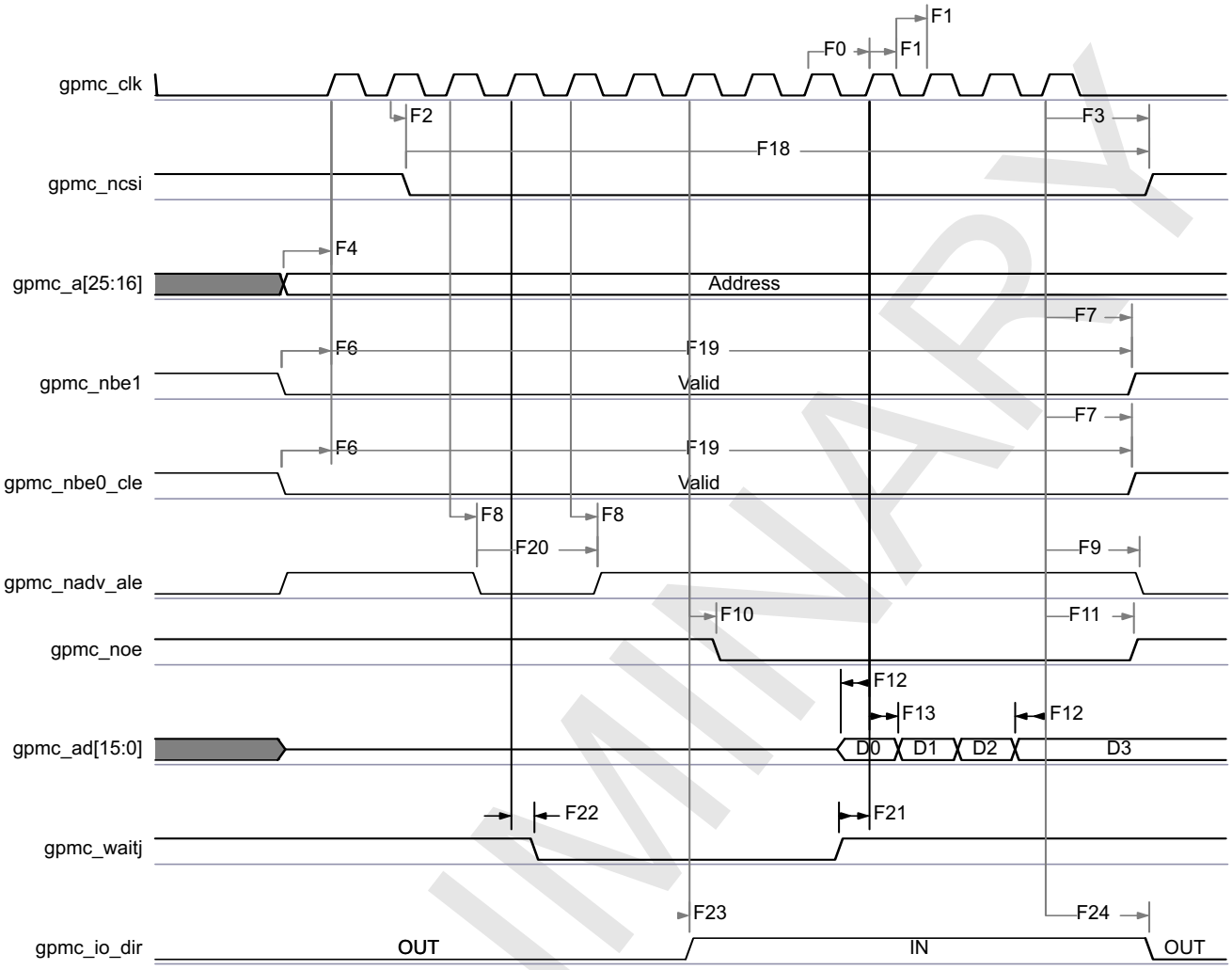


Figure 5-5. GPMC / Non-Multiplexed 16bits NOR Flash – Synchronous Burst Read 4×16 Bits(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

5.4.1.1.2 NOR Flash, Write Asynchronous Mode

Table 5-5 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-5. NOR Flash Switching Characteristics — Write Asynchronous Mode(9)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FA0	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 valid time	N(1)		ns
FA1	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx low	A(2)		ns
FA3	$t_{D(nCSV-nADVIV)}$	Delay time, gpmc_ncsx(8) valid to gpmc_nadv_ale invalid	B(3) – 0.2	B(3) + 2	ns
FA9	$t_{D(AV-nCSV)}$	Delay time, address bus valid to gpmc_ncsx(8) valid	J(4) – 0.2	J(4) + 2	ns
FA10	$t_{D(nBEV-nCSV)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_ncsx(8) valid	J(4) – 0.2	J(4) + 2	ns
FA12	$t_{D(nCSV-nADVV)}$	Delay time, gpmc_ncsx(8) valid to gpmc_nadv_ale valid	K(5) – 0.2	K(5) + 2	ns
FA25	$t_{D(nCSV-nWEV)}$	Delay time, gpmc_ncsx(8) valid to gpmc_nwe valid	E(6) – 0.2	E(6) + 2	ns

Table 5-5. NOR Flash Switching Characteristics — Write Asynchronous Mode[9] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FA27	$t_{D(nCSV-nWEIV)}$	Delay time, gpmc_ncsx[8] valid to gpmc_nwe invalid	F[7] - 0.2	F[7] + 2	ns
FA28	$t_{D(nWEV-DV)}$	Delay time, gpmc_ nwe valid to data bus valid		2.0	ns
FA29	$t_{D(DV-nCSV)}$	Delay time, data bus valid to gpmc_ncsx[8] valid	J[4] – 0.2	J[4] + 2	ns
	$t_{R(DO)}$	Rise time, output data gpmc_ad[15:0]		1.4	ns
	$t_{F(DO)}$	Fall time, output data gpmc_ad[15:0]		1.4	ns

(1) N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK

(2) A = (CSWrOffTime – CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK

(3) B = ((ADVWrOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK

(4) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK

(5) K = ((ADVOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay – CSExtraDelay)) × GPMC_FCLK

(6) E = ((WEOnTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK

(7) F = ((WEOffTime – CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay – CSExtraDelay)) × GPMC_FCLK

(8) In “gpmc_ncsx”, x is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(9) See DM Operating Condition Addendum for CORE OPP voltages.

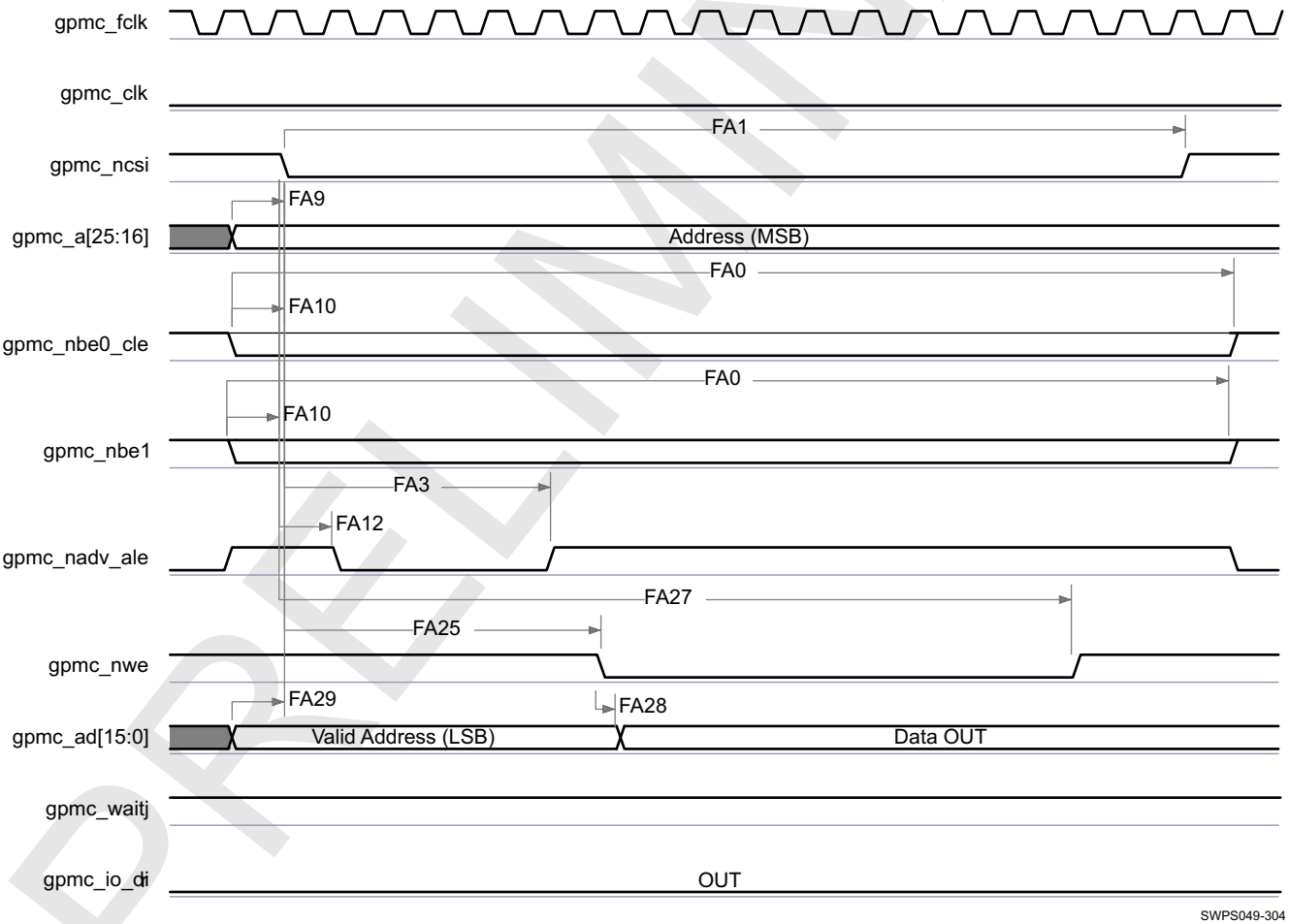


Figure 5-6. GPMC / Multiplexed 16bits NOR Flash – Asynchronous Single Write[1][2]

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

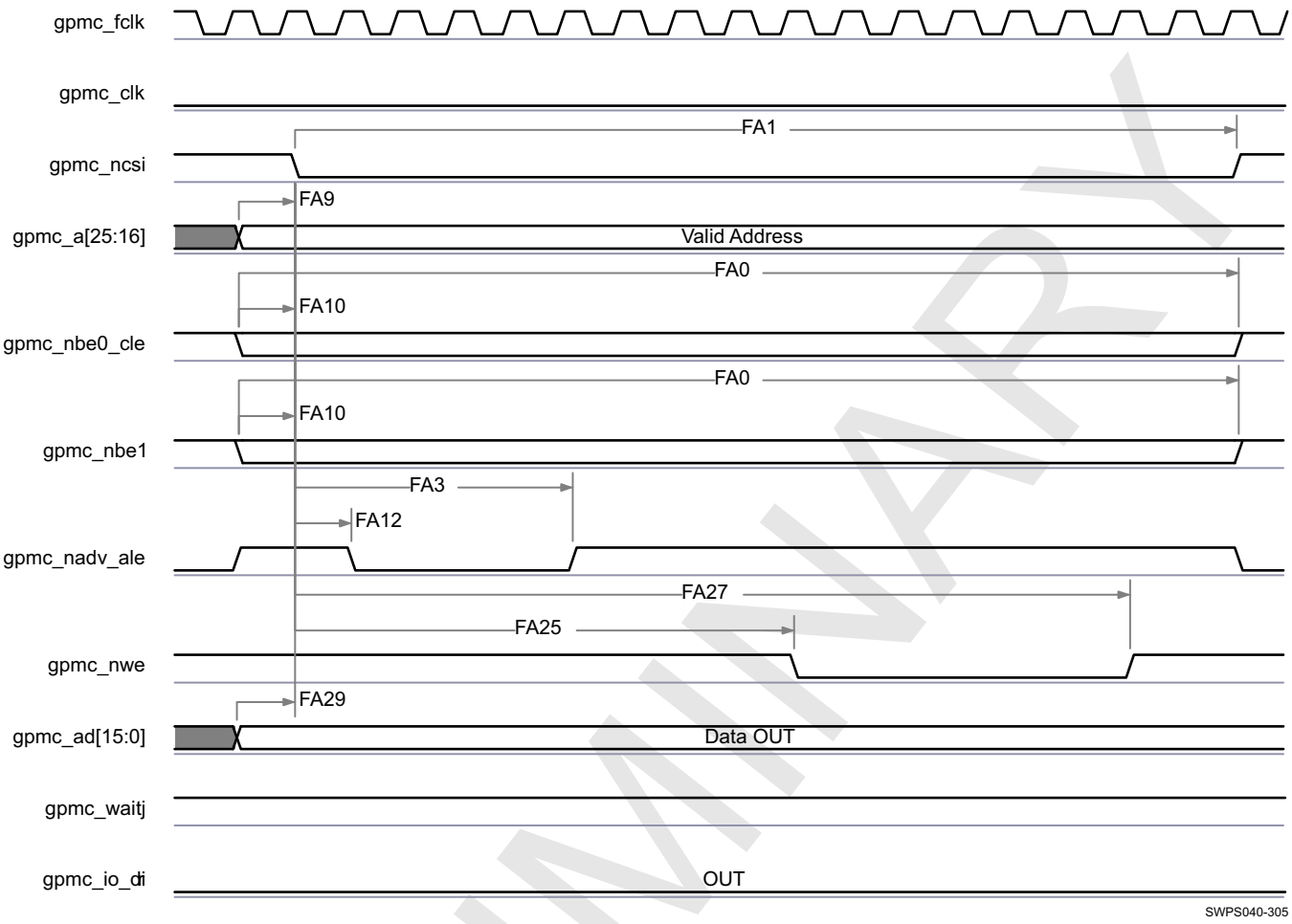


Figure 5-7. GPMC / Non-Multiplexed 16bits NOR Flash – Asynchronous Single Write(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

5.4.1.2 NAND, Synchronous mode, 66.5 MHz, 1.8 V

Table 5-6. NAND Timing Conditions — Synchronous mode

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	2.03	5.49	ns
t_F	Input signal fall time	1.38	6.09	ns
PCB Conditions(1)				

(1) See Table 8-2.

Table 5-7 and Table 5-8 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-7. NAND Timing Requirements —Synchronous Mode(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
F12	$t_{SU(dV-clkH)}$	Setup time, input data gpmc_ad[15:0] valid before output gpmc_clk high	2.5		ns
F13	$t_{H(clkH-dV)}$	Hold time, input data gpmc_ad[15:0] valid after output gpmc_clk high	1.9		ns
F21	$t_{SU(waitV-clkH)}$	Setup time, input wait gpmc_waitx(1) valid before output gpmc_clk high	2.5		ns
F22	$t_{H(clkH-waitV)}$	Hold time, input wait gpmc_waitx(1) valid after output gpmc_clk high	1.9		ns

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-8. NAND Switching Characteristics — Synchronous Mode(17)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
F0	$1 / t_{C(CLK)}$	Frequency(14), output gpmc_clk			66.5	MHz
F1	$t_{W(CLKH)}$	Typical Pulse duration, output gpmc_clk high		0.5 P(12)		ns
F1	$t_{W(CLKL)}$	Typical Pulse duration, output gpmc_clk low		0.5 P(12)		ns
	$t_{DC(CLK)}$	Duty cycle error, output gpmc_clk			752	ps
	$t_{J(CLK)}$	Jitter standard deviation(15), output gpmc_clk			97.3	ps
	$t_{R(CLK)}$	Rise time, output gpmc_clk		0.9	1.8	ns
	$t_{F(CLK)}$	Fall time, output gpmc_clk		0.9	1.6	ns
	$t_{R(DO)}$	Rise time, output data gpmc_ad[15:0]		0.9	1.8	ns
	$t_{F(DO)}$	Fall time, output data gpmc_ad[15:0]		0.9	1.6	ns
F2	$t_{D(CLKH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(11) valid		F(6) + 0.6	F(6) + 6.1	ns
F3	$t_{D(CLKH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(11) invalid		E(5) + 0.6	E(5) + 6.1	ns
F4	$t_{D(ADDV-CLK)}$	Delay time, gpmc_a[25:16] address bus valid to gpmc_clk first edge		B(2) – 6.1	B(2) – 0.7	ns
F5	$t_{D(CLKH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[25:16] gpmc address bus invalid		0.7		ns
F6	$t_{D(nBEV-CLK)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge		B(2) – 4.9	B(2) + 0.4	ns
F7	$t_{D(CLKH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid		D(4) – 0.4	D(4) + 4.9	ns
F8	$t_{D(CLKH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale valid		G(7) + 0.6	G(7) + 6.1	ns
F9	$t_{D(CLKH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid		D(4) + 0.6	D(4) + 6.1	ns
F10	$t_{D(CLKH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe valid		H(8) + 0.3	H(8) + 5.1	ns
F11	$t_{D(CLKH-nOEIV)}$	Delay time, gpmc rising edge to gpmc_noe invalid		E(5) + 0.3	E(5) + 5.1	ns
F14	$t_{D(CLKH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_nwe transition		I(9) + 0.6	I(9) + 6.1	ns
F15	$t_{D(CLKH-Data)}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition		J(10) – 0.4	J(10) + 4.9	ns
F17	$t_{D(CLKH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 transition		J(10) – 0.4	J(10) + 4.9	ns
F18	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx(11) low	Read	A(1)		ns
			Write	A(1)		ns
F19	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	Read	C(3)		ns
			Write	C(3)		ns
F20	$t_{W(nADVV)}$	Pulse duration, gpmc_nadv_ale low	Read	K(13)		ns
			Write	K(13)		ns
F23	$t_{D(CLKH-IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)		H(8) + 0.7	H(8) + 5.1	ns

Table 5-8. NAND Switching Characteristics — Synchronous Mode[17] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
F24	$t_{D(CLKH-IODIRIV)}$	Delay time, gpmc rising edge to gpmc_io_dir low (OUT direction)	M[16] + 0.7	M[16] + 5.1	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK period.
For burst read: A = (CSRdOffTime - CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period with n the page burst access number.
For burst write: A = (CSWrOffTime - CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period with n the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK with n the page burst access number.
For Burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

(4) For single read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) For single read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0:
F = 0.5 × CSExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
F = 0.5 × CSExtraDelay × GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
F = 0.5 × CSExtraDelay × GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV desactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV desactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
Case GpmcFCLKDivider = 0:
H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
For OE rising edge (OE desactivated):
Case GpmcFCLKDivider = 0:
H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(9) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)
For WE rising edge (WE desactivated):
Case GpmcFCLKDivider = 0:
I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period

(11) In “gpmc_ncsx”, x is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(12) P = gpmc_clk period

(13) For read: K = (ADVRdOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) Related to the gpmc_clk output clock Maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(15) The jitter probability density can be approximated by a Gaussian function.

(16) M = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
Above M parameter expression is given as one example of GPMC programmation. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automactically handled by GPMC controller

(17) See the Data Manual Operating Condition Addendum for CORE OPP voltages.

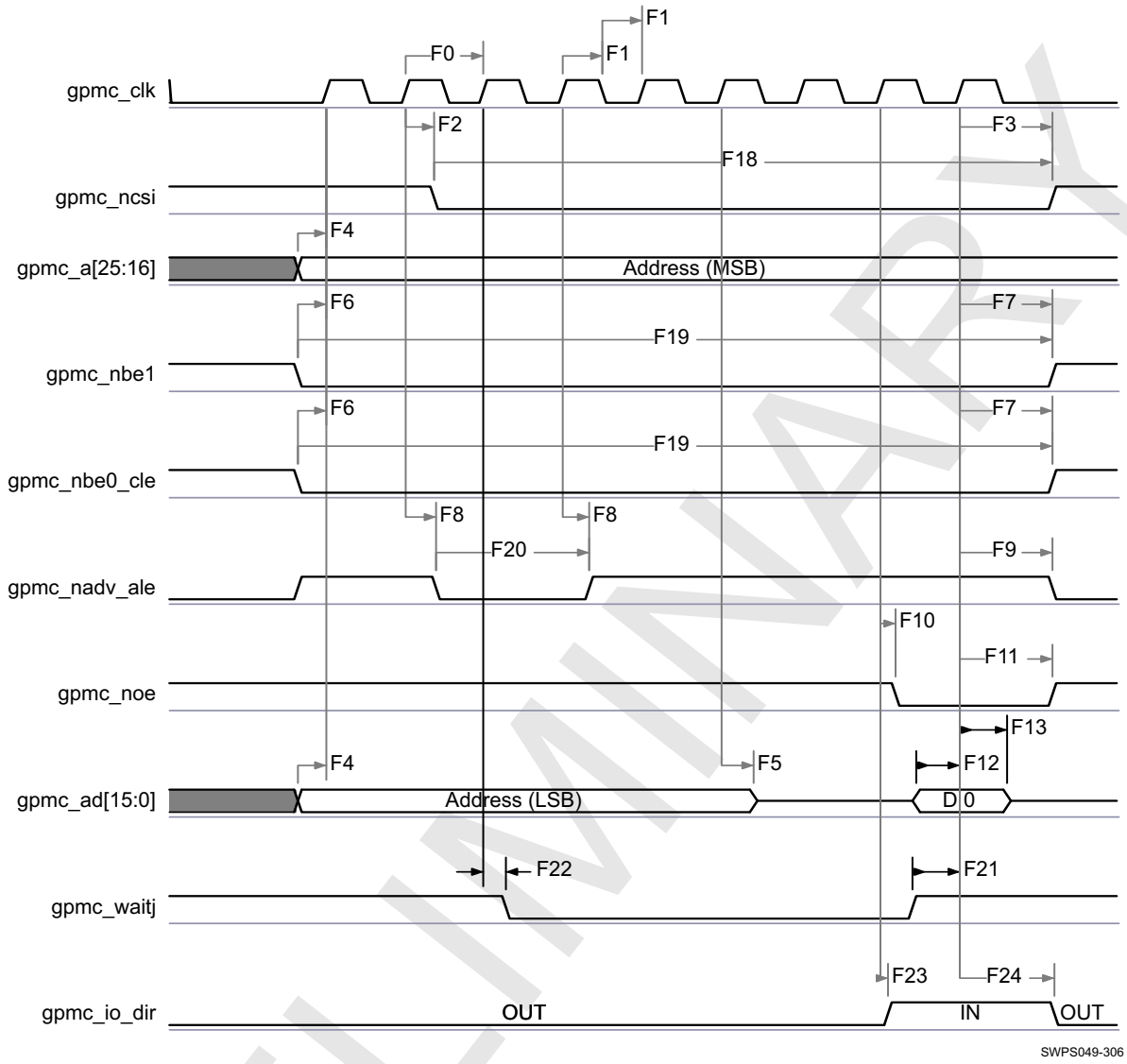


Figure 5-8. GPMC / Multiplexed 16bits NAND – Synchronous Single Read (1) (2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

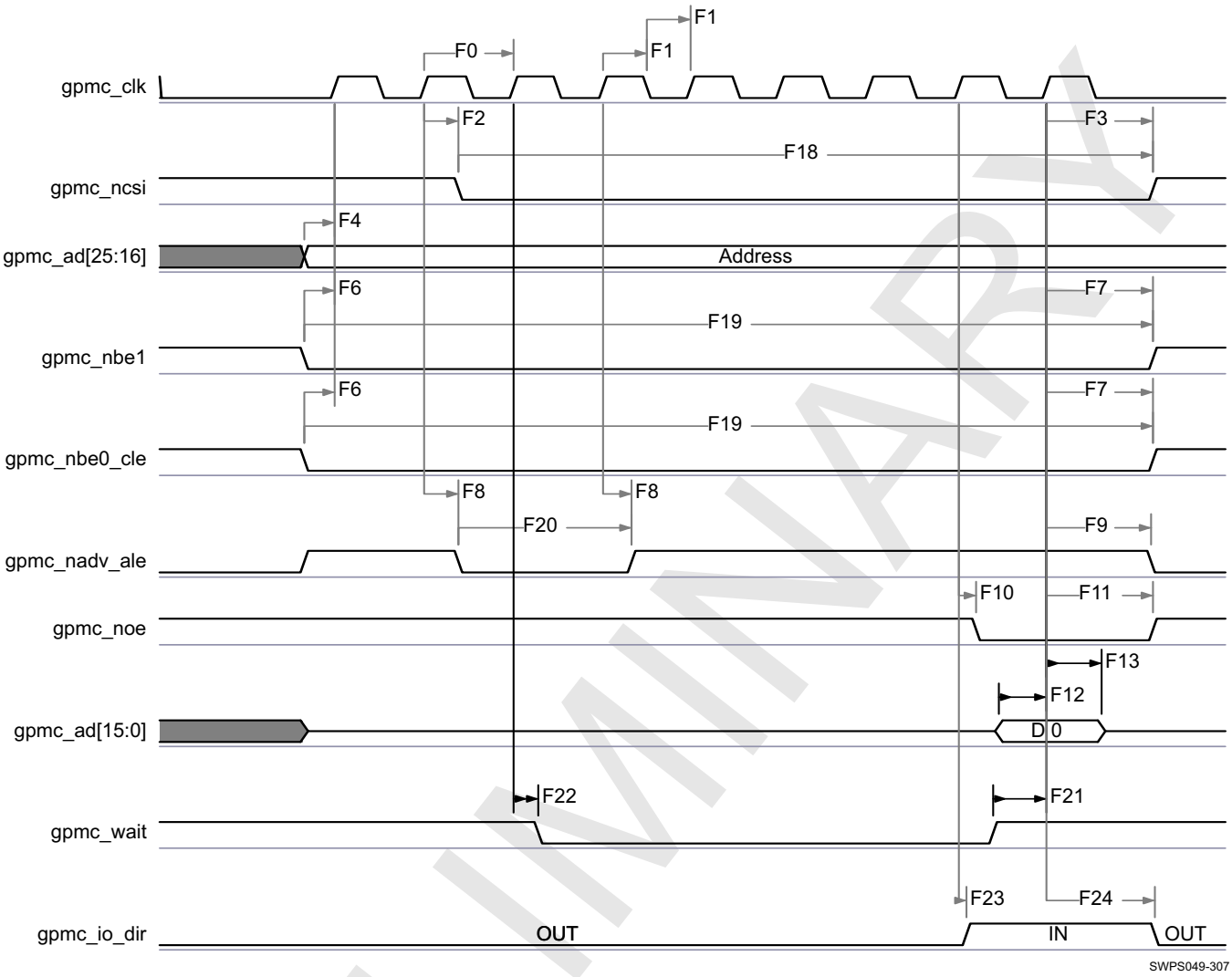


Figure 5-9. GPMC / Non-Multiplexed 16bits NAND – Synchronous Single Read (1) (2) (3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NAND interface can be used only with a limited address range corresponding to 10 address bits.

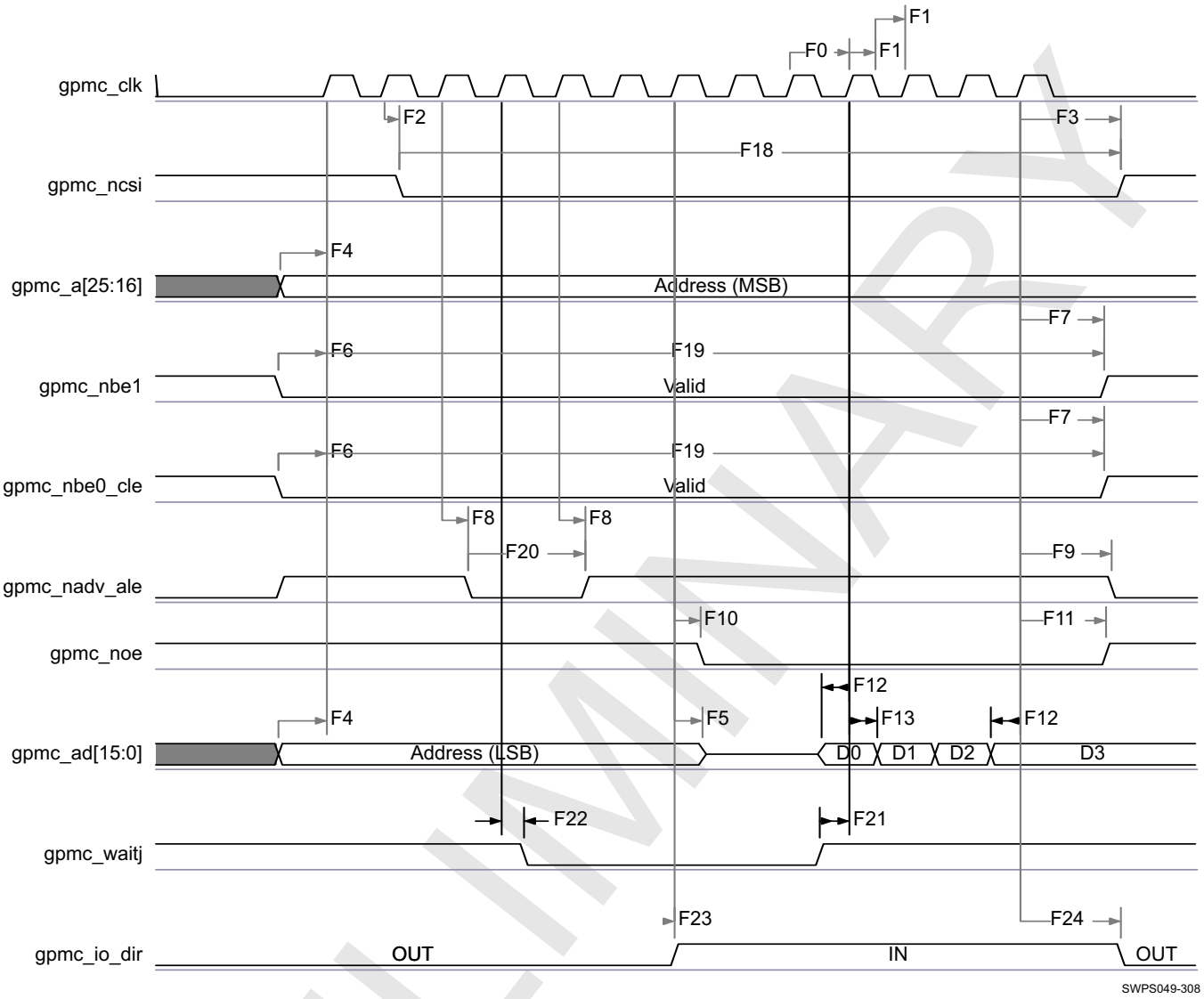


Figure 5-10. GPMC / Multiplexed 16bits NAND – Synchronous Burst Read 4x16 bits (1) (2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

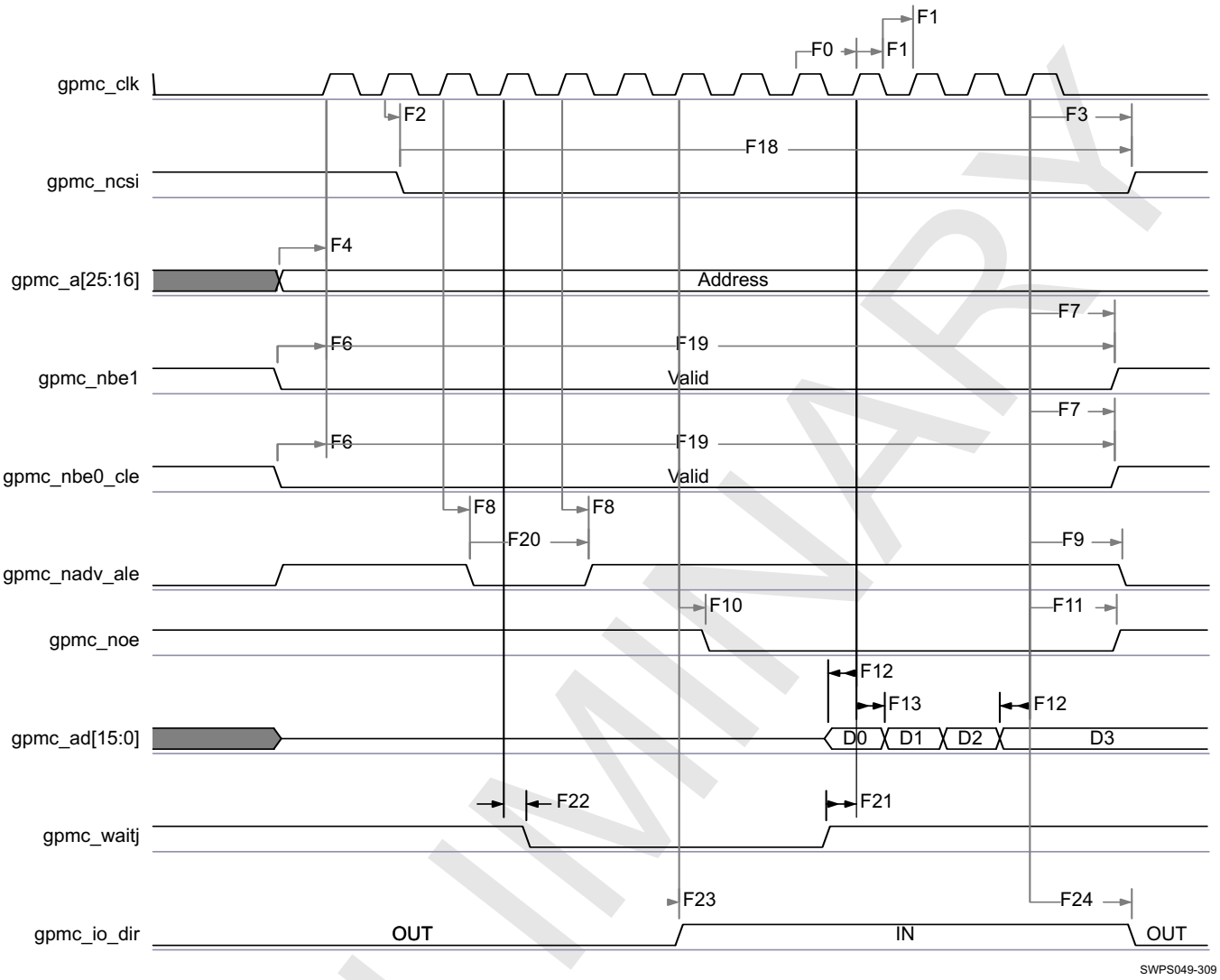


Figure 5-11. GPMC / Non-Multiplexed 16bits NAND – Synchronous Burst Read 4x16 bits (1) (2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NAND interface can be used only with a limited address range corresponding to 10 address bits.

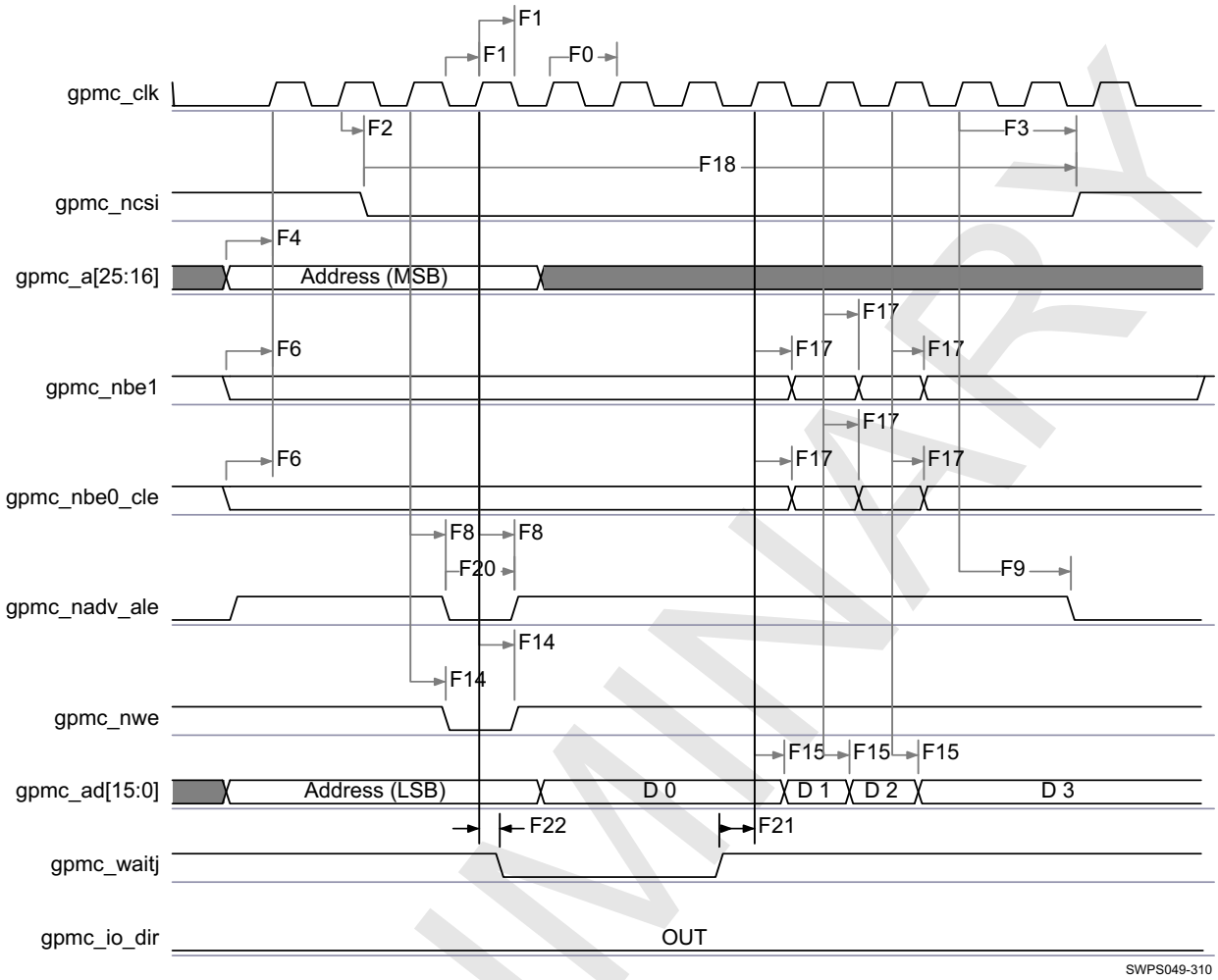


Figure 5-12. GPMC / Multiplexed 16bits NAND – Synchronous Burst Write 4x16 bits (1) (2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

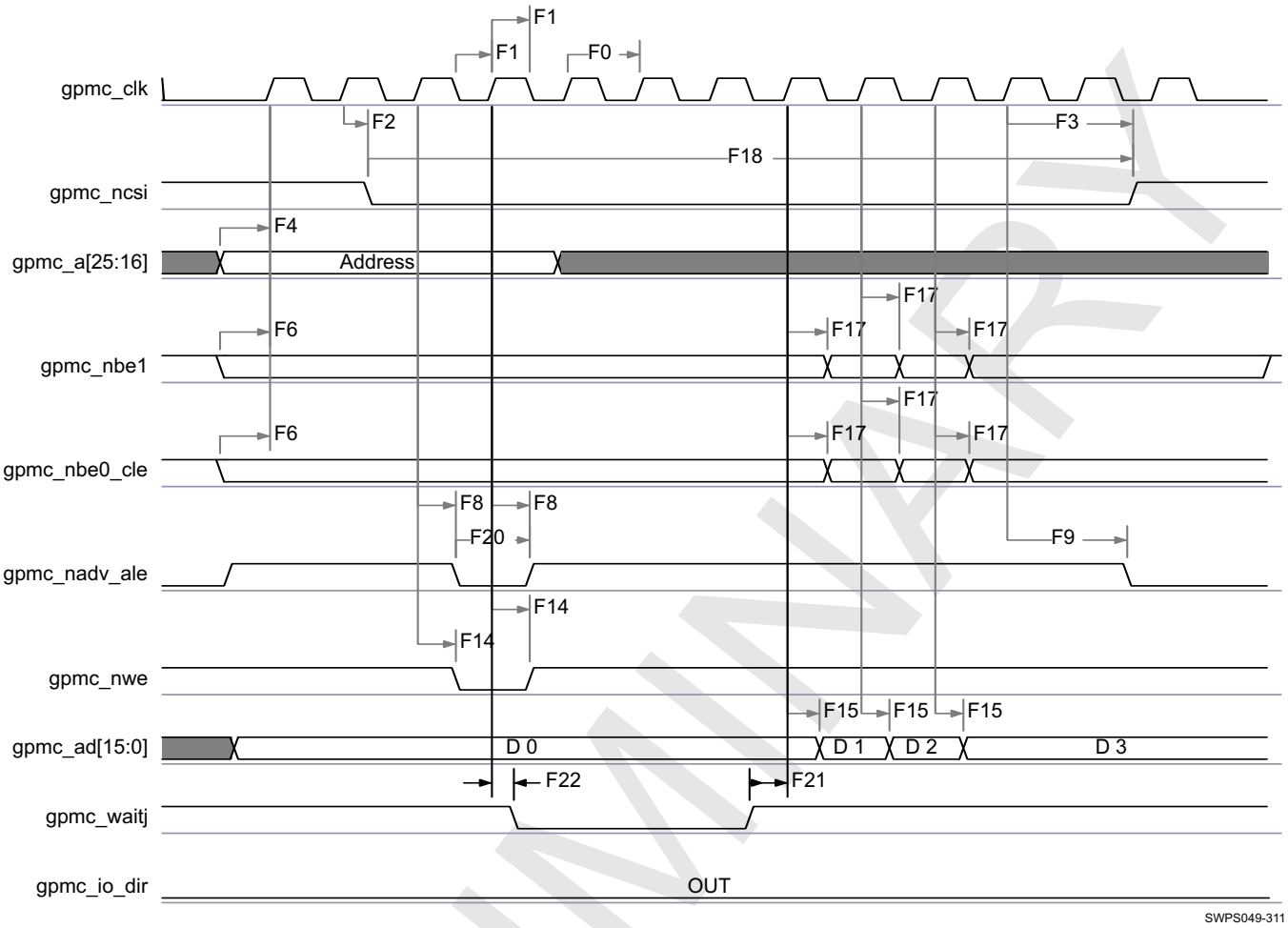


Figure 5-13. XGPMC / Non-Multiplexed 16bits NAND – Synchronous Burst Write 4x16 bits (1) (2) (3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NAND interface can be used only with a limited address range corresponding to 10 address bits

5.4.1.3 PSRAM, Synchronous mode, 88.6 MHz, 1.8 V

Table 5-9. PSRAM Timing Conditions — Synchronous mode

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.5	1.01	ns
t_F	Input signal fall time	0.46	0.97	ns
PCB Conditions(1)				

(1) See Table 8-2.

Table 5-9 and Table 5-10 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-10. PSRAM Timing Requirements — Synchronous Mode(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
F12	$t_{SU(dV-clkH)}$	Setup time, input data gpmc_ad[15:0] valid before output gpmc_clk high	2.3		ns
F13	$t_{H(clkH-dV)}$	Hold time, input data gpmc_ad[15:0] valid after output gpmc_clk high	1.6		ns
F21	$t_{SU(waitV-clkH)}$	Setup time, input wait gpmc_waitx(1) valid before output gpmc_clk high	2.3		ns
F22	$t_{H(clkH-waitV)}$	Hold time, input wait gpmc_waitx(1) valid after output gpmc_clk high	1.6		ns

(1) In gpmc_waitx, x is equal to 0, 1, 2, or 3.

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-11. PSRAM Switching Characteristics — Synchronous Mode(17)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
F0	$1 / t_{C(CLK)}$	Frequency(14), output gpmc_clk			66.5	MHz
F1	$t_{W(CLKH)}$	Typical Pulse duration, output gpmc_clk high		0.5 P(12)		ns
F1	$t_{W(CLKL)}$	Typical Pulse duration, output gpmc_clk low		0.5 P(12)		ns
	$t_{DC(CLK)}$	Duty cycle error, output gpmc_clk			752	ps
	$t_{J(CLK)}$	Jitter standard deviation(15), output gpmc_clk			97.3	ps
	$t_{R(CLK)}$	Rise time, output gpmc_clk		0.9	1.8	ns
	$t_{F(CLK)}$	Fall time, output gpmc_clk		0.9	1.6	ns
	$t_{R(DO)}$	Rise time, output data gpmc_ad[15:0]		0.9	1.8	ns
	$t_{F(DO)}$	Fall time, output data gpmc_ad[15:0]		0.9	1.6	ns
F2	$t_{D(CLKH-nCSV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(11) valid		F(6) + 0.6	F(6) + 6.1	ns
F3	$t_{D(CLKH-nCSIV)}$	Delay time, gpmc_clk rising edge to gpmc_ncsx(11) invalid		E(5) + 0.6	E(5) + 6.1	ns
F4	$t_{D(ADDV-CLK)}$	Delay time, gpmc_a[25:16] address bus valid to gpmc_clk first edge		B(2) – 6.1	B(2) – 0.7	ns
F5	$t_{D(CLKH-ADDIV)}$	Delay time, gpmc_clk rising edge to gpmc_a[25:16] gpmc address bus invalid		0.7		ns
F6	$t_{D(nBEV-CLK)}$	Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge		B(2) – 4.9	B(2) + 0.4	ns
F7	$t_{D(CLKH-nBEIV)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid		D(4) – 0.4	D(4) + 4.9	ns
F8	$t_{D(CLKH-nADV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale valid		G(7) + 0.6	G(7) + 6.1	ns
F9	$t_{D(CLKH-nADVIV)}$	Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid		D(4) + 0.6	D(4) + 6.1	ns
F10	$t_{D(CLKH-nOE)}$	Delay time, gpmc_clk rising edge to gpmc_noe valid		H(8) + 0.3	H(8) + 5.1	ns
F11	$t_{D(CLKH-nOEIV)}$	Delay time, gpmc rising edge to gpmc_noe invalid		E(5) + 0.3	E(5) + 5.1	ns
F14	$t_{D(CLKH-nWE)}$	Delay time, gpmc_clk rising edge to gpmc_nwe transition		I(9) + 0.6	I(9) + 6.1	ns
F15	$t_{D(CLKH-Data)}$	Delay time, gpmc_clk rising edge to gpmc_ad[15:0] data bus transition		J(10) – 0.4	J(10) + 4.9	ns
F17	$t_{D(CLKH-nBE)}$	Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 transition		J(10) – 0.4	J(10) + 4.9	ns
F18	$t_{W(nCSV)}$	Pulse duration, gpmc_ncsx(11) low	Read	A(1)		ns
			Write	A(1)		ns
F19	$t_{W(nBEV)}$	Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low	Read	C(3)		ns
			Write	C(3)		ns
F20	$t_{W(nADVV)}$	Pulse duration, gpmc_nadv_ale low	Read	K(13)		ns
			Write	K(13)		ns
F23	$t_{D(CLKH-IODIR)}$	Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction)		H(8) + 0.7	H(8) + 5.1	ns

Table 5-11. PSRAM Switching Characteristics — Synchronous Mode[17] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
F24	$t_{D(CLKH-IODIRIV)}$	Delay time, gpmc rising edge to gpmc_io_dir low (OUT direction)	M[16] + 0.7	M[16] + 5.1	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK period.
For burst read: A = (CSRdOffTime - CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period with n the page burst access number.
For burst write: A = (CSWrOffTime - CSOnTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK period with n the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: C = (RdCycleTime + (n – 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK with n the page burst access number.
For Burst write: C = (WrCycleTime + (n – 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK with n the page burst access number.

(4) For single read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: D = (RdCycleTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: D = (WrCycleTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(5) For single read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst read: E = (CSRdOffTime – AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For burst write: E = (CSWrOffTime – AccessTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(6) For nCS falling edge (CS activated):
Case GpmcFCLKDivider = 0:
F = 0.5 × CSExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
F = 0.5 × CSExtraDelay × GPMC_FCLK if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
F = 0.5 × CSExtraDelay × GPMC_FCLK if ((CSOnTime – ClkActivationTime) is a multiple of 3)
F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 1) is a multiple of 3)
F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK if ((CSOnTime – ClkActivationTime – 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVOnTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVOnTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV desactivated) in Reading mode:
Case GpmcFCLKDivider = 0:
G = 0.5 × ADVExtraDelay × GPMC_FCLK Case GpmcFCLKDivider = 1:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 × ADVExtraDelay × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK if ((ADVRdOffTime – ClkActivationTime – 2) is a multiple of 3)
For ADV rising edge (ADV desactivated) in Writing mode:
Case GpmcFCLKDivider = 0:
G = 0.5 * ADVExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK otherwise
Case GpmcFCLKDivider = 2:
G = 0.5 * ADVExtraDelay * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime) is a multiple of 3)
G = (1 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 1) is a multiple of 3)
G = (2 + 0.5 * ADVExtraDelay) * GPMC_FCLK if ((ADVWrOffTime – ClkActivationTime – 2) is a multiple of 3)

(8) For OE falling edge (OE activated) / IO DIR rising edge (IN direction):
Case GpmcFCLKDivider = 0:
H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOnTime – ClkActivationTime) is a multiple of 3)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 1) is a multiple of 3)
H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOnTime – ClkActivationTime – 2) is a multiple of 3)
For OE rising edge (OE desactivated):
Case GpmcFCLKDivider = 0:
H = 0.5 × OEExtraDelay × GPMC_FCLK
Case GpmcFCLKDivider = 1:
H = 0.5 × OEExtraDelay × GPMC_FCLK if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
H = 0.5 × OEExtraDelay × GPMC_FCLK if ((OEOffTime – ClkActivationTime) is a multiple of 3)
H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 1) is a multiple of 3)
H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK if ((OEOffTime – ClkActivationTime – 2) is a multiple of 3)

(9) For WE falling edge (WE activated):
Case GpmcFCLKDivider = 0:
I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOnTime – ClkActivationTime) is a multiple of 3)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 1) is a multiple of 3)
I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOnTime – ClkActivationTime – 2) is a multiple of 3)
For WE rising edge (WE desactivated):
Case GpmcFCLKDivider = 0:
I = 0.5 * WEExtraDelay * GPMC_FCLK
Case GpmcFCLKDivider = 1:
I = 0.5 * WEExtraDelay * GPMC_FCLK if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK
otherwise
Case GpmcFCLKDivider = 2:
I = 0.5 * WEExtraDelay * GPMC_FCLK if ((WEOffTime – ClkActivationTime) is a multiple of 3)
I = (1 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 1) is a multiple of 3)
I = (2 + 0.5 * WEExtraDelay) * GPMC_FCLK if ((WEOffTime – ClkActivationTime – 2) is a multiple of 3)

(10) J = GPMC_FCLK period

(11) In “gpmc_ncsx”, x is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(12) P = gpmc_clk period

(13) For read: K = (ADVRdOffTime – ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK
For write: K = (ADVWrOffTime – ADVOnTime) * (TimeParaGranularity + 1) * GPMC_FCLK

(14) Related to the gpmc_clk output clock Maximum and minimum frequency programmable in I/F module by setting the GPMC_CONFIG1_CSx configuration register bit fields GpmcFCLKDivider

(15) The jitter probability density can be approximated by a Gaussian function.

(16) M = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK
Above M parameter expression is given as one example of GPMC programmation. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behaviour of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non/multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behaviour is automactically handled by GPMC controller

(17) See the Data Manual Operating Condition Addendum for CORE OPP voltages.

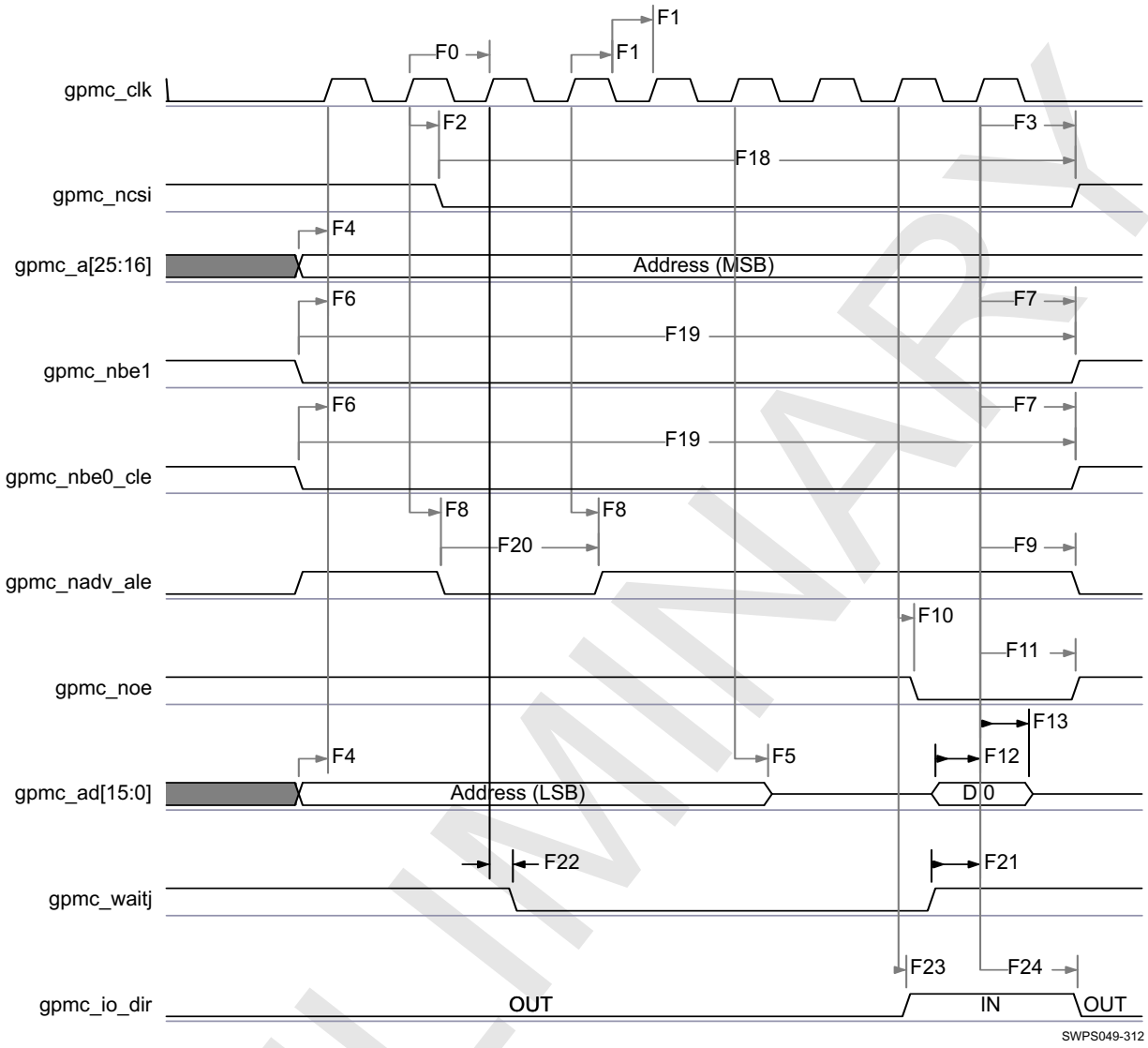


Figure 5-14. GPMC / Multiplexed 16bits PSRAM – Synchronous Single Read (1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

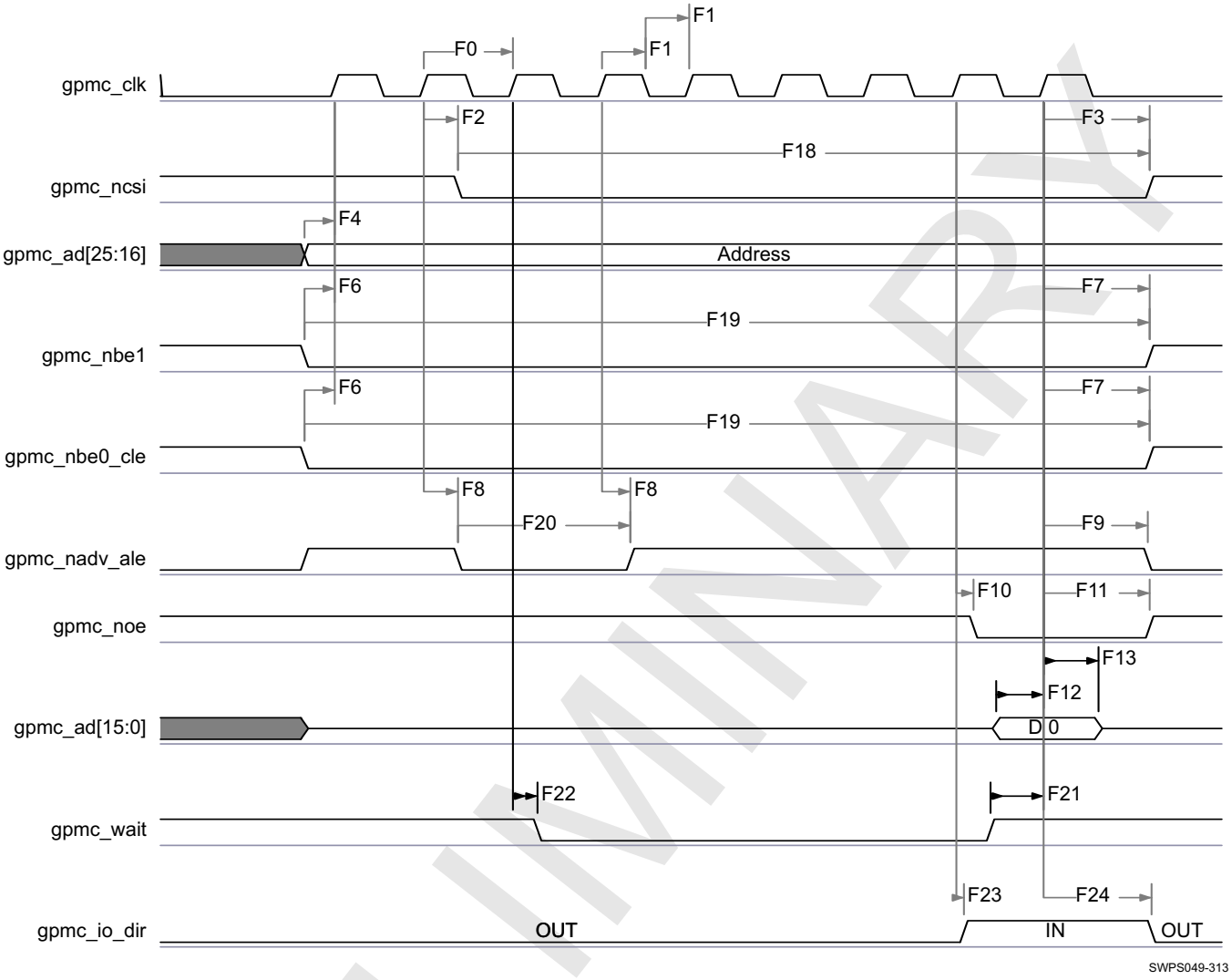


Figure 5-15. GPMC / Non-Multiplexed 16bits PSRAM – Synchronous Single Read(1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

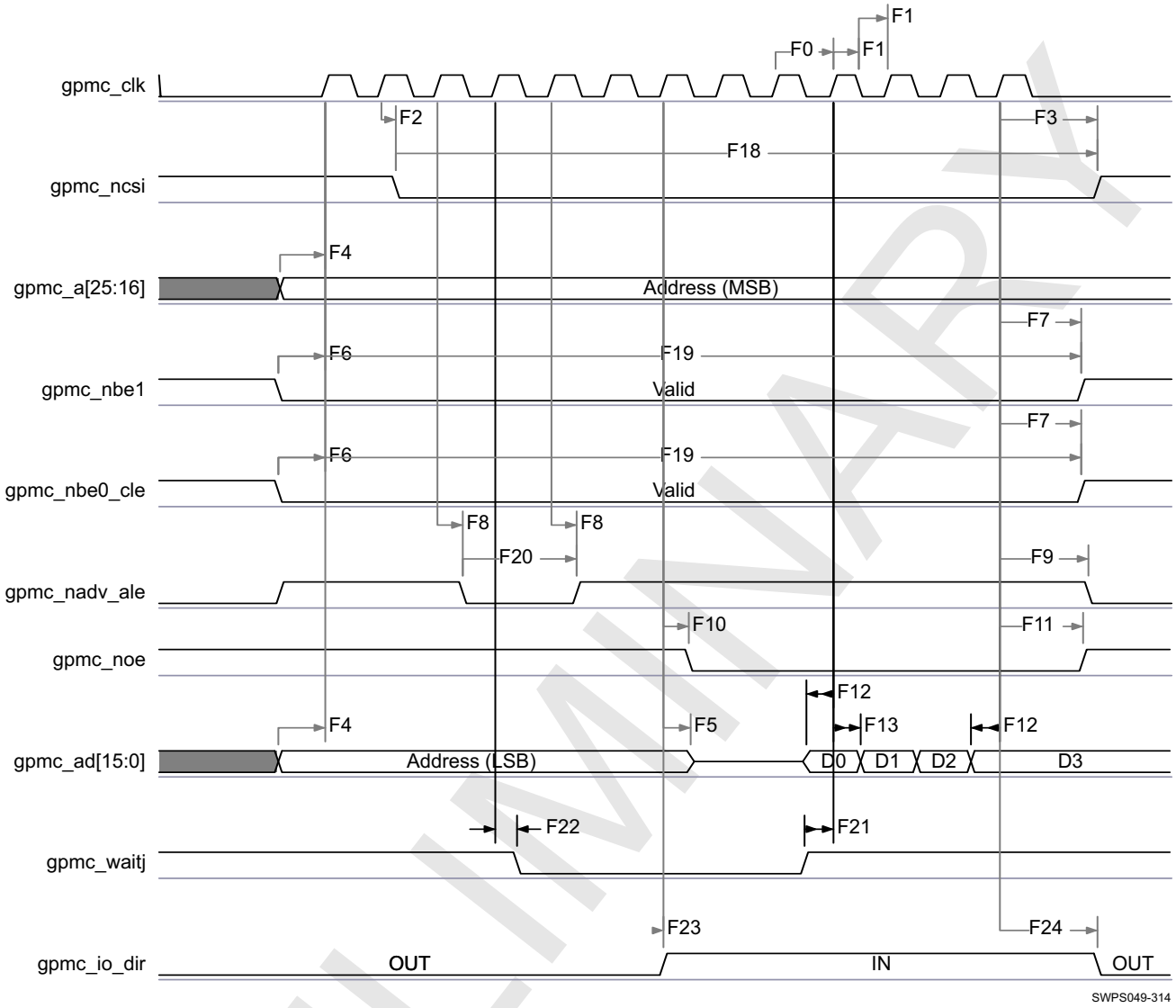


Figure 5-16. GPMC / Multiplexed 16bits PSRAM – Synchronous Burst Read 4x16 bits (1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

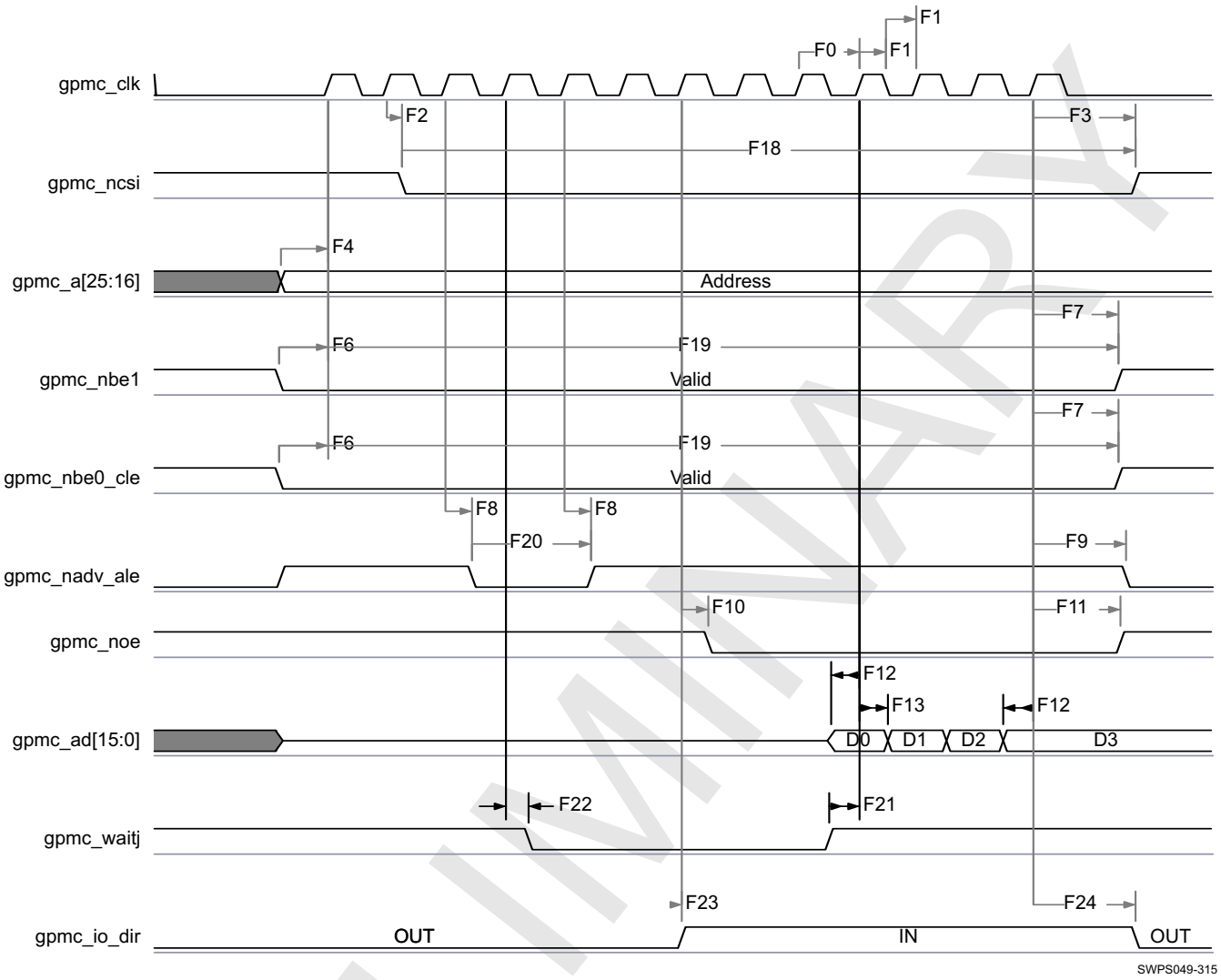


Figure 5-17. GPMC / Non-Multiplexed 16bits PSRAM – Synchronous Burst Read 4x16 bits (1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

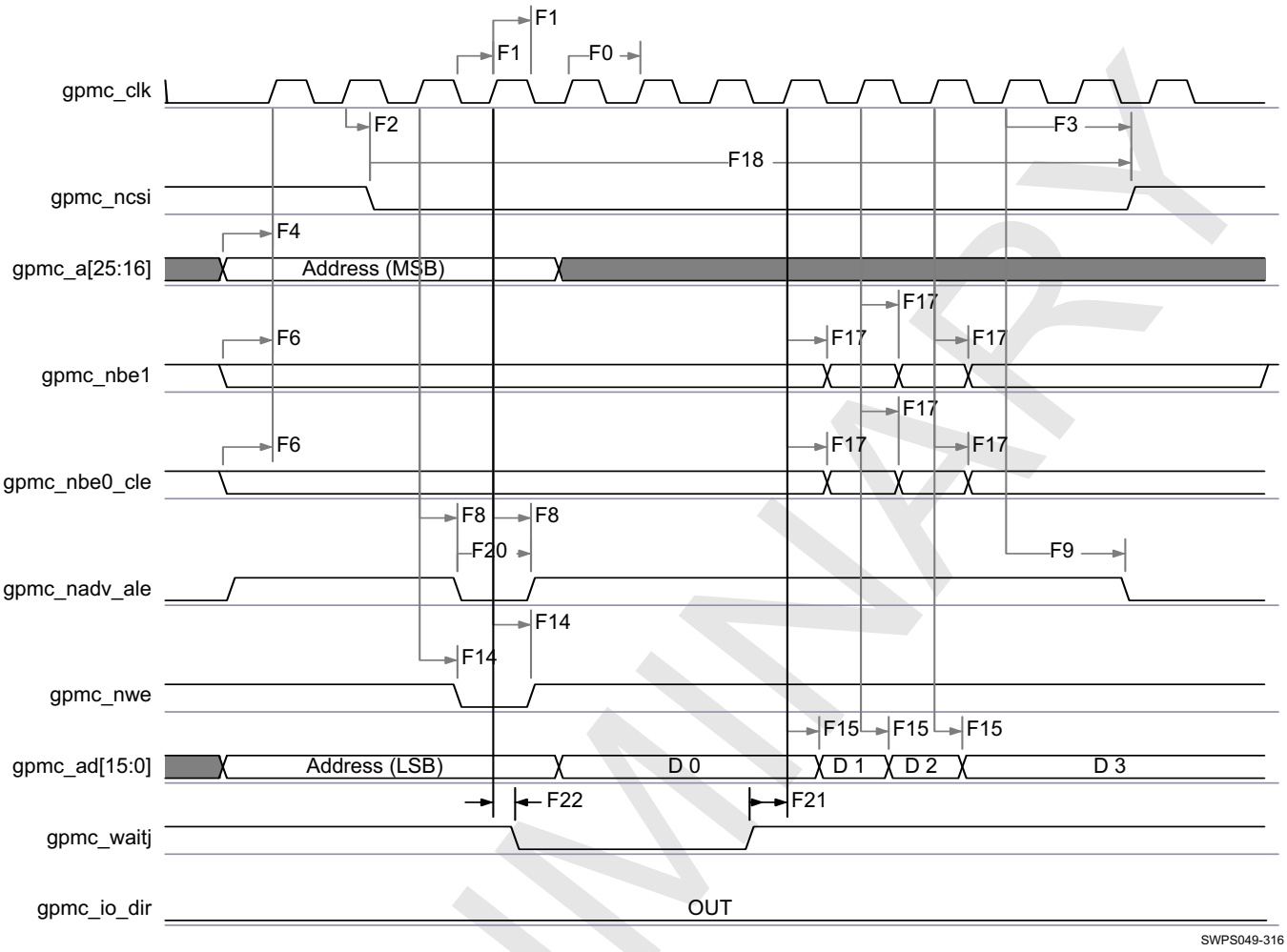


Figure 5-18. GPMC / Multiplexed 16bits PSRAM – Synchronous Burst Write 4x16 bits (1)(2)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

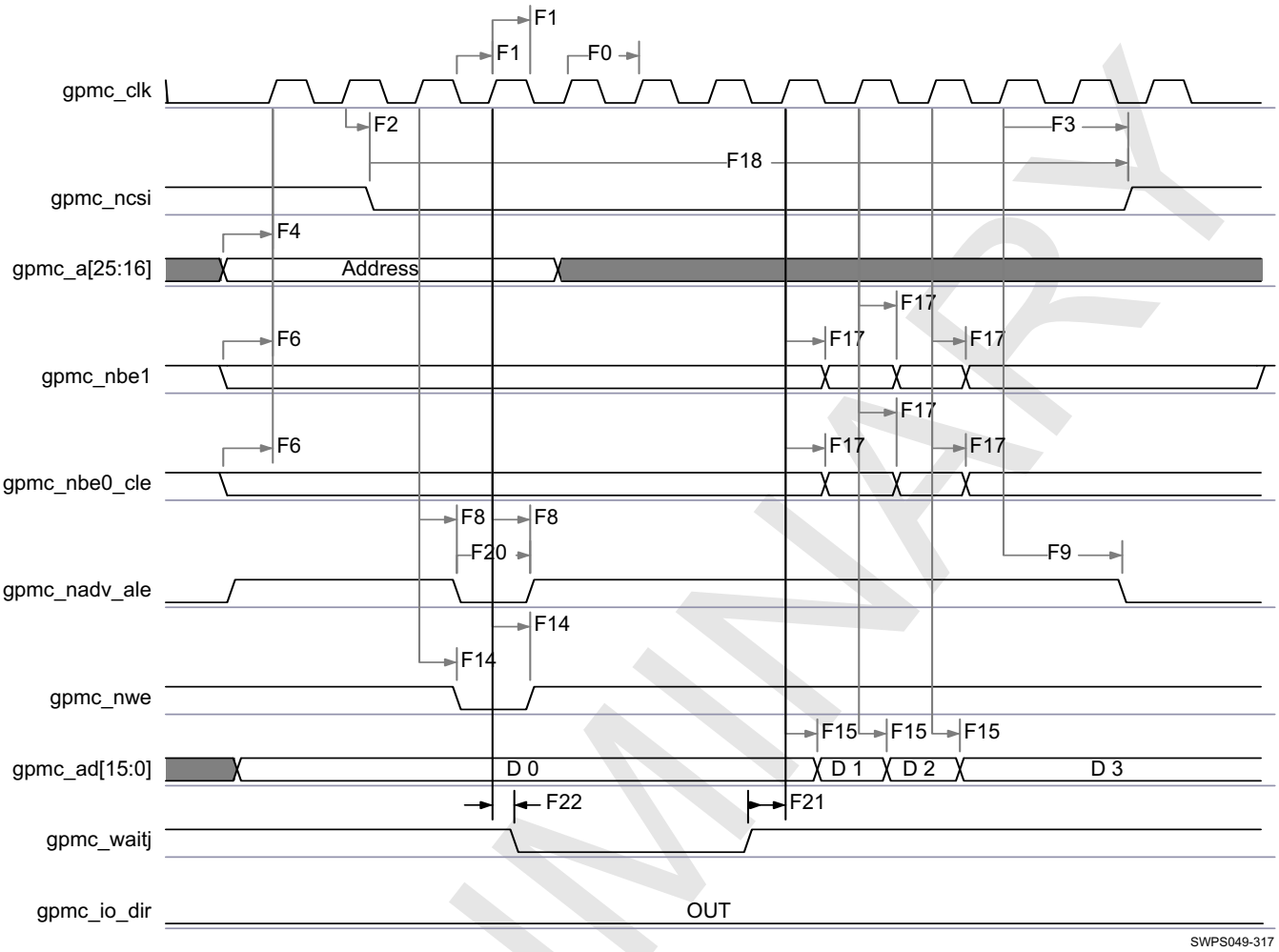


Figure 5-19. GPMC / Non-Multiplexed 16bits PSRAM – Synchronous Burst Write 4x16 bits (1)(2)(3)

(1) In gpmc_ncsi, i is equal to 0, 1, 2, 3, 4, 5, 6, 7.

(2) In gpmc_waitj, x is equal to 0, 1, 2, 3.

(3) Non Multiplexed NOR interface can be used only with a limited address range corresponding to 10 address bits.

5.4.2 External Memory Interface (EMIF), 1.2 V

NOTE

For more information, see the EMIF Controller section of the OMAP543x TRM.

The SDRAM controller subsystem module provides connectivity between the processor and external DRAM memory components.

The module includes support for double-data-rate SDRAM (mobile DDR).

The LPDDR2 module embedded in the OMAP5430 is compliant with the JESD209-2 LPDDR2 standard.

For more information on LPDDR2 timing requirements and switching characteristics, see the JESD209-2 LPDDR2 standard.

5.5 Multimedia Interfaces

5.5.1 Camera Interface

NOTE

For more information on the Imaging Subsystem, see the OMAP543x TRM.

The imaging subsystem (ISS) deals with the processing of the pixel data coming from an external image sensor, data from memory. The ISS is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture. The ISS has three serial camera interfaces (primary, secondary, and tertiary) and a parallel interface within the ISS boundary:

- The primary serial interface (CSI2 Port A) is compliant with MIPI CSI-2 protocol with four data lanes.
- The secondary serial interface (CSI2 Port B) is compliant with MIPI CSI-2 protocol with two data lanes or SMIA CCP2 protocol with one data lane.
- The tertiary serial interface (CSI2 Port C) is compliant with MIPI CSI-2 protocol with one data lane or CCP2 protocol with one data lane.
- The camera parallel interface (CPI) supports up to 16 data lanes.

5.5.1.1 CSI-2 MIPI D-PHY—1.5 V and 1.8 V

The CSI-2 port A is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 4 data differential lanes plus 1 clock differential lane in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane.

The CSI-2 port B is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 2 data lanes plus 1 clock lane (differential) in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane, in synchronous mode.

The CSI-2 port C is compliant with the MIPI D-PHY RX specification v1.00.00 and the MIPI CSI-2 specification v1.00, with 1 data differential lane plus 1 clock differential lane in synchronous mode, double data rate:

- 1.5 Gbps (750 MHz) @OPP_NOM for each lane.

5.5.1.2 SMIA CCP2—1.5 V and 1.8 V

The CSI-2 port B is compliant also with the SMIA CCP2 specification v1.0, with 1 data differential lane plus 1 clock differential lane in synchronous mode:

- Class 0 (signaling method: data or clock): up to 208 Mbps (208 MHz) @OPP_NOM.
- Class 1 (signaling method: data or strobe): up to 416 Mbps (208 MHz) @OPP_NOM.
- Class 2 (signaling method: data or strobe): up to 650 Mbps (325 MHz) @OPP_NOM.

The CSI-2 port C is compliant also with the SMIA CCP2 specification v1.0, with 1 data differential lane plus 1 clock differential lane in synchronous mode:

- Class 0 (signaling method: data or clock): up to 208 Mbps (208 MHz) @OPP_NOM.
- Class 1 (signaling method: data or strobe): up to 416 Mbps (208 MHz) @OPP_NOM.
- Class 2 (signaling method: data or strobe): up to 650 Mbps (325 MHz) @OPP_NOM.

5.5.1.3 Camera Parallel Interface (CPI)—1.8 V

5.5.1.3.1 Image Sensor

The camera parallel interface supports the CPI 16-bit ITU mode, in half-cycle mode (fall to rise), for image sensor 5 Mpix 15 fps (+30% blank margin).

NOTE

Regarding the CPI parallel camera applications, consider that only half-cycle mode in single data rate (SDR) is supported.

Moreover, only the fall-to-rise mode is supported (data generated by a peripheral on falling edge, and captured by OMAP543x on rising edge of the clock).

Table 5-13 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-12. CPI Timing Conditions—Image Sensor

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions(1)				
t_R	Input signal rise time	120	920	ps
t_F	Input signal fall time	110	830	ps
PCB Conditions				
	Number of external peripheral		1	
	Trace length	5	20	cm
	Characteristic impedance	30	65	Ω

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5430 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

Table 5-13. CPI Timing Requirements—Image Sensor(4)(5)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
ISP1	$1 / t_{c(pclk)}$	Frequency(1), cpi_pclk CPI input pixel clock		97.08	MHz
ISP2	$t_{w(pclkL)}$	Typical pulse duration, cpi_pclk low	0.5 × P(2)		ns
ISP3	$t_{w(pclkH)}$	Typical pulse duration, cpi_pclk high	0.5 × P(2)		ns
	$t_{dc(pclk)}$	Duty cycle error, cpi_pclk		0.5 × P—3.247	ns
	$t_{J(pclk)}$	Cycle jitter(3), cpi_pclk		0.06 × P(2)	ns
ISP4	$t_{su(vsV-pclk)}$	Setup time, cpi_vsync valid before cpi_pclk rising edge	1.76		ns
ISP5	$t_{h(pclk-vsV)}$	Hold time, cpi_vsync valid after cpi_pclk rising edge	4.16		ns
ISP6	$t_{su(hsV-pclk)}$	Setup time, cpi_hsync valid before cpi_pclk rising edge	1.76		ns
ISP7	$t_{h(pclk-hsV)}$	Hold time, cpi_hsync valid after cpi_pclk rising edge	4.16		ns
ISP8	$t_{su(dV-pclk)}$	Setup time, cpi_data[15:0] valid before cpi_pclk rising edge	1.76		ns
ISP9	$t_{h(pclk-dV)}$	Hold time, cpi_data[15:0] valid after cpi_pclk rising edge	4.16		ns
ISP10	$t_{su(wenV-pclk)}$	Setup time, cpi_wen valid before cpi_pclk rising edge	1.76		ns
ISP11	$t_{h(pclk-wenV)}$	Hold time, cpi_wen valid after cpi_pclk rising edge	4.16		ns
ISP12	$t_{su(fidV-pclk)}$	Setup time, cpi_fid valid before cpi_pclk rising edge	1.76		ns
ISP13	$t_{h(pclk-fidV)}$	Hold time, cpi_fid valid after cpi_pclk rising edge	4.16		ns

(1) Related with the input maximum frequency supported by the ISP module.

(2) P = cpi_pclk period in ns

(3) Maximum cycle jitter supported by cpi_pclk input pixel clock.

(4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

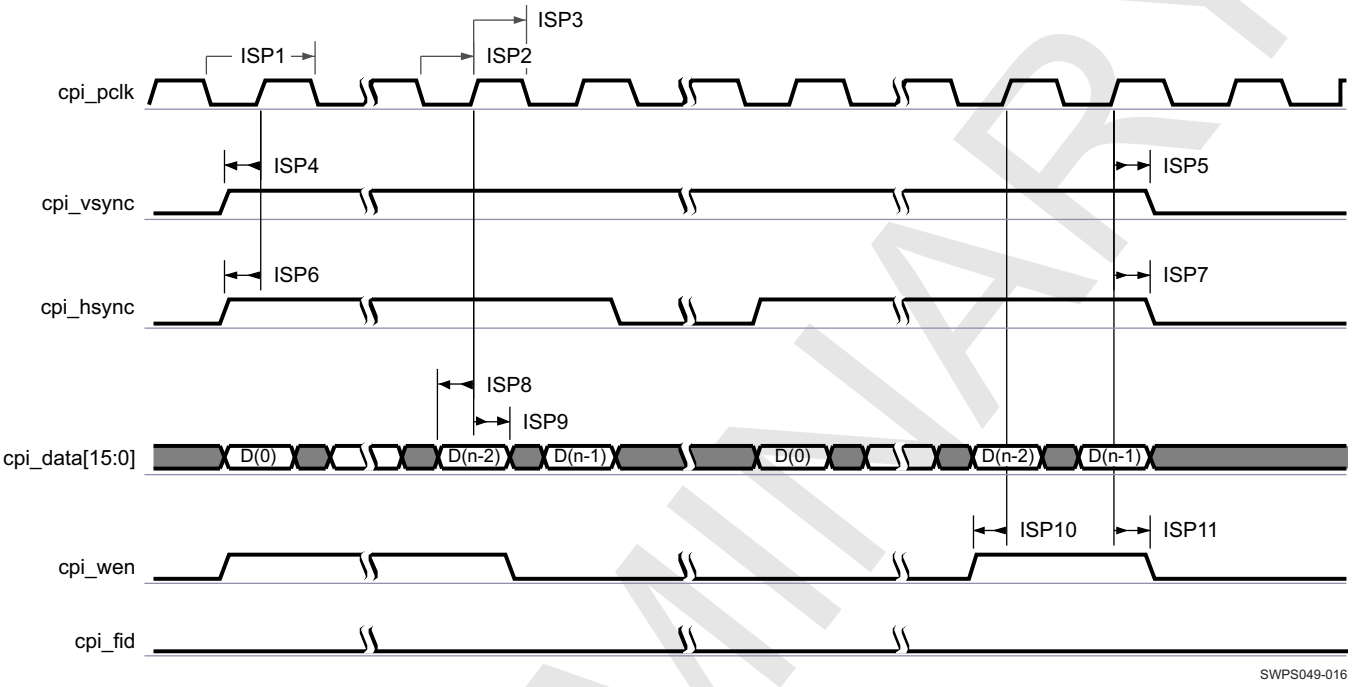


Figure 5-20. CPI—Image Sensor—1.8-V Progressive Mode(1)

(1) n = 16

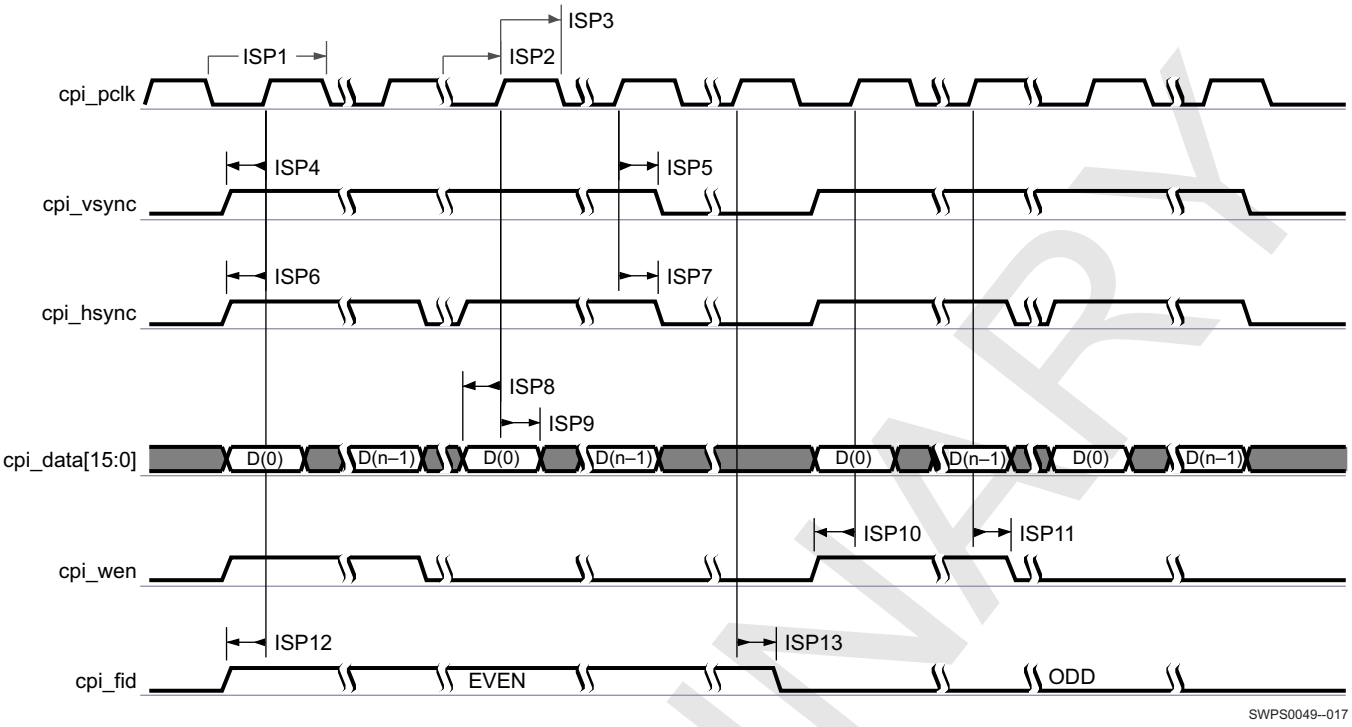


Figure 5-21. CPI—Image Sensor—1.8-V Interlaced Mode(1)

(1) n = 16

5.5.1.3.2 HDMI Receiver

The camera parallel interface supports the CPI 16-bit ITU mode, in half-cycle mode (fall to rise), for HDMI receiver 1080p 60fps YUV422.

NOTE

Regarding the CPI parallel camera applications, consider that only half-cycle mode in SDR is supported. Moreover, only the fall-to-rise mode is supported (data generated by a peripheral on falling edge, and captured by the OMAP543x device on rising edge of the clock).

Table 5-15 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-14. CPI Timing Conditions—HDMI Receiver

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions(1)				
t_R	Input signal rise time	120	920	ps
t_F	Input signal fall time	110	830	ps
PCB Conditions				
	Number of external peripheral		1	
	Trace length	2	5	cm
	Characteristic impedance	30	65	Ω

(1) In this table the rise and fall times are calculated for 10% to 90% of VDDS. For more information on the corresponding OMAP5430 VDDS power supply name, see Table 2-1, POWER NAME [10] column with the ball name.

Table 5-15. CPI Timing Requirements—HDMI Receiver(4)(5)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
ISP1	$1 / t_{c(pclk)}$	Frequency(1), cpi_pclk CPI input pixel clock		148.5	MHz
ISP2	$t_{w(pclkL)}$	Typical pulse duration, cpi_pclk low	0.5 × P(2)		ns
ISP3	$t_{w(pclkH)}$	Typical pulse duration, cpi_pclk high	0.5 × P(2)		ns
	$t_{dc(pclk)}$	Duty cycle error, cpi_pclk		0.5 × P—3.247	ns
	$t_{J(pclk)}$	Cycle jitter(3), cpi_pclk		0.06 × P(2)	ns
ISP4	$t_{su(vsV-pclk)}$	Setup time, cpi_vsync valid before cpi_pclk rising edge	0.27		ns
ISP5	$t_{h(pclk-vsV)}$	Hold time, cpi_vsync valid after cpi_pclk rising edge	2.67		ns
ISP6	$t_{su(hsV-pclk)}$	Setup time, cpi_hsync valid before cpi_pclk rising edge	0.27		ns
ISP7	$t_{h(pclk-hsV)}$	Hold time, cpi_hsync valid after cpi_pclk rising edge	2.67		ns
ISP8	$t_{su(dV-pclk)}$	Setup time, cpi_data[15:0] valid before cpi_pclk rising edge	0.27		ns
ISP9	$t_{h(pclk-dV)}$	Hold time, cpi_data[15:0] valid after cpi_pclk rising edge	2.67		ns
ISP10	$t_{su(wenV-pclk)}$	Setup time, cpi_wen valid before cpi_pclk rising edge	0.27		ns
ISP11	$t_{h(pclk-wenV)}$	Hold time, cpi_wen valid after cpi_pclk rising edge	2.67		ns
ISP12	$t_{su(fidV-pclk)}$	Setup time, cpi_fid valid before cpi_pclk rising edge	0.27		ns
ISP13	$t_{h(pclk-fidV)}$	Hold time, cpi_fid valid after cpi_pclk rising edge	2.67		ns

(1) Related with the input maximum frequency supported by the ISP module.

(2) P = cpi_pclk period in ns

(3) Maximum cycle jitter supported by cpi_pclk input pixel clock.

(4) The timing requirements are assured up to the cycle jitter and duty cycle error conditions specified.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

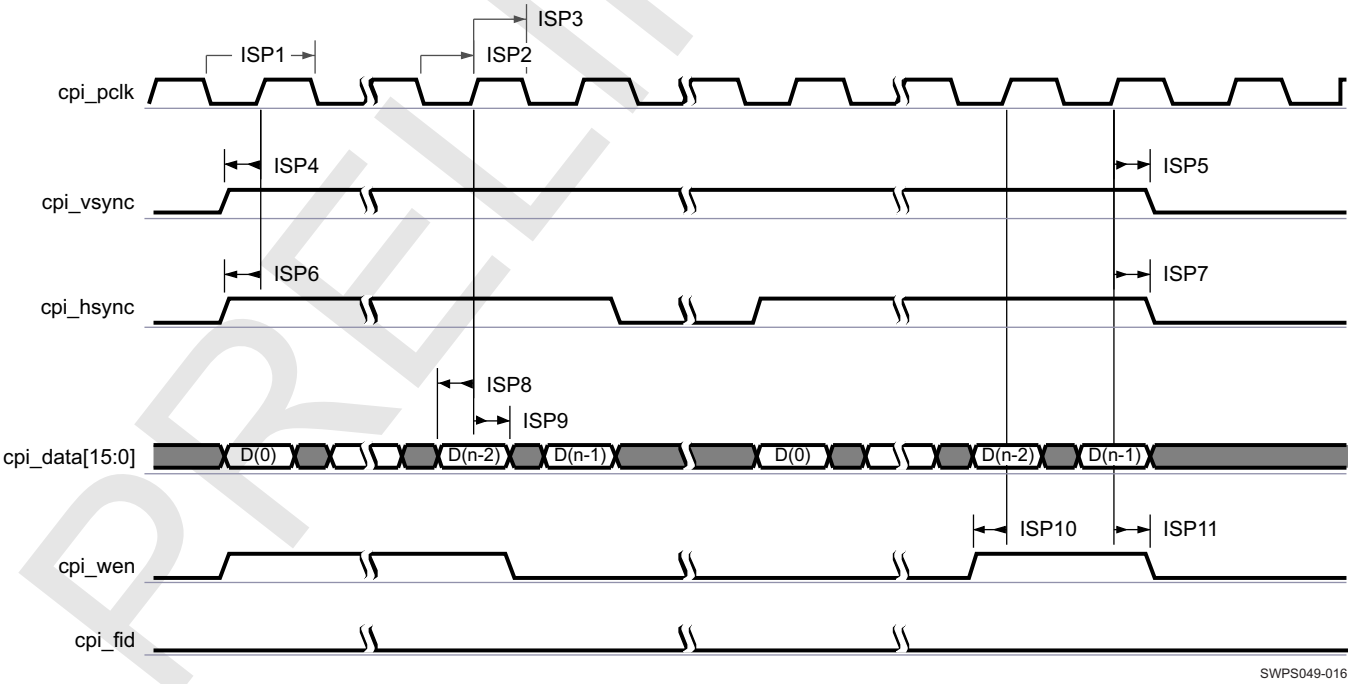


Figure 5-22. CPI—HDMI Receiver—1.8-V Progressive Mode(1)

(1) n = 16

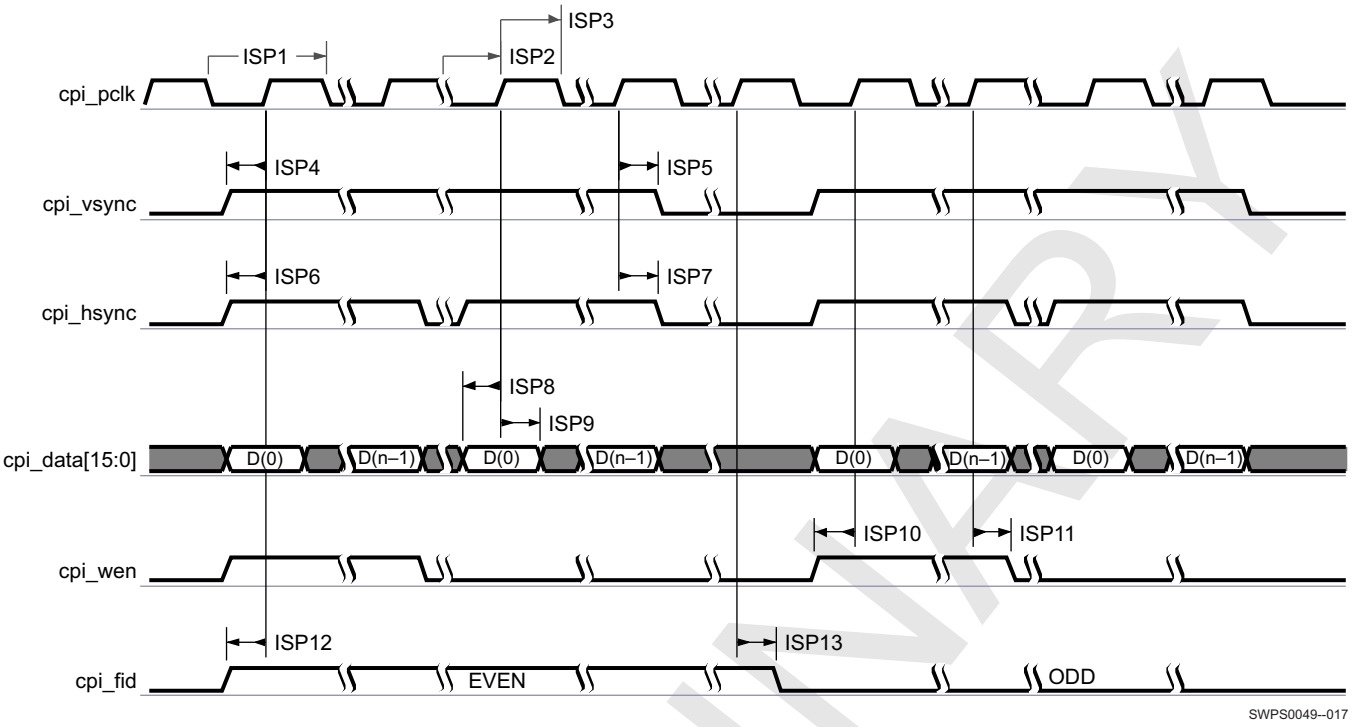


Figure 5-23. CPI—HDMI Receiver —1.8-V Interlaced Mode(1)

(1) n = 16

5.5.2 Display Interface

NOTE

For more information, see the Display Subsystem chapter in the OMAP543x TRM.

The display subsystem (DSS) provides the logic to display a video frame from the memory frame buffer on a liquid-crystal display (LCD) panel or TV set.

The display subsystem has three interfaces for LCD output:

- DSI Port A and Port C (display serial interface) supporting MIPI DSI-1 protocol.
- RFBI (remote frame buffer interface) supporting MIPI DBI 2.0 protocol.
- DISPC supporting MIPI DPI 2.0 protocol.

The display subsystem has two interfaces for TV output:

- DISPC supporting MIPI DPI 2.0 protocol.
- HDMI (high-definition multimedia interface)

5.5.2.1 Display Controller (DISPC)

NOTE

For more information, see the Display Subsystem / Display Controller section of the OMAP543x TRM.

The DISPC interface consists of:

- 24-bit data bus (data[23:0])
- Horizontal synchronization signal (HSYNC)
- Vertical synchronization signal (VSYNC)
- Data enable (DE)
- Pixel clock (PCLK)

This interface is compliant with MIPI DPI standard revision 2.0 and delivers the parallel pixel and synchronization signals for LCD panel or TV set.

5.5.2.1.1 DISPC—MIPI DPI 24 Bits for Display Extension—1.8 V

For DISPC PCB requirements and IO programming, see Table 8-51.

Table 5-16 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-16. DISPC Switching Characteristics—MIPI DPI 24 Bits for Display Extension(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
D1	$1 / t_{c(pclk)}$	Frequency, output pixel clock dispc_pclk		170	MHz
D2	$t_{w(pclkL)}$	Typical pulse duration, output pixel clock dispc_pclk low	0.5 × P(1)		ns
D3	$t_{w(pclkH)}$	Typical pulse duration, output pixel clock dispc_pclk high	0.5 × P(1)		ns
	$t_{dc(pclk)}$	Duty cycle error, output pixel clock dispc_pclk		294	ps
	$t_{j(pclk)}$	Jitter standard deviation(2), output pixel clock dispc_pclk		39	ps
	$t_{R(pclk)}$	Rise time, output pixel clock dispc_pclk		661	ps
	$t_{F(pclk)}$	Fall time, output pixel clock dispc_pclk		670	ps
D4	$t_{d(pclkA-vsyncV)}$	Delay time, output pixel clock dispc_pclk transition to output vertical synchronization dispc_vsync valid	–1653	153	ps
	$t_{R(vsync)}$	Rise time, output vertical synchronization dispc_vsync		661	ps

Table 5-16. DISPC Switching Characteristics—MIPI DPI 24 Bits for Display Extension[3] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$t_{F(vsync)}$	Fall time, output vertical synchronization dispc_vsync		670	ps
D5	$t_{d(pclkA-hsyncV)}$	Delay time, output pixel clock dispc_pclk transition to output horizontal synchronization dispc_hsync valid	–1653	153	ps
	$t_{R(hsync)}$	Rise time, output horizontal synchronization dispc_hsync		661	ps
	$t_{F(hsync)}$	Fall time, output horizontal synchronization dispc_hsync		670	ps
D6	$t_{d(pclkA-dV)}$	Delay time, output pixel clock dispc_pclk transition to output data dispc_data[23:0] valid	–1653	153	ps
	$t_{R(d)}$	Rise time, output data dispc_data[23:0]		661	ps
	$t_{F(d)}$	Fall time, output data dispc_data[23:0]		670	ps
D7	$t_{d(pclkA-deV)}$	Delay time, output pixel clock dispc_pclk transition to output data enable dispc_de valid	–1653	153	ps
	$t_{R(de)}$	Rise time, output data enable dispc_de		661	ps
	$t_{F(de)}$	Fall time, output data enable dispc_de		670	ps
D8	$t_{d(pclkA-fidV)}$	Delay time, output pixel clock dispc_pclk transition to output field ID dispc_fid valid	–1653	153	ps
	$t_{R(fid)}$	Rise time, output field ID dispc_fid		661	ps
	$t_{F(fid)}$	Fall time, output field ID dispc_fid		670	ps

(1) P = output dispc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

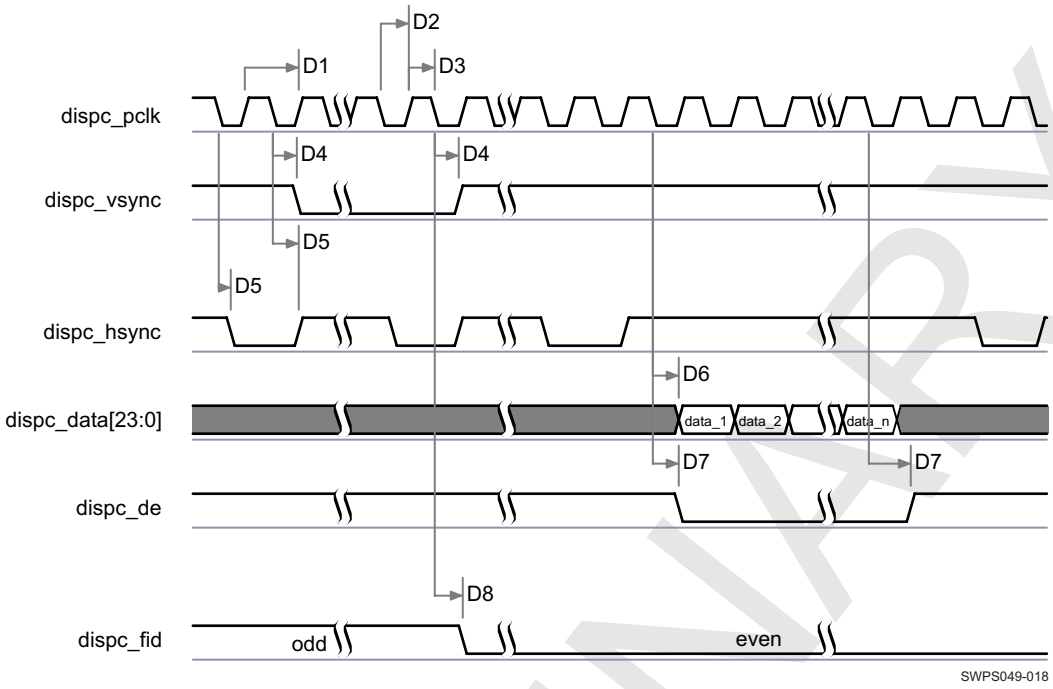


Figure 5-24. DISPC—MIPI DPI 24 Bits for Display Extension(1) (2)(3)

(1) The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
(2) The polarity and the pulse width of dispc_hsync and dispc_vsync are programmable, refer to the DISPC section of the OMAP543x TRM.
(3) The dispc_pclk frequency can be configured, refer to the DISPC section of the OMAP543x TRM.

5.5.2.2 DSS—Remote Frame Buffer Interface (RFBI) Applications—1.8 V

5.5.2.2.1 DSS—Remote Frame Buffer Interface (RFBI) Applications—Pico DLP

NOTE

For more information, see the Display Subsystem / Remote Frame Buffer Interface section of the OMAP543x TRM.

The RFBI module is part of the display subsystem that provides the logic to display a picture from the memory frame buffer (SDRAM or SRAM) on an LCD panel.

For RFBI PCB requirements and IO programming, see Table 8-53.

Table 5-17 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-17. DSS—RFBI Switching Characteristics—Pico DLP(9)

PARAMETER		OPP_NOM		UNIT
		MIN	MAX	
$t_{w(rfbi\_weH)}$	Pulse duration, output write enable rfbi_we high	A(1)		ns
$t_{w(rfbi\_weL)}$	Pulse duration, output write enable rfbi_we low	B(2)		ns
$t_{d(rfbi\_a0\text{-}rfbi\_weL)}$	Delay time, output command/data control rfbi_a0 transition to output write enable rfbi_we low	C(3)		ns
$t_{d(rfbi\_weH\text{-}rfbi\_a0)}$	Delay time, output write enable rfbi_we high to output command/data control rfbi_a0 transition	D(4)		ns
$t_{d(rfbi\_csx\text{-}rfbi\_weL)}$	Delay time, output chip select rfbi_cs0 low to output write enable rfbi_we low	E(5)		ns
$t_{d(rfbi\_weH\text{-}rfbi\_csxH)}$	Delay time, output write enable rfbi_we high to output chip select rfbi_cs0 high	F(6)		ns

Table 5-17. DSS—RFBI Switching Characteristics—Pico DLP[9] (continued)

PARAMETER		OPP_NOM		UNIT
		MIN	MAX	
$t_{d(dataV)}$	Output data rfbi_data[n:0][8] valid	G[7]		ns
$t_{d(Skew)}$	Skew between output write enable falling rfbi_we and output data rfbi_data[n:0][8] high or low	14.3		ns
$t_{R(rfbi\_we)}$	Rise time, output write enable rfbi_we		2	ns
$t_{F(rfbi\_we)}$	Fall time, output write enable rfbi_we		2	ns
$t_{R(rfbi\_a0)}$	Rise time, output command/data control rfbi_a0		2	ns
$t_{F(rfbi\_a0)}$	Fall time, output command/data control rfbi_a0		2	ns
$t_{R(rfbi\_csx)}$	Rise time, output chip select rfbi_cs0		2	ns
$t_{F(rfbi\_csx)}$	Fall time, output chip select rfbi_cs0		2	ns
$t_{R(rfbi\_da)}$	Rise time, output data rfbi_data[n:0][8]		2	ns
$t_{F(rfbi\_da)}$	Fall time, output data rfbi_data[n:0][8]		2	ns

(1) A = (WeCycleTime—WeOffTime) × (TimeParaGranularity + 1) × L3CLK

(2) B = (WeOffTime—WeOntime) × (TimeParaGranularity + 1) × L3CLK

(3) C = (WeOnTime) × (TimeParaGranularity + 1) × L3CLK

(4) D = (WeCycleTime + CsPulseWidth—WeOffTime) × (TimeParaGranularity + 1) × L3CLK

(5) E = (WeOnTime—CsOnTime) × (TimeParaGranularity + 1) × L3CLK

(6) F = (CsOffTime—WeOffTime) × (TimeParaGranularity + 1) × L3CLK

(7) G = (WeCycleTime) × (TimeParaGranularity + 1) × L3CLK

(8) rfbi_data[n:0], n up to 15

(9) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-18. DSS—RFBI Registers Configuration—LCD Panel[1]

DESCRIPTION	REGISTER and BIT FIELD	BIT
CS signal assertion time from start access time	RFBI_ONOFF_TIME and CSONTIME	[3:0]
CS signal de-assertion time from start access time	RFBI_ONOFF_TIME and CSOFFTIME	[9:4]
WE signal assertion time from start access time	RFBI_ONOFF_TIME and WEONTIME	[13:10]
WE signal de-assertion time from start access time	RFBI_ONOFF_TIME and WEOFFTIME	[19:14]
Write cycle time	RFBI_CYCLE_TIME and WECYCLETIME	[5:0]
CS pulse width	RFBI_CYCLE_TIME and CSPULSEWIDTH	[17:12]
Write-to-write CS pulse width enable	RFBI_CYCLE_TIME and WWENABLE	[20]
From start access time to CLK rising edge used for the first data capture	RFBI_CYCLE_TIME and ACCESSTIME	[27:22]
Latencies multiplied by 2	RFBI_CONFIG and TIMEGRANULARITY	[4]

(1) For more information on the RFBI registers, see the Display Subsystem / Remote Frame Buffer Interface section of the OMAP543x TRM.

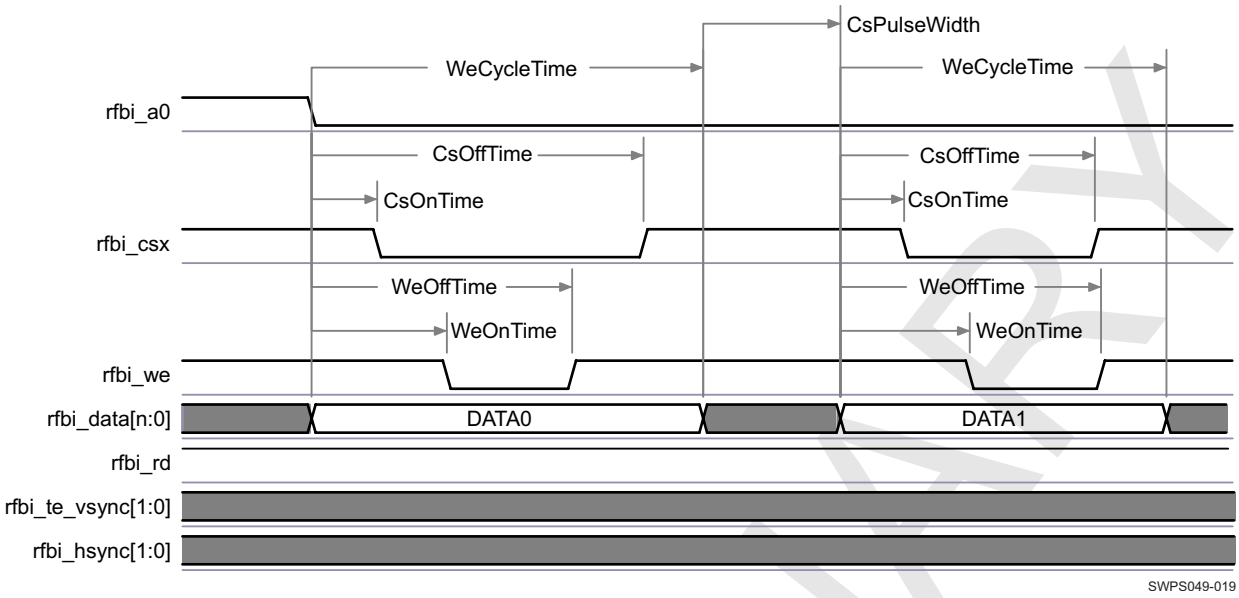


Figure 5-25. DSS—RFBI—Command / Data Write—Pico DLP(1)(2)

(1) In rfbi_csx, x is equal to 0.

(2) rfbi_data[n:0], n up to 15

5.5.2.3 Display Serial Interface—DSI-1 MIPI D-PHY—1.5 V and 1.8 V

The DSI-1 port A and port C (display serial interface) are compliant with the MIPI D-PHY TX specification v1.00.00 and the MIPI DSI v01.01.00 standard and support these features:

- Four data lane complex input or output in addition to the clock lane
- Bidirectional data link support (only one data lane is used in reverse direction in command mode from display to OMAP for status and control)
- Video mode and command mode support
- Data interleaving support

DSI-1 port A and DSI-1 port C interfaces, with 4 data differential lanes plus 1 clock differential lane, in synchronous mode, double data rate, support the following data bit rates:

- @OPP_NOM:
  - 1.255 Gbps ($f_{c(clk)}$ = 627.5 MHz) for each lane.
  - With $t_{UI(NOM)}$ = 0.796 ps, $t_{UI(NOM)}$ is the minimum unit interval, equal to 1 / (2 × $f_{c(clk)}$).
  - With $t_{UI(INST,MIN)}$ = 0.716 ps, $t_{UI(INST,MIN)}$ is the minimum instantaneous bit duration, equal to 0.9 × $t_{UI(NOM)}$.

Each DSI-1 interface supports the following display applications:

- WUXGA (Wide Ultra eXtended Graphics Array), 1920x1200, 60fps, 24bpp
- Up to QSXGA (Quad Super eXtended Graphics Array), 2560x1600, 30fps, 24bpp

5.5.2.4 High Definition Multimedia Interface (HDMI)

NOTE

For more information on HDMI, please contact your TI representative.

5.6 Serial and Parallel Communication Interfaces

5.6.1 Multichannel Buffered Serial Port (McBSP), 1.8 V

NOTE

For more information, see the Serial Communication Interface / Multichannel Buffered Serial Port (McBSP) / McBSP Functional Description section of the OMAP543x TRM.

The multichannel buffered serial port (McBSP) provides a full duplex direct serial interface between OMAP chip and other devices (digital baseband), audio and voice codec, etc. It can accommodate a wide range of peripherals and clocked frame oriented protocols (I2S, PCM, TDM) due to its high level of versatility.

5.6.1.1 McBSP1, McBSP2, and McBSP3—I2S/PCM—1 Peripheral—SDR—12.288 MHz—1.8 V

Table 5-19. McBSP1, McBSP2, and McBSP3 Timing Conditions—I2S/PCM

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	6500	ps
t_F	Input signal fall time	400	6500	ps
Output Condition(1)				

(1) See Table 8-39, *McBSP1 PCB Requirements and IO Programming*, Table 8-41, *McBSP2 PCB Requirements and IO Programming*, and Table 8-43, *McBSP3 PCB Requirements and IO Programming*.

Table 5-20 through Table 5-23 assume testing over the recommended operating conditions and electrical characteristic conditions below.

5.6.1.1.1 McBSP1, McBSP2, and McBSP3—I2S/PCM—Master Mode

Table 5-20. McBSP1, McBSP2, and McBSP3 Timing Requirements—I2S/PCM—Master Mode(1)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM5	$t_{su(drV\text{-}clkAE)}$	Setup time, abemcbspy_dr(2) valid before abemcbspy_clkx(2) active edge	4.6		ns
BM6	$t_{h(clkAE\text{-}drV)}$	Hold time, abemcbspy_dr(2) valid after abemcbspy_clkx(2) active edge	0.7		ns

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr and abemcbspy_clkx, y is equal to 1, 2, or 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-21. McBSP1, McBSP2, and McBSP3 Switching Characteristics—I2S/PCM—Master Mode(3)(5)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM0	$1 / t_{C(clk)}$	Frequency, output abemcbspy_clkx(4) clock		12.288(5)	MHz
BM1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(4) low	0.5 × P(1)		ns
BM2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(4) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(4)		4069	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(4)		527	ps
	$t_{R(clk)}$	Rise time, output abemcbspy_clkx(4)	400	6500	ps

Table 5-21. McBSP1, McBSP2, and McBSP3 Switching Characteristics—I2S/PCM—Master Mode[3][5] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$t_{F(clk)}$	Fall time, output abemcbspy_clkx[4]	400	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abemcbspy_clkx[4] active edge to output abemcbspy_fsx[4] valid	1.1	21.8	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output [4] active edge to output abemcbspy_dx[4] valid	1.1	21.8	ns
	$t_{R(fs)}$	Rise time, output abemcbspy_fsx[4]	400	6500	ps
	$t_{F(fs)}$	Fall time, output abemcbspy_fsx[4]	400	6500	ps
	$t_{R(dx)}$	Rise time, output abemcbspy_dx[4]	400	6500	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx[4]	400	6500	ps

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(4) In abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

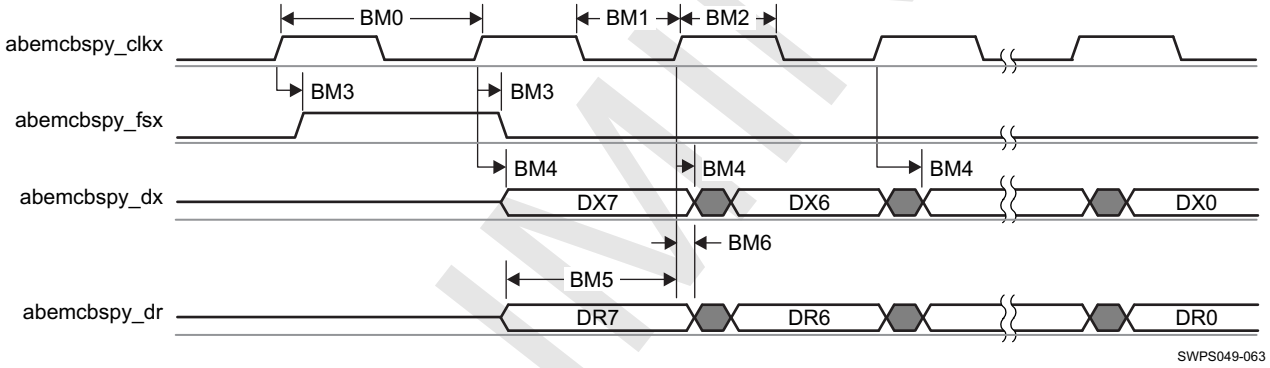


Figure 5-26. McBSP1, McBSP2, and McBSP3—I2S/PCM—Master Mode[1][2][3]

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.

5.6.1.1.2 McBSP1, McBSP2 and McBSP3—I2S/PCM—Slave Mode

Table 5-22. McBSP1, McBSP2, and McBSP3 Timing Requirements—I2S/PCM—Slave Mode(3)(4)(6)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS0	$1 / t_{C(clk)}$	Frequency, input abemcbspy_clkx(5) clock		12.288	MHz
BS1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(5) low	0.5 × P(1)		ns
BS2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(5) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(5)		4069	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(5)		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abemcbspy_fsx(5) valid before abemcbspy_clkx(5) active edge	12.1		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abemcbspy_fsx(5) valid after abemcbspy_clkx(5) active edge	–0.1		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(5) valid before abemcbspy_clkx(5) active edge	12.1		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(5) valid after abemcbspy_clkx(5) active edge	–0.1		ns

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 1, 2, or 3.

(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-23. McBSP1, McBSP2, and McBSP3 Switching Characteristics—I2S/PCM –Slave Mode(1)(2)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abemcbspy_clkx(2) active edge to output abemcbspy_dx(2) valid	1.0	20.7	ns
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(2)	400	6500	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(2)	400	6500	ps

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

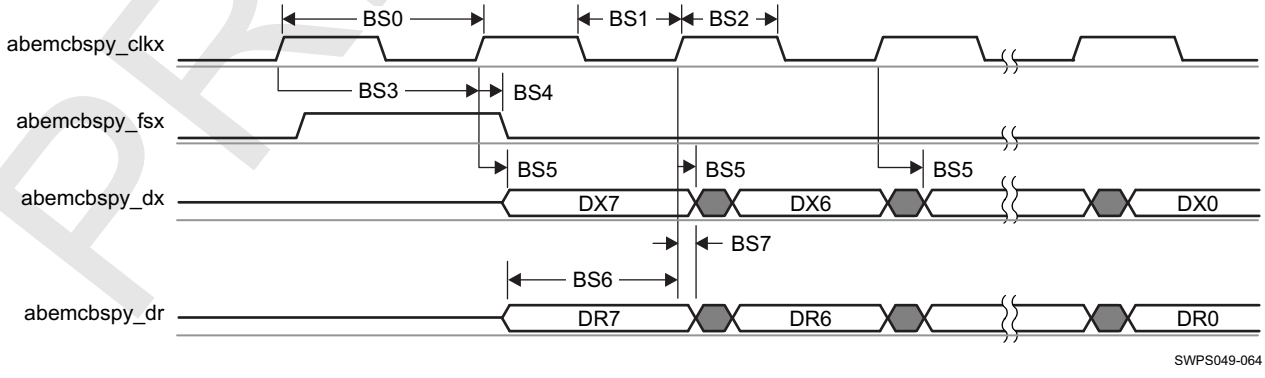


Figure 5-27. McBSP1, McBSP2, and McBSP3—I2S/PCM—Slave Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1, 2, or 3.

5.6.1.2 McBSP2 and McBSP3—I2S/PCM—2 Peripherals—SDR—12.288 MHz—1.8 V

Table 5-24. McBSP2 and McBSP3 Timing Conditions—I2S/PCM

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	6500	ps
t_F	Input signal fall time	400	6500	ps
Output Condition(1)				

(1) See Table 8-41, *McBSP2 PCB Requirements and IO Programming*, and Table 8-43, *McBSP3 PCB Requirements and IO Programming*.

Table 5-25 through Table 5-28 assume testing over the recommended operating conditions and electrical characteristic conditions below.

5.6.1.2.1 McBSP2 and McBSP3—I2S/PCM—Master Mode

Table 5-25. McBSP2 and McBSP3 Timing Requirements—I2S/PCM—Master Mode(1)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(2) valid before abemcbspy_clkx(2) active edge	10.6		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(2) valid after abemcbspy_clkx(2) active edge	–0.1		ns

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr and abemcbspy_clkx, y is equal to 2 or 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-26. McBSP2 and McBSP3 Switching Characteristics—I2S/PCM—Master Mode(3)(5)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM0	$1 / t_{C(clk)}$	Frequency, output abemcbspy_clkx(4) clock		12.288(5)	MHz
BM1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(4) low	0.5 × P(1)		ns
BM2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(4) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(4)		4069	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(4)		527	ps
	$t_{R(clk)}$	Rise time, output abemcbspy_clkx(4)	1000	6500	ps
	$t_{F(clk)}$	Fall time, output abemcbspy_clkx(4)	1000	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abemcbspy_clkx(4) active edge to output abemcbspy_fsx(4) valid	1.6	21.4	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output (4) active edge to output abemcbspy_dx(4) valid	1.6	21.4	ns
	$t_{R(fs)}$	Rise time, output abemcbspy_fsx(4)	1000	6500	ps
	$t_{F(fs)}$	Fall time, output abemcbspy_fsx(4)	1000	6500	ps
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(4)	1000	6500	ps

Table 5-26. McBSP2 and McBSP3 Switching Characteristics—I2S/PCM—Master Mode[3][5] (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$t_{F(dx)}$	Fall time, output abemcbspy_dx[4]	1000	6500	ps

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(4) In abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

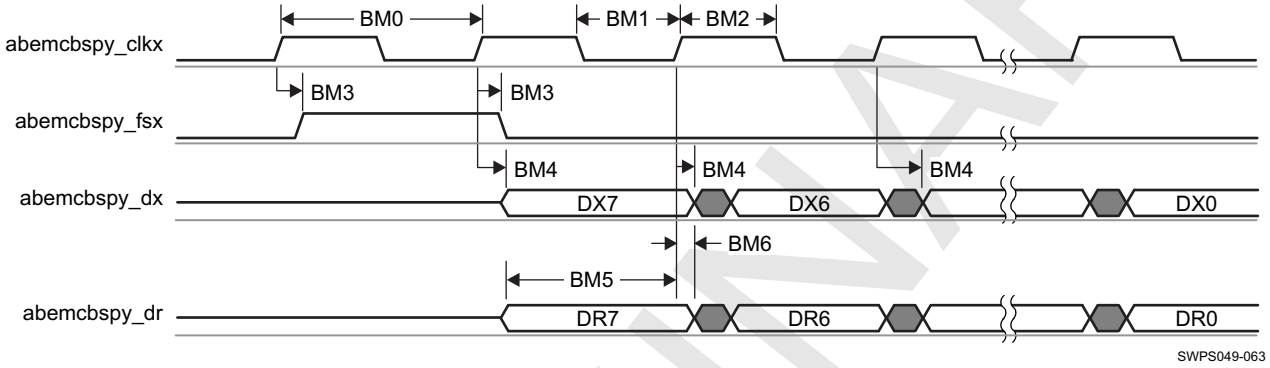


Figure 5-28. McBSP2 and McBSP3—I2S/PCM—Master Mode[1][2][3]

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

5.6.1.2.2 McBSP2 and McBSP3—I2S/PCM —Slave Mode

Table 5-27. McBSP2 and McBSP3 Timing Requirements—I2S/PCM—Slave Mode[3][4][6]

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS0	$1 / t_{C(clk)}$	Frequency, input abemcbspy_clkx[5] clock		12.288	MHz
BS1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx[5] low	0.5 × P[1]		ns
BS2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx[5] high	0.5 × P[1]		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx[5]		4069	ps
	$t_{J(clk)}$	Jitter standard deviation[2], output abemcbspy_clkx[5]		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abemcbspy_fsx[5] valid before abemcbspy_clkx[5] active edge	11.8		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abemcbspy_fsx[5] valid after abemcbspy_clkx[5] active edge	–0.5		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr[5] valid before abemcbspy_clkx[5] active edge	11.8		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr[5] valid after abemcbspy_clkx[5] active edge	–0.5		ns

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 2 or 3.

(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-28. McBSP2 and McBSP3 Switching Characteristics—I2S/PCM –Slave Mode(1)(2) (3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abemcbspy_clkx(2) active edge to output abemcbspy_dx(2) valid	1.1	18.9	ns
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(2)	400	6500	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(2)	400	6500	ps

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

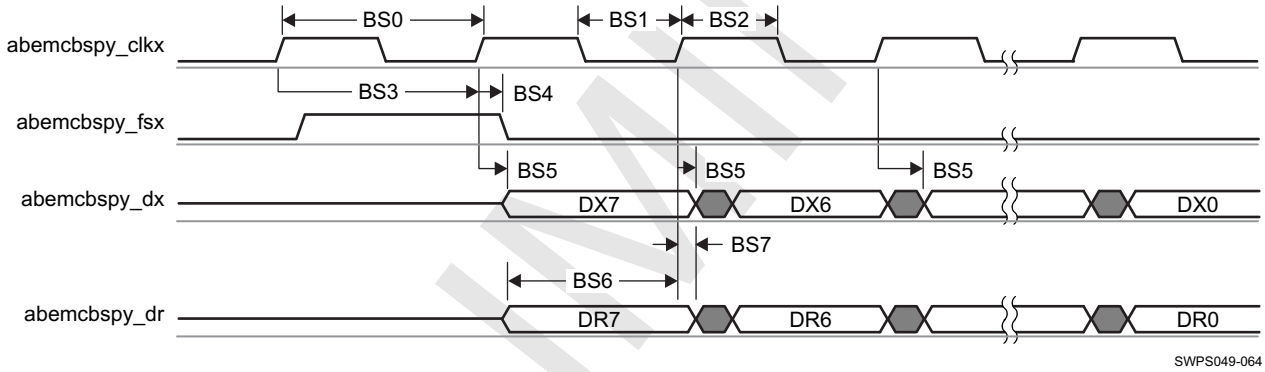


Figure 5-29. McBSP2 and McBSP3—I2S/PCM—Slave Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

5.6.1.3 McBSP1—TDM—5 Peripherals—SDR—6.144 MHz—1.8 V

Table 5-29. McBSP1Timing Conditions—TDM

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	17700	ps
t_F	Input signal fall time	1000	17700	ps
Output Condition(1)				

(1) See Table 8-39, *McBSP1 PCB Requirements and IO Programming*.

5.6.1.3.1 McBSP1—TDM—Master Mode

Table 5-30 through Table 5-33 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-30. McBSP1 Timing Requirements—TDM—Master Mode(1)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(2) valid before abemcbspy_clkx(2) active edge	19.5		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(2) valid after abemcbspy_clkx(2) active edge	–1.1		ns

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr and abemcbspy_clkx, y is equal to 1.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-31. McBSP1 Switching Characteristics—TDM –Master Mode(3)(5)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM0	1 / $t_{C(clk)}$	Frequency, output abemcbspy_clkx(4) clock		6.144(5)	MHz
BM1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(4) low	0.5 × P(1)		ns
BM2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(4) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(4)		8138	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(4)		65	ps
	$t_{R(clk)}$	Rise time, output abemcbspy_clkx(4)	1000	17700	ps
	$t_{F(clk)}$	Fall time, output abemcbspy_clkx(4)	1000	17700	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abemcbspy_clkx(4) active edge to output abemcbspy_fsx(4) valid	2.1	45.7	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output (4) active edge to output abemcbspy_dx(4) valid	2.1	45.7	ns
	$t_{R(fs)}$	Rise time, output abemcbspy_fsx(4)	1000	17700	ps
	$t_{F(fs)}$	Fall time, output abemcbspy_fsx(4)	1000	17700	ps
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(4)	1000	17700	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(4)	1000	17700	ps

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(4) In abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

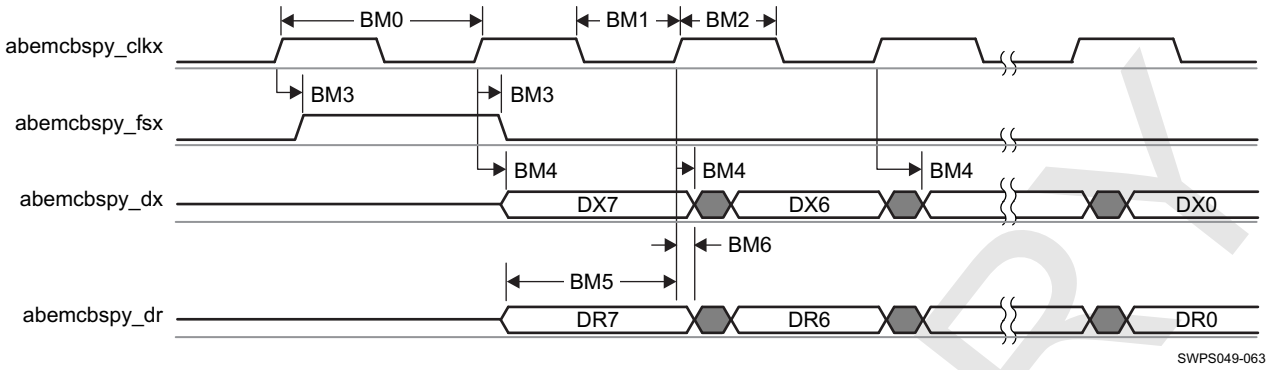


Figure 5-30. McBSP1—TDM—Master Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

5.6.1.3.2 McBSP1—TDM—Slave Mode

Table 5-32. McBSP1 Timing Requirements—TDM—Slave Mode(3)(4)(6)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS0	$1 / t_{C(clk)}$	Frequency, input abemcbspy_clkx(5) clock		6.144	MHz
BS1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(5) low	0.5 × P(1)		
BS2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(5) high	0.5 × P(1)		
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(5)		8138	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(5)		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abemcbspy_fsx(5) valid before abemcbspy_clkx(5) active edge	25.7		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abemcbspy_fsx(5) valid after abemcbspy_clkx(5) active edge	–0.8		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(5) valid before abemcbspy_clkx(5) active edge	25.7		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(5) valid after abemcbspy_clkx(5) active edge	–0.8		ns

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 1.

(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-33. McBSP1 Switching Characteristics—TDM—Slave Mode(1)(2)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abemcbspy_clkx(2) active edge to output abemcbspy_dx(2) valid	5.2	24.4	ns
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(2)	1000	17700	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(2)	1000	17700	ps

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

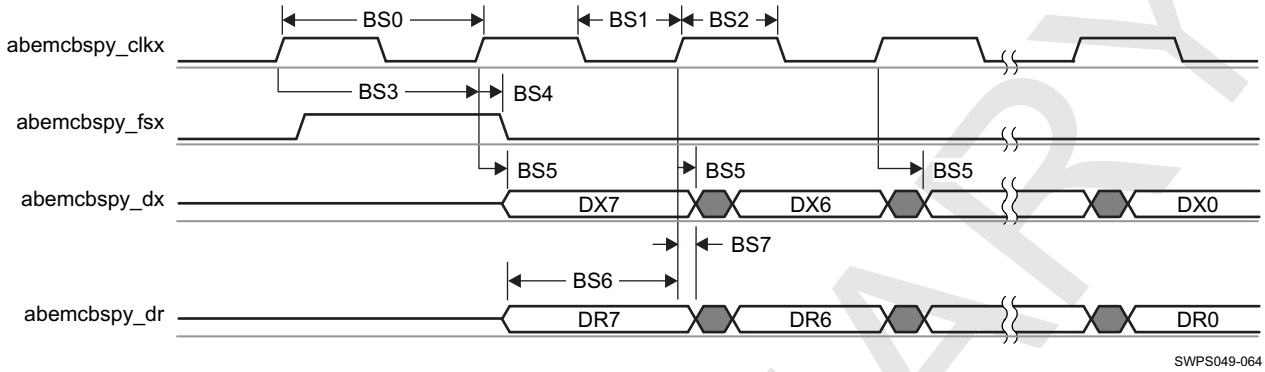


Figure 5-31. McBSP1—TDM—Slave Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

5.6.1.4 McBSP2 and McBSP3—TDM—1 Peripheral —SDR—12.288 MHz—1.8 V

Table 5-34. McBSP2 and McBSP3 Timing Conditions—TDM

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	600	6500	ps
t_F	Input signal fall time	600	6500	ps
Output Condition(1)				

(1) See Table 8-41, *McBSP2 PCB Requirements and IO Programming*, and Table 8-43, *McBSP3 PCB Requirements and IO Programming*.

Table 5-35 through Table 5-38 assume testing over the recommended operating conditions and electrical characteristic conditions below.

5.6.1.4.1 McBSP2 and McBSP3—TDM—Master Mode

Table 5-35. McBSP2 and McBSP3 Timing Requirements—TDM—Master Mode(1)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM5	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(2) valid before abemcbspy_clkx(2) active edge	8.6		ns
BM6	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(2) valid after abemcbspy_clkx(2) active edge	0.8		ns

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr and abemcbspy_clkx, y is equal to 2 or 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-36. McBSP2 and McBSP3 Switching Characteristics—TDM—Master Mode(3)(5)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BM0	$1 / t_{C(clk)}$	Frequency, output abemcbspy_clkx(4) clock		12.288(5)	MHz
BM1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(4) low	0.5 × P(1)		ns
BM2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(4) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(4)		4069	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(4)		658	ps
	$t_{R(clk)}$	Rise time, output abemcbspy_clkx(4)	600	6500	ps
	$t_{F(clk)}$	Fall time, output abemcbspy_clkx(4)	600	6500	ps
BM3	$t_{d(clkAE-fsV)}$	Delay time, output abemcbspy_clkx(4) active edge to output abemcbspy_fsx(4) valid	1.3	19.9	ns
BM4	$t_{d(clkxAE-dxV)}$	Delay time, output (4) active edge to output abemcbspy_dx(4) valid	1.3	19.9	ns
	$t_{R(fs)}$	Rise time, output abemcbspy_fsx(4)	600	6500	ps
	$t_{F(fs)}$	Fall time, output abemcbspy_fsx(4)	600	6500	ps
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(4)	600	6500	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(4)	600	6500	ps

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(4) In abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

(5) See DM Operating Condition Addendum for CORE OPP voltages.

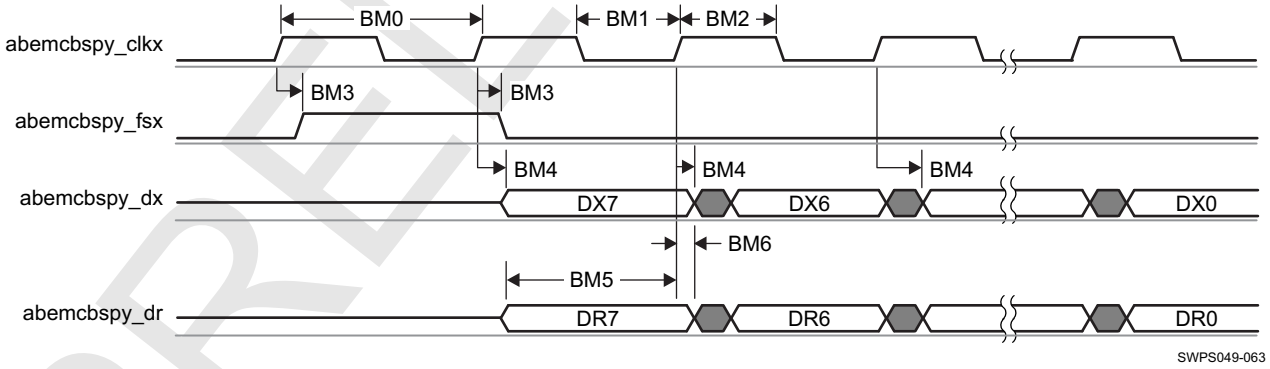


Figure 5-32. McBSP2 and McBSP3—TDM—Master Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

5.6.1.4.2 McBSP2 and McBSP3—TDM—Slave Mode

Table 5-37. McBSP2 and McBSP3 Timing Requirements—TDM—Slave Mode(3)(4)(6)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS0	$1 / t_{C(clk)}$	Frequency, input abemcbspy_clkx(5) clock		12.288	MHz
BS1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(5) low	0.5 × P(1)		ns
BS2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(5) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(5)		4069	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(5)		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abemcbspy_fsx(5) valid before abemcbspy_clkx(5) active edge	12.0		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abemcbspy_fsx(5) valid after abemcbspy_clkx(5) active edge	0.1		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(5) valid before abemcbspy_clkx(5) active edge	12.0		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(5) valid after abemcbspy_clkx(5) active edge	0.7		ns

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 2 or 3.

(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-38. McBSP2 and McBSP3 Switching Characteristics—TDM—Slave Mode(1)(2)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abemcbspy_clkx(2) active edge to output abemcbspy_dx(2) valid	1.3	16.8	ns
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(2)	600	6500	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(2)	600	6500	ps

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

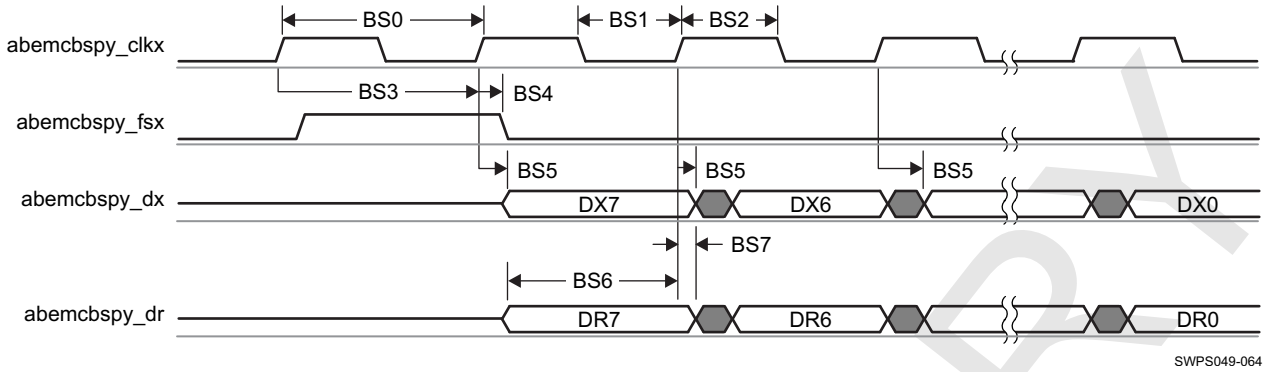


Figure 5-33. McBSP2 and McBSP3—TDM—Slave Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 2 or 3.

5.6.1.5 McBSP1—TDM—1 Peripheral—SDR—49.125 MHz—1.8 V

Table 5-39. McBSP1 Timing Conditions—TDM

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	400	6500	ps
t_F	Input signal fall time	400	6500	ps
Output Condition(1)				

(1) See Table 8-39, *McBSP1 PCB Requirements and IO Programming*.

Table 5-40 and Table 5-41 assume testing over the recommended operating conditions and electrical characteristic conditions below.

5.6.1.5.1 McBSP1—TDM—Slave Mode

Table 5-40. McBSP1 Timing Requirements—TDM—Slave Mode(3)(4)(6)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS0	$1 / t_{C(clk)}$	Frequency, input abemcbspy_clkx(5) clock		49.125	MHz
BS1	$t_{W(clkL)}$	Typical pulse duration, output abemcbspy_clkx(5) low	0.5 × P(1)		ns
BS2	$t_{W(clkH)}$	Typical pulse duration, output abemcbspy_clkx(5) high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcbspy_clkx(5)		8138	ps
	$t_{J(clk)}$	Jitter standard deviation(2), output abemcbspy_clkx(5)		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abemcbspy_fsx(5) valid before abemcbspy_clkx(5) active edge	–34.1		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abemcbspy_fsx(5) valid after abemcbspy_clkx(5) active edge	–34.1		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abemcbspy_dr(5) valid before abemcbspy_clkx(5) active edge	–34.1		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abemcbspy_dr(5) valid after abemcbspy_clkx(5) active edge	–34.1		ns

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(5) In abemcbspy_dr, abemcbspy_clkx, and abemcbspy_fsx, y is equal to 1.

(6) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-41. McBSP1 Switching Characteristics—TDM—Slave Mode(1)(2)(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS5	$t_{d(clkxAE-dxV)}$	Delay time, input abemcbspy_clkx(2) active edge to output abemcbspy_dx(2) valid	31.1	–49.1	ns
	$t_{R(dx)}$	Rise time, output abemcbspy_dx(2)	400	6500	ps
	$t_{F(dx)}$	Fall time, output abemcbspy_dx(2)	400	6500	ps

(1) The timings apply to all configurations regardless of abemcbspy_clkx polarity and which clock edges are used to drive output data and capture input data.

(2) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

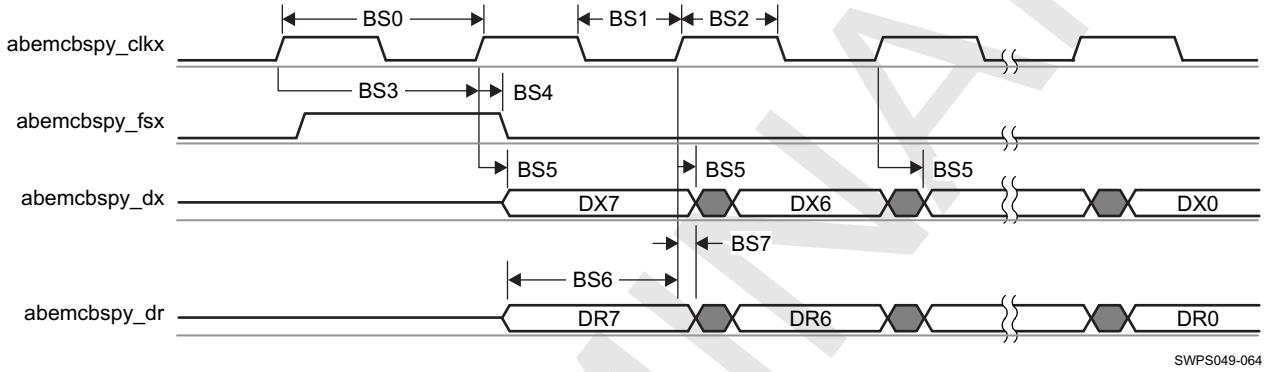


Figure 5-34. McBSP1—TDM—Slave Mode(1)(2)(3)

(1) The polarity of McBSP frame synchronization is software configurable.

(2) The active clock edge selection of abemcbspy_clkx (rising or falling) on which abemcbspy_dx data is latched and abemcbspy_dr data is sampled is software configurable.

(3) In abemcbspy_dr, abemcbspy_clkx, abemcbspy_fsx, and abemcbspy_dx, y is equal to 1.

5.6.2 Multichannel Audio Serial Port (McASP), 1.8 V

NOTE

For more information, see the Serial Communication Interface section of the OMAP543x TRM.

5.6.2.1 McASP – I2S - 1 Peripheral – SDR – 12.288 MHz – 1.8 V

Table 5-42. McASP Timing Conditions – I2S

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	5000	ps
t_F	Input signal fall time	1000	5000	ps
Output Condition (1)				

(1) See Table 8-49.

5.6.2.1.1 McASP—I2S—Slave Mode

Table 5-43 assumes testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-43. McASP Timing Requirements – I2S– Slave Mode (3)(4)(7)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
BS0	$1 / t_{C(clk)}$	Frequency, input abemcasp_aclk(5) clock		12.288	MHz
BS1	$t_{W(clkL)}$	Typical Pulse duration, abemcasp_aclk(5) low	0.5 × P(1)		
BS2	$t_{W(clkH)}$	Typical Pulse duration, abemcasp_aclk(5) high	0.5 × P(1)		
	$t_{dc(clk)}$	Duty cycle error, abemcasp_aclk(5)		8138	ps
	$t_{J(clk)}$	Cycle jitter(2), abemcasp_aclk(5)		2000	ps
BS3	$t_{su(fsV-clkAE)}$	Setup time, abemcasp_afs(6) valid before abemcasp_aclk(5) active edge	14.3		ns
BS4	$t_{h(clkAE-fsV)}$	Hold time, abemcasp_afs(6) valid after abemcasp_aclk(5) active edge	–0.3		ns
BS6	$t_{su(drV-clkAE)}$	Setup time, abemcasp_axr valid before abemcasp_aclk(5) active edge	14.3		ns
BS7	$t_{h(clkAE-drV)}$	Hold time, abemcasp_axr valid after abemcasp_aclk(5) active edge	–0.3		ns

(1) P = abemcasp_aclkx / abemcasp_aclkr period in ns

(2) Maximum cycle jitter supported by abemcasp_aclkx / abemcasp_aclkr input clock

(3) The timing requirements are guaranteed till the cycle jitter and duty cycle error conditions specified.

(4) The timings apply to all configurations regardless of abemcasp_aclk polarity and which clock edges are used to drive output data and capture input data.

(5) abemcasp_aclk corresponds to either abemcasp_aclkx or abemcasp_aclkr; abemcasp_aclkr is available in 6-pins mode only

(6) abemcasp_afs corresponds to either abemcasp_afsx or abemcasp_afsr; abemcasp_afsr is available in 6-pins mode only

(7) See DM Operating Condition Addendum for CORE OPP voltages.

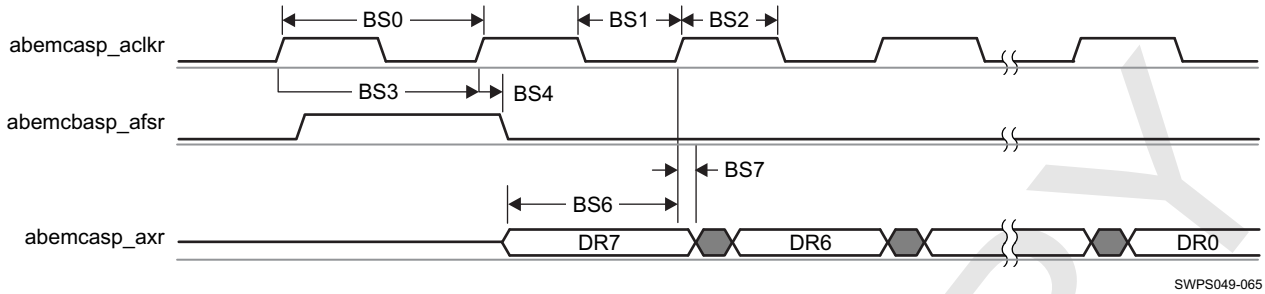


Figure 5-35. McASP – I2S – Slave Mode

5.6.3 Multichannel Serial Port Interface (McSPI), 1.8 V

NOTE

For more information, see the Serial Communication Interface section of the OMAP543x TRM.

McSPI allows a duplex, synchronous, serial communication between a local host and SPI compliant external devices.

5.6.3.1 McSPI1, McSPI2 and McSPI4 – 1 Peripheral – SDR – Master – 48 MHz

Table 5-44. McSPI1, McSPI2 and McSPI4 Timing Conditions – Master Mode – 48 MHz

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	100	4000	ps
t_F	Input signal fall time	100	4000	ps
Output Condition (1)				

(1) See Table 8-17, Table 8-19, and Table 8-43.

Table 5-45 and Table 5-46 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-45. McSPI1, McSPI2 and McSPI4 Timing Requirements – Master Mode – 48 MHz (3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspix_somi(2) valid before mcspix_clk(1)(2) active edge	4.59		ns
SM5	$t_{h(CLKAE-SOMI)}$	Hold time, mcspix_somi(2) valid after mcspix_clk(1)(2) active edge	3.43		ns

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 1, 2 or 4.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-46. McSPI1, McSPI2 and McSPI4 Switching Requirements – Master Mode – 48 MHz (10)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SM1	1 / $t_{C(CLK)}$	Frequency(2), mcspix_clk(1)(8)		48	MHz
SM2	$t_{W(CLKL)}$	Typical Pulse duration, mcspix_clk(4)(8) low	0.5*P(2)		ns

Table 5-46. McSPI1, McSPI2 and McSPI4 Switching Requirements – Master Mode – 48 MHz (10) (continued)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
SM3	$t_{W(CLKH)}$	Typical Pulse duration, mcspix_clk(4)(8) high		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk(8)			1042	ps
	$t_{J(clk)}$	Jitter standard deviation(3), mcspix_clk(8)			65	ps
	$t_{R(clk)}$	Rise time, mcspix_clk(8)			1928.3	ps
	$t_{F(clk)}$	Fall time, mcspix_clk(8)			1877.1	ps
SM6	$t_{d(CLK-SIMO)}$	Delay time, mcspix_clk(4)(8) active edge to mcspix_simo(8) transition		-2.43	3.63	ns
SM7	$t_{d9CS-SIMO)}$	Delay time, mcspix_cs(9) active edge to mcspix_simo(8) transition	PHA=0 (7)		3.63	ns
SM8	$t_{d(CS-CLK)}$	Delay time, mcspix_cs(9) active to mcspix_clk(4) first edge	PHA=1 (7)	A(5)-3.63		ns
			PHA=0 (7)	B(6)-3.63		ns
SM9	$t_{d(CLK-CS)}$	Delay time, mcspix_clk(4)(8) last edge to mcspix_cs(9) inactive	PHA=1 (7)	B(6)-2.43		ns
			PHA=0 (7)	A(5)-2.43		ns
	$t_{R(SIMO)}$	Rise time, mcspix_simo(8)			1928.3	ps
	$t_{F(SIMO)}$	Fall time, mcspix_simo(8)			1877.1	ps
	$t_{R(CS)}$	Rise time, mcspix_cs(9)			1928.3	ps
	$t_{F(CS)}$	Fall time, mcspix_cs(9)(9)			1877.1	ps

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF .For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP543x TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case 1/P = 48MHz:
- A=(TCS+1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of OMAP543x TRM.

(6) B = (TCS+0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even = 2).
For more information, see the McSPI chapter of OMAP543x TRM.

(7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.

(8) In mcspix_clk, mcspix_simo, x is equal to 1, 2 or 4.

(9) mcspix_cs is equal to mcspi1_cs[3:0], mcspi2_cs[1:0] or mcspi4_cs0

(10) See DM Operating Condition Addendum for CORE OPP voltages.

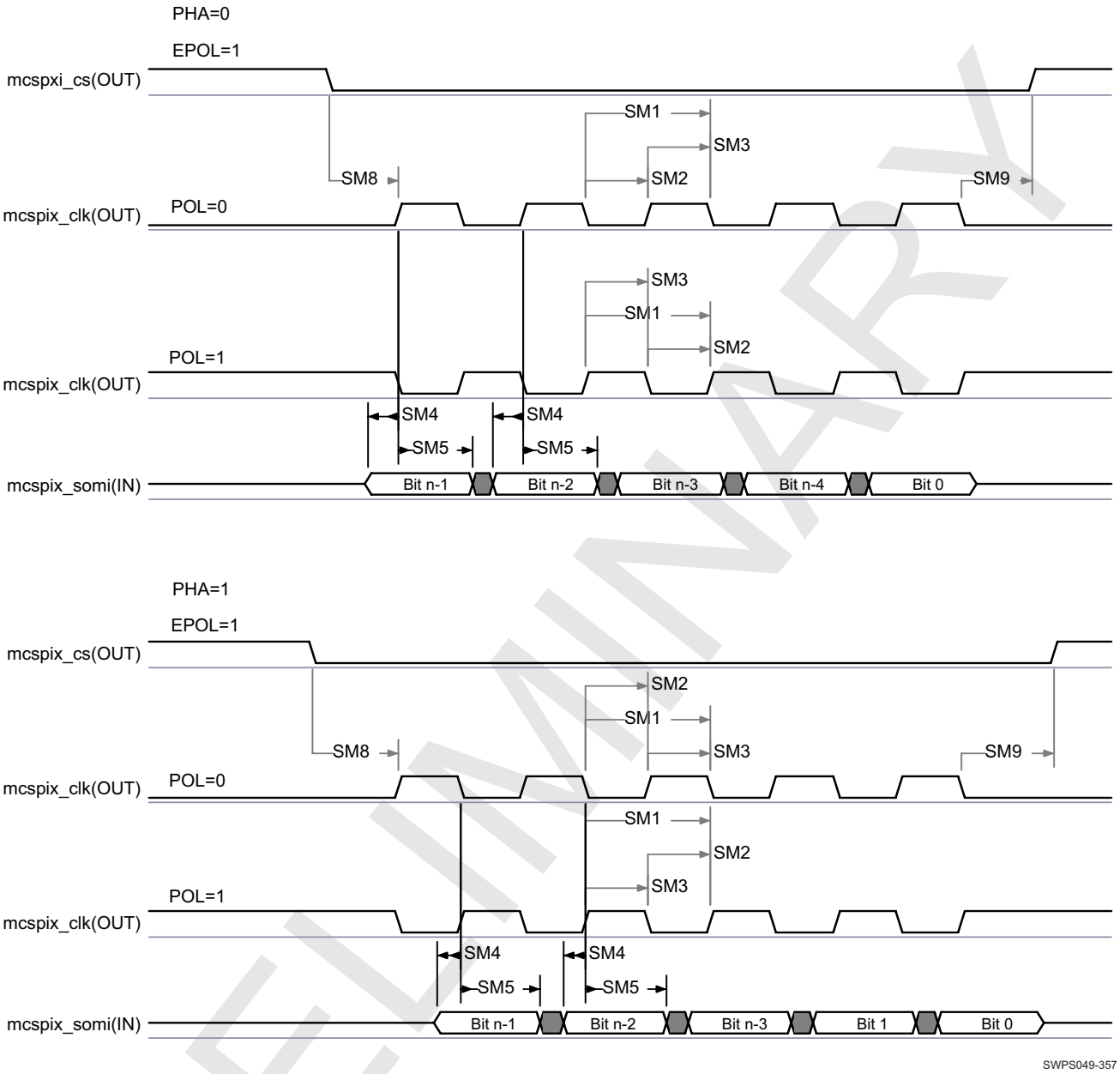


Figure 5-36. McSPI1, McSPI2 and McSPI4 – Master Mode Receive (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_simo, x is equal to 1, 2 or 4.

(4) mcspix_cs is equal to mcspi1_cs[3:0], mcspi2_cs[1:0] or mcspi4_cs0

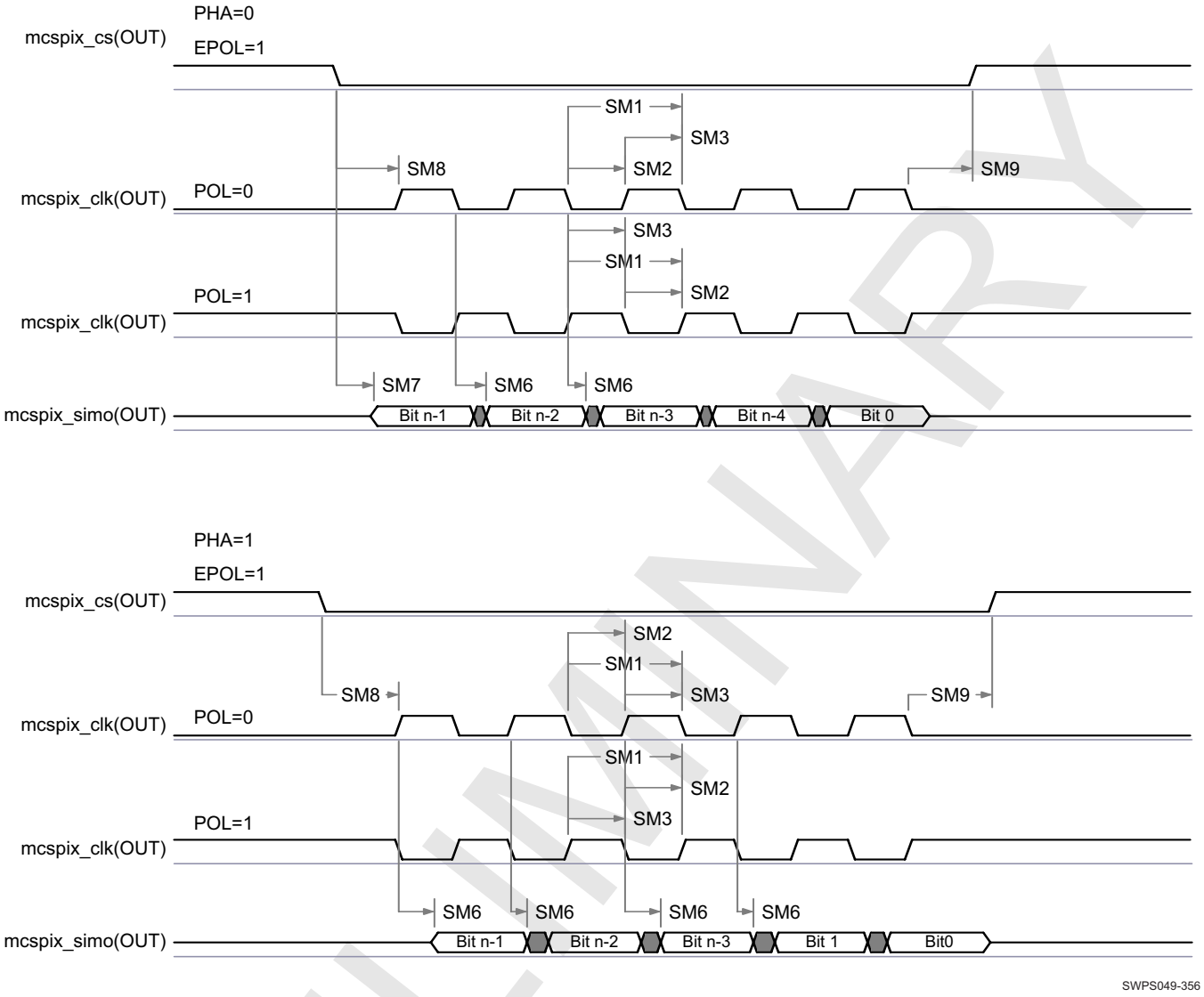


Figure 5-37. , McSPI2 and McSPI4 – Master Mode Transmit [(1)(2)(3)(4)]

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_simo, x is equal to 1, 2 or 4.

(4) mcspix_cs is equal to mcspi1_cs[3:0], mcspi2_cs[1:0] or mcspi4_cs0

5.6.3.2 McSPI3 – 1 Peripheral – SDR – Master – 48 MHz

Table 5-47. McSPI3 Timing Conditions – Master Mode – 48 MHz

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1000	4000	ps
t_F	Input signal fall time	1000	4000	ps
Output Condition[(1)]				

(1) See Table 8-21.

Table 5-48. McSPI3 Timing Requirements – Master Mode – 48 MHz (3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspix_somi(2) valid before mcspix_clk(1)(2)active edge	2.52		ns
SM5	$t_{h(CLKAE-SOMI)}$	Hold time, mcspix_somi(2) valid after mcspix_clk(1)(2) active edge	3.43		ns

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 3.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-49. McSPI3 Switching Requirements – Master Mode – 48 Mhz (10)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
SM1	1 / $t_{C(CLK)}$	Frequency(2), mcspix_clk(1) (8)			48	MHz
SM2	$t_{W(CLKL)}$	Typical Pulse duration, mcspix_clk(4) low		0.5*P(2)		ns
SM3 (8)	$t_{W(CLKH)}$	Typical Pulse duration, mcspix_clk(4)(8) high		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk(8)			1042	ps
	$t_{J(clk)}$	Jitter standard deviation(3), mcspix_clk(8)			65	ps
	$t_{R(clk)}$	Rise time, mcspix_clk(8)			4000.0	ps
	$t_{F(clk)}$	Fall time, mcspix_clk(8)			4000.0	ps
SM6	$t_{d(CLK-SIMO)}$	Delay time, mcspix_clk(4)(8) active edge to mcspix_simo(8) transition		-3.59	3.63	ns
SM7	$t_{d9CS-SIMO)}$	Delay time, mcspix_cs(9) active edge to mcspix_simo(8) transition	PHA=0 (7)	3.63	3.63	ns
SM8	$t_{d(CS-CLK)}$	Delay time, mcspix_cs(9) active to mcspix_clk(4) first edge	PHA=1 (7)	A(5)- 4.25		ns
			PHA=0 (7)	B(6)- 4.25		ns
SM9	$t_{d(CLK-CS)}$	Delay time, mcspix_clk(4)(8)last edge to mcspix_cs(9) inactive	PHA=1 (7)	B(6)- 4.22		ns
			PHA=0 (7)	A(5)- 4.22		ns
	$t_{R(SIMO)}$	Rise time, mcspix_simo(8)			4000.0	ps
	$t_{F(SIMO)}$	Fall time, mcspix_simo(8)			4000.0	ps
	$t_{R(CS)}$	Rise time, mcspix_cs(9)			4000.0	ps
	$t_{F(CS)}$	Fall time, mcspix_cs(9)			4000.0	ps

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF. For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP543x TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case 1/P = 48MHz:
- A=(TCS+1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of OMAP543x TRM.

(6) B = (TCS+0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even = 2).
For more information, see the McSPI chapter of OMAP543x TRM.

(7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.

(8) In mcspix_clk, mcspix_simo, x is equal to 3.

(9) mcspix_cs is equal to mcspi3_cs0

(10) See DM Operating Condition Addendum for CORE OPP voltages.

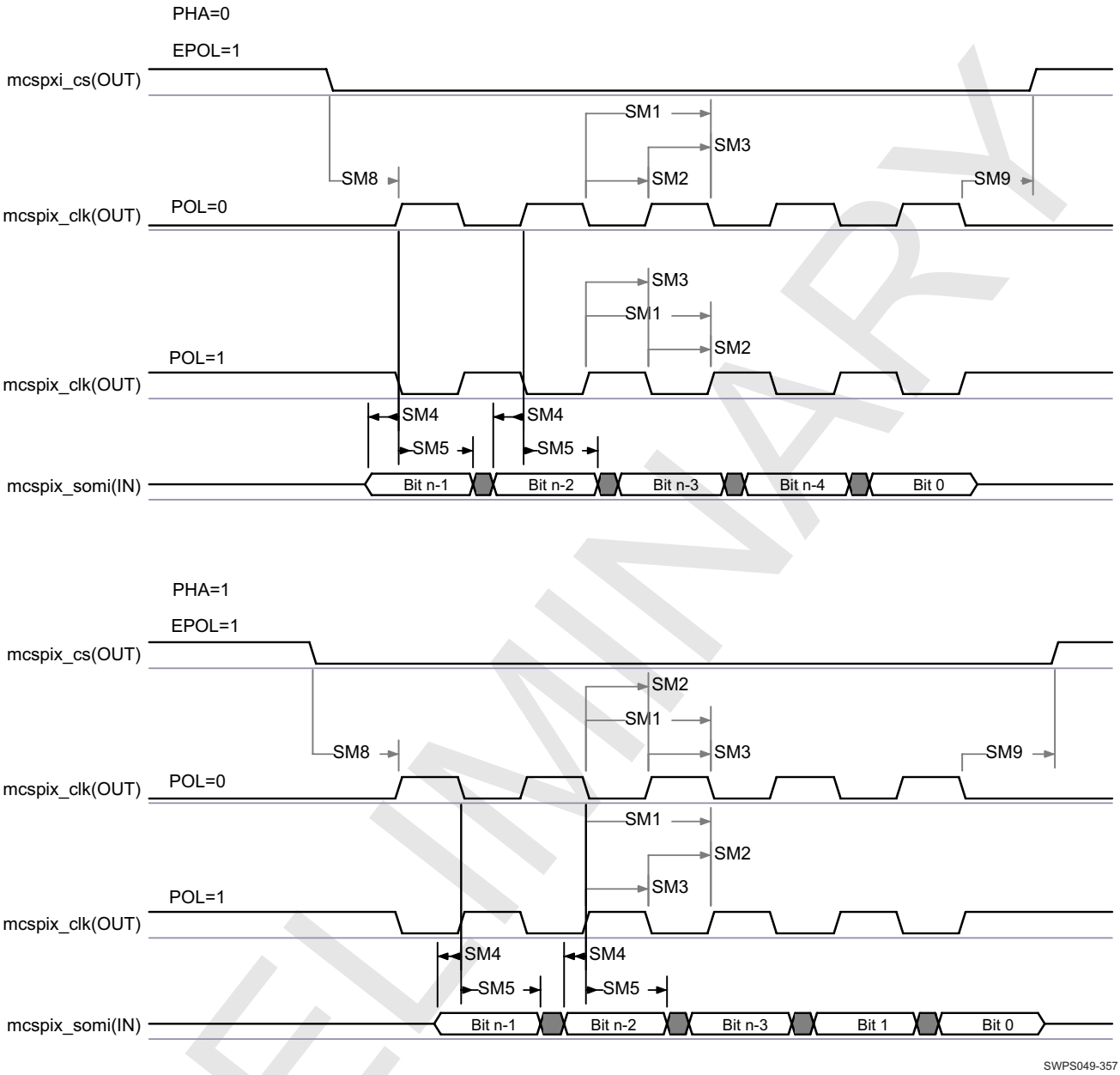


Figure 5-38. McSPI3 – Master Mode Receive (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_somi, x is equal to 3

(4) mcspix_cs is equal to mcspi3_cs0

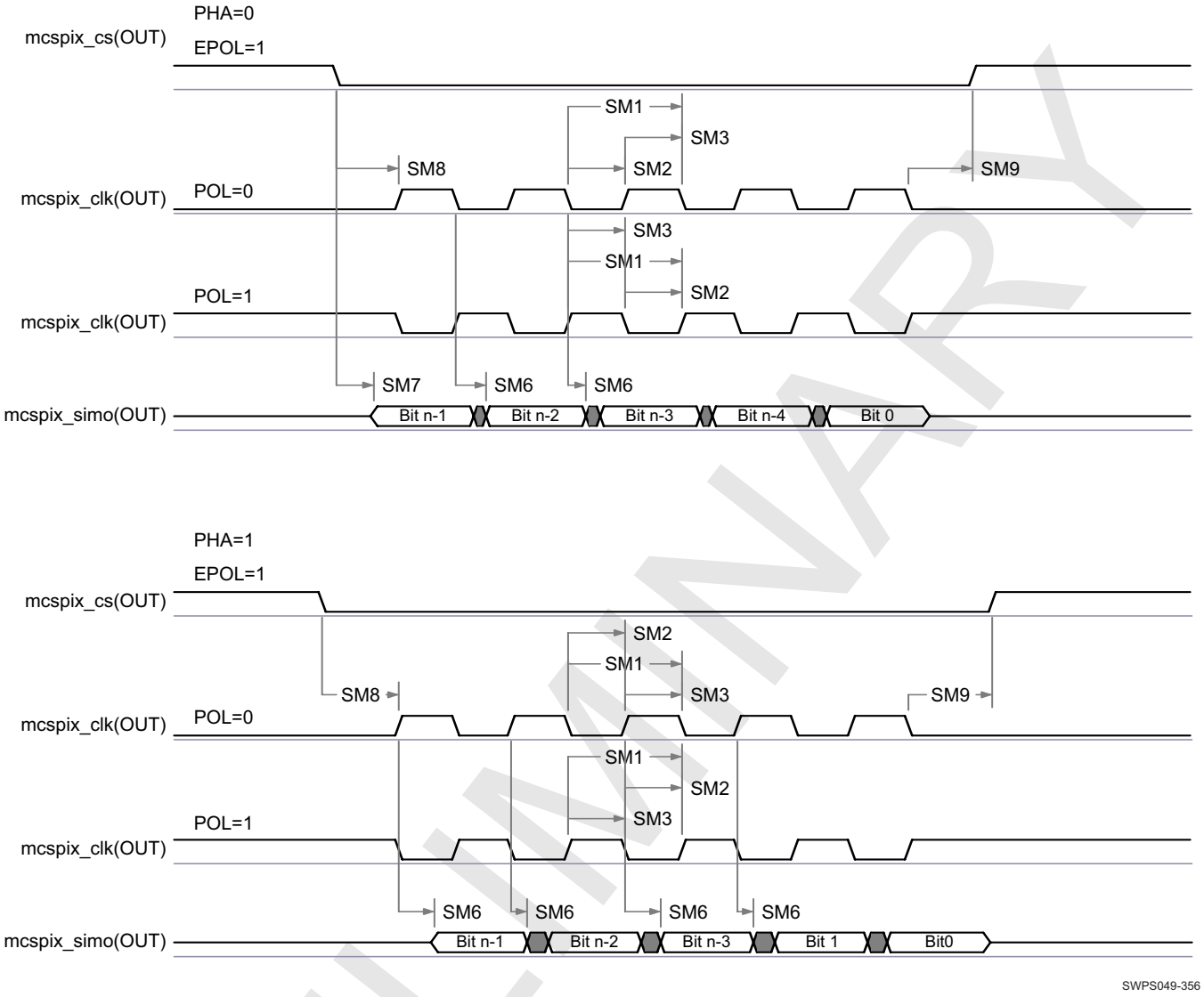


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Figure 5-39. McSPI3 – Master Mode Transmit (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_somi, x is equal to 3

(4) mcspix_cs is equal to mcspi3_cs0

5.6.3.3 McSPI1 and McSPI2 – 2 Peripherals – SDR – Master – 24 MHz

Table 5-50. McSPI1 and McSPI2 Timing Conditions – Master Mode – 24 MHz

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	100	7500	ps
t_F	Input signal fall time	100	7500	ps
Output Condition(1)				

(1) See Table 8-41 and Table 8-43.

Table 5-51 and Table 5-52 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-51. McSPI1 and McSPI2 Timing Requirements – Master Mode – 24 MHz (3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspix_somi(2) valid before mcspix_clk(1)(2) active edge	2.47		ns
SM5	$t_{h(CLKAE-SOMI)}$	Hold time, mcspix_somi(2) valid after mcspix_clk(1)(2) active edge	2.17		ns

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 1 or 2.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-52. Table 5-9: McSPI1 and McSPI2 Switching Requirements – Master Mode – 24 MHz (10)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
SM1	1 / $t_{C(CLK)}$	Frequency(2), mcspix_clk (1)(8)			24	MHz
SM2	$t_{W(CLKL)}$	Typical Pulse duration, mcspix_clk(4)(8) low		0.5*P(2)		ns
SM3	$t_{W(CLKH)}$	Typical Pulse duration, mcspix_clk(4)(8) high		0.5*P(2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk(8)			2083	ps
	$t_{J(clk)}$	Jitter standard deviation(3), mcspix_clk(8)			65	ps
	$t_{R(clk)}$	Rise time, mcspix_clk(8)			5542	ps
	$t_{F(clk)}$	Fall time, mcspix_clk(8)			5083	ps
SM6	$t_{d(CLK-SIMO)}$	Delay time, mcspix_clk(4)(8) active edge to mcspix_simo(8) transition		-4.59	4.59	ns
SM7	$t_{d9CS-SIMO)}$	Delay time, mcspix_cs (9) active edge to mcspix_simo(8) transition	PHA=0 (7)	4.59	3.63	ns
SM8	$t_{d(CS-CLK)}$	Delay time, mcspix_cs (9) active to mcspix_clk(4) first edge	PHA=1 (7)	A(5) - 2.5		ns
			PHA=0 (7)	B(6)- 2.5		ns
SM9	$t_{d(CLK-CS)}$	Delay time, mcspix_clk(4)(8) last edge to mcspix_cs(9) inactive	PHA=1 (7)	B(6) - 2.57		ns
			PHA=0 (7)	A(5) - 2.57		ns
	$t_{R(SIMO)}$	Rise time, mcspix_simo(8)			5542	ps
	$t_{F(SIMO)}$	Fall time, mcspix_simo(8)			5083	ps
	$t_{R(CS)}$	Rise time, mcspix_cs(9)			5542	ps
	$t_{F(CS)}$	Fall time, mcspix_cs(9)			5083	ps

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP543x TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case 1/P = 48MHz:
- A=(TCS+1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of OMAP543x TRM.

(6) B = (TCS+0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, FRATIO: Even = 2).
For more information, see the McSPI chapter of OMAP543x TRM.

(7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.

(8) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.

(9) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0].

(10) See DM Operating Condition Addendum for CORE OPP voltages.

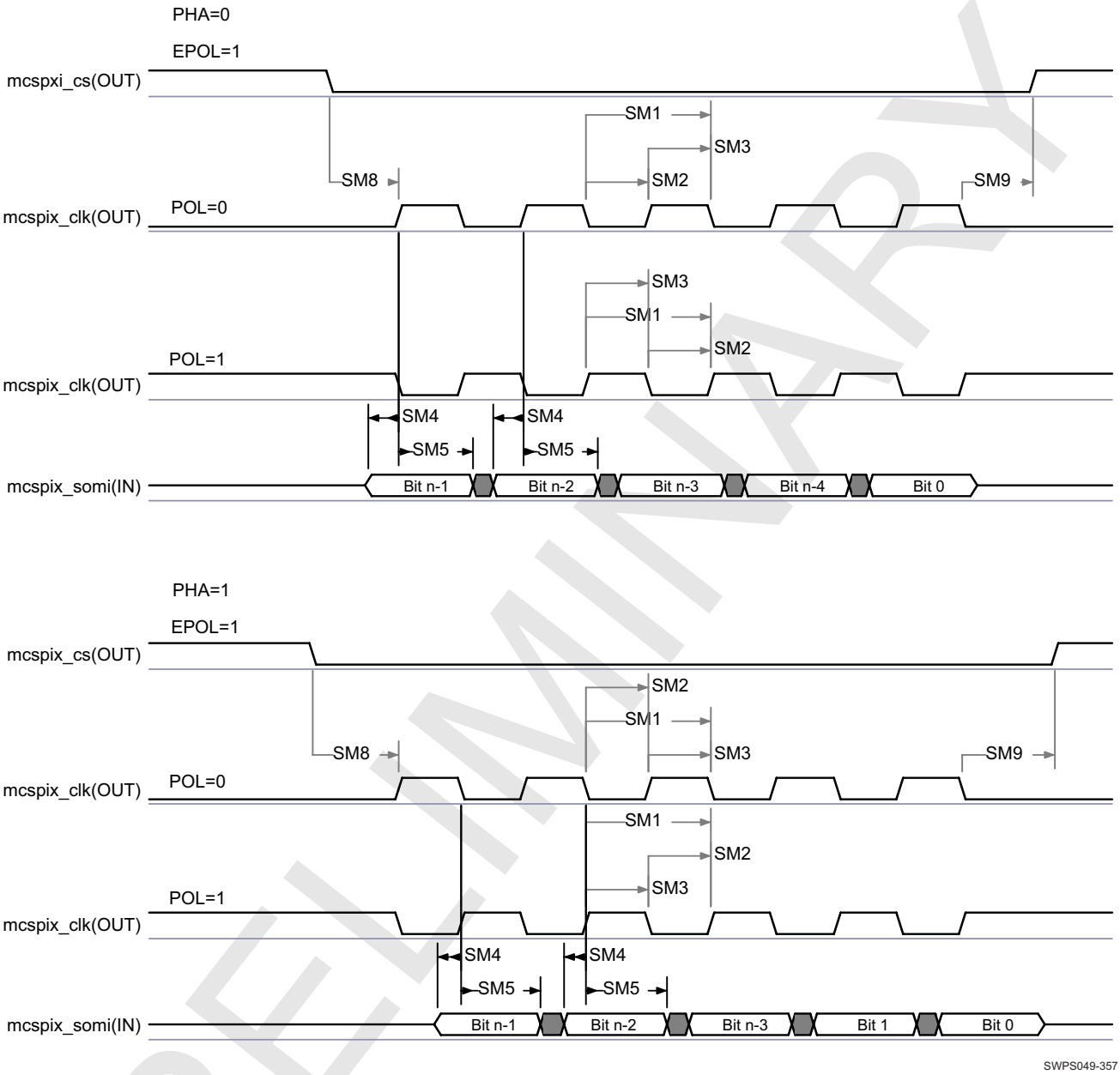


Figure 5-40. McSPI1 McSPI2 – Master Mode Receive (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.

(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

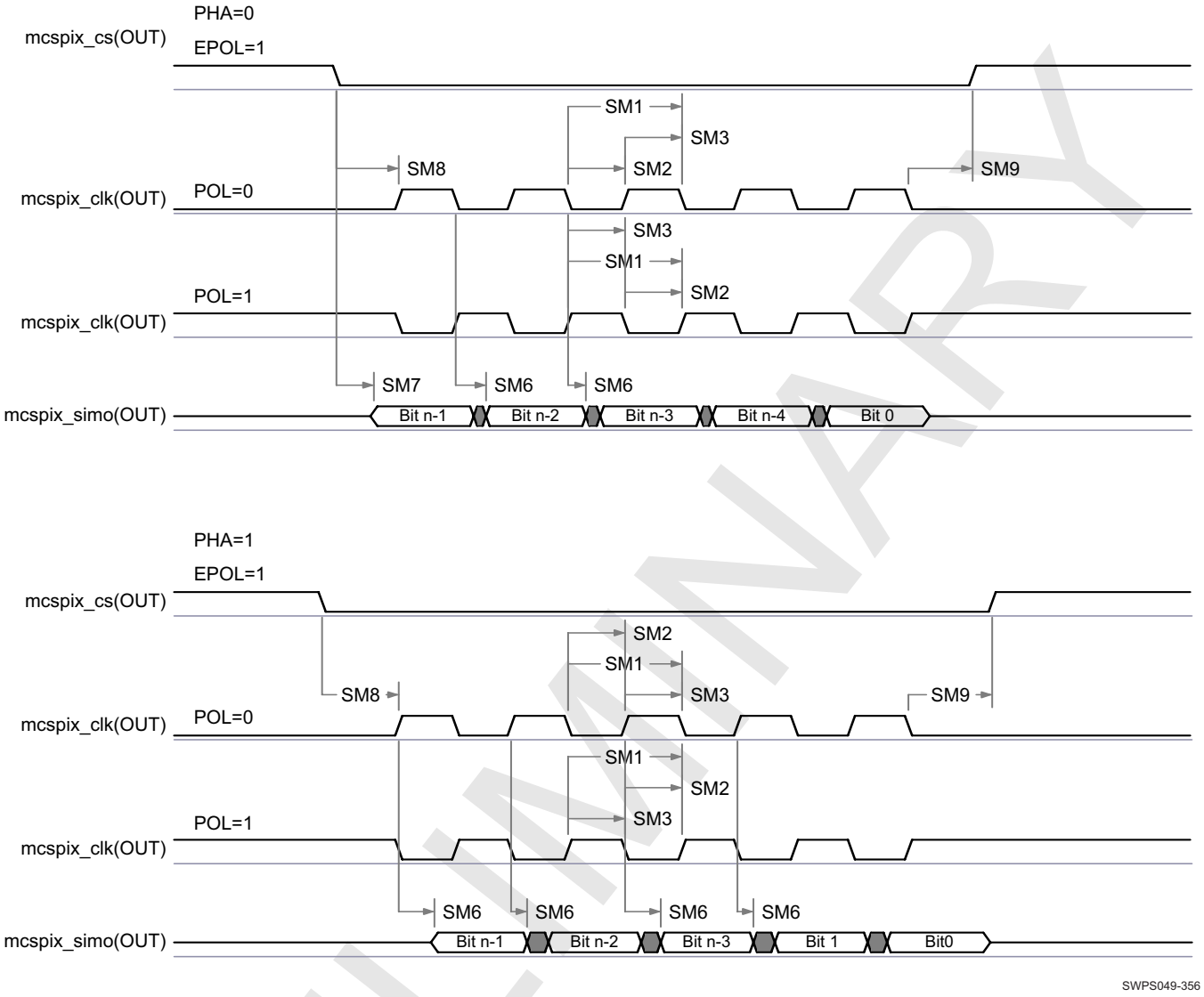


Figure 5-41. McSPI1 McSPI2 – Master Mode Transmit (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.

(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

5.6.3.4 McSPI1 and McSPI2 – 1 Peripheral – SDR – Master – 12 MHz

Table 5-53. McSPI1 and McSPI2 Timing Conditions – Master Mode – 12 MHz

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	100	12000	ps
t_F	Input signal fall time	100	12000	ps
Output Condition (1)				

(1) See Table 8-41 and Table 8-43.

Table 5-54 and Table 5-55 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-54. McSPI1 and McSPI2 Timing Requirements – Master Mode – 12 MHz (3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspix_somi (2)valid before mcspix_clk (1)(2) active edge	4.25		ns
SM5	$t_{h(CLKAE-SOMI)}$	Hold time, mcspix_somi (2)valid after mcspix_clk (1)(2)active edge	-0.34		ns

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 1 or 2.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-55. McSPI1 and McSPI2 Switching Requirements – Master Mode – 12 MHz (10)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
SM1	$1 / t_{C(CLK)}$	Frequency (2), mcspix_clk (1)(8)			12	MHz
SM2	$t_{W(CLKL)}$	Typical Pulse duration, mcspix_clk (4)(8)low		0.5*P (2)		ns
SM3	$t_{W(CLKH)}$	Typical Pulse duration, mcspix_clk (4)(8)high		0.5*P (2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk (8)			4167	ps
	$t_{J(clk)}$	Jitter standard deviation (3), mcspix_clk (8)			65	ps
	$t_{R(clk)}$	Rise time, mcspix_clk (8)			5544	ps
	$t_{F(clk)}$	Fall time, mcspix_clk (8)			5234	ps
SM6	$t_{d(CLK-SIMO)}$	Delay time, mcspix_clk (4)(8)active edge to mcspix_simo (8)transition		-16.62	12.80	ns
SM7	$t_{d9CS-SIMO)}$	Delay time, mcspix_cs (9)active edge to mcspix_simo (8)transition	PHA=0 (7)	12.80	3.63	ns
SM8	$t_{d(CS-CLK)}$	Delay time, mcspix_cs (9)active to mcspix_clk (4)first edge	PHA=1 (7)	A (5) – 12.8		ns
			PHA=0 (7)	B (6) – 12.8		ns
SM9	$t_{d(CLK-CS)}$	Delay time, mcspix_clk (4)(8)last edge to mcspix_cs (9)inactive	PHA=1 (7)	B (6) – 0.01		ns
			PHA=0 (7)	A (5) – 0.01		ns
	$t_{R(SIMO)}$	Rise time, mcspix_simo (8)			5544	ps
	$t_{F(SIMO)}$	Fall time, mcspix_simo (8)			5234	ps
	$t_{R(CS)}$	Rise time, mcspix_cs (9)			5544	ps
	$t_{F(CS)}$	Fall time, mcspix_cs (9)			5234	ps

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP543x TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case 1/P = 48MHz:
- A=(TCS+1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of OMAP543x TRM.

(6) B = (TCS+0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even = 2).
For more information, see the McSPI chapter of OMAP543x TRM.

(7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.

(8) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.

(9) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

(10) See DM Operating Condition Addendum for CORE OPP voltages.

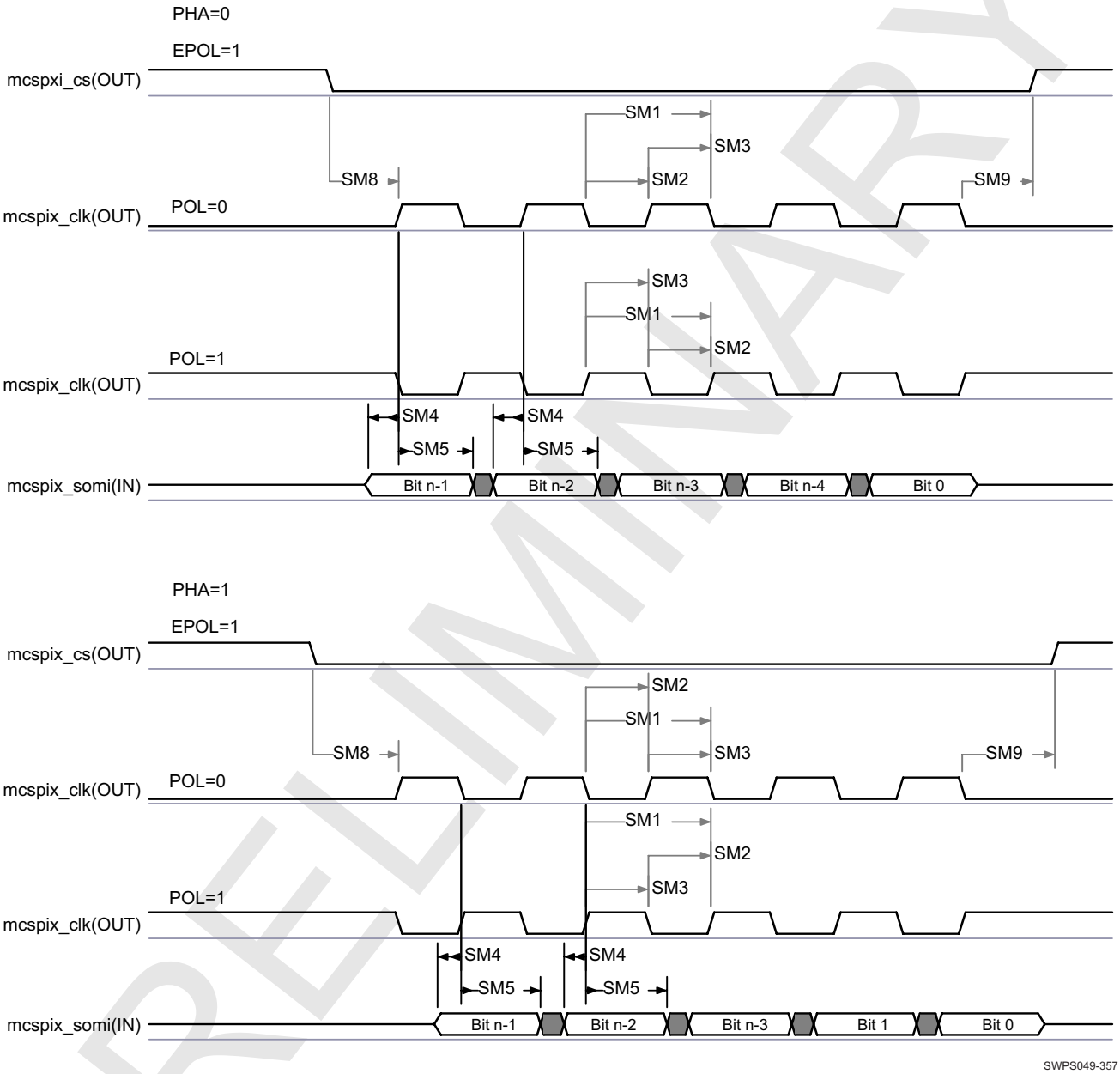


Figure 5-42. McSPI1 and McSPI2 - Master Mode Receive (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_somi, x is equal to 1 or 2

(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

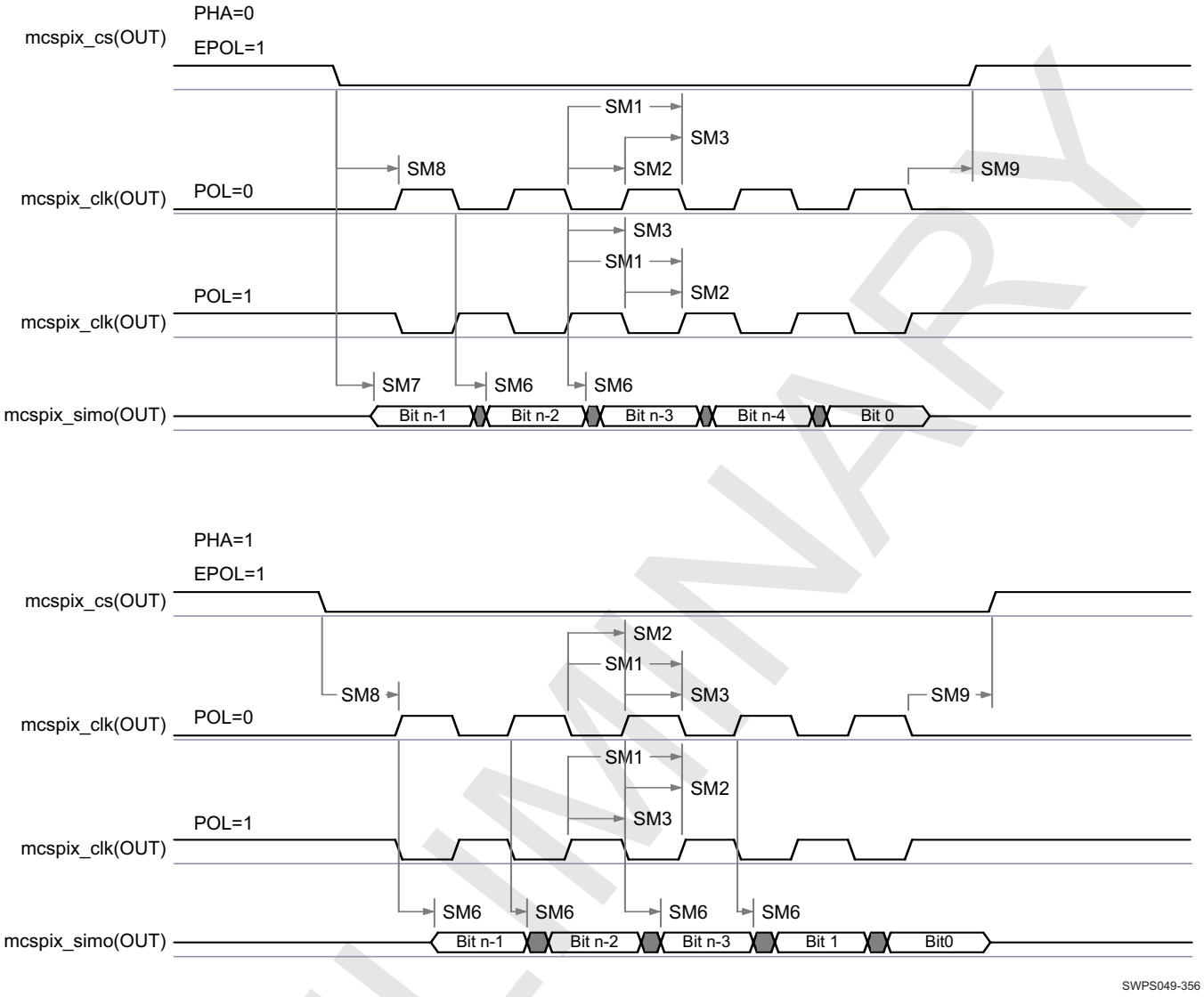


Figure 5-43. McSPI1 and McSPI2 – Master Mode Transmit (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_somi, x is equal to 1 or 2

(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

5.6.3.5 McSPI1 and McSPI2 – 1 Peripheral – SDR – Master – 12 MHz

Table 5-56. McSPI1 and McSPI2 Timing Conditions – Master Mode – 12 MHz

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	100	12000	ps
t_F	Input signal fall time	100	12000	ps
Output Condition (1)				

(1) See Table 8-41 and Table 8-43.

Table 5-57 and Table 5-58 assume testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-57. Table 5-14: McSPI1 and McSPI2 Timing Requirements – Master Mode – 12 MHz (3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SM4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspix_somi (2)valid before mcspix_clk (1) (2) active edge	18.87		ns
SM5	$t_{h(CLKAE-SOMI)}$	Hold time, mcspix_somi (2)valid after mcspix_clk (1) (2)active edge	-0.99		ns

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) In mcspix_clk and mcspix_somi, x is equal to 1 or 2.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-58. McSPI1 and McSPI2 Switching Requirements – Master Mode – 12 MHz (10)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
SM1	1 / $t_{C(CLK)}$	Frequency (2), mcspix_clk (1)(8)			12	MHz
SM2	$t_{W(CLKL)}$	Typical Pulse duration, mcspix_clk (4)(8)low		0.5*P (2)		ns
SM3	$t_{W(CLKH)}$	Typical Pulse duration, mcspix_clk (4)(8)high		0.5*P (2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk (8)			4167	ps
	$t_{J(clk)}$	Jitter standard deviation (3), mcspix_clk (8)			539	ps
	$t_{R(clk)}$	Rise time, mcspix_clk (8)			4860	ps
	$t_{F(clk)}$	Fall time, mcspix_clk (8)			4140	ps
SM6	$t_{d(CLK-SIMO)}$	Delay time, mcspix_clk (4)(8)active edge to mcspix_simo (8)transition		-7.10	2.97	ns
SM7	$t_{d9CS-SIMO)}$	Delay time, mcspix_cs (9)active edge to mcspix_simo (8)transition	PHA=0 (7)	2.97	3.63	ns
SM8	$t_{d(CS-CLK)}$	Delay time, mcspix_cs (9)active to mcspix_clk (4)first edge	PHA=1 (7)	A (5)-39.49		ns
			PHA=0 (7)	B (6)-39.49		ns
SM9	$t_{d(CLK-CS)}$	Delay time, mcspix_clk (4)(8)last edge to mcspix_cs (9)inactive	PHA=1 (7)	B (6)-43.63		ns
			PHA=0 (7)	A (5)-43.63		ns
	$t_{R(SIMO)}$	Rise time, mcspix_simo (8)			4860	ps
	$t_{F(SIMO)}$	Fall time, mcspix_simo (8)			4140	ps
	$t_{R(CS)}$	Rise time, mcspix_cs (9)			4860	ps
	$t_{F(CS)}$	Fall time, mcspix_cs (9)			4140	ps

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP543x TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(5) Case 1/P = 48MHz:
- A=(TCS+1) * $T_{SPICLKREF}$ (TCS is a bit field of MCSPI_CHxCONF register).
Case 1/P < 48MHz
- A=(TCS+0.5) * F_{RATIO} * $T_{SPICLKRE}$F (TCS is a bit field of MCSPI_CHxCONF register).
For more information, see the McSPI chapter of OMAP543x TRM.

(6) B = (TCS+0.5) * $T_{SPICLKREF}$ * F_{RATIO} (TCS is a bit field of MCSPI_CHxCONF register, F_{RATIO}: Even ≥ 2).
For more information, see the McSPI chapter of OMAP543x TRM.

(7) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.
(8) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.
(9) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0].
(10) See DM Operating Condition Addendum for CORE OPP voltages.

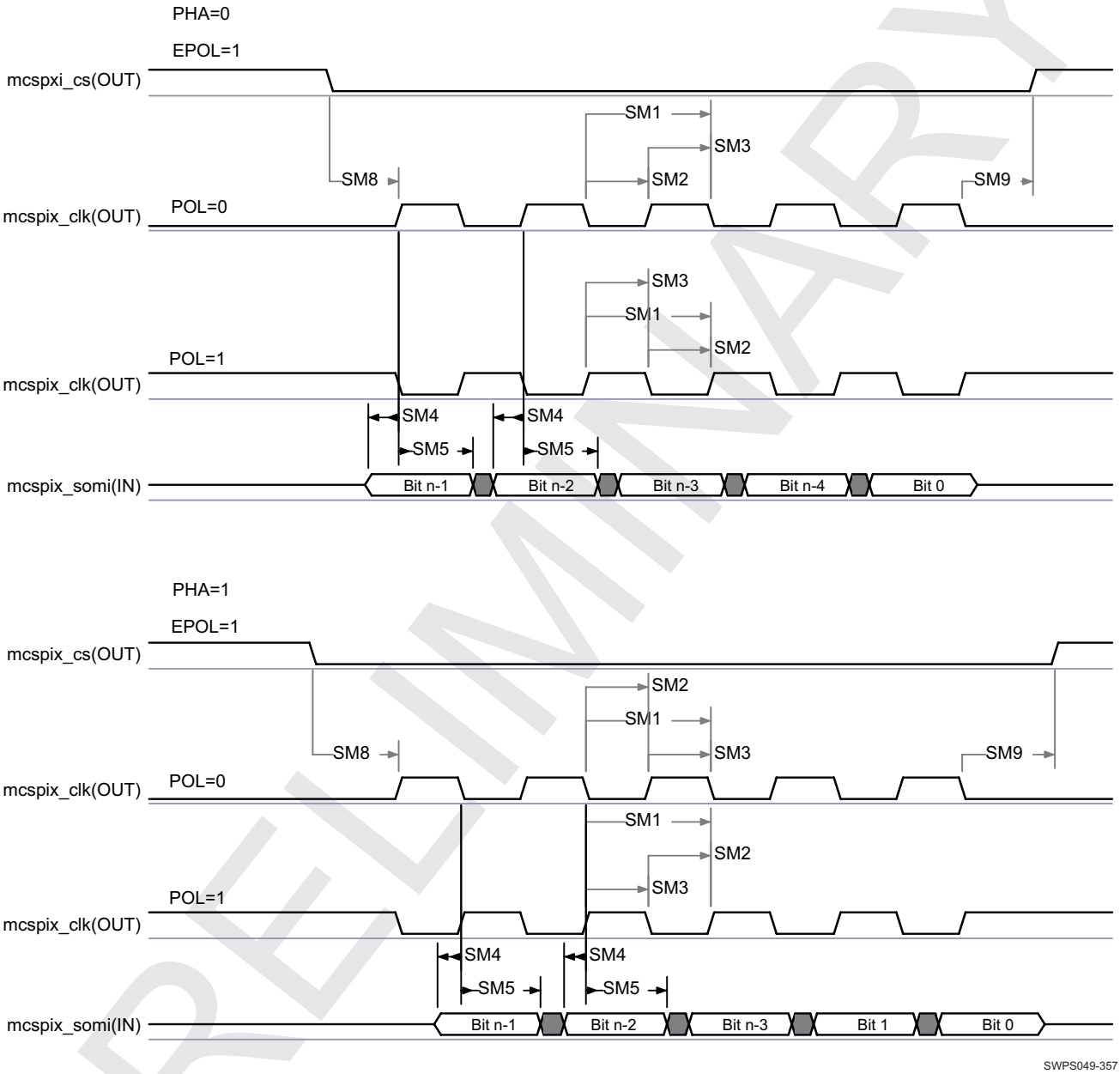


Figure 5-44. McSPI1 McSPI2 – Master Mode Receive (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.
(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL
(3) In mcspix_clk, mcspix_somi, x is equal to 1 or 2.
(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0].

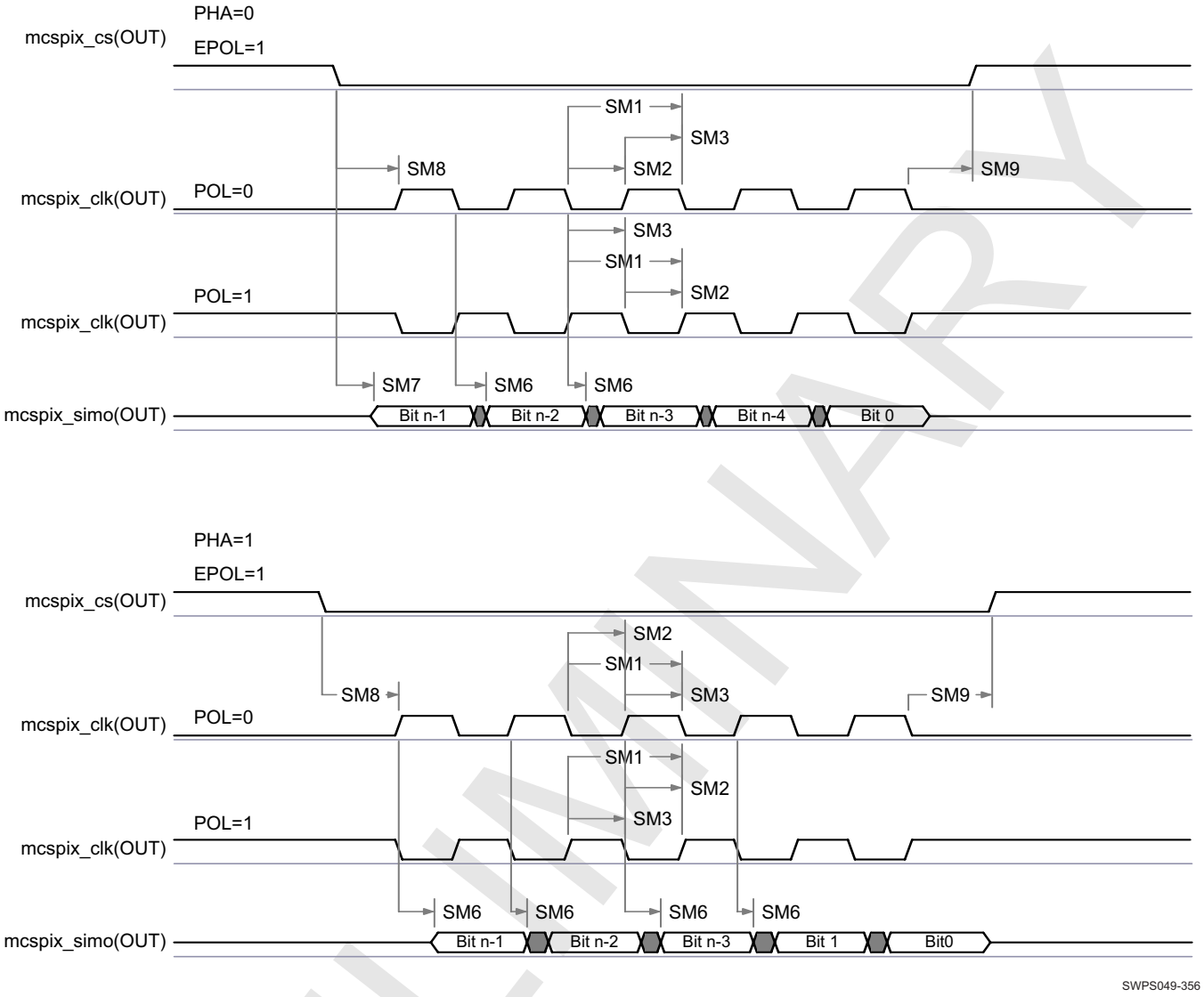


Figure 5-45. McSPI1 and McSPI2 – Master Mode Transmit (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_simo, x is equal to 1 or 2.

(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

5.6.3.6 McSPI3 and McSPI4 – 1 Peripheral – SDR – Slave – 24 MHz

Table 5-59. Table 5-16 McSPI3 and McSPI4 Timing Conditions – Slave Mode – 24 MHz

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	370	1840	ps
t_F	Input signal fall time	370	1840	ps
Output Condition (1)				

(1) See Table 8-21 and Table 8-23

Table 5-60 and Table 5-61 assumes testing over the recommended operating conditions and electrical characteristic conditions below.

Table 5-60. McSPI3 and McSPI4 Timing Requirements – Slave Mode – 24 MHz (4)(8)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SS1	1 / $t_{C(CLK)}$	Frequency (2), mcspix_clk (1)(6)		24	MHz
SS2	$t_{W(CLKL)}$	Typical Pulse duration, mcspix_clk (5)(6)low	0.5*P (2)		ns
SS3	$t_{W(CLKH)}$	Typical Pulse duration, mcspix_clk (5)(6)high	0.5*P (2)		ns
	$t_{dc(clk)}$	Duty cycle error, mcspix_clk (6)		2083	ps
	$t_{J(clk)}$	Jitter standard deviation (3), mcspix_clk (6)		1250	ps
	$t_{R(clk)}$	Rise time, mcspix_clk (6)		1840	ps
	$t_{F(clk)}$	Fall time, mcspix_clk (6)		1840	ps
SS4	$t_{su(SOMI-CLKAE)}$	Setup time, mcspix_simo (6) valid before mcspix_clk (5)(6) active edge	5.84		ns
SS5	$t_{h(CLKAE-SOMI)}$	Hold time, mcspix_simo (6) valid after mcspix_clk (5)(6) active edge	5.84		ns
SS8	$t_{su(CS-CLKAE)}$	Setup time, mcspix_cs (7) valid before mcspix_clk (5)(6) active edge	6.05		ns
SS9	$t_{h(CLKAE-CS)}$	Hold time, mcspix_cs (7) valid after mcspix_clk (5)(6) active edge	6.05		ns

(1) Related with the mcspix_clk maximum frequency programmable in the MCSPI module by setting the configuration register MCSPI_CHxCONF.
For more information, see the McSPI environment chapter, Data Format Configurations section of the OMAP543x TRM for modes and phase correspondence description.

(2) P = mcspix_clk clock period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) The timing requirements are guaranteed till the cycle jitter and duty cycle error conditions specified.

(5) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(6) In mcspix_clk and mcspix_simo, x is equal to 3 or 4.

(7) mcspix_cs is equal to mcspi3_cs0 or mcspi4_cs0

(8) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-61. McSPI3 and McSPI4 Switching Requirements – Slave Mode – 24 MHz (5)

NO.	PARAMETER			OPP_NOM		UNIT
				MIN	MAX	
SS6	$t_{d(CLK-SIMO)}$	Delay time, mcspix_clk (1)(3)active edge to mcspix_somi (3)transition		1.39	10.28	ns
SS7	$t_{d9CS-SIMO)}$	Delay time, mcspix_cs (4)active edge to mcspix_somi (3)transition	PHA=0 (2)		10.28	ns
	$t_{R(SIMO)}$	Rise time, mcspix_somi (3)			4885	ps
	$t_{F(SIMO)}$	Fall time, mcspix_somi (3)			4885	ps

(1) This timing applies to all configurations regardless of mcspix_clk polarity and which clock edges are used to drive output data and capture input data.

(2) mcspix_clk phase is programmable with the bit PHA, of MCSPI_CHxCONF register.

(3) In mcspix_clk, mcspix_somi, x is equal to 3 or 4.

(4) mcspix_cs is equal to mcspi3_cs0 or mcspi4_cs0

(5) See DM Operating Condition Addendum for CORE OPP voltages.

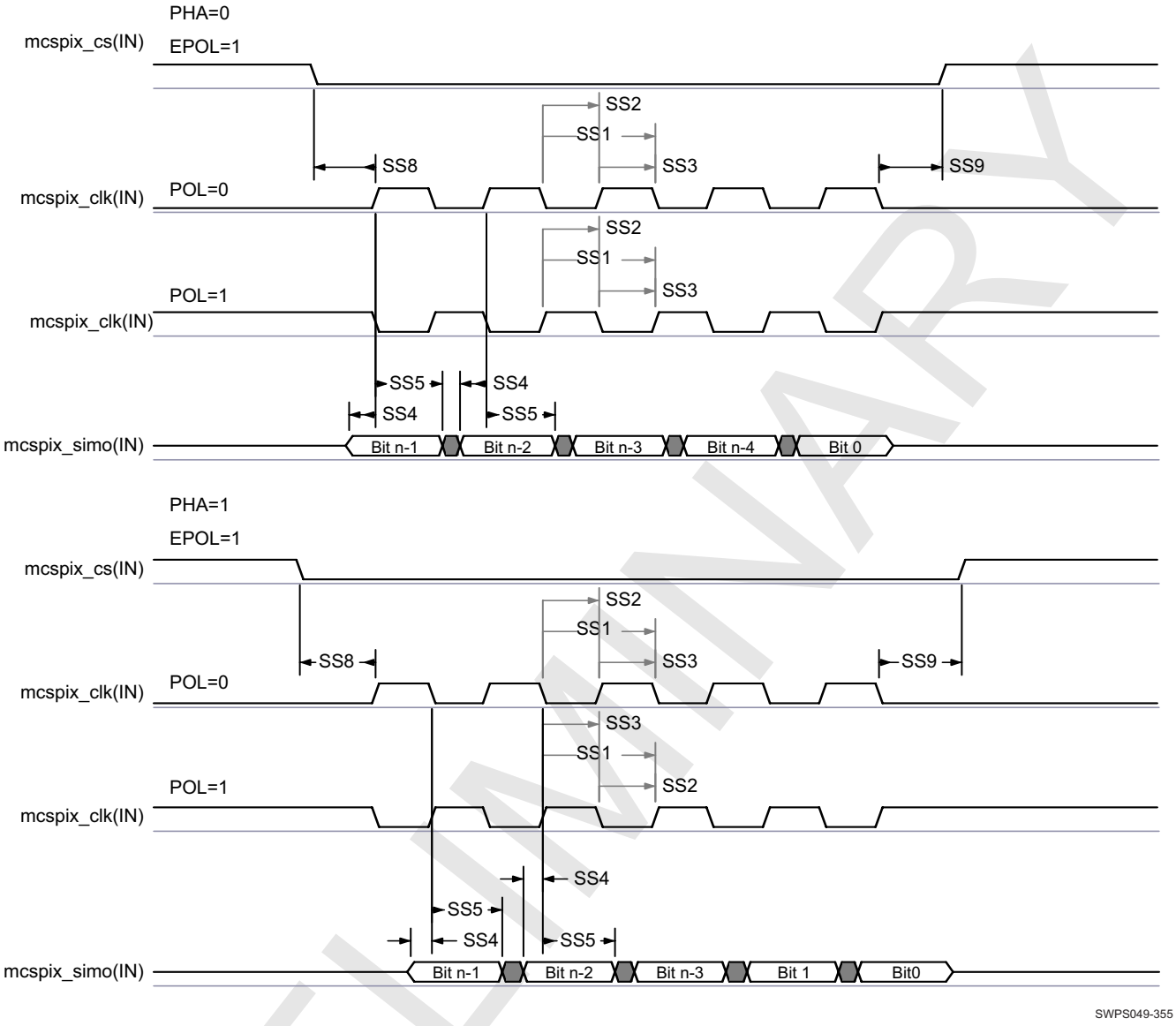


Figure 5-46. McSPI3 and McSPI4 – Slave Mode Receive (1)(2)(3)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_simo is driven is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_somi, x is equal to 1 or 2

(4) mcspix_cs is equal to mcspi1_cs[3:0] or mcspi2_cs[1:0]

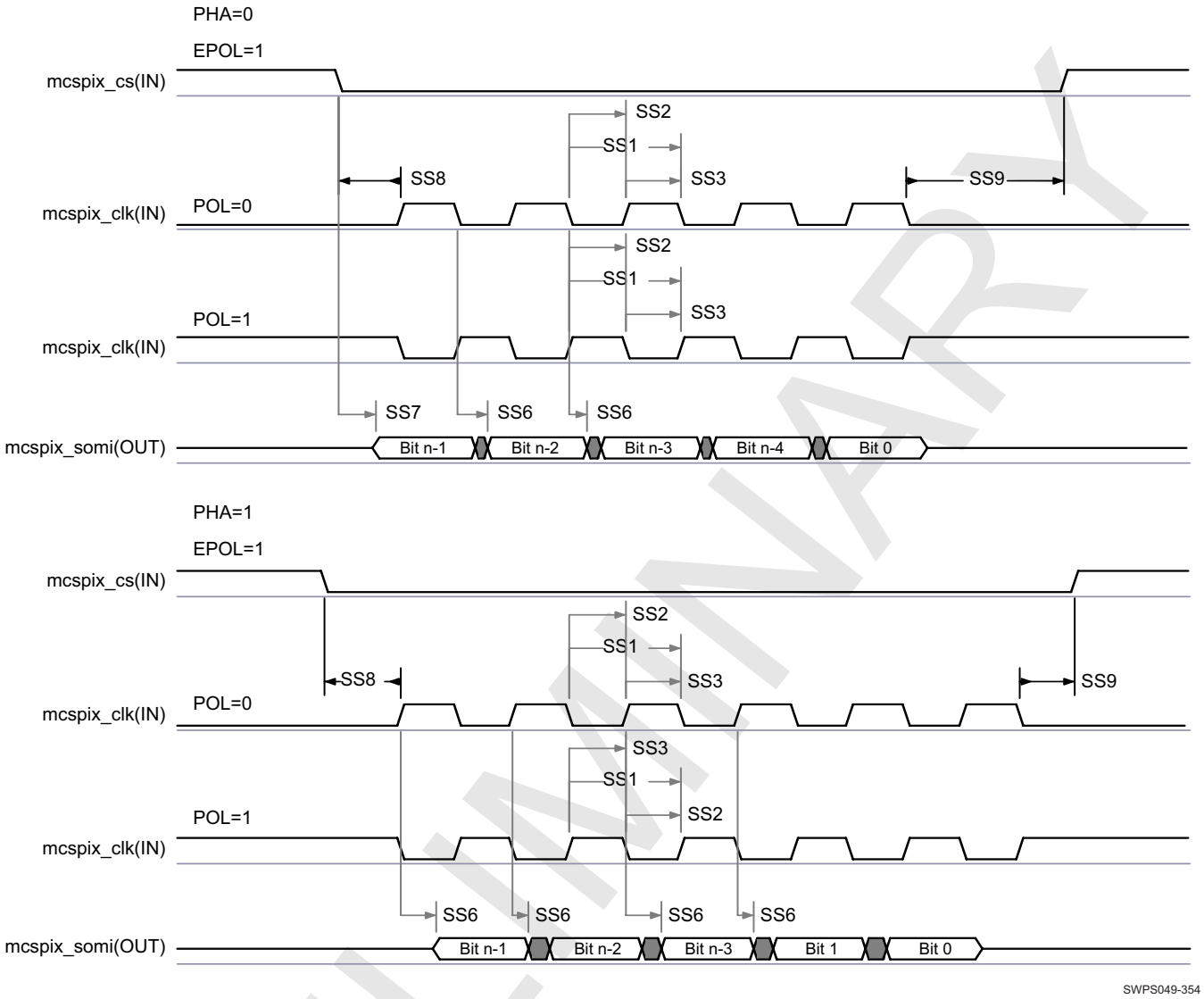


Figure 5-47. McSPI3 and McSPI4 – Slave Mode Transmit (1)(2)(3)(4)

(1) The active clock edge selection of mcspix_clk (rising or falling) on which mcspix_somi data is latched is software configurable with the bit MCSPI_CHxCONF[1] = POL and the bit MCSPI_CHxCONF[0] = PHA.

(2) The polarity of mcspix_cs is software configurable with the bit MCSPI_CHxCONF[6] = EPOL

(3) In mcspix_clk, mcspix_somi, x is equal to 3 or 4.

(4) mcspix_cs is equal to mcspi3_cs0 or mcspi4_cs0.

5.6.4 Digital Microphone (DMIC)—1.8 V

NOTE

For more information, see the Digital Microphone Controller chapter in the OMAP543x TRM.

The module consists in an audio module dedicated to mobile telephone terminal. The DMIC module allows supporting up to three pairs of digital microphones. Digital microphone generates a pulse-density modulated (PDM) stream of bits. The data are transferred from the external microphone on one half-period of the clock (DDR) provided by the DMIC module.

Table 5-62. DMIC Timing Conditions—DDR—Master/Receive Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time		10.00	ns
t_F	Input signal fall time		10.00	ns
Output Condition(1)				

(1) See Table 8-47, *Audio—DMIC PCB Requirements and IO Programming*.

Table 5-63 and Table 5-64 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-63. DMIC Timing Requirements—DDR—Master/Receive Mode—1.8 V

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
DMIC4	$t_{su(dV-clkH)}$	Setup time, data valid before clk rising or falling edge	56.0		MHz
DMIC5	$t_{h(clkH-dV)}$	Hold time, data valid after clk rising or falling edge	–0.7		ns

Table 5-64. DMIC Switching Characteristics—DDR—Master/Receive Mode—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
DMIC1	1 / $t_{c(clk)}$	Frequency, output abedmic_clk		3.84	MHz
DMIC2	$t_{w(clkL)}$	Typical pulse duration, output abedmic_clk low	0.5 × P(1)		ns
DMIC3	$t_{w(clkH)}$	Typical pulse duration, output abedmic_clk high	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abedmic_clk		13	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output abedmic_clk		67	ps
	$t_{R(clk)}$	Rise time, output abedmic_clk		10	ns
	$t_{F(clk)}$	Fall time, output abedmic_clk		10	ns

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

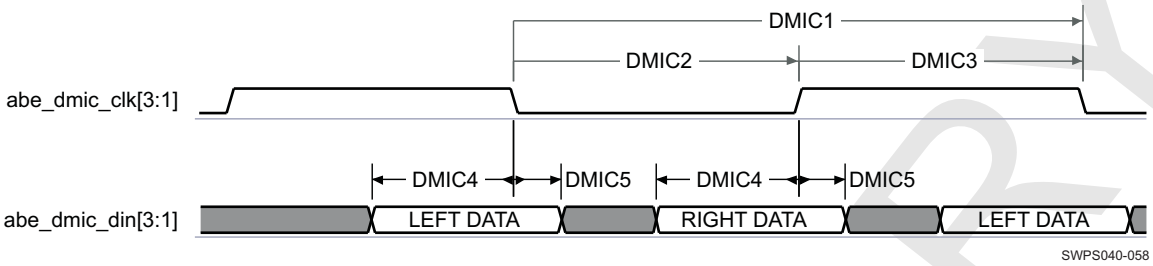


Figure 5-48. DMIC—DDR—Master/Receive Mode—1.8 V(1)

(1) RIGHT/LEFT DATA capturing edges depend on the TLV1310 DOS pin implementation (Data Output Select, selects the data output for the rising or falling edge of CLK). In this figure, RIGHT DATA is on rising clock edge (DOS high for right digital microphone) and LEFT DATA is on falling clock edge (DOS low for left digital microphone).

5.6.5 Multichannel Pulse Density Modulation (McPDM), 1.8 V

NOTE

For more information, see the Multichannel Pulse Density Modulation Controller chapter in the OMAP543x TRM.

Multichannel pulse density modulation interface (McPDM) is an audio module dedicated to mobile telephone terminal. It is composed of uplink and downlink paths both communicating with the audio companion chip through a dedicated interface.

Table 5-65. McPDM Timing Conditions—Master Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	6.00	ns
t_F	Input signal fall time	1.00	6.00	ns
Output Condition(1)				

(1) See Table 8-45, *Audio—McPDM PCB Requirements and IO Programming*.

Table 5-66 and Table 5-67 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-66. McPDM Timing Requirements—Master Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$1 / t_{c(clk)}$	Frequency, input abe_clks		19.20	MHz
PDM6	$t_{su(ulV-clkH)}$	Setup time, abemcpdm_ul_data valid before abemcpdm_lb_clk rising edge	21.68		ns
PDM7	$t_{h(clkH-ulV)}$	Hold time, abemcpdm_ul_data valid after abemcpdm_lb_clk rising edge	0.10		ns
PDM8	$t_{su(frameV-clkH)}$	Setup time, abemcpdm_frame valid before abemcpdm_lb_clk rising edge	21.68		ns
PDM9	$t_{h(clkH-frameV)}$	Hold time, abemcpdm_frame valid after abemcpdm_lb_clk rising edge	0.10		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-67. McPDM Switching Characteristics—Master Mode—1.8 V(3)(4)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
PDM1	$1 / t_{c(clk)}$	Frequency, output abemcpdm_lb_clk		19.20	MHz
PDM2	$t_{w(clkH)}$	Typical pulse duration, output abemcpdm_lb_clk high	0.5 × P(1)		ns
PDM3	$t_{w(clkL)}$	Typical pulse duration, output abemcpdm_lb_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output abemcpdm_lb_clk		2604	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output abemcpdm_lb_clk		434	ps
	$t_{R(clk)}$	Rise time, output abemcpdm_lb_clk		5	ns
	$t_{F(clk)}$	Fall time, output abemcpdm_lb_clk		5	ns
PDM4	$t_{d(clkH-dlV)}$	Delay time, output abemcpdm_lb_clk high to output abemcpdm_dl_data valid	1.45	33.03	ns
PDM5	$t_{d(clkH-frameV)}$	Delay time, output abemcpdm_lb_clk high to output abemcpdm_frame valid	1.45	33.03	ns
	$t_{R(dl)}$	Rise time, output abemcpdm_dl_data		5	ns
	$t_{F(dl)}$	Fall time, output abemcpdm_dl_data		5	ns
	$t_{R(frame)}$	Rise time, output abemcpdm_frame		5	ns

(1) P = output clk period in ns
(2) The jitter probability density can be approximated by a Gaussian function.
(3) The timing requirements are assured for the Jitter standard deviation and duty cycle error conditions specified.
(4) See DM Operating Condition Addendum for CORE OPP voltages.

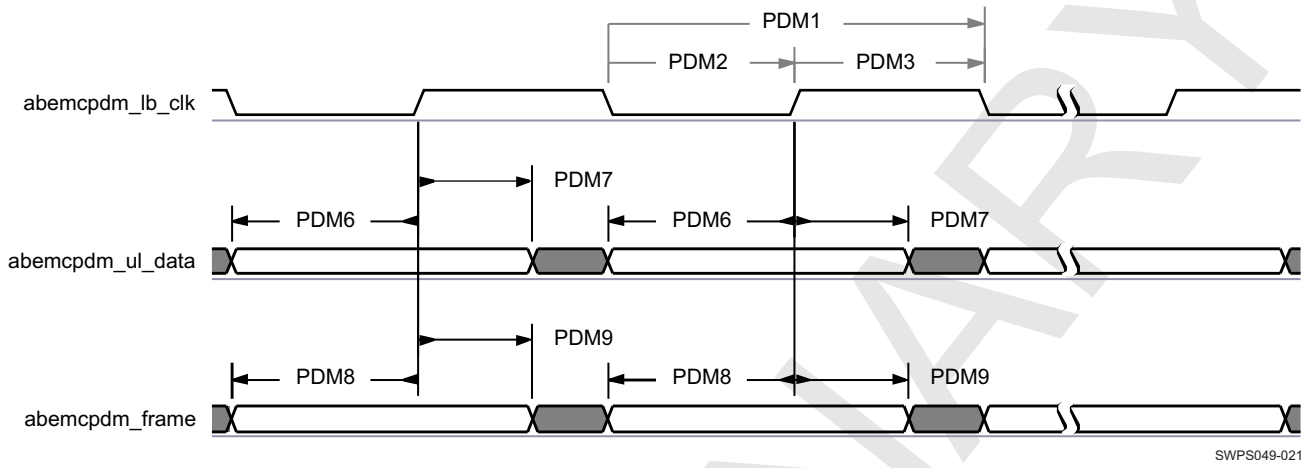


Figure 5-49. McPDM—SDR—Master Mode—Receiver—1.8 V

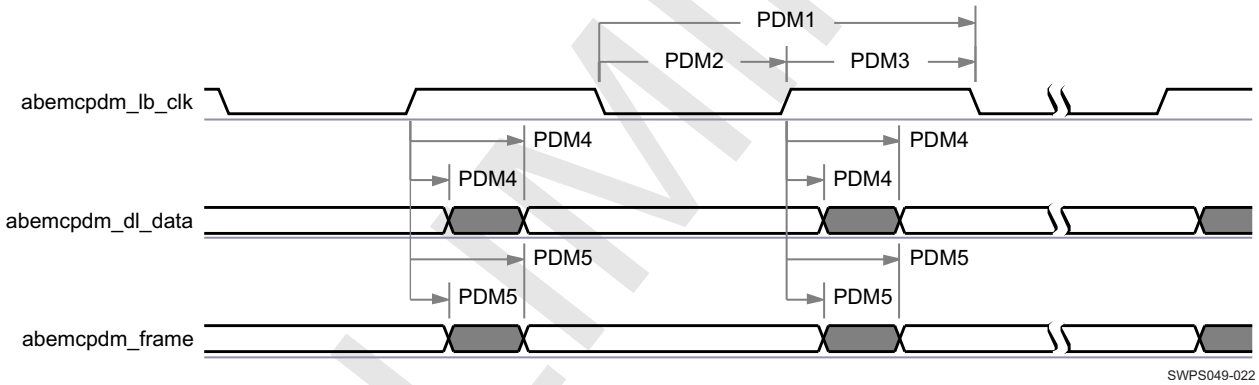


Figure 5-50. McPDM—SDR—Master Mode—Transmitter—1.8 V

5.6.6 MIPI HSI1 and HSI2 (High-Speed Synchronous Interface), 1.8 V

NOTE

For more information, see the MIPI HSI chapter in the OMAP543x TRM.

The HSI1 and HSI2 interfaces are compliant with the MIPI HSI protocol and typically used for communication with a modem. The HSI1 and HSI2 interfaces support maximum data rates of:

- In receive mode, 225.2 Mbps @OPP_NOM.
- In transmit mode, 192 Mbps @OPP_NOM.

Table 5-68. HSI1 and HSI2 Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	611	1366	ps
t_F	Input fall time	611	1366	ps
Output Conditions(1)				

(1) See Table 8-4, *HSI PCB Requirements and IO Programming*.

Table 5-69 and Table 5-70 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-69. HSI1 and HSI2 Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit	225.2		MHz
HSI2	$t_{d(DAT-FLAG)}$	Delay time, hsi_cadata transition to hsi_caflag transition	1.56		ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_caflag transition to hsi_cadata transition	1.56		ns
HSI3	$t_{d(DAT)}$	Duration time, hsi_cadata low level or high level duration	4.22		ns
	$t_{d(FLAG)}$	Duration time, hsi_caflag low level or high level duration	4.22		ns
HSI4	t_R	Rise time, hsi_cadata and hsi_caflag (20% to 80%)	0.61	1.37	ns
HSI5	t_F	Fall time, hsi_cadata and hsi_caflag (80% to 20%)	0.61	1.37	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-70. HSI1 and HSI2 Switching Characteristics—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSI1	$1 / t_{c(NomBit)}$	Frequency, nominal bit	192		MHz
HSI6	$t_{d(DAT-FLAG)}$	Delay time, hsi_acdata transition to hsi_acflag transition	2.08		ns
	$t_{d(FLAG-DAT)}$	Delay time, hsi_acflag transition to hsi_acdata transition	2.08		ns
HSI7	$t_{d(DAT)}$	Duration time, hsi_acdata low level or high level duration	4.95		ns
	$t_{d(FLAG)}$	Duration time, hsi_acflag low level or high level duration	4.95		ns
HSI8	t_R	Rise time, hsi_acdata and hsi_acflag (20% to 80%)	1.0	1.84	ns
HSI9	t_F	Fall time, hsi_acdata and hsi_acflag (80% to 20%)	1.0	1.84	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

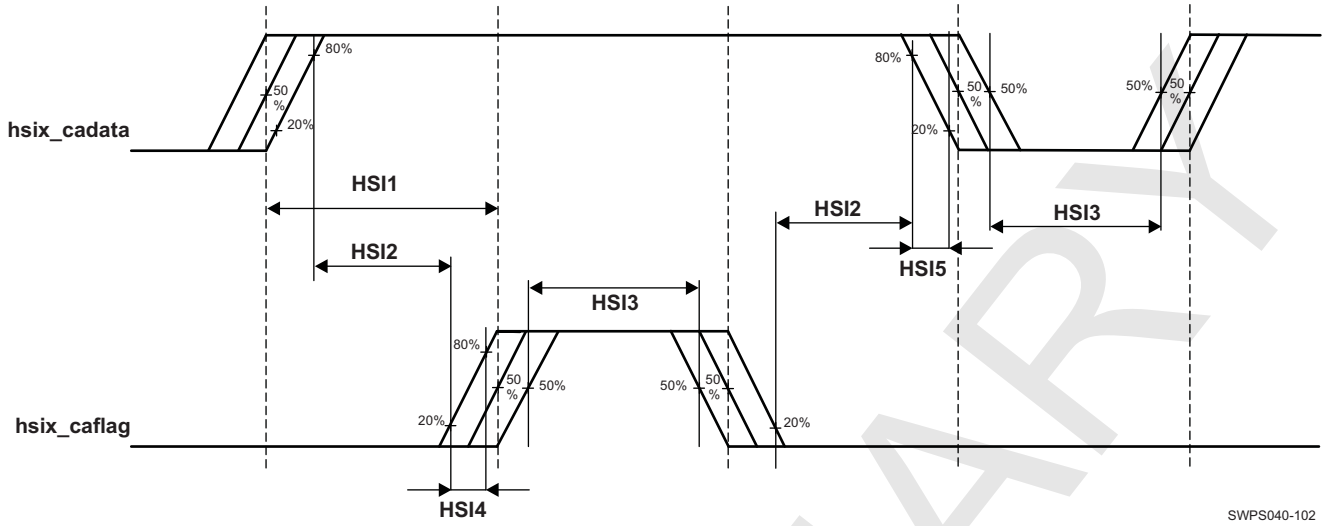


Figure 5-51. HSI1 and HSI2—1.8 V—Receive Mode

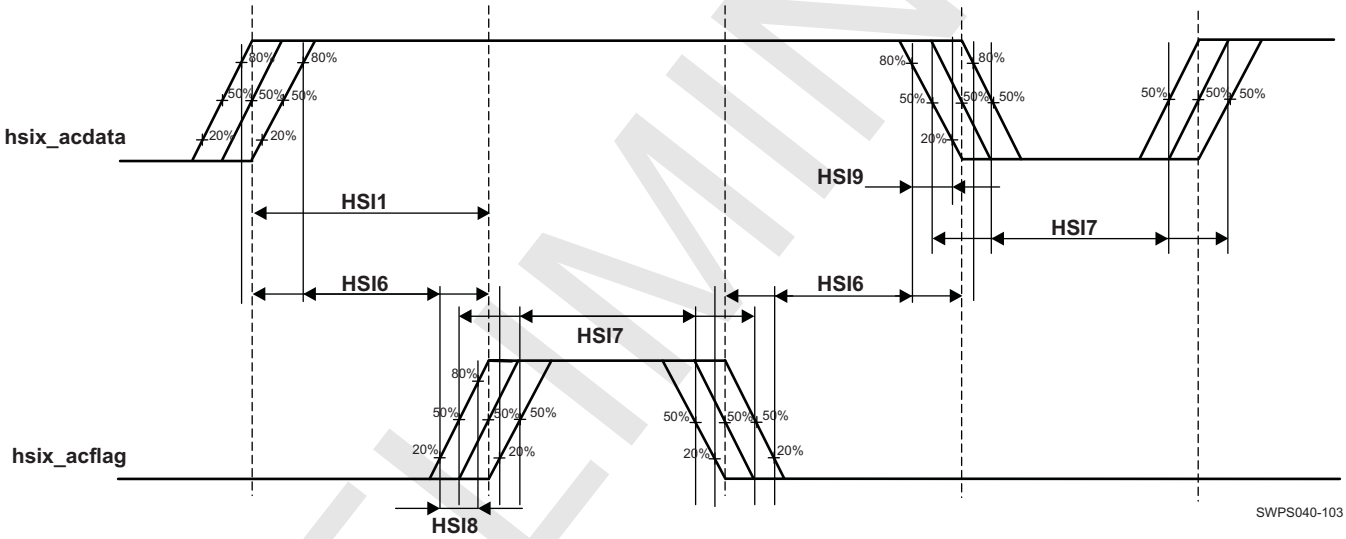


Figure 5-52. HSI1 and HSI 2—1.8 V—Transmit Mode

5.6.7 Universal Serial Bus (USB)

5.6.7.1 Super-Speed USB Dual-Role Device—USBD0—1.8 V and 3.3 V

NOTE

For more information, see the Serial Communication Interface / Super-Speed USB Dual-Role Subsystem chapter in the OMAP543x TRM.

5.6.7.1.1 USBD0 DRD PHY

The USBD0 DRD interface supports the following applications:

- USB2.0 High-Speed PHY port (1.8 V and 3.3 V): this asynchronous high-speed interface is compliant with the USB2.0 PHY standard with an internal transceiver (USB2.0 standard v2.0), for a maximum data rate of 480 Mbps at OPP_NOM.

- USB3.0 Super-Speed PHY port (1.8 V): this asynchronous differential super-speed interface is compliant with the USB3.0 RX/TX PHY standard (USB3.0 standard v1.0) for a maximum data bit rate of 5Gbps at OPP_NOM.

5.6.7.1.2 USBD0 DRD ULPI—SDR—Slave Mode—12-pin Mode—1.8 V

The USBD0 DRD interface supports the following application:

- USB ULPI port (1.8 V): this synchronous interface is compliant with the USB2.0 ULPI SDR standard (UTMI+ v1.22), for alternative off-chip USB2.0 PHY interface; that is, with external transceiver with a maximum frequency of 60 MHz at OPP_NOM (synchronous slave mode, SDR, 12-pin, 8-data-bit).

Table 5-71. HS USBD0 ULPI Timing Conditions—SDR—Slave Mode—12-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
Output Condition(1)				

(1) See Table 8-25, *USBD0 ULPI PHY PCB Requirements and IO Programming*.

Table 5-72 and Table 5-73 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-72. HS USBD0 ULPI Timing Requirements—SDR—Slave Mode—12-pin Mode—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
US1	$1 / t_{c(clk)}$	Frequency, input usbd0_ulpiphy_clk		60	MHz
US2	$t_{w(clkH)}$	Typical pulse duration, usbd0_ulpiphy_clk high	0.5 × P(1)		ns
US3	$t_{w(clkL)}$	Typical pulse duration, usbd0_ulpiphy_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, usbd0_ulpiphy_clk		833	ps
	$t_{j(clk)}$	Jitter standard deviation(2), usbd0_ulpiphy_clk		500	ps
US5	$t_{su(ctrlV-clkH)}$	Setup time, DIR and NXT valid before usbd0_ulpiphy_clk rising edge	6.73		ns
US6	$t_{h(clkH-ctrlV)}$	Hold time, DIR and NXT valid after usbd0_ulpiphy_clk rising edge	0.00		ns
US7	$t_{su(dV-clkH)}$	Setup time, Data valid before usbd0_ulpiphy_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, Data valid after usbd0_ulpiphy_clk rising edge	0.00		ns

(1) P = clk period in ns

(2) Maximum cycle jitter supported by input clock.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-73. HS USBD0 ULPI Switching Characteristics—SDR—Slave Mode—12-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
US4	$t_{d(clkL-ctrlV)}$	Delay time, output clk rising edge high to output STP valid	0.44	8.35	ns
	$t_{R(ctrl)}$	Rise time, output STP		3.0	ps
	$t_{F(ctrl)}$	Fall time, output STP		3.0	ps
US9	$t_{d(clkL-doV)}$	Delay time, output clk rising edge to output Data valid	0.44	8.35	ns
	$t_{R(do)}$	Rise time, output Data		3.0	ps
	$t_{F(do)}$	Fall time, output Data		3.0	ps

(1) See DM Operating Condition Addendum for CORE OPP voltages.

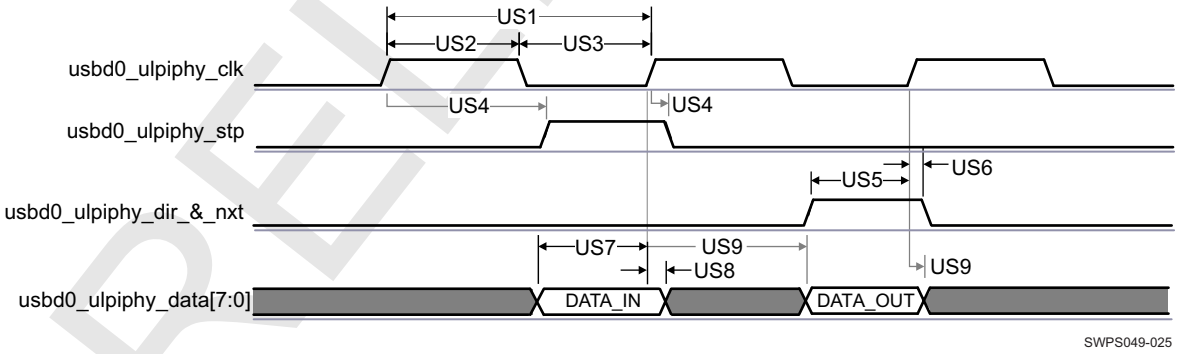


Figure 5-53. HS USBD0 ULPI —SDR—Slave Mode—12-pin Mode—1.8 V

5.6.7.2 USB Host High-Speed (USB HOST HS)—USBB1, 1.8 V (1.2 V for HSIC)

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem chapter in the OMAP543x TRM.

5.6.7.2.1 HS USBB1 ULPI—SDR—Slave Mode—12-pin Mode—1.8 V

The USBB1 interface supports the following application:

- USB ULPI (1.8 V): this synchronous interface follows the USB2.0 ULPI SDR standard (UTMI+ v1.22), for USB ULPI external transceiver, with a maximum frequency of 60 MHz at OPP_NOM (synchronous slave mode, SDR, 12-pin, 8 data bits).

Table 5-74. HS USBB1 ULPI Timing Conditions—SDR—Slave Mode—12-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
Output Condition(1)				

(1) See Table 8-29, *USBB1 ULPI PHY PCB Requirements and IO Programming*.

Table 5-75 and Table 5-76 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-75. HS USBB1 ULPI Timing Requirements—SDR—Slave Mode—12-pin Mode—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
US1	$1 / t_{c(clk)}$	Frequency, input usbb1_ulpiphy_clk		60	MHz
US2	$t_{w(clkH)}$	Typical pulse duration, usbb1_ulpiphy_clk high	0.5 × P(1)		ns
US3	$t_{w(clkL)}$	Typical pulse duration, usbb1_ulpiphy_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, usbb1_ulpiphy_clk		833	ps
	$t_{j(clk)}$	Jitter standard deviation(2), usbb1_ulpiphy_clk		500	ps
US5	$t_{su(ctrlV-clkH)}$	Setup time, DIR and NXT valid before usbb1_ulpiphy_clk rising edge	6.73		ns
US6	$t_{h(clkH-ctrlV)}$	Hold time, DIR and NXT valid after usbb1_ulpiphy_clk rising edge	0		ns
US7	$t_{su(dV-clkH)}$	Setup time, data valid before usbb1_ulpiphy_clk rising edge	6.73		ns
US8	$t_{h(clkH-dV)}$	Hold time, data valid after usbb1_ulpiphy_clk rising edge	0		ns

(1) P = clk period in ns

(2) Maximum cycle jitter supported by input clock.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-76. HS USBB1 ULPI Switching Characteristics—SDR—Slave Mode—12-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
US4	$t_{d(clkL-ctrlV)}$	Delay time, output clk rising edge high to output STP valid	0.44	8.35	ns
	$t_{R(ctrl)}$	Rise time, output STP		3.0	ps
	$t_{F(ctrl)}$	Fall time, output STP		3.0	ps
US9	$t_{d(clkL-doV)}$	Delay time, output clk rising edge to output data valid	0.44	8.35	ns
	$t_{R(do)}$	Rise time, output data		3.0	ps
	$t_{F(do)}$	Fall time, output data		3.0	ps

(1) See DM Operating Condition Addendum for CORE OPP voltages.

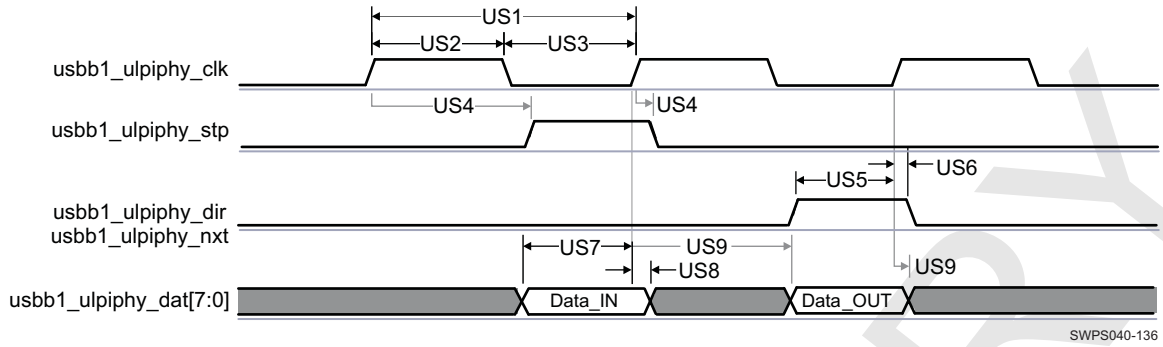


Figure 5-54. HS USBB1 ULPI —SDR—Slave Mode—12-pin Mode—1.8 V

5.6.7.2.2 HS USBB1 HSIC—DDR—2-pin Mode—1.2 V

The USBB1 interface supports the following application:

- USB HSIC (high-speed interchip) (1.2 V): this synchronous application for USB chip-to-chip interconnect (without transceiver) supports a maximum data rate of 480Mbps (240 MHz) at OPP_NOM (synchronous, DDR, 2-pin, data/strobe).

Table 5-77. HS USBB1 HSIC Timing Conditions—DDR—2-pin Mode—1.2 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.60	0.60	ns
t_F	Input signal fall time	0.60	0.60	ns
Output Condition(1)				

(1) See Table 8-27, *USBB1 HSIC PCB Requirements and IO Programming*.

Table 5-78 and Table 5-79 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-78. HS USBB1 HSIC Timing Requirements—DDR—2-pin Mode—1.2 V(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clki)}$	Frequency, input usbb1_hsic_strobe		240	MHz
HSIC2	$t_{w(clkiH)}$	Typical pulse duration, usbb1_hsic_strobe high	0.5 × P(1)		ns
HSIC3	$t_{w(clkiL)}$	Typical pulse duration, usbb1_hsic_strobe low	0.5 × P(1)		ns
	$t_{R(clki)}$	Rise time, usbb1_hsic_strobe (30% to 70%)	0.60	0.60	ns
	$t_{F(clki)}$	Fall time, usbb1_hsic_strobe (70% to 30%)	0.60	0.60	ns
	$t_{R(di)}$	Rise time, input data usbb1_hsic_data (30% to 70%)	0.60	0.60	ns
	$t_{F(di)}$	Fall time, input data usbb1_hsic_data (70% to 30%)	0.60	0.60	ns
HSIC5	$t_{su(strobe-dataV)}$	Setup time, usbb1_hsic_data valid before usbb1_hsic_strobe low or high	0.301		ns
HSIC6	$t_{h(strobe-dataV)}$	Hold time, usbb1_hsic_data valid after usbb1_hsic_strobe low or high	0.301		ns

(1) P = usbb1_hsic_strobe period in ns

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-79. HS USBB1 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clko)}$	Frequency, output usbb1_hsic_strobe		240	MHz
HSIC2	$t_{w(clkoH)}$	Typical pulse duration, usbb1_hsic_strobe high	0.5 × P(1)		ns
HSIC3	$t_{w(clkoL)}$	Typical pulse duration, usbb1_hsic_strobe low	0.5 × P(1)		ns
	$t_{dc(clko)}$	Duty cycle error, usbb1_hsic_strobe		83	ps
	$t_{R(clko)}$	Slew rate rise, usbb1_hsic_strobe	0.65	1.60	V/ns
	$t_{F(clko)}$	Slew rate fall, usbb1_hsic_strobe	0.65	1.60	V/ns
HSIC4	$t_{d(clk-dataV)}$	Delay time, usbb1_hsic_strobe low or high to usbb1_hsic_data valid	–0.422	0.422	ns
	$t_{R(do)}$	Slew rate rise, output data usbb1_hsic_data	0.65	1.60	V/ns
	$t_{F(do)}$	Slew rate fall, output data usbb1_hsic_data	0.65	1.60	V/ns

(1) P = usbb1_hsic_strobe period in ns

(2) See DM Operating Condition Addendum for CORE OPP voltages.

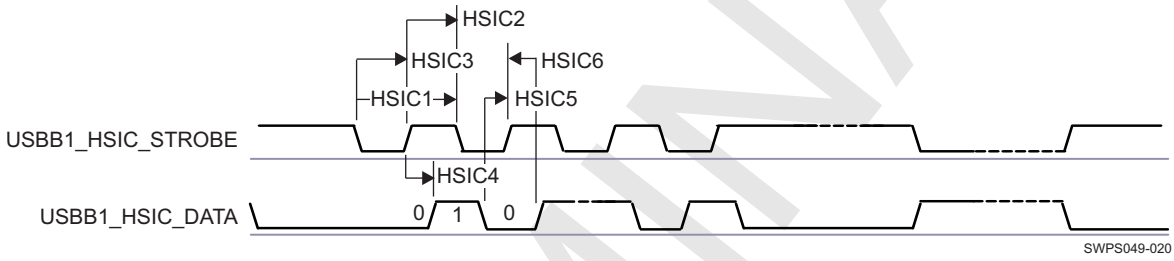


Figure 5-55. HS USBB1 HSIC —DDR—2-pin Mode—1.2 V

5.6.7.3 USB Host High–Speed (USB HOST HS)—USBB2, 1.8 V (1.2 V for HSIC)

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem chapter in the OMAP543x TRM.

5.6.7.3.1 HS USBB2 ULPI TLL—SDR—Master Mode —12-pin Mode—1.8 V

The USBB2 interface supports the following application:

- USB ULPI TLL (1.8 V): this synchronous application for USB ULPI device without transceiver (TLL: transceiverless link), with a maximum frequency of 60 MHz at OPP_NOM (synchronous master mode, SDR, 12-pin, 8-data-bit).

Table 5-80. HS USBB2 ULPI TLL Timing Conditions —SDR—Master Mode—12-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	1.00	3.00	ns
t_F	Input signal fall time	1.00	3.00	ns
Output Condition(1)				

(1) See Table 8-33, *USBB2 ULPI TLL PHY PCB Requirements and IO Programming*.

Table 5-81 and Table 5-82 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-81. HS USBB2 ULPI TLL Timing Requirements—SDR—Master Mode—12-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
UT4	$t_{su(ctrlV-clkH)}$	Setup time, STP valid before usbb2_ulpitll_clk rising edge	5.86		ns
UT5	$t_{h(clkH-ctrlV)}$	Hold time, STP valid after usbb2_ulpitll_clk rising edge	0.02		ns
UT6	$t_{su(dV-clkH)}$	Setup time, data valid before usbb2_ulpitll_clk rising edge	5.86		ns
UT7	$t_{h(clkH-dV)}$	Hold time, data valid after usbb2_ulpitll_clk rising edge	0.02		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-82. HS USBB2 ULPI TLL Switching Characteristics—SDR—Master Mode—12-pin Mode—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
UT1	$1 / t_{c(clk)}$	Frequency, usbb2_ulpitll_clk		60	MHz
UT2	$t_{w(clkH)}$	Typical pulse duration, usbb2_ulpitll_clk high	0.5 × P(1)		ns
UT3	$t_{w(clkL)}$	Typical pulse duration, usbb2_ulpitll_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, usbb2_ulpitll_clk		833	ps
	$t_{j(clk)}$	Jitter standard deviation(2), usbb2_ulpitll_clk		400	ps
	$t_{R(clk)}$	Rise time, usbb2_ulpitll_clk		3.0	ps
	$t_{F(clk)}$	Fall time, usbb2_ulpitll_clk		3.0	ps
UT8	$t_{d(clkL-ctrlV)}$	Delay time, usbb2_ulpitll_clk rising edge to output DIR and NXT valid	0.04	9.12	ns
	$t_{R(ctrl)}$	Rise time, output DIR and NXT		3.0	ps
	$t_{F(ctrl)}$	Fall time, output DIR and NXT		3.0	ps
UT9	$t_{d(clkL-doV)}$	Delay time, usbb2_ulpitll_clk rising edge to output data valid	0.04	9.12	ns
	$t_{R(do)}$	Rise time, output data		3.0	ps
	$t_{F(do)}$	Fall time, output data		3.0	ps

(1) P = output clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

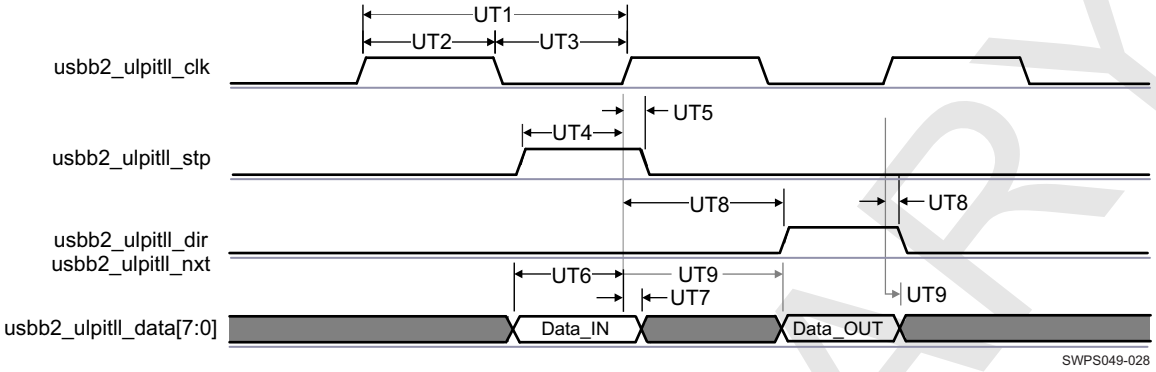


Figure 5-56. HS USBB2 ULPI TLL—SDR—Master Mode—12-pin Mode—1.8 V

5.6.7.3.2 HS USBB2 HSIC—DDR—2-pin Mode—1.2 V

The USBB2 interface supports the following application:

- USB HSIC (1.2 V): this synchronous application for USB chip-to-chip interconnect (without transceiver) supports a maximum data rate of 480Mbps (240 MHz) at OPP_NOM (synchronous, DDR, 2-pin, data/strobe)

Table 5-83. HS USBB2 HSIC Timing Conditions—DDR—2-pin Mode—1.2 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.6	0.6	ns
t_F	Input signal fall time	0.6	0.6	ns
Output Condition(1)				

(1) See Table 8-31, *USBB2 HSIC PCB Requirements and IO Programming*.

Table 5-84 and Table 5-85 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-84. HS USBB2 HSIC Timing Requirements—DDR—2-pin Mode—1.2 V(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clki)}$	Frequency, input usbb2_hsic_strobe		240	MHz
HSIC2	$t_{w(clkiH)}$	Typical pulse duration, usbb2_hsic_strobe high	0.5 × P(1)		ns
HSIC3	$t_{w(clkiL)}$	Typical pulse duration, usbb2_hsic_strobe low	0.5 × P(1)		ns
	$t_{R(clki)}$	Rise time, usbb2_hsic_strobe (30% to 70%)	0.6	0.6	ns
	$t_{F(clki)}$	Fall time, usbb2_hsic_strobe (70% to 30%)	0.6	0.6	ns
	$t_{R(di)}$	Rise time, input usbb2_data hsic_data (30% to 70%)	0.6	0.6	ns
	$t_{F(di)}$	Fall time, input data usbb2_hsic_data (70% to 30%)	0.6	0.6	ns
HSIC5	$t_{su(strobe-dataV)}$	Setup time, usbb2_hsic_data valid before usbb2_hsic_strobe low or high	0.301		ns
HSIC6	$t_{h(strobe-dataV)}$	Hold time, usbb2_hsic_data valid after usbb2_hsic_strobe low or high	0.301		ns

(1) P = usbb2_hsic_strobe period in ns

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-85. HS USBB2 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clko)}$	Frequency, output usbb2_hsic_strobe		240	MHz
HSIC2	$t_{w(clkoH)}$	Typical pulse duration, usbb2_hsic_strobe high	0.5 × P(1)		ns
HSIC3	$t_{w(clkoL)}$	Typical pulse duration, usbb2_hsic_strobe low	0.5 × P(1)		ns
	$t_{dc(clko)}$	Duty cycle error, usbb2_hsic_strobe		83	ps
	$t_{R(clko)}$	Slew rate rise, usbb2_hsic_strobe	0.65	1.6	V/ns
	$t_{F(clko)}$	Slew rate fall, usbb2_hsic_strobe	0.65	1.6	V/ns
HSIC4	$t_{d(clk-dataV)}$	Delay time, usbb2_hsic_strobe low or high to usbb2_hsic_data valid	–0.422	0.422	ns
	$t_{R(do)}$	Slew rate rise, output data usbb2_hsic_data	0.65	1.6	V/ns
	$t_{F(do)}$	Slew rate fall, output data usbb2_hsic_data	0.65	1.6	V/ns

(1) P = usbb2_hsic_strobe period in ns

(2) See DM Operating Condition Addendum for CORE OPP voltages.

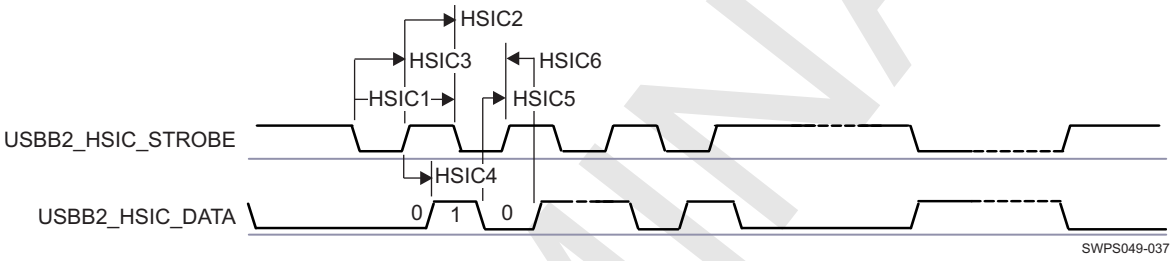


Figure 5-57. HS USBB2 HSIC —DDR—2-pin Mode—1.2 V

5.6.7.3.3 Low- and Full-Speed USBB2

The USBB2 interface supports the low-speed and full-speed standard (1.8 V) for USB TLL peripheral applications with maximum data rate of 1.5Mbps (LS) and 12Mbps (FS).

5.6.7.3.3.1 Low- and Full-Speed USBB2—Unidirectional TLL 2-pin Mode—1.8 V

Table 5-86. Low- and Full-Speed USBB2 Timing Conditions—Unidirectional TLL 2-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Condition(1)			

(1) See Table 8-35, *USBB2 Low-Speed / Full-Speed Multimode PCB Requirements and IO Programming*.

Table 5-87 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-87. Low- and Full-Speed USBB2 Timing Requirements—Unidirectional TLL 2-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSU1	$t_{d(Vp,Vm)}$	Time duration, usbb2_mm_rxdp and usbb2_mm_rxdm low together during transition		14	ns
FSU2	$t_{d(Vp,Vm)}$	Time duration, usbb2_mm_rxdp and usbb2_mm_rxdm high together during transition		8	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

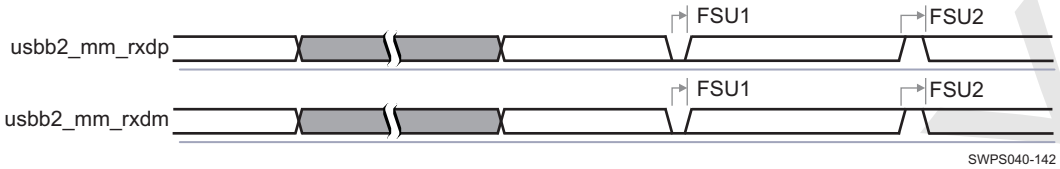


Figure 5-58. Low- and Full-Speed USB—Unidirectional TLL 2-pin Mode—1.8 V

5.6.7.3.3.2 Low- and Full-Speed USBB2—Bidirectional TLL 3-pin Mode—1.8 V

Table 5-88. Low/Full-Speed USBB2 Timing Conditions—Bidirectional TLL 3-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Condition(1)			

(1) See Table 8-35, *USBB2 Low-Speed / Full-Speed Multimode PCB Requirements and IO Programming*.

Table 5-89 and Table 5-90 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-89. Low- and Full-Speed USBB2 Timing Requirements—Bidirectional TLL 3-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSUT17	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition		14	ns
FSUT18	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 high together during transition		8	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-90. Low- and Full-Speed USBB2 Switching Characteristics—Bidirectional TLL 3-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSUT19	$t_{d(TXENH-DATV)}$	Delay time usbb2_mm_txen high to usbb2_mm_txdat valid	81.8	84.8	ns
FSUT20	$t_{d(TXENH-SE0V)}$	Delay time usbb2_mm_txen high to usbb2_mm_txse0 valid	81.8	84.8	ns
FSUT21	$t_{s(DAT-SE0)}$	Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition		1.5	ns
FSUT22	$t_{d(DATI-TXENL)}$	Delay time usbb2_mm_txdat invalid usbb2_mm_txen low	81.8		ns
FSUT23	$t_{d(SE0I-TXENL)}$	Delay time usbb2_mm_txse0 invalid usbb2_mm_txen low	81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

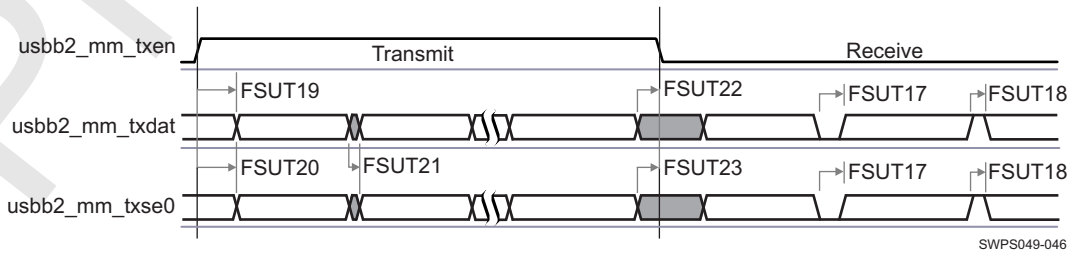


Figure 5-59. Low- and Full-Speed USB—Bidirectional TLL 3-pin Mode—1.8 V

5.6.7.3.3.3 Low- and Full-Speed USBB2—Bidirectional TLL 4-pin Mode—1.8 V

Table 5-91. Low- and Full-Speed USBB2 Timing Conditions—Bidirectional TLL 4-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Condition(1)			

(1) See Table 8-35, *USBB2 Low-Speed / Full-Speed Multimode PCB Requirements and IO Programming*.

Table 5-92 and Table 5-93 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-92. Low- and Full-Speed USBB2 Timing Requirements—Bidirectional TLL 4-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSUT9	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_txdat and usbb2_mm_txse0 low together during transition		14	ns
FSUT10	$t_{d(DAT,SE0)}$	Time duration, usbb2_mm_tsdat and usbb2_mm_txse0 high together during transition		8	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-93. Low- and Full-Speed USBB2 Switching Characteristics—Bidirectional TLL 4-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSUT11	$t_{d(TXENL-DATV)}$	Delay time usbb2_mm_txen active to usbb2_mm_txdat valid	81.8	84.8	ns
FSUT12	$t_{d(TXENL-SE0V)}$	Delay time usbb2_mm_txen active to usbb2_mm_txse0 valid	81.8	84.8	ns
FSUT13	$t_{s(DAT-SE0)}$	Skew between usbb2_mm_txdat and usbb2_mm_txse0 transition		1.5	ns
FSUT14	$t_{s(DP,DM-RCV)}$	Skew between usbb2_mm_ and usbb2_mm_rxrcv transition		1.5	ns
FSUT15	$t_{d(DATI-TXENL)}$	Delay time usbb2_mm_txse0 invalid to usbb2_mm_txen low	81.8		ns
FSUT16	$t_{d(SE0I-TXENL)}$	Delay time usbb2_mm_txdat invalid to usbb2_mm_txen low	81.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

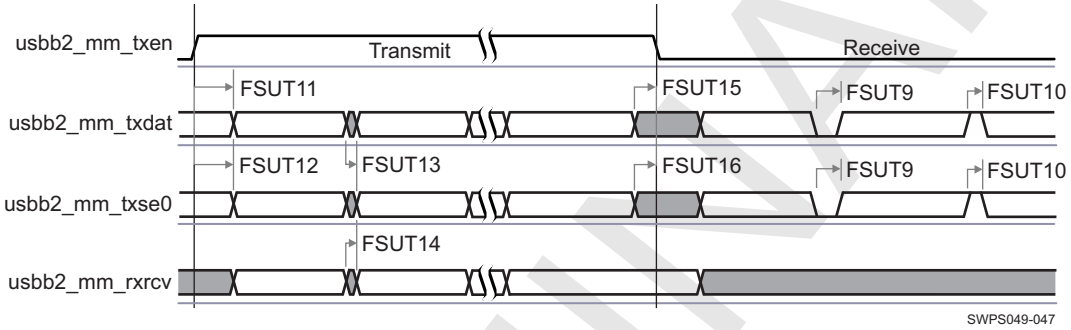


Figure 5-60. Low- and Full-Speed USB—Bidirectional TLL 4-pin Mode—1.8 V

5.6.7.3.3.4 Low- and Full-Speed USBB2—Unidirectional TLL 6-pin Mode—1.8 V

Table 5-94. Low- and Full-Speed USBB2 Timing Conditions—Unidirectional TLL 6-pin Mode—1.8 V

TIMING CONDITION PARAMETER		VALUE	UNIT
Input Conditions			
t_R	Input signal rise time	2	ns
t_F	Input signal fall time	2	ns
Output Condition(1)			

(1) See Table 8-35, *USBB2 Low-Speed / Full-Speed Multimode PCB Requirements and IO Programming*.

Table 5-95 and Table 5-96 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-95. Low- and Full-Speed USBB2 Timing Requirements—Unidirectional TLL 6-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSUT1	$t_{d(SE0,DAT)}$	Time duration, usbb2_mm_txse0 and usbb2_mm_txdat low together during transition		14	ns
FSUT2	$t_{d(SE0,DAT)}$	Time duration, usbb2_mm_txse0 and usbb2_mm_txdat high together during transition		8	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-96. Low- and Full-Speed USBB2 Switching Characteristics—Unidirectional TLL 6-pin Mode—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
FSUT3	$t_{d(TXENH-DPV)}$	Delay time usbb2_mm_txen high to usbb2_mm_rxdp valid	81.8	84.8	ns
FSUT4	$t_{d(TXENH-DMV)}$	Delay time usbb2_mm_txen high to usbb2_mm_rxdm valid	81.8	84.8	ns
FSUT5	$t_{d(DPI-TXENL)}$	Delay time usbb2_mm_rxdp invalid usbb2_mm_txen low	81.8		ns
FSUT6	$t_{d(DMI-TXENL)}$	Delay time usbb2_mm_rxdm invalid usbb2_mm_txen low	81.8		ns
FSUT7	$t_{s(DP-DM)}$	Skew between usbb2_mm_rxdp and usbb2_mm_rxdm transition		1.5	ns
FSUT8	$t_{s(DP,DM-RCV)}$	Skew between usbb2_mm_rxdp, usbb2_mm_rxdm and mmx_rxrcv transition		1.5	ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

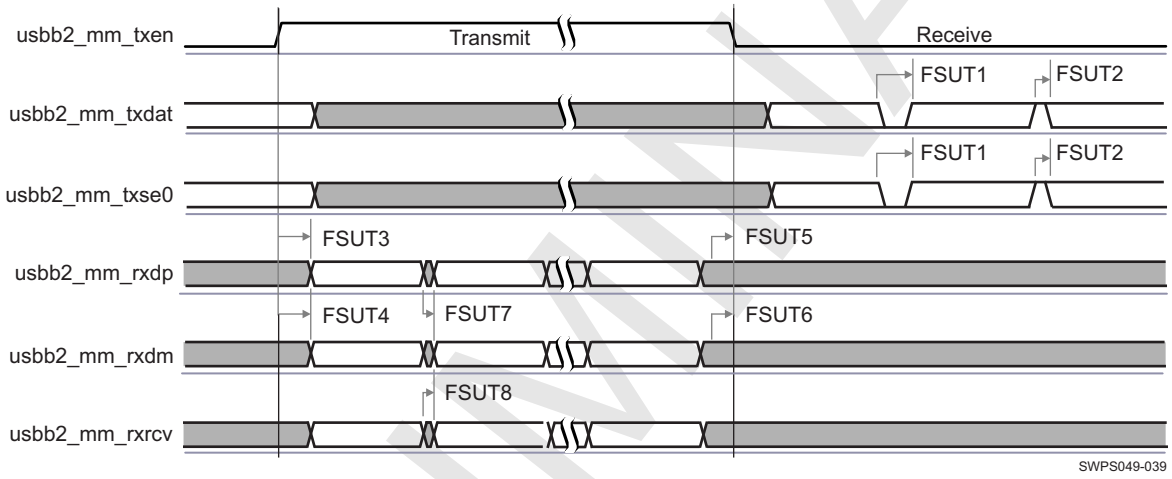


Figure 5-61. Low- and Full-Speed USB—Unidirectional TLL 6-pin Mode—1.8 V

5.6.7.4 USB Host High-Speed (USB HOST HS)—USBB3, HSIC 1.2 V

NOTE

For more information, see the Serial Communication Interface / High-Speed Multiport USB Host Subsystem chapter in the OMAP543x TRM.

5.6.7.4.1 HS USBB3 HSIC—2-pin Mode—1.2 V

The USBB3 interface supports the following application:

- USB HSIC (1.2 V): this synchronous application for USB chip-to-chip interconnect (without transceiver) supports a maximum data rate of 480Mbps (240 MHz) at OPP_NOM (synchronous, DDR, 2-pin, data/strobe).

Table 5-97. HS USBB3 HSIC Timing Conditions—DDR—2-pin Mode—1.2 V

TIMING CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input signal rise time	0.60	0.60	ns
t_F	Input signal fall time	0.60	0.60	ns
Output Condition(1)				

(1) See Table 8-37, *USBB3 HSIC PCB Requirements and IO Programming*.

Table 5-98 and Table 5-99 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-98. HS USBB3 HSIC Timing Requirements—DDR—2-pin Mode—1.2 V(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clki)}$	Frequency, input usbb3_hsic_strobe		240	MHz
HSIC2	$t_{w(clkiH)}$	Typical pulse duration, usbb3_hsic_strobe high	0.5 × P(1)		ns
HSIC3	$t_{w(clkiL)}$	Typical pulse duration, usbb3_hsic_strobe low	0.5 × P(1)		ns
	$t_{R(clki)}$	Rise time, usbb3_hsic_strobe (30% to 70%)	0.60	0.60	ns
	$t_{F(clki)}$	Fall time, usbb3_hsic_strobe (70% to 30%)	0.60	0.60	ns
	$t_{R(di)}$	Rise time, input usbb3_data hsic_data (30% to 70%)	0.60	0.60	ns
	$t_{F(di)}$	Fall time, input data usbb3_hsic_data (70% to 30%)	0.60	0.60	ns
HSIC5	$t_{su(strobe-dataV)}$	Setup time, usbb3_hsic_data valid before usbb3_hsic_strobe low or high	0.301		ns
HSIC6	$t_{h(strobe-dataV)}$	Hold time, usbb3_hsic_data valid after usbb3_hsic_strobe low or high	0.301		ns

(1) P = usbb3_hsic_strobe period in ns

(2) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-99. HS USBB3 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V(2)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC1	$1 / t_{c(clko)}$	Frequency, output usbb3_hsic_strobe		240	MHz
HSIC2	$t_{w(clkoH)}$	Typical pulse duration, usbb3_hsic_strobe high	0.5 × P(1)		ns
HSIC3	$t_{w(clkoL)}$	Typical pulse duration, usbb3_hsic_strobe low	0.5 × P(1)		ns
	$t_{dc(clko)}$	Duty cycle error, usbb3_hsic_strobe		83	ps
	$t_{R(clko)}$	Slew Rate rise, usbb3_hsic_strobe	0.65	1.6	V/ns
	$t_{F(clko)}$	Slew rate fall, usbb3_hsic_strobe	0.65	1.6	V/ns

Table 5-99. HS USBB3 HSIC Switching Characteristics—DDR—2-pin Mode—1.2 V(2) (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSIC4	$t_{d(clk-dataV)}$	Delay time, usbb3_hsic_strobe low or high to usbb3_hsic_data valid	–0.422	0.422	ns
	$t_{R(do)}$	Slew Rate rise, output data usbb3_hsic_data	0.65	1.6	V/ns
	$t_{F(do)}$	Slew Rate fall, output data usbb3_hsic_data	0.65	1.6	V/ns

(1) P = usbb3_hsic_strobe period in ns

(2) See DM Operating Condition Addendum for CORE OPP voltages.

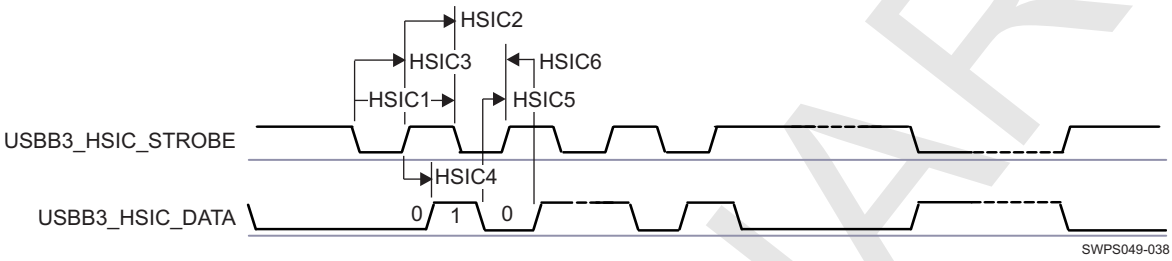


Figure 5-62. HS USBB3 HSIC —DDR—2-pin mode—1.2 V

5.6.8 Inter-Integrated Circuit Interface (I^2C), 1.8 V

NOTE

For more information, see the Serial Communication Interface / Multimaster High-Speed I^2C Controller / HS I^2C Functional Description section of the OMAP543x TRM.

The I^2C interface is compliant with the I^2C standard version 2.1.

5.6.9 HDQ / 1-Wire Interface (HDQ/1-Wire), 1.8 V

NOTE

For more information, see the Serial Communication Interface / HDQ1W section of the OMAP543x TRM.

The HDQ / 1-Wire interface is intended to work with both HDQ and 1-Wire protocols. The protocols use a single wire to communicate between the master (HDQ1W controller) and the slaves (HDQ/1-Wire external compliant devices). The HDQ/1-Wire typical application is the communication with battery monitor (gas gauge) integrated devices.

5.6.9.1 HDQ Mode

Table 5-100 through Table 5-102 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-100. HDQ Timing Requirements(3)

PARAMETER		OPP_NOM		UNIT
		MIN	MAX	
t_{CYCH}	Read bit window timing	190	250	µs
t_{HW1}	Read one data valid after HDQ low	32(2)	66(2)	
t_{HW0}	Read zero data hold after HDQ low	70(2)	145(2)	
t_{RSPS}	Response time from HDQ slave device(1)	190	320	

(1) Defined by software.

(2) If HDQ slave device drives a logic-low state after t_{HW0} max, it can be interpreted as a break pulse. For more information see Table 5-102 below and the HDQ1W section of the OMAP543x TRM.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-101. HDQ Sampling Cases(1)

CASE	FIRST SAMPLING (at 68 µs)	SECOND SAMPLING (at 180 µs)
1	L (logic-low state)	L (logic-low state)
2	L (logic-low state)	H (logic-high state)
3	H (logic-high state)	L (logic-low state)
4	H (logic-high state)	H (logic-high state)

(1) The different cases can be interpreted as follow:

- Case 1: If a logic-low state is present at the first sampling time and also at the second sampling time, the receive data can be interpreted as a break pulse.
- Case 2: If a logic-low state is present at the first sampling time and a logic-high state is present at the second sampling time, the receive data on the line is a zero (data).
- Case 3: Undefined.
- Case 4: If a logic-high state is present at the first sampling time and also at the second sampling time, the receive data on the line is a one (data).

Table 5-102. HDQ Switching Characteristics(1)

PARAMETER		OPP_NOM		UNIT
		MIN	MAX	
t_B	Break timing	190		µs
t_{BR}	Break recovery time	40		
t_{CYCD}	Write bit windows timing	190		
t_{DW1}	Write one data valid after HDQ low	0.5	50	
t_{DW0}	Write zero data hold after HDQ low	86	145	

(1) See DM Operating Condition Addendum for CORE OPP voltages.

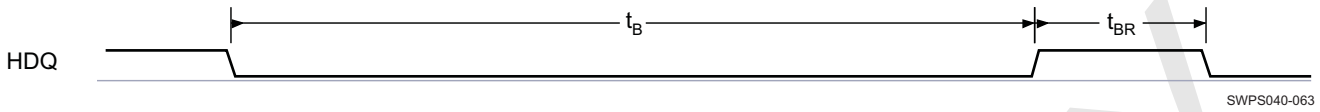


Figure 5-63. HDQ Break and Break Recovery Timing—OMAP HDQ Interface Writing Slave

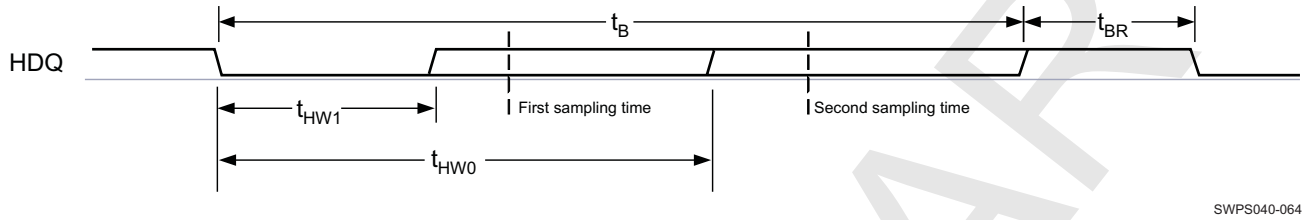


Figure 5-64. HDQ Break Detection Timing—OMAP HDQ Interface Reading Slave

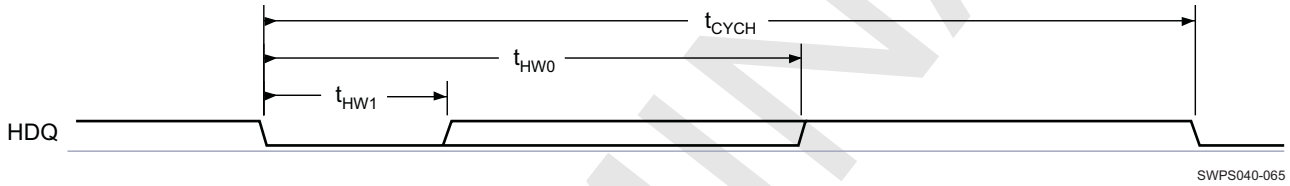


Figure 5-65. HDQ Bit Read Timing (Data)

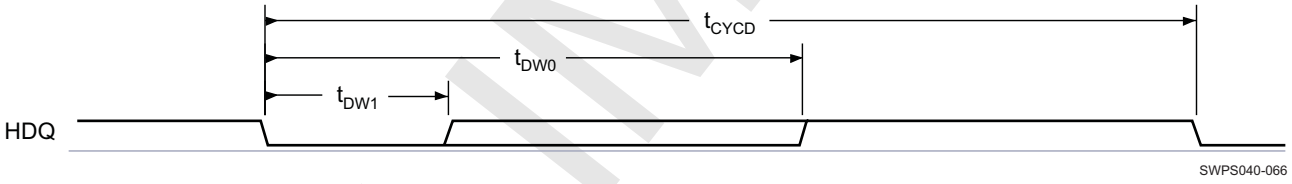


Figure 5-66. HDQ Bit Write Timing (Command / Address / Data)

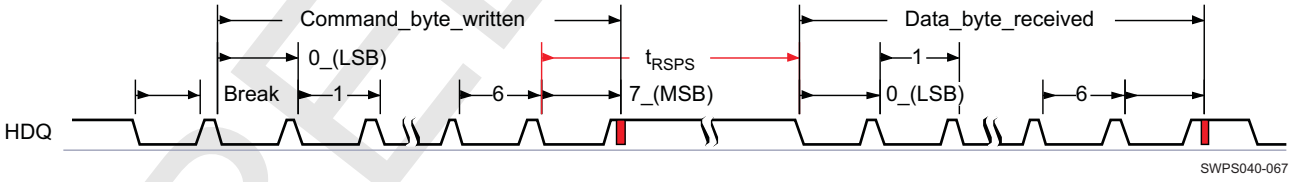


Figure 5-67. HDQ Communication Timing

5.6.9.2 1-Wire Mode

Table 5-103 and Table 5-104 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-103. 1-Wire Timing Requirements(1)

PARAMETER		OPP_NOM		UNIT
		MIN	MAX	
t_{PDH}	Presence pulse delay high	15	60	µs
t_{PDL}	Presence pulse delay low	60	240	
t_{RDV}	Read data valid time	t_{LOWR}	15	
t_{REL}	Read data release time	0	45	

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-104. 1-Wire Switching Characteristics(3)

PARAMETER		OPP_NOM		UNIT
		MIN	MAX	
t_{RSTL}	Reset time low	480	960	µs
t_{RSTH}	Reset time high	480		µs
t_{SLOT}	Bit cycle time	60	120	µs
t_{LOW1}	Write bit-one time	1	15	µs
t_{LOW0}	Write bit-zero time(2)	60	120	µs
t_{REC}	Recovery time	1		µs
t_{LOWR}	Read bit strobe time(1)	1	15	µs

(1) t_{LOWR} (low pulse sent by the master) must be short as possible to maximize the master sampling window.

(2) t_{LOW0} must be less than t_{SLOT}.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

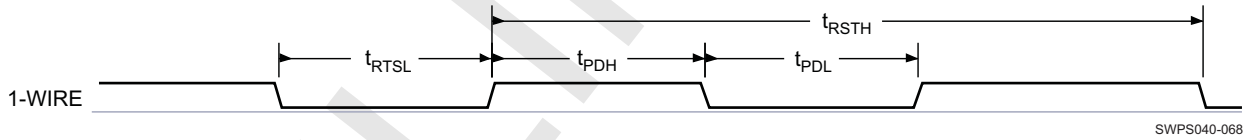


Figure 5-68. 1-Wire Reset Timing

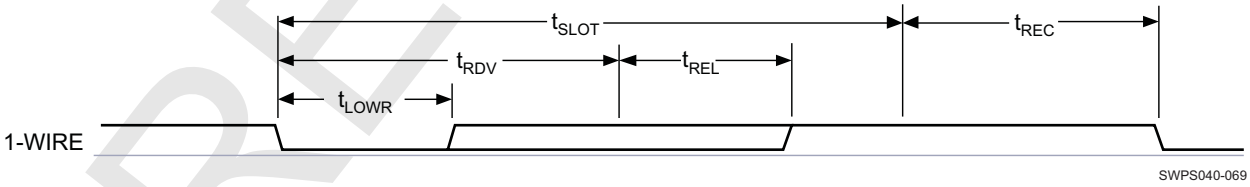


Figure 5-69. 1-Wire Bit Read Timing (Data)

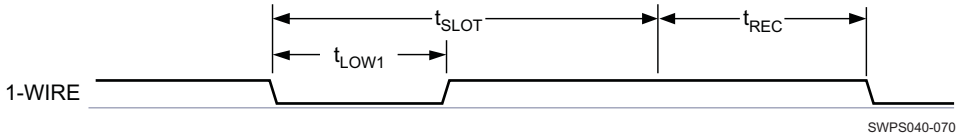


Figure 5-70. 1-Wire Bit-One Write Timing (Command / Address / Data)

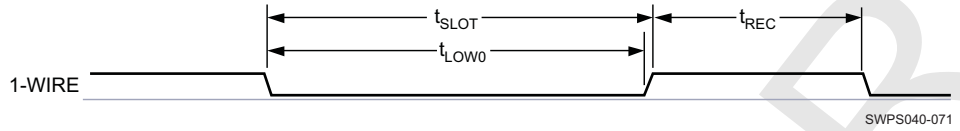


Figure 5-71. 1-Wire Bit-Zero Write Timing (Command / Address / Data)

5.6.10 Universal Asynchronous Receiver Transmitter (UART), 1.8 V

NOTE

For more information, see the Serial Communication Interface section of the OMAP543x TRM.

5.6.10.1 UART1, UART2, UART4, UART5, UART6

Table 5-105. UART1 Switching Characteristics

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	NOM	MAX	UNIT
uart1_tx (D10/AF3), uart1_rx (D9/AE3), uart1_cts (E9/AF2), uart1_rts(E10/AE2)	0 or 2	Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
			SC[1:0] = 01 (slow)	0.9		2.0	
			SC[1:0] = 10 (fast)	0.6		1.1	
			SC[1:0] = 11 (fastest)(1)	NA		NA	
		Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.75	
			SC[1:0] = 01 (slow)	1.0		2.25	
			SC[1:0] = 10 (fast)	0.7		1.4	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

Table 5-106. UART2 Switching Characteristics

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	NOM	MAX	UNIT
uart2_tx (B6), uart2_rx (C6), uart2_cts (B5), uart2_rts(C5)	0	Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
			SC[1:0] = 01 (slow)	0.9		2.0	
			SC[1:0] = 10 (fast)	0.6		1.1	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	
		Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.75	
			SC[1:0] = 01 (slow)	1.0		2.25	
			SC[1:0] = 10 (fast)	0.7		1.4	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

Table 5-107. UART4 Switching Characteristics

SIGNAL NAME	MUX MODE	DESCRIPTION	MIN	NOM	MAX	UNIT
uart4_tx (AL31), uart4_rx (AL32)	2	Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for CLOAD = 40 pF			6	ns

Table 5-107. UART4 Switching Characteristics (continued)

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	NOM	MAX	UNIT
uart4_cts (AJ32), uart4_rts (AK32)	2	Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
			SC[1:0] = 01 (slow)	0.9		2.0	
			SC[1:0] = 10 (fast)	0.6		1.1	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	
		Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.75	
			SC[1:0] = 01 (slow)	1.0		2.25	
			SC[1:0] = 10 (fast)	0.7		1.4	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

Table 5-108. UART5 Switching Characteristics

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	NOM	MAX	UNIT
uart5_tx (AE29), uart5_rx (AD30), uart5_cts (AE30), uart5_rts (AD29)	0	Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
			SC[1:0] = 01 (slow)	0.9		2.0	
			SC[1:0] = 10 (fast)	0.6		1.1	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	
		Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.75	
			SC[1:0] = 01 (slow)	1.0		2.25	
			SC[1:0] = 10 (fast)	0.7		1.4	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

Table 5-109. UART6 Switching Characteristics

SIGNAL NAME	MUX MODE	DESCRIPTION		MIN	NOM	MAX	UNIT
uart6_tx (AJ27), uart6_rx (AJ26), uart6_cts (AK26), uart6_rts (AK27)	0	Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 40 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.6	ns
			SC[1:0] = 01 (slow)	0.9		2.0	
			SC[1:0] = 10 (fast)	0.6		1.1	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	
		Output transition time (tR or tF evaluated between 10% and 90% of VPAD) for drive strength = 60 Ω and CLOAD = 10 pF	SC[1:0] = 00 (slowest)	1.6		3.75	
			SC[1:0] = 01 (slow)	1.0		2.25	
			SC[1:0] = 10 (fast)	0.7		1.4	
			SC[1:0] = 11 (fastest)(1)	N/A		N/A	
uart6_rx (E2)	4	Output transition time (tR or tF evaluated between VOL and VOH) for CLOAD = 15 pF	IC[1:0] = 00	0.4		1.32	ns
		Output transition time (tR or tF evaluated between VOL and VOH) for CLOAD = 30 pF	IC[1:0] = 00	0.7		2.75	

(1) SC[1:0] = 11 is the fastest bit setting. It is not supported.

5.6.10.2 UART3 IrDA

The IrDA module can operate in the following three modes:

- Slow infrared (SIR) (≤ 115.2 Kbits/s)
- Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
- Fast infrared (FIR) (4 Mbits/s)

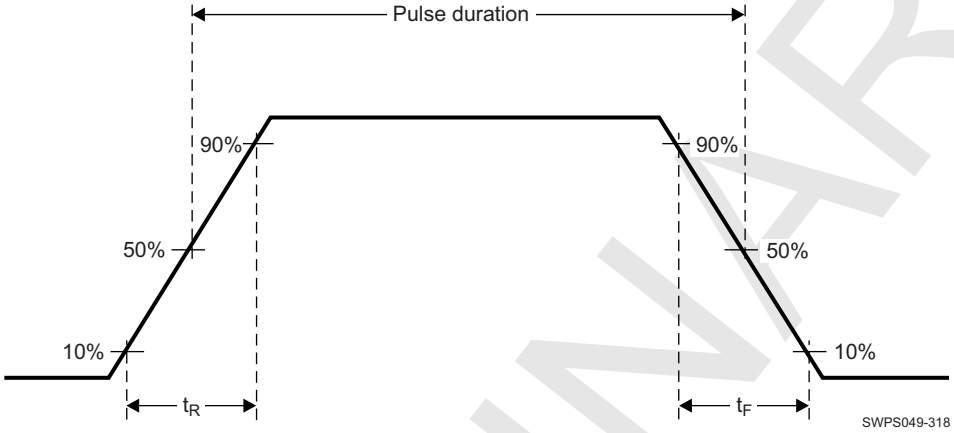


Figure 5-72. UART IrDA Pulse Parameters

5.6.10.2.1 UART3 IrDA – Receive Mode

Table 5-110. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding – Receive Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	TYP	MAX	
SIR				
2.4 Kbit/s	52.17	78.13	208.33	µs
9.6 Kbit/s	13.10	19.53	52.08	µs
19.2 Kbit/s	6.59	9.77	26.04	µs
38.4 Kbit/s	3.34	4.88	13.02	µs
57.6 Kbit/s	2.25	3.26	8.68	µs
115.2 Kbit/s	1.17	1.63	4.34	µs
MIR				
0.576 Mbit/s	300.55	416.67	867.86	ns
1.152 Mbit/s	192.04	208.33	433.83	ns
FIR				
4.0 Mbit/s (Single pulse)	62.70	125.00	170.63	ns
4.0 Mbit/s (Double pulse)	208.53	250.00	291.47	ns

NOTE

In SIR Receive mode, both the 3/16th and the 1.6µs pulse duration methods are supported. For more information, see the UART/IrDA/CIR section of the Serial Communication Interface chapter in the OMAP543x TRM.

Table 5-111. UART3 IrDA Rise and Fall Times – Receive Mode

PARAMETER		MIN	TYP	MAX	UNIT
t_R	Rise time, input data uart3_rx_irrx			200	ns
t_F	Fall time, input data uart3_rx_irrx			200	ns

5.6.10.2.2 UART3 IrDA – Transmit Mode

Table 5-112. UART3 IrDA Signaling Rate and Pulse Duration with 3/16th Encoding – Transmit Mode

SIGNALING RATE	ELECTRICAL PULSE DURATION			UNIT
	MIN	TYP	MAX	
SIR				
2.4 Kbit/s	78.1	78.1	78.1	µs
9.6 Kbit/s	19.5	19.5	19.5	µs
19.2 Kbit/s	9.75	9.75	9.75	µs
38.4 Kbit/s	4.87	4.87	4.87	µs
57.6 Kbit/s	3.25	3.25	3.25	µs
115.2 Kbit/s	1.62	1.62	1.62	µs
MIR				
0.576 Mbit/s	414	416	419	ns
1.152 Mbit/s	206	208	211	ns
FIR				
4.0 Mbit/s (Single pulse)	123	125	128	ns
4.0 Mbit/s (Double pulse)	248	250	253	ns

NOTE

In SIR Receive mode, both the 3/16th and the 1.6µs pulse duration methods are supported. For more information, see the UART/IrDA/CIR section of the Serial Communication Interface chapter in the OMAP543x TRM.

5.6.11 Serial Advanced Technology Attachment (SATA), 1.8 V

NOTE

For more information, see the SATA Controller section of the OMAP543x TRM.

The SATA RX/TX PHY interface is compliant with the SATA standard v2.6 for a maximum data rate:

- Gen2i, Gen2m, Gen2x: 3Gbps at OPP_NOM.
- Gen1i, Gen1m, Gen1x: 1.5Gbps at OPP_NOM.

5.6.12 MMC2—eMMC, 1.2 V and 1.8 V

NOTE

For more information, see the MMC/SDIO chapter of the OMAP543x TRM.

MMC2 interface is compliant with the JC64 eMMC Standard v4.5 and it supports the following eMMC applications:

- Standard JC64 SDR at 24 MHz, 8-bit data, half cycle, 1.2 V and 1.8 V
- High-speed JC64 SDR at 48 MHz, 8-bit data, half cycle, 1.2 V and 1.8 V
- High-speed HS200 JC64 SDR at 192 MHz, 8-bit data, half cycle, 1.2 V and 1.8 V
- High-speed JC64 DDR at 48 MHz, 8-bit data, 1.2 V and 1.8 V

5.6.12.1 eMMC, Standard JC64 SDR, 24 MHz, Half Cycle, 1.8 V

Table 5-113. Standard JC64 SDR eMMC Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.13	1.6	ns
t_F	Input fall time	0.13	1.6	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-114 and Table 5-115 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-114. Standard JC64 SDR eMMC Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
STDeMMC5	$t_{su(dV-clkH)}$	Setup time, emmc_cmd valid before emmc_clk rising edge	2.9		ns
STDeMMC6	$t_{h(clkH-dV)}$	Hold time, emmc_cmd valid after emmc_clk rising edge	20.1		ns
STDeMMC7	$t_{su(dV-clkH)}$	Setup time, emmc_data[7:0] valid before emmc_clk rising edge	2.9		ns
STDeMMC8	$t_{h(clkH-dV)}$	Hold time, emmc_data[7:0] valid after emmc_clk rising edge	20.1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-115. Standard JC64 SDR eMMC Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
STDeMMC1	1 / $t_{c(clk)}$	Frequency, output emmc_clk		24	MHz
STDeMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
STDeMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		2083	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		65	ps
	$t_{R(clk)}$	Rise time, output emmc_clk		2263	ps
	$t_{F(clk)}$	Fall time, output emmc_clk		2136	ps
STDeMMC3	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_cmd transition	–14.4	14.4	ns
	$t_{R(do)}$	Rise time, output emmc_cmd		2263	ps
	$t_{F(do)}$	Fall time, output emmc_cmd		2136	ps
STDeMMC4	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_data[7:0] transition	–14.4	14.4	ns

Table 5-115. Standard JC64 SDR eMMC Switching Characteristics—1.8 V(3) (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$t_{R(do)}$	Rise time, output emmc_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]		2136	ps

(1) P = output emmc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

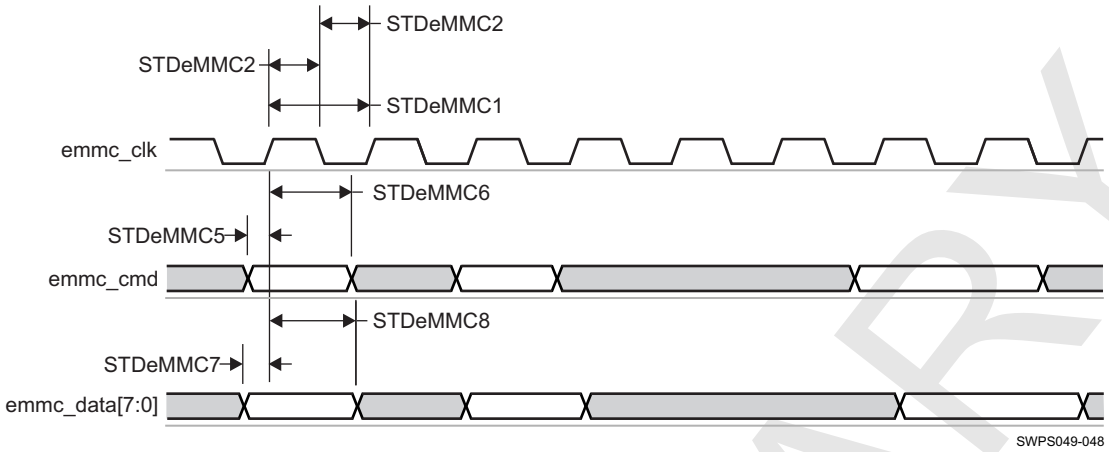


Figure 5-73. Standard JC64 SDR eMMC, 1.8 V—Receiver Mode

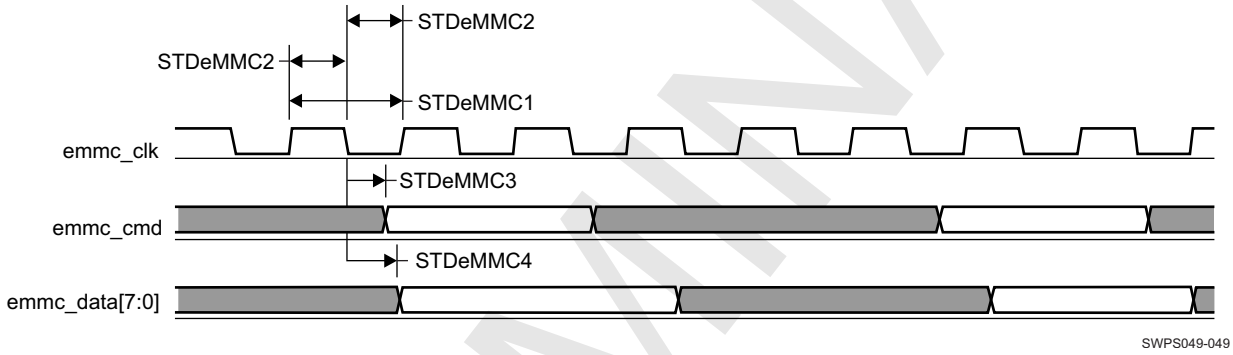


Figure 5-74. Standard JC64 SDR eMMC, 1.8 V—Transmitter Mode

5.6.12.2 eMMC, Standard JC64 SDR, 24 MHz, Half Cycle, 1.2 V

Table 5-116. Standard JC64 SDR eMMC Timing Conditions—1.2 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.13	1.6	ns
t_F	Input fall time	0.13	1.6	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-117 and Table 5-118 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-117. Standard JC64 SDR eMMC Timing Requirements—1.2 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
STDeMMC5	$t_{su(dV-clkH)}$	Setup time, emmc_cmd valid before emmc_clk rising edge	3.1		ns
STDeMMC6	$t_{h(clkH-dV)}$	Hold time, emmc_cmd valid after emmc_clk rising edge	19.8		ns
STDeMMC7	$t_{su(dV-clkH)}$	Setup time, emmc_data[7:0] valid before emmc_clk rising edge	3.1		ns
STDeMMC8	$t_{h(clkH-dV)}$	Hold time, emmc_data[7:0] valid after emmc_clk rising edge	19.8		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-118. Standard JC64 SDR eMMC Switching Characteristics—1.2 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
STDeMMC1	$1 / t_{c(clk)}$	Frequency, output emmc_clk		24	MHz
STDeMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
STDeMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		2083	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		65	ps
	$t_{R(clk)}$	Rise time, output emmc_clk		2263	ps
	$t_{F(clk)}$	Fall time, output emmc_clk		2136	ps
STDeMMC3	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_cmd transition	–14.4	14.4	ns
	$t_{R(do)}$	Rise time, output emmc_cmd		2263	ps
	$t_{F(do)}$	Fall time, output emmc_cmd		2136	ps
STDeMMC4	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_data[7:0] transition	–14.4	14.4	ns
	$t_{R(do)}$	Rise time, output emmc_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]		2136	ps

(1) P = output emmc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

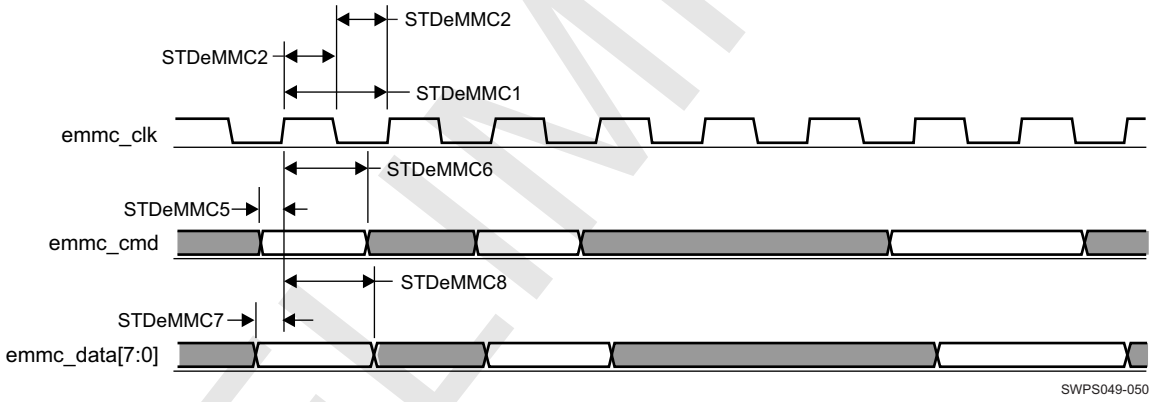


Figure 5-75. Standard JC64 SDR eMMC, 1.2 V—Receiver Mode

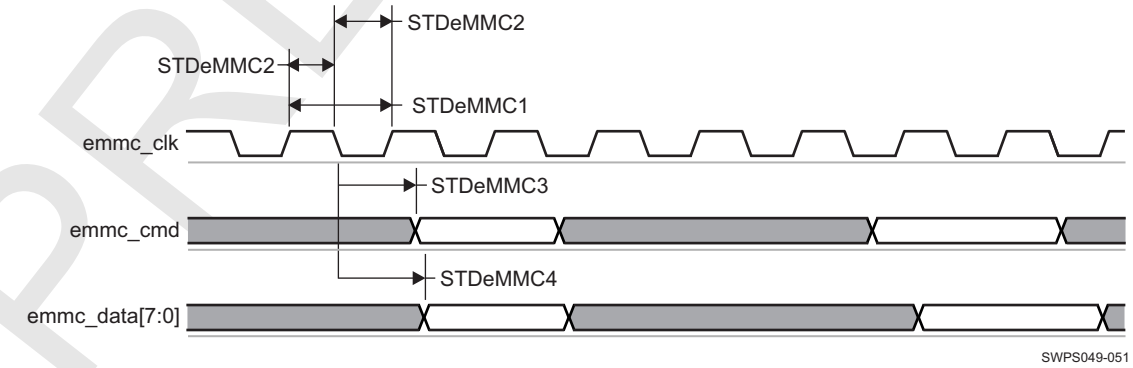


Figure 5-76. Standard JC64 SDR eMMC, 1.2 V—Transmitter Mode

5.6.12.3 eMMC, High-Speed JC64 SDR, 48 MHz, Half Cycle, 1.8 V

Table 5-119. High-Speed JC64 SDR eMMC Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.13	1.6	ns
t_F	Input fall time	0.13	1.6	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-120 and Table 5-121 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-120. High-Speed JC64 SDR eMMC Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSeMMC3	$t_{su(dV-clkH)}$	Setup time, emmc_cmd valid before emmc_clk rising edge	5.8		ns
HSeMMC4	$t_{h(clkH-dV)}$	Hold time, emmc_cmd valid after emmc_clk rising edge	1.9		ns
HSeMMC7	$t_{su(dV-clkH)}$	Setup time, emmc_data[7:0] valid before emmc_clk rising edge	5.8		ns
HSeMMC8	$t_{h(clkH-dV)}$	Hold time, emmc_data[7:0] valid after emmc_clk rising edge	1.9		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-121. High-Speed JC64 SDR eMMC Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSeMMC1	$1 / t_{c(clk)}$	Frequency, output emmc_clk		48	MHz
HSeMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
HSeMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		65	ps
	$t_{R(clk)}$	Rise time, output emmc_clk		2263	ps
	$t_{F(clk)}$	Fall time, output emmc_clk		2136	ps
HSeMMC5	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_cmd transition	–6.6	6.6	ns
	$t_{R(do)}$	Rise time, output emmc_cmd		2263	ps
	$t_{F(do)}$	Fall time, output emmc_cmd		2136	ps
HSeMMC6	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_data[7:0] transition	–6.6	6.6	ns
	$t_{R(do)}$	Rise time, output emmc_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]		2136	ps

(1) P = output emmc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

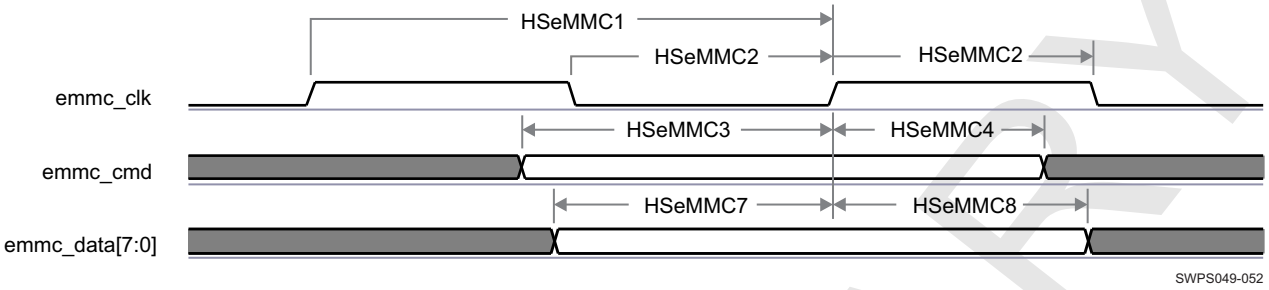


Figure 5-77. High-Speed JC64 SDR eMMC, 1.8 V—Receiver Mode

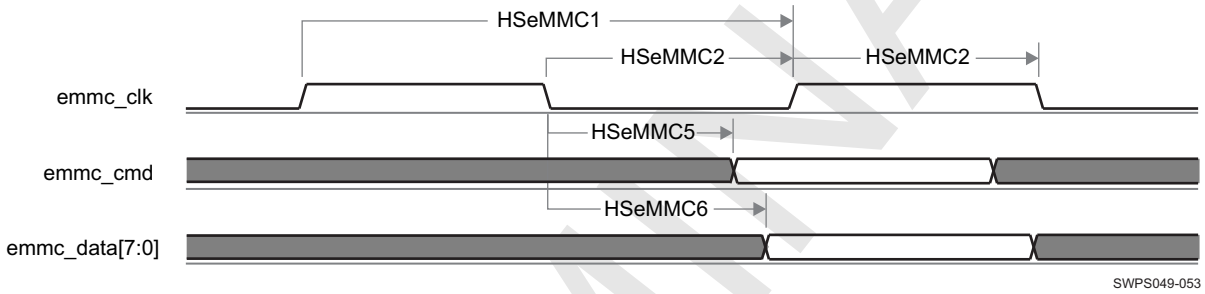


Figure 5-78. High- Speed JC64 SDR eMMC, 1.8 V—Transmitter Mode

5.6.12.4 eMMC, High-Speed JC64 SDR, 48 MHz, Half Cycle, 1.2 V

Table 5-122. High-Speed JC64 SDR eMMC Timing Conditions—1.2 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.13	1.6	ns
t_F	Input fall time	0.13	1.6	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-123 and Table 5-124 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-123. High-Speed JC64 SDR eMMC Timing Requirements—1.2 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSeMMC3	$t_{su(dV-clkH)}$	Setup time, emmc_cmd valid before emmc_clk rising edge	5.6		ns
HSeMMC4	$t_{h(clkH-dV)}$	Hold time, emmc_cmd valid after emmc_clk rising edge	1.0		ns
HSeMMC7	$t_{su(dV-clkH)}$	Setup time, emmc_data[7:0] valid before emmc_clk rising edge	5.6		ns
HSeMMC8	$t_{h(clkH-dV)}$	Hold time, emmc_data[7:0] valid after emmc_clk rising edge	1.0		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-124. High-Speed JC64 SDR eMMC Switching Characteristics—1.2 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSeMMC1	$1 / t_{c(clk)}$	Frequency, output emmc_clk		48	MHz
HSeMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
HSeMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		65	ps
	$t_{R(clk)}$	Rise time, output emmc_clk		2263	ps
	$t_{F(clk)}$	Fall time, output emmc_clk		2136	ps
HSeMMC5	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_cmd transition	–5.9	5.9	ns
	$t_{R(do)}$	Rise time, output emmc_cmd		2263	ps
	$t_{F(do)}$	Fall time, output emmc_cmd		2136	ps
HSeMMC6	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_data[7:0] transition	–5.9	5.9	ns
	$t_{R(do)}$	Rise time, output emmc_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]		2136	ps

(1) P = output emmc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

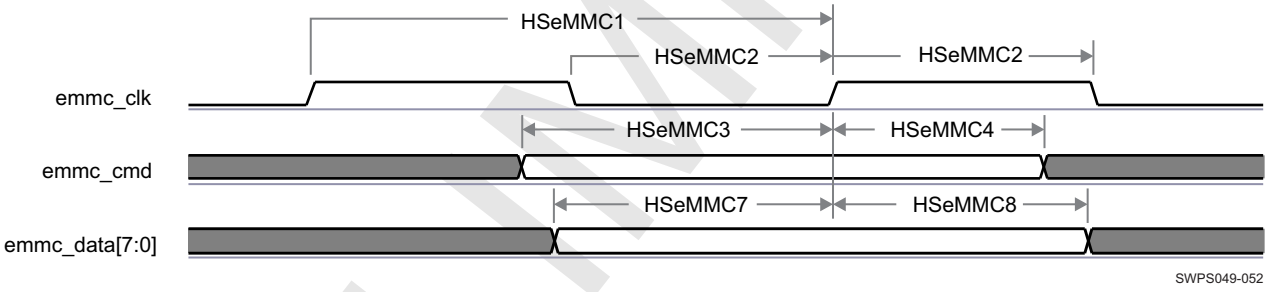


Figure 5-79. High-Speed JC64 SDR eMMC, 1.2 V—Receiver Mode

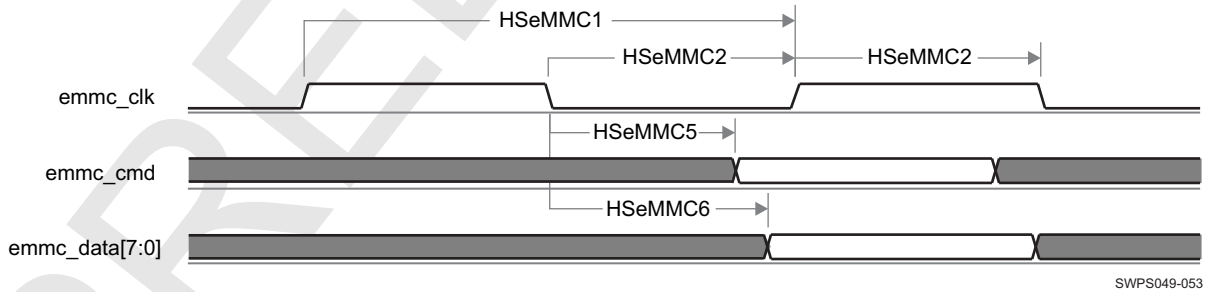


Figure 5-80. High-Speed JC64 SDR eMMC, 1.2 V—Transmitter Mode

5.6.12.5 eMMC, High-Speed HS200 JC64 SDR, 192 MHz, Half Cycle, 1.8 V

Table 5-125. High-Speed HS200 JC64 SDR eMMC Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time		0.39	ns
t_F	Input fall time		0.39	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-126 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-126. High-Speed HS200 JC64 SDR eMMC Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HS200eMMC1	$1 / t_{c(clk)}$	Frequency, output emmc_clk		192	MHz
HS200eMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
HS200eMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		260	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		42	ps
	$t_{R(clk)}$	Rise time, output emmc_clk	140	390	ps
	$t_{F(clk)}$	Fall time, output emmc_clk	161	356	ps
HS200eMMC5	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_cmd transition	–1.2	0.4	ns
	$t_{R(do)}$	Rise time, output emmc_cmd	140	390	ps
	$t_{F(do)}$	Fall time, output emmc_cmd	161	356	ps
HS200eMMC6	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_data[7:0] transition	–1.2	0.4	ns
	$t_{F(do)}$	Rise time, output emmc_data[7:0]	140	390	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]	161	356	ps

(1) P = output emmc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

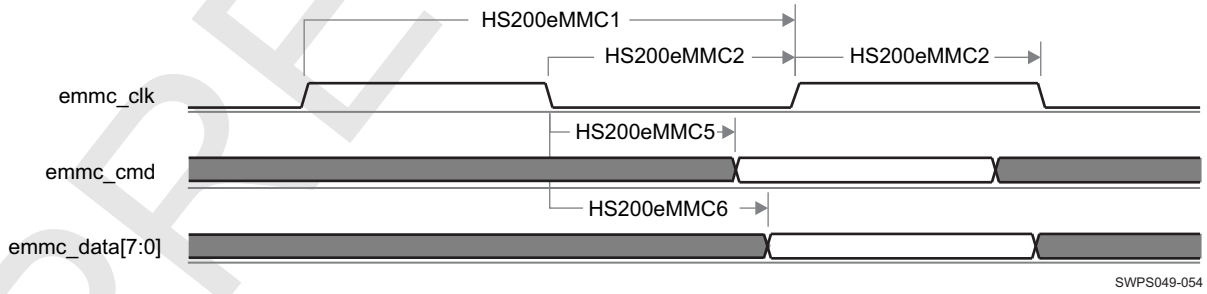


Figure 5-81. High-Speed HS200 JC64 SDR eMMC, 1.8 V—Transmitter Mode

5.6.12.6 eMMC, High-Speed HS200 JC64 SDR, 192 MHz, Half Cycle, 1.2 V

Table 5-127. High-Speed HS200 JC64 SDR eMMC Timing Conditions—1.2 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time		0.45	ns
t_F	Input fall time		0.45	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-128 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-128. High-Speed HS200 JC64 SDR eMMC Switching Characteristics—1.2 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HS200eMMC1	$1 / t_{c(clk)}$	Frequency, output emmc_clk		192	MHz
HS200eMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
HS200eMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		260	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		42	ps
	$t_{R(clk)}$	Rise time, output emmc_clk	125	445	ps
	$t_{F(clk)}$	Fall time, output emmc_clk	147	351	ps
HS200eMMC5	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_cmd transition	–1.0	0.3	ns
	$t_{R(do)}$	Rise time, output emmc_cmd	125	445	ps
	$t_{F(do)}$	Fall time, output emmc_cmd	147	351	ps
HS200eMMC6	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling edge to emmc_data[7:0] transition	–1.0	0.3	ns
	$t_{R(do)}$	Rise time, output emmc_data[7:0]	125	445	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]	147	351	ps

(1) P = output emmc_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

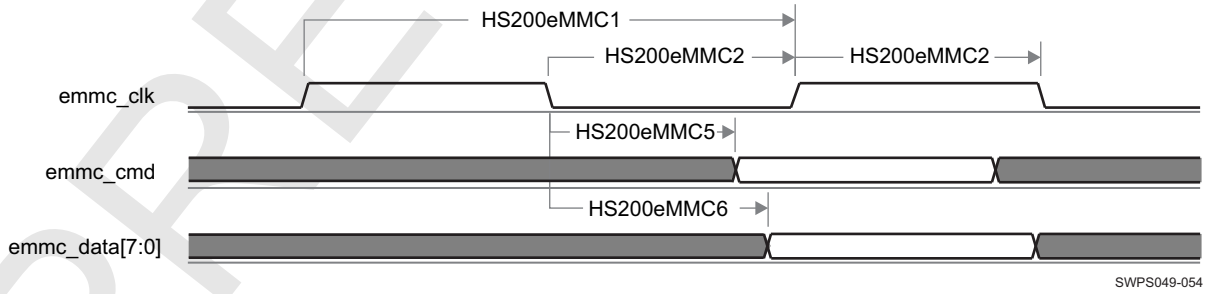


Figure 5-82. High-Speed HS200 JC64 SDR eMMC, 1.2 V—Transmitter Mode

5.6.12.7 eMMC, High-Speed JC64 DDR, 48 MHz, 1.8 V

Table 5-129. High-Speed JC64 DDR eMMC Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input command signal rise time	0.33	0.64	ns
t_F	Input command signal fall time	0.33	0.76	ns
t_R	Input data signal rise time	0.38	2.26	ns
t_F	Input data signal fall time	0.37	2.54	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-130 and Table 5-131 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-130. High-Speed JC64 DDR eMMC Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
DDReMMC3	$t_{su(dV-clkH)}$	Setup time, emmc_cmd valid before emmc_clk rising edge	5.9		ns
DDReMMC4	$t_{h(clkH-dV)}$	Hold time, emmc_cmd valid after emmc_clk rising edge	1.9		ns
DDReMMC7	$t_{su(dV-clkH)}$	Setup time, emmc_data[7:0] valid before emmc_clk falling/rising edge	2.3		ns
DDReMMC8	$t_{h(clkH-dV)}$	Hold time, emmc_data[7:0] valid after emmc_clk falling/rising edge	0.4		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-131. High-Speed JC64 DDR eMMC Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
DDReMMC1	1 / $t_{c(clk)}$	Frequency, output emmc_clk		48	MHz
DDReMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
DDReMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		65	ps
	$t_{R(clk)}$	Rise time, output emmc_clk		2263	ps
	$t_{F(clk)}$	Fall time, output emmc_clk		2136	ps
DDReMMC5	$t_{d(clkL-doV)}$	Delay time, emmc_clk rising edge to emmc_cmd transition	3.5	16.9	ns
	$t_{R(do)}$	Rise time, output emmc_cmd		2263	ps
	$t_{F(do)}$	Fall time, output emmc_cmd		2136	ps
DDReMMC6	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling/rising edge to emmc_data[7:0] transition	3.0	7.1	ns
	$t_{R(do)}$	Rise time, output emmc_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]		2136	ps

(1) P = output emmc_clk period in ns
(2) The jitter probability density can be approximated by a Gaussian function.
(3) See DM Operating Condition Addendum for CORE OPP voltages.

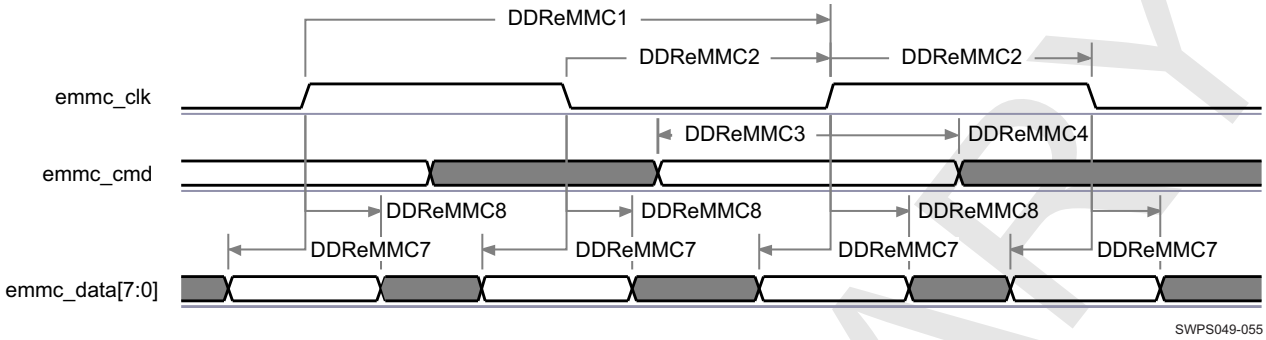


Figure 5-83. High-Speed JC64 DDR eMMC, 1.8 V—Receiver Mode

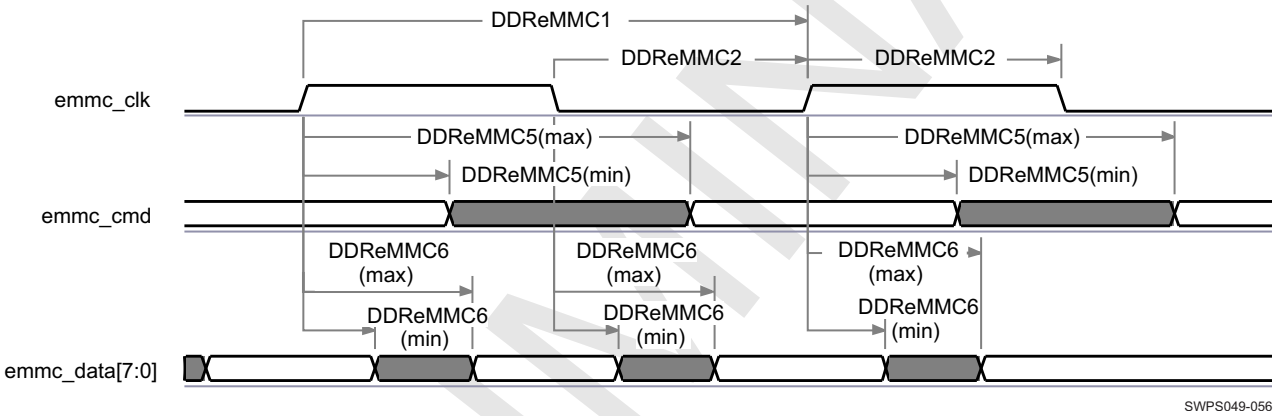


Figure 5-84. High-Speed JC64 DDR eMMC, 1.8 V—Transmitter Mode

5.6.12.8 eMMC, High-Speed JC64 DDR, 48 MHz, 1.2 V

Table 5-132. High-Speed JC64 DDR eMMC Timing Conditions—1.2 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input command signal rise time	0.13	1.6	ns
t_F	Input command signal fall time	0.13	1.6	ns
t_R	Input data signal rise time	0.38	2.26	ns
t_F	Input data signal fall time	0.37	2.54	ns
Output Conditions(1)				

(1) See Table 8-15, *eMMC PCB Requirements and IO Programming*.

Table 5-133 and Table 5-134 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-133. High-Speed JC64 DDR eMMC Timing Requirements—1.2 V(1)

NO.	PARAME TER		OPP_NOM		UNIT
			MIN	MAX	
DDReMMC3	$t_{su(dV-clkH)}$	Setup time, emmc_cmd valid before emmc_clk rising edge	5.6		ns
DDReMMC4	$t_{h(clkH-dV)}$	Hold time, emmc_cmd valid after emmc_clk rising edge	1.0		ns
DDReMMC7	$t_{su(dV-clkH)}$	Setup time, emmc_data[7:0] valid before emmc_clk falling or rising edge	2.5		ns
DDReMMC8	$t_{h(clkH-dV)}$	Hold time, emmc_data[7:0] valid after emmc_clk falling or rising edge	–0.5		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-134. High-Speed JC64 DDR eMMC Switching Characteristics—1.2 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
DDReMMC1	1 / $t_{c(clk)}$	Frequency, output emmc_clk		48	MHz
DDReMMC2	$t_{W(clkH)}$	Typical pulse duration, output emmc_clk high	0.5 × P(1)		ns
DDReMMC2	$t_{W(clkL)}$	Typical pulse duration, output emmc_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output emmc_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output emmc_clk		65	ps
	$t_{R(clk)}$	Rise time, output emmc_clk		2263	ps
	$t_{F(clk)}$	Fall time, output emmc_clk		2136	ps
DDReMMC5	$t_{d(clkL-doV)}$	Delay time, emmc_clk rising edge to emmc_cmd transition	3.8	16.6	ns
	$t_{R(do)}$	Rise time, output emmc_cmd		2263	ps
	$t_{F(do)}$	Fall time, output emmc_cmd		2136	ps
DDReMMC6	$t_{d(clkL-doV)}$	Delay time, emmc_clk falling/rising edge to emmc_data[7:0] transition	3.3	6.8	ns
	$t_{R(do)}$	Rise time, output emmc_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output emmc_data[7:0]		2136	ps

(1) P = output emmc_clk period in ns
(2) The jitter probability density can be approximated by a Gaussian function.
(3) See DM Operating Condition Addendum for CORE OPP voltages.

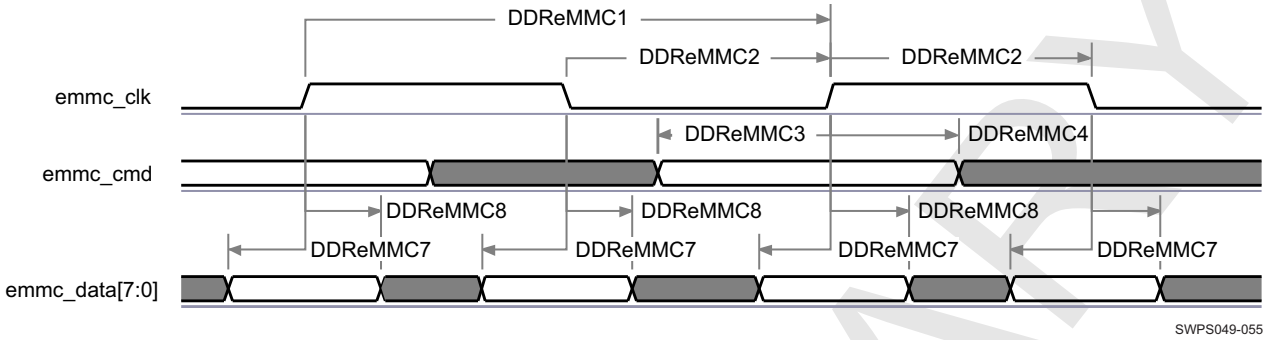


Figure 5-85. High-Speed JC64 DDR eMMC, 1.2 V—Receiver Mode

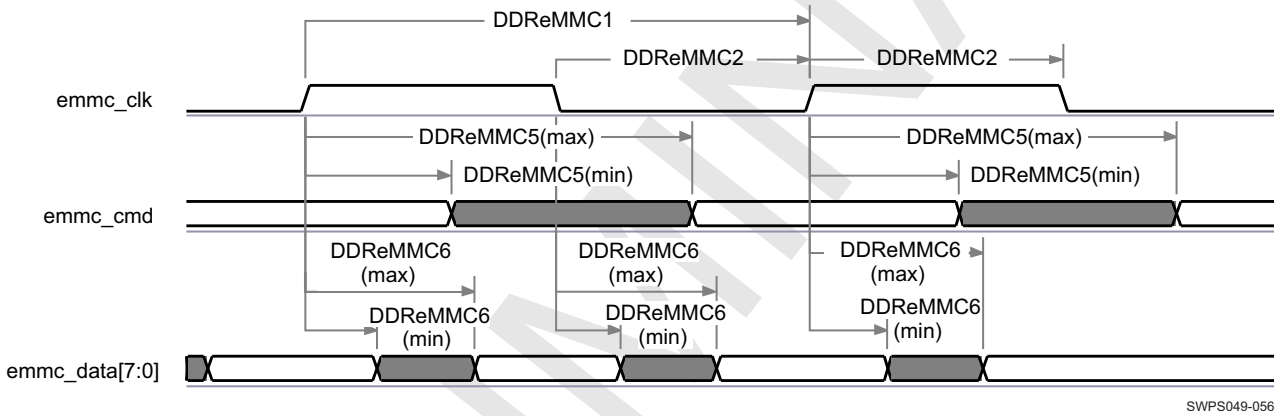


Figure 5-86. High-Speed JC64 DDR eMMC, 1.2 V—Transmitter Mode

5.6.13 MMC3, MMC4, and MMC5—SDIO, 1.8 V

NOTE

For more information, see the MMC/SDIO chapter of the OMAP543x TRM.

MMC3, MMC4 and MMC5 interfaces are compliant with the SDIO3.0 standard v1.0, SD Part E1 and for generic SDIO devices, it supports the following applications:

- SDIO Standard speed at 24 MHz (SDR12 mode of the SD Standard v3.01), 4-bit data, SDR, half cycle, 1.8 V
- SDIO High speed at 48 MHz (SDR25 mode of the SD Standard v3.01), 4-bit data, SDR, half cycle, 1.8 V

MMC5 interface is compliant with the SDIO3.0 standard v1.0, SD Part E1 and for modem devices, it supports the following application:

- SDIO High Speed at 96 MHz (UHS-I SDR50 mode of the SD Standard v3.01) 8-bit data, half cycle, 1.8 V

5.6.13.1 MMC3, MMC4, and MMC5, SDIO Standard Speed (SDR12), 24 MHz, Half Cycle, 1.8 V

Table 5-135. SDIO Standard Speed Timing Conditions —1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.14	3.14	ns
t_F	Input fall time	0.14	3.15	ns
Output Conditions(1)				

(1) See Table 8-9, *WLSDIO PCB Requirements and IO Programming*, Table 8-11, *SDIO4 PCB Requirements and IO Programming*, and Table 8-13, *SDIO5 PCB Requirements and IO Programming*.

Table 5-136 and Table 5-137 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-136. SDIO Standard Speed Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SDIO5	$t_{su(dV-clkH)}$	Setup time, sdio_cmd valid before sdio_clk rising edge	2.5		ns
SDIO6	$t_{h(clkH-dV)}$	Hold time, sdio_cmd valid after sdio_clk rising edge	16		ns
SDIO7	$t_{su(dV-clkH)}$	Setup time, sdio_data[3:0] valid before sdio_clk rising edge	2.5		ns
SDIO8	$t_{h(clkH-dV)}$	Hold time, sdio_data[3:0] valid after sdio_clk rising edge	16		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-137. SDIO Standard Speed Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SDIO1	$1 / t_{c(clk)}$	Frequency, output sdio_clk		24	MHz
SDIO2	$t_{W(clkH)}$	Typical pulse duration, output sdio_clk high	0.5 × P(1)		ns
SDIO2	$t_{W(clkL)}$	Typical pulse duration, output sdio_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdio_clk		2083	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdio_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdio_clk		2263	ps
	$t_{F(clk)}$	Fall time, output sdio_clk		2136	ps

Table 5-137. SDIO Standard Speed Switching Characteristics—1.8 V(3) (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SDIO3	$t_{d(clkL-doV)}$	Delay time, sdio_clk falling edge to sdio_cmd transition	–13.9	9.9	ns
	$t_{R(do)}$	Rise time, output sdio_cmd		2263	ps
	$t_{F(do)}$	Fall time, output sdio_cmd		2136	ps
SDIO4	$t_{d(clkL-doV)}$	Delay time, sdio_clk falling edge to sdio_data[3:0] transition	–13.9	9.9	ns
	$t_{R(do)}$	Rise time, output sdio_data[3:0]		2263	ps
	$t_{F(do)}$	Fall time, output sdio_data[3:0]		2136	ps

(1) P = output sdio_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

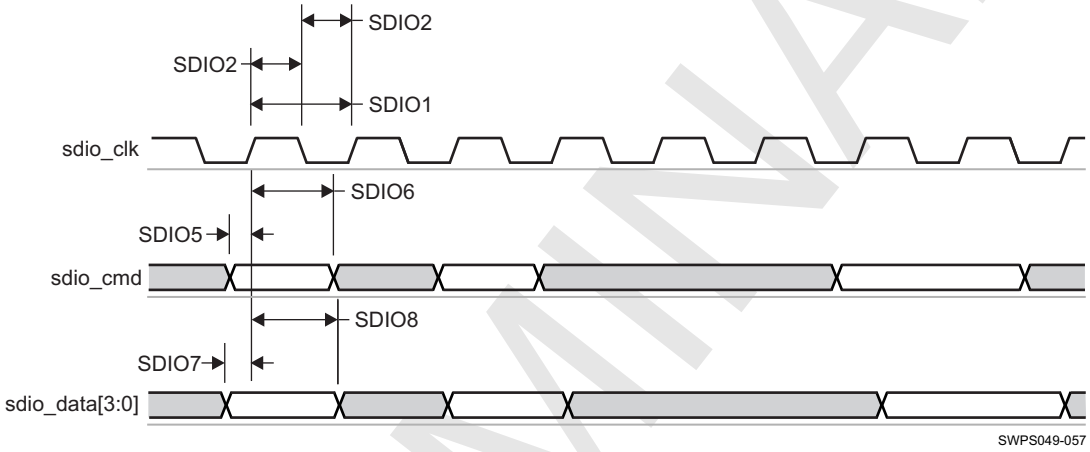


Figure 5-87. SDIO Standard Speed, 1.8 V—Receiver Mode

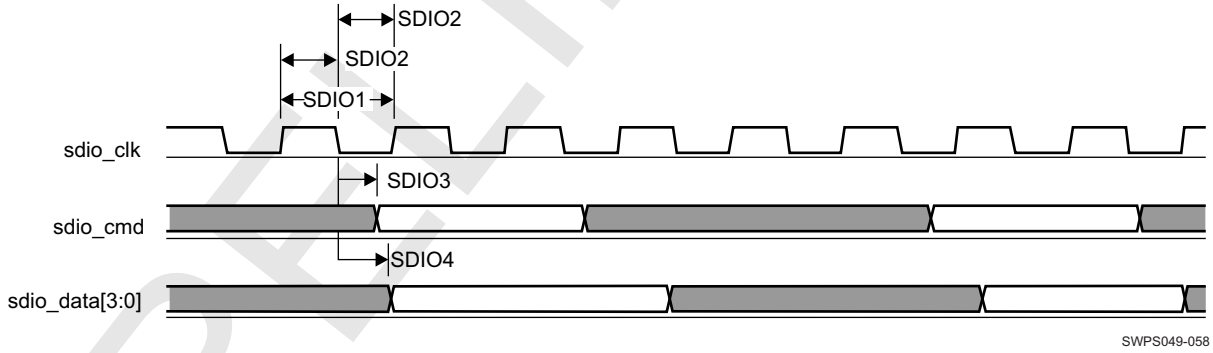


Figure 5-88. SDIO Standard Speed, 1.8 V—Transmitter Mode

5.6.13.2 MMC3, MMC4, and MMC5, SDIO High-Speed (SDR25), 48 MHz, Half Cycle, 1.8 V

Table 5-138. SDIO High-Speed Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.14	3.14	ns
t_F	Input fall time	0.14	3.15	ns
Output Conditions(1)				

(1) See Table 8-9, *WLSDIO PCB Requirements and IO Programming*, Table 8-11, *SDIO4 PCB Requirements and IO Programming*, and Table 8-13, SDIO5 PCB Requirements and IO Programming.

Table 5-139 and Table 5-140 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-139. SDIO High-Speed Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDIO3	$t_{su(dV-clkH)}$	Setup time, sdio_cmd valid before sdio_clk rising edge	4.9		ns
HSSDIO4	$t_{h(clkH-dV)}$	Hold time, sdio_cmd valid after sdio_clk rising edge	2.0		ns
HSSDIO7	$t_{su(dV-clkH)}$	Setup time, sdio_data[3:0] valid before sdio_clk rising edge	4.9		ns
HSSDIO8	$t_{h(clkH-dV)}$	Hold time, sdio_data[3:0] valid after sdio_clk rising edge	2.0		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-140. SDIO High-Speed Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDIO1	$t_{c(clk)}$	Frequency, output sdio_clk		48	MHz
HSSDIO2	$t_{W(clkH)}$	Typical pulse duration, output sdio_clk high	0.5 × P(1)		ns
HSSDIO2	$t_{W(clkL)}$	Typical pulse duration, output sdio_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdio_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdio_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdio_clk		2263	ps
	$t_{F(clk)}$	Fall time, output sdio_clk		2136	ps
HSSDIO5	$t_{d(clkL-doV)}$	Delay time, sdio_clk falling edge to sdio_cmd transition	–5.3	1.3	ns
	$t_{R(do)}$	Rise time, output sdio_cmd		2263	ps
	$t_{F(do)}$	Fall time, output sdio_cmd		2136	ps
HSSDIO6	$t_{d(clkL-doV)}$	Delay time, sdio_clk falling edge to sdio_data[3:0] transition	–5.3	1.3	ns
	$t_{R(do)}$	Rise time, output sdio_data[3:0]		2263	ps
	$t_{F(do)}$	Fall time, output sdio_data[3:0]		2136	ps

(1) P = output sdio_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

Figure 5-89. SDIO High-Speed, 1.8 V—Receiver Mode

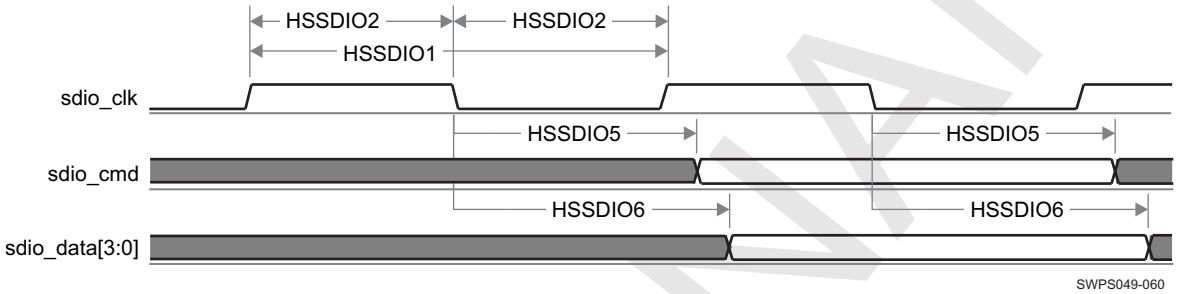


Figure 5-90. SDIO High-Speed, 1.8 V—Transmitter Mode

5.6.13.3 MMC5, SDIO High-Speed (UHS-I SDR50), 96 MHz, Half Cycle, 1.8 V

Table 5-141. SDIO High-Speed SDR50 Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	0.13	1.83	ns
t_F	Input fall time	0.13	1.83	ns
Output Conditions(1)				

(1) See Table 8-13.

Table 5-142 and Table 5-143 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-142. SDIO High-Speed SDR50 Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SDR503	$t_{su(dV-clkH)}$	Setup time, sdio5_cmd valid before sdio5_clk rising edge	1.5		ns
SDR504	$t_{h(clkH-dV)}$	Hold time, sdio5_cmd valid after sdio5_clk rising edge	1.1		ns
SDR507	$t_{su(dV-clkH)}$	Setup time, sdio5_data[7:0] valid before sdio5_clk rising edge	1.5		ns
SDR508	$t_{h(clkH-dV)}$	Hold time, sdio5_data[7:0] valid after sdio5_clk rising edge	1.1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-143. SDIO High-Speed SDR50 Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SDR501	$1 / t_{c(clk)}$	Frequency, output sdio5_clk		96	MHz
SDR502	$t_{W(clkH)}$	Typical pulse duration, output sdio5_clk high	0.5 × P(1)		ns
SDR502	$t_{W(clkL)}$	Typical pulse duration, output sdio5_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdio5_clk		521	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdio5_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdio5_clk		2263	ps
	$t_{F(clk)}$	Fall time, output sdio5_clk		2136	ps
SDR505	$t_{d(clkL-doV)}$	Delay time, sdio5_clk falling edge to sdio5_cmd transition	–3.0	0.8	ns
	$t_{R(do)}$	Rise time, output sdio5_cmd		2263	ps
	$t_{F(do)}$	Fall time, output sdio5_cmd		2136	ps
SDR506	$t_{d(clkL-doV)}$	Delay time, sdio5_clk falling edge to sdio5_data[7:0] transition	–3.0	0.8	ns
	$t_{R(do)}$	Rise time, output sdio5_data[7:0]		2263	ps
	$t_{F(do)}$	Fall time, output sdio5_data[7:0]		2136	ps

(1) P = output sdio5_clk period in ns
(2) The jitter probability density can be approximated by a Gaussian function.
(3) See DM Operating Condition Addendum for CORE OPP voltages.

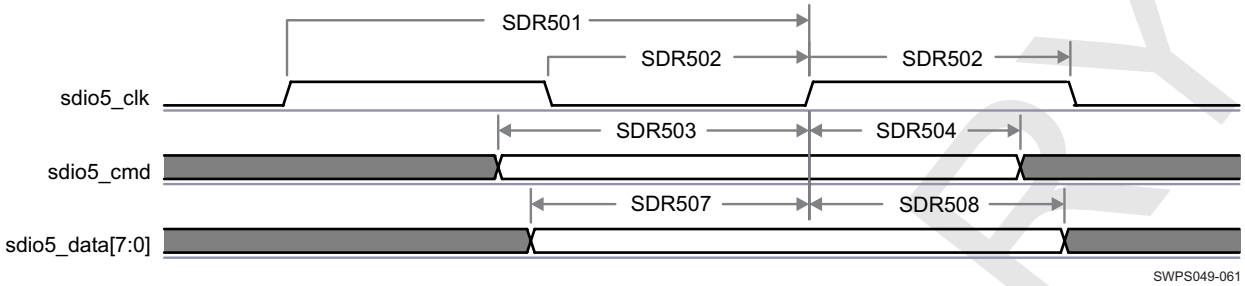


Figure 5-91. SDIO High-Speed SDR50, 1.8 V—Receiver Mode

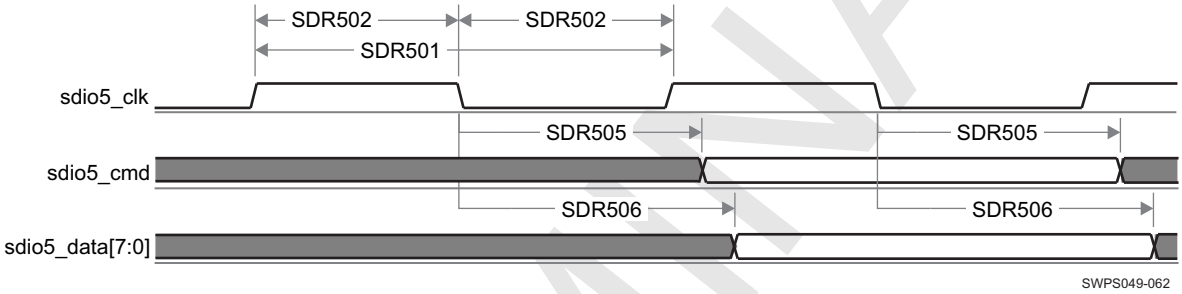


Figure 5-92. SDIO High-Speed SDR50, 1.8 V—Transmitter Mode

5.7 Removable Media Interfaces

5.7.1 MMC1—SD Card Interface, 1.8 V and 3.0 V

NOTE

For more information, see the MMC/SDIO chapter of the OMAP543x TRM.

MMC1 interface is compliant with the SD Standard v3.01 and it supports the following SD Card applications:

- Default speed at 24 MHz, 4-bit data, SDR, half-cycle, 3.3 V
- High speed at 48 MHz, 4-bit data, SDR, half-cycle, 3.3 V
- SDR12 at 24 MHz, 4-bit data, half-cycle, 1.8 V
- SDR25 at 48 MHz, 4-bit data, half-cycle, 1.8 V
- UHS-I SDR50 at 96 MHz, 4-bit data, half-cycle, 1.8 V
- UHS-I SDR104 at 192 MHz, 4-bit data, half-cycle, 1.8 V
- UHS-I DDR50 at 48 MHz, 4-bit data, 1.8 V

5.7.1.1 SD Card, Default Speed (DS), SDR, 24 MHz, Half-Cycle Mode, 3.3 V

Table 5-144. Default Speed SD Card Timing Conditions—3.3 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	1345	5283	ps
t_F	Input fall time	1345	5283	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-145 and Table 5-146 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-145. Default Speed SD Card Timing Requirements—3.3 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SSD5	$t_{su(dV-clkH)}$	Setup time, sdcard_cmd valid before sdcard_clk rising edge	2.1		ns
SSD6	$t_{h(clkH-dV)}$	Hold time, sdcard_cmd valid after sdcard_clk rising edge	19.1		ns
SSD7	$t_{su(dV-clkH)}$	Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge	2.1		ns
SSD8	$t_{h(clkH-dV)}$	Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge	19.1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-146. Default Speed SD Card Switching Characteristics—3.3 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
SSD0	$1 / t_{c(clk)}$	Frequency, output sdcard_clk		24	MHz
SSD1	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	0.5 × P(1)		ns
SSD2	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		2083	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		3012	ps

Table 5-146. Default Speed SD Card Switching Characteristics—3.3 V(3) (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
	$t_{F(clk)}$	Fall time, output sdcard_clk		3012	ps
SSD3	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_cmd transition	–11.1	11.1	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		3012	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		3012	ps
SSD4	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition	–11.1	11.1	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		3012	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		3012	ps

(1) P = output sdcard_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

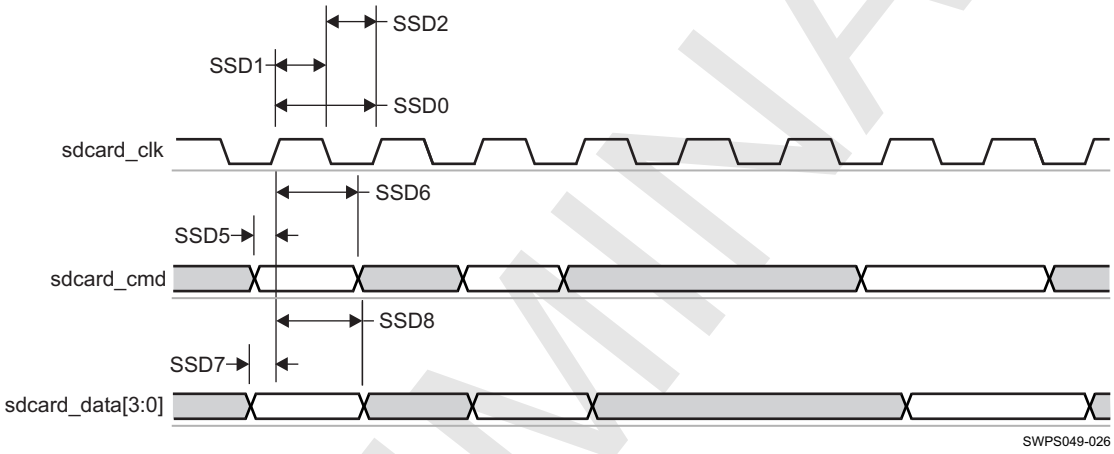


Figure 5-93. Default Speed SD Card, 3.3 V—Receiver Mode

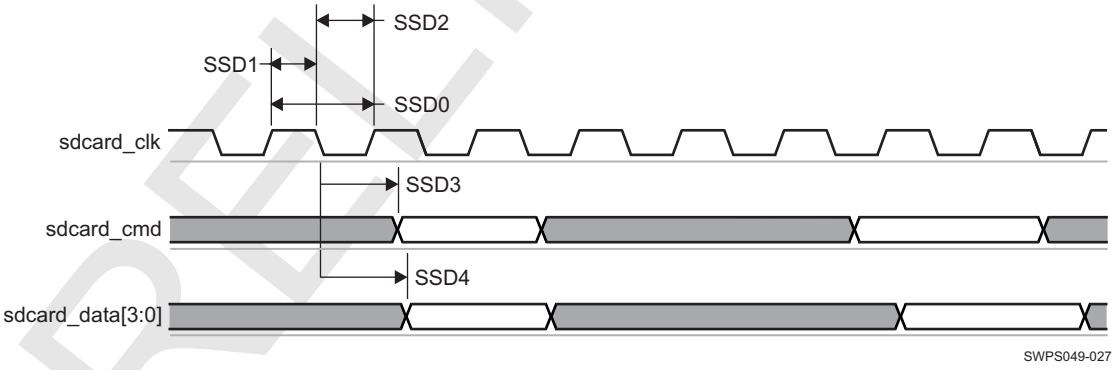


Figure 5-94. Default Speed SD Card, 3.3 V—Transmitter Mode

5.7.1.2 SD Card, High Speed (HS), SDR, 48 MHz, Half-Cycle Mode, 3.3 V

Table 5-147. High-Speed SD Card Timing Conditions—3.3 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	1345	5283	ps
t_F	Input fall time	1345	5283	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-148 and Table 5-149 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-148. High Speed SD Card Timing Requirements—3.3 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSD333	$t_{su(dV-clkH)}$	Setup time, sdcard_cmd valid before sdcard_clk rising edge	4.6		ns
HSSD334	$t_{h(clkH-dV)}$	Hold time, sdcard_cmd valid after sdcard_clk rising edge	2.1		ns
HSSD337	$t_{su(dV-clkH)}$	Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge	4.6		ns
HSSD338	$t_{h(clkH-dV)}$	Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge	2.1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-149. High Speed SD Card Switching Characteristics—3.3 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSD331	$1 / t_{c(clk)}$	Frequency, output sdcard_clk		48	MHz
HSSD332	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	0.5 × P(1)		ns
HSSD332	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		3012	ps
	$t_{F(clk)}$	Fall time, output sdcard_clk		3012	ps
HSSD335	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_cmd transition	–5.7	1.3	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		3012	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		3012	ps
HSSD336	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition	–5.7	1.3	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		3012	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		3012	ps

(1) P = output sdcard_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

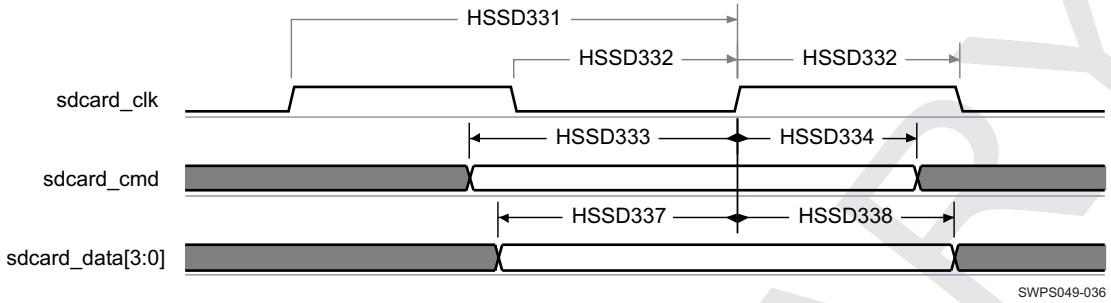


Figure 5-95. High Speed SD Card, 3.3 V—Receiver Mode

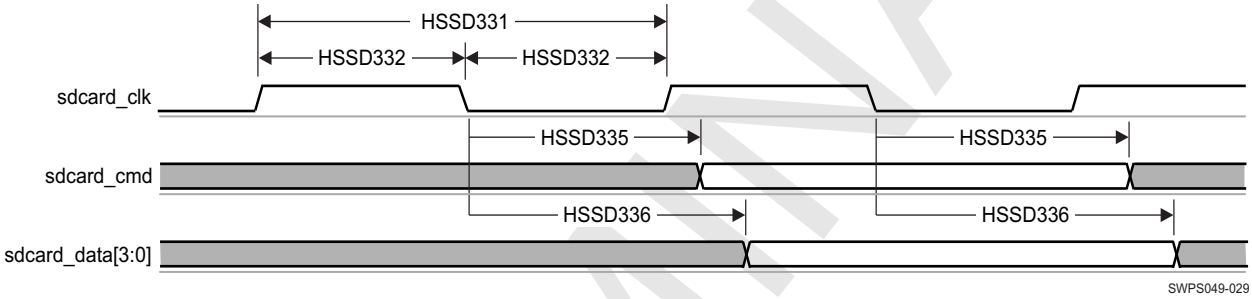


Figure 5-96. High Speed SD Card, 3.3 V—Transmitter Mode

5.7.1.3 SD Card, SDR12, 24 MHz, Half-Cycle Mode, 1.8 V

Table 5-150. SDR12 SD Card Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	1091	4284	ps
t_F	Input fall time	1091	4284	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-151 and Table 5-152 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-151. SDR12 SD Card Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR125	$t_{su(dV-clkH)}$	Setup time, sdcard_cmd valid before sdcard_clk rising edge	2.2		ns
HSSDR126	$t_{h(clkH-dV)}$	Hold time, sdcard_cmd valid after sdcard_clk rising edge	19.1		ns
HSSDR127	$t_{su(dV-clkH)}$	Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge	2.2		ns
HSSDR128	$t_{h(clkH-dV)}$	Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge	19.1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-152. SDR12 SD Card Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR120	$1 / t_{c(clk)}$	Frequency, output sdcard_clk		24	MHz
HSSDR121	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	0.5 × P(1)		ns
HSSDR122	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		2083	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		2750	ps
	$t_{F(clk)}$	Fall time, output sdcard_clk		2750	ps
HSSDR123	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_cmd transition	–14.1	10.1	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		2750	ps
HSSDR124	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition	–14.1	10.1	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		2750	ps

(1) P = output sdcard_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

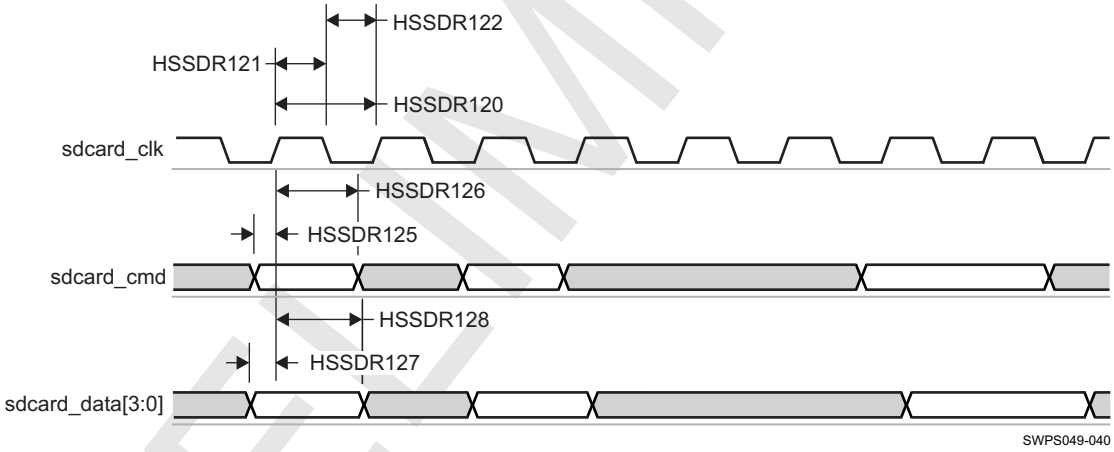


Figure 5-97. SDR12 SD Card, 1.8-V—Receiver Mode

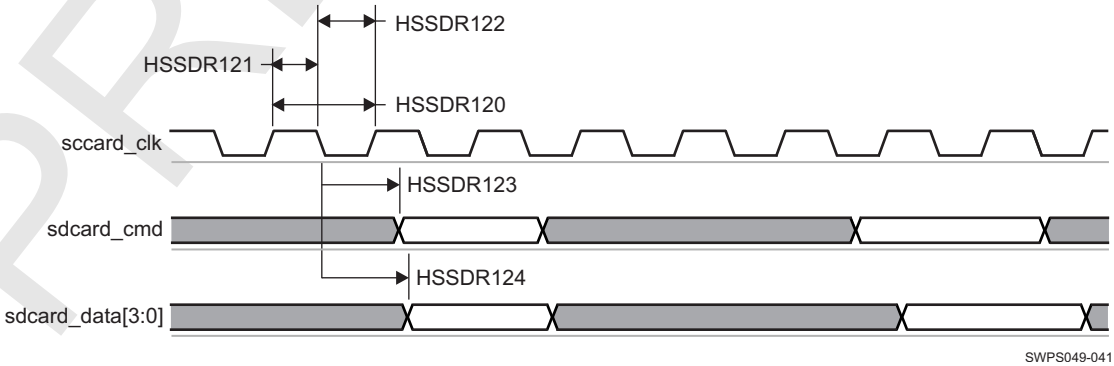


Figure 5-98. SDR12 SD Card, 1.8-V—Transmitter Mode

5.7.1.4 SD Card, SDR25, 48 MHz, Half-Cycle Mode, 1.8 V

Table 5-153. SDR25 SD Card Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	1091	4284	ps
t_F	Input fall time	1091	4284	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-154 and Table 5-155 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-154. SDR25 SD Card Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR253	$t_{su(dV-clkH)}$	Setup time, sdcard_cmd valid before sdcard_clk rising edge	4.6		ns
HSSDR254	$t_{h(clkH-dV)}$	Hold time, sdcard_cmd valid after sdcard_clk rising edge	2.1		ns
HSSDR257	$t_{su(dV-clkH)}$	Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge	4.6		ns
HSSDR258	$t_{h(clkH-dV)}$	Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge	2.1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-155. SDR25 SD Card Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR251	$1 / t_{c(clk)}$	Frequency, output sdcard_clk		48	MHz
HSSDR252	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	$0.5 \times P$(1)		ns
HSSDR252	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	$0.5 \times P$(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		1042	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		2750	ps
	$t_{F(clk)}$	Fall time, output sdcard_clk		2750	ps
HSSDR255	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_cmd transition	–6.1	2	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		2750	ps
HSSDR256	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition	–6.1	2	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		2750	ps

(1) P = output sdcard_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

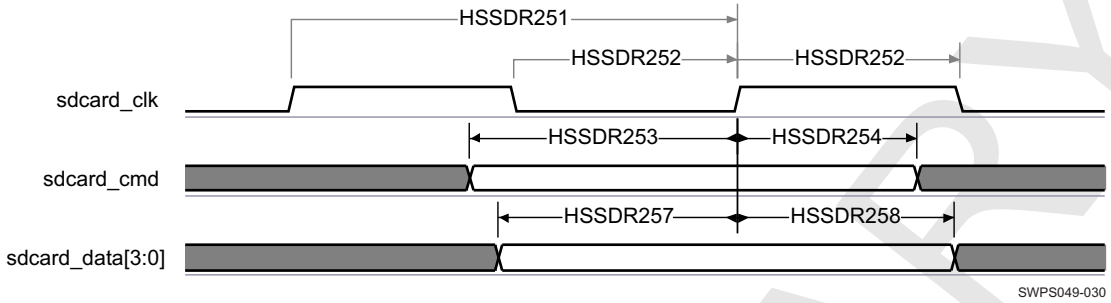


Figure 5-99. SDR25 SD Card, 1.8 V—Receiver Mode

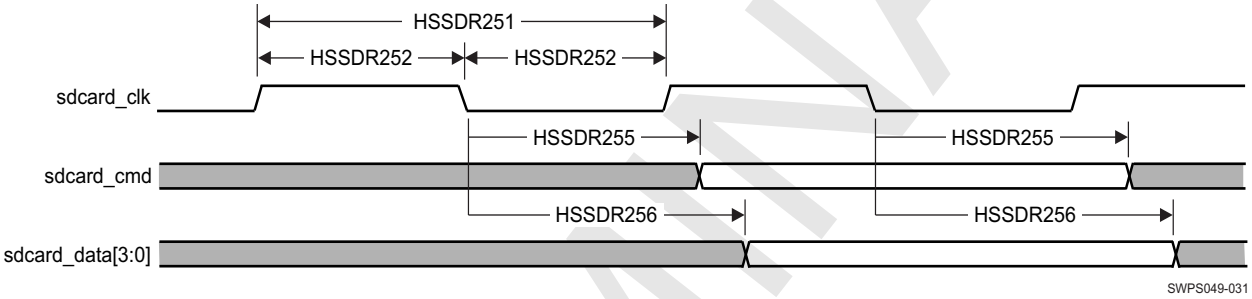


Figure 5-100. SDR25 SD Card, 1.8 V—Transmitter Mode

5.7.1.5 SD Card, UHS-I SDR50, 96 MHz, Half-Cycle Mode, 1.8 V

Table 5-156. UHS-I SDR50 SD Card Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	620	3854	ps
t_F	Input fall time	607	3091	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-157 and Table 5-158 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-157. UHS-I SDR50 SD Card Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR503	$t_{su(dV-clkH)}$	Setup time, sdcard_cmd valid before sdcard_clk rising edge	0.9		ns
HSSDR504	$t_{h(clkH-dV)}$	Hold time, sdcard_cmd valid after sdcard_clk rising edge	1.3		ns
HSSDR507	$t_{su(dV-clkH)}$	Setup time, sdcard_data[3:0] valid before sdcard_clk rising edge	0.9		ns
HSSDR508	$t_{h(clkH-dV)}$	Hold time, sdcard_data[3:0] valid after sdcard_clk rising edge	1.3		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-158. UHS-I SDR50 SD Card Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR501	$1 / t_{c(clk)}$	Frequency, output sdcard_clk		96	MHz
HSSDR502	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	0.5 × P(1)		ns
HSSDR502	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		521	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		2083	ps
	$t_{F(clk)}$	Fall time, output sdcard_clk		2083	ps
HSSDR505	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_cmd transition	–2.9	0.6	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		2083	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		2083	ps
HSSDR506	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition	–2.9	0.6	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		2083	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		2083	ps

(1) P = output sdcard_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

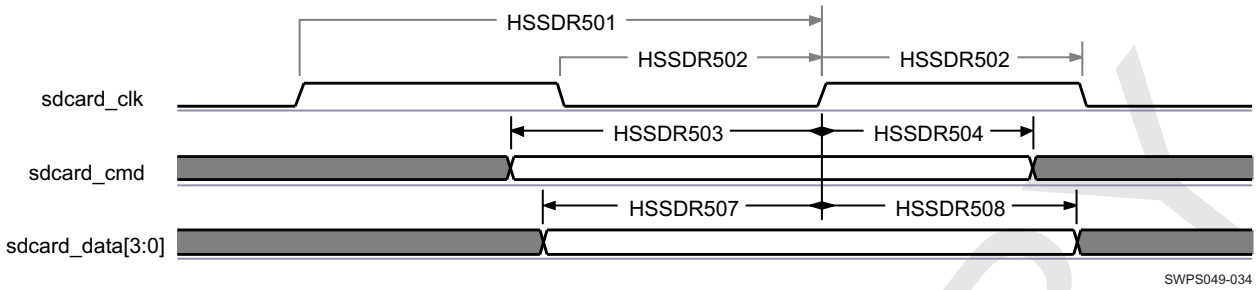


Figure 5-101. UHS-I SDR50 SD Card, 1.8 V—Receiver Mode

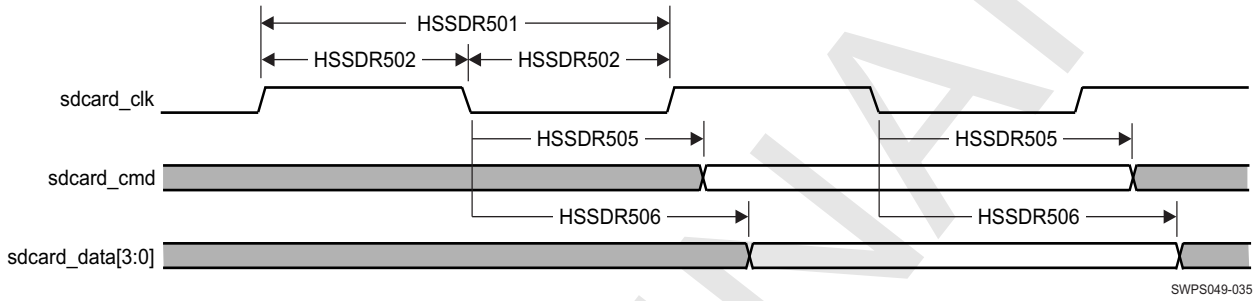


Figure 5-102. UHS-I SDR50 SD Card, 1.8 V—Transmitter Mode

5.7.1.6 SD Card, UHS-I SDR104, 192 MHz, Half-Cycle Mode, 1.8 V

Table 5-159. UHS-I SDR104 SD Card Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	1091	4284	ps
t_F	Input fall time	1091	4284	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-160 assumes testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-160. UHS-I SDR104 SD Card Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR1041	1 / $t_{c(clk)}$	Frequency, output sdcard_clk		192	MHz
HSSDR1042	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	0.5 × P(1)		ns
HSSDR1042	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		260	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		2750	ps
	$t_{F(clk)}$	Fall time, output sdcard_clk		2750	ps
HSSDR1045	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_cmd transition	–0.6	–0.1	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		2750	ps

Table 5-160. UHS-I SDR104 SD Card Switching Characteristics—1.8 V(3) (continued)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSSDR1046	$t_{d(clkL-doV)}$	Delay time, sdcard_clk falling edge to sdcard_data[3:0] transition	–0.6	–0.1	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		2750	ps

(1) P = output sdcard_clk period in ns.

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

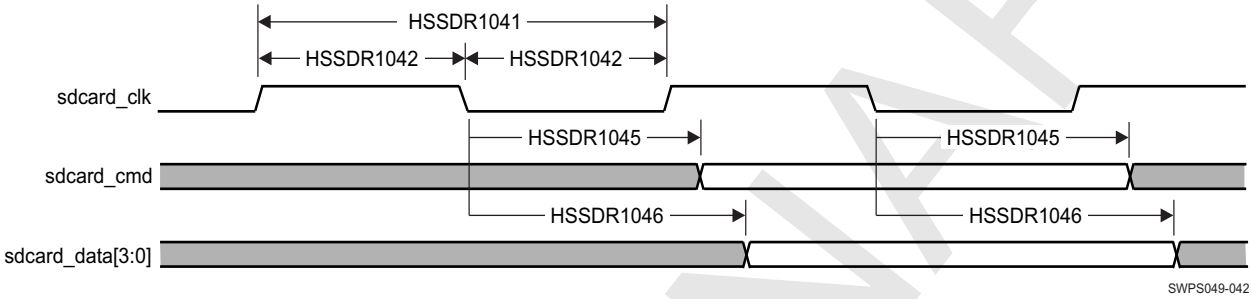


Figure 5-103. UHS-I SDR104 SD Card, 1.8 V—Transmitter Mode

5.7.1.7 SD Card, UHS-I DDR50, 48 MHz, Half-Cycle Mode, 1.8 V

Table 5-161. UHS-I DDR50 SD Card Timing Conditions—1.8 V

SYSTEM CONDITION PARAMETER		VALUE		UNIT
		MIN	MAX	
Input Conditions				
t_R	Input rise time	607	3854	ps
t_F	Input fall time	607	3854	ps
Output Condition(1)				

(1) See Table 8-6, *SD Card PCB Requirements and IO Programming*.

Table 5-162 and Table 5-163 assume testing over the recommended operating conditions and electrical characteristic conditions.

Table 5-162. UHS-I DDR50 SD Card Timing Requirements—1.8 V(1)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSDDR505	$t_{su(dV-clkH)}$	Setup time, sdcard_cmd valid before sdcard_clk rising edge	5		ns
HSDDR506	$t_{h(clkH-dV)}$	Hold time, sdcard_cmd valid after sdcard_clk rising edge	1		ns
HSDDR507	$t_{su(dV-clkH)}$	Setup time, sdcard_data[3:0] valid before sdcard_clk rising or falling edge	0.9		ns
HSDDR508	$t_{h(clkH-dV)}$	Hold time, sdcard_data[3:0] valid after sdcard_clk rising or falling edge	1		ns

(1) See DM Operating Condition Addendum for CORE OPP voltages.

Table 5-163. UHS-I DDR50 SD Card Switching Characteristics—1.8 V(3)

NO.	PARAMETER		OPP_NOM		UNIT
			MIN	MAX	
HSDDR500	$1 / t_{c(clk)}$	Frequency, output sdcard_clk		48	MHz
HSDDR501	$t_{w(clkH)}$	Typical pulse duration, output sdcard_clk high	0.5 × P(1)		ns
HSDDR502	$t_{w(clkL)}$	Typical pulse duration, output sdcard_clk low	0.5 × P(1)		ns
	$t_{dc(clk)}$	Duty cycle error, output sdcard_clk		521	ps
	$t_{j(clk)}$	Jitter standard deviation(2), output sdcard_clk		65	ps
	$t_{R(clk)}$	Rise time, output sdcard_clk		2750	ps
	$t_{F(clk)}$	Fall time, output sdcard_clk		2750	ps
HSDDR503	$t_{d(clkL-doV)}$	Delay time, sdcard_clk rising edge to sdcard_cmd transition	1.1	14.1	ns
	$t_{R(do)}$	Rise time, output sdcard_cmd		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_cmd		2750	ps
HSDDR504	$t_{d(clkL-doV)}$	Delay time, sdcard_clk rising or falling edge to sdcard_data[3:0] transition	1.1	6.3	ns
	$t_{R(do)}$	Rise time, output sdcard_data[3:0]		2750	ps
	$t_{F(do)}$	Fall time, output sdcard_data[3:0]		2750	ps

(1) P = output sdcard_clk period in ns

(2) The jitter probability density can be approximated by a Gaussian function.

(3) See DM Operating Condition Addendum for CORE OPP voltages.

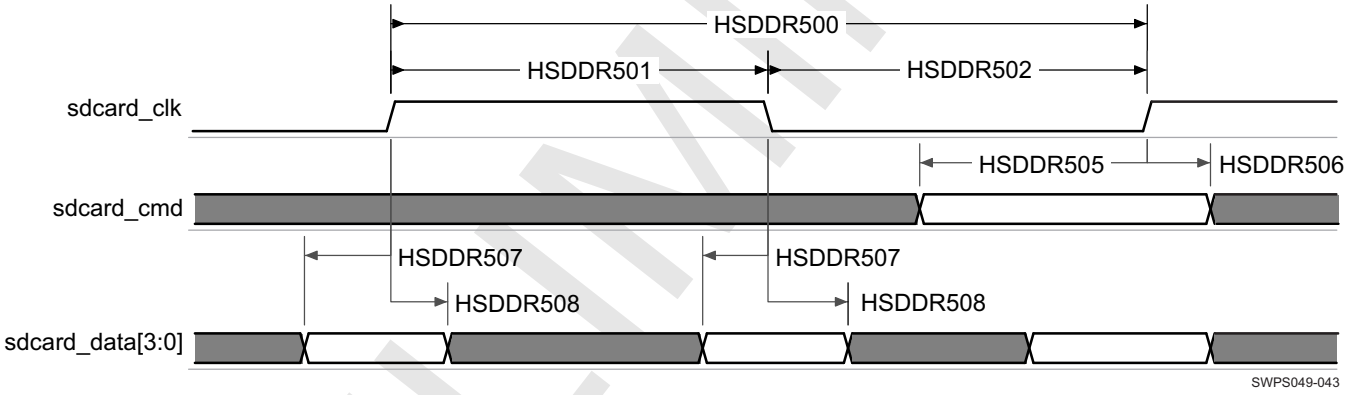


Figure 5-104. UHS-I SDCard DDR, 1.8 V—Receiver Mode

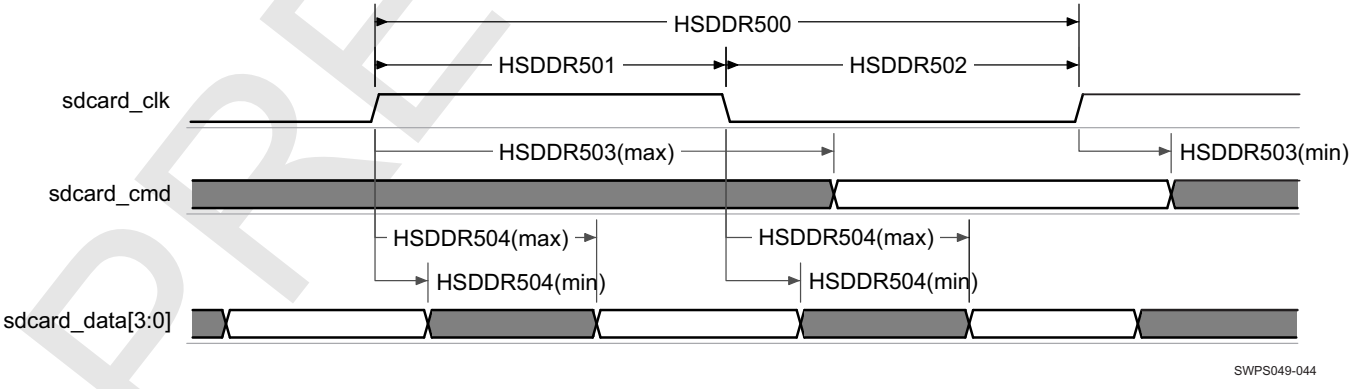


Figure 5-105. UHS-I SDCard DDR, 1.8 V—Transmitter Mode

5.8 Debug and Trace Interface, 1.8 V

NOTE

To be supplied

6 Thermal Management

For reliability and operability concerns, the maximum junction temperature of the OMAP5430 device has to be at or below the T_J value identified in Table 3-3, *Recommended Operating Conditions*.

Depending on the thermal mechanical design and worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level with the power worst use case.

Based on the results, if the temperature limits are exceeded, an OMAP5430 level software thermal policy must be set up; for detailed information, see the *OMAP5430 Thermal Management* application note.

The OMAP5430 level thermal policy relies on a PCB sensor. Therefore, it is recommended to have such sensors located on the PCB; for more information, see Section 6.2.1, *PCB Temperature Sensor*. In addition, it is recommended to avoid having another significant thermal source near the OMAP5430 device.

The risks of not managing this junction temperature are hazardous heating, power supply clamping, reliability issues, and malfunction.

6.1 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1. Thermal Resistance Characteristics

PACKAGE	POWER (W)	Θ_{JA} (°C/W)(2)	Ψ_{JB} (°C/W)(3)	T_J (°C)(4)	BOARD TYPE
OMAP5430 ES2.0	2.6	20.9	9.3	109	2S2P(1)

(1) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

(2) Θ_{JA} (Theta-JA) = Thermal Resistance Junction-to-Ambient, °C/W.

(3) Ψ_{JB} (Psi-JB) = Pseudo Resistance Junction-to-Board, °C/W derived from thermal simulation following JEDEC reference (JEDEC standard JESD51-9, *Test Board for Array Surface Mount Package Thermal Measurements*). The board temperature is measured at 1 mm from the package edge.

(4) $T_J = P \times \Psi_{JB} + T_B$. T_J is the junction temperature and T_B is the board temperature (85°C).

CAUTION

The Ψ_{JB} (Psi-JB) could vary, depending on the board (PCB) and the device power distribution related to the power use case: 9.3ºC/W is given for a 2.6-W dissipated power.

6.2 Temperature Sensor Recommendation

6.2.1 PCB Temperature Sensor

To manage the OMAP5430 junction temperature, an external PCB temperature sensor is required in addition to the internal OMAP5430 thermal sensor.

The accuracy of the temperature sensor is critical to optimize the OMAP performance; the minimum recommended accuracy is ±2ºC; see the TI TMP102 temperature sensor component. The temperature sensor can be located at one position to correctly monitor the OMAP5430 junction temperature:

- OMAP north side, 1 mm from package on same PCB side than OMAP

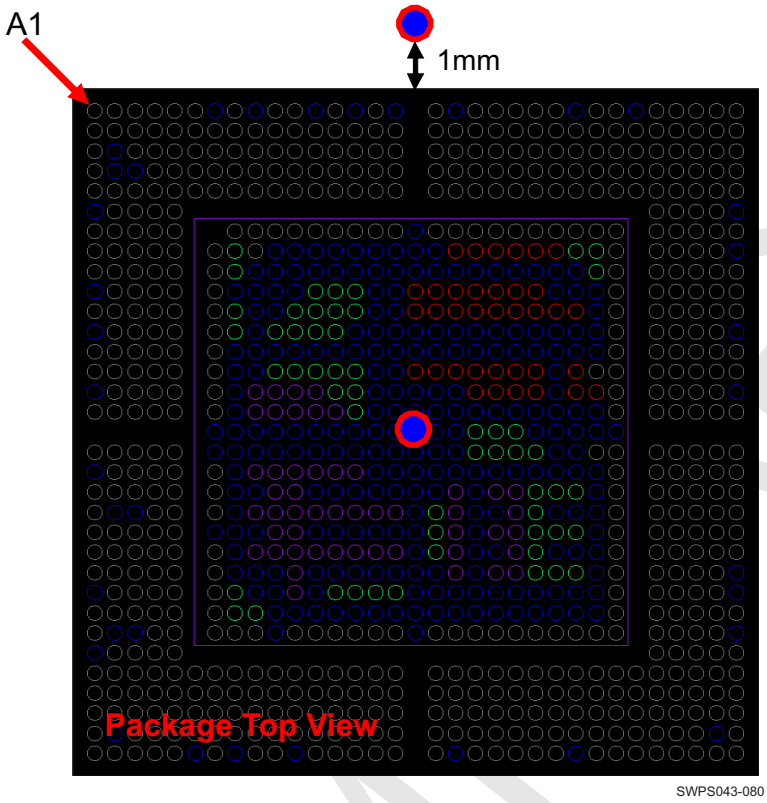


Figure 6-1. PCB Temperature Sensor Recommendation (Package Top View)

6.2.2 Junction Temperature Sensor

The OMAP5430 device supplies a temperature sensor feature which is in the band gap voltage and temperature sensor (VBGAPTS) module. An analog-to-digital converter (ADC) converts the silicon temperature into a 10-bit output decimal value.

NOTE

For more information, see Control Module / Control Module Functional Description / Band Gap Voltage and Temperature Sensor / Temperature Sensor section of the OMAP543x TRM.

Table 6-2 gives the temperature sensor characteristics.

Table 6-2. Temperature Sensor Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
ADC resolution (DTEMP[9:0])		10		Bit
ADC temperature step	0.4	0.5	0.6	°C
ADC temperature accuracy			±2(1)	°C
ADC conversion time			50	µs

(1) The maximum accuracy ±2°C means the worst case of the ADC accuracy.

7 Package Characteristics

7.1 Device Nomenclature

7.1.1 Standard Package Symbolization

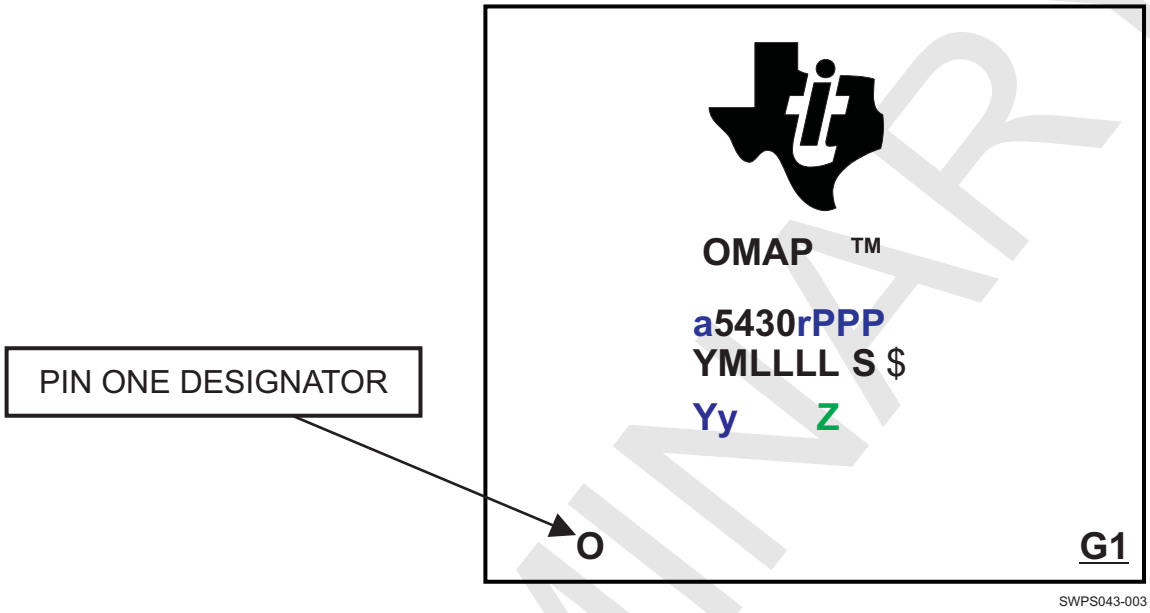


Figure 7-1. Printed Device Reference

NOTE

Black: Static field

Blue: Variable field coded with letters and/or numbers

Green: Variable fields coded with numbers

The letters and numbers fields are interleaved to facilitate the reading of the parameters.

During the prototyping phase, a generic symbolization can be applied for flexibility reasons (see Figure 7-2). TI will ensure the right fuse content and test program usage by part number.

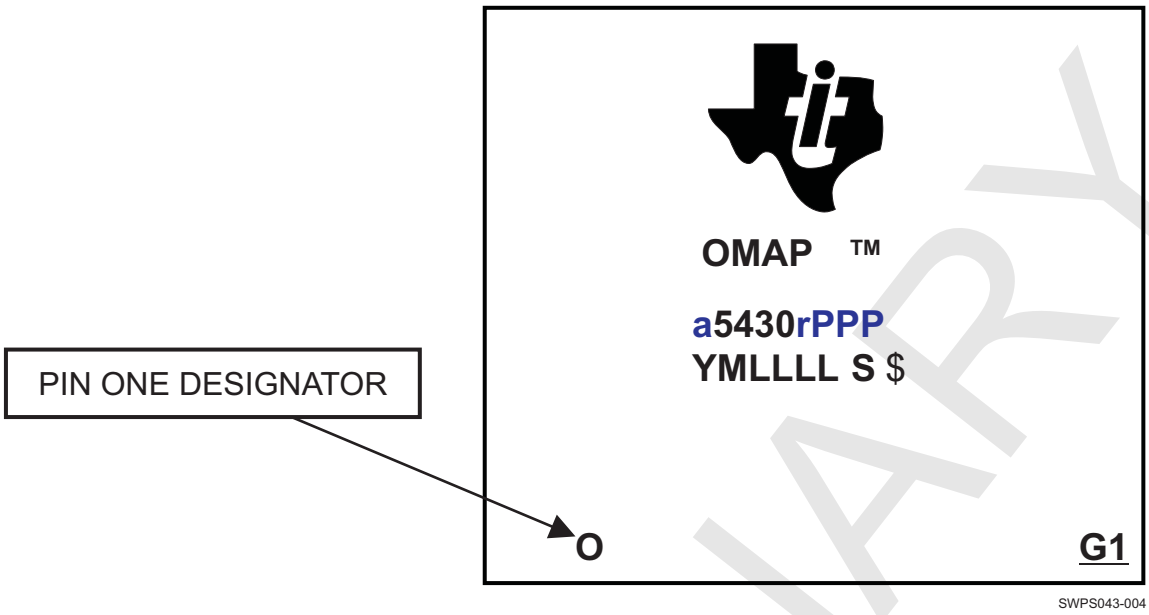


Figure 7-2. Prototype Device Reference

NOTE

Black: Static field

Blue: Variable field coded with letters and/or numbers

The letters and numbers fields are interleaved to facilitate the parameters reading.

7.1.2 SAP Part Number

The actual part number used in the system follows this syntax (SAP allows a maximum of 14 characters):

- SAP part number in Tray: a**5430**rFZYyPPP
- SAP part number in Tape and Reel: a**5430**rFZYyPPP**R**

7.1.3 Device Naming Convention

Table 7-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage(1)	X	X for TMX (prototypes)
		P	P for TMP (preproduction, production not yet qualified
		BLANK	blank for TMV (qualified production) blank when qualified
r	Device revision	BLANK	ES 1.0
		A	ES 2.0
PPP	Package designator	CBU	CBU S-PBGA-N980 (Prototype and Production)
F	Reserved	XX	Reserved
Yy	Device type	GP	General purpose (Prototype and Production)
		XX	Reserved
Z	Device Speed	BLANK or 0	OMAP5430 standard speed grade
		1, 2, …	OMAP5430 alternate speed grade
YM	Lot Trace Code (LTC): Y = Year, M = Month		
LLLL	Lot Trace Code (LTC): Assembly lot number		

Table 7-1. Nomenclature Description (continued)

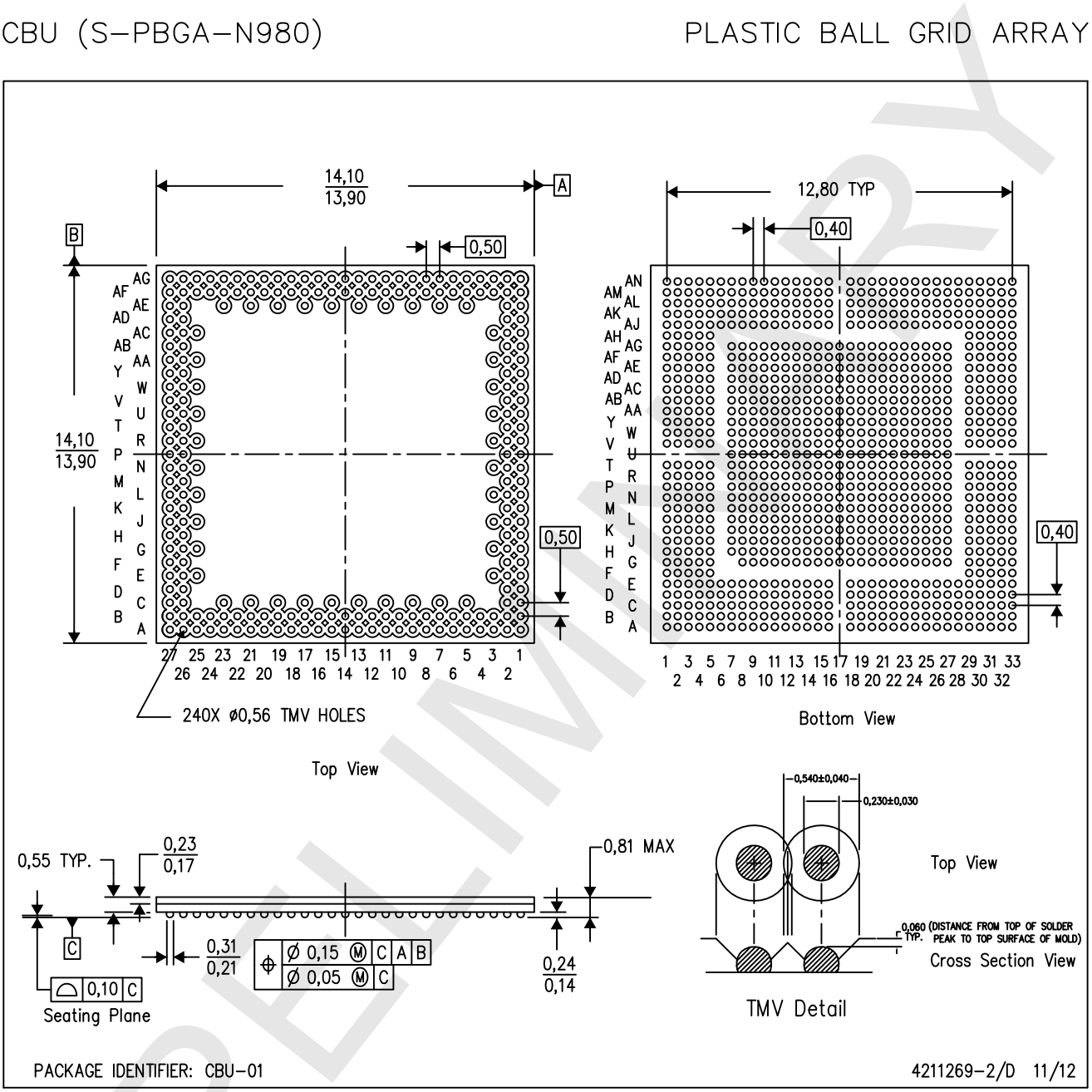
FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
S	Reserved		
$	Reserved		
O	Pin one designator		
G1	ECAT—Green package designator		

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.
Nonqualified / production devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

NOTE

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

7.2 Mechanical Data



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

Figure 7-3. Mechanical Package

8 PCB Guidelines

8.1 Introduction

NOTE

These PCB guidelines are in a draft maturity and, consequently, are subject to change depending on the verification steps during the IC development.

Any references to the OMAP5430 ballout or pin muxing are subject to change following the OMAP5430 ballout maturity.

This chapter provides:

- Guidelines for the design of the PCB focusing first on power delivery network (PDN) implementation which is essential to achieve the desired level of performance on the OMAP5430 device.
- General principles and step-by-step approach for good PDN implementation and specific requirements for the different power supplies of the OMAP5 device.
- Methodology and requirements to meet the PCB routing of the OMAP5430 differential interfaces (MIPI CSI-2 and DSI-1 D-PHY, MIPI HDMI PHY, USB PHY, and SATA PHY).
- PCB requirements for the general-purpose interface using a CMOS driver to meet timing requirements and minimize overshoot and undershoot at the far-end peripheral and minimize overshoot and undershoot at the far-end.
- The trace lengths given in this chapter are aligned with the FR-4 standard specification for PCB (e_r = 4.0). To provide a rough idea of the corresponding trace length: 67 ps per cm is considered.

8.2 Initial Requirements and Guidelines

8.2.1 Introduction

The recommendation for OMAP5430 board stackup is a 10-layer design with two options:

- Option 1: 3+4+3 with core via from layer 3 to layer 8
- Option 2: 3+4+3 with core via from layer 4 to layer 7 when routing is congested.

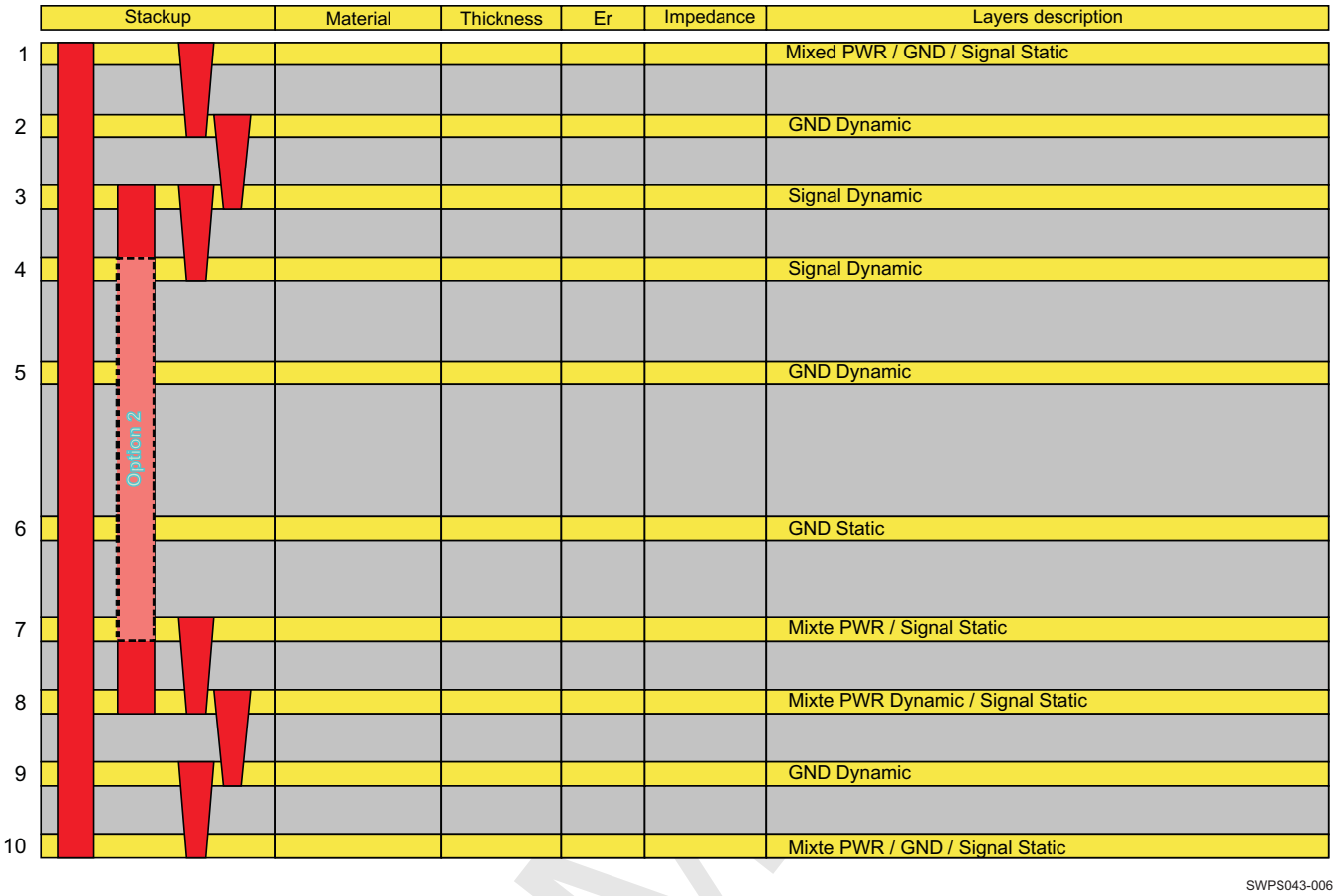


Figure 8-1. PCB Stackup

- The PDN must be optimized for low trace resistance and low trace inductance between the power management IC (PMIC) and OMAP5 device especially for vdd_mpu, vdd_mm, and vdd_core power supplies (ranked by order of criticality per their respective peak currents).
- Optimize routing power routing between vdd_mpu and the PMIC.
- It is highly recommended to run board frequency domain analysis on the vdd_mpu, vdd_mm, and vdd_core power supplies to check if proper board decoupling is implemented and confirm that the respective target impedances are met. For more information on target impedance, see Section 8.6, *External Capacitors*.
- Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 30 O and 65 O to minimize overshoot and undershoot on far-end loads. For more information see Section 8.4, *Single-Ended Interfaces*.
- Characteristic impedance for differential interfaces must be routed as differential traces on the same layer. The trace width and spacing must be chosen to yield the recommended differential impedance. For more information see Section 8.5, *Differential Interfaces*.
- An external interface using a connector must be protected following the IEC61000-4-2 level 4 system ESD.

- LPDDR2 memory for the OMAP5430 POP:
  - The OMAP5430 device supports two LPDDR2 channels. Each of these channels supports two chip selects. Two LPDDR2 memory dies per channel (two channels) can be connected on top of the OMAP5 package via Package-on-Package implementation.
  - The memory components LPDDR2-S4A and LPDDR2-S4B have different voltage requirements. The S4B type needs a single 1.2-V source to supply vdd2 and vddq / vddca.
  - For the OMAP5432 device, the DDR3 memory is used—bottom:
    - There are two DDR3 channels. Each of these channels supports two chip selects and then two ranks. This means the DDR3 package can support two dies.

NOTE

The cutout technique is recommended each time it is needed to locally lower unexpected high capacitance (a wide PCB footprint of a discrete component on the top or bottom layer in regards to GND or supply shape, for instance). This technique prevents impedance discontinuities by locally removing the ground reference below the line (ground cutout) so that the actual electrical reference for the signal line will be located further away (on the next ground layer or on the edges of the plane cutout).

Special attention must be paid while doing such cutouts to limit coupling of unwanted noise coming from PCB traces that are present under the cutouts.

8.3 PCB Power General Guidelines

In this section you will find the necessary steps for the PCB power general routing:

- Section 8.3.1, *Step 1: Requirements and Guidelines for PCB Stack-up*
- Section 8.3.2, *Step 2: Physical Layout Guidelines of the PDN*
- Section 8.3.3, *Step 3: Static IR Drop PDN Guidelines*, to minimize resistance, avoid neck-down, and reduce current density.

8.3.1 Step 1: Requirements and Guidelines for PCB Stack-up

The PCB stack-up (layer assignment) is an important factor in determining the optimal performance of the PDN. An optimized PCB stack-up for higher power integrity performance can be achieved by following these requirements:

- Power and ground plane pairs must be closely coupled together. The capacitance formed between the planes can decouple the power supply at high frequencies. Whenever possible, the power and ground planes must be solid to provide a continuous return path for the return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair. Minimizing the separation distance (the dielectric thickness) will maximize the capacitance.
- Keep the power and ground plane pair as close as possible to the top and bottom surfaces (see Figure 8-2). This will help to minimize the decoupling capacitors mounting, the via, and the power and ground plane pair spreading loop inductance.

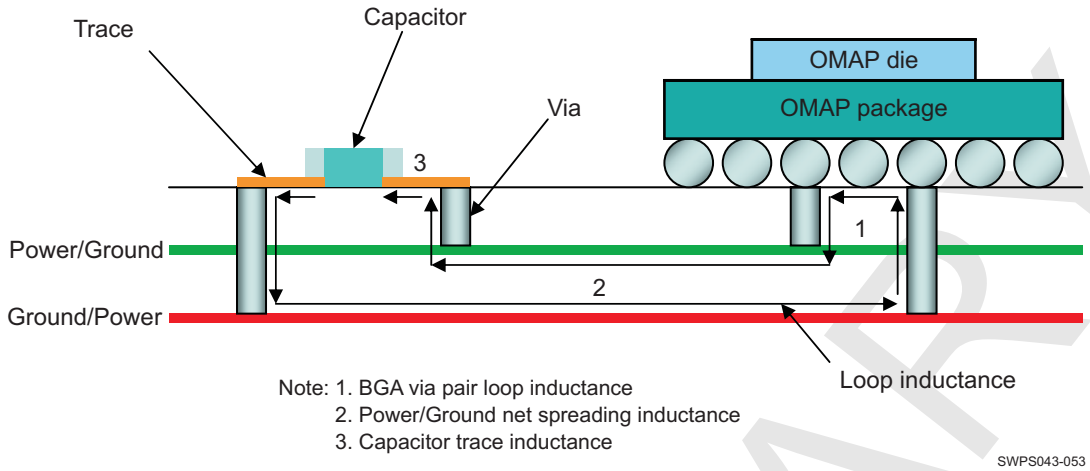


Figure 8-2. Minimize Loop Inductance With Proper Layer Assignment

The placement of power and ground planes in the PCB stackup (determined by layer assignment) has a significant impact on the parasitic inductances of the power current path as shown in Figure 8-2. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high priority supplies in the top half of the stackup and low-priority supplies in the bottom half of the stackup as shown in the examples below (vias have parasitic inductances which impact the bottom layers more, so it is advised to put the sensitive and high priority power supplies on the top layers).

Figure 8-3 and Figure 8-4 show examples of typical PCB stack-up designed with power integrity in mind.

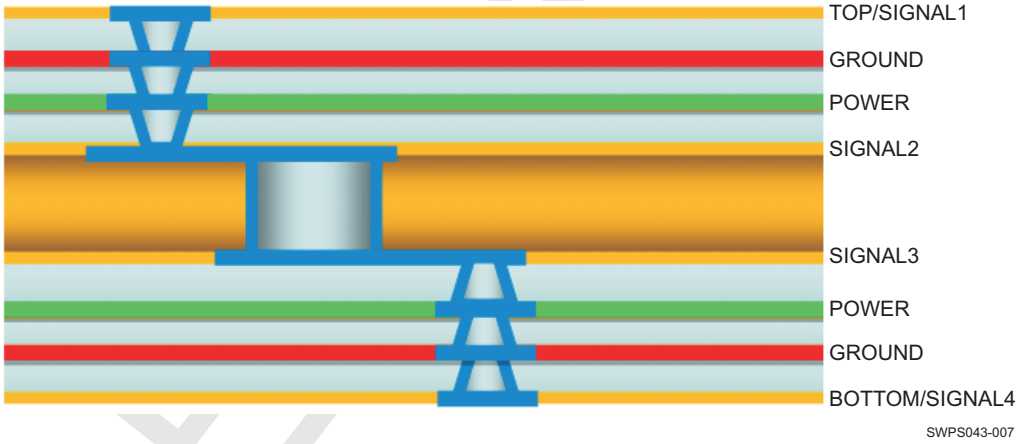


Figure 8-3. Layer PCB With High Density Interconnect (HDI) Vias

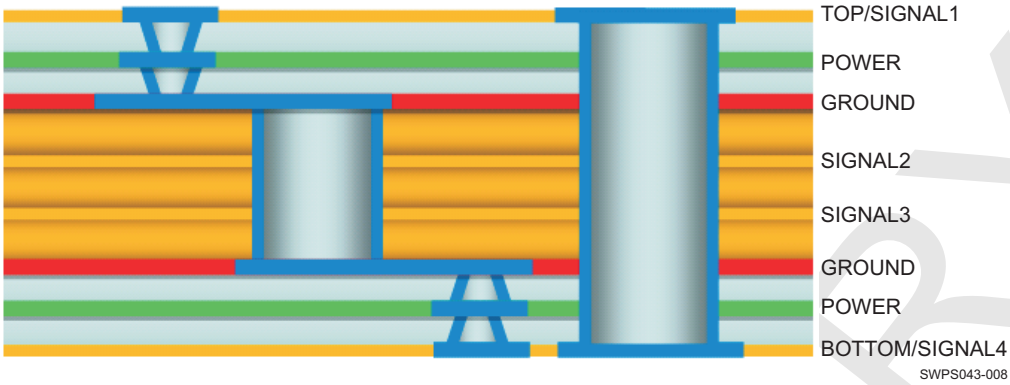


Figure 8-4. Layer PCB With Plated Though Holes (PTH) Vias

8.3.2 Step 2: Physical Layout Guidelines of the PDN

A critical step in designing an optimized PDN is that proper care must be taken to ensure that the initial layout is accomplished with good power integrity design guidelines in mind. The following points are important requirements that will need to be implemented in the PCB PDN design:

- External trace routing between components must be as wide as possible. The wider the trace, the lower the dc resistance and consequently the lower the static IR drop.
- Whenever possible, try aiming for a ratio of 1:1 or better for component (for example, capacitors and resistors) pins and vias. Do not share vias among multiple capacitors.
- Placement of the vias must be as close as possible to the solder pad.

Figure 8-5 shows an example of acceptable width for power net routing but with poor via placement.

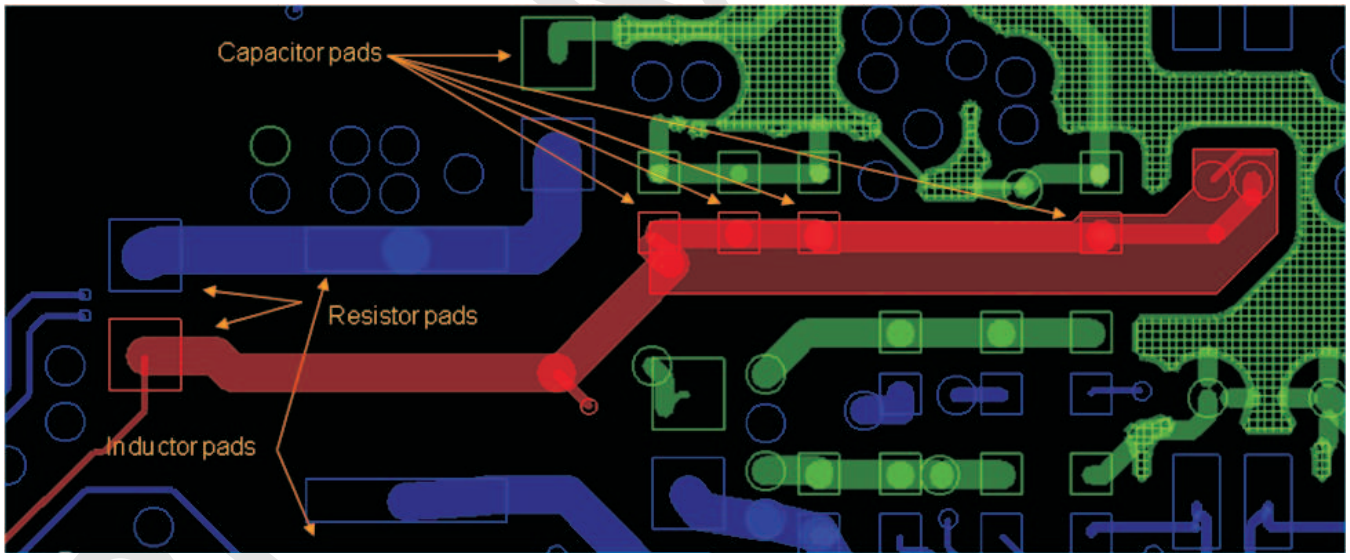


Figure 8-5. Poor Via Assignment for PDN

Figure 8-6 shows an improved power net routing with appropriate via assignment and placement, respectively.

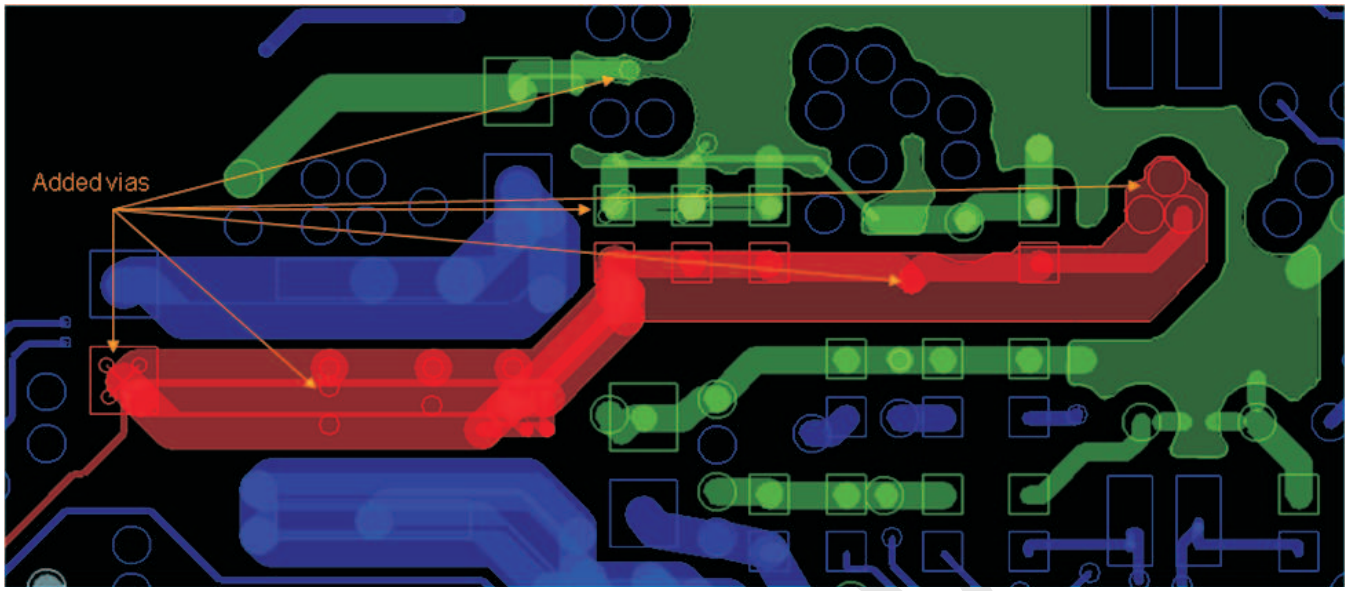


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Figure 8-6. Improved Via Assignment for PDN

To avoid any ampacity issue (this means the maximum current carrying capacity of each transitional via) an evaluation must be performed to determine the appropriate number of vias required to connect components.

Figure 8-7 and Figure 8-8 show examples of via starvation on a power net transitioning from the top routing layer to the internal layers and the improved layout, respectively.

SWPS043-056

One via for five capacitor pads is not good practice.

Figure 8-7. Via Starvation

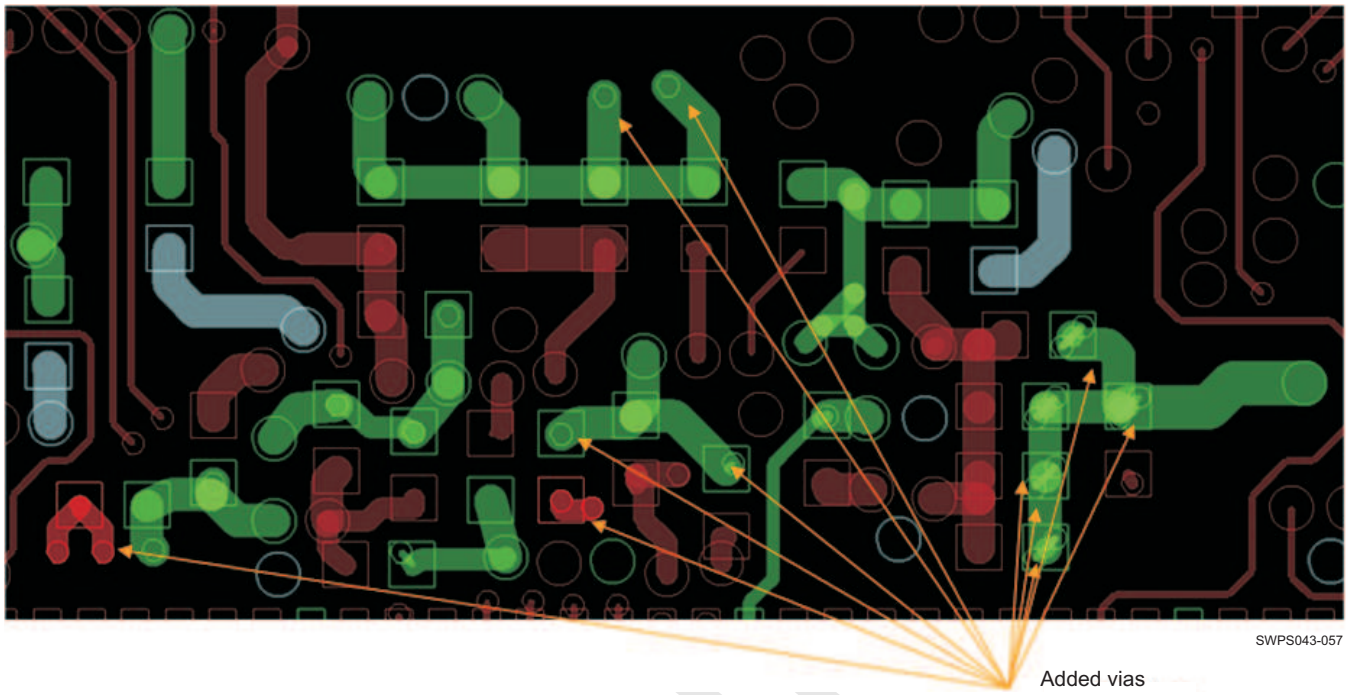

Figure 8-8. Improved Layout With More Transitional Vias

- It is also a good practice to perform a static IR drop. This analysis can assess the appropriate number of vias and geometrical trace width dimensions required for the expected IR drop requirement.
- Whenever possible for the internal layers (routing and plane), wide traces and copper area fills are preferred for PDN layout. The routing power nets in plane provide for more interplane capacitance and improve high frequency performance of the PDN.
- Try to avoid different power nets (for example, VDD_MPU with VDD_CORE) coupling on the PCB by using coplanar shielding whenever appropriate.

Figure 8-9 represents an example of coplanar shielding for power nets.

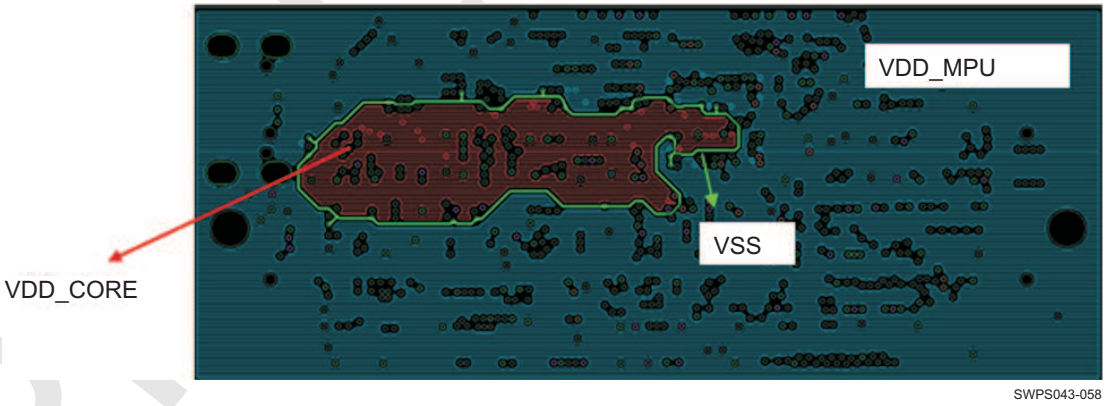

Figure 8-9. Coplanar Shielding of Power Net Using Ground Guard-band

- Decoupling capacitors must be mounted with minimum impact to inductance. A real capacitor has characteristics not only of capacitance but also inductance and resistance.

  Figure 8-10 shows the parasitic model of a real capacitor. A real capacitor must be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

ADVANCE INFORMATION

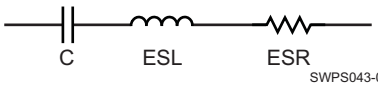

Figure 8-10. Characteristics of a Real Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given as:

$$|Z| = \sqrt{ESR^2 + \left(\omega ESL - \frac{1}{\omega C}\right)^2}$$

$$\text{where :} \quad \omega = 2\pi f$$

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Figure 8-11. Series Model Impedance Equation

Figure 8-12 shows the resonant frequency response of a typical capacitor with self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance, reactive capacitance, and inductance as shown in Figure 8-11.

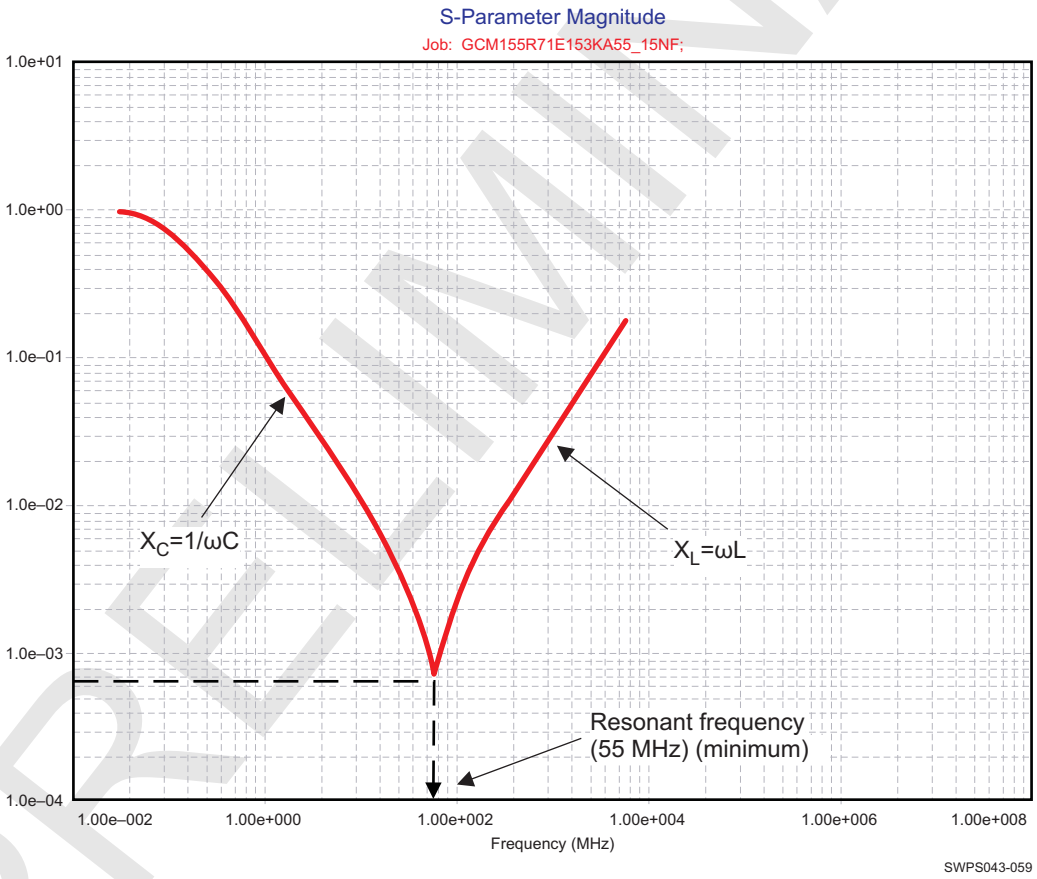

Figure 8-12. Typical Impedance Profile of a Capacitor

Since a capacitor has series inductance and resistance that will impact its effectiveness, it is important that the following recommendations are adopted in placing them on the PDN.

Whenever possible, please mount the capacitor with the geometry that will minimize the mounting inductance and resistance. This was shown earlier in Figure 8-2. The capacitor mounting inductance and resistance here includes the inductance and resistance of the pads, trace, and vias.

The length of a trace used to connect a capacitor has a big impact on parasitic inductance and resistance of the mounting. This trace must be as short and wide as possible. Wherever possible, minimize the trace by locating vias near the solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or doubling the number of vias as shown in Figure 8-13. If the PCB manufacturing processes allow and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up (as shown in Figure 8-4).

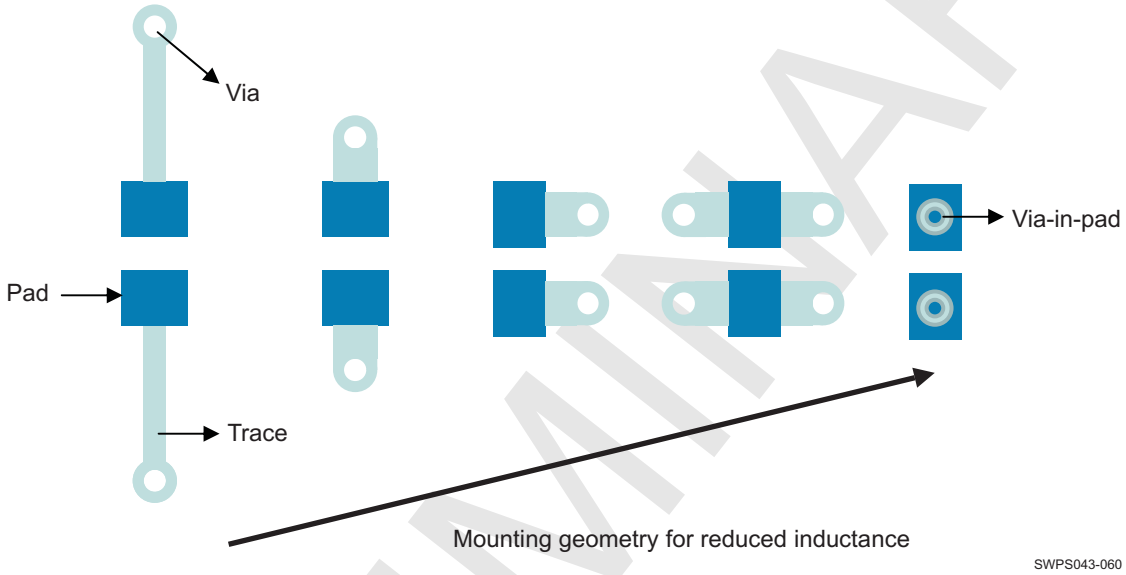

Figure 8-13. Capacitor Placement Geometry for Improved Mounting Inductance

8.3.3 Step 3: Static IR Drop PDN Guidelines

Delivering reliable power to circuits is always of critical importance because IR drops can happen at every level in a chip, package, and board system. Components that are distant from their associated power source are particularly susceptible to an IR drop. The designs that rely on battery power must minimize the voltage drop to avoid unacceptable power loss. Early dc assessments help determine power distribution basics such as the best available entry point for power, layer stackup choices, and estimates for the amount of copper needed to carry the current.

The resistance, Rs, of a plane conductor for a unit length and unit width is called the surface resistivity (ohms per square).

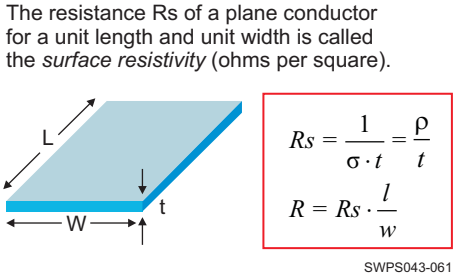

Figure 8-14. Depiction of Sheet Resistivity and Resistance

Ohm's Law (V = I × R) relates conduction current to voltage drop and at dc the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor.

System-level IR drop budget is made up of three portions: on-chip, package, and PCB board. Static IR or dc analysis and design methodology consists of designing the PDN such that the voltage drop (under dc operating conditions) across power and ground pads of the transistors of the application processor device is within a specified value of the nominal voltage for proper functioning of the device.

Figure 8-15 shows the PCB-level static IR drop budget is defined between the pins of the power management device PMIC or VRM and the BGA pads on the PCB to the application processor device to which the PMIC is supplying power.

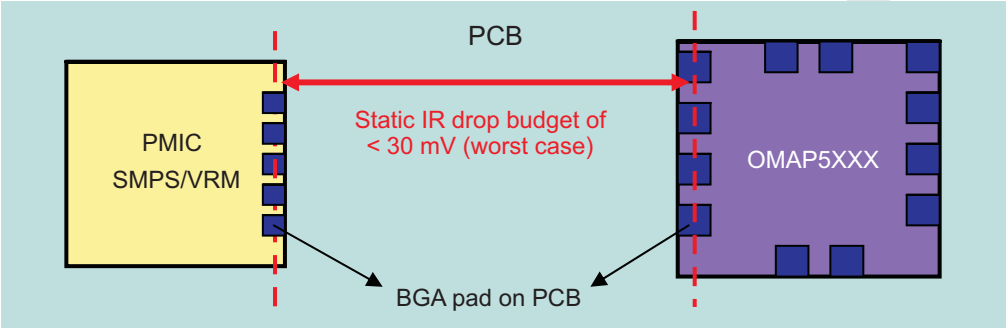

Figure 8-15. Static IR Drop Budget for PCB Only

The total system-level margin allowed for proper device function is given, the allowable voltage variation at the BGA of the device is specified at 1.5% of the nominal voltage. For a 1.35-V supply, this must be = 20 mV. It is highly recommended to connect the VRM or the PMIC as close as physically possible on the PCB to the OMAP5430 device.

To accurately analyze the PCB static IR drop, the actual geometry of the PDN must often be properly modeled and simulated to accurately characterize long distribution paths, low weight copper, electro-migration violations of current-carrying vias, and swiss-cheese effects. It is recommended to perform the following analyses:

- Lumped resistance and IR drop analysis
- Distributed resistance and IR drop analysis

The requirements are present to perform both analyses and to show compliance. In the following sections each methodology is described in detail and examples provided of analysis flow that can be used by the PCB designer to validate compliance to the requirements on their PCB PDN design.

8.3.4 Lumped and Distributed Resistance and IR Drop Analysis Methodology

Lumped methodology consists of grouping all of the power and ground pins of the PMIC and the processor device. This is followed by extracting the lumped resistance or dc voltage drop of the equivalent path by applying a voltage source at the PMIC end and a current sink at the device end. Figure 8-16 describes the pin-grouping concept.

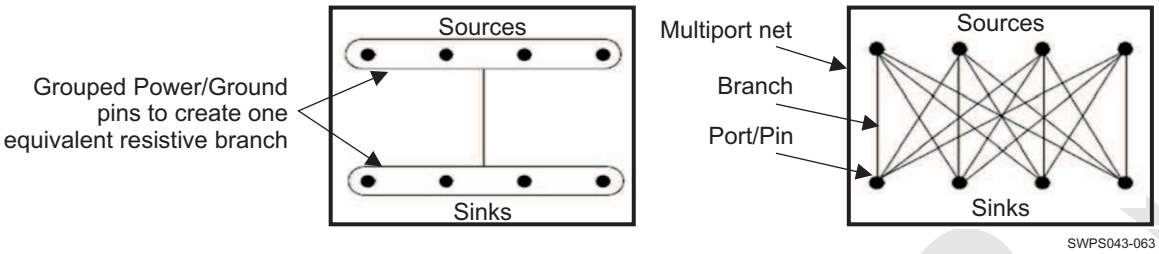

Figure 8-16. Pin-grouping Concept: Lumped and Distributed Methodologies

The lumped methodology consists of importing the PCB layout database (from the Cadence Allegro tool or any other layout design tool) into the static IR drop modeling and simulation tool of preference for the PCB designer. This is followed by applying the correct PCB stack-up information (thickness and material properties) of the PCB dielectric and metallization layers. The material properties of the dielectric consist of permittivity (Dk) and loss tangent (Df).

For the conductor layers, the correct conductivity needs to be programmed into the simulation tool. This is followed by pin-grouping of the power and ground nets, and applying appropriate voltage and current sources. The current and voltage information can be obtained from the power and voltage specifications of the device under different operating conditions and use-modes. After running the simulation, the lumped resistance and lumped IR drop can be examined as shown in Figure 8-16.

8.3.5 System ESD Generic Guidelines

8.3.5.1 System ESD Generic PCB Guidelines

- Protection devices must be placed close to the ESD source which means close to the connector. This allows the device to subtract the energy associated with an ESD strike before it reaches the internal circuitry of the application board.
- To help minimize the residual voltage pulse that will be built-up at the protection device due to its nonzero turn-on impedance, it is mandatory to route the ESD device with minimum stub length so that the low-resistive, low-inductive path from signal to ground is established and does not increase the impedance between signal and ground.
- For an ESD protection array being railed to a power supply when no decoupling capacitor is available in close vicinity, consider using a decoupling capacitor (= 0.1 µF) tight to the VCC pin of the ESD protection. A positive strike will be partially diverted to this capacitor resulting in a lower residual voltage pulse.
- Ensure that there is enough metallization for the supply of signals at the interconnect side (VCC and GND in Figure 8-17) from connector to external protection because the interconnect may see between 8- to 30-A current in a short period of time during the ESD event.

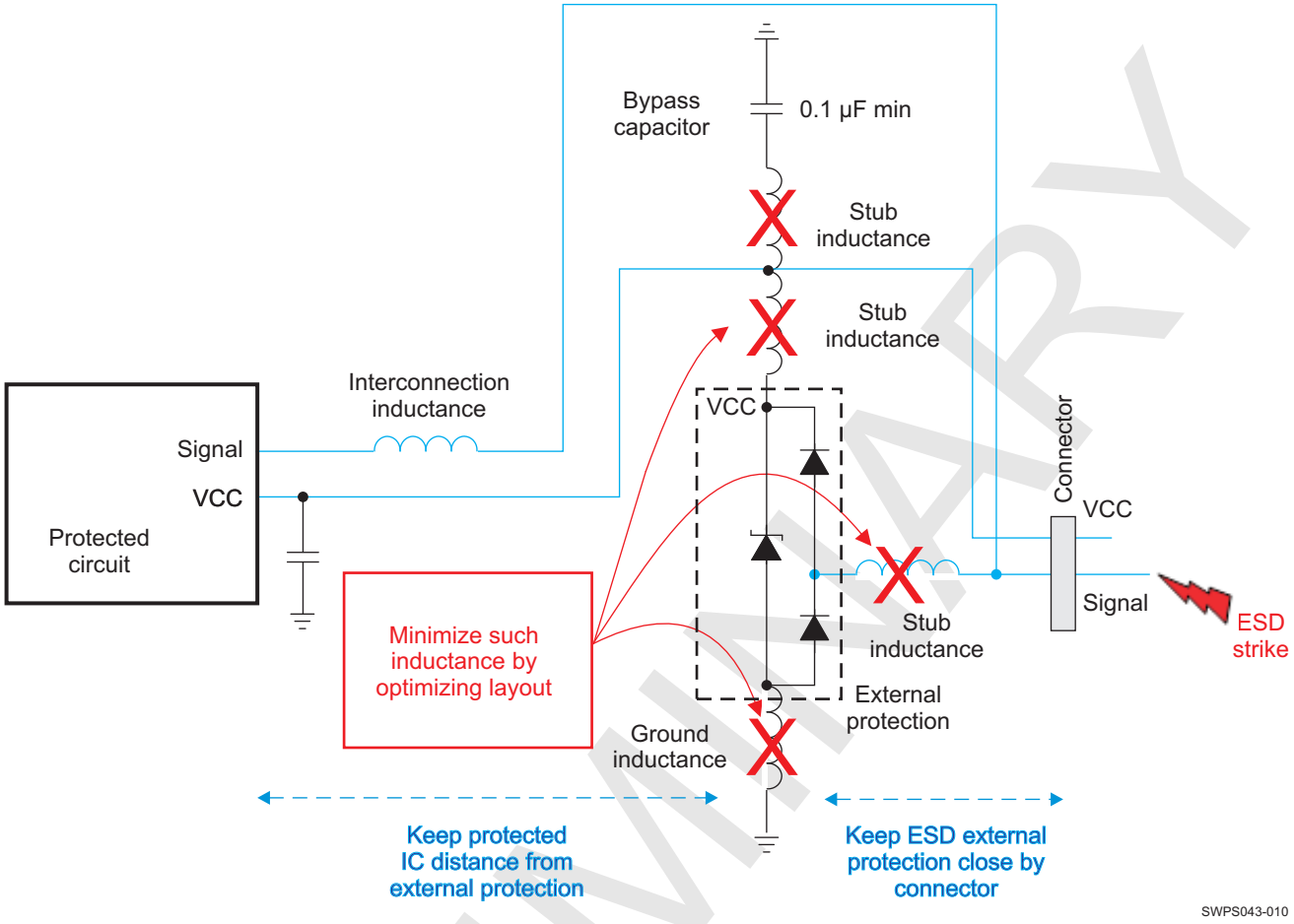

Figure 8-17. Recommendation for an ESD External Protection(1)

(1) To ensure normal behavior of the ESD protection (unwanted leakage), it is better to ground the ESD protection to the board ground rather than any local ground (example isolated shield or audio ground).

8.3.5.2 Miscellaneous EMC Guidelines to Mitigate ESD Immunity

- Avoid running critical signal traces (clocks, resets, interrupts, control signals, etc.) near PCB edges.
- Add high-frequency filtering: Decoupling capacitors close to the receivers rather than close to the drivers to minimize ESD coupling.
- Put a ground (guard) ring around the entire periphery of the PCB to act as a lightning rod.
- Connect the guard ring to the PCB ground plane to provide a low-impedance path for ESD-coupled current on the ring.
- Fill unused portions of the PCB with ground plane.
- Minimize circuit loops between power and ground by using a multilayer PCB with dedicated power and ground planes.
- Shield long line lengths (strip lines) to minimize radiated ESD.
- Avoid running traces over split ground planes. It is better to use a bridge connecting the two planes in one area.

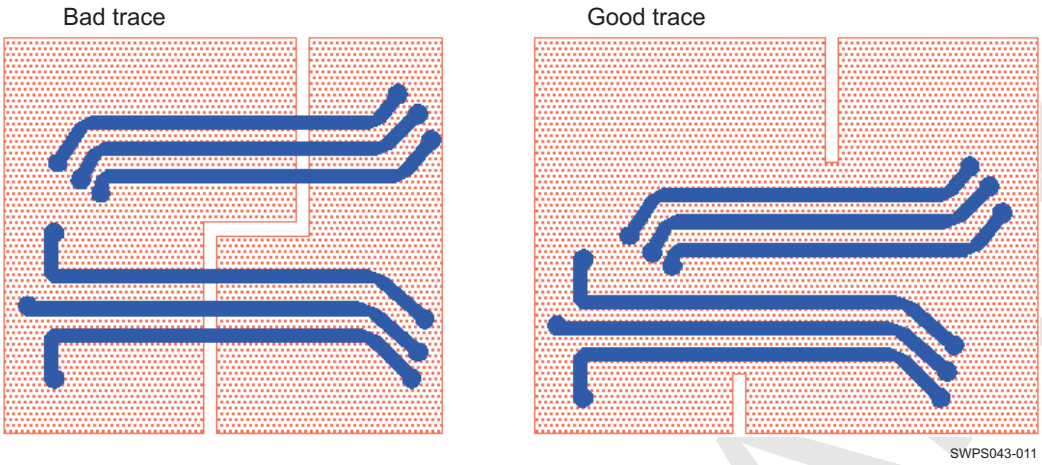

Figure 8-18. Trace Examples

- Always route signal traces and their associated ground returns as close to one another as possible to minimize the loop area enclosed by current flow:
  - At high frequencies current follows the path of least inductance.
  - At low frequencies current follows the path of least resistance.

8.3.6 EMI / EMC Issues Prevention

All high-speed digital integrated circuits can be sources of unwanted radiation, which can affect nearby sensitive circuitry and cause the final product to have radiated emission levels above the limits allowed by the EMC regulations if prevention steps are not taken. Likewise, analog and digital circuits can be susceptible to interferences from the outside world and picked up by the circuitry interconnections. To minimize the potential for EMI/EMC issues, the following guidelines are recommended to be followed.

8.3.6.1 Signal Bandwidth

To evaluate the frequency of digital signals, an estimated rule of thumb is to consider its bandwidth, f_{BW}, with respect to its rise time, t_R:

$f_{BW} \tilde{} 0.35 / t_R$

This frequency actually corresponds to the break point in the signal spectrum, where the harmonics start to decay at 40 dB per decade instead of 20 dB per decade.

8.3.6.2 Signal Routing

8.3.6.2.1 Signal Routing—Sensitive Signals and Shielding

Keep radio frequency (RF) sensitive circuitry (like GPS receivers, GSM/WCDMA, *Bluetooth*/WLAN transceivers, frequency modulation (FM) radio, ...) away from high-speed ICs (such as, the OMAP device, power and audio managers, chargers, memories) and ideally on the opposite side of the PCB. For improved protection it is recommended to place these emission sources in a shield can. If the shield can have a removable lid (two-piece shield), ensure there is low contact impedance between the fence and the lid. Leave some space between the lid and the components under it to limit the high-frequency currents induced in the lid. Limit the shield size to put any potential shield resonances above the frequencies of interest; see Figure 8-12, *Typical Impedance Profile of a Capacitor*.

8.3.6.2.2 Signal Routing—Outer Layer Routing

In case there is a need to use the outer layers for routing outside of shielded areas, it is recommended to route only static signals and make sure that these static signals do not carry any high-frequency components (due to parasitic coupling with other signals). In case of long traces, make provisions for a bypass capacitor near the signal source.

Routing of high-frequency clock signals on outer layers, even for a short distance, is discouraged, because their emission energy is concentrated at the discrete harmonics and can become significant even with poor radiators. Coplanar shielding of traces on outer layers (placing the ground near the sides of a track along its length) is effective only if the distance between the trace sides and the ground is smaller that the trace height above the ground reference plane. For modern multilayer PCBs this is often not possible so coplanar shielding will not be effective.

Do not route high-frequency traces near the periphery of the PCB, as the lack of a ground reference near the trace edges can increase EMI; see Section 8.3.6.3, *Ground Guidelines*.

8.3.6.3 Ground Guidelines

8.3.6.3.1 PCB Outer Layers

Ideally the areas on the top and bottom layers of the PCB that are not enclosed by a shield must be filled with ground after the routing is completed and connected with an adequate number of vias to the ground on the inner ground planes.

8.3.6.3.2 Metallic Frames

Ensure that all metallic parts are well connected to the PCB ground (like metallic frames for LCD screens, antenna reference planes, connector cages, flex cable grounds, and so forth). If using flex PCB ribbon cables to bring high-frequency signals off the PCB then ensure they are adequately shielded (coaxial cables or flex ribbons with a solid reference ground).

8.3.6.3.3 Connectors

For high-frequency signals going to connectors choose a fully shielded connector, if possible (for example, SD card connectors). For signals going to external connectors or that are routed over long distances, it is recommended to reduce their bandwidth by using low-pass filters (RC (resistor, capacitor) combinations or lossy ferrite inductors). These filters will help to prevent emissions from the board and can also improve the immunity from external disturbances.

8.3.6.3.4 Guard Ring on PCB Edges

The major advantage of a multilayer PCB with ground planes is the ground return path below each and every signal or power trace. As shown in Figure 8-19 the field lines of the signal return to the PCB ground as long as an infinite ground is available.

Traces or planes near the PCB edges do not have this infinite ground and therefore may radiate more than others. Thus, signals (like clocks) or power traces (like core power) identified as critical must not be routed in the vicinity of PCB edges, or, if not avoidable, must be accompanied by a guard ring on the PCB edge.

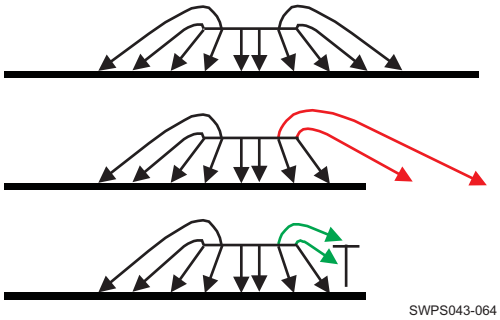

Figure 8-19. Field Lines of a Signal Above Ground

Figure 8-20. Guard Ring Routing

The intention of the guard ring is that HF energy, that otherwise would have been emitted from the PCB edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including the power layer) must be applied as shown in Figure 8-20.

As these traces must have the same (HF–) potential as the ground plane, they must be connected to the ground plane at least every 10 mm.

8.3.6.3.5 Analog and Digital Grounds

For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source at the same point. This ensures that both planes are at the same potential, while the transfer of noise from the digital to the analog domain is minimized.

8.4 Single-Ended Interfaces

8.4.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces:

- Line spacing:
  - For a line width equal to W, the spacing between two lines must be 2 × W, at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the OMAP5430 package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see Figure 8-21).

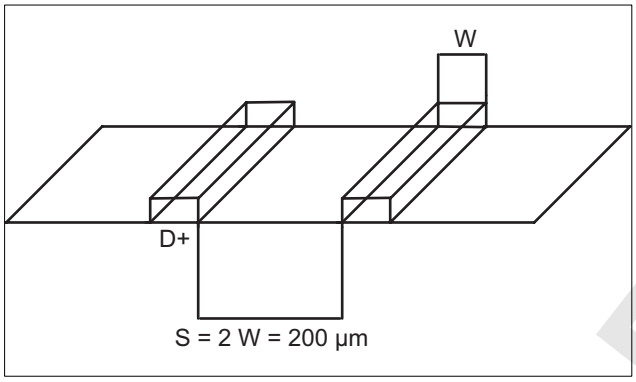

Figure 8-21. Guard Illustration

- Length matching (unless otherwise specified):
  - For bus or traces at frequencies less than 10 MHz: the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  - For bus or traces at frequencies greater than 10 MHz: the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance:
  - Unless otherwise specified, characteristic impedance for single-ended interfaces is recommended to be between 30 and 65 Ω.
- Multiple peripheral support:
  - For interfaces where multiple peripherals have to be supported in a star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

NOTE

The PCB recommendations described in the next sections make references to the default multiplexing mode signals. Different multiplexing modes other than the default one (usually mode 0) are available and configurable by software programming. For more information, see Table 2-2, *Multiplexing Characteristics*.

8.4.2 Single-Ended PCB Guidelines

The following interfaces follow the general guidelines of single-ended interfaces.

8.4.2.1 GPMC PCB Guidelines

The GPMC interface is used to interface with external memory and in particular supports various flash types [NOR or NAND] and can be set up to support different synchronous and asynchronous protocols.

It can support up to 88.6 MHz in read mode (NOR read synchronous mode) and write mode (NOR write synchronous mode).

8.4.2.1.1 GPMC Interface Pin Description

Table 8-1 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-1. GPMC Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NUMBER	SIGNAL NAME	BOTTOM BALL	IO SET NUMBER
gpmc_clk	C22	IO SMART(1)	gpmc_a22	E18	IO SMART(1)
gpmc_ad0	B21		gpmc_a23	D18	
gpmc_ad1	C21		gpmc_a24	B8	
gpmc_ad2	B20		gpmc_a25	C8	
gpmc_ad3	C20		gpmc_ncs0	E29	
gpmc_ad4	B19		gpmc_ncs1	C10	
gpmc_ad5	C19		gpmc_ncs2	B10	
gpmc_ad6	B18		gpmc_ncs3	B9 / E10	
gpmc_ad7	C18		gpmc_ncs4	C9	
gpmc_ad8	E26		gpmc_ncs5	C6	
gpmc_ad9	D26		gpmc_ncs6	B6	
gpmc_ad10	E25		gpmc_ncs7	E10	
gpmc_ad11	D25		gpmc_wait0	C29	
gpmc_ad12	E24		gpmc_wait1	C7	
gpmc_ad13	D24		gpmc_wait2	B7	
gpmc_ad14	E23		gpmc_wait3	E9	
gpmc_ad15	D23		gpmc_noe_nre	B5	
gpmc_a16	E21		gpmc_nwe	C5	
gpmc_a17	D21		gpmc_nwp	B22	
gpmc_a18	E20		gpmc_nbe1	B22	
gpmc_a19	D20		gpmc_nadv_ale	E22	
gpmc_a20	E19		gpmc_nbe0_cle	D22	
gpmc_a21	D19				

(1) The same IO buffer is used for all GPMC interfaces.

8.4.2.1.2 GPMC Interface PCB Requirements

Table 8-2 describes the GPMC PCB requirements for NOR and NAND applications.

Table 8-2. GPMC PCB Requirements and IO Programming

GPMC APPLICATIONS	MAXIMUM NUMBER OF PERIPHERALS	MAXIMUM FREQ. (MHz)	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
			MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
NOR flash read synchronous, write asynchronous	1	88.6	4	10	2	10	30	50	10	10
							51	65	10	01
PSRAM read or write synchronous	1	88.6	3	8	2	10	30	50	10	10
							51	65	10	01
NAND read or write synchronous	Up to 5	66.5	Clock = 12 Data = 16	Clock = 22 Data = 25	2	6	30	50	10	10
							51	65	10	01

8.4.2.2 HSI PCB Guidelines

The HSI interface is a high-speed serial interface that is typically used for communication with a modem. It supports maximum data rates of:

- In receive mode, 225 Mbps @OPP_NOM.
- In transmit mode, 192 Mbps @OPP_NOM.

NOTE

The 1.2-V mode is not supported in the OMAP5430 ES2.0 device.

8.4.2.2.1 HSI Interface Pin Description

Table 8-3 provides for each HSI signal the corresponding bottom ball and the IO set name.

Table 8-3. HSI Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME	SIGNAL NAME	BOTTOM BALL	IO SET NAME
hsi1_acdata	D14	IO SMART(1)	hsi2_acdata	C9	IO SMART(1)
hsi1_acflag	D15		hsi2_acflag	B9	
hsi1_acready	E13		hsi2_acready	C10	
hsi1_acwake	D13		hsi2_acwake	C8	
hsi1_cadata	E12		hsi2_cadata	B10	
hsi1_caflag	D12		hsi2_caflag	B7	
hsi1_caready	E14		hsi2_caready	C7	
hsi1_cawake	E15		hsi2_cawake	B8	

(1) The same IO buffer is used for all HSI interface signals.

8.4.2.2.2 HSI PCB Requirements

The HSI PCB recommendations are listed in Table 8-4:

Table 8-4. HSI PCB Requirements and IO Programming

FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		EXTERNAL RESISTANCE(1) (Ω)	IO REGISTER PROGRAMMING	
MIN	MAX	MIN	MAX	MIN	MAX		SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
1.5		3	5	42	58	50(2)(3)(5)	10	01
		5	7	42	58	27(2)(4)(5)		
2	5	3	5	42	50	10(6)		
				51	58	20(6)		
		5	7	42	50	NA		
				51	58	10(6)		

(1) External serial resistances have to be placed on the acdata and acflag PCB traces, close to the OMAP543x device.

(2) External resistance has been characterized with 50-Ω PCB trace.

(3) 50 O is the recommended value for a 3-cm PCB trace.

(4) 27 O is the recommended value for a 9-cm PCB trace.

(5) For all other PCB trace lengths, external resistance must be tuned between 27 Ω and 50 Ω.

(6) Recommendation for approximate value of external resistances. Values need to be fine tuned based on exact PCB characteristics and timing requirements.

8.4.2.3 SDMMC PCB Guidelines

The OMAP5430 device supports five SD / MMC Card interfaces.

8.4.2.3.1 SD Card PCB Guidelines

The OMAP5 can support external SD cards according to the SD standard:

- DS—Default speed at 24 MHz, 3-V signaling
- HS—High speed at 48 MHz, 3-V signaling
- SDR12—SDR mode at 24 MHz, 1.8-V signaling
- SDR25—SDR mode at 48 MHz, 1.8-V signaling
- SDR50—SDR mode at 96 MHz, 1.8-V signaling
- SDR104—SDR mode at 192 MHz, 1.8-V signaling
- DDR50—DDR mode at 48 MHz, 1.8-V signaling

8.4.2.3.1.1 SD Card Interface Pin Description

Table 8-5 provides for each SD Card signal the corresponding bottom ball and the IO set name.

Table 8-5. SD Card Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
sdcard_clk	E3	SDIO Set (1.8 V, 3.0 V)
sdcard_cmd	E2	
sdcard_data0	G3	
sdcard_data1	G2	
sdcard_data2	F2	
sdcard_data3	F3	

8.4.2.3.1.2 SD Card PCB Requirements With External SD Card

The SD Card PCB recommendations are listed in Table 8-6:

Table 8-6. SD Card PCB Requirements and IO Programming

SD CARD APPLICATIONS	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING
		MIN	MAX	MIN	MAX	MIN	MAX	IMPEDANCE ic[1:0]
DS—Default speed at 24 MHz, 3-V signaling, SDR, half-cycle mode	1	7	10	2	10	30	40	01 (Type A)
						41	50	10 (Type C)
						51	65	10 (Type C)
HS—High speed at 48 MHz, 3-V signaling, SDR, half-cycle mode	1	7	10	2	10	30	40	01 (Type A)
						41	50	10 (Type C)
						51	65	10 (Type C)
SDR12 at 24 MHz, 1.8-V signaling, SDR, half-cycle mode	1	7	10	2	10	30	40	01 (Type A)
						41	50	00 (Type B)
						51	65	10 (Type C)
SDR25 at 48 MHz, 1.8-V signaling, SDR, half-cycle mode	1	7	10	2	10	30	40	01 (Type A)
						41	50	00 (Type B)
						51	65	10 (Type C)
SDR50 at 96 MHz, 1.8-V signaling, SDR, half-cycle mode	1	7	10	2	10	30	40	01 (Type A)
						41	50	00 (Type B)
						51	65	10 (Type C)
DDR50 at 48 MHz, 1.8-V signaling DDR	1	7	10	2	10	30	40	01 (Type A)
						41	50	00 (Type B)
						51	65	10 (Type C)

Table 8-6. SD Card PCB Requirements and IO Programming (continued)

SD CARD APPLICATIONS	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING
		MIN	MAX	MIN	MAX	MIN	MAX	IMPEDANCE ic[1:0]
SDR104 at 192 MHz, 1.8-V signaling, SDR, half-cycle mode	1	7	10	2	10	30	40	01 (Type A)
						41	50	00 (Type B)
						51	65	10 (Type C)

8.4.2.3.1.3 SD Card System ESD With External SD Card Configuration

NOTE

For more information on system ESD or EMI / EMC, see Section 8.3.5, *System ESD Generic Guidelines* and Section 8.3.6, *EMI / EMC Issues Prevention*.

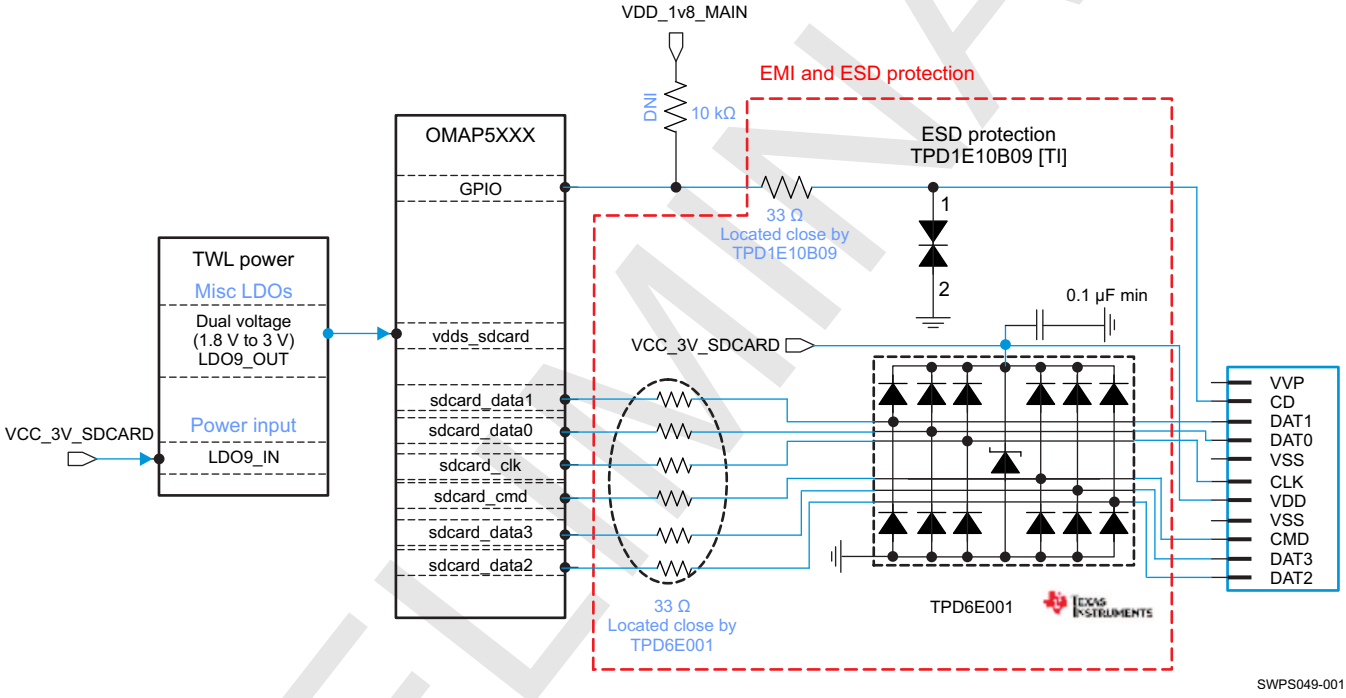

Figure 8-22. SD Card Implementation Proposal With External SD Card

Table 8-7. SD Card Component Reference

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
SD Card	TVS	TI	TPD6E001RSE
	TVS	TI	TPD1E10B09
	CFB	Murata	[600R / 100M / 0402] BLM15AG601SN1
	C	Murata	[0.1 µF / 10 V / 0402] GRM155R71A104KA0
	R	-	33 Ω

Some guidelines regarding SD Card system ESD:

- SD connector may have card detect and write protect pins, consider using an ESD external protection device with low turn-on resistance (R_{dyn} = 1 Ω).
- TPD1E10B09 being asymmetrical, it is recommended to respect the mounting configuration (1: signal, 2: ground).

CAUTION

System level ESD results are dependent on the components being connected to the product.

Part numbers that are different than the reference board specification (see Table 8-7, *SD Card Component Reference*) are not assured to meet system level ESD requirements.

8.4.2.3.2 WLSDIO (SDIO3) PCB Guidelines

The OMAP5 can support on-board peripherals compliant with the SD standard:

- SDR12—SDR mode at 24 MHz
- SDR25—SDR mode at 48 MHz

8.4.2.3.2.1 WLSDIO (SDIO3) Interface Pin Description

Table 8-8 provides for each WLSDIO signal the corresponding bottom ball and the IO set name.

Table 8-8. WLSDIO Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
wlsdio_clk	AK29	IO SMART
wlsdio_cmd	AJ29	
wlsdio_data0	AJ30	
wlsdio_data1	AK30	
wlsdio_data2	AJ31	
wlsdio_data3	AK31	

8.4.2.3.2.2 WLSDIO (SDIO3) PCB Requirements

The WLSDIO (SDIO3) PCB recommendations are listed in Table 8-9:

Table 8-9. WLSDIO PCB Requirements and IO Programming

WLSDIO APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
SDR12—SDR mode at 24 MHz, half-cycle mode	1	2.5	5	2	10	30	40	10	10
						41	50	10	01
						51	65	10	00
SDR25—SDR mode at 48 MHz, half-cycle mode	1	2.5	5	2	10	30	40	01	00
						41	50	01	00
						51	65	01	00

8.4.2.3.3 SDIO4 PCB Guidelines

The OMAP5430 device can support on-board peripherals compliant with the SD standard:

- SDR12—SDR mode at 24 MHz
- SDR25—SDR mode at 48 MHz

8.4.2.3.3.1 SDIO4 Interface Pin Description

Table 8-10 provides for each SDIO4 signal the corresponding bottom ball and the IO set name.

Table 8-10. SDIO4 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
sdio4_clk	AL28	IO SMART
sdio4_cmd	AM28	
sdio4_data0	AE30	
sdio4_data1	AD30	
sdio4_data2	AE29	
sdio4_data3	AD29	

8.4.2.3.3.2 SDIO4 PCB Requirements

The SDIO4 PCB recommendations are listed in Table 8-11:

Table 8-11. SDIO4 PCB Requirements and IO Programming

SDIO4 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
SDR12—SDR mode at 24 MHz, half-cycle mode	1	2.5	5	2	10	30	40	10	10
						41	50	10	01
						51	65	10	00
SDR25—SDR mode at 48 MHz, half-cycle mode	1	2.5	5	2	10	30	40	01	00
						41	50	01	00
						51	65	01	00

8.4.2.3.4 SDIO5 PCB Guidelines

The OMAP5 can support on-board peripherals compliant with the SD standard:

- SDR12—SDR mode at 24 MHz
- SDR25—SDR mode at 48 MHz
- SDR50—SDR mode at 96 MHz (modem application—8 data bits)

Data bus of the SDIO5 interface is extended to 8 bits to support the modem application in the SDR50 prototocol.

8.4.2.3.4.1 SDIO5 Interface Pin Description

Table 8-12 provides for each SDIO5 signal the corresponding bottom ball and the IO set name.

Table 8-12. SDIO5 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
sdio5_clk	AJ32	IO SMART
sdio5_cmd	AK32	
sdio5_data0	AK27	
sdio5_data1	AK26	
sdio5_data2	AJ26	
sdio5_data3	AJ27	
sdio5_data4	AM28	
sdio5_data5	AL28	
sdio5_data6	AK28	
sdio5_data7	AJ28	

8.4.2.3.4.2 SDIO5 PCB Requirements

The SDIO5 PCB recommendations are listed in Table 8-13:

Table 8-13. SDIO5 PCB Requirements and IO Programming

SDIO5 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
SDR12—SDR mode at 24 MHz, half-cycle mode	1	2.5	5	2	10	30	40	10	10
						41	50	10	01
						51	65	10	00
SDR25—SDR mode at 48 MHz, half-cycle mode	1	2.5	5	4	10	30	40	01	00
						41	50	01	00
						51	65	01	00
SDR50—SDR mode at 96 MHz, half-cycle mode (8 data bits)	1	2.5	5	1	5	30	40	10	11
						41	50	10	10
						51	65	10	01

8.4.2.3.5 eMMC PCB Guidelines

The eMMC interface supports 1.2-V and 1.8-V operations.

8.4.2.3.5.1 eMMC Interface

The eMMC interface is used to interface with external memory. It can support the eMMC JC64 standard:

- Standard JC64 SDR at 24 MHz
- High-speed JC64 SDR at 48 MHz
- High-speed JC64 DDR at 48 MHz
- High-speed HS200 JC64 SDR at 192 MHz

8.4.2.3.5.2 eMMC Interface Pin Description

Table 8-14 provides for each eMMC signal the corresponding bottom ball and the IO set name.

Table 8-14. eMMC Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
emmc_clk	AL2	IO SMART
emmc_cmd	AK4	
emmc_data0	AK3	
emmc_data1	AJ4	
emmc_data2	AK2	
emmc_data3	AJ3	
emmc_data4	AH2	
emmc_data5	AJ2	
emmc_data6	AH3	
emmc_data7	AH4	

8.4.2.3.5.3 eMMC PCB Requirements

The eMMC PCB recommendations are listed in Table 8-15:

Table 8-15. eMMC PCB Requirements and IO Programming

eMMC APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
Standard JC64 SDR at 24 MHz, half-cycle mode	1	2.5	5	2	10	30	40	10	10
						41	50	10	01
						51	65	10	01
High-speed JC64 SDR at 48 MHz, half-cycle mode	1	2.5	5	2	10	30	40	10	10
						41	50	10	01
						51	65	10	01
High-speed JC64 DDR at 48 MHz	1	2.5	5	2	10	30	40	10	10
						41	50	10	01
						51	65	10	01
High-speed HS200 JC64 SDR at 192 MHz, half-cycle mode	1	2.5	5	2	10	30	35	11	11
						36	45	11	10
						46	65	11	01

8.4.2.4 SPI PCB Guidelines

The OMAP5 processor provides four SPI interfaces:

- SPI1 and SPI2 are used in master mode only.
- SPI3 and SPI4 can be used in master or slave mode.

See the following sections for a complete description of the different SPI configurations supported by the OMAP5430 device.

8.4.2.4.1 SPI1 Interface

The maximum speed of the SPI1 interface in master mode is 48 MHz, 24 MHz, or 12 MHz depending on the number of external peripherals.

8.4.2.4.1.1 SPI1 Interface Pin Description

Table 8-16 provides for each SPI1 signal the corresponding bottom ball and the IO set name.

Table 8-16. SPI1 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
mcspi1_clk	AH32	IO SMART
mcspi1_cs0	AG31	
mcspi1_cs1	AH30	
mcspi1_cs2	AJ32	
mcspi1_cs3	AK32	
mcspi1_simo	AH31	
mcspi1_somi	AG32	

8.4.2.4.1.2 SPI1 PCB Requirements

The SPI interface 1 PCB recommendations are listed in Table 8-17:

Table 8-17. SPI1 PCB Requirements and IO Programming(1)(2)

SPI1 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
12-MHz master mode	2	7	10	4	10	30	65	01	00
24-MHz master mode	2	7	10	2	10	30	65	01	00
48-MHz master mode	1	2.5	5	2	10	30	65	10	01
12-MHz master mode—bidirectional simo signal (somi unused)	1	2.5	5	1	10	30	65	10	00

(1) Bussed signals (mcspi1_clk, mcspi1_simo, and mcspi1_somi) must be T-routed or star routed.

(2) Chip selects (mcspi1_cs[3:0]) are point-to-point routed.

8.4.2.4.2 SPI2 Interface

The maximum speed of the SPI2 interface in master mode is 48 MHz, 24 MHz, or 12 MHz depending on the number of external peripherals.

8.4.2.4.2.1 SPI2 Interface Pin Description

Table 8-18 provides for each SPI2 signal the corresponding bottom ball and the IO set name.

Table 8-18. SPI2 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
mcspi2_clk	AK21	IO SMART
mcspi2_cs0	Ak20	
mcspi2_cs1	AJ9	
mcspi2_simo	AJ18	
mcspi2_somi	AK23	

8.4.2.4.2.2 SPI2 PCB Requirements

The SPI interface 2 PCB recommendations are listed in Table 8-19:

Table 8-19. SPI2 PCB Requirements and IO Programming(1)(2)

SPI2 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
12-MHz master mode	2	7	10	4	10	30	65	01	00
24-MHz master mode	2	7	10	2	10	30	65	01	00
48-MHz master mode	1	2.5	5	2	10	30	65	10	01
12-MHz master mode—bidirectional simo signal (somi unused)	1	2.5	5	1	10	30	65	10	00

(1) Bussed signals (mcspi2_clk, mcspi2_simo, and mcspi2_somi) must be T-routed or star routed.

(2) Chip selects (mcspi2_cs[1:0]) are point-to-point routed.

8.4.2.4.3 SPI3 Interface

The maximum speed of the SPI3 interface is 48 MHz in master mode and 24 MHz in slave mode. Only 1 external peripheral is supported.

8.4.2.4.3.1 SPI3 Interface Pin Description

Table 8-20 provides for each SPI3 signal the corresponding bottom ball and the IO set name.

Table 8-20. SPI3 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
mcspi3_clk	B6	IO SMART
mcspi3_cs0	B5	
mcspi3_simo	C6	
mcspi3_somi	C5	

8.4.2.4.3.2 SPI3 PCB Requirements

The SPI interface 3 PCB recommendations are listed in Table 8-21:

Table 8-21. SPI3 PCB Requirements and IO Programming

SPI3 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
16-MHz slave mode	1	2.5	5	2	10	30	65	10	00
48-MHz master mode	1	2.5	5	2	10	30	65	10	01

8.4.2.4.4 SPI4 Interface

The maximum speed of the SPI4 interface is 48 MHz in master mode and 24 MHz in slave mode. Only 1 external peripheral is supported.

8.4.2.4.4.1 SPI4 Interface Pin Description

Table 8-22 provides for each SPI4 signal the corresponding bottom ball and the IO set name.

Table 8-22. SPI4 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
mcspi4_clk	AK29	IO SMART
mcspi4_cs0	AJ31	
mcspi4_simo	AJ30	
mcspi4_somi	AK30	

8.4.2.4.4.2 SPI4 PCB Requirements

The SPI interface 4 PCB recommendations are listed in Table 8-23:

Table 8-23. SPI4 PCB Requirements and IO Programming

SPI4 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
16-MHz slave mode	1	2.5	5	2	10	30	65	10	00
48-MHz master mode	1	2.5	5		10	30	65	10	01

8.4.2.5 USB PCB Guidelines

The OMAP5430 device features two USB controllers which support the following configurations:

- The first controller (USBD0, USB SS DRD controller) supports the following protocols:
  - High-speed [480 Mbits] DRD with OMAP5430 embedded PHY.

NOTE

For more information on USBD0 PHY in HS, see Section 8.5.3.1, *USB High-Speed PHY Interface (480 Mbps)*.

  - Super-speed [5 Gbits] DRD with OMAP5430 embedded PHY.

NOTE

For more information on USBD0 PHY in super speed, see Section 8.5.3.2, *USB Super-Speed PHY Interface (5 Gbps)*.

  - High-speed [480 Mbits] DRD ULPI PHY implementation.

NOTE

For more information on USBD0 ULPI PHY PCB recommendations, see Section 8.4.2.5.1, *USBD0 (USB SS DRD Controller) ULPI PHY Interface.*

- The second controller (USBB, host controller) supports, on three different ports, B1, B2, and B3, the following protocols:
  - Port B1:
    - High-speed [480 Mbits] HS IC interchip 2-pin configuration
    - High-speed [480 Mbits] ULPI PHY implementation

NOTE

For more information on USBB1 HSIC or ULPI PHY PCB recommendations, see Section 8.4.2.5.2, *USBB1 (Host Controller) Interface.*

  - Port B2:
    - High-speed [480 Mbits] HS IC interchip 2-pin configuration
    - High-speed [480 Mbits] ULPI TLL PHY implementation
    - Low-speed and Full-speed [12 Mbits] multimode implementations in 2-, 3-, 4-, or 6-pin configuration

NOTE

For more information on USBB1 HSIC or ULPI PHY PCB recommendations, see Section 8.4.2.5.3, *USBB2 (Host Controller) Interface.*

  - Port B3:
    - High-speed [480 Mbits] HS IC interchip 2-pin configuration

NOTE

For more information on USBB1 HSIC or ULPI PHY PCB recommendations, see Section 8.4.2.5.4, *USBB3 (Host Controller) Interface.*

8.4.2.5.1 USBD0 (USB SS DRD Controller) ULPI PHY Interface

8.4.2.5.1.1 USBD0 ULPI PHY Pin Description

Table 8-24 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-24. USBD0 ULPI PHY Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbd0_ulpiphy_clk	AH32	IO SMART
usbd0_ulpiphy_dir	AH31	
usbd0_ulpiphy_nxt	AG32	
usbd0_ulpiphy_stp	AK27	
usbd0_ulpiphy_data0	AG31	
usbd0_ulpiphy_data1	AH30	
usbd0_ulpiphy_data2	AJ32	
usbd0_ulpiphy_data3	AK32	
usbd0_ulpiphy_data4	AK28	
usbd0_ulpiphy_data5	AM28	
usbd0_ulpiphy_data6	AE30	
usbd0_ulpiphy_data7	AL28	

8.4.2.5.1.2 USBD0 ULPI PHY PCB Requirements

Table 8-25 describes the USBD0 ULPI PHY PCB requirements.

Table 8-25. USBD0 ULPI PHY PCB Requirements and IO Programming

USBD0 ULPI PHY APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
60 MHz ULPI Slave mode SDR—8 data bits	2.5	5	1	10	30	40	10	10
					41	50	10	10
					51	65	10	01

8.4.2.5.2 USBB1 (Host Controller) Interface

8.4.2.5.2.1 USBB1 (Host Controller) High-Speed Interchip (HSIC)—2 Pins

This implementation supports HS (480 Mbits) in 2-pin configuration at 1.2 V.

8.4.2.5.2.1.1 USBB1—HSIC Pin Description

Table 8-26 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-26. USBB1 HSIC Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbb1_hsic_data	C26	DDR SE IO SET
usbb1_hsic_strobe	B26	

8.4.2.5.2.1.2 USBB1—HSIC PCB Requirements

Table 8-27 describes the USBB1 HSIC PCB requirements.

Table 8-27. USBB1 HSIC PCB Requirements and IO Programming

USBB1 HSIC APPLICATION (1)	TRACE LENGTH (cm)		FAR-END LOAD (pF)		NEAR END EXTERNAL RESISTOR REQUIRED (2) (O)	CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX		MIN	MAX	SLEW RATE REGISTER SR[1:0]	IMPEDANCE REGISTER I[1:0]
USBB1 HOST HSIC 480 Mbits 2-pin asynchronous	0	2	3		39	45	55	010	000
			4		39	45	55	010	001 (3)
			5		33	45	55	010	001
			6		22	45	55	010	001
			7		10	45	55	010	001
			8	9	not required	45	55	010	001
			10		not required	45	55	010	010
	>2	6	3		22	45	55	010	001 (3)
			4		18	45	55	010	001 (3)
			5		15	45	55	010	001
			6	10	not required	45	55	010	001 (3)
	>6	10 (4)	3	4	not required	45	55	010	000 (3)
			5		10	45	55	010	001
			6	8	not required	45	55	010	001
			9	10	not required	45	55	010	010

PARAMETER	VALUE		UNIT
	MIN	MAX	
Skew due to crosstalk between data and strobe signals, including board skew(5)		50	ps

(1) Recommendations of the table are valid for a skew between the strobe and data signals of 50 ps. This skew value includes the crosstalk between signals and the trace length uncertainty.

(2) For some specific cases, external resistors have to be added for the data and strobe PCB traces to fulfill the slew rate defined by the High-Speed Inter-Chip USB (v1.0) specification. Resistors have to be located as close as possible to the OMAP5430 device.

(3) For some specific cases, the High-Speed Inter-Chip USB (v1.0) specification is not fully verified from a slew rate perspective, the rise and fall times can be faster. No functional issue is expected, but a bit higher than in the specification.

(4) To ensure performances with interconnect length up to 10 cm, the coupling between lines has to be minimized. Spacing between the strobe and data lines must be > 3 × W (5 × W recommended).

(5) This skew budget includes the effect of the crosstalk between the traces and the PCB trace length uncertainty.

8.4.2.5.2.2 USBB1 (Host Controller)—ULPI PHY

This interface operates at 480 Mbits in high-speed mode with external PHY transceiver.

8.4.2.5.2.2.1 USBB1—ULPI PHY Pin Description

Table 8-28 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-28. USBB1 ULPI PHY Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbb1_ulpiphy_clk	C7	IO SMART
usbb1_ulpiphy_dir	B8	
usbb1_ulpiphy_nxt	C10	
usbb1_ulpiphy_stp	C8	
usbb1_ulpiphy_data0	B7	
usbb1_ulpiphy_data1	B10	
usbb1_ulpiphy_data2	B9	
usbb1_ulpiphy_data3	C9	
usbb1_ulpiphy_data4	C5	
usbb1_ulpiphy_data5	B5	
usbb1_ulpiphy_data6	C6	
usbb1_ulpiphy_data7	B6	

8.4.2.5.2.2.2 USBB1—ULPI PHY PCB Requirements

Table 8-29 describes the USBB1 ULPI PHY PCB requirements.

Table 8-29. USBB1 ULPI PHY PCB Requirements and IO Programming

USBB2 ULPI PHY APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
USBB1 (HOST controller) 60 MHz ULPI slave mode SDR —8 data bits	2.5	5	1	10	30	40	10	10
					41	50	10	10
					51	65	10	01

8.4.2.5.3 USBB2 (Host Controller) Interface

8.4.2.5.3.1 USBB2 (Host Controller) HSIC—2 Pins

This implementation supports high-speed (480 Mbits) in 2-pin configuration at 1.2 V.

8.4.2.5.3.1.1 USBB2—HSIC Pin Description

Table 8-30 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-30. USBB2 HSIC Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbb2_hsic_data	C25	DDR SE IO SET
usbb2_hsic_strobe	B25	

8.4.2.5.3.1.2 USBB2—HSIC PCB Requirements

Table 8-31 describes the USBB2 HSIC PCB requirements.

Table 8-31. USBB2 HSIC PCB Requirements and IO Programming

USBB2 HSIC APPLICATION (1)	TRACE LENGTH (cm)		FAR-END LOAD (pF)		NEAR END EXTERNAL RESISTOR REQUIRED (2) (Ω)	CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX		MIN	MAX	SLEW RATE REGISTER SR[1:0]	IMPEDANCE REGISTER I[1:0]
USBB1 HOST HSIC 480 Mbits 2-pin asynchronous	0	2	3		39	45	55	010	000
			4		39	45	55	010	001 (3)
			5		33	45	55	010	001
			6		22	45	55	010	001
			7		10	45	55	010	001
			8	9	not required	45	55	010	001
			10		not required	45	55	010	010
	>2	6	3		22	45	55	010	001 (3)
			4		18	45	55	010	001 (3)
			5		15	45	55	010	001
			6	10	not required	45	55	010	001 (3)
	>6	10 (4)	3	4	not required	45	55	010	000 (3)
			5		10	45	55	010	001
			6	8	not required	45	55	010	001
			9	10	not required	45	55	010	010

PARAMETER	VALUE		UNIT
	MIN	MAX	
Skew due to crosstalk between data and strobe signals, including board skew (5)		50	ps

(1) Recommendations of the table are valid for a skew between the strobe and data signals of 50 ps. This skew value includes the crosstalk between signals and the trace length uncertainty.

(2) For some specific cases, external resistors have to be added for the data and strobe PCB traces to fulfill the slew rate defined by the High-Speed Inter-Chip USB (v1.0) specification. Resistors have to be located as close as possible to the OMAP5430 device.

(3) For some specific cases, the High-Speed Inter-Chip USB (v1.0) specification is not fully verified from slew rate perspective, the rise and fall times can be faster. No functional issue expected but a bit higher than in the specification.

(4) To ensure performances with interconnect length up to 10 cm, the coupling between lines has to be minimized. Spacing between the strobe and data lines must be > 3 × W (5 × W recommended).

(5) This skew budget includes the effect of the crosstalk between the traces and the PCB trace length uncertainty.

8.4.2.5.3.2 USBB2 (Host Controller)—ULPI TLL PHY

This USBB2 TLL PHY interface operates at 480 Mbits in HS without an external PHY transceiver (transceiverless link).

8.4.2.5.3.2.1 USBB2—ULPI TLL PHY Pin Description

Table 8-32 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-32. USBB2 ULPI PHY Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbb2_ulpitll_clk	E13	IO SMART
usbb2_ulpitll_dir	D13	
usbb2_ulpitll_nxt	E14	
usbb2_ulpitll_stp	E15	
usbb2_ulpitll_data0	D15	
usbb2_ulpitll_data1	D14	
usbb2_ulpitll_data2	D12	
usbb2_ulpitll_data3	E12	
usbb2_ulpitll_data4	D10	
usbb2_ulpitll_data5	E9	
usbb2_ulpitll_data6	D9	
usbb2_ulpitll_data7	E10	

8.4.2.5.3.2.2 USBB2—ULPI TLL PHY PCB Requirements

Table 8-33 describes the USBB2 ULPI PHY PCB requirements.

Table 8-33. USBB2 ULPI TLL PHY PCB Requirements and IO Programming

USBB2 ULPI PHY TLL APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
USBB2 (HOST controller) 60 MHz ULPI Slave mode SDR —8 data bits	2.5	5	1	10	30	40	10	10
					41	50	10	10
					51	65	10	01

8.4.2.5.3.3 USBB2 (Host Controller)—Low-Speed / Full-Speed Multimode Interface

This interface supports low- / full-speed multimode implementations in 2-, 3-, 4-, or 6-pin configuration and is multiplexed twice on the OMAP5 device.

8.4.2.5.3.3.1 USBB2—Low-Speed / Full-Speed Multimode Pin Description

Table 8-34 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-34. USBB2 Low-Speed / Full-Speed Multimode Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbb2_mm_txen	AJ28	IO SMART
usbb2_mm_txdat	AK28	
usbb2_mm_rxrcv	AK26	
usbb2_mm_txse0	AK27	
usbb2_mm_rxdm	AJ26	
usbb2_mm_rxdp	AJ27	

8.4.2.5.3.3.2 USBB2—Low-Speed / Full-Speed Multimode PCB Requirements

Table 8-35 describes the USBB2 low-speed / full-speed multimode PCB requirements.

Table 8-35. USBB2 Low-Speed / Full-Speed Multimode PCB Requirements and IO Programming

USBB2 LOW-/ FULL-SPEED MULTIMODE APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
USBB2 (HOST controller) Up to 12 MHz low- / full-speed multimode	2.5	5	1	10	30	40	01	11
					41	50	01	10
					51	65	01	01

8.4.2.5.4 USBB3 (Host Controller) Interface

8.4.2.5.4.1 USBB3 (Host Controller) HSIC—2 Pins

This implementation supports HS (480 Mbits) in 2-pin configuration at 1.2 V.

8.4.2.5.4.1.1 USBB3—HSIC Pin Description

Table 8-36 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-36. USBB3 HSIC Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
usbb3_hsic_data	D30	DDR SE IO SET
usbb3_hsic_strobe	D29	

8.4.2.5.4.1.2 USBB3—HSIC PCB Requirements

Table 8-37 describes the USBB3 HSIC PCB requirements.

Table 8-37. USBB3 HSIC PCB Requirements and IO Programming

USBB3 HSIC APPLICATION (1)	TRACE LENGTH (cm)		FAR-END LOAD (pF)		NEAR END EXTERNAL RESISTOR REQUIRED (2) (Ω)	CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX		MIN	MAX	SLEW RATE REGISTER SR[1:0]	IMPEDANCE REGISTER I[1:0]
USBB1 HOST HSIC 480 Mbits 2-pin asynchronous	0	2	3		39	45	55	010	000
			4		39	45	55	010	001 (3)
			5		33	45	55	010	001
			6		22	45	55	010	001
			7		10	45	55	010	001
			8	9	not required	45	55	010	001
			10		not required	45	55	010	010
	>2	6	3		22	45	55	010	001 (3)
			4		18	45	55	010	001 (3)
			5		15	45	55	010	001
			6	10	not required	45	55	010	001 (3)
	>6	10 (4)	3	4	not required	45	55	010	000 (3)
			5		10	45	55	010	001
			6	8	not required	45	55	010	001
			9	10	not required	45	55	010	010

PARAMETER	VALUE		UNIT
	MIN	MAX	
Skew due to cross talk between data and strobe signals, including board skew (5)		50	ps

(1) Recommendations of the table are valid for a skew between the strobe and data signals of 50 ps. This skew value includes the crosstalk between signals and the trace length uncertainty.

(2) For some specific cases, external resistors have to be added for the data and strobe PCB traces to fulfill the slew rate defined by the High-Speed Inter-Chip USB (v1.0) specification. Resistors have to be located as close as possible to the OMAP5430 device.

(3) For some specific cases, the high-speed interchip USB (v1.0) specification is not fully verified from slew rate perspective, the rise and fall times can be faster. No functional issue expected but a bit higher than in the specification.

(4) To ensure performances with interconnect length up to 10 cm, the coupling between lines has to be minimized. Spacing between the strobe and data lines must be > 3 × W (5 × W recommended).

(5) This skew budget includes the effect of the crosstalk between the traces and the PCB trace length uncertainty.

8.4.2.6 Audio McBSP PCB Guidelines

The OMAP5 provides three McBSP interfaces. These interfaces are used for transmission of audio to or from various peripherals.

8.4.2.6.1 McBSP1 Interface

McBSP1 interface supports different modes: half- or full-cycle mode, master-slave and TDM multichannel configuration.

8.4.2.6.1.1 McBSP1 Interface Pin Description

Table 8-38 provides for each McBSP1 signal the corresponding bottom ball and the IO set name.

Table 8-38. McBSP1 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
abemcbsp1_clkx	T30	IO SMART
abemcbsp1_dr	T29	
abemcbsp1_dx	N29	
abemcbsp1_fsx	P30	

8.4.2.6.1.2 McBSP1 PCB Requirements

The McBSP1 interface PCB recommendations are listed in Table 8-39:

Table 8-39. McBSP1 PCB Requirements and IO Programming

McBSP1 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
I2S format (non-TDM mode), master or slave mode, full- or half-cycle mode at 12.288 MHz	1	2.5	5	1	10	30	40	10	10
						41	50	10	10
						51	65	10	01
I2S format in TDM mode, multiple peripherals, master or slave mode, half-cycle mode at 6.144 MHz	up to 5	5	25	1	10	30	40	00	00
						41	50	00	00
						51	65	00	00
I2S format in TDM mode, single peripheral, slave mode, full-cycle mode at 49.12 MHz (input only)	1	2.5	5	2.5	5	30	40	10	10
						41	50	10	10
						51	65	10	01

8.4.2.6.2 McBSP2 Interface

McBSP2 interface supports different modes: half- or full-cycle mode, master-slave.

8.4.2.6.2.1 McBSP2 Interface Pin Description

Table 8-40 provides for each McBSP2 signal the corresponding bottom ball and the IO set name.

Table 8-40. McBSP2 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
abemcbsp2_clkx	M32	IO SMART
abemcbsp2_dr	N31	
abemcbsp2_dx	N32	
abemcbsp2_fsx	M31	

8.4.2.6.2.2 McBSP2 PCB Requirements

The McBSP2 interface PCB recommendations are listed in Table 8-41:

Table 8-41. McBSP2 PCB Requirements and IO Programming

McBSP2 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
I2S format (non-TDM mode), master or slave mode, full- or half-cycle mode at 12.288 MHz	2	7	10	1	10	30	40	01	00
I2S format in TDM mode, single peripheral, master or slave mode, full- or half-cycle mode at 12.288 MHz	1	2.5	5	2.5	5	30	40	10	10
						41	50	10	10
						51	65	10	01

8.4.2.6.3 McBSP3 Interface

McBSP3 interface is multiplexed twice on the OMAP5430 device and supports different modes: half- or full-cycle mode, master-slave.

8.4.2.6.3.1 McBSP3 Interface Pin Description

Table 8-42 provides for each McBSP3 signal the corresponding bottom ball and the IO set name.

Table 8-42. McBSP3 Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME	BOTTOM BALL	IO SET NAME
abemcbsp3_clkx	L30	IO SMART(1)	P29	IO SMART(1)
abemcbsp3_dr	M29		P31	
abemcbsp3_dx	M30		P32	
abemcbsp3_fsx	L29		R30	

(1) Same IO buffer is used for all McBSP3 interfaces.

8.4.2.6.3.2 McBSP3 PCB Requirements

The McBSP3 interface PCB recommendations are listed in Table 8-43:

Table 8-43. McBSP3 PCB Requirements and IO Programming

McBSP3 APPLICATION	PERIPHERAL NUMBER	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER PROGRAMMING	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE SC[1:0]	IMPEDANCE DS[1:0]
I2S format (non-TDM mode), master or slave mode, full- or half-cycle mode at 12.288 MHz	2	7	10	1	10	30	40	01	00
I2S format in TDM mode, single peripheral, master or slave mode, full- or half-cycle mode at 12.288 MHz	1	2.5	5	2.5	5	30	40	10	10
						41	50	10	10
						51	65	10	01

8.4.2.7 Audio PCB Guidelines

This section describes the other audio interfaces of the OMAP5430 device implemented in the audio back-end module. For more information on the overall audio scheme and implementation proposals, see the OMAP543x TRM.

8.4.2.7.1 Audio—McPDM interface

McPDM is a proprietary interface based on multichannel pulse density modulation. This interface supports 5 downlink and 2 uplink channels, and operates up to 19.2 Mbps.

8.4.2.7.1.1 Audio—McPDM Pin Description

Table 8-44 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-44. Audio—McPDM Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
abe_clks	N30	IO SMART
abemcpdm_lb_clk	L29	
abemcpdm_frame	L30	
abemcpdm_dl_data	M30	
abemcpdm_ul_data	M29	

8.4.2.7.1.2 Audio—McPDM PCB Requirements

Table 8-45 describes the audio—McPDM PCB requirements.

Table 8-45. Audio—McPDM PCB Requirements and IO Programming

McPDM APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
up to 19.2 Mbps McPDM	7	10	1	10	30	40	01	00
					41	50	01	00
					51	65	01	00

8.4.2.7.2 Audio—DMIC Interface

DMIC interface operates at 3.84 MHz with external digital microphones.

8.4.2.7.2.1 Audio—DMIC Pin Description

Table 8-46 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-46. Audio—DMIC Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
abedmic_clk1	P29	IO SMART
abedmic_clk2	P30	
abedmic_clk3	N29	
abedmic_din1	R30	
abedmic_din2	P32	
abedmic_din3	P31	

8.4.2.7.2.2 Audio—DMIC PCB Requirements

Table 8-47 describes the audio—DMIC PCB requirements.

Table 8-47. Audio—DMIC PCB Requirements and IO Programming

DMIC APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
3.84-MHz DMIC	7	10		25	30	40	00	00
					41	50	00	00
					51	65	00	00

Figure 8-23 describes a DMIC implementation proposal.

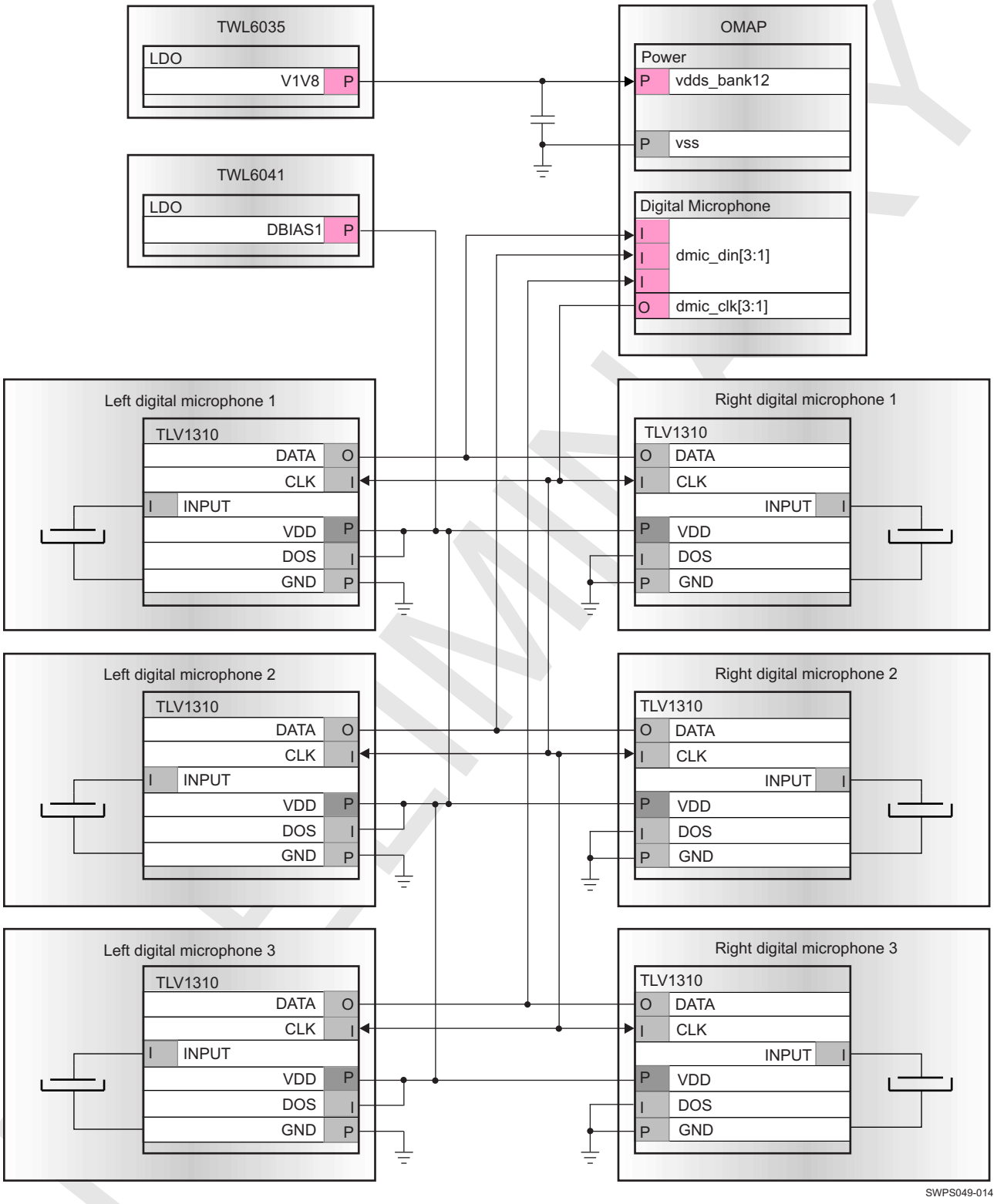

Figure 8-23. DMIC Implementation Proposal

(1) It is not recommended to use different PCB guideline clock outputs rather than sharing one as described in the above implementation.

In such case, each pair (pair [3:1]) of digital microphones can be connected to a dedicated data and clock signals (dmic_din[3:1], dmic_clk[3:1]). This way each microphone is turned on or off independently from the others.

8.4.2.7.3 Audio—McASP Interface

8.4.2.7.3.1 Audio—McASP Pin Description

Table 8-48 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-48. Audio—McASP Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
abemcasp_aclkx	N29	IO SMART
abemcasp_ahclkx	M32	
abemcasp_amutein	P30	
abemcasp_amuteout	N32	
abemcasp_axr	N31, N30, P32	
abemcasp_axr1	L30	
abemcasp_axr2	M30	
abemcasp_axr3	M29	
abemcasp_afsx	M31	

8.4.2.7.3.2 Audio—McASP PCB Requirements

Table 8-49 describes the audio—McASP PCB requirements.

Table 8-49. Audio—McASP PCB Requirements and IO Programming

McASP APPLICATION	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
	MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
McASP S/PDIF mode 24.576 Mbits/s	5	10	10	30	45	85(1)	01	00

(1) PCB impedance is extended to 85 Ω to support 75-Ω coaxial cable as defined in the S/PDIF standard. For long coaxial cable (up to 10 m), a redriver has to be implemented on the PCB, close to the coaxial cable connector.

8.4.2.8 Display Parallel Interface PCB Guidelines

This section addresses the parallel display interface.

8.4.2.8.1 Display Parallel Interface (DPI) Interface

The OMAP5430 processor provides a 24-bit parallel display subsystem (DSS) interface running up to 170 MHz.

8.4.2.8.1.1 Display Parallel Pin Description

Table 8-50 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-50. Display Parallel Interface (DPI) Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME	SIGNAL NAME	BOTTOM BALL	IO SET NAME
dispc_pclk	AK9	IO SMART	dispc_data10	AL5	IO SMART
dispc_vsync	AK8		dispc_data11	AL6	
dispc_hsync	AK6		dispc_data12	AJ8	
dispc_de	AM5		dispc_data13	AM9	
dispc_fid	AK20		dispc_data14	AL9	
dispc_data0	AM6		dispc_data15	AJ9	
dispc_data1	AL7		dispc_data16	AJ7	
dispc_data2	AJ6		dispc_data17	AK7	
dispc_data3	AM7		dispc_data18	AJ10	
dispc_data4	AM8		dispc_data19	AK10	
dispc_data5	AL8		dispc_data20	AJ11	
dispc_data6	AM10		dispc_data21	AK11	
dispc_data7	AL10		dispc_data22	AJ12	
dispc_data8	AK5		dispc_data23	AK12	
dispc_data9	AJ5		-	-	-

8.4.2.8.1.2 Display Parallel Interface (DPI) PCB Requirements

Table 8-51 describes the display parallel interface PCB requirements.

Table 8-51. Display Parallel Interface (DPI) PCB Requirements and IO Programming

DPI APPLICATION	NUMBER OF PERIPHERALS	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
DPI—24-bit display extension at 170 MHz (bridge to display port or DSI)	1	2.5	5	1	5	30	40	10	11
						41	50	10	10
						51	60	10	01

8.4.2.8.2 Remote Frame Buffer Interface (RFBI) Interface

The OMAP5430 processor provides a 16-bit RFBI running up to 30 Mbps.

8.4.2.8.2.1 Remote Frame Buffer Interface Pin Description

Table 8-52 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-52. Remote Frame Buffer Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME	SIGNAL NAME	BOTTOM BALL	IO SET NAME
rfbi_we	AK8	IO SMART	rfbi_data5	AL8	IO SMART
rfbi_re	AK9		rfbi_data6	AM10	
rfbi_te_vsync0	AJ7		rfbi_data7	AL10	
rfbi_hsync0	AK7		rfbi_data8	AK5	
rfbi_a0	AM5		rfbi_data9	AJ5	
rfbi_cs0	AK6		rfbi_data10	AL5	
rfbi_data0	AM6		rfbi_data11	AL6	
rfbi_data1	AL7		rfbi_data12	AJ8	
rfbi_data2	AJ6		rfbi_data13	AM9	
rfbi_data3	AM7		rfbi_data14	AL9	
rfbi_data4	AM8		rfbi_data15	AJ9	

8.4.2.8.2.2 Remote Frame Buffer Interface PCB Requirements

Table 8-53 describes the remote frame buffer interface PCB requirements.

Table 8-53. Remote Frame Buffer Interface PCB Requirements and IO Programming

RFBI APPLICATION	NUMBER OF PERIPHERALS	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
RFBI 16 bits at 30 Mbps (Pico DLP)	1	2.5	5	1	10	30	65	10	01

8.4.2.9 I^2C Interface PCB Guidelines

The OMAP5430 processor provides five I^2C interfaces. The I^2C interface supports the high-speed mode at 3.8 MHz and fast mode at 400 kHz.

It additionally provides a fifth I^2C interface (sr_pmic_scl and sr_pmic_sda) that is dedicated to controlling the SmartReflex circuitry within the power IC companion chip.

8.4.2.9.1 I^2C Interface Pin Description

Table 8-54 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-54. I²C Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
i2c1_pmic_scl	K29	IO I²C
i2c1_pmic_sda	H30	
i2c2_scl	AF30	
i2c2_sda	AF29	
i2c3_scl	AB3	
i2c3_sda	AB2	
i2c4_scl	AK22	
i2c4_sda	AJ20	
i2c5_scl	AL32	
i2c5_sda	AL31	
sr_pmic_scl	H29	
sr_pmic_sda	J29	

8.4.2.9.2 I²C Interface PCB Requirements

I²C rise time is specified for loads up to 80 pF in high-speed mode and 150 pF in fast mode.

LB[1:0] register can select the appropriate pullup resistor for given load range.

Table 8-55 describes the I²C interface PCB requirements.

Table 8-55. I²C Pulls and Load Description

PARAMETER				MIN	NOM	MAX	UNIT
RINPU	Internal pullup resistance for a given load range	LB[1:0] = 00	High-speed mode		1.8 (for a load in the range of 5 pF to 12 pF)		kΩ
			Fast mode		4.0 (for a load in the range of 5 pF to 15 pF)		
		LB[1:0] = 01	High-speed mode		1.0 (for a load in the range of 12 pF to 25 pF)		
			Fast mode		2.1 (for a load in the range of 15 pF to 50 pF)		
		LB[1:0] = 10	High-speed mode		0.525 (for a load in the range of 25 pF to 50 pF)		
			Fast mode		0.840 (for a load in the range of 50 pF to 150 pF)		
		LB[1:0] = 11	High-speed mode		0.300 (for a load in the range of 50 pF to 80 pF)		
			Fast mode		NA		

8.4.2.10 UART Interface PCB Guidelines

The OMAP5430 processor provides six UART interfaces.

8.4.2.10.1 UART Interface Pin Description

Table 8-56 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-56. UART Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
uart1_cts	E9	IO SMART
uart1_rts	E10	
uart1_rx	D9	
uart1_tx	D10	
uart2_cts	B5	
uart2_rts	C5	
uart2_rx	C6	
uart2_tx	B6	
uart3_cts_rctx	AJ28	
uart3_rts_irsd	AK28	
uart3_rx_irrx (multiplexing mode 1)	AM28	
uart3_rx_irrx (multiplexing mode 2)	AM20	USB2 PHY IO SET
uart3_tx_irtx (multiplexing mode 1)	AL28	IO SMART
uart3_tx_irtx (multiplexing mode 2)	AL20	USB2 PHY IO SET
uart5_cts	AE30	IO SMART
uart5_rts	AD29	
uart5_rx	AD30	
uart5_tx	AE29	
uart6_cts	AK26	
uart6_rts	AK27	
uart6_rx	AJ26	
uart6_tx	AJ27	

8.4.2.10.2 UART Interface PCB Requirements

The PCB requirements that must be met for the routing of the UART signals are:

- Far-end load is less than 5 pF
- Maximum trace length = 10 cm
- The trace impedance must be between 30 Ω and 65 Ω
- Output buffer settings:
  - SR[1:0] = 00
  - DS[1:0] = 01

8.4.2.11 PWM Timer Interface PCB Guidelines

OMAP5430 processor provides six PWM outputs. These outputs can have their duty cycle controlled by software to provide controls such as display backlight control or keypad backlight control.

8.4.2.11.1 PWM Timer Interface Pin Description

Table 8-57 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-57. PWM Timer Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME
timer5_pwm_evt	AF2	IO SMART
timer6_pwm_evt	AE3	
timer8_pwm_evt (multiplexing mode 1)	AE2	
timer8_pwm_evt (multiplexing mode 2)	AC2	
timer9_pwm_evt	AC29	
timer10_pwm_evt	V30	
timer11_pwm_evt	AF3	

8.4.2.11.2 PWM Timer Interface PCB Requirements

The PCB requirements that must be met for the routing of the PWM timer signals are:

- The trace impedance must be between 35 Ω and 65 Ω
- Maximum trace length = 10 cm

8.4.2.12 KeyPad Interface PCB Guidelines

The OMAP5430 processor provides a 9x9 keypad controller multiplexed twice in the OMAP5430 device.

8.4.2.12.1 KeyPad Interface Pin Description

Table 8-58 provides for each signal the corresponding bottom ball and the IO set name.

Table 8-58. KeyPad Interface Signals

SIGNAL NAME	BOTTOM BALL	IO SET NAME	SIGNAL NAME	BOTTOM BALL	IO SET NAME
kbd_row0	B21	IO SMART	kbd_row0	AK11	IO SMART
kbd_row1	C21		kbd_row1	AJ12	
kbd_row2	B20		kbd_row2	AK12	
kbd_row3	C20		kbd_row3	AJ5	
kbd_row4	B19		kbd_row4	AM5	
kbd_row5	C19		kbd_row5	AJ7	
kbd_row6	B18		kbd_row6	AJ8	
kbd_row7	C18		kbd_row7	AL6	
kbd_row8	C22		kbd_row8	AL5	
kbd_col0	E26		kbd_col0	AJ10	
kbd_col1	D26		kbd_col1	AK10	
kbd_col2	E25		kbd_col2	AJ11	
kbd_col3	D25		kbd_col3	AK5	
kbd_col4	E24		kbd_col4	AK9	
kbd_col5	D24		kbd_col5	AK7	
kbd_col6	E23		kbd_col6	AJ9	
kbd_col7	D23		kbd_col7	AL9	
kbd_col8	D22		kbd_col8	AM9	

8.4.2.12.2 KeyPad Interface PCB Requirements

The PCB requirements that must be met for the routing of the KeyPad row and column signals are:

- The trace impedance must be between 30 Ω and 65 Ω
- Maximum trace length = 20 cm

8.4.2.13 Debug Interface PCB Guidelines

8.4.2.13.1 MPU Traces (PTM) and System Traces (STM) Through DRM Interface

MPU and system traces can be exported to an external trace receiver through the DRM interface.

8.4.2.13.1.1 DRM Interface Pin Description

Table 8-59 provides for each signal the corresponding bottom balls and the IO set name.

Table 8-59. DRM Interface Signals

SIGNAL NAME	BOTTOM BALLS	IO SET NAME	SIGNAL NAME	BOTTOM BALLS	IO SET NAME
drm_emu0	B30(1)	IO SMART	drm_emu10	AM10	IO SMART
drm_emu1	B31(1)		drm_emu11	AL10	
drm_emu2	AK8 / J31(1)		drm_emu12	AK5	
drm_emu3	AK6 / K31(1)		drm_emu13	AJ5	
drm_emu4	AM6 / L32(1)		drm_emu14	AL5	
drm_emu5	AL7 / K32(1)		drm_emu15	AL6 / J31(1)	
drm_emu6	AJ6 / J32(1)		drm_emu16	AJ8 / K31(1)	
drm_emu7	AM7		drm_emu17	AM9 / L32(1)	
drm_emu8	AM8		drm_emu18	AL9 / K32(1)	
drm_emu9	AL8		drm_emu19	AJ9 / J32(1)	

(1) These balls correspond to the DRM signals belonging to the wake-up domain.

8.4.2.13.1.2 DRM Interface PCB Requirements

Table 8-60 describes the DRM interface PCB requirements.

Table 8-60. DRM Interface PCB Requirements and IO Programming

DRM APPLICATION	RE-DRIVER AT MIPI60 JTAG CONNECTOR LEVEL(3)	FAR-END LOAD (pF)		TRACE LENGTH (cm)		CHARACTERISTIC IMPEDANCE (Ω)		IO REGISTER CONFIGURATION	
		MIN	MAX	MIN	MAX	MIN	MAX	SLEW RATE REGISTER SC[1:0]	IMPEDANCE REGISTER DS[1:0]
PTM (ARM trace over TPIU)—180-MHz DDR, 16-data-bit mode(1), with Lauterbach LA-7992	Yes	5(4)	10(3)	10	20	40	51(5)	11	10
PTM (ARM trace over TPIU)—180-MHz DDR, 16-data-bit mode(1), with XDS60v2_pro	No	2	5	10	20	40	51(5)	11	10
STMv2 (System Trace)—180-MHz DDR mode, 4-data-bit mode(2), with Lauterbach LA-7992 or XDS560v2	Yes	5(4)	10(3)	10	20	40	51(5)	11	10
STMv1 (System Trace)—80-MHz DDR mode, 4-data-bit mode(2), with XDS560v2	Yes	5(4)	10(3)	10	20	40	51(5)	11	10

(1) Only the 16-data-bit mode is supported (data = drm_emu[4:19], ctrl = drm_emu3, and clock = drm_emu2). The 18-data-bit mode muxing signals from core domain (drm_emu[2:19) and wake-up domain (drm_emu[0:1]) are not supported at this frequency.

(2) Only 4-data-bit mode using the pin signals located in the wake-up domain (data = drm_emu[0;1;4;5], ctrl = drm_emu3, and clock = drm_emu2) is supported. Muxing of wake-up domain emu[0:1] with core domain RFBI signals is not supported.

(3) Level shifter can be implemented on the OMAP5430 board close to the MIPI60 JTAG connector or plugged in the MIPI 60JTAG connector.

(4) Far-end load values correspond to the input capacitance of the re-driver requested to support the application.

(5) For PCB trace lengths shorter than the maximum recommendation, the maximum trace impedance value can be extended to 55 Ω. In

that case, a fine-tuned electrical study has to be performed to limit the signal integrity issue.

8.4.2.13.2 System (STM) and JTAG Traces Through SD Card Interface

System trace can be exported to the external trace receiver through the SD card interface (SD card slot).

8.4.2.13.2.1 Narrow Interface for Debug and Test (NIDnT) Interface Pin Description

Table 8-61 provides for each signal the corresponding bottom balls and the IO set name.

Table 8-61. STM NIDnT Interface Signals

SIGNAL NAME	BOTTOM BALLS	IO SET NAME
n_clk	E3 (sdcard_clk)	SDIO card (1.8-V, 3.0-V)
n_d0	G3 (sdcard_data0)	
n_d1	G2 (sdcard_data1)	
n_d2	F2 (sdcard_data2)	
	E2 (sdcard_cmd)	
n_d3	F3 (sdcard_data3)	

8.4.2.13.2.2 NIDnT Interface PCB Requirements

The NIDnT PCB requirements and IO settings are those described for the SD card interface, see Section 8.4.2.3.1, *OMAP5430 Single-Ended Interfaces—SD Card PCB Guidelines*.

8.5 Differential Interfaces

8.5.1 General Routing Guidelines

The following general routing guidelines describe the routing guidelines for differential lanes and differential signals.

Specific guidelines by the OMAP5 interface are outlined in that chapter.

- As much as possible, no other high frequency signals must be routed in close proximity to the differential pair.
- Differential traces must be routed on the same layer. For each signal of the pair, the trace width and spacing must be chosen to yield the differential impedance value recommended.
- Minimize external components on differential lanes (like external ESD, probe points).
- Through-hole pins are not recommended.
- Differential lanes must not cross image planes (ground planes).
- No sharp bend on differential lanes.
- Number of vias on the differential pairs must be minimized, and identical on each line of the differential pair. In case of multiple differential lanes in the same interface, all lines must have the same number of vias.
- Shielded routing is to be promoted as much as possible (for instance, signals must be routed on internal layers that are inside power and/or ground planes).

8.5.2 MIPI D-PHY PCB Guidelines

The MIPI D-PHY signals include the CSIPORTA, CSIPORTB, CSIPORTC, DSIPORTA, and DSIPORTC interfaces to or from the OMAP5430 device.

For more information regarding the MIPI-PHY signals and corresponding balls, see Section 2.4, *Signal Descriptions*.

For more information, you can also see the MIPI D-PHY specification v1-01-00_r0-03 (specifically the Interconnect and Lane Configuration and Annex B Interconnect Design Guidelines chapters).

In the next section, the PCB guidelines of the following five differential interfaces are presented:

- CSIPORTA, CSIPORTB, and CSIPORTC MIPI CSI-2 at 1.5 Gbps
- DSIPORTA and DSIPORTC MIPI DSI-1 at 1.255 Gbps

Table 8-62 lists the MIPI D-PHY interface signals in the OMAP5430 device.

Table 8-62. MIPI D-PHY Interface Signals in OMAP5

SIGNAL NAME	BOTTOM BALL	SIGNAL NAME	BOTTOM BALL
csiporta_lane0x	R2	csiporta_lane0y	R3
csiporta_lane1x	P2	csiporta_lane1y	P3
csiporta_lane2x	N2	csiporta_lane2y	N3
csiporta_lane3x	M2	csiporta_lane3y	M3
csiporta_lane4x	L2	csiporta_lane4y	L3
csiportb_lane0x	V3	csiportb_lane0y	V2
csiportb_lane1x	W3	csiportb_lane1y	W2
csiportb_lane2x	Y3	csiportb_lane2y	Y2
csiportc_lane0x	K2	csiportc_lane0y	K3
csiportc_lane1x	J2	csiportc_lane1y	J3
dsiporta_lane0x	Y32	dsiporta_lane0y	Y31
dsiporta_lane1x	W32	dsiporta_lane1y	W31
dsiporta_lane2x	V32	dsiporta_lane2y	V31

Table 8-62. MIPI D-PHY Interface Signals in OMAP5 (continued)

SIGNAL NAME	BOTTOM BALL	SIGNAL NAME	BOTTOM BALL
dsiporta_lane3x	T32	dsiporta_lane3y	T31
dsiporta_lane4x	R32	dsiporta_lane4y	R31
dsiportc_lane0x	AF32	dsiportc_lane0y	AF31
dsiportc_lane1x	AE32	dsiportc_lane1y	AE31
dsiportc_lane2x	AD32	dsiportc_lane2y	AD31
dsiportc_lane3x	AC32	dsiportc_lane3y	AC31
dsiportc_lane4x	AB32	dsiportc_lane4y	AB31

8.5.2.1 CSIPORTA, CSIPORTB, and CSIPORTC MIPI CSI-2 (1.5 Gbps), and DSIPORTA and DSIPORTC MIPI DSI-1 (1.255 Gbps)

8.5.2.1.1 General Guidelines

The general guidelines for the PCB differential lines are:

- Differential trace impedance Z_0 = 100 Ω (minimum = 85 Ω, maximum = 115 Ω)
- Total conductor length from the OMAP5 package pins to the peripheral device package pins is 25 to 30 cm with common FR4 PCB and flex materials.

NOTE

Longer interconnect length can be supported at the expense of detailed simulations of the complete link including driver and receiver models.

The general rule of thumb for the space S = 2 × W is not designated (see Figure 8-21, *Guard Illustration*). It is because although the S = 2 × W rule is a good rule of thumb, it is not always the best solution. The electrical performance will be checked with the frequency-domain specification. Even though the designer does not follow the S = 2 × W rule, the differential lines are ok if the lines satisfy the frequency-domain specification.

Because the MIPI signals are used for low-power, single-ended signaling in addition to their high-speed differential implementation, the pairs must be loosely coupled.

8.5.2.1.2 Length Mismatch Guidelines

8.5.2.1.2.1 CSIPORTA, CSIPORTB, and CSIPORTC MIPI CSI-2 (1.5 Gbps)

The guidelines of the length mismatch for CSI-2 are presented in Table 8-63.

Table 8-63. Length Mismatch Guidelines for CSI-2 (1.5 Gbps)

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	1500	Mbps
UI (bit time)	667	ps
Intralane skew	Have to satisfy mode-conversion S parameters(1)	
Interlane skew (UI / 50)	13.34	ps

(1) sdc12, scd21, scd12, sdc21, scd11, sdc11, scd22, and sdc22

8.5.2.1.2.2 DSIPORTA and DSIPORTC MIPI DSI-1 (1.255 Gbps)

The guidelines of the length mismatch for DSI-1 are presented in Table 8-64.

Table 8-64. Length Mismatch Guidelines for DSI-1 (1.255 Gbps)

PARAMETER	TYPICAL VALUE	UNIT
Operating speed	1255.5	Mbps
UI (bit time)	797	ps
Intralane skew (UI / 150)	5.31	ps
Interlane skew (UI / 50)	15.93	ps

8.5.2.1.3 Frequency-domain Specification Guidelines

After the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) or equivalent, and compared to the frequency-domain specification as defined in the section 7 of the MIPI Alliance Specification for D-PHY Version v1-01-00_r0-03.

If the PCB lines satisfy the frequency-domain specification, the design is finished. Otherwise, the design needs to be improved.

8.5.3 USB PHY PCB Guidelines

8.5.3.1 USB High-Speed PHY Interface (480 Mbps)

The USBD0_HS PHY signals are the positive and negative (DP and DM) signals from the USB transceiver contained within the OMAP5430 device.

Table 8-65 lists the USB high-speed interface signals.

Table 8-65. USB High-Speed PHY Interface Signals

SIGNAL NAME	BOTTOM BALL
usbd0_hs_dm	AL20
usbd0_hs_dp	AM20

8.5.3.1.1 General Guidelines and Length Mismatch Guidelines

8.5.3.1.1.1 USB High-Speed (HS) PCB Requirements

- DP and DM lines must have Z_0 = 90 Ω differential trace impedance (minimum = 80 Ω, maximum = 100 Ω).
- Intralane delay mismatch between DP and DM is less than 5 ps.
- DP and DM trace lengths between the OMAP5 package pins and the USB HS connector < 30 cm (including ESD and CMF)
- Distance between the common mode choke (CMF) and the ESD protection device (TVS) must be as short as possible.
- Distance between the ESD protection device (TVS) and the connector must be as short as possible.
- USB standard connector must be used (micro-AB or mini-AB).
- USB grounds must be shorted to the board ground plane with minimum routing (only a via must be connected to the ground plane to avoid loop creation and so to reduce EMI).

8.5.3.1.1.2 USB High-Speed (HS) Implementation Proposal

Figure 8-24 proposes an example of USB high-speed (HS) PHY implementation with a PMIC and a TPD4S012 component.

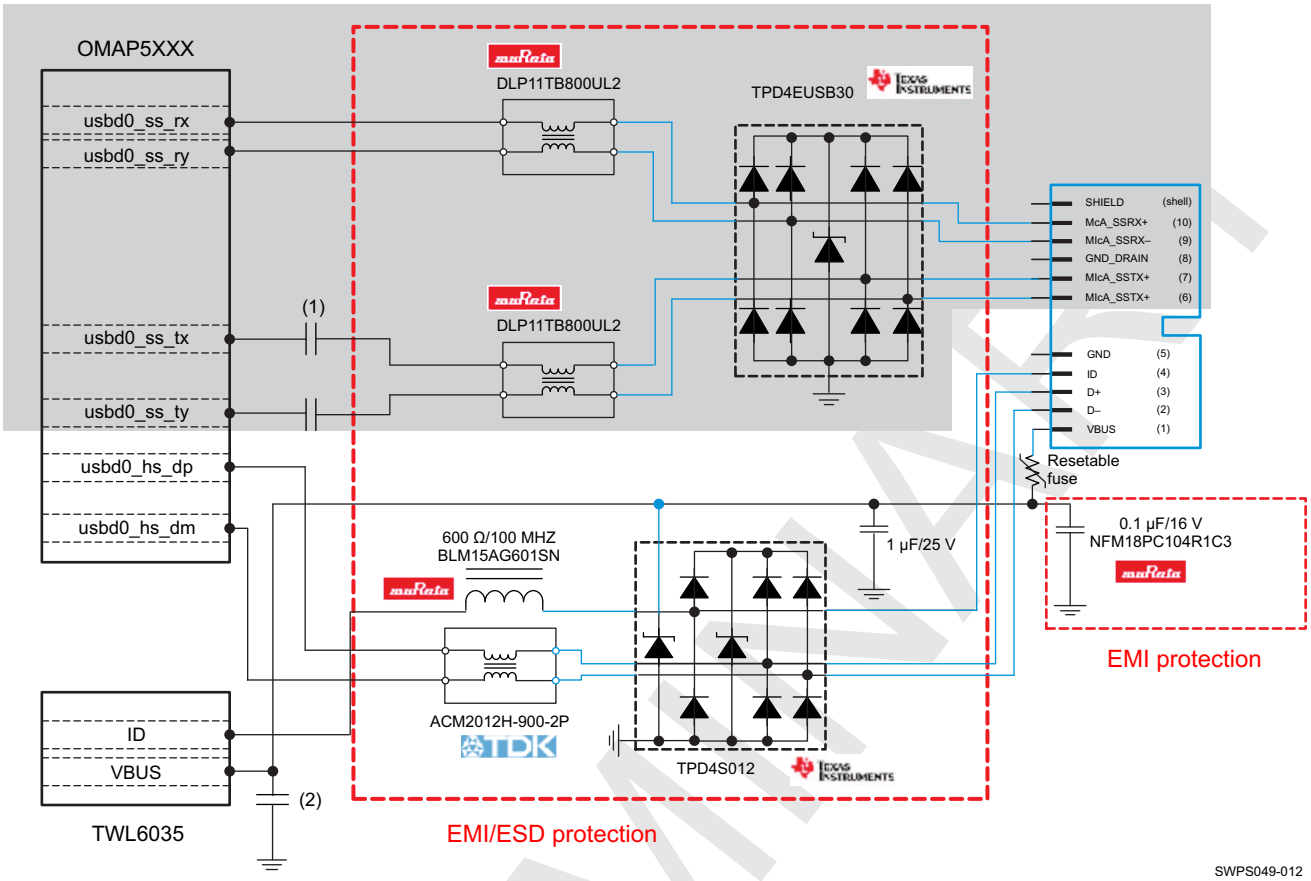

Figure 8-24. USB HS Implementation Proposal (ESD/EMI Protection)

(1) For capacitor value, please refer to the USB3 standard specification.

(2) For capacitor value, please refer to the TWL6035 TRM.

NOTE

System level ESD results (following IEC 61000-4-2 standard) are dependent on the components being connected to the product.

Part numbers that are different from the reference board specification described in Table 8-66, *USB HS PHY Component References*, are not assured to meet system level ESD requirements.

For more information on USB HS PHY ESD recommendation see Section 8.5.3.1.1.3, *USB High-Speed (HS) ESD Implementation.*

Table 8-66. USB HS PHY Component References

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
USB HS PHY	TVS	TI	TPD4S012DRY
	CMF	TDK	ACM2012H-900-2P
	CFB	Murata	[600R / 100M / 0402] BLM15AG601SN1
	C	Murata	[1 µF / 25 V / 0603] GRM188R71E105KA12D
	EMICAP	Murata	[0.1 µF / 16 V] NFM18PC104R1C3

8.5.3.1.1.3 USB High-Speed (HS) ESD Implementation

NOTE

For more information on system ESD or EMI/EMC, see Section 8.3.5, *System ESD Generic Guidelines* and Section 8.3.6, *EMI / EMC Issues Prevention*.

ESD: USB HS has the following pins to protect: DP and DM attached to the OMAP5430 device, and ID and VBUS pins attached to the PMIC device.

For DP and DM pins:

- ESD protection device must be preferably an array with a low capacitance (= 1.0 pF typical) and a low turn-on resistance (R_{dyn} = 1.2 Ω) while the VBUS pin is designed to tolerate 20 V.
- Common mode choke filter (CMF) must be placed between the ESD protection and the OMAP5430 device to minimize electromagnetic interference (EMI).
- DC series resistance of the CMF needs to be 3 Ω maximum.

For VBUS and ID pins:

- For the VBUS pin, a broadband decoupling capacitor reduces noise in the VBUS power line. In addition, a large decoupling capacitor will absorb the ESD pulse energy.
- For the ID pin, a chip ferrite bead placed between the ESD protection and the PMIC is recommended.

NOTE

System level ESD results (following IEC 61000-4-2 standard) are dependent on the components being connected to the product.

Part numbers that are different from the reference board specification described in Table 8-66, *USB HS PHY Component References*, are not assured to meet system level ESD requirements.

8.5.3.1.2 Interconnect Simulation

After the PCB design is finished, the S-parameters of the PCB differential lines will be extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) and run simulations to check that the link meets the USB HS performances at the USB2 conformance test points:

- TP2 when simulating the USB2 driver
- TP1 when simulating the USB2 receiver

If the performances are met, the design is finished. Otherwise, the design needs to be improved.

8.5.3.2 USB Super-Speed PHY Interface (5 Gbps)

Table 8-67 lists the USB super-speed interface signals.

Table 8-67. USB Super-Speed PHY Interface Signals

SIGNAL NAME	BOTTOM BALL
usbd0_ss_rx	AM22
usbd0_ss_ry	AL22
usbd0_ss_tx	AM21
usbd0_ss_ty	AL21

8.5.3.2.1 General Guidelines and Length Mismatch Guidelines

8.5.3.2.1.1 USB Super-Speed (SS) PCB Requirements

- Differential trace impedance Z_0 = 90 Ω (minimum = 80 Ω, maximum = 100 Ω).

- The intralane skew requirement is 5 ps maximum.
- Total conductor length from the OMAP5 package pins to the USB-SS connector < 30 cm (including ESD and CMF).
- Distance between the common mode choke (CMF) and the ESD protection device (TVS) must be as short as possible.
- The distance between the ESD device (TVS) and the USB connector must be as short as possible.
- USB standard connector must be used (micro-AB or mini-AB).
- USB grounds must be shorted to the board ground plane with minimum routing (only via must be used to connect to ground plane to avoid loop creation and so to reduce EMI).

8.5.3.2.1.2 USB Super-Speed (SS) Implemenation Proposal

Figure 8-25 proposes an example of USB super-speed (SS) PHY implementation.

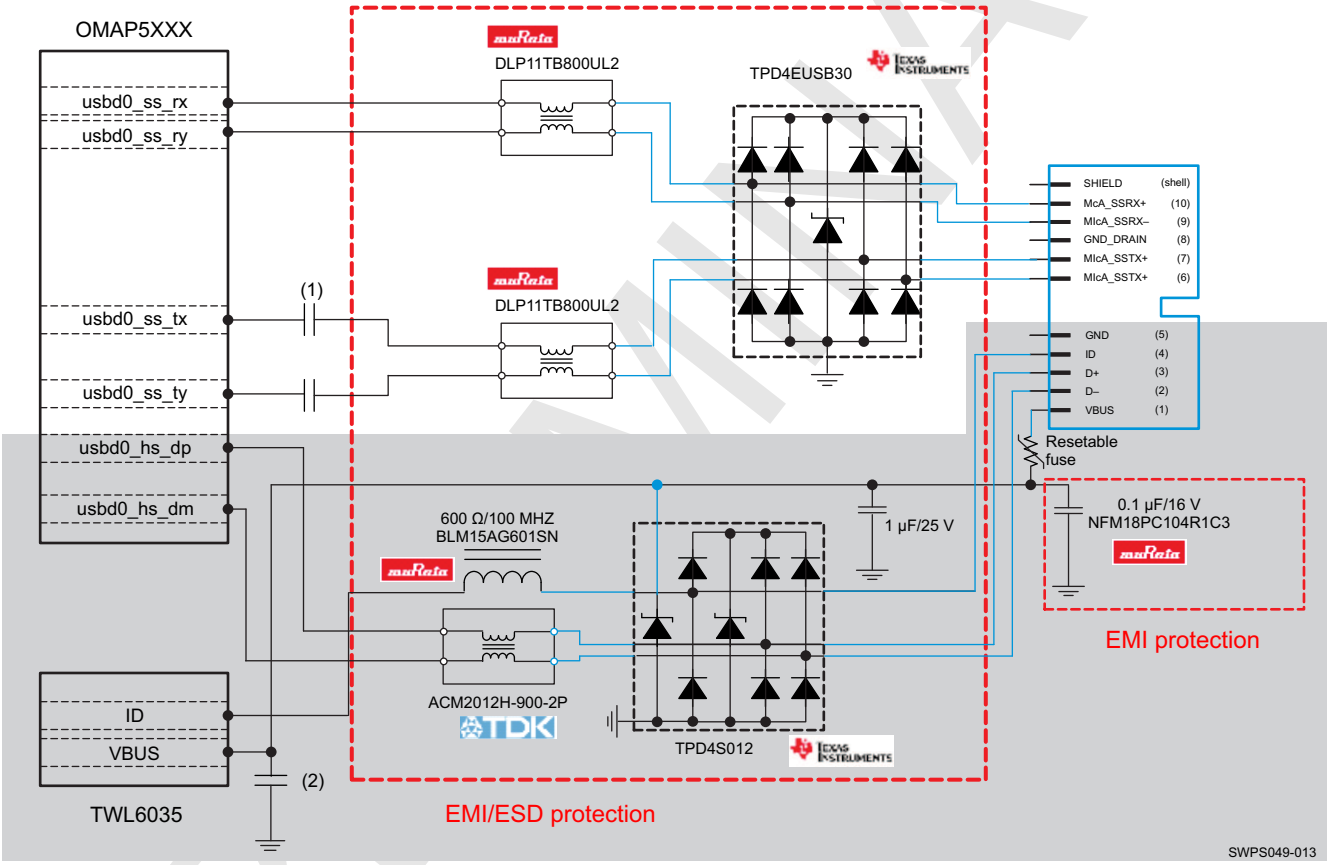

Figure 8-25. USB SS Implementation Proposal (ESD/EMI Protection)

(1) For capacitor value, please refer to the USB3 standard specification.

(2) For capacitor value, please refer to the TWL6035 TRM.

Table 8-68. USB SS DRD PHY Component References

INTERFACE	DEVICE	SUPPLIER	PART NUMBER
USB SS DRD PHY	TVS	TI	TPD4EUSB30
	CMF	Murata	DLP11TB800UL2

8.5.3.2.1.3 USB Super-Speed (SS) ESD Implementation

NOTE

For more information on system ESD or EMI/EMC, see Section 8.3.5, *System ESD Generic Guidelines*, and Section 8.3.6, *EMI / EMC Issues Prevention*.

ESD: USB SS has four additional pins to protect: SS_RX, SS_RY, SS_TX, and SS_TY.

- ESD protection device must have a low capacitance (= 0.8 pF typical) and a low turn-on resistance (R_{dyn} = 1.2 Ω) while the VBUS pin is designed to tolerate 20 V.
- Common mode choke filter (CMF) must be placed between the ESD protection and the OMAP5430 device to minimize electromagnetic interference (EMI).

NOTE

System level ESD results (following IEC 61000-4-2 standard) are dependent on the components being connected to the product.

Part numbers that are different from the reference board specification described in Table 8-68, *USB SS DRD PHY Component References*, are not assured to meet system level ESD requirements.

8.5.3.2.2 Interconnect Simulation

After the PCB design is finished, the S-parameters of the PCB differential lines are extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) and run simulations to check that the link meets the USB SS performances at the USB3 connector pins.

If the performances are met, the design is done. Otherwise, the design needs to be improved.

8.5.4 HDMI PCB Guidelines

NOTE

For more information on HDMI, please contact your TI representative.

NOTE

For more information on system ESD or EMI, see Section 8.3.5, *System ESD Generic Guidelines* and Section 8.3.6, *EMI/EMC Issues Prevention*.

8.5.5 SATA PHY PCB Guidelines

Table 8-69 lists the SATA PHY interface signals.

Table 8-69. SATA PHY Interface Signals

SIGNAL NAME	BOTTOM BALL
sata_rx	E7
sata_ry	D7
sata_tx	E6
sata_ty	D6

8.5.5.1 General Guidelines and Length Mismatch Guidelines

8.5.5.1.1 SATA PHY PCB Requirements

Due to the high speed of the SATA PHY signals (3 Gbps maximum), and with following assumptions for common mode interference (less than 400 mV) and with e_r = 4.0 material:

- Differential trace impedance Z_0 = 100 Ω (minimum = 85 Ω, maximum = 115 Ω).
- Total conductor length from the OMAP5 package pins to the iSSD (integrated solid-state drive) device package pins < 30 cm.
- The intralane skew requirement is 10 ps maximum.

8.5.5.2 Interconnect Simulation

After the PCB design is finished, the S-parameters of the PCB differential lines are extracted with a 3D Maxwell Equation Solver such as the high-frequency structure simulator (HFSS) and run simulations to check that the link meets the performances at the receiver pins. If the performances are met, the design is finished. Otherwise, the design needs to be improved.

8.6 External Capacitors

8.6.1 Voltage Decoupling Capacitors

NOTE

For power IC which can support more than 10 µF close to the OMAP5 device, a bulk capacitor of at least 22 µF is strongly recommended for vdd_mpu.

8.6.1.1 Core, MPU, MM, Audio Voltage Decoupling

8.6.1.1.1 Core, MPU, MM, Audio Voltage Decoupling Values

Here are some core, MPU, and MM (multimedia) voltage decoupling PCB recommendations.

PCB guidelines between the power IC (PMIC) balls and the OMAP5430 balls are:

- Maximum recommended inductance by power supply rail is less than 2 nH (VDD + VSS).
- Maximum recommended static IR drop by power supply rail is less than 1.5% (with rise on ground accounted for).
- For more information on maximum peak-peak noise on the supply, see Table 3-3, *Recommended Operating Conditions*.
- The main characteristics of the decoupling bypass capacitors are shown in Table 8-70:

Table 8-70. Main Characteristics of the Decoupling Bypass Capacitors(1)(2)

CAPACITOR	PACKAGE	VERSION	TOLERANCE	VOLTAGE	REFERENCE
22 µF	0603	X5R	±20%	6.3 V	GRM188R60J226MEA
10 µF	0402	X5R	±20%	6.3 V	GRM155R60J106ME44
2.2 µF	0402	X5R	±20%	6.3 V	GRM155R60J225ME95
1 µF	0201	X5R	±20%	6.3 V	GRM033R60J105MEA2
470 nF	0201	X5R	±20%	6.3 V	GRM033R60G474ME90
100 nF	0201	X5R	±20%	6.3 V	GRM033R60J104ME19
220 nF	0201	X5R	±20%	6.3 V	GRM033R60J224ME15

(1) Minimum value for each PCB capacitor: 100 nF.

(2) Among the different capacitors, 470 nF is recommended (not required) to filter at 5-MHz to 10-MHz frequency range.

Table 8-71. Core, MPU, MM, Audio Voltage Decoupling Characteristics(6)

PARAMETER	PDN IMPEDANCE CHARACTERISTICS(4)		PCB RES. BETWEEN SPMS And OMAP5430 (mΩ)(5)	MAXIMUM LOOP INDUCTANCE PER CAPACITOR (WITHOUT ESL)(2)	DECOUPLING CAPACITOR VALUES(3)						
	IMPEDANCE TARGET (mΩ)	FREQUENCY OF INTEREST (MHz)			100 nF	220 nF	470 nF	1 µF	2.2 µF	4.7 µF	22 µF
C_{vdd_core}	82	63	20	0.6	2	1	1	0	2	0	0
C_{vdd_mpu}	28	16	5	0.4	5	0	3	4	0	0	1
C_{vdd_mm}	41	30	10	0.5	2	1	1	0	2	0	1

(1) For more information on peak-to-peak noise values, see Table 3-3, *Recommended Operating Conditions*.

(2) ESL must be as low as possible and must not exceed 0.5 nH.

(3) To take into account the aging effects and voltage impact on capacitance, their values, as described in this table, are specified at ±50%.

(4) The PDN impedance characteristics are defined versus the device activity (that runs at different frequency) based on see Table 3-3, *Recommended Operating Conditions*.

(5) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the OMAP5 power balls.

(6) Assuming that the external SMPS (power IC) feedback sense is taken close to the OMAP5430 power balls.

8.6.1.1.2 Core, MPU, MM Voltage Decoupling PCB Examples

8.6.1.1.2.1 MPU Voltage Decoupling PCB Examples

Figure 8-26 and Figure 8-27 show an example of PCB layout of vdd_mpu with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-26 and Figure 8-27 describe a working board. They do not show an optimized board.

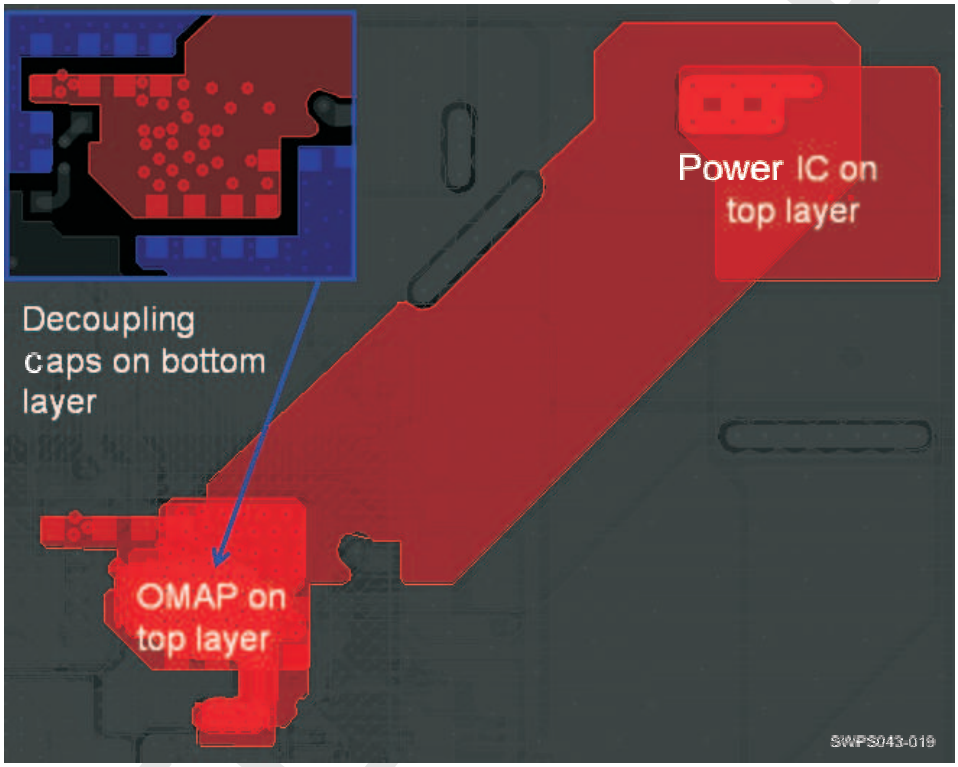

Figure 8-26. vdd_mpu PCB Requirements(1)

(1) Figure 8-26 shows an example of PCB layout of vdd_mpu that meets the IR drop requirements with 2.5-mΩ resistance and the capacitance-inductance loop with 0.4 nH.

Figure 8-27 describes the vdd_mpu PDN analysis versus frequency.

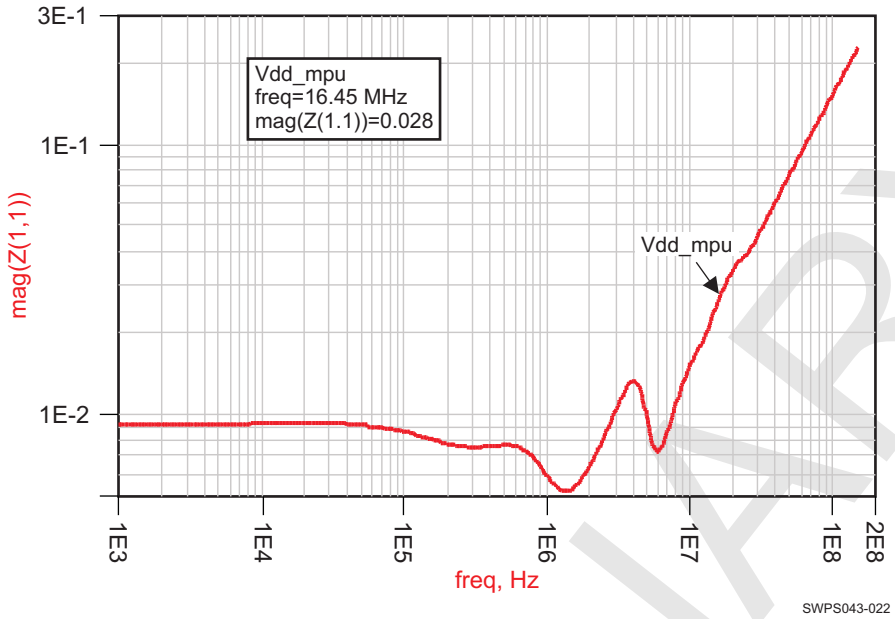

Figure 8-27. vdd_mpu PDN Analysis

8.6.1.1.2.2 MM Voltage Decoupling PCB Examples

Figure 8-28 and Figure 8-29 show an example of PCB layout of vdd_mm with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-28 and Figure 8-29 describe a working board. They do not show an optimized board.

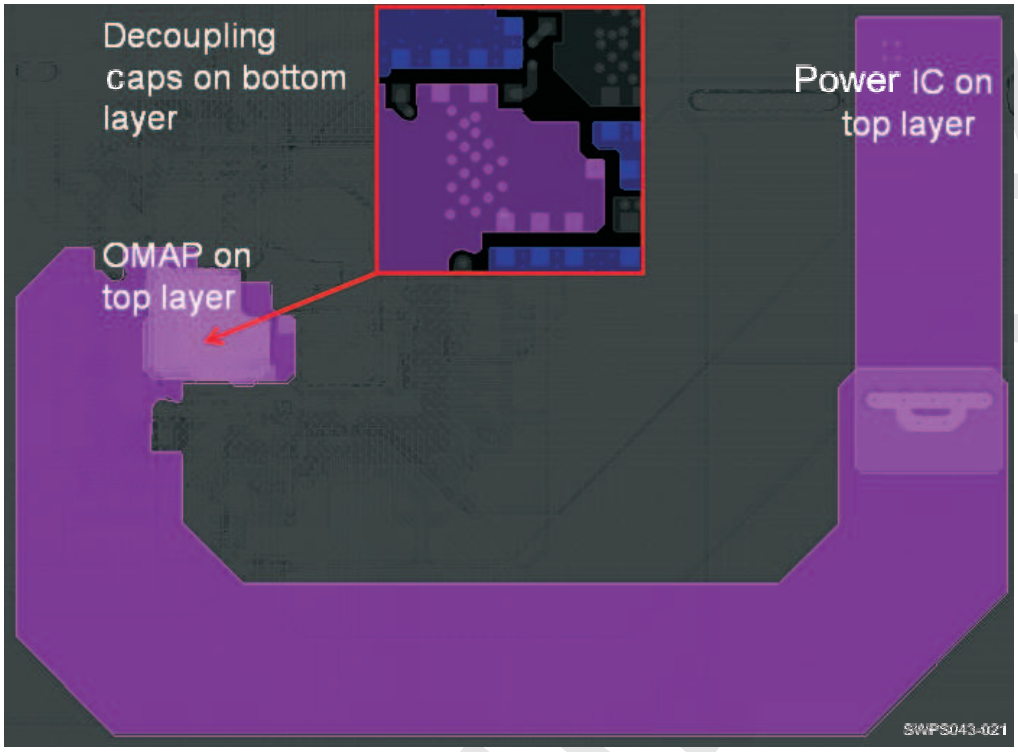

Figure 8-28. vdd_mm PCB Routing(1)

(1) Figure 8-28 shows an example of PCB layout of vdd_mm that meets the IR drop requirements with 12-mΩ resistance and the capacitance-inductance loop with 0.5 nH.

Figure 8-29 shows the vdd_mm PDN analysis versus frequency.

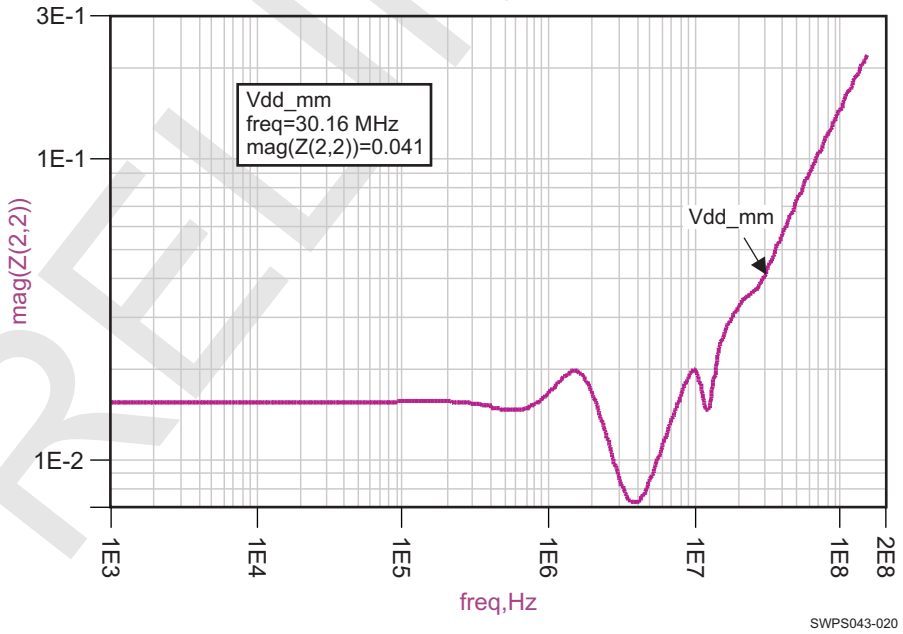

Figure 8-29. vdd_mm PDN Analysis

8.6.1.1.2.3 Core Voltage Decoupling PCB Examples

Figure 8-30 and Figure 8-31 show an example of PCB layout of vdd_core with the PMIC that meets the IR drop requirements and the PCB inductance loop.

NOTE

Figure 8-30 and Figure 8-31 describe a working board. They do not show an optimized board.

Figure 8-30. vdd_core PCB Routing(1)

(1) Figure 8-30 describes an example of vdd_core PCB layout that meets the IR drop requirements with 5-mΩ resistance and 0.6 nH of the capacitance-inductance loop.

Figure 8-31 shows the vdd_core PDN analysis versus frequency.

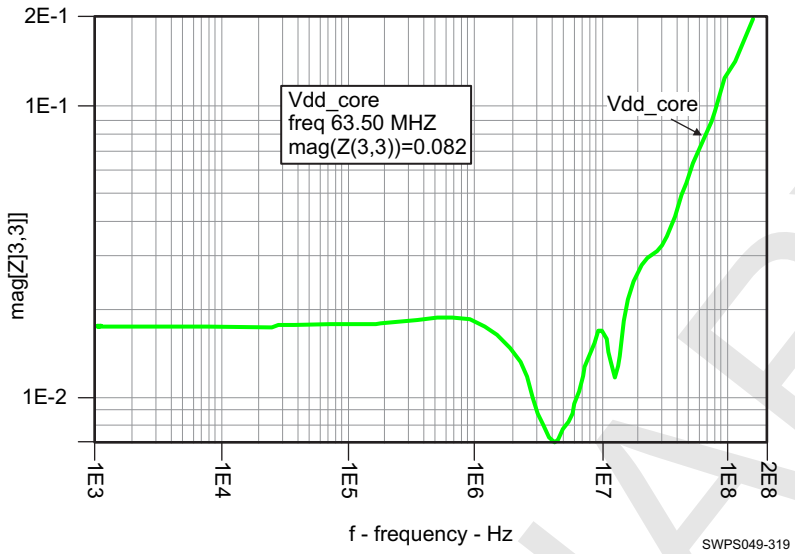

Figure 8-31. vdd_core PDN Analysis

8.6.1.2 IO and Analog Voltage Decoupling

PCB guidelines between the power IC (PMIC) balls and the OMAP5430 balls are:

- Maximum recommended static IR drop by power supply rail:
  - Less than 1% (included ground) of the supplied voltage for standard IOs
  - Less than 0.8% for analog IPs and PHYs.
- For more information on maximum peak-peak noise on the supply, see Table 3-3, *Recommended Operating Conditions*.
- Decoupling bypass capacitors main characteristics:
  - TCC size code:
    - 10 µF: 0603/X5R
    - 4.7 µF: 0603/X5R
    - 1 µF: 0402/X5R
    - 470 nF: 0402/X5R
    - 100 nF: 0201/X5R
  - Minimum value for each PCB capacitor: 100 nF
  - The capacitor value is defined at ±50% of the value to take in account the aging effects, and the voltage impact.
  - Maximum maximum ESR = 0.3 Ω at 1 GHz and maximum ESL = 0.45 nH.

8.6.1.2.1 VDDS-1.8-MAIN Power Domain

8.6.1.2.1.1 Power Distribution Example

Figure 8-32 describes an example of power distribution for the main vdds 1.8-V power supplies.

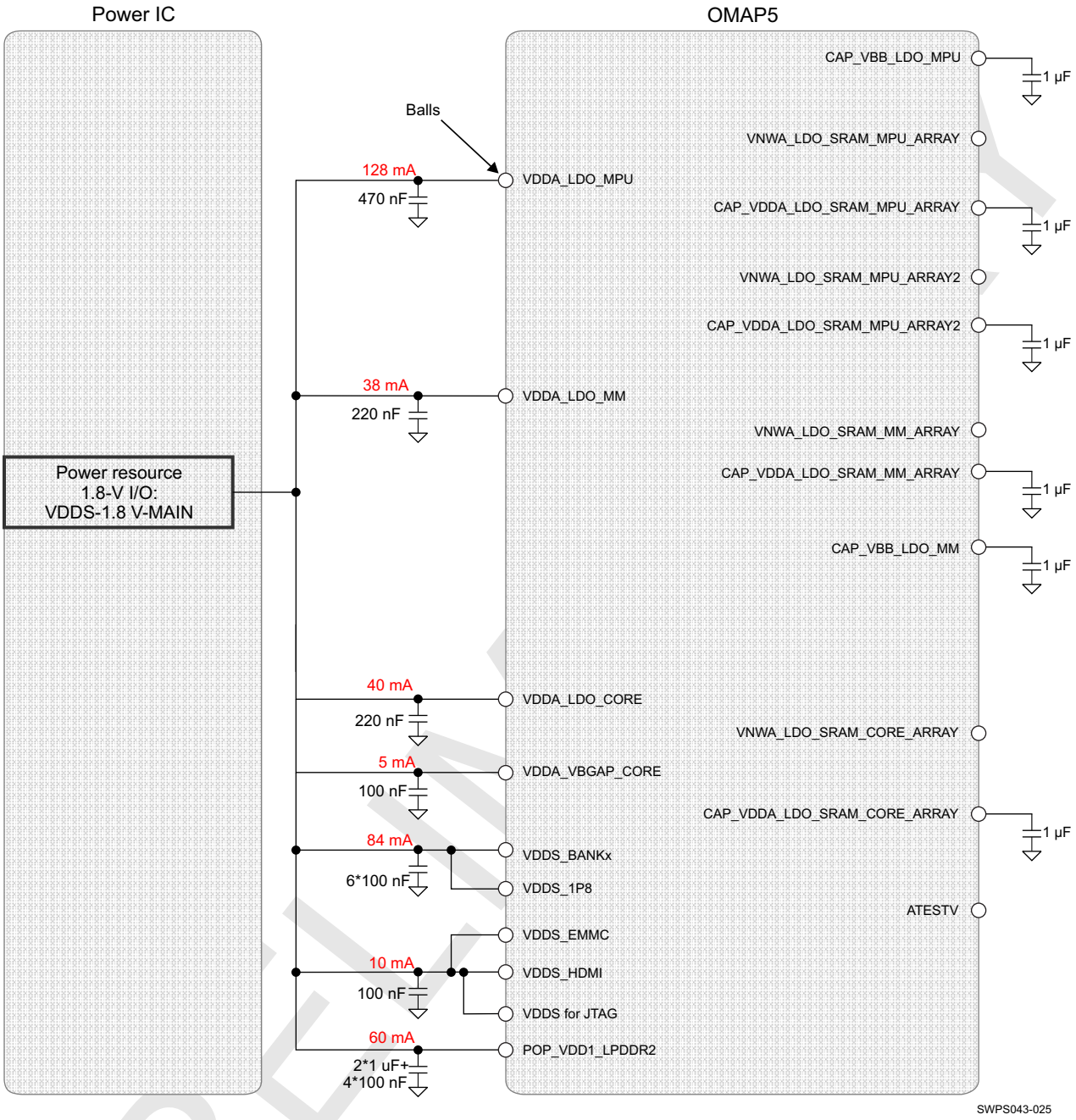

Figure 8-32. VDDS-1.8-MAIN Power Distribution

8.6.1.2.1.2 PCB Recommendation

- A power plan is recommended to meet the static drop requirement (1%) betwen the power IC and the OMAP5430 balls. In this case, considering only 1 global power domain the target impedance of this domain is 225 mΩ.

- In case where no power plan is used, use a star connection between the power IC and the OMAP5430 device:
  - 1 rail for vdda_ldo_mpu
  - 1 rail for vdda_ldo_core, vdda_ldo_mm, and vdda_vbgap_core
  - 1 rail for vdds_bankX (with X = 2, 4, 5, 8, 9, 10, 11, 12, 14, 15, 16, 18, 19, 21, 23, 24, 25, or 26), vdds_1p8v, vdds_emmc, and vdds_hdmi
  - 1 rail for pop_vdd1_lpddr2_shared
- Maximum PCB resistance:
  - 100 mΩ for vdda_ldo_mpu
  - 180 mΩ for for vdda_ldo_core, vdda_ldo_mm, and vdda_vbgap_core
  - 150 mΩ for vdds_bankX (with X = 2, 4, 5, 8, 9, 10, 11, 12, 14, 15, 16, 18, 19, 21, 23, 24, 25, or 26), vdds_1p8v, vdds_emmc, and vdds_hdmi
  - 20 mΩ for pop_vdd1_lpddr2_shared
- In any case, the maximum inductance from the power IC to each OMAP5430 power ball is 15 nH.
- Special requirements for the OMAP5430 embedded power management IPs (LDOs and BandGap):
  - Each bypass (or decoupling) capacitance must be located as close as possible to the OMAP5430 power balls (especially all vdda_ldo_x and vdda_bd_core balls): less than 2 nH for loop inductances.
  - The loop inductances on output capacitance (filtering capacitances) must be limited to:
    - 1.5 nH for cap_vdda_ldo_mpu_array and cap_vdda_ldo_mpu_array2
    - 2 nH: all other capacitors (cap_ ×)
  - The output filtering capacitors for the following output capacitor balls is 1 µF:
    - cap_vdda_ldo_sra m_core_array
    - cap_vdda_ldo_sram_mm_array
    - cap_vdda_ldo_sra m_mpu_array
    - cap_vdda_ldo_sram_mpu_array2
    - cap_vddldo_emu_wkup
    - cap_vbb_ldo_mm
    - cap_vbb_ldo_mpu
- Special PCB requirements for LPDDR2 power supply:
  - Maximum PCB resistance must be 20 mΩ.
  - Maximum inductance from the power IC to the OMAP5430 power ball is 15 nH.
  - Bypass capacitor must be located as close as possible to OMAP5430 power balls: less than 1 nH for loop inductances.

Table 8-72 describes the impedance target for each supply grouped by function (inside VDDS_1.8v domain):

Table 8-72. Impedance Target and Decoupling Capacitors for VDDA–1.8-MAIN

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdds_bankx(1), vdds_1p8v	1.8	84	90	1	6 x 100 nF	100
vdds_emmc, vdds_hdmi, vdds for jtag(2)	1.8	10	90	9	100 nF	100
pop_vdd1_lpddr2_shared	1.8	60	90	1.5	2 x 1 µF + 4 x 100 nF	500
vdda_ldo_mpu	1.8	120	50	0.45	470 nF	80
vdda_ldo_mm	1.8	40	50	2.0	220 nF	80

Table 8-72. Impedance Target and Decoupling Capacitors for VDDA–1.8-MAIN (continued)

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdda_ldo_core	1.8	40	50	1.0	220 nF	40
vdda_vbgap_core	1.8	11	50	3.6	100 nF	150

(1) In vdds_bankx, x = 2, 4, 5, 8, 9, 10, 11, 12, 14, 15, 16, 18, 19, 21, 23, 24, 25, or 26)

(2) One 100-nF decoupling capacitor for the three power supplies: vdds_emmc, vdds_hdmi, and vdds for jtag. The capacitor must be located as close as possible to the vdds_emmc power ball.

8.6.1.2.2 VDDS-1.2-MAIN Power Domain

8.6.1.2.2.1 Power Distribution Example

Figure 8-33 describes an example of power distribution for the main vdds 1.2-V power supplies.

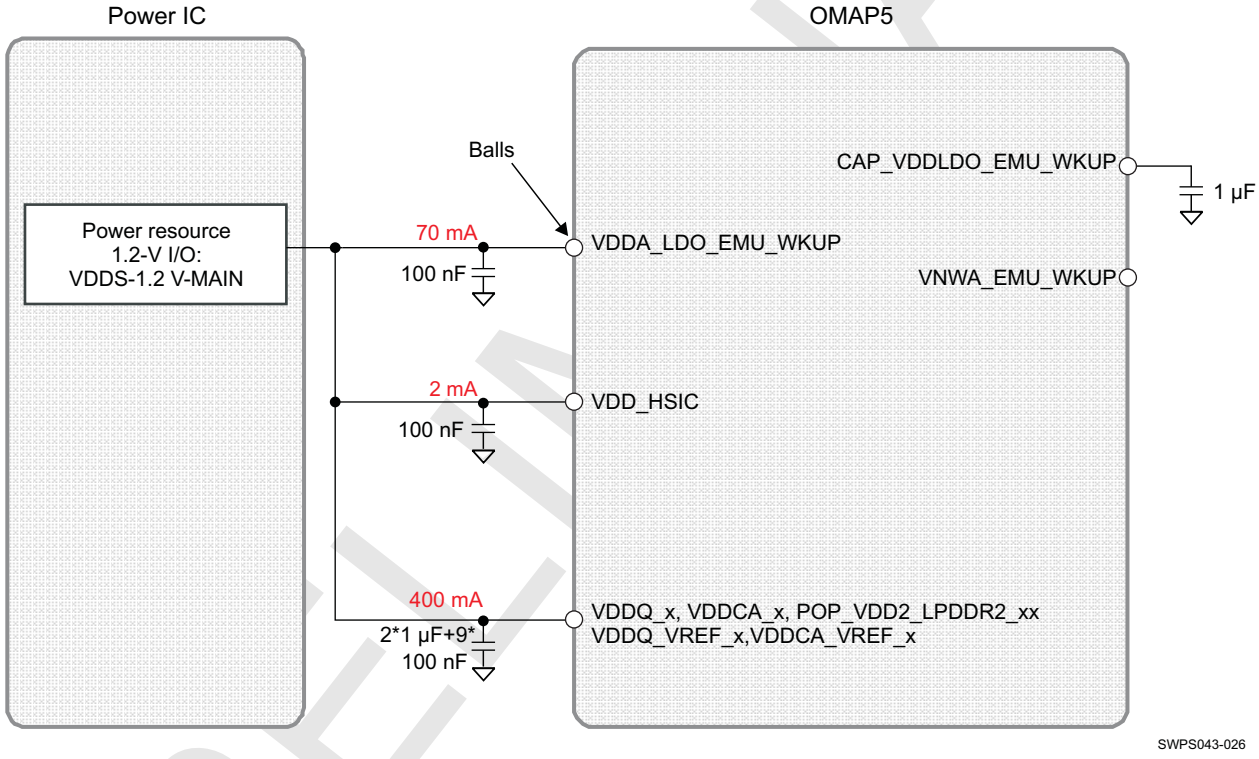

Figure 8-33. VDDS-1.2-MAIN Power Distribution

CAUTION

vnwa_emu_wkup and vdda_ldo_emu_wkup must be connected together on the board.

8.6.1.2.2 PCB Recommendation

- A power plan is strongly recommended to meet the static drop requirement (1%) between the power IC and the OMAP5430 balls. In this case, considering only 1 global power domain the target impedance of this domain is 75 mΩ.

- Special PCB requirements for wakeup LDO power supply vdda_ldo_emu_wkup:
  - Maximum resistance must be 0.15 Ω
  - Maximum inductance from power IC to OMAP5430 power ball: 15 nH
  - Bypass capacitor must be located as close as possible to the OMAP5430 power balls (vdda_ldo_emu_wkup): less than 2 nH for loop inductances.
  - Loop inductances on output capacitance (filtering capacitances) limited to:
    - 3 nH for cap_vdd_ldo_emu_wkup
- Special PCB requirements for LPDDR2 power supply:
  - Maximum resistance must be 20 mΩ
  - Maximum inductance from power IC to OMAP5430 power ball: 15 nH
  - Bypass capacitor must be located as close as possible to the OMAP5430 power balls: less than 1 nH for loop inductances.

Table 8-73 describes the impedance target for each supply grouped by function (inside vdds_1.2 domain):

Table 8-73. Impedance Target and Decoupling Capacitors for VDDA–1.2-MAIN(1)

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vddq_x, vddca_x, vddq_vref_x, vddca_vref_x, pop_vdd2_lpddr2_shared	1.2	400	60	0.15	2 x 1 µF + 9 x 100 nF	100
vdds_hsic	1.2	2	60	30	100 nF	100
vdda_ldo_emu_wkup(2)	1.2	70	60	0.85	100 nF	60

(1) In vddq_x, x = vddq_ddr_ch1 and vddq_ddr_ch2
In vddq_vref_x, x = vddq_vref_ddrch1 and vddq_vref_ddrch2
In vddca_x, x = vddca_lpddr2ch1 and vddca_lpddr2ch2
In vddca_vref_x, x = vddca_vref_lpddr2ch1 and vddca_vref_lpddr2ch2

(2) **CAUTION**: vnwa_emu_wkup and vdda_ldo_emu_wkup must be connected together on the board.

8.6.1.2.3 VDDA Power Domain

8.6.1.2.3.1 VDDAPHY–CAMERAS PCB Recommendation

- PCB routing recommendation: star connection between the power IC and the OMAP5430 device:
  - 1 rail for vdda_csiporta,
  - 1 rail for vdda_csiportb, vdda_csiportc,
  - With the star point located at 5 nH or more from the OMAP5430 ball to ensure a good noise isolation between the different IPs.
- With a maximum resistance of 0.3 Ω for each vdda_csiporta.
- With a maximum resistance of 0.5 Ω for each vdda_csiportb, vdda_csiportc.
- With a maximum inductance from the power IC to each OMAP5430 power ball: 15 nH for each rail.
- Each bypass capacitor must be located as close as possible to the OMAP5430 device:
  - With a loop inductance less than 1.5 nH.

The impedance targets for each vdda_csiporta, vdda_csiportb, vdda_csiportc and the corresponding bypass capacitor values are described in Table 8-74.

Table 8-74. Impedance Target and Decoupling Capacitors for VDDAPHY–CAMERAS

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdda_csiporta	1.5 V or 1.8 V	11	50	4.5	220 nF	140
vdda_csiportb	1.5 V or 1.8 V	10	50	5.0	220 nF	140
vdda_csiportc	1.5 V or 1.8 V	10	50	5.0	220 nF	140

8.6.1.2.3.2 VDDAPHY–DISPLAYS PCB Recommendation

- PCB routing recommendation: star connection between the power IC and the OMAP5430 device:
  - 1 rail for vdda_hdmi,
  - 1 rail for vdda_dsiporta, vdda_dsiportc,
  - With the star point located at 5 nH or more from the OMAP5430 ball to ensure a good noise isolation between the different IPs.
- With a maximum resistance of 0.4 Ω for each vdda_hdmi.
- With a maximum resistance of 0.5 Ω for each vdda_dsiporta, vdda_dsiportc.
- With a maximum inductance from the power IC to each OMAP5430 power ball: 15 nH for each rail.
- Each bypass capacitor must be located as close as possible to the OMAP5430 device:
  - With a loop inductance less than 1.5 nH.

The impedance targets for each vdda_hdmi, vdda_dsiporta, vdda_dsiportc and the corresponding bypass capacitor values are described in Table 8-75:

Table 8-75. Impedance Target and Decoupling Capacitors for VDDAPHY–Displays

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdda_hdmi	1.5 V or 1.8 V	15	50	3.3	470 nF	50
vdda_dsiporta	1.5 V or 1.8 V	16	50	3.0	220 nF	140
vdda_dsiportc	1.5 V or 1.8 V	16	50	3.0	220 nF	140

8.6.1.2.3.3 VDDAPHY–1.8V-REF PCB Recommendation

- PCB routing recommendation: star connection between the power IC and the OMAP5430 device:
  - 1 rail for vdda_dpll_mpu, vdda_dpll_mm_l4per, and vdda_dpll_core_emu_abe
  - 1 rail for vdda_slicer, vdds_osc
  - With the star point located at 5 nH or more from the OMAP5430 ball to ensure a good noise isolation between the different IPs.
- With a maximum resistance of 0.3 Ω for each rail listed above.
- With a maximum inductance from the power IC to each OMAP5430 power ball: 15 nH for each rail.
- Each bypass capacitor must be located as close as possible to the OMAP5430 device:
  - With a loop inductance less than 1.5 nH.

The impedance targets for each vdda_dpll_mpu, vdda_dpll_mm_l4per, vdda_dpll_core_emu_abe, vdda_slicer, and vdds_osc, and the corresponding bypass capacitor values are described in Table 8-76:

Table 8-76. Impedance Target and Decoupling Capacitors for VDDA–1.8-REF

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdda_dpll_mpu	1.8	10	50	5	100 nF	250
vdda_dpll_mm_l4per	1.8	15	50	3.5	100 nF	250
vdda_dpll_core_emu_abe	1.8	10	50	5	100 nF	250
vdda_slicer	1.8	10	50	5	100 nF	50
vdds_osc	1.8	10	50	5	100 nF	100

8.6.1.2.3.4 VDDA–1.8-PHY PCB Recommendation

- PCB routing recommendation: star connection between the power IC and the OMAP5430 device:
  - 1 rail for vdda_sata
  - 1 rail for vdds_usbhs18, vdda_usbss18
  - 1 rail for vdda_dpll_hdmi (HDMI and USBSS)
  - With the star point located at 5 nH or more from the OMAP5430 ball to ensure a good noise isolation between the different IPs.
- With a maximum resistance of 0.5 Ω for vdda_sata.
- With a maximum resistance of 0.3 Ω for vdds_usbhs18, vdda_usbss18.
- With a maximum resistance of 0.3 Ω for vdda_dpll_hdmi (HDMI and USBSS)
- With a maximum inductance from the power IC to each OMAP5430 power ball: 15 nH for each rail.
- Each bypass capacitor must be located as close as possible to the OMAP5430 device:
  - With a loop inductance less than 1.5 nH.

The impedance targets for each vdda_sata, vdds_usbhs18, vdda_usbss18, vdda_dpll_hdmi (HDMI and USBSS), and the corresponding bypass capacitor values are described in Table 8-77:

Table 8-77. Impedance Target and Decoupling Capacitors for VDDA–1.8-PHY

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdda_sata	1.8	24	50	2	220 nF	140
vdds_usbhs18	1.8	26	50	2	220 nF	140
vdda_usbss18	1.8	24	50	2	220 nF	140
vdda_dpll_hdmi	1.8	5	50	10	100 nF	140

8.6.1.2.3.5 VDDA–3V-USB PCB Recommendation

- With a maximum resistance of 0.5 Ω for vdda_usbhs33.
- With a maximum inductance from the power IC to each OMAP5430 power ball: 15 nH for each rail.
- Each bypass capacitor must be located as close as possible to the OMAP5430 device:
  - With a loop inductance less than 1.5 nH.

The impedance targets for vdda_usbhs33 and the corresponding bypass capacitor values are described in Table 8-78:

Table 8-78. Impedance Target and Decoupling Capacitors for VDDA–3.3-PHY

POWER SIGNAL NAME	VOLTAGE (V)	MAXIMUM CURRENT VARIATION BTW [0 to 50 MHz] (mA)	MAXIMUM RIPPLE PEAK-PEAK (mV)	PCB IMPEDANCE TARGET (Ω)	NOMINAL PCB CAPACITOR VALUE	MAXIMUM FREQUENCY BANDWIDTH (MHz)
vdda_usbhs33	3.3	35	70	1.7	220	100

8.6.1.2.4 VSYS Power Domain

8.6.1.2.4.1 VSYS PCB Recommendation

VSYS power domain supplies the battery voltage to the different ICs in the platform described in Figure 8-34.

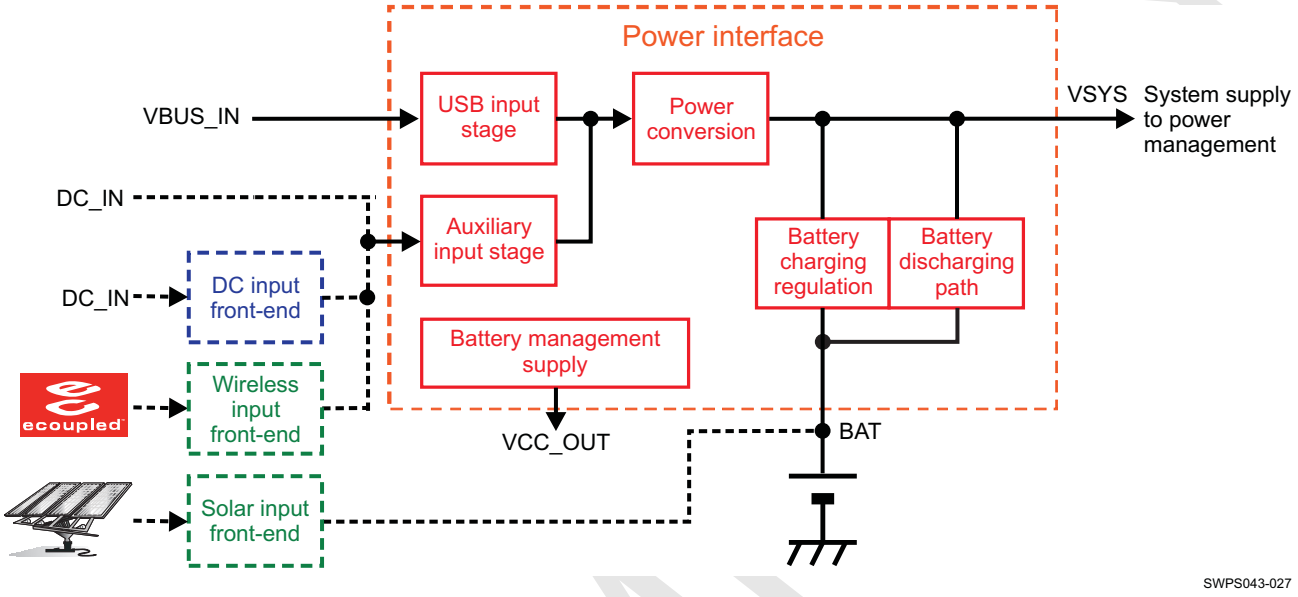

Figure 8-34. VSYS Power Domain

The static constraints are:

- The battery discharge path includes an N-MOSFET component which is turned off during the charging. During the battery discharge (MOSFET = ON), as this MOSFET will add some drop in the battery path (R on ~15 mΩ FDS6680A), the additional drop due to PCB routing has to be optimized between the battery VBAT and:
  - The PA (2.5-A peak current consumption)
  - The voltage input of the buck converter which provides the MPU voltage vdd_mpu (2-A peak from the battery)
  - The power Flash LEDs input boost regulator (3-A peak from the battery)
- By considering maximum 2% drop allowed between the battery and these 3 above critical paths, with a 3-A maximum current, the maximum PCB resistance is ~10 mΩ.
  - The path from VSYS and the load when the battery is dead or when there is no battery, is less critical than the previous one as this path is direct to the load (without any FETs). With the same assumption as above: the maximum PCB resistance is 25 mΩ.

The dynamic constraints are:

- By considering the GSM transmission use case where the transient time is 10 µs for a 2.5-A maximum current variation, and with a 350-mV allowed drop on VSYS (~1%), the total amount of bypass capacitance on VSYS domain is ~100 µF **(2 x 47 µF)**.
- Bypass capacitor must be located as close as possible to PA and the Power IC.

8.7 Clock Guidelines

NOTE

For more information on system clocks, see , *Clock Specifications*.

8.7.1 32-kHz Oscillator Routing

When designing the printed-circuit board:

- Keep the crystal as close as possible to the crystal pins X1 and X2.
- Keep the trace lengths short and small to reduce capacitor loading and prevent unwanted noise pickup.
- Place a guard ring around the crystal and tie the ring to ground to help isolate the crystal from unwanted noise pickup.
- Keep all signals out from beneath the crystal and the X1 and X2 pins to prevent noise coupling.
- Finally, an additional local ground plane on an adjacent PCB layer can be added under the crystal to shield it from unwanted pickup from traces on other layers of the board. This plane must be isolated from the regular PCB ground plane and tied to the GND pin of the RTC. The plane must not be any larger than the perimeter of the guard ring. Make sure that this ground plane does not contribute to significant capacitance (a few pF) between the signal line and ground on the connections that run from X1 and X2 to the crystal.

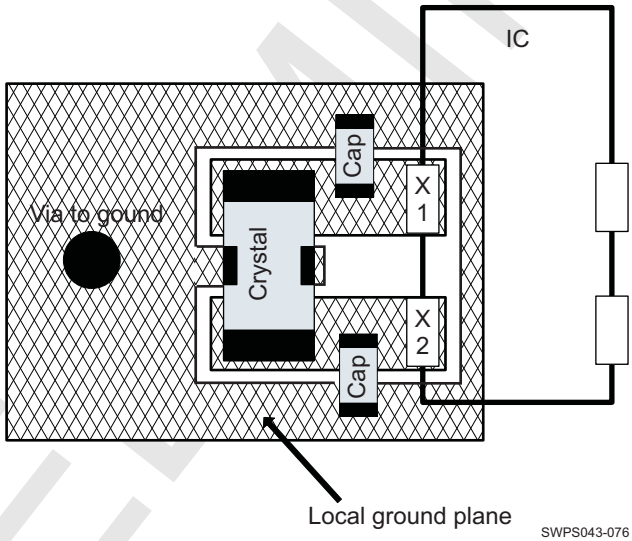

Figure 8-35. Slow Clock PCB Requirements

8.7.2 Oscillator Ground Connection

Although the impedance of a ground plane is low it is, of course, not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. If the two capacitors of the oscillator are connected directly to the ground plane, the voltage drop in the red portion of the ground in Figure 8-36 will be overlaid to the oscillator signals. If the noise related voltage drop is big enough, the oscillator may be disturbed.

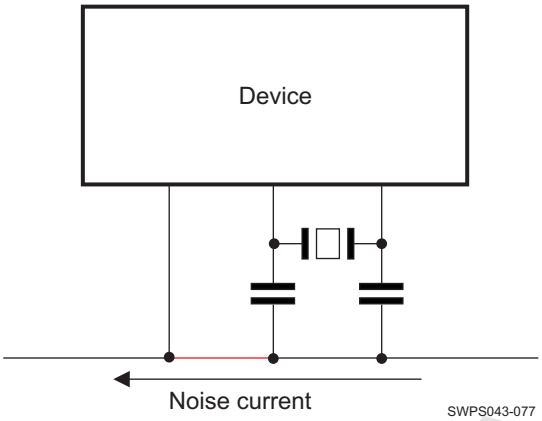

Figure 8-36. Slow Clock PCB Requirements

The overlay of ground noise may be avoided by providing an extra ground trace for the oscillator ground as indicated in green in Figure 8-37. Even in a multilayer PCB this is a powerful measure to improve the susceptibility of the oscillator.

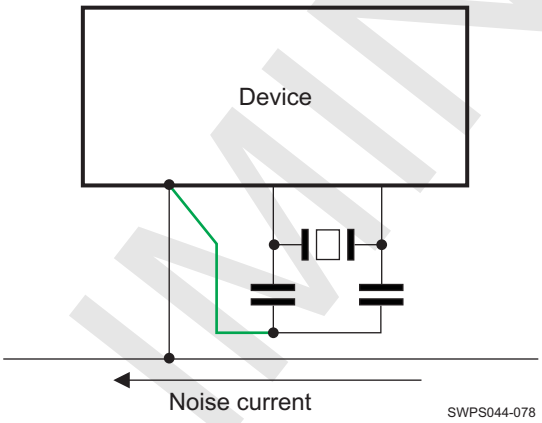

Figure 8-37. Optimized Oscillator Ground Connection

9 Glossary

AC or ac	Alternating Current
APLL	Analog Phase-Locked Loop
ARM	Advanced RISC Machine
ASIC	Application-Specific Integrated Circuit
BG	Bandgap
CAM	Parallel Camera Interface
CCP	Compact Camera Port
CDM	Charged Device Modem
CJTAG	Component Joint Test Action Group, IEEE 1149.1 Standard
CM	Clock Manager
CMOS	Complementary Metal Oxide Silicon
CSI	Camera Serial Interface
DAC	Digital-to-Analog Converter
DC or dc	Direct Current
DDR	Double Data Rate
DISPC	Display Controller
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DMIC	Digital Microphone
DPLL	Digital Phase-Locked Loop
DSI	Display Serial Interface
DSS	Display Subsystem
eFuse	Electrical Fuse
EMIF	External Memory Inferface
EMU	Emulation
ESD	Electrostatic Discharge
ESR	Equivalent series resistance
ETK	Embedded Trace kit
ETM	Embedded Trace Macrocell
FIR	Fast Infrared
FSR	Full-Scale Range
FSUSB	Full-Speed Universal Serial Bus
GP	General-Purpose
GPIN	General-Purpose Input
GPIO	General-Purpose Input Output
GPMC	General-Purpose Memory Controller
HBM	Human Body Model
HDMI	High Definition Multimedia Interface
HDQ	High-Speed Data Queue
HDTV	High-Definition Television
HS	High speed or high security
HSI	High-speed Synchronous Interface
HSUSB	High-Speed Universal Serial Bus
HWDBG	Hardware Debug
HYS	Hysteresis
I^2C	Inter-Integrated Circuit
I2S	Inter IC Sound
IC	Integrated Circuit

ICE	In-Circuit Emulator
IEEE	Institute of Electrical and Electronics Engineers
IO	Input or Output
IR	Infrared
IrDA	Infrared Data Association
ISP	Image Sensing Product
ITU	International Telecommunications Union
IVA	Image and Video Accelerator
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group (Image format)
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LCD	Liquid-Crystal Display
LDO	Low Dropout
LJF	Left-Justified Format
LP	Low Power
LVCMOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signaling
McBSP	Multichannel Buffered Serial Port
McSPI	Multichannel Serial Port Interface
MIPI®	Mobile Industry Processor Interface (MIPI ® is a registered trademark of Mobile Industry Processor (MIPI) Alliance.)
MIR	Medium Infrared
MMC	MultiMedia Card
MPU	Microprocessor Unit
MS-PRO	Memory Stick PRO
NA	Not Applicable
NAND	Not AND (Boolean Logic)
NOR	Not OR (Boolean Logic)
OMAP	Open Multimedia Applications Platform
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PDN	Power Delivery Network
PD	Pull Down
PHY	Physical Layer Controller
PLL	Phase-Locked Loop
POP	Package On Package
PU	Pull Up
QXGA	Quad eXtended Graphics Array
RAW	Raw (Image format)
RFBI	Remote Frame Buffer Interface
RGB	Red Green Blue (Image format)
RMS	Root Mean Square
RX	Receiver / Receive
SAP	TBD
SCL	Serial Clock: programmable serial clock used in the I^2C interface (can be called also SCLK)
SDA	Serial Data: serial data bus in the I^2C interface
SDI	Serial Display Interface
SDIO	Secure Digital Input Output

SDMMC	Secure Digital MultiMedia Card
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SDRC	SDRAM Controller
SDTI	System Debug Trace Interface
SIM	Subscriber Identity Module
SIR	Slow Infrared
SPI	Serial Port Interface
SRAM	Synchronous Random Access Memory
SSI	Synchronous Serial Interface
STN	Super Twist Nematic (LCD Panel)
SYNC	Synchronous
SYS	System
TAP	Test Access Point
TBD	To Be Defined
TDM	Time Division Multiplexing
TFT	Thin Film Transistor (LCD Panel)
TLL	Transistor-Transistor Logic
TX	Transmitter / Transmit
UART	Universal Asynchronous Receiver Transmitter
ULPI	UTMI Low Pin Interface
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
UTMI	USB2.0 Transceiver Macrocell Interface
WKUP	Wake-Up
YUV	Luminance + 2 Chrominance Difference Signals (PAL Y, Cr, Cb) Color Encoding

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