Low-Power Sub-GHz RF Transceiver
(470-510 MHz & 950-960 MHz)

Applications

- *Ultra low-power wireless applications operating in the 470/950 MHz ISM/SRD bands*
- *Wireless sensor networks*
- *Home and building automation*
- *Advanced Metering Infrastructure (AMI)*
- *Wireless metering*
- *Wireless alarm and security systems*

Product Description

The **CC1100E** is a Sub-GHz high performance radio transceiver designed for very low power RF applications. It is intended for the Industrial, Scientific and Medical (ISM) and Short Range Device (SRD) frequency bands at 470-510 MHz and 950-960 MHz. The **CC1100E** is especially suited for wireless applications targeted at the Japanese ARIB STD-T96 and the Chinese Short Range Device Regulations at 470-510 MHz.

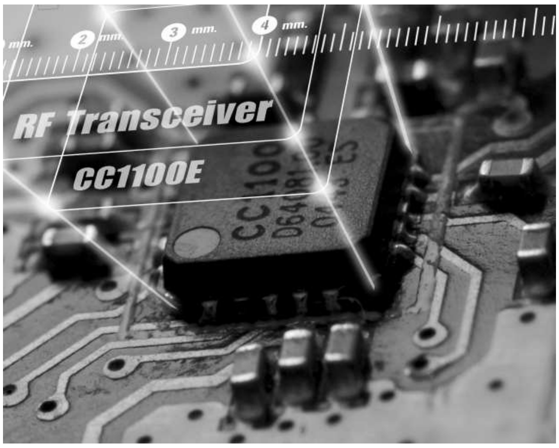
The **CC1100E** is code, package and pin out compatible with both the **CC1101** [1] and **CC1100** [2] RF transceivers. The **CC1100E**, **CC1101** and **CC1100** support complementary frequency bands and can be used to cover RF designs at the most commonly used sub-1 GHz license free frequencies around the world:

- **CC1100E**: 470-510 MHz and 950-960 MHz
- **CC1101**: 300-348 MHz, 387-464 MHz and 779-928 MHz
- **CC1100**: 300-348 MHz, 400-464 MHz and 800-928 MHz

The **CC1100E** RF transceiver is integrated with a highly configurable baseband modem. The modem supports various modulation formats and has a configurable data rate of up to 500 kBaud.

The **CC1100E** provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication, and wake-on-radio.

The main operating parameters and the 64-byte transmit/receive FIFOs of the **CC1100E** can be controlled via an SPI interface. In a typical system, the **CC1100E** will be used with a microcontroller and a few additional passive components.



This product shall not be used in any of the following products or systems without prior express written permission from Texas Instruments:

- *(i) implantable cardiac rhythm management systems, including without limitation pacemakers, defibrillators and cardiac resynchronization devices,*
- *(ii) external cardiac rhythm management systems that communicate directly with one or more implantable medical devices; or*
- *(iii) other devices used to monitor or treat cardiac function, including without limitation pressure sensors, biochemical sensors and neurostimulators.*

Please contact lpw-medical-approval@list.ti.com if your application might fall within the category described above.

Key Features

RF Performance

- High sensitivity (–112 dBm at 1.2 kBaud, 480 MHz, 1% packet error rate)
- Low current consumption (15.5 mA in RX, 1.2 kBaud, 480 MHz)
- Programmable output power up to +10 dBm for all supported frequencies
- Excellent receiver selectivity and blocking performance
- Programmable data rate from 1.2 to 500 kBaud
- Frequency bands: 470-510 MHz and 950-960 MHz

Analog Features

- 2-FSK, GFSK, and MSK supported as well as OOK and flexible ASK shaping
- Suitable for frequency hopping systems due to a fast settling frequency synthesizer; 90 µs settling time
- Automatic Frequency Compensation (AFC) can be used to align the frequency synthesizer to the actual received signal center frequency
- Integrated analog temperature sensor

Digital Features

- Flexible support for packet oriented systems; On-chip support for sync word detection, address check, flexible packet length, and automatic CRC handling
- Efficient SPI interface; All registers can be programmed with one “burst” transfer
- Digital RSSI output
- Programmable channel filter bandwidth
- Programmable Carrier Sense (CS) indicator
- Programmable Preamble Quality Indicator (PQI) for improved protection against false sync word detection in random noise
- Support for automatic Clear Channel Assessment (CCA) before transmitting (for listen-before-talk systems)
- Support for per-package Link Quality Indication (LQI)
- Optional automatic whitening and de-whitening of data

Low-Power Features

- 400 nA sleep mode current consumption
- Fast start-up time; 240 µs from sleep to RX or TX mode (measured on EM reference design [3] and [4])
- Wake-on-radio functionality for automatic low-power RX polling
- Separate 64-byte RX and TX data FIFOs (enables burst mode data transmission)

General

- Few external components; Completely on-chip frequency synthesizer, no external filters or RF switch needed
- Green package: RoHS compliant and no antimony or bromine
- Small size (QFN 4x4 mm package, 20 pins)
- Suited for systems targeting compliance with ARIB STD-T96
- Suited for systems targeting compliance with the Chinese Short Range Device Regulations at 470-510 MHz
- Support for asynchronous and synchronous serial receive/transmit mode for backwards compatibility with existing radio communication protocols

Abbreviations

Abbreviations used in this data sheet are described below.

ACP	Adjacent Channel Power	MSK	Minimum Shift Keying
ADC	Analog to Digital Converter	N/A	Not Applicable
AFC	Automatic Frequency Compensation	NRZ	Non Return to Zero (Coding)
AGC	Automatic Gain Control	OOK	On-Off Keying
AMR	Automatic Meter Reading	PA	Power Amplifier
ARIB	Association of Radio Industries and Businesses	PCB	Printed Circuit Board
ASK	Amplitude Shift Keying	PD	Power Down
BER	Bit Error Rate	PER	Packet Error Rate
BT	Bandwidth-Time product	PLL	Phase Locked Loop
CCA	Clear Channel Assessment	POR	Power-On Reset
CFR	Code of Federal Regulations	PQI	Preamble Quality Indicator
CRC	Cyclic Redundancy Check	PQT	Preamble Quality Threshold
CS	Carrier Sense	PTAT	Proportional To Absolute Temperature
CW	Continuous Wave (Unmodulated Carrier)	QFN	Quad Leadless Package
DC	Direct Current	QPSK	Quadrature Phase Shift Keying
DVGA	Digital Variable Gain Amplifier	RC	Resistor-Capacitor
ESR	Equivalent Series Resistance	RF	Radio Frequency
FEC	Forward Error Correction	RSSI	Received Signal Strength Indicator
FIFO	First-In-First-Out	RX	Receive, Receive Mode
FHSS	Frequency Hopping Spread Spectrum	SAW	Surface Acoustic Wave
2-FSK	Binary Frequency Shift Keying	SMD	Surface Mount Device
GFSK	Gaussian shaped Frequency Shift Keying	SNR	Signal to Noise Ratio
IF	Intermediate Frequency	SPI	Serial Peripheral Interface
I/Q	In-Phase/Quadrature	SRD	Short Range Devices
ISM	Industrial, Scientific, Medical	TBD	To Be Defined
LC	Inductor-Capacitor	T/R	Transmit/Receive
LNA	Low Noise Amplifier	TX	Transmit, Transmit Mode
LO	Local Oscillator	UHF	Ultra High frequency
LSB	Least Significant Bit	VCO	Voltage Controlled Oscillator
LQI	Link Quality Indicator	WOR	Wake on Radio, Low power polling
MCU	Microcontroller Unit	XOSC	Crystal Oscillator
MSB	Most Significant Bit	XTAL	Crystal

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1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD + 0.3 max 3.9	V	
Voltage on the pins RF_P, RF_N, and DCOUPL	–0.3	2.0	V	
Voltage ramp-up rate		120	kV/µs	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020
ESD		2000	V	According to JEDEC STD 22, method A114, Human Body Model (HBM)
ESD		750	V	According to JEDEC STD 22, C101C, Charged Device Model (CDM)

Table 1: Absolute Maximum Ratings

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

2 Operating Conditions

The operating conditions for the **CC1100E** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	-40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

3 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	470		510	MHz	
	950		960	MHz	
Data rate	1.2		500	kBaud	2-FSK
	1.2		250	kBaud	GFSK, OOK, and ASK
	26		500	kBaud	(Shaped) MSK (also known as differential offset QPSK)
					Optional Manchester encoding (the data rate in kbps will be half the baud rate)

Table 3: General Characteristics

4 Electrical Specifications

4.1 Current Consumption

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1100E EM reference designs ([3] and[4]). Reduced current settings (`MDMCFG2.DEM_DCFILT_OFF=1`) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See Table 6: RF Receive Section for additional details on current consumption and sensitivity.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		0.3		µA	Voltage regulator to digital part off, register values retained (SLEEP state). All GDO pins programmed to 0x2F (HW to 0)
		0.7		µA	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)
		100		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with `MCSM0.OSC_FORCE_ON` set)
		165		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		10.0		µA	Automatic RX polling once each second, using low-power RC oscillator, with 460 kHz filter bandwidth and 250 kBaud data rate, PLL calibration every 4th wakeup. Average current with signal in channel *below* carrier sense level (`MCSM2.RX_TIME_RSSI=1`)
		35		µA	Same as above, but with signal in channel *above* carrier sense level, 1.95 ms RX timeout, and no preamble/sync word found
		1.3		µA	Automatic RX polling every 15th second, using low-power RC oscillator, with 460 kHz filter bandwidth and 250 kBaud data rate, PLL calibration every 4th wakeup. Average current with signal in channel below carrier sense level (`MCSM2.RX_TIME_RSSI=1`)
		32		µA	Same as above, but with signal in channel *above* carrier sense level, 29.3 ms RX timeout, and no preamble/sync word found
		1.7		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		9		mA	Only the frequency synthesizer is running (FSTXON state). This currents consumption is also representative for the other intermediate states when going from IDLE to RX or TX, including the calibration state
Current consumption, 480 MHz		16.5		mA	Receive mode, 1.2 kBaud, reduced current, input at sensitivity limit
		15.4		mA	Receive mode, 1.2 kBaud, reduced current, input well above sensitivity limit
		16.6		mA	Receive mode, 38.4 kBaud , reduced current, input at sensitivity limit
		15.5		mA	Receive mode, 38.4 kBaud , reduced current, input well above sensitivity limit
		17.5		mA	Receive mode, 250 kBaud, reduced current, input at sensitivity limit
		16.1		mA	Receive mode, 250 kBaud, reduced current, input well above sensitivity limit
		20		mA	Receive mode, 500 kBaud, input at sensitivity limit
		18.7		mA	Receive mode, 500 kBaud, input well above sensitivity limit
		29.6		mA	Transmit mode, +10 dBm output power
		16.6		mA	Transmit mode, 0 dBm output power
		16.5		mA	Transmit mode, –6 dBm output power

Parameter	Min	Typ	Max	Unit	Condition
Current consumption, 955 MHz		16.3		mA	Receive mode, 1.2 kBaud , reduced current, input at sensitivity limit
		15.2		mA	Receive mode, 1.2 kBaud , reduced current, input well above sensitivity limit
		17.7		mA	Receive mode, 38.4 kBaud , reduced current, input at sensitivity limit
		17.0		mA	Receive mode, 38.4 kBaud , reduced current, input well above sensitivity limit
		16.8		mA	Receive mode, 76.8 kBaud , reduced current, input at sensitivity limit
		15.1		mA	Receive mode, 76.8 kBaud , reduced current, input well above sensitivity limit
		30.9		mA	Transmit mode, +10 dBm output power
		16.5		mA	Transmit mode, 0 dBm output power
		15.8		mA	Transmit mode, –6 dBm output power

Table 4: Electrical Specifications

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Current [mA]	29.3	28.7	28.1	31.6	30.9	30.3	31.9	31.2	30.6

Table 5: Typical Variation in TX Current Consumption over Temperature and Supply Voltage, 955 MHz and +10 dBm Output Power Setting

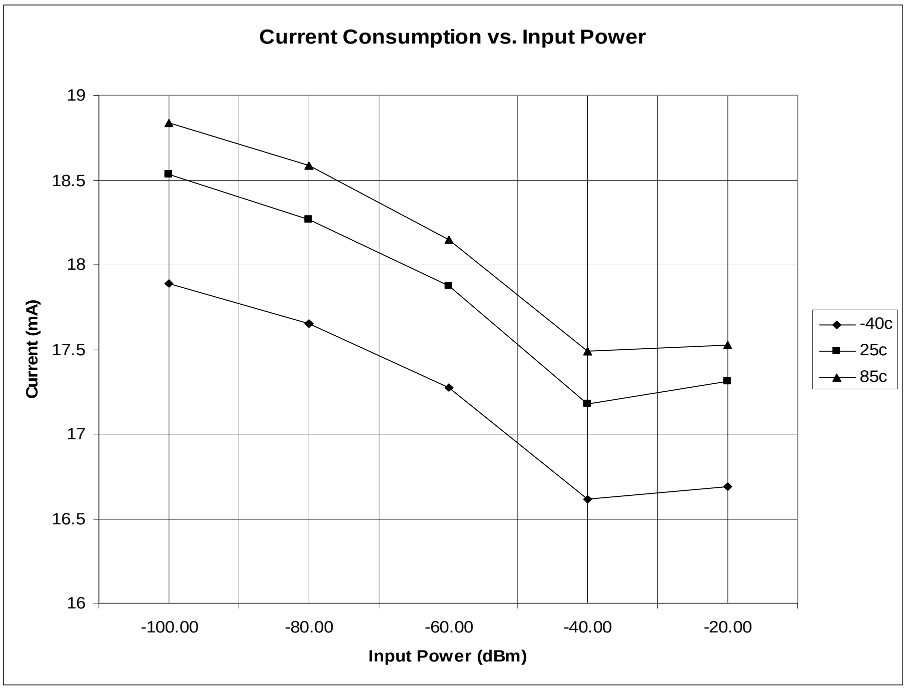


Figure 1: Typical Variation in RX Current Consumption overt Temperature and Input Power Level, 955 MHz, 76.8 kBaud GFSK, Sensitivity Optimized Setting

4.2 RF Receive Section

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1100E EM reference designs ([3] and[4]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
480 MHz, 1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK with BT=1, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		-112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.9 mA to 16.5 mA at sensitivity limit. The sensitivity is typically reduced to -110 dBm
480 MHz, 38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK with BT=1, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18mA to 16.6 mA at sensitivity limit.
480 MHz, 250 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK with BT=1, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		-95		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 19.2mA to 17.5 mA at sensitivity limit.
480 MHz, 500 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (MSK, 1% packet error rate, 20 bytes packet length, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		-88		dBm	Setting `MDMCFG2.DEM_DCFILT_OFF=1` is not an valid option at 500 kBaud dara rate
955 MHz, 1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK with BT=1, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–111		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.2 mA to 16.3 mA at sensitivity limit. The sensitivity is typically reduced to -109 dBm
Saturation		-15		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [11]
Adjacent channel rejection		28		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
Alternate channel rejection		37		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
					See Figure 2 for plot of selectivity versus frequency offset
Image channel rejection, 955 MHz		32		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using the CC1100E EM reference designs ([3] and[4])

955 MHz, 38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK with BT=1, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		-104		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.3mA to 17.7 mA at sensitivity limit.
Saturation		-18		dBm	`FIFOTHR.CLOSE_IN_RX=0.` See more in DN010 [11]
Adjacent channel rejection		12		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
Alternate channel rejection		27		dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing
					See Figure 3 for plot of selectivity versus frequency offset
Image channel rejection, 955 MHz		23		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit

Parameter	Min	Typ	Max	Unit	Condition/Note
955 MHz, 76.8 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK with BT=1, 1% packet error rate, 20 bytes packet length, 32 kHz deviation, 232 kHz digital channel filter bandwidth)					
Receiver sensitivity		-100		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.6mA to 16.8 mA at sensitivity limit.
Blocking					
Blocking at ±2 MHz offset, 1.2 kBaud, 955 MHz		-49		dBm	Desired channel 3 dB above the sensitivity limit
Blocking at ±2 MHz offset, 38.4 kBaud, 955 MHz		-49		dBm	Desired channel 3 dB above the sensitivity limit
Blocking at ±10 MHz offset, 1.2 kBaud, 955 MHz		-39		dBm	Desired channel 3 dB above the sensitivity limit
Blocking at ±10 MHz offset, 38.4 kBaud, 955 MHz		-40		dBm	Desired channel 3 dB above the sensitivity limit
General					
Spurious Emmissions			-38 -32	dBm dBm	25 MHz – 1 GHz Excluding the 470-510 MHz band, signal at 960 MHz, 2nd harmonicAbove 1 GHz Typical radiated spurious emission is -49 dBm measured at the VCO frequency Data above is for the 470-510 MHz band, for spurious emmisions at 950-960 MHz, look at section 28.
RX latency		9		Bit	Serial operation. Time from start of reception until data is available on the receiver data output pin is equal to 9 bits.

Table 6: RF Receive Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Sensitivity [dBm]	-101	-100	-96	-102	-100	-98	-102	-100	-98

Table 7: Typical Variation in Sensitivity over Temperature and Supply Voltage, 955 MHz, 76.8 kBaud GFSK, Sensitivity Optimized Setting, 770 MHz notch filter Used

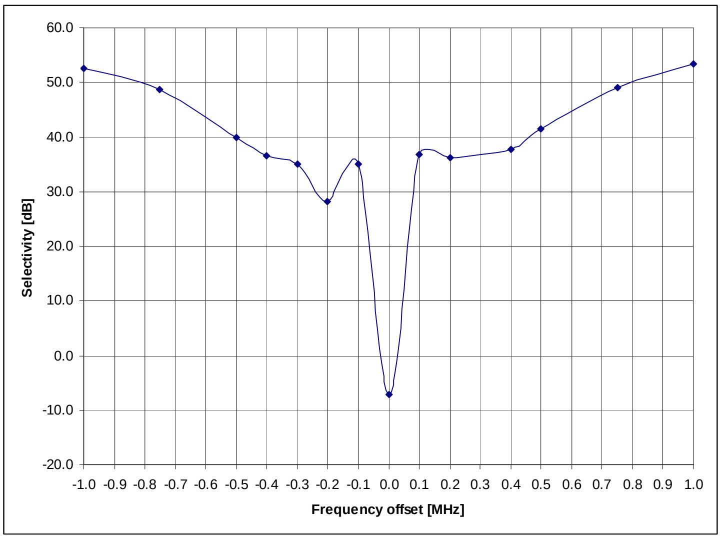


Figure 2: Typical Selectivity at 1.2 kBaud Data Rate, 955 MHz, GFSK, 5.2 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 58 kHz

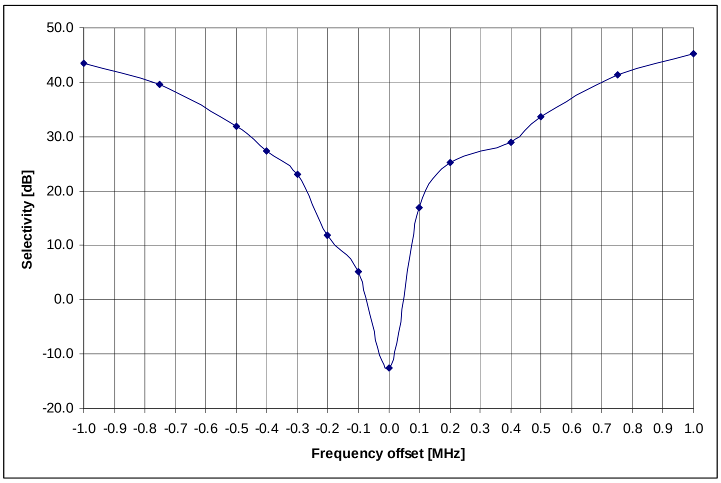


Figure 3: Typical Selectivity at 38.4 kBaud Data Rate, 955 MHz, GFSK, 20 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 100 kHz

4.3 RF Transmit Section

T_A = 25°C, VDD = 3.0 V, +10dBm if nothing else stated. All measurement results are obtained using the CC1100E EM reference designs ([3] and[4]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance 480 MHz 955 MHz		 132 – j2 59 – j67		 Ω Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC1100E EM reference designs ([3] and 0) available from the TI website
Output power, highest setting 480 MHz 955 MHz		 +10 +9		 dBm dBm	Output power is programmable, and full range is available in all frequency bands. Output power may be restricted by regulatory limits. Delivered to a 50 Ω single-ended load via the CC1100E EM reference designs ([3] and 0) RF matching network
Output power, lowest setting		-30		dBm	Output power is programmable, and full range is available in all frequency bands Delivered to a 50Ω single-ended load via the CC1100E EM reference designs ([3] and 0) RF matching network
Harmonics, conducted 480 MHz 2nd Harm, 480 MHz 3rd Harm, 480 MHz 955 MHz 2nd Harm, 955 MHz 3rd Harm, 955 MHz		 -40 -48 -34 -50		 dBm dBm dBm dBm	Measured with 10 dBm CW, TX frequency at 480 / 955 MHz Frequencies below 960 MHz Frequencies above 960 MHz
Spurious emissions, conducted, harmonics not included 480 MHz 955MHz		 -39 -50		 dBm dBm	Measured with +10 dBm CW, TX frequency at 480 / 955 MHz Frequencies below 1 GHz, outside 470-510 MHz band Frequencies above 1 GHz Refer to section 28.1 for information on Spurious Emissions
General					
TX latency		8		bit	Serial operation. Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports

Table 8: RF Transmit Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Output Power [dBm]	10.1	10.8	10.8	10.2	10.4	10.5	9.2	9.9	9.9

Table 9: Typical Variation in Output Power over Temperature and Supply Voltage, 480 MHz, +10 dBm Output Power Setting

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	-40	25	85	-40	25	85	-40	25	85
Output Power [dBm]	8.8	8.4	7.9	9.6	9.2	8.8	9.6	9.2	8.8

Table 10: Typical Variation in Output Power over Temperature and Supply Voltage, 955 MHz, +10 dBm Output Power Setting

4.4 Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC1100E EM reference designs ([3] and[4]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	
Start-up time		150		µs	This parameter is to a large degree crystal dependent. Measured on the CC1100E EM reference designs ([3] and[4]) using crystal AT-41CD2 from NDK

Table 11: Crystal Oscillator Parameters

4.5 Low Power RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC1100E EM reference designs ([3] and[4]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency	34.7	34.7	36	kHz	Calibrated RC Oscillator frequency is XTAL frequency divided by 750
Frequency accuracy after calibration			±1	%	
Temperature coefficient		+0.5		% / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running

Table 12: RC Oscillator Parameters

4.6 Frequency Synthesizer Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results are obtained using the CC1100E EM reference designs ([3] and[4]). Min figures are given using a 27 MHz crystal. Typ and max figures are given using a 26 MHz crystal.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26-27 MHz crystal. The resolution (in Hz) is equal for all frequency bands
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing
RF carrier phase noise		–92		dBc/Hz	@ 50 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 100 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 200 kHz offset from carrier
RF carrier phase noise		–98		dBc/Hz	@ 500 kHz offset from carrier
RF carrier phase noise		–107		dBc/Hz	@ 1 MHz offset from carrier
RF carrier phase noise		–113		dBc/Hz	@ 2 MHz offset from carrier
RF carrier phase noise		–119		dBc/Hz	@ 5 MHz offset from carrier
RF carrier phase noise		–129		dBc/Hz	@ 10 MHz offset from carrier
PLL turn-on / hop time	85.1	88.4	88.4	µs	Time from leaving the IDLE state until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running
PLL RX/TX settling time	9.3	9.6	9.6	µs	Settling time for the 1·IF frequency step from RX to TX
PLL TX/RX settling time	20.7	21.5	21.5	µs	Settling time for the 1·IF frequency step from TX to RX
PLL calibration time	694	721	721	µs	Calibration can be initiated manually or automatically before entering or after leaving RX/TX

Table 13: Frequency Synthesizer Parameters

4.7 Analog Temperature Sensor

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using the CC1100E EM reference designs ([3] and[4]). Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.651		V	
Output voltage at 0°C		0.747		V	
Output voltage at +40°C		0.847		V	
Output voltage at +80°C		0.945		V	
Temperature coefficient		2.47		mV/°C	Fitted from –20 °C to +80 °C
Error in calculated temperature, calibrated	-2 *	0	2 *	°C	From –20 °C to +80 °C when using 2.47 mV / °C, after 1-point calibration at room temperature * The indicated minimum and maximum error with 1-point calibration is based on simulated values for typical process parameters
Current consumption increase when enabled		0.3		mA	

Table 14: Analog Temperature Sensor Parameters

4.8 DC Characteristics

T_A = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	N/A	–50	nA	Input equals 0V
Logic "1" input current	N/A	50	nA	Input equals VDD

Table 15: DC Characteristics

4.9 Power-On Reset

When the power supply complies with the requirements in Table 16 below, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. See Section 19.1 on page 45 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time			5	ms	From 0V until reaching 1.8V
Power off time	1			ms	Minimum time between power-on and power-off

Table 16: Power-On Reset Requirements

5 Pin Configuration

The **CC1100E** pin-out is shown in Figure 4 and Table 17. See Section 26 for details on the I/O configuration.

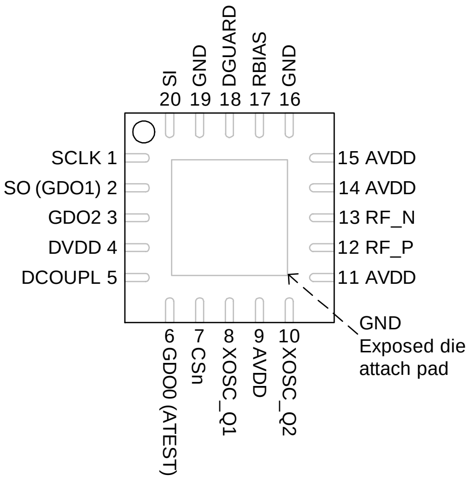


Figure 4: Pin out Top View

.

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip

Pin #	Pin Name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data
4	DVDD	Power (Digital)	1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator
5	DCOUPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling **NOTE:** This pin is intended for use only by the **CC1100E**. It can not be used to provide supply voltage to other devices
6	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode Negative RF output signal from PA in transmit mode
14	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
15	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

Table 17: Pin out Overview

6 Circuit Description

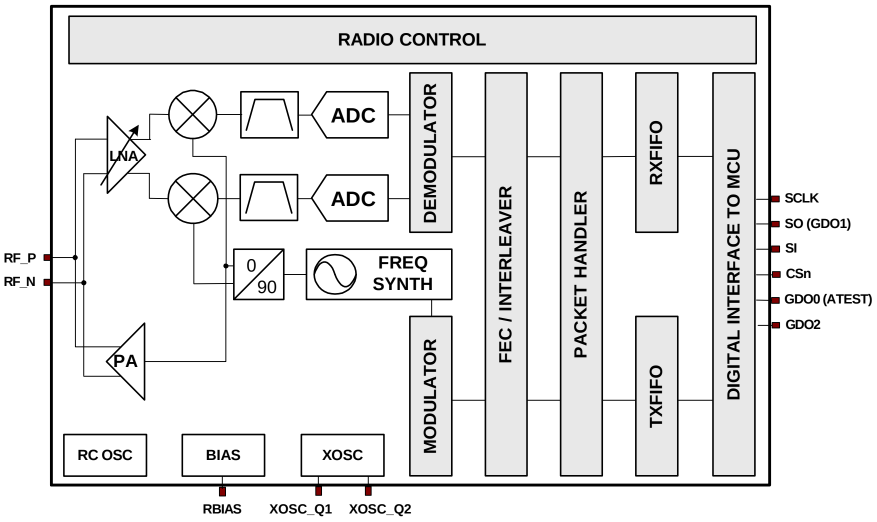


Figure 5: **CC1100E** Simplified Block Diagram

A simplified block diagram of the **CC1100E** is shown in Figure 5.

The **CC1100E** features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the ADCs. Automatic gain control (AGC), fine channel filtering and demodulation bit/packet synchronization are performed digitally.

The transmitter part of the **CC1100E** is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90 degree phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

7 Application Circuit

Only a few external components are required for using the **CC1100E**. The recommended application circuits for the **CC1100E** are shown in Figure 6 and Figure 7. The external components are described in Table 18, and typical values are given in Table 19.

7.1 Bias Resistor

The bias resistor R171 is used to set an accurate bias current.

7.2 Balun and RF Matching

The balanced RF input and output of the **CC1100E** share two common pins and are designed for a simple, low-cost matching and balun network on the printed circuit board. The receive and transmit switching at the **CC1100E** front-end is controlled by a dedicated on-chip function, eliminating the need for an external RX/TX-switch.

A few external passive components combined with the internal RX/TX switch/termination circuitry ensures match in both RX and TX mode. The components between the RF_N/RF_P pins and the point where the two signals are joined together (C131, C121, L121 and L131 for the 470 MHz reference design [3], and L121, L131, C121, L122, C131, C122 and L132 for the 950 MHz reference design [4]) form a balun that converts the differential RF signal on the **CC1100E** to a single-ended RF signal. C124 is needed for DC blocking. Together with an appropriate LC network, the balun components also transform the impedance to match a 50 Ω load. C125 provides DC blocking and is only needed if there is a DC path in the antenna. For the 950 MHz reference design, this component may also be used for additional filtering, see section 7.5 below. Suggested values for 470 MHz, and 950 MHz are listed in Table 19.

The balun and LC filter component values and their placement are important to keep the performance optimized. It is highly recommended to follow the CC1100E EM reference design ([3] and 0). Gerber files and schematics for the reference designs are available for download from the TI website.

7.3 Crystal

A crystal in the frequency range 26-27 MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C81 and C101) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{81}} + \frac{1}{C_{101}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4 Vpp signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see Section 4.4 on page 14).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application.

7.4 Reference Signal

The chip can alternatively be operated with a reference signal from 26 to 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to VDD) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC_Q1 input. The sine wave must be connected to XOSC_Q1 using a serial capacitor. This capacitor can be omitted when using a full-swing digital signal. The XOSC_Q2 line must be left un-connected. C81 and C101 can be omitted when using a reference signal.

7.5 Additional Filtering

In the 950 MHz reference design, C126 and L125 together with C125 build an optional filter to reduce emission at 770 MHz. This filter is necessary for applications with an external antenna connector that target compliance with ARIB STD-T96. If this filtering is not necessary, C125 will work as a DC block (only necessary if there is a DC path in the antenna). C126 and L125 should in that case be left unmounted.

Additional external components (e.g. an RF SAW filter) may be used in order to improve the performance in specific applications.

7.6 Power Supply Decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. The CC1100E EM reference designs ([3] and 0) should be followed closely.

7.7 Antenna Considerations

The reference designs ([3] and 0) contain an SMA connector and are matched for a 50 Ω load. The SMA connector makes it easy to connect evaluation modules and prototypes to different test equipment for example a spectrum analyzer. The SMA connector can also be replaced by an antenna suitable for the desired application. Please refer to the antenna selection guide [14] for further details regarding antenna solutions provided by TI.

Component	Description
C51	Decoupling capacitor for on-chip voltage regulator to digital part
C81/C101	Crystal loading capacitors
C121/C131	RF balun/matching capacitors
C122	RF LC filter/matching filter capacitor (470 MHz). RF balun/matching capacitor (950 MHz).
C123	RF LC filter/matching capacitor
C124	RF balun DC blocking capacitor
C125	RF LC filter DC blocking capacitor and part of optional RF LC filter (950 MHz)
C126	Part of optional RF LC filter and DC-block (950 MHz)
L121/L131	RF balun/matching inductors (wire wound or multi-layer type)
L122	RF LC filter/matching filter inductor (470 MHz). RF balun/matching inductor (950 MHz). (wire wound or multi-layer type)
L123	RF LC filter/matching filter inductor (wire wound or multi-layer type)
L124	RF LC filter/matching filter inductor (wire wound or multi-layer type)
L125	Optional RF LC filter/matching filter inductor (950 MHz) (wire wound or multi-layer type)
L132	RF balun/matching inductor. (wire wound or multi-layer type)
R171	Resistor for internal bias current reference
XTAL	26MHz - 27MHz crystal

Table 18: Overview of External Components (excluding supply decoupling capacitors)

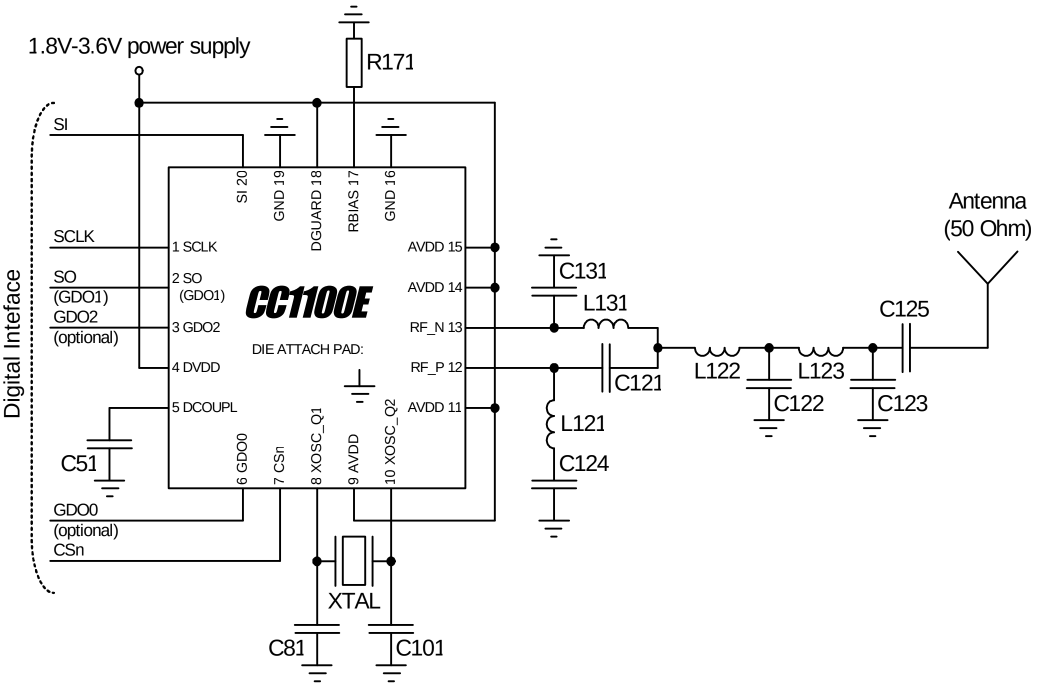


Figure 6: Typical Application and Evaluation Circuit 470 MHz (excluding supply decoupling capacitors)

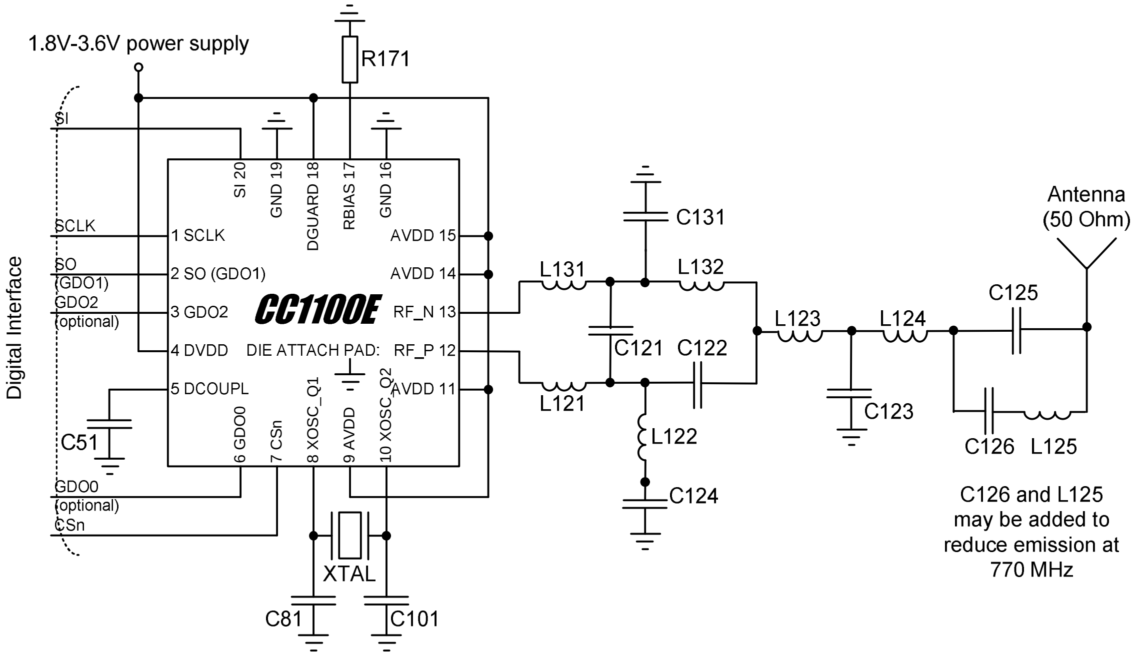


Figure 7: Typical Application and Evaluation Circuit 950 MHz (excluding supply decoupling capacitors)

Component	Value at 470MHz	Value at 950MHz	Manufacturer
C51	100 nF ± 10%, 0402 X5R		Murata GRM1555C series
C81	27 pF ± 5%, 0402 NP0		Murata GRM1555C series
C101	27 pF ± 5%, 0402 NP0		Murata GRM1555C series
C121	3.9 pF ± 0.25 pF, 0402 NP0	1.0 pF ± 0.25 pF, 0402 NP0	Murata GRM1555C series
C122	6.8 pF ± 5% pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0	Murata GRM1555C series
C123	5.6 pF ± 0.5 pF, 0402 NP0	2.7 pF ± 0.25 pF, 0402 NP0	Murata GRM1555C series
C124	.220 pF pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0	Murata GRM1555C series
C125	220 pF ± 5%, 0402 NP0	100 pF ± 5%, 0402 NP0 or 11 pF ± 5%, 0402 NP0 when part of optional filter	Murata GRM1555C series
C126		47 pF ± 5%, 0402 NP0	Murata GRM1555C series
C131	3.9 pF ± 0.25 pF, 0402 NP0	1.5 pF ± 0.25 pF, 0402 NP0	Murata GRM1555C series
L121	27 nH ± 5%, 0402 wire wound	12 nH ± 5%, 0402 wire wound	Murata LQW15 series
L122	22 nH ± 5%, 0402 wire wound	18 nH ± 5%, 0402 wire wound	Murata LQW15 series
L123	27 nH ± 5%, 0402 wire wound	12 nH ± 5%, 0402 wire wound	Murata LQW15 series
L124		12 nH ± 5%, 0402 wire wound	Murata LQW15 series
L125		2.7 nH ± 0.2nH, 0402 wire wound	Murata LQW15 series
L131	27 nH ± 5%, 0402 wire wound	12 nH ± 5%, 0402 wire wound	Murata LQW15 series
L132		18 nH ± 5%, 0402 wire wound	Murata LQW15 series
R171	56k Ω, 0402, 1%		Koa RK73 series
XTAL	26.0 MHz surface mount crystal		NDK, AT-41CD2

Table 19: Bill Of Materials for the Application Circuit

7.8 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias for good thermal performance and sufficiently low inductance to ground.

In the CC1100E EM reference designs ([3] and 0), 5 vias are placed inside the exposed die attached pad. These vias should be "tented" (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using "tented" vias reduces the solder paste coverage below

100%. See Figure 8 for top solder resist and top paste masks.

Each decoupling capacitor should be placed as close as possible to the supply pin it decouples. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the **CC1100E** supply pin. Supply power filtering is very important.

Each decoupling capacitor ground pad should be connected to the ground plane by separate vias. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary. Routing in the ground plane underneath the chip or the balun/RF matching circuit, or between the chip's ground vias and the decoupling capacitor's ground vias should be avoided. This improves the grounding and ensures the shortest possible current return path.

The external components should ideally be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Please note that components with different sizes than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A **CC1100E** DK Development Kit with a fully assembled **CC1100E** EM Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The schematic, BOM and layout Gerber files are all available from the TI website ([3] and 0).

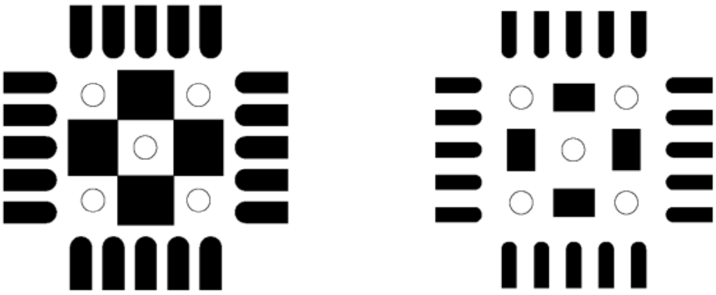


Figure 8: Left: Top Solder Resist Mask (Negative). Right: Top Paste Mask. Circles are Vias

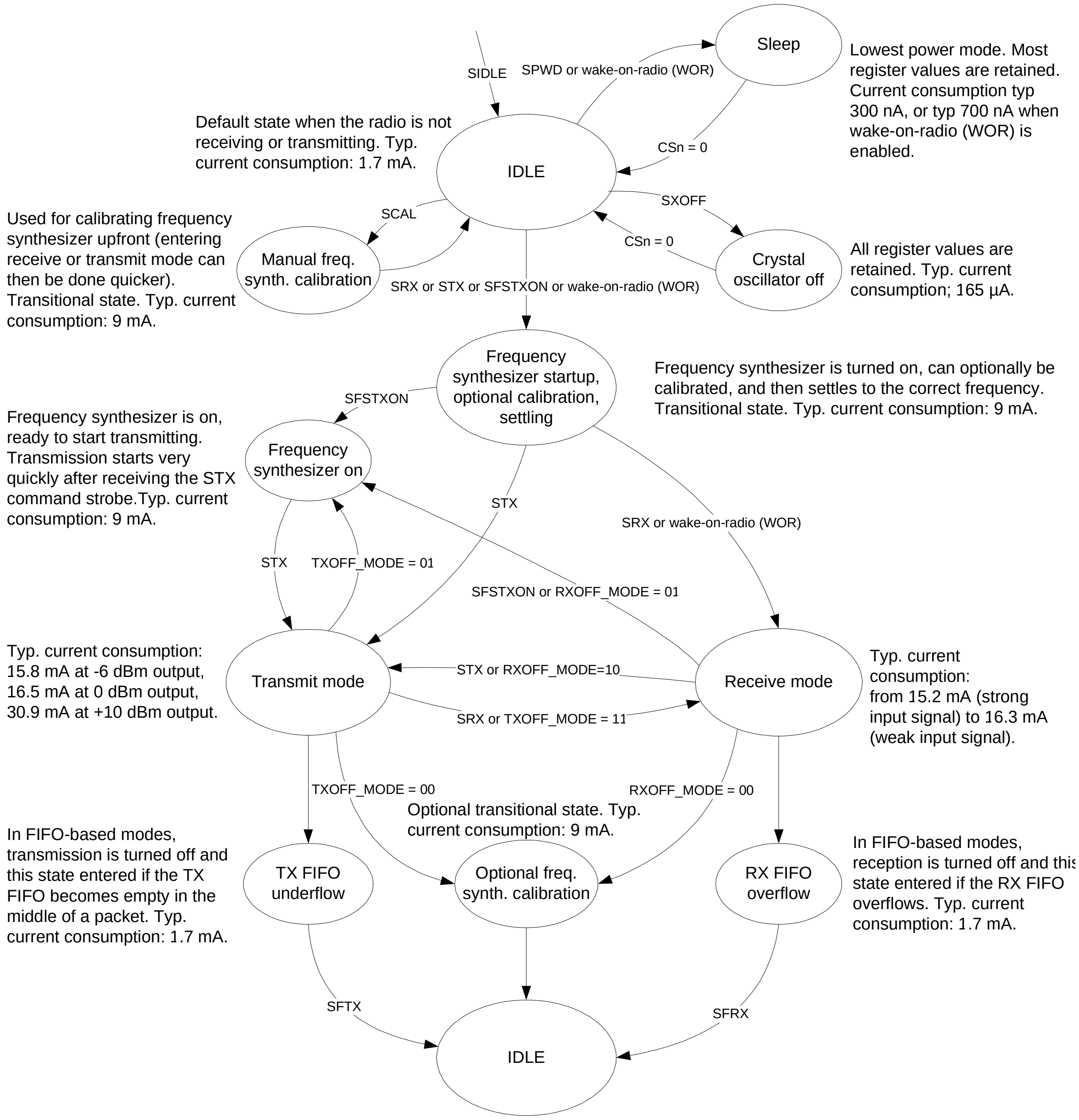
8 Configuration Overview

The **CC1100E** can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. See Section 10 below for more description of the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power-down
- Receive / transmit mode
- RF channel selection
- Data rate
- Modulation format
- RX channel filter bandwidth
- RF output power
- Data buffering with separate 64-byte receive and transmit FIFOs
- Packet radio hardware support
- Forward Error Correction (FEC) with interleaving
- Data whitening
- Wake-On-Radio (WOR)

Details of each configuration register can be found in Section 29, starting on page 59.

Figure 9 shows a simplified state diagram that explains the main **CC1100E** states together with typical usage and current consumption. For detailed information on controlling the **CC1100E** state machine, and a complete state diagram, see Section 19, starting on page 45.



Lowest power mode. Most register values are retained. Current consumption typ 300 nA, or typ 700 nA when wake-on-radio (WOR) is enabled.

Default state when the radio is not receiving or transmitting. Typ. current consumption: 1.7 mA.

Used for calibrating frequency synthesizer upfront (entering receive or transmit mode can then be done quicker). Transitional state. Typ. current consumption: 9 mA.

All register values are retained. Typ. current consumption; 165 µA.

Frequency synthesizer is turned on, can optionally be calibrated, and then settles to the correct frequency. Transitional state. Typ. current consumption: 9 mA.

Frequency synthesizer is on, ready to start transmitting. Transmission starts very quickly after receiving the STX command strobe.Typ. current consumption: 9 mA.

Typ. current consumption:
15.8 mA at -6 dBm output,
16.5 mA at 0 dBm output,
30.9 mA at +10 dBm output.

Typ. current consumption:
from 15.2 mA (strong input signal) to 16.3 mA (weak input signal).

Optional transitional state. Typ. current consumption: 9 mA.

In FIFO-based modes, transmission is turned off and this state entered if the TX FIFO becomes empty in the middle of a packet. Typ. current consumption: 1.7 mA.

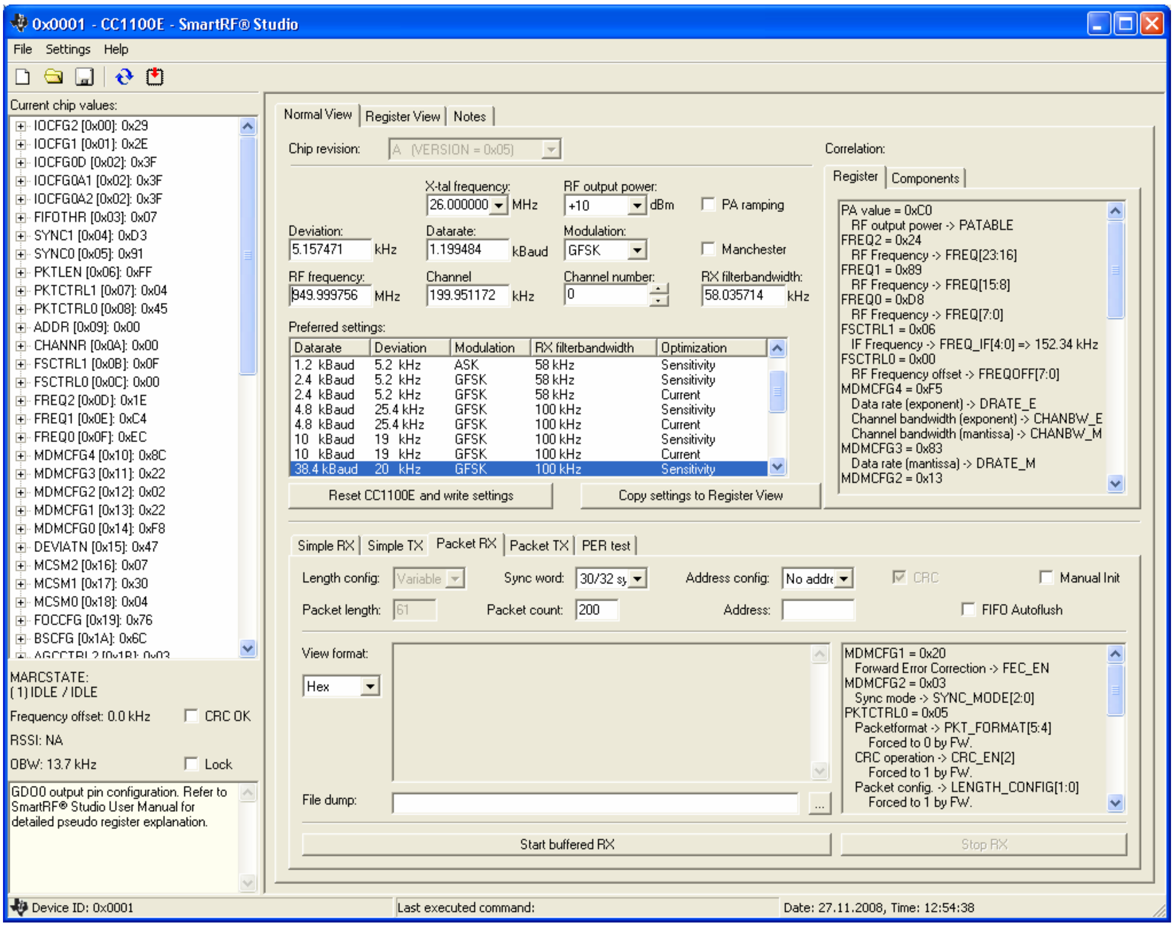
In FIFO-based modes, reception is turned off and thi state entered if the RX FIFO overflows. Typ. current consumption: 1.7 mA.

Figure 9: Simplified State Diagram, with Typical Current Consumption at 1.2 kBaud Data Rate and `MDMCFG2.DEM_DCFILT_OFF=1` (current optimized). Frequency Band = 955 MHz

9 Configuration Software

The **CC1100E** can be configured using the SmartRF® Studio software [8]. The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality. A screenshot of the SmartRF® Studio user interface for the **CC1100E** is shown in Figure 10.

After chip reset, all the registers have default values as shown in the tables in Section 29. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.



Current chip values:

```
IOCFG2 [0x00]: 0x29
IOCFG1 [0x01]: 0x2E
IOCFG0D [0x02]: 0x3F
IOCFG0A1 [0x02]: 0x3F
IOCFG0A2 [0x02]: 0x3F
FIFOTHR [0x03]: 0x07
SYNC1 [0x04]: 0xD3
SYNC0 [0x05]: 0x91
PKTLEN [0x06]: 0xFF
PKTCTRL1 [0x07]: 0x04
PKTCTRL0 [0x08]: 0x45
ADDR [0x09]: 0x00
CHANNR [0x0A]: 0x00
FSCTRL1 [0x0B]: 0x0F
FSCTRL0 [0x0C]: 0x00
FREQ2 [0x0D]: 0x1E
FREQ1 [0x0E]: 0xC4
FREQ0 [0x0F]: 0xEC
MDMCFG4 [0x10]: 0x8C
MDMCFG3 [0x11]: 0x22
MDMCFG2 [0x12]: 0x02
MDMCFG1 [0x13]: 0x22
MDMCFG0 [0x14]: 0xF8
DEVIATN [0x15]: 0x47
MCSM2 [0x16]: 0x07
MCSM1 [0x17]: 0x30
MCSM0 [0x18]: 0x04
FOCCFG [0x19]: 0x76
BSCFG [0x1A]: 0x6C
```

MARCSTATE:
(1) IDLE / IDLE

Frequency offset: 0.0 kHz ☐ CRC OK

RSSI: NA

OBW: 13.7 kHz ☐ Lock

GDO0 output pin configuration. Refer to SmartRF® Studio User Manual for detailed pseudo register explanation.

Chip revision: A (VERSION = 0x05)

X-tal frequency: 26.000000 MHz

RF output power: +10 dBm

☐ PA ramping

Deviation: 5.157471 kHz

Datarate: 1.199484 kBaud

Modulation: GFSK

☐ Manchester

RF frequency: 849.999756 MHz

Channel 199.951172 kHz

Channel number: 0

RX filterbandwidth: 58.035714 kHz

Preferred settings:

Datarate	Deviation	Modulation	RX filterbandwidth	Optimization
1.2 kBaud	5.2 kHz	ASK	58 kHz	Sensitivity
2.4 kBaud	5.2 kHz	GFSK	58 kHz	Sensitivity
2.4 kBaud	5.2 kHz	GFSK	58 kHz	Current
4.8 kBaud	25.4 kHz	GFSK	100 kHz	Sensitivity
4.8 kBaud	25.4 kHz	GFSK	100 kHz	Current
10 kBaud	19 kHz	GFSK	100 kHz	Sensitivity
10 kBaud	19 kHz	GFSK	100 kHz	Current
38.4 kBaud	20 kHz	GFSK	100 kHz	Sensitivity

```
PA value = 0xC0
  RF output power -> PATABLE
FREQ2 = 0x24
  RF Frequency -> FREQ[23:16]
FREQ1 = 0x89
  RF Frequency -> FREQ[15:8]
FREQ0 = 0xD8
  RF Frequency -> FREQ[7:0]
FSCTRL1 = 0x06
  IF Frequency -> FREQ_IF[4:0] => 152.34 kHz
FSCTRL0 = 0x00
  RF Frequency offset -> FREQOFF[7:0]
MDMCFG4 = 0xF5
  Data rate (exponent) -> DRATE_E
  Channel bandwidth (exponent) -> CHANBW_E
  Channel bandwidth (mantissa) -> CHANBW_M
MDMCFG3 = 0x83
  Data rate (mantissa) -> DRATE_M
MDMCFG2 = 0x13
```

Length config: Variable

Sync word: 30/32 sy

Address config: No addre

☑ CRC

☐ Manual Init

Packet length: 61

Packet count: 200

Address:

☐ FIFO Autoflush

View format: Hex

File dump:

```
MDMCFG1 = 0x20
  Forward Error Correction -> FEC_EN
MDMCFG2 = 0x03
  Sync mode -> SYNC_MODE[2:0]
PKTCTRL0 = 0x05
  Packetformat -> PKT_FORMAT[5:4]
    Forced to 0 by FW.
  CRC operation -> CRC_EN[2]
    Forced to 1 by FW.
  Packet config. -> LENGTH_CONFIG[1:0]
    Forced to 1 by FW.
```

Device ID: 0x0001

Last executed command:

Date: 27.11.2008, Time: 12:54:38

Figure 10: SmartRF® Studio [8] User Interface

10 4-wire Serial Configuration and Data Interface

The **CC1100E** is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where the **CC1100E** is the slave. This interface is also used to read and write buffered data. All transfers on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing an $R/\overline{W}$ bit, a burst access bit (B), and a 6-bit address (A_5 – A_0).

The CSn pin must be kept low during transfers on the SPI bus. If CSn goes high during the transfer of a header byte or during read/write from/to a register, the transfer will be cancelled. The timing for the address and data transfer on the SPI interface is shown in Figure 11 with reference to Table 20.

When CSn is pulled low, the MCU must wait until the **CC1100E** SO pin goes low before starting to transfer the header byte. This indicates that the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

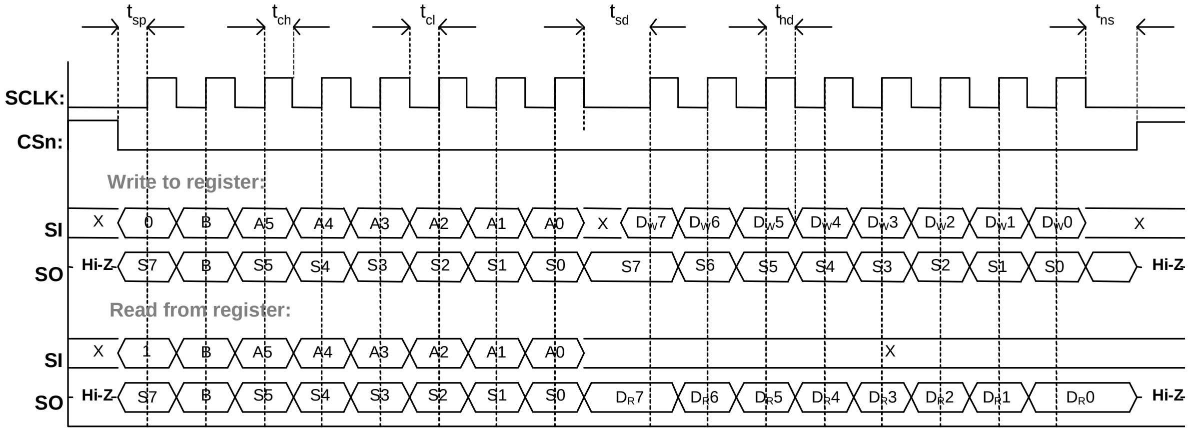


Figure 11: Configuration Registers Write and Read Operations

Parameter	Description	Min	Max	Units
f_{SCLK}	SCLK frequency 100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).	-	10	MHz
	SCLK frequency, single access No delay between address and data byte	-	9	
	SCLK frequency, burst access No delay between address and data byte, or between data bytes	-	6.5	
$t_{sp,pd}$	CSn low to positive edge on SCLK, in power-down mode	150	-	µs
t_{sp}	CSn low to positive edge on SCLK, in active mode	20	-	ns
t_{ch}	Clock high	50	-	ns
t_{cl}	Clock low	50	-	ns
t_{rise}	Clock rise time	-	5	ns
t_{fall}	Clock fall time	-	5	ns
t_{sd}	Setup data (negative SCLK edge) to positive edge on SCLK (t_{sd} applies between address and data bytes, and between data bytes) — Single access Burst access	55 76	- -	ns
t_{hd}	Hold data after positive edge on SCLK	20	-	ns
t_{ns}	Negative edge on SCLK to CSn high.	20	-	ns

Table 20: SPI Interface Timing Requirements

Note: The minimum $t_{sp,pd}$ figure in Table 20 can be used in cases where the user does not read the `CHIP_RDYn` signal. CSn low to positive edge on SCLK when the chip is woken from power-down depends on the start-up time of the crystal being used. The 150 µs in Table 20 is the crystal oscillator start-up time measured on CC1100E EM reference designs (0 and 0) using crystal AT-41CD2 from NDK.

10.1 Chip Status Byte

When the header byte, data byte, or command strobe is sent on the SPI interface, the chip status byte is sent by the **CC1100E** on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the `CHIP_RDYn` signal; this signal must go low before the first positive edge of SCLK. The `CHIP_RDYn` signal indicates that the crystal is running.

Bits 6, 5, and 4 comprise the `STATE` value. This value reflects the state of the chip. The XOSC and power to the digital core are on in the IDLE state, but all other modules are in power down. The frequency and channel configuration should only be updated when the chip is in this state. The RX state will be active when the chip is in the receive mode. Likewise, TX is active when the chip is transmitting.

The last four bits (3:0) in the status byte contains `FIFO_BYTES_AVAILABLE.` For read operations (the R/W;¯ bit in the header byte is set to 1), the `FIFO_BYTES_AVAILABLE` field contains the number of bytes available for reading from the RX FIFO. For write operations (the R/W;¯ bit in the header byte is set to 0), the `FIFO_BYTES_AVAILABLE` field contains the number of bytes that can be written to the TX FIFO. When `FIFO_BYTES_AVAILABLE=15`, 15 or more bytes are available/free.

Table 21 gives a status byte summary.

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>CHIP_RDYn</td><td>Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.</td></tr>
<tr><td>6:4</td><td>STATE[2:0]</td><td>Indicates the current main state machine mode
<table>
<tr><td>Value</td><td>State</td><td>Description</td></tr>
<tr><td>000</td><td>IDLE</td><td>IDLE state
(Also reported for some transitional states instead of SETTLING or CALIBRATE)</td></tr>
<tr><td>001</td><td>RX</td><td>Receive mode</td></tr>
<tr><td>010</td><td>TX</td><td>Transmit mode</td></tr>
<tr><td>011</td><td>FSTXON</td><td>Fast TX ready</td></tr>
<tr><td>100</td><td>CALIBRATE</td><td>Frequency synthesizer calibration is running</td></tr>
<tr><td>101</td><td>SETTLING</td><td>PLL is settling</td></tr>
<tr><td>110</td><td>RXFIFO_OVERFLOW</td><td>RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX</td></tr>
<tr><td>111</td><td>TXFIFO_UNDERFLOW</td><td>TX FIFO has underflowed. Acknowledge with SFTX</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>FIFO_BYTES_AVAILABLE[3:0]</td><td>The number of bytes available in the RX FIFO or free bytes in the TX FIFO</td></tr>
</table>

Table 21: Status Byte Summary

10.2 Register Access

The configuration registers on the **CC1100E** are located on SPI addresses from 0x00 to 0x2E. Table 39 on page 61 lists all configuration registers. It is highly recommended to use SmartRF® Studio [8] to generate optimum register settings. The detailed description of each register is found in Section 29.1 and 29.2, starting on page 64. All configuration registers can be both written to and read. The R/W;¯ bit controls if the register should be written to or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit (B) in the header byte. The address bits (A_5 – A_0) set the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30-0x3D, the burst bit is used to select between status registers when burst bit is one, and between command strobes when burst bit is zero. See more in Section 10.3 below. Because of this, burst access is not available for status registers and they must be accessed one at a time. The status registers can only be read.

10.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated by the radio hardware (e.g. `MARCSTATE` or `TXBYTES`), there is a small, but finite, probability that a single read from the register is corrupt. As an example, the probability of any single read from `TXBYTES` being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. Refer to the **CC1100E** Errata Note [5] for more details.

10.4 Command Strobes

Command Strobes may be viewed as single byte instructions to the **CC1100E**. By addressing a command strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable receive mode, enable wake-on-radio etc. The 13 command strobes are listed in Table 38 on page 60.

> **Note:** An SIDLE strobe will clear all pending command strobes until IDLE state is reached. This means that if for example an SIDLE strobe is issued while the radio is in RX state, any other command strobes issued before the radio reaches IDLE state will be ignored.

The command strobe registers are accessed by transferring a single header byte (no data is being transferred). That is, only the R/W;¯ bit, the burst access bit (set to 0), and the six address bits (in the range 0x30 through 0x3D) are written. The R/W;¯ bit can be either one or zero and will determine how the `FIFO_BYTES_AVAILABLE` field in the status byte should be interpreted.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling CSn high. However, if an `SRES` strobe is being issued, one will have to wait for SO to go low again before the next header byte can be issued as shown in Figure 12. The command strobes are executed immediately, with the exception of the `SPWD` and the `SXOFF` strobes that are executed when CSn goes high.

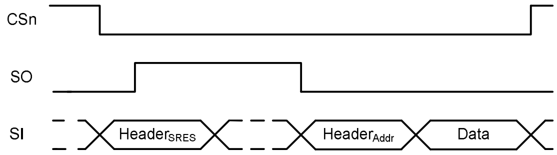


Figure 12: SRES Command Strobe

10.5 FIFO Access

The 64-byte TX FIFO and the 64-byte RX FIFO are accessed through the 0x3F address. When the R/W;¯ bit is zero, the TX FIFO is accessed, and the RX FIFO is accessed when the R/W;¯ bit is one.

The TX FIFO is write-only, while the RX FIFO is read-only.

The burst bit is used to determine if the FIFO access is a single byte access or a burst access. The single byte access method expects a header byte with the burst bit set to zero and one data byte. After the data byte, a new header byte is expected; hence, CSn can remain low. The burst access method expects one header byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the FIFOs:

- 0x3F: Single byte access to TX FIFO
- 0x7F: Burst access to TX FIFO
- 0xBF: Single byte access to RX FIFO
- 0xFF: Burst access to RX FIFO

When writing to the TX FIFO, the status byte (see Section 10.1) is output on SO for each new data byte as shown in Figure 11. This status byte can be used to detect TX FIFO underflow while writing data to the TX FIFO. Note that the status byte contains the number of bytes free before writing the byte in progress to the TX FIFO. When the last byte that fits in the TX FIFO is transmitted on SI, the status byte received concurrently on SO will indicate that one byte is free in the TX FIFO.

The TX FIFO may be flushed by issuing a `SFTX` command strobe. Similarly, a `SFRX` command strobe will flush the RX FIFO. A `SFTX` or `SFRX` command strobe can only be issued in the IDLE, TXFIFO_UNDERFLOW, or RXFIFO_OVERFLOW states. Both FIFOs are flushed when going to the SLEEP state.

Figure 13 gives a brief overview of different register access types possible.

10.6 PATABLE Access

The `0x3E` address is used to access the `PATABLE`, which is used for selecting PA power control settings. The SPI expects up to eight data bytes after receiving the address. By programming the `PATABLE`, controlled PA power ramp-up and ramp-down can be achieved, as well as ASK modulation shaping for reduced bandwidth. See SmartRF® Studio [8] for recommended shaping / PA ramping sequences. See also Section 24 on page 52 for details on output power programming.

The `PATABLE` is an 8-byte table that defines the PA control settings to use for each of the eight PA power values (selected by the 3-bit value `FREND0.PA_POWER`). The table is written and read from the lowest setting (0) to the highest (7), one byte at a time. An index counter is used to control the access to the table. This counter is incremented each time a byte is read or written to the table, and set to the lowest index when CSn is high. When the highest value is reached the counter restarts at zero.

The access to the `PATABLE` is either single byte or burst access depending on the burst bit. When using burst access the index counter will count up; when reaching 7 the counter will restart at 0. The R/W;¯ bit controls whether the access is a read or a write access.

If one byte is written to the `PATABLE` and this value is to be read out, CSn must be set high before the read access in order to set the index counter back to zero.

Note that the content of the `PATABLE` is lost when entering the SLEEP state, except for the first byte (index 0).

Please referr to Design Note DN501 [17] for more information

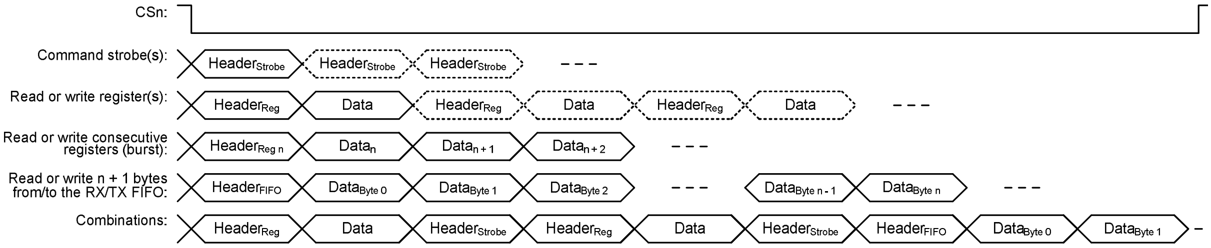


Figure 13: Register Access Types

11 Microcontroller Interface and Pin Configuration

In a typical system, the **CC1100E** will interface to a microcontroller. This microcontroller must be able to:

- Program the **CC1100E** into different modes
- Read and write buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn)

11.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). The SPI is described in Section 10 on page 25.

11.2 General Control and Status Pins

The **CC1100E** has two dedicated configurable pins (GDO0 and GDO2) and one shared pin (GDO1) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See Section 26 page 54 for more details on the signals that can be programmed.

GDO1 is shared with the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options, the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

In the synchronous and asynchronous serial modes, the GDO0 pin is used as a serial TX data input pin while in transmit mode.

The GDO0 pin can also be used for an on-chip analog temperature sensor. By measuring the voltage on the GDO0 pin with an external ADC, the temperature can be calculated. Specifications for the temperature sensor are found in Section 4.7 on page 15. With default `PTEST` register setting (0x7F), the temperature sensor output is only available if the frequency synthesizer is enabled (e.g. the MANCAL, FSTXON, RX, and TX states). It is necessary to write 0xBF to the `PTEST` register to use the analog temperature sensor in the IDLE state. Before leaving the IDLE state, the `PTEST` register should be restored to its default value (0x7F).

11.3 Optional Radio Control Feature

The **CC1100E** has an optional way of controlling the radio by reusing SI, SCLK, and CSn from the SPI interface. This feature allows for a simple three-pin control of the major states of the radio: SLEEP, IDLE, RX, and TX. This optional functionality is enabled with the `MCSM0.PIN_CTRL_EN` configuration bit.

State changes are commanded as follows:

- If CSn is high, the SI and SCLK are set to the desired state according to Table 22.
- If CSn goes low, the state of SI and SCLK is latched and a command strobe is generated internally according to the pin configuration.

It is only possible to change state with the latter functionality. That means that for instance RX will not be restarted if SI and SCLK are set to RX and CSn toggles. When CSn is low the SI and SCLK has normal SPI functionality.

All pin control command strobes are executed immediately except the `SPWD` strobe. The `SPWD` strobe is delayed until CSn goes high.

CSn	SCLK	SI	Function
1	X	X	Chip unaffected by SCLK/`SI`
↓	0	0	Generates `SPWD` strobe
↓	0	1	Generates `STX` strobe
↓	1	0	Generates `SIDLE` strobe
↓	1	1	Generates `SRX` strobe
0	SPI mode	SPI mode	SPI mode (wakes up into IDLE if in SLEEP/XOFF)

Table 22: Optional Pin Control Coding

12 Data Rate Programming

The data rate used when transmitting, or the data rate expected in receive is programmed by the `MDMCFG3.DRATE_M` and the `MDMCFG4.DRATE_E` configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE\_E = \left\lfloor \log_2 \left(\frac{R_{DATA} \cdot 2^{20}}{f_{XOSC}} \right) \right\rfloor$$

$$DRATE\_M = \frac{R_{DATA} \cdot 2^{28}}{f_{XOSC} \cdot 2^{DRATE\_E}} - 256$$

If `DRATE_M` is rounded to the nearest integer and becomes 256, increment `DRATE_E` and use `DRATE_M` = 0.

The data rate can be set from 0.8 kBaud to 500 kBaud with the minimum step size according to Table 23 below.

Min Data Rate [kBaud]	Typical Data Rate [kBaud]	Max Data Rate [kBaud]	Data rate Step Size [kBaud]
0.8	1.2 / 2.4	3.17	0.0062
3.17	4.8	6.35	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.4	0.0496
25.4	38.4	50.8	0.0992
50.8	76.8	101.6	0.1984
101.6	153.6	203.1	0.3967
203.1	250	406.3	0.7935
406.3	500	500	1.5869

Table 23: Data Rate Step Size

13 Receiver Channel Filter Bandwidth

In order to meet different channel width requirements, the receiver channel filter is programmable. The `MDMCFG4.CHANBW_E` and `MDMCFG4.CHANBW_M` configuration registers control the receiver channel filter bandwidth, which scales with the crystal oscillator frequency.

The following formula gives the relation between the register settings and the channel filter bandwidth:

$$BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$$

Table 24 lists the channel filter bandwidths supported by the **CC1100E**.

For best performance, the channel filter bandwidth should be selected so that the signal bandwidth occupies at most 80% of the channel filter bandwidth. The channel centre tolerance due to crystal inaccuracy should also be subtracted from the channel filter bandwidth. The following example illustrates this:

With the channel filter bandwidth set to 500 kHz, the signal should stay within 80% of 500 kHz, which is 400 kHz. Assuming 955 MHz frequency and ±20 ppm frequency uncertainty for both the transmitting device and the receiving device, the total frequency uncertainty is ±40 ppm of 955 MHz, which is ±38.2 kHz. If the whole transmitted signal bandwidth is to be received within 400 kHz, the transmitted signal bandwidth should be maximum 400 kHz – 2·38.2 kHz, which is 323.6 kHz.

By compensating for a frequency offset between the transmitter and the receiver, the filter bandwidth can be reduced and the sensitivity can be improved, see more in DN005 [16] and in Section 14.1.

MDMCFG4. CHANBW_M	MDMCFG4.CHANBW_E			
	00	**01**	**10**	**11**
00	812	406	203	102
01	650	325	162	81
10	541	270	135	68
11	464	232	116	58

Table 24: Channel Filter Bandwidths [kHz] (assuming a 26 MHz crystal)

14 Demodulator, Symbol Synchronizer, and Data Decision

The **CC1100E** contains an advanced and highly configurable demodulator. Channel filtering and frequency offset compensation is performed digitally. To generate the RSSI level (see Section 17.3 for more information), the signal level in the channel is estimated. Data filtering is also included for enhanced performance.

14.1 Frequency Offset Compensation

The **CC1100E** has a very fine frequency resolution (see Table 13). This feature can be used to compensate for frequency offset and drift.

When using 2-FSK, GFSK, or MSK modulation, the demodulator will compensate for the offset between the transmitter and receiver frequency within certain limits, by estimating the centre of the received data. The frequency offset compensation configuration is controlled from the FOCCFG register. By compensating for a large frequency offset between the transmitter and the receiver, the sensitivity can be improved, see DN005 [16].

The tracking range of the algorithm is selectable as fractions of the channel bandwidth with the `FOCCFG.FOC_LIMIT` configuration register.

If the `FOCCFG.FOC_BS_CS_GATE` bit is set, the offset compensator will freeze until carrier sense asserts. This may be useful when the radio is in RX for long periods with no traffic, since the algorithm may drift to the boundaries when trying to track noise.

The tracking loop has two gain factors, which affects the settling time and noise sensitivity of the algorithm. `FOCCFG.FOC_PRE_K` sets the gain before the sync word is detected, and `FOCCFG.FOC_POST_K` selects the gain after the sync word has been found.

Note: Frequency offset compensation is not supported for ASK or OOK modulation.

The estimated frequency offset value is available in the `FREQEST` status register. This can be used for permanent frequency offset compensation. By writing the value from `FREQEST` into `FSCTRL0.FREQOFF`, the frequency synthesizer will automatically be adjusted according to the estimated frequency offset. More details regarding this permanent frequency compensation algorithm can be found in DN015 [12].

14.2 Bit Synchronization

The bit synchronization algorithm extracts the clock from the incoming symbols. The algorithm requires that the expected data rate is programmed as described in Section 12 on page 31. Re-synchronization is performed continuously to adjust for error in the incoming symbol rate.

14.3 Byte Synchronization

Byte synchronization is achieved by a continuous sync word search. The sync word is a 16 bit configurable field (can be repeated to get a 32 bit) that is automatically inserted at the start of the packet by the modulator in transmit mode. The MSB in the sync word is sent first. The demodulator uses this field to find the byte boundaries in the stream of bits. The sync word will also function as a system identifier; since only packets with the correct predefined sync word will be received if the sync word detection in RX is enabled in register `MDMCFG2` (see Section 17.1). The sync word detector correlates against the user-configured 16 or 32 bit sync word. The correlation threshold can be set to 15/16, 16/16, or 30/32 bits match. The sync word can be further qualified using the preamble quality indicator mechanism described below and/or a carrier sense condition. The sync word is configured through the `SYNC1` and `SYNC0` registers.

In order to make false detections of sync words less likely, a mechanism called preamble quality indication (PQI) can be used to qualify the sync word. A threshold value for the preamble quality must be exceeded in order for a detected sync word to be accepted. See Section 17.2 on page 39 for more details.

15 Packet Handling Hardware Support

The **CC1100E** has built-in hardware support for packet oriented radio protocols.

In transmit mode, the packet handler can be configured to add the following elements to the packet stored in the TX FIFO:

- A programmable number of preamble bytes
- A two byte synchronization (sync) word. Can be duplicated to give a 4-byte sync word (recommended). It is not possible to only insert preamble or only insert a sync word
- A CRC checksum computed over the data field.

The recommended setting is 4-byte preamble and 4-byte sync word, except for 500 kBaud data rate where the recommended preamble length is 8 bytes. In addition, the following can be implemented on the data field and the optional 2-byte CRC checksum:

- Whitening of the data with a PN9 sequence
- Forward Error Correction (FEC) by the use of interleaving and coding of the data (convolutional coding)

In receive mode, the packet handling support will de-construct the data packet by implementing the following (if enabled):

- Preamble detection
- Sync word detection
- CRC computation and CRC check
- One byte address check
- Packet length check (length byte checked against a programmable maximum length)
- De-whitening
- De-interleaving and decoding

Optionally, two status bytes (see Table 25 and Table 26) with RSSI value, Link Quality Indication, and CRC status can be appended in the RX FIFO.

Bit	Field Name	Description
7:0	RSSI	RSSI value

Table 25: Received Packet Status Byte 1 (first byte appended after the data)

Bit	Field Name	Description
7	CRC_OK	1: CRC for received data OK (or CRC disabled) 0: CRC error in received data
6:0	LQI	Indicating the link quality

Table 26: Received Packet Status Byte 2 (second byte appended after the data)

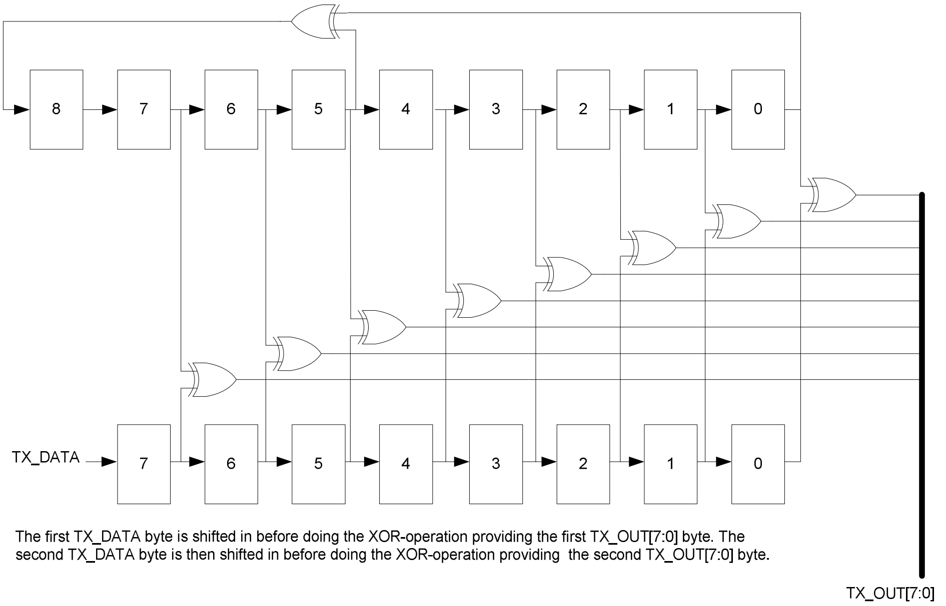
Note: Register fields that control the packet handling features should only be altered when **CC1100E** is in the IDLE state.

15.1 Data Whitening

From a radio perspective, the ideal over the air data are random and DC free. This results in the smoothest power distribution over the occupied bandwidth. This also gives the regulation loops in the receiver uniform operation conditions (no data dependencies).

Real data often contain long sequences of zeros and ones. In these cases, performance can be improved by whitening the data before transmitting, and de-whitening the data in the receiver.

With the **CC1100E**, this can be done automatically. By setting `PKTCTRL0.WHITE_DATA=1`, all data, except the preamble and the sync word will be XOR-ed with a 9-bit pseudo-random (PN9) sequence before being transmitted. This is shown in Figure 14. At the receiver end, the data are XOR-ed with the same pseudo-random sequence. In this way, the whitening is reversed, and the original data appear in the receiver. The PN9 sequence is initialized to all 1's.



The first TX_DATA byte is shifted in before doing the XOR-operation providing the first TX_OUT[7:0] byte. The second TX_DATA byte is then shifted in before doing the XOR-operation providing the second TX_OUT[7:0] byte.

Figure 14: Data Whitening in TX Mode

15.2 Packet Format

The format of the data packet can be configured and consists of the following items (see Figure 15):

- Preamble
- Synchronization word
- Optional length byte
- Optional address byte
- Payload
- Optional 2 byte CRC

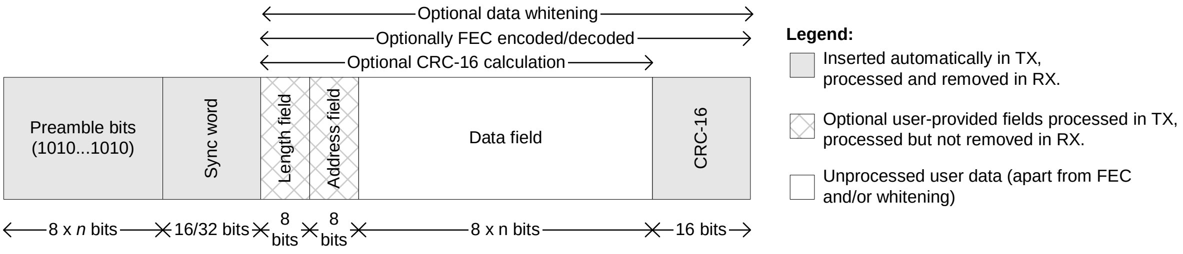


Figure 15: Packet Format

The preamble pattern is an alternating sequence of ones and zeros (10101010…). The minimum length of the preamble is programmable through the value of `MDMCFG1.NUM_PREAMBLE`. When enabling TX, the modulator will start transmitting the preamble. When the programmed number of preamble bytes has been transmitted, the modulator will send the sync word and then data from the TX FIFO if data is available. If the TX FIFO is empty, the modulator will continue to send preamble bytes until the first byte is written to the TX FIFO. The modulator will then send the sync word and then the data bytes.

The synchronization word is a two-byte value set in the `SYNC1` and `SYNC0` registers. The sync word provides byte synchronization of the incoming packet. A one-byte sync word can be emulated by setting the `SYNC1` value to the preamble pattern. It is also possible to emulate a 32 bit sync word by setting `MDMCFG2.SYNC_MODE` to 3 or 7. The sync word will then be repeated twice.

The **CC1100E** supports both constant packet length protocols and variable length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting `PKTCTRL0.LENGTH_CONFIG=0`. The desired packet length is set by the `PKTLEN` register.

In variable packet length mode, `PKTCTRL0.LENGTH_CONFIG=1`, the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional CRC. The `PKTLEN` register is used to set the maximum packet length allowed in RX. Any packet received with a length byte with a value greater than `PKTLEN` will be discarded.

With `PKTCTRL0.LENGTH_CONFIG=2`, the packet length is set to infinite and transmission and reception will continue until turned off manually. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by the **CC1100E**. One should make sure that TX mode is not turned off during the transmission of the first half of any byte. Refer to the **CC1100E** Errata Note [5] for more details.

Note: The minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

15.2.1 Arbitrary Length Field Configuration

The packet length register, `PKTLEN`, can be reprogrammed during receive and transmit. In combination with fixed packet length mode (`PKTCTRL0.LENGTH_CONFIG=0`), this opens the possibility to have a different length field configuration than supported for variable length packets (in variable packet length mode the length byte is the first byte after the sync word). At the start of reception, the packet length is set to a large value. The MCU reads out enough bytes to interpret the length field in the packet. Then the `PKTLEN` value is set according to this value. The end of packet will occur when the byte counter in the packet handler is equal to the `PKTLEN` register. Thus, the MCU must be able to program the correct length, before the internal counter reaches the packet length.

15.2.2 Packet Length > 255

The packet automation control register, `PKTCTRL0`, can be reprogrammed during TX and RX. This opens the possibility to transmit and receive packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite packet length mode (`PKTCTRL0.LENGTH_CONFIG=2`) must be active. On the TX side, the `PKTLEN` register is set to mod (length, 256). On the RX side the MCU reads out enough bytes to interpret the length field in the packet and sets the `PKTLEN` register to mod (length, 256). When less than 256 bytes remains of the packet, the MCU disables infinite packet length mode and activates fixed packet length mode. When the internal byte counter reaches the `PKTLEN` value, the transmission or reception ends (the radio enters the state determined by `TXOFF_MODE` or `RXOFF_MODE`). Automatic CRC appending/checking can also be used (by setting `PKTCTRL0.CRC_EN=1`).

When for example a 600-byte packet is to be transmitted, the MCU should do the following (see also Figure 16)

- Set `PKTCTRL0.LENGTH_CONFIG=2`.
- Pre-program the `PKTLEN` register to mod (600, 256) = 88.
- Transmit at least 345 bytes (600 - 255), for example by filling the 64-byte TX FIFO six times (384 bytes transmitted).
- Set `PKTCTRL0.LENGTH_CONFIG=0`.
- The transmission ends when the packet counter reaches 88. A total of 600 bytes are transmitted.

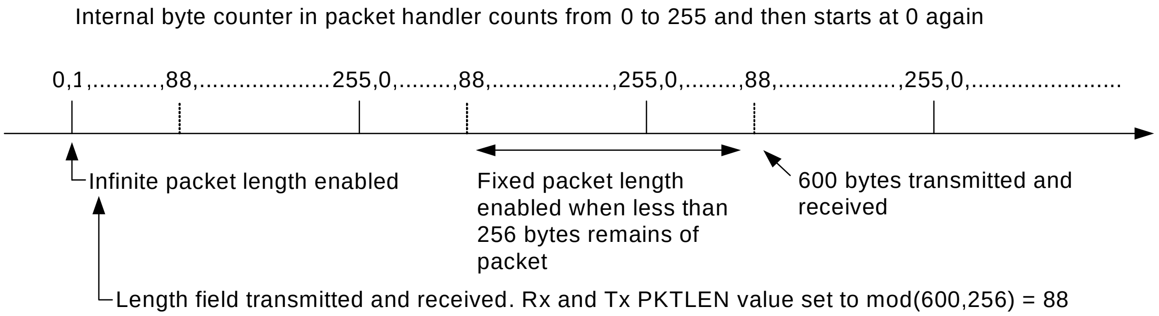


Figure 16: Packet Length > 255

15.3 Packet Filtering in Receive Mode

The **CC1100E** supports three different types of packet-filtering; address filtering, maximum length filtering, and CRC filtering.

15.3.1 Address Filtering

Setting `PKTCTRL1.ADR_CHK` to any other value than zero enables the packet address filter. The packet handler engine will compare the destination address byte in the packet with the programmed node address in the `ADDR` register and the 0x00 broadcast address when `PKTCTRL1.ADR_CHK=10` or both the 0x00 and 0xFF broadcast addresses when `PKTCTRL1.ADR_CHK=11`. If the received address matches a valid address, the packet is received and written into the RX FIFO. If the address match fails, the packet is discarded and receive mode restarted (regardless of the `MCSM1.RXOFF_MODE` setting).

If the received address matches a valid address when using infinite packet length mode and address filtering is enabled, 0xFF will be written into the RX FIFO followed by the address byte and then the payload data.

15.3.2 Maximum Length Filtering

In variable packet length mode, `PKTCTRL0.LENGTH_CONFIG=1`, the `PKTLEN.PACKET_LENGTH` register value is used to set the maximum allowed packet length. If the received length byte has a larger value than this, the packet is discarded and receive mode restarted (regardless of the `MCSM1.RXOFF_MODE` setting).

15.3.3 CRC Filtering

The filtering of a packet when CRC check fails is enabled by setting `PKTCTRL1.CRC_AUTOFLUSH=1`. The CRC auto flush function will flush the entire RX FIFO if the CRC check fails. After auto flushing the RX FIFO, the next state depends on the `MCSM1.RXOFF_MODE` setting.

When using the auto flush function, the maximum packet length is 63 bytes in variable packet length mode and 64 bytes in fixed packet length mode. Note that when `PKTCTRL1.APPEND_STATUS` is enabled, the maximum allowed packet length is reduced by two bytes in order to make room in the RX FIFO for the two status bytes appended at the end of the packet. Since the entire RX FIFO is flushed when the CRC check fails, the previously received packet must be read out of the FIFO before receiving the current packet. The MCU must not read from the current packet until the CRC has been checked as OK.

15.4 Packet Handling in Transmit Mode

The payload that is to be transmitted must be written into the TX FIFO. The first byte written must be the length byte when variable packet length is enabled. The length byte has a value equal to the payload of the packet (including the optional address byte). If address recognition is enabled on the receiver, the second byte written to the TX FIFO must be the address byte.

If fixed packet length is enabled, the first byte written to the TX FIFO should be the address (assuming the receiver uses address recognition).

The modulator will first send the programmed number of preamble bytes. If data is available in the TX FIFO, the modulator will send the two-byte (optionally 4-byte) sync word followed by the payload in the TX FIFO. If CRC is enabled, the checksum is calculated over all the data pulled from the TX FIFO, and the result is sent as two extra bytes following the payload data. If the TX FIFO runs empty before the complete packet has been transmitted, the radio will enter TXFIFO_UNDERFLOW state. The only way to exit this state is by issuing an SFTX strobe. Writing to the TX FIFO after it has underflowed will not restart TX mode.

If whitening is enabled, everything following the sync words will be whitened. This is done before the optional FEC/Interleave stage. Whitening is enabled by setting `PKTCTRL0.WHITE_DATA=1`.

If FEC/Interleaving is enabled, everything following the sync words will be scrambled by the interleave and FEC encoded before being modulated. FEC is enabled by setting `MDMCFG1.FEC_EN=1`.

15.5 Packet Handling in Receive Mode

In receive mode, the demodulator and packet handler will search for a valid preamble and the sync word. When found, the demodulator has obtained both bit and byte synchronism and will receive the first payload byte.

If FEC/Interleaving is enabled, the FEC decoder will start to decode the first payload byte. The interleaver will de-scramble the bits before any other processing is done to the data.

If whitening is enabled, the data will be de-whitened at this stage.

When variable packet length mode is enabled, the first byte is the length byte. The packet handler stores this value as the packet length and receives the number of bytes indicated by the length byte. If fixed packet length mode is used, the packet handler will accept the programmed number of bytes.

Next, the packet handler optionally checks the address and only continues the reception if the address matches. If automatic CRC check is enabled, the packet handler computes CRC and matches it with the appended CRC checksum.

At the end of the payload, the packet handler will optionally write two extra packet status bytes (see Table 25 and Table 26) that contain CRC status, link quality indication, and RSSI value.

15.6 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been received/transmitted. Additionally, for packets longer than 64 bytes, the RX FIFO needs to be read while in RX and the TX FIFO needs to be refilled while in TX. This means that the MCU needs to know the number of bytes that can be read from or written to the RX FIFO and TX FIFO respectively. There are two possible solutions to get the necessary status information:

a) Interrupt Driven Solution

The GDO pins can be used in both RX and TX to give an interrupt when a sync word has been received/transmitted or when a complete packet has been received/transmitted by setting `IOCFGx.GDOx_CFG=0x06`. In addition, there are two configurations for the `IOCFGx.GDOx_CFG` register that can be used as an interrupt source to provide information on how many bytes are in the RX FIFO and TX FIFO respectively. The `IOCFGx.GDOx_CFG=0x00` and the `IOCFGx.GDOx_CFG=0x01` configurations are associated with the RX FIFO while the `IOCFGx.GDOx_CFG=0x02` and the `IOCFGx.GDOx_CFG=0x03` configurations are associated with the TX FIFO. See Table 36 for more information.

b) SPI Polling

The `PKTSTATUS` register can be polled at a given rate to get information about the current GDO2 and GDO0 values respectively. The `RXBYTES` and `TXBYTES` registers can be polled at a given rate to get information about the number of bytes in the RX FIFO and TX FIFO respectively. Alternatively, the number of bytes in the RX FIFO and TX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus.

It is recommended to employ an interrupt driven solution since high rate SPI polling reduces the RX sensitivity. Furthermore, as explained in Section 10.3 and the **CC1100E** Errata Note [5], when using SPI polling, there is a small, but finite, probability that a single read from registers `PKTSTATUS` , `RXBYTES` and `TXBYTES` is being corrupt. The same is the case when reading the chip status byte.

Refer to the TI website for SW examples ([9] and [10]).

16 Modulation Formats

The **CC1100E** supports amplitude, frequency, and phase shift modulation formats. The desired modulation format is set in the `MDMCFG2.MOD_FORMAT` register.

Optionally, the data stream can be Manchester coded by the modulator and decoded by the demodulator. This option is enabled by setting `MDMCFG2.MANCHESTER_EN=1`.

Note: Manchester encoding is not supported at the same time as using the FEC/Interleaver option or when using MSK modulation.

16.1 Frequency Shift Keying

The **CC1100E** has the possibility to use Gaussian shaped 2-FSK (GFSK). The 2-FSK signal is then shaped by a Gaussian filter with BT = 1, producing a GFSK modulated signal. This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth.

In ‘true’ 2-FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift ‘softer’, the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

When 2-FSK/GFSK modulation is used, the `DEVIATN` register specifies the expected frequency deviation of incoming signals in RX and should be the same as the TX deviation for demodulation to be performed reliably and robustly.

The frequency deviation is programmed with the `DEVIATION_M` and `DEVIATION_E` values in the `DEVIATN` register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$$

The symbol encoding is shown in Table 27.

Format	Symbol	Coding
2-FSK/GFSK	‘0’	– Deviation
	‘1’	+ Deviation

Table 27: Symbol Encoding for 2-FSK/GFSK Modulation

16.2 Minimum Shift Keying

When using MSK[1], the complete transmission (preamble, sync word, and payload) will be MSK modulated.

Phase shifts are performed with a constant transition time. The fraction of a symbol period used to change the phase can be modified with the `DEVIATN.DEVIATION_M` setting. This is equivalent to changing the shaping of the symbol. The `DEVIATN` register setting has no effect in RX when using MSK.

When using MSK, Manchester encoding/decoding should be disabled by setting `MDMCFG2` MANCHESTER_EN = 0

The MSK modulation format implemented in the **CC1100E** inverts the sync word and data compared to e.g. signal generators.

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[1] Identical to offset QPSK with half-sine shaping (data coding may differ).

16.3 Amplitude Modulation

The **CC1100E** supports two different forms of amplitude modulation: On-Off Keying (OOK) and Amplitude Shift Keying (ASK).

OOK modulation simply turns the PA on or off to modulate ones and zeros respectively.

The ASK variant supported by the **CC1100E** allows programming of the modulation depth (the difference between 1 and 0), and shaping of the pulse amplitude. Pulse shaping produces a more bandwidth constrained output spectrum.

When using OOK/ASK, the AGC settings from the SmartRF® Studio [8] preferred FSK/MSK settings are not optimum. DN022 [15] give guidelines on how to find optimum OOK/ASK settings from the preferred settings in SmartRF® Studio [8]. The `DEVIATN` register setting has no effect in either TX or RX when using OOK/ASK.

17 Received Signal Qualifiers and Link Quality Information

The **CC1100E** has several qualifiers that can be used to increase the likelihood that a valid sync word is detected:

- Sync Word Qualifier
- Preamble Quality Threshold
- RSSI
- Carrier Sense
- Clear Channel Assessment
- Link Quality Indicator

17.1 Sync Word Qualifier

If sync word detection in RX is enabled in the `MDMCFG2` register, the **CC1100E** will not start filling the RX FIFO and perform the packet filtering described in Section 15.3 before a valid sync word has been detected. The sync word qualifier mode is set by `MDMCFG2.SYNC_MODE` and is summarized in Table 28. Carrier sense in Table 28 is described in Section 17.4.

MDMCFG2. SYNC_MODE	Sync Word Qualifier Mode
000	No preamble/sync
001	15/16 sync word bits detected
010	16/16 sync word bits detected
011	30/32 sync word bits detected
100	No preamble/sync + carrier sense above threshold
101	15/16 + carrier sense above threshold
110	16/16 + carrier sense above threshold
111	30/32 + carrier sense above threshold

Table 28: Sync Word Qualifier Mode

17.2 Preamble Quality Threshold (PQT)

The Preamble Quality Threshold (PQT) sync word qualifier adds the requirement that the received sync word must be preceded with a preamble with a quality above the programmed threshold.

Another use of the preamble quality threshold is as a qualifier for the optional RX termination timer. See Section 19.7 on page 49 for details.

The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by eight each time a bit is received that is the same as the last bit.

The threshold is configured with the register field `PKTCTRL1.PQT`. A threshold of 4·`PQT` for this counter is used to gate sync word detection. By setting the value to zero, the preamble quality qualifier of the sync word is disabled.

A “Preamble Quality Reached” signal can be observed on one of the GDO pins by setting `IOCFGx.GDOx_CFG=8`. It is also possible to determine if preamble quality is reached by checking the `PQT_REACHED` bit in the `PKTSTATUS` register. This signal / bit asserts when the received signal exceeds the PQT.

17.3 RSSI

The RSSI value is an estimate of the signal power level in the chosen channel. This value is based on the current gain setting in the RX chain and the measured signal level in the channel.

In RX mode, the RSSI value can be read continuously from the `RSSI` status register until the demodulator detects a sync word (when sync word detection is enabled). At that point the RSSI readout value is frozen until the next time the chip enters the RX state.

Note: It takes some time from the radio enters RX mode until a valid RSSI value is present in the `RSSI` register. Please see DN505 [13] for details on how the RSSI response time can be estimated.

The RSSI value is given in dBm with a ½ dB resolution. The RSSI update rate, f_{RSSI}, depends on the receiver filter bandwidth ($BW_{channel}$ is defined in Section 13) and `AGCCTRL0.FILTER_LENGTH`.

$$f_{RSSI} = \frac{2 \cdot BW_{channel}}{8 \cdot 2^{FILTER\_LENGTH}}$$

If `PKTCTRL1.APPEND_STATUS` is enabled, the last RSSI value of the packet is automatically added to the first byte appended after the payload.

The RSSI value read from the `RSSI` status register is a 2's complement number. The following procedure can be used to convert the RSSI reading to an absolute power level (RSSI_dBm)

1) Read the `RSSI` status register
2) Convert the reading from a hexadecimal number to a decimal number (RSSI_dec)
3) If RSSI_dec ≥ 128 then RSSI_dBm = (RSSI_dec - 256)/2 – RSSI_offset
4) Else if RSSI_dec < 128 then RSSI_dBm = (RSSI_dec)/2 – RSSI_offset

Table 29 gives typical values for the RSSI_offset. Figure 17 and Figure 18 show typical plots of RSSI readings as a function of input power level for different data rates.

Data rate [kBaud]	RSSI_offset [dB], 490 MHz	RSSI_offset [dB], 955 MHz
1.2	75	75
38.4	75	75
76.8	N/A	79
250	79	N/A

Table 29: Typical RSSI_offset Values

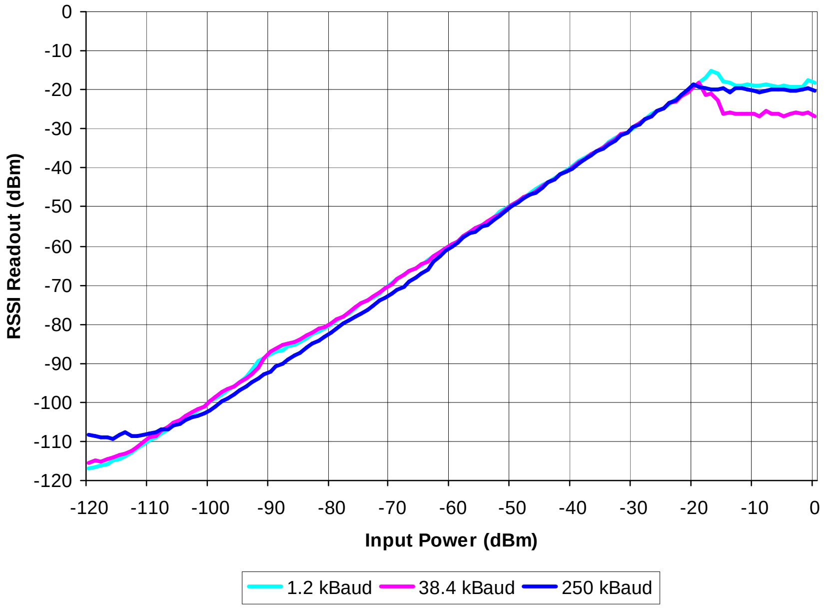


Figure 17: Typical RSSI Value vs. Input Power Level for Different Data Rates at 480 MHz

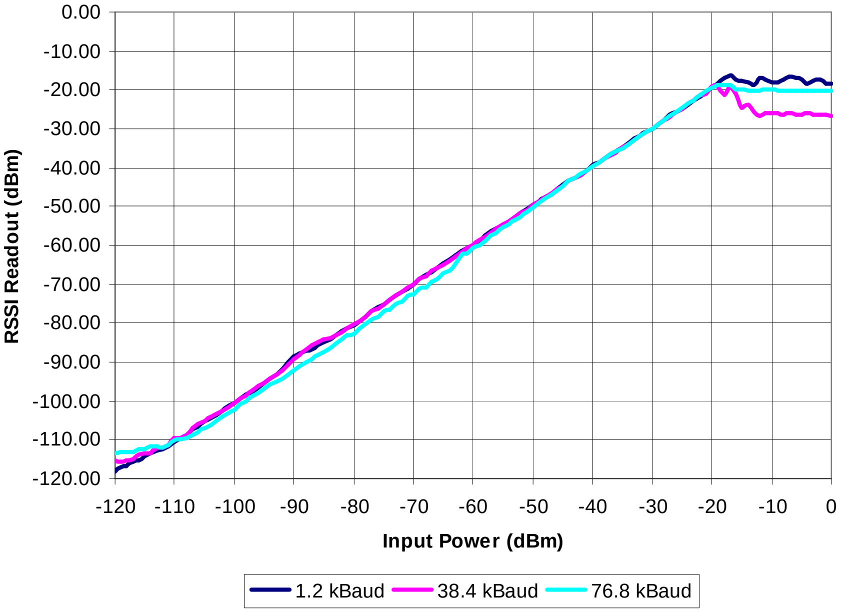


Figure 18: Typical RSSI Value vs. Input Power Level for Different Data Rates at 955 MHz

17.4 Carrier Sense (CS)

Carrier sense (CS) is used as a sync word qualifier and for Clear Channel Assessment (see Section 17.5). CS can be asserted based on two conditions which can be individually adjusted:

- CS is asserted when the RSSI is above a programmable absolute threshold, and de-asserted when RSSI is below the same threshold (with hysteresis). See more in Section 17.4.1.
- CS is asserted when the RSSI has increased with a programmable number of dB from one RSSI sample to the next, and de-asserted when RSSI has decreased with the same number of dB. This setting is not dependent on the absolute signal

level and is thus useful to detect signals in environments with time varying noise floor. See more in Section 17.4.2.

Carrier sense can be used as a sync word qualifier that requires the signal level to be higher than the threshold for a sync word search to be performed and is set by setting `MDMCFG2` The carrier sense signal can be observed on one of the GDO pins by setting `IOCFGx.GDOx_CFG=14` and in the status register bit `PKTSTATUS.CS`.

Other uses of Carrier sense include the TX-if-CCA function (see Section 17.5 on page 43) and the optional fast RX termination (see Section 19.7 on page 49).

CS can be used to avoid interference from other RF sources in the ISM bands.

17.4.1 CS Absolute Threshold

The absolute threshold related to the RSSI value depends on the following register fields:

- `AGCCTRL2.MAX_LNA_GAIN`
- `AGCCTRL2.MAX_DVGA_GAIN`
- `AGCCTRL1.CARRIER_SENSE_ABS_THR`
- `AGCCTRL2.MAGN_TARGET`

For given `AGCCTRL2.MAX_LNA_GAIN` and `AGCCTRL2.MAX_DVGA_GAIN` settings, the absolute threshold can be adjusted ±7 dB in steps of 1 dB using `CARRIER_SENSE_ABS_THR`.

The `MAGN_TARGET` setting is a compromise between blocker tolerance/selectivity and sensitivity. The value sets the desired signal level in the channel into the demodulator. Increasing this value reduces the headroom for blockers, and therefore close-in selectivity. It is strongly recommended to use SmartRF® Studio [8] to generate the correct `MAGN_TARGET` setting. Table 30 and Table 31 show the typical RSSI readout values at the CS threshold at 2.4 kBaud and 250 kBaud data rate respectively. The default `CARRIER_SENSE_ABS_THR=0` (0 dB) and `MAGN_TARGET=3` (33 dB) have been used. For other data rates, the user must generate similar tables to find the CS absolute threshold.

		MAX_DVGA_GAIN[1:0]			
		00	01	10	11
MAX_LNA_GAIN[2:0]	000	-97.5	-91.5	-85.5	-79.5
	001	-94	-88	-82.5	-76
	010	-90.5	-84.5	-78.5	-72.5
	011	-88	-82.5	-76.5	-70.5
	100	-85.5	-80	-73.5	-68
	101	-84	-78	-72	-66
	110	-82	-76	-70	-64
	111	-79	-73.5	-67	-61

Table 30: Typical RSSI Value in dBm at CS Threshold with Default `MAGN_TARGET` at 2.4 kBaud, 955 MHz

		MAX_DVGA_GAIN[1:0]			
		00	01	10	11
MAX_LNA_GAIN[2:0]	000	-90.5	-84.5	-78.5	-72.5
	001	-88	-82	-76	-70
	010	-84.5	-78.5	-72	-66
	011	-82.5	-76.5	-70	-64
	100	-80.5	-74.5	-68	-62
	101	-78	-72	-66	-60
	110	-76.5	-70	-64	-58
	111	-74.5	-68	-62	-56

Table 31: Typical RSSI Value in dBm at CS Threshold with Default `MAGN_TARGET` at 250 kBaud, 955 MHz

If the threshold is set high, i.e. only strong signals are wanted; the threshold should be adjusted upwards by first reducing the `MAX_LNA_GAIN` value and then the `MAX_DVGA_GAIN` value. This will reduce power consumption in the receiver front end, since the highest gain settings are avoided.

17.4.2 CS Relative Threshold

The relative threshold detects sudden changes in the measured signal level. This setting does not depend on the absolute signal level and is thus useful to detect signals in environments with a time varying noise floor. The register field `AGCCTRL1.CARRIER_SENSE_REL_THR` is used to enable/disable relative CS, and to select threshold of 6 dB, 10 dB, or 14 dB RSSI change.

17.5 Clear Channel Assessment (CCA)

The Clear Channel Assessment (CCA) is used to indicate if the current channel is free or busy. The current CCA state is viewable on any of the GDO pins by setting `IOCFGx.GDOx_CFG=0x09`.

`MCSM1.CCA_MODE` selects the mode to use when determining CCA.

When the `STX` or `SFSTXON` command strobe is given while the **CC1100E** is in the RX state, the TX or FSTXON state is only entered if the clear channel requirements are fulfilled. Otherwise, the chip will remain in RX. If the channel then becomes available, the radio will not enter TX or FSTXON state before a new strobe command is sent on the SPI interface. This feature is called TX-if-CCA. Four CCA requirements can be programmed:

- Always (CCA disabled, always goes to TX)
- If RSSI is below threshold
- Unless currently receiving a packet
- Both the above (RSSI below threshold and not currently receiving a packet)

17.6 Link Quality Indicator (LQI)

The Link Quality Indicator is a metric of the current quality of the received signal. If `PKTCTRL1.APPEND_STATUS` is enabled, the value is automatically added to the last byte appended after the payload. The value can also be read from the `LQI` status register. The LQI gives an estimate of how easily a received signal can be demodulated by accumulating the magnitude of the error between ideal constellations and the received signal over the 64 symbols immediately following the sync word. LQI is best used as a relative measurement of the link quality (a high value indicates a better link than what a low value does), since the value is dependent on the modulation format.

18 Forward Error Correction with Interleaving

18.1 Forward Error Correction (FEC)

The **CC1100E** has built in support for Forward Error Correction (FEC). To enable this option, set `MDMCFG1.FEC_EN` to `1`. FEC is only supported in fixed packet length mode, i.e. when `PKTCTRL0.LENGTH_CONFIG=0`. FEC is employed on the data field and CRC word in order to reduce the gross bit error rate when operating near the sensitivity limit. Redundancy is added to the transmitted data in such a way that the receiver can restore the original data in the presence of some bit errors.

The use of FEC allows correct reception at a lower Signal-to-Noise Ratio (SNR), thus extending communication range if the receiver bandwidth remains constant. Alternatively, for a given SNR, using FEC decreases the bit error rate (BER). The packet error rate (PER) is related to BER by

$$PER = 1 - (1 - BER)^{packet\_length}$$

A lower BER can therefore be used to allow longer packets, or a higher percentage of packets of a given length, to be transmitted successfully. Finally, in realistic ISM radio environments, transient and time-varying phenomena will produce occasional errors even in otherwise good reception conditions. FEC will mask such errors and, combined with interleaving of the coded data, even correct relatively long periods of faulty reception (burst errors).

The FEC scheme adopted for the **CC1100E** is convolutional coding, in which *n* bits are generated based on *k* input bits and the *m* most recent input bits, forming a code stream able to withstand a certain number of bit errors between each coding state (the *m*-bit window).

The convolutional coder is a rate ½ code with a constraint length of $m = 4$. The coder codes one input bit and produces two output bits; hence, the effective data rate is halved. This means that in order to transmit at the same effective data rate when using FEC, it is necessary to use twice as high over-the-air data rate. This will require a higher receiver bandwidth, and thus reduce sensitivity. In other words the improved reception by using FEC and the degraded sensitivity from a higher receiver bandwidth will be counteracting factors. Please see Design Note DN504 [18] for more information

18.2 Interleaving

Data received through radio channels will often experience burst errors due to interference and time-varying signal strengths. In order to increase the robustness to errors spanning multiple bits, interleaving is used when FEC is enabled. After de-interleaving, a continuous span of errors in the received stream will become single errors spread apart.

The **CC1100E** employs matrix interleaving, which is illustrated in Figure 19. The on-chip interleaving and de-interleaving buffers are 4 x 4 matrices. In the transmitter, the data bits from the rate ½ convolutional coder are written into the rows of the matrix, whereas the bit sequence to be transmitted is read from the columns of the matrix. Conversely, in the receiver, the received symbols are written into the rows of the matrix, whereas the data passed onto the convolutional decoder is read from the columns of the matrix.

When FEC and interleaving is used, at least one extra byte is required for trellis termination. In addition, the amount of data transmitted over the air must be a multiple of the size of the interleaver buffer (two bytes). The packet control hardware therefore automatically inserts one or two extra bytes at the end of the packet, so that the total length of the data to be interleaved is an even number. Note that these extra bytes are invisible to the user, as they are removed before the received packet enters the RX FIFO.

When FEC and interleaving is used the minimum data payload is 2 bytes.

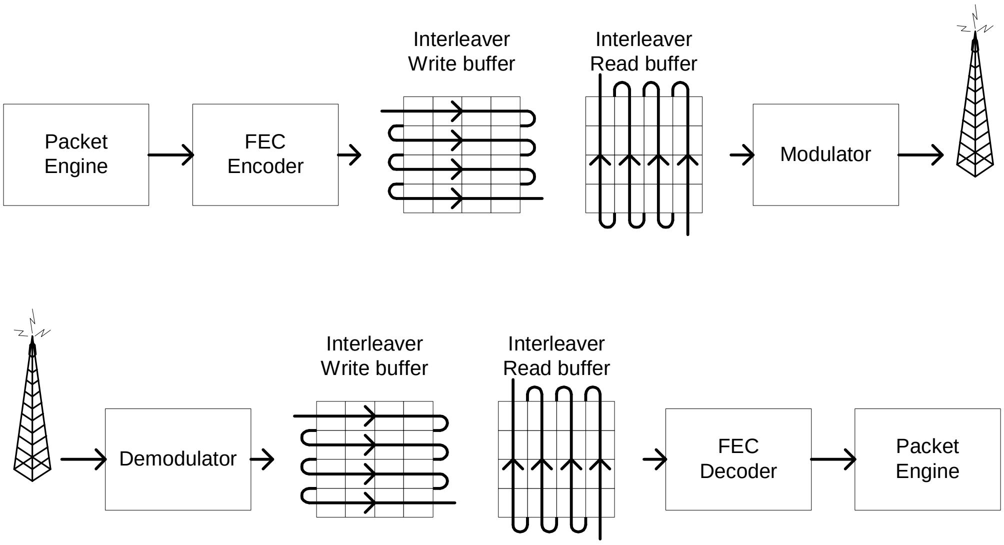


Figure 19: General Principle of Matrix Interleaving

19 Radio Control

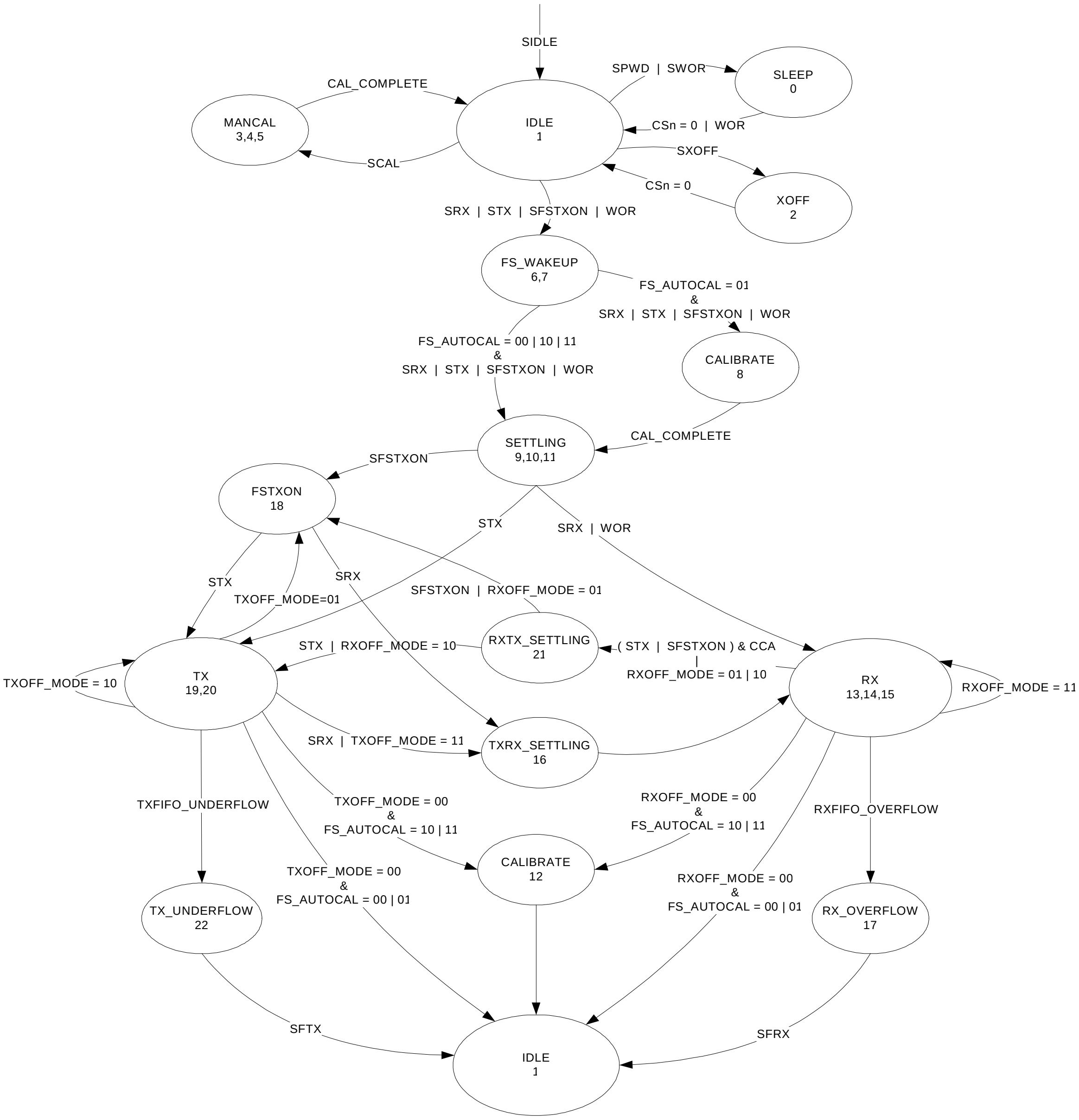


Figure 20: Complete Radio Control State Diagram

The **CC1100E** has a built-in state machine that is used to switch between different operational states (modes). The change of state is done either by using command strobes or by internal events such as TX FIFO underflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 9 on page 24. The complete radio control state diagram is shown in Figure 20. The numbers refer to the state number readable in the `MARCSTATE` status register. This register is primarily for test purposes.

19.1 Power-On Start-Up Sequence

When the power supply is turned on, the system must be reset. This is achieved by one of the two sequences described below, i.e. Automatic power-on reset (POR) or manual reset. After the automatic power-on reset or manual reset, it is also recommended to change the signal that is output on the GDO0 pin. The default setting is to output a clock signal with a frequency of CLK_XOSC/192. However, to optimize performance in TX and RX, an alternative GDO setting from the settings found in Table 36 on page 55 should be selected.

19.1.1 Automatic POR

A power-on reset circuit is included in the **CC1100E**. The minimum requirements stated in Table 16 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when `CHIP_RDYn` goes low. `CHIP_RDYn` is observed on the SO pin after CSn is pulled low. See Section 10.1 for more details on `CHIP_RDYn`.

When the **CC1100E** reset is completed, the chip will be in the IDLE state and the crystal oscillator will be running. If the chip has had sufficient time for the crystal oscillator to stabilize after the power-on-reset, the SO pin will go low immediately after taking CSn low. If CSn is taken low before reset is completed, the SO pin will first go high, indicating that the crystal oscillator is not stabilized, before going low as shown in Figure 21.

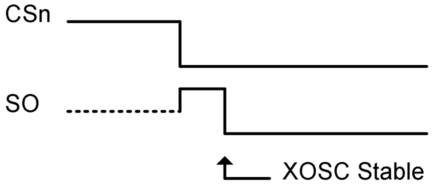


Figure 21: Power-On Reset

19.1.2 Manual Reset

The other global reset possibility on the **CC1100E** uses the `SRES` command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The manual power-up sequence is as follows (see Figure 22):

- Set SCLK = 1 and SI = 0, to avoid potential problems with pin control mode (see Section 11.3 on page 30).
- Strobe CSn low / high.
- Hold CSn low and then high for at least 40 µs relative to pulling CSn low
- Pull CSn low and wait for SO to go low (`CHIP_RDYn`).
- Issue the `SRES` strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

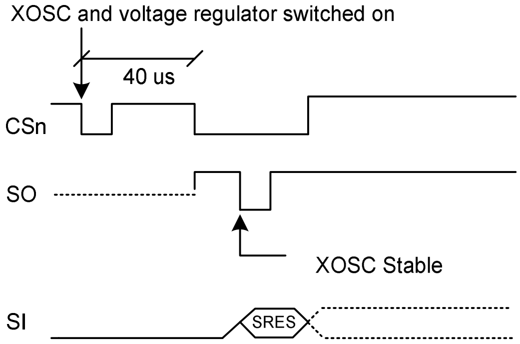


Figure 22: Power-On Reset with SRES

Note that the above reset procedure is only required just after the power supply is first turned on. If the user wants to reset the **CC1100E** after this, it is only necessary to issue an SRES command strobe.

19.2 Crystal Control

The crystal oscillator (XOSC) is either automatically controlled or always on, if `MCSM0.XOSC_FORCE_ON` is set.

In the automatic mode, the XOSC will be turned off if the `SXOFF` or `SPWD` command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can only be done from the IDLE state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used as described in Section 10.1 on page 27.

If the XOSC is forced on, the crystal will always stay on even in the SLEEP state.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in Section 4.4 on page 14.

19.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after CSn is released when a `SPWD` command strobe has been sent on the SPI interface. The chip is then in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

When Wake on Radio is enabled, the WOR module will control the voltage regulator as described in Section19.5.

19.4 Active Modes

The **CC1100E** has two active modes: receive and transmit. These modes are activated directly by the MCU by using the `SRX` and `STX` command strobes, or automatically by Wake on Radio.

The frequency synthesizer must be calibrated regularly. The **CC1100E** has one manual calibration option (using the `SCAL` strobe), and three automatic calibration options that are controlled by the `MCSM0.FS_AUTOCAL` setting:

- Calibrate when going from IDLE to either RX or TX (or FSTXON)
- Calibrate when going from either RX or TX to IDLE automatically
- Calibrate every fourth time when going from either RX or TX to IDLE automatically

If the radio goes from TX or RX to IDLE by issuing an `SIDLE` strobe, calibration will not be performed. The calibration takes a constant number of XOSC cycles; see Table 32 for timing details regarding calibration.

When RX is activated, the chip will remain in receive mode until a packet is successfully received or the RX termination timer expires (see Section 19.7). The probability that a false sync word is detected can be reduced by using PQT, CS, maximum sync word length, and sync word qualifier mode as described in Section 17. After a packet is successfully received, the radio controller goes to the state indicated by the `MCSM1.RXOFF_MODE` setting. The possible destinations are:

- IDLE
- FSTXON: Frequency synthesizer on and ready at the TX frequency. Activate TX with `STX`
- TX: Start sending preamble
- RX: Start search for a new packet

Note: When `MCSM1.RXOFF_MODE=11` and a packet has been received, it will take some time before a valid RSSI value is present in the `RSSI` register again even if the radio has never exited RX mode. This time is the same as the RSSI response time discussed in DN505 [13].

Similarly, when TX is active the chip will remain in the TX state until the current packet has been successfully transmitted. Then the state will change as indicated by the `MCSM1.TXOFF_MODE` setting. The possible destinations are the same as for RX.

The MCU can manually change the state from RX to TX and vice versa by using the command strobes. If the radio controller is currently in transmit and the `SRX` strobe is used, the current transmission will be ended and the transition to RX will be done.

If the radio controller is in RX when the `STX` or `SFSTXON` command strobes are used, the TX-if-CCA function will be used. If the channel is not clear, the chip will remain in RX. The `MCSM1.CCA_MODE` setting controls the conditions for clear channel assessment. See Section 17.5 on page 43 for details.

The `SIDLE` command strobe can always be used to force the radio controller to go to the IDLE state.

19.5 Wake On Radio (WOR)

The optional Wake on Radio (WOR) functionality enables the **CC1100E** to periodically wake up from SLEEP and listen for incoming packets without MCU interaction.

When the `SWOR` strobe command is sent on the SPI interface, the **CC1100E** will go to the SLEEP state when CSn is released. The RC oscillator must be enabled before the `SWOR` strobe can be used, as it is the clock source for the WOR timer. The on-chip timer will set the **CC1100E** into IDLE state and then RX state. After a programmable time in RX, the chip will go back to the SLEEP state, unless a packet is received. See Figure 23 and Section 19.7 for details on how the timeout works.

To exit WOR mode, set the **CC1100E** into the IDLE state

The **CC1100E** can be set up to signal the MCU that a packet has been received by using the GDO pins. If a packet is received, the `MCSM1.RXOFF_MODE` will determine the behaviour at the end of the received packet. When the MCU has read the packet, it can put the chip back into SLEEP with the `SWOR` strobe from the IDLE state.

Note: The FIFO looses its content in the SLEEP state.

The WOR timer has two events, Event 0 and Event 1. In the SLEEP state with WOR activated, reaching Event 0 will turn on the digital regulator and start the crystal oscillator. Event 1 follows Event 0 after a programmed timeout.

The time between two consecutive Event 0 is programmed with a mantissa value given by `WOREVT1.EVENT0` and `WOREVT0.EVENT0`, and an exponent value set by `WORCTRL.WOR_RES`. The equation is:

$$t_{Event0} = \frac{750}{f_{XOSC}} \cdot EVENT0 \cdot 2^{5 \cdot WOR\_RES}$$

The Event 1 timeout is programmed with `WORCTRL.EVENT1`. Figure 23 shows the timing relationship between Event 0 timeout and Event 1 timeout.

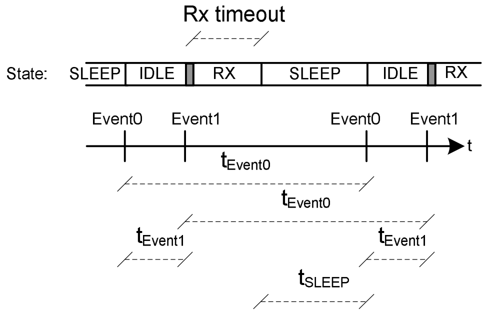


Figure 23: Event 0 and Event 1 Relationship

The time from the **CC1100E** enters SLEEP state until the next Event0 is programmed to appear, t_{SLEEP} in Figure 23, should be larger than 11.08 ms when using a 26 MHz crystal and 10.67 ms when a 27 MHz crystal is used. If t_{SLEEP} is less than 11.08 (10.67) ms, there is a chance that the consecutive Event 0 will occur

$$\frac{750}{f_{XOSC}} \cdot 128 \text{ seconds}$$

too early. Application Note AN047 [7] explains in detail the theory of operation and the different registers involved when using WOR, as well as highlighting important aspects when using WOR mode.

19.5.1 RC Oscillator and Timing

The frequency of the low-power RC oscillator used for the WOR functionality varies with temperature and supply voltage. In order to keep the frequency as accurate as possible, the RC oscillator will be calibrated whenever possible, which is when the XOSC is running and the chip is not in the SLEEP state. When the power and XOSC are enabled, the clock used by the WOR timer is a divided XOSC clock. When the chip goes to the sleep state, the RC oscillator will use the last valid calibration result. The frequency of the RC oscillator is locked to the main crystal frequency divided by 750.

In applications where the radio wakes up very often, typically several times every second, it is possible to do the RC oscillator calibration once and then turn off calibration to reduce the current consumption. This is done by setting `WORCTRL.RC_CAL=0` and requires that RC oscillator calibration values are read from registers `RCCTRL0_STATUS` and `RCCTRL1_STATUS` and written back to `RCCTRL0` and `RCCTRL1` respectively. If the

RC oscillator calibration is turned off, it will have to be manually turned on again if the temperature and/or the supply voltage changes. Refer to Application Note AN047 [7] for further details.

19.6 Timing

The radio controller controls most of the timing in the **CC1100E**, such as synthesizer calibration, PLL lock time, and RX/TX turnaround times. Timing from IDLE to RX and IDLE to TX is constant, dependent on the auto calibration setting. RX/TX and TX/RX turnaround times are constant. The calibration time is constant 18739 clock periods. Table 32 shows timing in crystal clock cycles for key state transitions.

Power on time and XOSC start-up times are variable, but within the limits stated in Table 11.

Note that in a frequency hopping spread spectrum or a multi-channel protocol the calibration time can be reduced from 721 µs to approximately 150 µs. This is explained in Section 28.2.

Description	XOSC Periods	26 MHz Crystal
IDLE to RX, no calibration	2298	88.4µs
IDLE to RX, with calibration	~21037	809µs
IDLE to TX/FSTXON, no calibration	2298	88.4µs
IDLE to TX/FSTXON, with calibration	~21037	809µs
TX to RX switch	560	21.5µs
RX to TX switch	250	9.6µs
RX or TX to IDLE, no calibration	2	0.1µs
RX or TX to IDLE, with calibration	~18739	721µs
Manual calibration	~18739	721µs

Table 32: State Transition Timing

19.7 RX Termination Timer

The **CC1100E** has optional functions for automatic termination of RX after a programmable time. The main use for this functionality is Wake on Radio, but it may also be useful for other applications. The termination timer starts when in RX state. The timeout is programmable with the `MCSM2.RX_TIME` setting. When the timer expires, the radio controller will check the condition for staying in RX; if the condition is not met, RX will terminate.

The programmable conditions are:

- `MCSM2.RX_TIME_QUAL=0`: Continue receive if sync word has been found
- `MCSM2.RX_TIME_QUAL=1`: Continue receive if sync word has been found, or if the preamble quality is above threshold (PQT)

If the system expects the transmission to have started when enabling the receiver, the `MCSM2.RX_TIME_RSSI` function can be used. The radio controller will then terminate RX if the first valid carrier sense sample indicates no carrier (RSSI below threshold). See Section 17.4 on page 41 for details on Carrier Sense.

For ASK/OOK modulation, lack of carrier sense is only considered valid after eight symbol periods. Thus, the `MCSM2.RX_TIME_RSSI` function can be used in ASK/OOK mode when the distance between "1" symbols is eight or less.

If RX terminates due to no carrier sense when the `MCSM2.RX_TIME_RSSI` function is used, or if no sync word was found when using the `MCSM2.RX_TIME` timeout function, the chip will always go back to IDLE if WOR is disabled and back to SLEEP if WOR is enabled. Otherwise, the `MCSM1.RXOFF_MODE` setting determines the state to go to when RX ends. This means that the chip will not automatically go back to SLEEP once a sync word has been received. It is therefore recommended to always wake up the microcontroller on sync word detection when using WOR mode. This can be done by selecting output signal 6 (see Table 36 on page 55) on one of the programmable GDO output pins, and programming the microcontroller to wake up on an edge-triggered interrupt from this GDO pin.

20 Data FIFO

The **CC1100E** contains two 64 byte FIFOs, one for received data and one for data to be transmitted. The SPI interface is used to read from the RX FIFO and write to the TX FIFO. Section 10.5 contains details on the SPI FIFO access. The FIFO controller will detect overflow in the RX FIFO and underflow in the TX FIFO.

When writing to the TX FIFO it is the responsibility of the MCU to avoid TX FIFO overflow. A TX FIFO overflow will result in an error in the TX FIFO content.

Likewise, when reading the RX FIFO the MCU must avoid reading the RX FIFO past its empty value since a RX FIFO underflow will result in an error in the data read out of the RX FIFO.

The chip status byte that is available on the SO pin while transferring the SPI header and contains the fill grade of the RX FIFO if the access is a read operation and the fill grade of the TX FIFO if the access is a write operation. Section 10.1 on page 27 contains more details on this.

The number of bytes in the RX FIFO and TX FIFO can be read from the status registers `RXBYTES.NUM_RXBYTES` and `TXBYTES.NUM_TXBYTES` respectively. If a received data byte is written to the RX FIFO at the exact same time as the last byte in the RX FIFO is read over the SPI interface, the RX FIFO pointer is not properly updated and the last read byte will be duplicated. To avoid this problem, the RX FIFO should never be emptied before the last byte of the packet is received.

For packet lengths less than 64 bytes it is recommended to wait until the complete packet has been received before reading it out of the RX FIFO.

If the packet length is larger than 64 bytes, the MCU must determine how many bytes can be read from the RX FIFO (`RXBYTES.NUM_RXBYTES-1`). The following software routine can be used:

1. Read `RXBYTES.NUM_RXBYTES` repeatedly at a rate guaranteed to be at least twice that of which RF bytes are received until the same value is returned twice; store value in *n*.
2. If *n* < # of bytes remaining in packet, read *n*-1 bytes from the RX FIFO.
3. Repeat steps 1 and 2 until *n* = # of bytes remaining in packet.
4. Read the remaining bytes from the RX FIFO.

The 4-bit `FIFOTHR.FIFO_THR` setting is used to program threshold points in the FIFOs.

Table 33 lists the 16 `FIFO_THR` settings and the corresponding thresholds for the RX and TX FIFOs. The threshold value is coded in opposite directions for the RX FIFO and TX FIFO. This gives equal margin to the overflow and underflow conditions when the threshold is reached.

`FIFO_THR`	Bytes in TX FIFO	Bytes in RX FIFO
0 (0000)	61	4
1 (0001)	57	8
2 (0010)	53	12
3 (0011)	49	16
4 (0100)	45	20
5 (0101)	41	24
6 (0110)	37	28
7 (0111)	33	32
8 (1000)	29	36
9 (1001)	25	40
10 (1010)	21	44
11 (1011)	17	48
12 (1100)	13	52
13 (1100E)	9	56
14 (1110)	5	60
15 (1111)	1	64

Table 33: `FIFO_THR` Settings and the Corresponding FIFO Thresholds

A signal will assert when the number of bytes in the FIFO is equal to or higher than the programmed threshold. This signal can be viewed on the GDO pins (see Table 36 on page 55).

Figure 24 shows the number of bytes in both the RX FIFO and TX FIFO when the threshold signal toggles in the case of `FIFO_THR=13`. Figure 25 shows the signal on the GDO pin as the respective FIFO is filled above the threshold, and then drained below in the case of `FIFO_THR=13`.

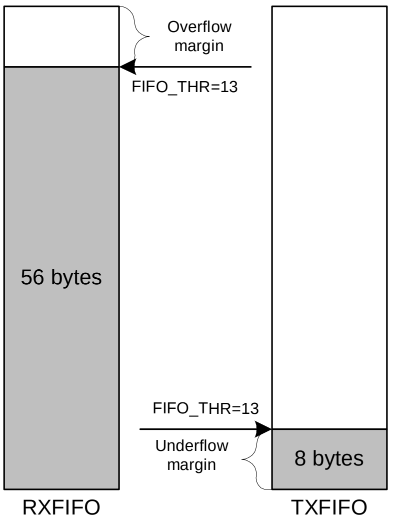


Figure 24 Example of FIFOs at Threshold

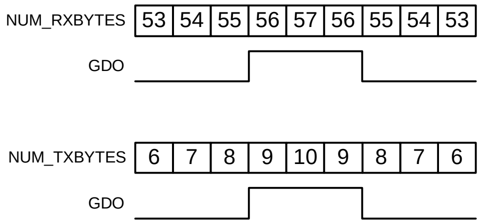


Figure 25: Number of Bytes in FIFO vs. the GDO Signal (`GDOx_CFG=0x00` in RX and `GDOx_CFG=0x02` in TX, `FIFO_THR=13`)

21 Frequency Programming

The frequency programming in the **CC1100E** is designed to minimize the programming needed in a channel-oriented system.

To set up a system with channel numbers, the desired channel spacing is programmed with the `MDMCFG0.CHANSPC_M` and `MDMCFG1.CHANSPC_E` registers. The channel spacing registers are mantissa and exponent respectively. The base or start frequency is set by the 24 bit frequency word located in the `FREQ2`, `FREQ1`, and `FREQ0` registers. This word will typically be set to the centre of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, `CHANNR.CHAN`, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot \left(FREQ + CHAN \cdot \left(\left(256 + CHANSPC\_M\right) \cdot 2^{CHANSPC\_E-2}\right)\right)$$

With a 26 MHz crystal the maximum channel spacing is 405 kHz. To get e.g. 1 MHz channel spacing, one solution is to use 333 kHz channel spacing and select each third channel in `CHANNR.CHAN`.

The preferred IF frequency is programmed with the `FSCTRL1.FREQ_IF` register. The IF frequency is given by:

$$f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$$

Note that the SmartRF® Studio software [8] automatically calculates the optimum `FSCTRL1.FREQ_IF` register setting based on channel spacing and channel filter bandwidth.

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency programming should only be updated when the radio is in the IDLE state.

22 VCO

The VCO is completely integrated on-chip.

22.1 VCO and PLL Self-Calibration

The VCO characteristics vary with temperature and supply voltage changes as well as the desired operating frequency. In order to ensure reliable operation, the **CC1100E** includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 32 on page 49.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off automatically. This is configured with the `MCSM0.FS_AUTOCAL` register setting. In manual mode, the calibration is initiated when the `SCAL` command strobe is activated in the IDLE mode.

Note: The calibration values are maintained in SLEEP mode, so the calibration is still valid after waking up from SLEEP mode unless supply voltage or temperature has changed significantly.

To check that the PLL is in lock, the user can program register `IOCFGx.GDOx_CFG` to 0x0A, and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0,1, or 2). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register FSCAL1. The PLL is in lock if the register content is different from 0x3F. Refer also to the **CC1100E** Errata Note [5].

For more robust operation, the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

23 Voltage Regulators

The **CC1100E** contains several on-chip linear voltage regulators that generate the supply voltages needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in Table 1 and Table 17 are not exceeded.

By setting the CSn pin low, the voltage regulator to the digital core turns on and the crystal oscillator starts. The SO pin on the SPI interface must go low before the first positive edge of SCLK (setup time is given in Table 20).

If the chip is programmed to enter power-down mode (`SPWD` strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator for the digital core requires one external decoupling capacitor.

The voltage regulator output should only be used for driving the **CC1100E**.

24 Output Power Programming

The RF output power level from the device has two levels of programmability as illustrated in Figure 26. The special `PATABLE` register can hold up to eight user selected output power settings. The 3-bit `FREND0.PA_POWER` value selects the `PATABLE` entry to use. This two-level functionality provides flexible PA power ramp up and ramp down at the start and end of transmission as well as ASK modulation shaping. All the PA power settings in the `PATABLE` from index 0 up to the `FREND0.PA_POWER` value are used.

The power ramping at the start and at the end of a packet can be turned off by setting `FREND0.PA_POWER=0` and then program the desired output power to index 0 in the `PATABLE`.

If OOK modulation is used, the logic 0 and logic 1 power levels shall be programmed to index 0 and 1 respectively.

Table 33 contains recommended `PATABLE` settings for various output levels and frequency bands. DN013 **Error! Reference source not found.** gives the complete tables for the different frequency bands. Using PA settings from 0x61 to 0x6F is not recommended.

Table 34 contains output power and current consumption for default `PATABLE` setting (0xC6).

See Section 10.6 on page 29 for `PATABLE` programming details. `PATABLE` must be programmed in burst mode if you want to write to other entries than `PATABLE[0]`.

Note: All content of the `PATABLE` except for the first byte (index 0) is lost when entering the SLEEP state.

	480 MHz		955 MHz	
Output Power [dBm]	**Setting**	**Current Consumption, Typ. [mA]**	**Setting**	**Current Consumption, Typ. [mA]**
-30	0x04	12.5	0x30	13.0
-20	0x0E	13.0	0x14	12.9
-15	0x1C	13.5	0x18	13.6
-10	0x26	14.9	0x24	14.6
-5	0x2B	16.9	0x28	16.2
0	0x60	16.6	0x60	16.5
5	0x86	19.8	0x86	19.1
7	0xCB	24.6	0xC7	26.3
10 (9)	0xC2	29.6	0xC0	30.9

Table 34: Optimum `PATABLE` Settings for Various Output Power Levels and Frequency Bands

	480 MHz		955 MHz	
Default Power Setting	**Output Power [dBm]**	**Current Consumption, Typ. [mA]**	**Output Power [dBm]**	**Current Consumption, Typ. [mA]**
0xC6	8.8	26.9	7.3	26.7

Table 35: Output Power and Current Consumption for Default `PATABLE` Setting

25 Shaping and PA Ramping

With ASK modulation, up to eight power settings are used for shaping. The modulator contains a counter that counts up when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate. The counter saturates at `FREND0.PA_POWER` and 0 respectively. This counter value is used as an index for a lookup in the power table. Thus, in order to utilize the whole table, `FREND0.PA_POWER` should be 7 when ASK is active. The shaping of the ASK signal is dependent on the configuration of the PATABLE. Figure 27 shows some examples of ASK shaping.

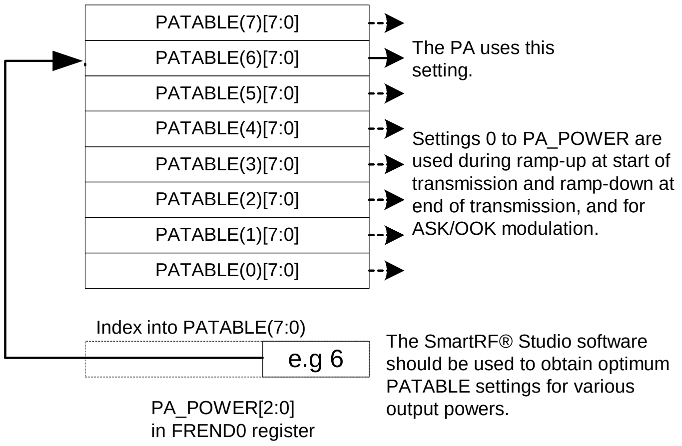


Figure 26: PA_POWER and PATABLE

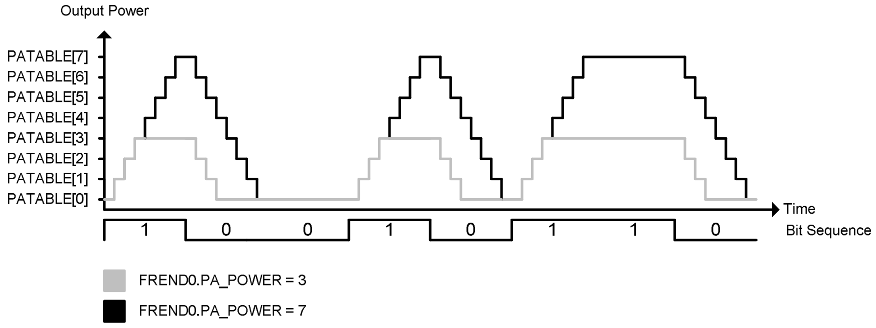


Figure 27: Shaping of ASK Signal

26 General Purpose / Test Output Control Pins

The three digital output pins GDO0, GDO1, and GDO2 are general control pins configured with `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG`, and `IOCFG2.GDO2_CFG` respectively. Table 36 shows the different signals that can be monitored on the GDO pins. These signals can be used as inputs to the MCU.

GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CSn is high. The default value for GDO1 is 3-stated which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 135-141 kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to `IOCFG0.GDO0_CFG.`

An on-chip analog temperature sensor is enabled by writing the value 128 (0x80) to the `IOCFG0` register. The voltage on the GDO0 pin is then proportional to temperature. See Section 4.7 on page 15 for temperature sensor specifications.

If the `IOCFGx.GDOx_CFG` setting is less than 0x20 and `IOCFGx_GDOx_INV` is 0 (1), the GDO0 and GDO2 pins will be hardwired to 0 (1), and the GDO1 pin will be hardwired to 1 (0) in the SLEEP state. These signals will be hardwired until the `CHIP_RDYn` signal goes low.

If the `IOCFGx.GDOx_CFG` setting is 0x20 or higher, the GDO pins will work as programmed also in SLEEP state. As an example, GDO1 is high impedance in all states if `IOCFG1.GDO1_CFG=0x2E`.

GDOx_CFG[5:0]	Description	
0 (0x00)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold. De-asserts when RX FIFO is drained below the same threshold.	
1 (0x01)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold or the end of packet is reached. De-asserts when the RX FIFO is empty.	
2 (0x02)	Associated to the TX FIFO: Asserts when the TX FIFO is filled at or above the TX FIFO threshold. De-asserts when the TX FIFO is below the same threshold.	
3 (0x03)	Associated to the TX FIFO: Asserts when TX FIFO is full. De-asserts when the TX FIFO is drained below the TX FIFO threshold.	
4 (0x04)	Asserts when the RX FIFO has overflowed. De-asserts when the FIFO has been flushed.	
5 (0x05)	Asserts when the TX FIFO has underflowed. De-asserts when the FIFO is flushed.	
6 (0x06)	Asserts when sync word has been sent / received, and de-asserts at the end of the packet. In RX, the pin will de-assert when the optional address check fails or the RX FIFO overflows. In TX the pin will de-assert if the TX FIFO underflows.	
7 (0x07)	Asserts when a packet has been received with CRC OK. De-asserts when the first byte is read from the RX FIFO.	
8 (0x08)	Preamble Quality Reached. Asserts when the PQI is above the programmed PQT value.	
9 (0x09)	Clear channel assessment. High when RSSI level is below threshold (dependent on the current CCA_MODE setting).	
10 (0x0A)	Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.	
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. In RX mode, data is set up on the falling edge by the **CC1100E** when GDOx_INV=0. In TX mode, data is sampled by the **CC1100E** on the rising edge of the serial clock when GDOx_INV=0.	
12 (0x0C)	Serial Synchronous Data Output. Used for synchronous serial mode.	
13 (0x0D)	Serial Data Output. Used for asynchronous serial mode.	
14 (0x0E)	Carrier sense. High if RSSI level is above threshold.	
15 (0x0F)	CRC_OK. The last CRC comparison matched. Cleared when entering/restarting RX mode.	
16 (0x10)	Reserved – used for test.	
17 (0x11)	Reserved – used for test.	
18 (0x12)	Reserved – used for test.	
19 (0x13)	Reserved – used for test.	
20 (0x14)	Reserved – used for test.	
21 (0x15)	Reserved – used for test.	
22 (0x16)	RX_HARD_DATA [1]. Can be used together with RX_SYMBOL_TICK for alternative serial RX output.	
23 (0x17)	RX_HARD_DATA [0]. Can be used together with RX_SYMBOL_TICK for alternative serial RX output.	
24 (0x18)	Reserved – used for test.	
25 (0x19)	Reserved – used for test.	
26 (0x1A)	Reserved – used for test.	
27 (0x1B)	Reserved – used for test.	
28 (0x1C)	Reserved – used for test.	
29 (0x1D)	RX_SYMBOL_TICK. Can be used together with RX_HARD_DATA for alternative serial RX output.	
30 (0x1E)	Reserved – used for test.	
31 (0x1F)	Reserved – used for test.	
32 (0x20)	Reserved – used for test.	
33 (0x21)	Reserved – used for test.	
34 (0x22)	Reserved – used for test.	
35 (0x23)	Reserved – used for test.	
36 (0x24)	WOR_EVNT0.	
37 (0x25)	WOR_EVNT1.	
38 (0x26)	Reserved – used for test.	
39 (0x27)	CLK_32k.	
40 (0x28)	Reserved – used for test.	
41 (0x29)	CHIP_RDYn.	
42 (0x2A)	Reserved – used for test.	
43 (0x2B)	XOSC_STABLE.	
44 (0x2C)	Reserved – used for test.	
45 (0x2D)	GDO0_Z_EN_N. When this output is 0, GDO0 is configured as input (for serial TX data).	
46 (0x2E)	High impedance (3-state).	
47 (0x2F)	HW to 0 (HW1 achieved by setting GDOx_INV=1). Can be used to control an external LNA/PA or RX/TX switch.	
48 (0x30)	CLK_XOSC/1	Note: There are 3 GDO pins, but only one CLK_XOSC/n can be selected as an output at any time. If CLK_XOSC/n is to be monitored on one of the GDO pins, the other two GDO pins must be configured to values less than 0x30. The GDO0 default value is CLK_XOSC/192. To optimize RF performance, these signals should not be used while the radio is in RX or TX mode.
49 (0x31)	CLK_XOSC/1.5	
50 (0x32)	CLK_XOSC/2	
51 (0x33)	CLK_XOSC/3	
52 (0x34)	CLK_XOSC/4	
53 (0x35)	CLK_XOSC/6	
54 (0x36)	CLK_XOSC/8	
55 (0x37)	CLK_XOSC/12	
56 (0x38)	CLK_XOSC/16	
57 (0x39)	CLK_XOSC/24	
58 (0x3A)	CLK_XOSC/32	
59 (0x3B)	CLK_XOSC/48	
60 (0x3C)	CLK_XOSC/64	
61 (0x3D)	CLK_XOSC/96	
62 (0x3E)	CLK_XOSC/128	
63 (0x3F)	CLK_XOSC/192	

Table 36: GDOx Signal Selection (x = 0, 1, or 2)

27 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the **CC1100E** to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller, and simplify software development.

27.1 Asynchronous Serial Operation

Asynchronous transfer is included in the **CC1100E** for backward compatibility with systems that are already using the asynchronous data transfer.

When asynchronous transfer is enabled, several of the support mechanisms for the MCU that are included in the **CC1100E** will be disabled, such as packet handling hardware, buffering in the FIFO, and so on. The asynchronous transfer mode does not allow for the use of the data whitener, interleaver, and FEC, and it is not possible to use Manchester encoding. MSK is not supported for asynchronous transfer.

Setting `PKTCTRL0.PKT_FORMAT` to 3 enables asynchronous serial mode. In TX, the GDO0 pin is used for data input (TX data). Data output can be on GDO0, GDO1, or GDO2. This is set by the `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG` and `IOCFG2.GDO2_CFG` fields.

The **CC1100E** modulator samples the level of the asynchronous input 8 times faster than the programmed data rate. The timing requirement for the asynchronous stream is that the error in the bit period must be less than one eighth of the programmed data rate.

27.2 Synchronous Serial Operation

Setting `PKTCTRL0.PKT_FORMAT` to 1 enables synchronous serial mode. In the synchronous serial mode, data is transferred on a two-wire serial interface. The **CC1100E** provides a clock that is used to set up new data on the data input line or sample data on the data output line. Data input (TX data) is on the GDO0 pin. This pin will automatically be configured as an input when TX is active. The TX latency is 8 bits. The data output pin can be any of the GDO pins. This is set by the `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG`, and `IOCFG2.GDO2_CFG` fields. Time from start of reception until data is available on the receiver data output pin is equal to 9 bit.

Preamble and sync word insertion/detection may or may not be active, dependent on the sync mode set by the `MDMCFG2.SYNC_MODE`.

If preamble and sync word is disabled, all other packet handler features and FEC should also be disabled. The MCU must then handle preamble and sync word insertion and detection in software.

If preamble and sync word insertion/detection is left on, all packet handling features and FEC can be used. One exception is that the address filtering feature is unavailable in synchronous serial mode.

When using the packet handling features in synchronous serial mode, the **CC1100E** will insert and detect the preamble and sync word and the MCU will only provide/get the data payload. This is equivalent to the recommended FIFO operation mode.

An alternative serial RX output option is to configure any of the GD0 pins for `RX_SYMBOL_TICK` and `RX_HARD_[1:0]`, see Table 36. `RX_HARD_[1:0]` is the hard decision symbol. `RX_HARD_[1:0]` contain data for 4-ary modulation formats while RX_HARD_DATA [1] contain data for 2-ary modulation formats. The `RX_SYMBOL_TICK` signal is the symbol clock and is high for one half symbol period whenever a new symbol is presented on the hard and soft data outputs. This option may be used for both synchronous and asynchronous interfaces.

28 System Considerations and Guidelines

28.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. The **CC1100E** is specifically designed for use in the license free 470-510 MHz and 950-960 MHz frequency bands in China and Japan, respectively.

28.1.1 ARIB STD-T96

The applicable regulatory requirements for using the **CC1100E** at the 950-956 MHz frequency band in Japan are specified by the ARIB STD-T96 [6].

For applications targeting ARIB STD-T96, `FSCAL3 [7:4]` needs to be set to 0xA and `FSCAL0` needs to be set to 0x07 for optimum performance.

The **CC1100E** can support operation with one (200 kHz), two (400 kHz) and three (600 kHz) unit channels as defined by the ARIB STD-T96 but will typically be used in wireless systems with two and three unit channels. For data rates higher than 100 kbps, the frequency deviation may have to be reduced compared to the default settings in order to comply with the ARIB STD-T96 transmit specifications.

Typical margins to the transmit spectrum mask measured according to the ARIB STD-T96 using the CC1100E reference design at 0 dBm output power are shown in Table 37. Higher margins can be achieved by reducing the output power accordingly.

Please note that compliance with regulations is dependent on the complete system performance. It is the customer’s responsibility to ensure that the system complies with regulations.

Data Rate [kbps]	**Deviation** [kHz]	**Typical Sensitivity** [dBm]	**Typical Margin** [dB]	
			400 kHz	**600 kHz**
1.2	5.2	-111	3	4
4.8	25.4	-110	1.5	5.5
10	19	-106	3	4.5
38.4	20	-103	1.5	6.5
76.8	32	-100	3	6
100	47	-100	1	5.5
175	41	-91	2.5	5.5
200	100	-96	N/A	2
200	38	-89	1.5	4.5
250	70	-93	N/A	2.5

Table 37: CC1100E typical performance values for ARIB STD-T96 using the CC1100E reference design, 25°C and 3V (`FSCAL3 [7:4]` set to 0xA and `FSCAL0` set to 0x07)

28.2 Frequency Hopping and Multi-Channel Systems

The 470 MHz and 950 MHz bands are shared by many systems both in industrial, office, and home environments. It is therefore recommended to use frequency hopping spread spectrum (FHSS) or a multi-channel protocol because the frequency diversity makes the system more robust with respect to interference from other systems operating in the same frequency band. FHSS also combats multipath fading.

The **CC1100E** is highly suited for FHSS or multi-channel systems due to its agile frequency synthesizer and effective communication interface. Using the packet handling support and data buffering is also beneficial in such systems as these features will significantly offload the host controller.

Charge pump current, VCO current, and VCO capacitance array calibration data is required for each frequency when implementing frequency hopping for the **CC1100E**. There are 3 ways of obtaining the calibration data from the chip:

1) Frequency hopping with calibration for each hop. The PLL calibration time is approximately 720 µs. The blanking interval between each frequency hop is then approximately 810 us.

2) Fast frequency hopping without calibration for each hop can be done by performing the necessary calibrating at startup and saving the resulting `FSCAL3`, `FSCAL2`, and `FSCAL1` register values in MCU memory. The VCO capacitance array calibration `FSCAL1` register value must be found for each RF frequency to be used. The VCO current calibration value and the charge pump current calibration value available in `FSCAL2` and `FSCAL3` respectively are not dependent on the RF frequency, so the same value can therefore be used for all RF frequencies for these two registers. Between each frequency hop, the calibration process can then be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values that corresponds to the next RF frequency. The PLL turn on time is approximately 90 µs. The blanking interval between each frequency hop is then approximately 90 µs.

3) Run calibration on a single frequency at startup. Next write 0 to `FSCAL3 [5:4]` to disable the charge pump calibration. After writing to `FSCAL3 [5:4]`, strobe `SRX` (or `STX`) with `MCSM0.FS_AUTOCAL=1` for each new frequency hop. That is, VCO current and VCO capacitance calibration is done, but not charge pump current calibration. When charge pump current calibration is disabled the calibration time is reduced from approximately 720 µs to approximately 150 µs. The blanking interval between each frequency hop is then approximately 240 µs.

There is a trade off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2) above gives the shortest blanking interval, but requires more memory space to store calibration values. This solution also requires that the supply voltage and temperature do not vary much in order to have a robust solution. Solution 3) gives approximately 570 µs smaller blanking interval than solution 1).

The recommended settings for `TEST0.VCO_SEL_CAL_EN` changes with frequency. This means that one should always use SmartRF® Studio [8] to get the correct settings for a specific frequency before doing a calibration, regardless of which calibration method is being used.

Note: The content in the `TESTn` registers (n = 0, 1, or 2) are not retained in SLEEP state, thus it is necessary to re-write these registers when returning from the SLEEP state.

28.3 Data Burst Transmissions

The high maximum data rate of the **CC1100E** opens up for burst transmissions. A low average data rate link (e.g. 10 kBaud) can be realized by using a higher over-the-air data rate. Buffering the data and transmitting in bursts at high data rate (e.g. 500 kBaud) will reduce the time in active mode, and hence also reduce the average current consumption significantly. Reducing the time in active mode will reduce the likelihood of collisions with other systems in the same frequency range.

Note: The sensitivity and thus transmission range is reduced for high data rate bursts compared to lower data rates.

28.4 Continuous Transmissions

In data streaming applications, the **CC1100E** opens up for continuous transmissions at a 500 kBaud effective data rate. As the modulation is done with a closed loop PLL, there is no limitation in the length of a transmission (open loop modulation used in some transceivers often prevents this kind of continuous data streaming and reduces the effective data rate).

28.5 Low Cost Systems

As the **CC1100E** provides 1.2 - 500 kBaud multi-channel performance without any external SAW or loop filters, a very low cost system can be made.

A HC-49 type SMD crystal is used in the CC1100E EM reference designs ([3] and 0). The crystal package strongly influences the price. In a size constrained PCB design, a smaller, but more expensive, crystal may be used.

28.6 Battery Operated Systems

In low power applications, the SLEEP state with the crystal oscillator core switched off should be used when the **CC1100E** is not active. It is possible to leave the crystal oscillator core running in the SLEEP state if start-up time is critical. The WOR functionality should be used in low power applications.

28.7 Increasing Output Power

In some applications it may be necessary to extend the link range. Adding an external power amplifier is the most effective way of doing this. The power amplifier should be inserted between the antenna and the balun and matching circuit. Two T/R switches are needed to disconnect the PA in RX mode, see details in Figure 28.

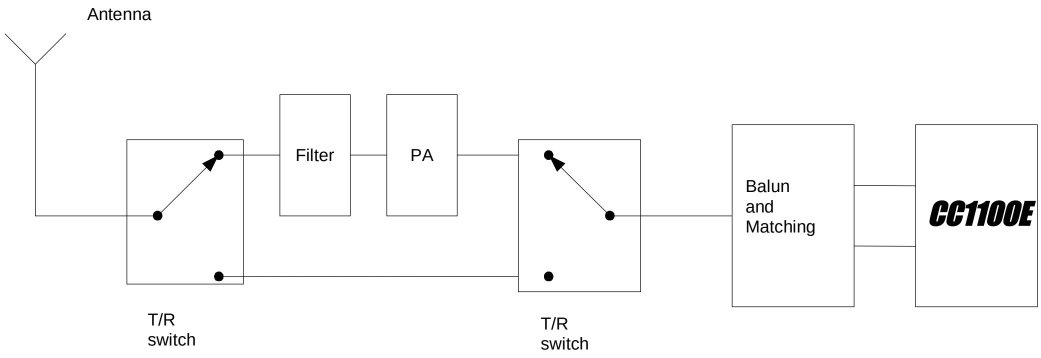


Figure 28: Block Diagram of the CC1100E Usage with External Power Amplifier

29 Configuration Registers

The configuration of the **CC1100E** is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software [8]. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset, all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 13 command strobe registers, listed in Table 38. Accessing these registers will initiate the change of an internal state or mode. There are 47 normal 8-bit configuration registers listed in Table 39. Many of these registers are for test purposes only, and need not be written for normal operation of the **CC1100E**.

There are also 12 status registers that are listed in Table 40. These registers, which are read-only, contain information about the status of the **CC1100E**.

The two FIFOs are accessed through one 8-bit register. Write operations write to the TX FIFO, while read operations read from the RX FIFO.

During the header byte transfer and while writing data to a register or the TX FIFO, a status byte is returned on the SO line. This status byte is described in Table 21 on page 27.

Table 41 summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if `MCSM0.FS_AUTOCAL`=1). If in RX (with CCA): Go to a wait state where only the synthesizer is running (for quick RX / TX turnaround).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. `SCAL` can be strobed from IDLE mode without setting manual calibration mode (`MCSM0.FS_AUTOCAL`=0)
0x34	SRX	Enable RX. Perform calibration first if coming from IDLE and `MCSM0.FS_AUTOCAL`=1.
0x35	STX	In IDLE state: Enable TX. Perform calibration first if `MCSM0.FS_AUTOCAL`=1. If in RX state and CCA is enabled: Only go to TX if channel is clear.
0x36	SIDLE	Exit RX / TX, turn off frequency synthesizer and exit Wake-On-Radio mode if applicable.
0x38	SWOR	Start automatic RX polling sequence (Wake-on-Radio) as described in Section 19.5 if `WORCTRL.RC_PD=0`.
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue `SFRX` in IDLE or RXFIFO_OVERFLOW states.
0x3B	SFTX	Flush the TX FIFO buffer. Only issue `SFTX` in IDLE or TXFIFO_UNDERFLOW states.
0x3C	SWORRST	Reset real time clock to Event1 value.
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

Table 38: Command Strobes

Address	Register	Description	Preserved in SLEEP State	Details on Page Number
0x00	IOCFG2	`GDO2` output pin configuration	Yes	64
0x01	IOCFG1	`GDO1` output pin configuration	Yes	64
0x02	IOCFG0	`GDO0` output pin configuration	Yes	64
0x03	FIFOTHR	RX FIFO and TX FIFO thresholds	Yes	65
0x04	SYNC1	Sync word, high byte	Yes	66
0x05	SYNC0	Sync word, low byte	Yes	66
0x06	PKTLEN	Packet length	Yes	66
0x07	PKTCTRL1	Packet automation control	Yes	66
0x08	PKTCTRL0	Packet automation control	Yes	67
0x09	ADDR	Device address	Yes	67
0x0A	CHANNR	Channel number	Yes	67
0x0B	FSCTRL1	Frequency synthesizer control	Yes	68
0x0C	FSCTRL0	Frequency synthesizer control	Yes	68
0x0D	FREQ2	Frequency control word, high byte	Yes	68
0x0E	FREQ1	Frequency control word, middle byte	Yes	68
0x0F	FREQ0	Frequency control word, low byte	Yes	68
0x10	MDMCFG4	Modem configuration	Yes	69
0x11	MDMCFG3	Modem configuration	Yes	69
0x12	MDMCFG2	Modem configuration	Yes	70
0x13	MDMCFG1	Modem configuration	Yes	71
0x14	MDMCFG0	Modem configuration	Yes	71
0x15	DEVIATN	Modem deviation setting	Yes	72
0x16	MCSM2	Main Radio Control State Machine configuration	Yes	73
0x17	MCSM1	Main Radio Control State Machine configuration	Yes	74
0x18	MCSM0	Main Radio Control State Machine configuration	Yes	75
0x19	FOCCFG	Frequency Offset Compensation configuration	Yes	76
0x1A	BSCFG	Bit Synchronization configuration	Yes	77
0x1B	AGCTRL2	AGC control	Yes	78
0x1C	AGCTRL1	AGC control	Yes	79
0x1D	AGCTRL0	AGC control	Yes	80
0x1E	WOREVT1	High byte Event 0 timeout	Yes	80
0x1F	WOREVT0	Low byte Event 0 timeout	Yes	81
0x20	WORCTRL	Wake On Radio control	Yes	81
0x21	FREND1	Front end RX configuration	Yes	82
0x22	FREND0	Front end TX configuration	Yes	82
0x23	FSCAL3	Frequency synthesizer calibration	Yes	82
0x24	FSCAL2	Frequency synthesizer calibration	Yes	83
0x25	FSCAL1	Frequency synthesizer calibration	Yes	83
0x26	FSCAL0	Frequency synthesizer calibration	Yes	83
0x27	RCCTRL1	RC oscillator configuration	Yes	83
0x28	RCCTRL0	RC oscillator configuration	Yes	83
0x29	FSTEST	Frequency synthesizer calibration control	No	84
0x2A	PTEST	Production test	No	84
0x2B	AGCTEST	AGC test	No	84
0x2C	TEST2	Various test settings	No	84
0x2D	TEST1	Various test settings	No	84
0x2E	TEST0	Various test settings	No	85

Table 39: Configuration Registers Overview

Address	Register	Description	Details on page number
0x30 (0xF0)	PARTNUM	Part number for the **CC1100E**	85
0x31 (0xF1)	VERSION	Current version number	85
0x32 (0xF2)	FREQEST	Frequency Offset Estimate	85
0x33 (0xF3)	LQI	Demodulator estimate for Link Quality	85
0x34 (0xF4)	RSSI	Received signal strength indication	85
0x35 (0xF5)	MARCSTATE	Control state machine state	86
0x36 (0xF6)	WORTIME1	High byte of WOR timer	86
0x37 (0xF7)	WORTIME0	Low byte of WOR timer	86
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	87
0x39 (0xF9)	VCO_VC_DAC	Current setting from PLL calibration module	87
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO	87
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO	87
0x3C (0xFC)	RCCTRL1_STATUS	Last RC oscillator calibration result	87
0x3D (0xFD)	RCCTRL0_STATUS	Last RC oscillator calibration result	88

Table 40: Status Registers Overview

	Write		Read		
	Single Byte	Burst	Single Byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	WOREVT1				
0x1F	WOREVT0				
0x20	WORCTRL				
0x21	FREND1				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	RCCTRL1				
0x28	RCCTRL0				
0x29	FSTEST				
0x2A	PTEST				
0x2B	AGCTEST				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F					
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	LQI	
0x34	SRX		SRX	RSSI	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	WORTIME1	
0x37				WORTIME0	
0x38	SWOR		SWOR	PKTSTATUS	
0x39	SPWD		SPWD	VCO_VC_DAC	
0x3A	SFRX		SFRX	TXBYTES	
0x3B	SFTX		SFTX	RXBYTES	
0x3C	SWORRST		SWORRST	RCCTRL1_STATUS	
0x3D	SNOP		SNOP	RCCTRL0_STATUS	
0x3E	PATABLE	PATABLE	PATABLE	PATABLE	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

Table 41: SPI Address Space

29.1 Configuration Register Details – Registers with preserved values in SLEEP state

0x00: IOCFG2 – GDO2 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6	GDO2_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	41 (0x29)	R/W	Default is `CHP_RDYn` (See Table 36 on page 55).

0x01: IOCFG1 – GDO1 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO1_CFG[5:0]	46 (0x2E)	R/W	Default is 3-state (See Table 36 on page 55).

0x02: IOCFG0 – GDO0 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor.
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (See Table 36 on page 55). It is recommended to disable the clock output in initialization, in order to optimize RF performance.

0x03: FIFOTHR – RX FIFO and TX FIFO Thresholds

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td></td><td>0</td><td>R/W</td><td>Reserved , write 0 for compatibility with possible future extensions</td></tr>
<tr><td>6</td><td>ADC_RETENTION</td><td>0</td><td>R/W</td><td>0: TEST1 = 0x31 and TEST2= 0x88 when waking up from SLEEP
1: TEST1 = 0x35 and TEST2 = 0x81 when waking up from SLEEP
Note that the changes in the TEST registers due to the ADC_RETENTION bit setting are only seen INTERNALLY in the analog part. The values read from the TEST registers when waking up from SLEEP mode will always be the reset value.
The ADC_RETENTION bit should be set to 1 before going into SLEEP mode if settings with an RX filter bandwidth below 325 kHz are wanted at time of wake-up.</td></tr>
<tr><td>5:4</td><td>CLOSE_IN_RX [1:0]</td><td>0 (00)</td><td>R/W</td><td>For more details, please see DN010 [11]
<table>
<tr><th>Setting</th><th>RX Attenuation, Typical Values</th></tr>
<tr><td>0 (00)</td><td>0dB</td></tr>
<tr><td>1 (01)</td><td>6dB</td></tr>
<tr><td>2 (10)</td><td>12dB</td></tr>
<tr><td>3 (11)</td><td>18dB</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>FIFO_THR[3:0]</td><td>7 (0111)</td><td>R/W</td><td>Set the threshold for the TX FIFO and RX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value.
<table>
<tr><th>Setting</th><th>Bytes in TX FIFO</th><th>Bytes in RX FIFO</th></tr>
<tr><td>0 (0000)</td><td>61</td><td>4</td></tr>
<tr><td>1 (0001)</td><td>57</td><td>8</td></tr>
<tr><td>2 (0010)</td><td>53</td><td>12</td></tr>
<tr><td>3 (0011)</td><td>49</td><td>16</td></tr>
<tr><td>4 (0100)</td><td>45</td><td>20</td></tr>
<tr><td>5 (0101)</td><td>41</td><td>24</td></tr>
<tr><td>6 (0110)</td><td>37</td><td>28</td></tr>
<tr><td>7 (0111)</td><td>33</td><td>32</td></tr>
<tr><td>8 (1000)</td><td>29</td><td>36</td></tr>
<tr><td>9 (1001)</td><td>25</td><td>40</td></tr>
<tr><td>10 (1010)</td><td>21</td><td>44</td></tr>
<tr><td>11 (1011)</td><td>17</td><td>48</td></tr>
<tr><td>12 (1100)</td><td>13</td><td>52</td></tr>
<tr><td>13 (1100E)</td><td>9</td><td>56</td></tr>
<tr><td>14 (1110)</td><td>5</td><td>60</td></tr>
<tr><td>15 (1111)</td><td>1</td><td>64</td></tr>
</table></td></tr>
</table>

0x04: SYNC1 – Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 – Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN – Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length mode is enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed.

0x07: PKTCTRL1 – Packet Automation Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:5</td><td>PQT[2:0]</td><td>0 (0x00)</td><td>R/W</td><td>Preamble quality estimator threshold. The preamble quality estimator increases an internal counter by one each time a bit is received that is different from the previous bit, and decreases the counter by 8 each time a bit is received that is the same as the last bit.
A threshold of 4·<code>PQT</code> for this counter is used to gate sync word detection. When <code>PQT=0</code> a sync word is always accepted.</td></tr>
<tr><td>4</td><td></td><td>0</td><td>R0</td><td>Not Used.</td></tr>
<tr><td>3</td><td>CRC_AUTOFLUSH</td><td>0</td><td>R/W</td><td>Enable automatic flush of RX FIFO when CRC is not OK. This requires that only one packet is in the RXIFIFO and that packet length is limited to the RX FIFO size.</td></tr>
<tr><td>2</td><td>APPEND_STATUS</td><td>1</td><td>R/W</td><td>When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain RSSI and LQI values, as well as CRC OK.</td></tr>
<tr><td>1:0</td><td>ADR_CHK[1:0]</td><td>0 (00)</td><td>R/W</td><td>Controls address check configuration of received packages.
<table>
<tr><th>Setting</th><th>Address check configuration</th></tr>
<tr><td>0 (00)</td><td>No address check</td></tr>
<tr><td>1 (01)</td><td>Address check, no broadcast</td></tr>
<tr><td>2 (10)</td><td>Address check and 0 (0x00) broadcast</td></tr>
<tr><td>3 (11)</td><td>Address check and 0 (0x00) and 255 (0xFF) broadcast</td></tr>
</table>
</td></tr>
</table>

0x08: PKTCTRL0 – Packet Automation Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>6</td><td>WHITE_DATA</td><td>1</td><td>R/W</td><td>Turn data whitening on / off
0: Whitening off
1: Whitening on</td></tr>
<tr><td>5:4</td><td>PKT_FORMAT[1:0]</td><td>0 (00)</td><td>R/W</td><td>Format of RX and TX data
<table>
<tr><th>Setting</th><th>Packet format</th></tr>
<tr><td>0 (00)</td><td>Normal mode, use FIFOs for RX and TX</td></tr>
<tr><td>1 (01)</td><td>Synchronous serial mode, Data in on GDO0 and data out on either of the GDOx pins</td></tr>
<tr><td>2 (10)</td><td>Random TX mode; sends random data using PN9 generator. Used for test.
Works as normal mode, setting 0 (00), in RX</td></tr>
<tr><td>3 (11)</td><td>Asynchronous serial mode, Data in on GDO0 and data out on either of the GDOx pins</td></tr>
</table></td></tr>
<tr><td>3</td><td></td><td>0</td><td>R0</td><td>Not used</td></tr>
<tr><td>2</td><td>CRC_EN</td><td>1</td><td>R/W</td><td>1: CRC calculation in TX and CRC check in RX enabled
0: CRC disabled for TX and RX</td></tr>
<tr><td>1:0</td><td>LENGTH_CONFIG[1:0]</td><td>1 (01)</td><td>R/W</td><td>Configure the packet length
<table>
<tr><th>Setting</th><th>Packet length configuration</th></tr>
<tr><td>0 (00)</td><td>Fixed packet length mode. Length configured in PKTLEN register</td></tr>
<tr><td>1 (01)</td><td>Variable packet length mode. Packet length configured by the first byte after sync word</td></tr>
<tr><td>2 (10)</td><td>Infinite packet length mode</td></tr>
<tr><td>3 (11)</td><td>Reserved</td></tr>
</table></td></tr>
</table>

0x09: ADDR – Device Address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR – Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 – Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5		0	R/W	Reserved
4:0	FREQ_IF[4:0]	15 (0x0F)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$ The default value gives an IF frequency of 381kHz, assuming a 26.0 MHz crystal.

0x0C: FSCTRL0 – Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the frequency synthesizer. (2s-complement). Resolution is $F_{XTAL}/2^{14}$ (1.59kHz-1.65kHz); range is ±202 kHz to ±210 kHz, dependent of XTAL frequency.

0x0D: FREQ2 – Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	0 (00)	R	`FREQ[23:22]` is always 0 (the `FREQ2` register is less than 36 with 26-27 MHz crystal)
5:0	FREQ[21:16]	30 (0x1E)	R/W	`FREQ [23:0]` is the base frequency for the frequency synthesiser in increments of $f_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$

0x0E: FREQ1 – Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. `FREQ2` register

0x0F: FREQ0 – Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. `FREQ2` register

0x10: MDMCFG4 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	2 (0x02)	R/W	
5:4	CHANBW_M[1:0]	0 (0x00)	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. $BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$ The default values give 203 kHz channel filter bandwidth, assuming a 26.0 MHz crystal.
3:0	DRATE_E[3:0]	12 (0x0C)	R/W	The exponent of the user specified symbol rate

0x11: MDMCFG3 – Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9^{th} bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.

0x12: MDMCFG2 – Modem Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>DEM_DCFILT_OFF</td><td>0</td><td>R/W</td><td>Disable digital DC blocking filter before demodulator.
0 = Enable (better sensitivity)
1 = Disable (current optimized). Only for data rates ≤ 250 kBaud
The recommended IF frequency changes when the DC blocking is disabled. Please use SmartRF® Studio [8] to calculate correct register setting.</td></tr>
<tr><td>6:4</td><td>MOD_FORMAT[2:0]</td><td>0 (000)</td><td>R/W</td><td>The modulation format of the radio signal
<table>
<tr><th>Setting</th><th>Modulation format</th></tr>
<tr><td>0 (000)</td><td>2-FSK</td></tr>
<tr><td>1 (001)</td><td>GFSK</td></tr>
<tr><td>2 (010)</td><td>-</td></tr>
<tr><td>3 (011)</td><td>ASK/OOK</td></tr>
<tr><td>4 (100)</td><td>-</td></tr>
<tr><td>5 (101)</td><td>-</td></tr>
<tr><td>6 (110)</td><td>-</td></tr>
<tr><td>7 (111)</td><td>MSK</td></tr>
</table>
ASK is only supported for output powers up to -1 dBm
MSK is only supported for data rates above 26 kBaud</td></tr>
<tr><td>3</td><td>MANCHESTER_EN</td><td>0</td><td>R/W</td><td>Enables Manchester encoding/decoding.
0 = Disable
1 = Enable</td></tr>
<tr><td>2:0</td><td>SYNC_MODE[2:0]</td><td>2 (010)</td><td>R/W</td><td>Combined sync-word qualifier mode.
The values 0 (000) and 4 (100) disables preamble and sync word transmission in TX and preamble and sync word detection in RX.
The values 1 (001), 2 (010), 5 (101) and 6 (110) enables 16-bit sync word transmission in TX and 16-bits sync word detection in RX. Only 15 of 16 bits need to match in RX when using setting 1 (001) or 5 (101). The values 3 (011) and 7 (111) enables repeated sync word transmission in TX and 32-bits sync word detection in RX (only 30 of 32 bits need to match).
<table>
<tr><th>Setting</th><th>Sync-word qualifier mode</th></tr>
<tr><td>0 (000)</td><td>No preamble/sync</td></tr>
<tr><td>1 (001)</td><td>15/16 sync word bits detected</td></tr>
<tr><td>2 (010)</td><td>16/16 sync word bits detected</td></tr>
<tr><td>3 (011)</td><td>30/32 sync word bits detected</td></tr>
<tr><td>4 (100)</td><td>No preamble/sync, carrier-sense above threshold</td></tr>
<tr><td>5 (101)</td><td>15/16 + carrier-sense above threshold</td></tr>
<tr><td>6 (110)</td><td>16/16 + carrier-sense above threshold</td></tr>
<tr><td>7 (111)</td><td>30/32 + carrier-sense above threshold</td></tr>
</table></td></tr>
</table>

0x13: MDMCFG1– Modem Configuration

Bit	Field Name	Reset	R/W	Description
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload 0 = Disable 1 = Enable (Only supported for fixed packet length mode, i.e. `PKTCTRL0.LENGTH_CONFIG=0`)
6:4	NUM_PREAMBLE[2:0]	2 (010)	R/W	Sets the minimum number of preamble bytes to be transmitted Setting / Number of preamble bytes 0 (000) / 2 1 (001) / 3 2 (010) / 4 3 (011) / 6 4 (100) / 8 5 (101) / 12 6 (110) / 16 7 (111) / 24
3:2			R0	Not used
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing

0x14: MDMCFG0– Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing. The channel spacing is multiplied by the channel number `CHAN` and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E}$ The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.

0x15: DEVIATN – Modem Deviation Setting

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used.	
6:4	DEVIATION_E[2:0]	4 (100)	R/W	Deviation exponent.	
3			R0	Not used.	
2:0	DEVIATION_M[2:0]	7 (111)	R/W	TX	
				2-FSK/ GFSK	Specifies the nominal frequency deviation from the carrier for a '0' (-DEVIATN) and '1' (+DEVIATN) in a mantissa-exponent format, interpreted as a 4-bit value with MSB implicit 1. The resulting frequency deviation is given by: $f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$ The default values give ±47.607 kHz deviation assuming 26.0 MHz crystal frequency.
				MSK	Specifies the fraction of symbol period (1/8-8/8) during which a phase change occurs ('0': +90deg, '1':-90deg). Refer to the SmartRF® Studio software [8] for correct DEVIATN setting when using MSK.
				ASK/OOK	This setting has no effect.
				RX	
				2-FSK/ GFSK	Specifies the expected frequency deviation of incoming signal, must be approximately right for demodulation to be performed reliably and robustly.
				MSK/ ASK/OOK	This setting has no effect.

0x16: MCSM2 – Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:5			R0	Not used
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense). For ASK/OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.
3	RX_TIME_QUAL	0	R/W	When the `RX_TIME` timer expires, the chip checks if sync word is found when `RX_TIME_QUAL=0`, or either sync word is found or PQI is set when `RX_TIME_QUAL=1.`
2:0	RX_TIME[2:0]	7 (111)	R/W	Timeout for sync word search in RX for both WOR mode and normal RX operation. The timeout is relative to the programmed `EVENT0` timeout.

The RX timeout in µs is given by `EVENT0`·C(`RX_TIME`, `WOR_RES`) ·26/X, where C is given by the table below and X is the crystal oscillator frequency in MHz:

Setting	WOR_RES = 0	WOR_RES = 1	WOR_RES = 2	WOR_RES = 3
0 (000)	3.6058	18.0288	32.4519	46.8750
1 (001)	1.8029	9.0144	16.2260	23.4375
2 (010)	0.9014	4.5072	8.1130	11.7188
3 (011)	0.4507	2.2536	4.0565	5.8594
4 (100)	0.2254	1.1268	2.0282	2.9297
5 (101)	0.1127	0.5634	1.0141	1.4648
6 (110)	0.0563	0.2817	0.5071	0.7324
7 (111)	Until end of packet			

As an example, `EVENT0=34666`, `WOR_RES=0` and `RX_TIME=6` corresponds to 1.96 ms RX timeout, 1 s polling interval and 0.195% duty cycle. Note that `WOR_RES` should be 0 or 1 when using WOR because using `WOR_RES` > 1 will give a very low duty cycle. In applications where WOR is not used all settings of `WOR_RES` can be used.

The duty cycle using WOR is approximated by:

Setting	`WOR_RES=0`	`WOR_RES=1`
0 (000)	12.50%	1.95%
1 (001)	6.250%	9765ppm
2 (010)	3.125%	4883ppm
3 (011)	1.563%	2441ppm
4 (100)	0.781%	NA
5 (101)	0.391%	NA
6 (110)	0.195%	NA
7 (111)	NA	

Note that the RC oscillator must be enabled in order to use setting 0-6, because the timeout counts RC oscillator periods. WOR mode does not need to be enabled.
The timeout counter resolution is limited: With `RX_TIME=0`, the timeout count is given by the 13 MSBs of `EVENT0`, decreasing to the 7MSBs of `EVENT0` with `RX_TIME=6`.

0x17: MCSM1– Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>5:4</td><td>CCA_MODE[1:0]</td><td>3 (11)</td><td>R/W</td><td>Selects <code>CCA_MODE</code>; Reflected in CCA signal
<table>
<tr><th>Setting</th><th>Clear channel indication</th></tr>
<tr><td>0 (00)</td><td>Always</td></tr>
<tr><td>1 (01)</td><td>If RSSI below threshold</td></tr>
<tr><td>2 (10)</td><td>Unless currently receiving a packet</td></tr>
<tr><td>3 (11)</td><td>If RSSI below threshold unless currently receiving a packet</td></tr>
</table></td></tr>
<tr><td>3:2</td><td>RXOFF_MODE[1:0]</td><td>0 (00)</td><td>R/W</td><td>Select what should happen when a packet has been received
<table>
<tr><th>Setting</th><th>Next state after finishing packet reception</th></tr>
<tr><td>0 (00)</td><td><code>IDLE</code></td></tr>
<tr><td>1 (01)</td><td>FSTXON</td></tr>
<tr><td>2 (10)</td><td>TX</td></tr>
<tr><td>3 (11)</td><td>Stay in RX</td></tr>
</table>
It is not possible to set <code>RXOFF_MODE</code> to be TX or FSTXON and at the same time use CCA.</td></tr>
<tr><td>1:0</td><td>TXOFF_MODE[1:0]</td><td>0 (00)</td><td>R/W</td><td>Select what should happen when a packet has been sent (TX)
<table>
<tr><th>Setting</th><th>Next state after finishing packet transmission</th></tr>
<tr><td>0 (00)</td><td>IDLE</td></tr>
<tr><td>1 (01)</td><td>FSTXON</td></tr>
<tr><td>2 (10)</td><td>Stay in TX (start sending preamble)</td></tr>
<tr><td>3 (11)</td><td>RX</td></tr>
</table></td></tr>
</table>

0x18: MCSM0– Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>5:4</td><td>FS_AUTOCAL[1:0]</td><td>0 (00)</td><td>R/W</td><td>Automatically calibrate when going to RX or TX, or back to IDLE
<table>
<tr><th>Setting</th><th>When to perform automatic calibration</th></tr>
<tr><td>0 (00)</td><td>Never (manually calibrate using SCAL strobe)</td></tr>
<tr><td>1 (01)</td><td>When going from IDLE to RX or TX (or FSTXON)</td></tr>
<tr><td>2 (10)</td><td>When going from RX or TX back to IDLE automatically</td></tr>
<tr><td>3 (11)</td><td>Every 4th time when going from RX or TX to IDLE automatically</td></tr>
</table>
In some automatic wake-on-radio (WOR) applications, using setting 3 (11) can significantly reduce current consumption.</td></tr>
<tr><td>3:2</td><td>PO_TIMEOUT</td><td>1 (01)</td><td>R/W</td><td>Programs the number of times the six-bit ripple counter must expire after XOSC has stabilized before CHP_RDYn goes low.
If XOSC is on (stable) during power-down, PO_TIMEOUT should be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT=2 recommended). Typical start-up time for the voltage regulator is 50 μs.
If XOSC is off during power-down and the regulated digital supply voltage has sufficient time to stabilize while waiting for the crystal to be stable, PO_TIMEOUT can be set to 0. For robust operation it is recommended to use PO_TIMEOUT=2.
<table>
<tr><th>Setting</th><th>Expire count</th><th>Timeout after XOSC start</th></tr>
<tr><td>0 (00)</td><td>1</td><td>Approx. 2.3 – 2.4 μs</td></tr>
<tr><td>1 (01)</td><td>16</td><td>Approx. 37 – 39 μs</td></tr>
<tr><td>2 (10)</td><td>64</td><td>Approx. 149 – 155 μs</td></tr>
<tr><td>3 (11)</td><td>256</td><td>Approx. 597 – 620 μs</td></tr>
</table>
Exact timeout depends on crystal frequency.</td></tr>
<tr><td>1</td><td>PIN_CTRL_EN</td><td>0</td><td>R/W</td><td>Enables the pin radio control option</td></tr>
<tr><td>0</td><td>XOSC_FORCE_ON</td><td>0</td><td>R/W</td><td>Force the XOSC to stay on in the SLEEP state.</td></tr>
</table>

0x19: FOCCFG – Frequency Offset Compensation Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>5</td><td>FOC_BS_CS_GATE</td><td>1</td><td>R/W</td><td>If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CS signal goes high.</td></tr>
<tr><td>4:3</td><td>FOC_PRE_K[1:0]</td><td>2 (10)</td><td>R/W</td><td>The frequency compensation loop gain to be used before a sync word is detected.
<table>
<tr><th>Setting</th><th>Freq. compensation loop gain before sync word</th></tr>
<tr><td>0 (00)</td><td>K</td></tr>
<tr><td>1 (01)</td><td>$2K$</td></tr>
<tr><td>2 (10)</td><td>$3K$</td></tr>
<tr><td>3 (11)</td><td>$4K$</td></tr>
</table></td></tr>
<tr><td>2</td><td>FOC_POST_K</td><td>1</td><td>R/W</td><td>The frequency compensation loop gain to be used after a sync word is detected.
<table>
<tr><th>Setting</th><th>Freq. compensation loop gain after sync word</th></tr>
<tr><td>0</td><td>Same as FOC_PRE_K</td></tr>
<tr><td>1</td><td>$K/2$</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>FOC_LIMIT[1:0]</td><td>2 (10)</td><td>R/W</td><td>The saturation point for the frequency offset compensation algorithm:
<table>
<tr><th>Setting</th><th>Saturation point (max compensated offset)</th></tr>
<tr><td>0 (00)</td><td>±0 (no frequency offset compensation)</td></tr>
<tr><td>1 (01)</td><td>$\pm BW_{CHAN}/8$</td></tr>
<tr><td>2 (10)</td><td>$\pm BW_{CHAN}/4$</td></tr>
<tr><td>3 (11)</td><td>$\pm BW_{CHAN}/2$</td></tr>
</table>
Frequency offset compensation is not supported for ASK/OOK; Always use FOC_LIMIT=0 with these modulation formats.</td></tr>
</table>

0x1A: BSCFG – Bit Synchronization Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>BS_PRE_KI[1:0]</td><td>1 (01)</td><td>R/W</td><td>The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):
<table>
<tr><th>Setting</th><th>Clock recovery loop integral gain before sync word</th></tr>
<tr><td>0 (00)</td><td>K_I</td></tr>
<tr><td>1 (01)</td><td>$2K_I$</td></tr>
<tr><td>2 (10)</td><td>$3K_I$</td></tr>
<tr><td>3 (11)</td><td>$4K_I$</td></tr>
</table></td></tr>
<tr><td>5:4</td><td>BS_PRE_KP[1:0]</td><td>2 (10)</td><td>R/W</td><td>The clock recovery feedback loop proportional gain to be used before a sync word is detected.
<table>
<tr><th>Setting</th><th>Clock recovery loop proportional gain before sync word</th></tr>
<tr><td>0 (00)</td><td>K_P</td></tr>
<tr><td>1 (01)</td><td>$2K_P$</td></tr>
<tr><td>2 (10)</td><td>$3K_P$</td></tr>
<tr><td>3 (11)</td><td>$4K_P$</td></tr>
</table></td></tr>
<tr><td>3</td><td>BS_POST_KI</td><td>1</td><td>R/W</td><td>The clock recovery feedback loop integral gain to be used after a sync word is detected.
<table>
<tr><th>Setting</th><th>Clock recovery loop integral gain after sync word</th></tr>
<tr><td>0</td><td>Same as BS_PRE_KI</td></tr>
<tr><td>1</td><td>$K_I/2$</td></tr>
</table></td></tr>
<tr><td>2</td><td>BS_POST_KP</td><td>1</td><td>R/W</td><td>The clock recovery feedback loop proportional gain to be used after a sync word is detected.
<table>
<tr><th>Setting</th><th>Clock recovery loop proportional gain after sync word</th></tr>
<tr><td>0</td><td>Same as BS_PRE_KP</td></tr>
<tr><td>1</td><td>K_P</td></tr>
</table></td></tr>
<tr><td>1:0</td><td>BS_LIMIT[1:0]</td><td>0 (00)</td><td>R/W</td><td>The saturation point for the data rate offset compensation algorithm:
<table>
<tr><th>Setting</th><th>Data rate offset saturation (max data rate difference)</th></tr>
<tr><td>0 (00)</td><td>±0 (No data rate offset compensation performed)</td></tr>
<tr><td>1 (01)</td><td>±3.125 % data rate offset</td></tr>
<tr><td>2 (10)</td><td>±6.25 % data rate offset</td></tr>
<tr><td>3 (11)</td><td>±12.5 % data rate offset</td></tr>
</table></td></tr>
</table>

0x1B: AGCCTRL2 – AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:6</td><td>MAX_DVGA_GAIN[1:0]</td><td>0 (00)</td><td>R/W</td><td>Reduces the maximum allowable DVGA gain.
<table>
<tr><th>Setting</th><th>Allowable DVGA settings</th></tr>
<tr><td>0 (00)</td><td>All gain settings can be used</td></tr>
<tr><td>1 (01)</td><td>The highest gain setting can not be used</td></tr>
<tr><td>2 (10)</td><td>The 2 highest gain settings can not be used</td></tr>
<tr><td>3 (11)</td><td>The 3 highest gain settings can not be used</td></tr>
</table></td></tr>
<tr><td>5:3</td><td>MAX_LNA_GAIN[2:0]</td><td>0 (000)</td><td>R/W</td><td>Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.
<table>
<tr><th>Setting</th><th>Maximum allowable LNA + LNA 2 gain</th></tr>
<tr><td>0 (000)</td><td>Maximum possible LNA + LNA 2 gain</td></tr>
<tr><td>1 (001)</td><td>Approx. 2.6 dB below maximum possible gain</td></tr>
<tr><td>2 (010)</td><td>Approx. 6.1 dB below maximum possible gain</td></tr>
<tr><td>3 (011)</td><td>Approx. 7.4 dB below maximum possible gain</td></tr>
<tr><td>4 (100)</td><td>Approx. 9.2 dB below maximum possible gain</td></tr>
<tr><td>5 (101)</td><td>Approx. 11.5 dB below maximum possible gain</td></tr>
<tr><td>6 (110)</td><td>Approx. 14.6 dB below maximum possible gain</td></tr>
<tr><td>7 (111)</td><td>Approx. 17.1 dB below maximum possible gain</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>MAGN_TARGET[2:0]</td><td>3 (011)</td><td>R/W</td><td>These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).
<table>
<tr><th>Setting</th><th>Target amplitude from channel filter</th></tr>
<tr><td>0 (000)</td><td>24 dB</td></tr>
<tr><td>1 (001)</td><td>27 dB</td></tr>
<tr><td>2 (010)</td><td>30 dB</td></tr>
<tr><td>3 (011)</td><td>33 dB</td></tr>
<tr><td>4 (100)</td><td>36 dB</td></tr>
<tr><td>5 (101)</td><td>38 dB</td></tr>
<tr><td>6 (110)</td><td>40 dB</td></tr>
<tr><td>7 (111)</td><td>42 dB</td></tr>
</table></td></tr>
</table>

0x1C: AGCCTRL1 – AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>6</td><td>AGC_LNA_PRIORITY</td><td>1</td><td>R/W</td><td>Selects between two different strategies for LNA and LNA 2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA 2 gain is decreased to minimum before decreasing LNA gain.</td></tr>
<tr><td>5:4</td><td>CARRIER_SENSE_REL_THR[1:0]</td><td>0 (00)</td><td>R/W</td><td>Sets the relative change threshold for asserting carrier sense
<table>
<tr><td>Setting</td><td>Carrier sense relative threshold</td></tr>
<tr><td>0 (00)</td><td>Relative carrier sense threshold disabled</td></tr>
<tr><td>1 (01)</td><td>6 dB increase in RSSI value</td></tr>
<tr><td>2 (10)</td><td>10 dB increase in RSSI value</td></tr>
<tr><td>3 (11)</td><td>14 dB increase in RSSI value</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>CARRIER_SENSE_ABS_THR[3:0]</td><td>0 (0000)</td><td>R/W</td><td>Sets the absolute RSSI threshold for asserting carrier sense. The 2-complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.
<table>
<tr><td>Setting</td><td>Carrier sense absolute threshold
(Equal to channel filter amplitude when AGC has not decreased gain)</td></tr>
<tr><td>-8 (1000)</td><td>Absolute carrier sense threshold disabled</td></tr>
<tr><td>-7 (1001)</td><td>7 dB below MAGN_TARGET setting</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>-1 (1111)</td><td>1 dB below MAGN_TARGET setting</td></tr>
<tr><td>0 (0000)</td><td>At MAGN_TARGET setting</td></tr>
<tr><td>1 (0001)</td><td>1 dB above MAGN_TARGET setting</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>7 (0111)</td><td>7 dB above MAGN_TARGET setting</td></tr>
</table></td></tr>
</table>

0x1D: AGCCTRL0 – AGC Control

Bit	Field Name	Reset	R/W	Description
7:6	HYST_LEVEL[1:0]	2 (10)	R/W	Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determine gain changes). Setting / Description: 0 (00): No hysteresis, small symmetric dead zone, high gain 1 (01): Low hysteresis, small asymmetric dead zone, medium gain 2 (10): Medium hysteresis, medium asymmetric dead zone, medium gain 3 (11): Large hysteresis, large asymmetric dead zone, low gain
5:4	WAIT_TIME[1:0]	1 (01)	R/W	Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples. Setting / Channel filter samples: 0 (00): 8 1 (01): 16 2 (10): 24 3 (11): 32
3:2	AGC_FREEZE[1:0]	0 (00)	R/W	Control when the AGC gain should be frozen. Setting / Function: 0 (00): Normal operation. Always adjust gain when required. 1 (01): The gain setting is frozen when a sync word has been found. 2 (10): Manually freeze the analogue gain setting and continue to adjust the digital gain. 3 (11): Manually freezes both the analogue and the digital gain setting. Used for manually overriding the gain.
1:0	FILTER_LENGTH[1:0]	1 (01)	R/W	Sets the averaging length for the amplitude from the channel filter. Sets the OOK/ASK decision boundary for OOK/ASK reception. Setting / Channel filter samples / OOK/ASK decision boundary: 0 (00): 8, 4 dB 1 (01): 16, 8 dB 2 (10): 32, 12 dB 3 (11): 64, 16 dB

0x1E: WOREVT1 – High Byte Event0 Timeout

Bit	Field Name	Reset	R/W	Description
7:0	EVENT0[15:8]	135 (0x87)	R/W	High byte of `EVENT0` timeout register $t_{Event0} = \frac{750}{f_{XOSC}} \cdot EVENT0 \cdot 2^{5 \cdot WOR\_RES}$

0x1F: WOREVT0 –Low Byte Event0 Timeout

Bit	Field Name	Reset	R/W	Description
7:0	EVENT0[7:0]	107 (0x6B)	R/W	Low byte of `EVENT0` timeout register. The default `EVENT0` value gives 1.0s timeout, assuming a 26.0 MHz crystal.

0x20: WORCTRL – Wake On Radio Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>RC_PD</td><td>1</td><td>R/W</td><td>Power down signal to RC oscillator. When written to 0, automatic initial calibration will be performed</td></tr>
<tr><td>6:4</td><td>EVENT1[2:0]</td><td>7 (111)</td><td>R/W</td><td>Timeout setting from register block. Decoded to Event 1 timeout. RC oscillator clock frequency equals F_{XOSC}/750, which is 34.7 – 36 kHz, depending on crystal frequency. The table below lists the number of clock periods after Event 0 before Event 1 times out.
<table>
<tr><th>Setting</th><th>t_{Event1}</th></tr>
<tr><td>0 (000)</td><td>4 (0.111 – 0.115 ms)</td></tr>
<tr><td>1 (001)</td><td>6 (0.167 – 0.173 ms)</td></tr>
<tr><td>2 (010)</td><td>8 (0.222 – 0.230 ms)</td></tr>
<tr><td>3 (011)</td><td>12 (0.333 – 0.346 ms)</td></tr>
<tr><td>4 (100)</td><td>16 (0.444 – 0.462 ms)</td></tr>
<tr><td>5 (101)</td><td>24 (0.667 – 0.692 ms)</td></tr>
<tr><td>6 (110)</td><td>32 (0.889 – 0.923 ms)</td></tr>
<tr><td>7 (111)</td><td>48 (1.333 – 1.385 ms)</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>RC_CAL</td><td>1</td><td>R/W</td><td>Enables (1) or disables (0) the RC oscillator calibration.</td></tr>
<tr><td>2</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>1:0</td><td>WOR_RES</td><td>0 (00)</td><td>R/W</td><td>Controls the Event 0 resolution as well as maximum timeout of the WOR module and maximum timeout under normal RX operation::
<table>
<tr><th>Setting</th><th>Resolution (1 LSB)</th><th>Max timeout</th></tr>
<tr><td>0 (00)</td><td>1 period (28 – 29 μs)</td><td>1.8 – 1.9 seconds</td></tr>
<tr><td>1 (01)</td><td>2^{5} periods (0.89 – 0.92 ms)</td><td>58 – 61 seconds</td></tr>
<tr><td>2 (10)</td><td>2^{10} periods (28 – 30 ms)</td><td>31 – 32 minutes</td></tr>
<tr><td>3 (11)</td><td>2^{15} periods (0.91 – 0.94 s)</td><td>16.5 – 17.2 hours</td></tr>
</table>
Note that `WOR_RES` should be 0 or 1 when using WOR because `WOR_RES` > 1 will give a very low duty cycle.
In normal RX operation all settings of `WOR_RES` can be used.</td></tr>
</table>

0x21: FREND1 – Front End RX Configuration

Bit	Field Name	Reset	R/W	Description
7:6	LNA_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	1 (01)	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	2 (10)	R/W	Adjusts current in mixer

0x22: FREND0 – Front End TX Configuration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5:4	LODIV_BUF_CURRENT_TX[1:0]	1 (0x01)	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF® Studio software [8].
3			R0	Not used
2:0	PA_POWER[2:0]	0 (0x00)	R/W	Selects PA power setting. This value is an index to the PATABLE, which can be programmed with up to 8 different PA settings. In OOK/ASK mode, this selects the PATABLE index to use when transmitting a ‘1’. PATABLE index zero is used in OOK/ASK when transmitting a ‘0’. The PATABLE settings from index ‘0’ to the PA_POWER value are used for ASK TX shaping, and for power ramp-up/ramp-down at the start/end of transmission in all TX modulation formats.

0x23: FSCAL3 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (0x02)	R/W	Frequency synthesizer calibration configuration. The value to write in this field before calibration is given by the SmartRF® Studio software.
5:4	CHP_CURR_CAL_EN[1:0]	2 (0x02)	R/W	Disable charge pump calibration stage when 0.
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration results register. Digital bit vector defining the charge pump output current, on an exponential scale: $I\_OUT = I_0 \cdot 2^{FSCAL3[3:0]/4}$ Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency. Please note that for operation at 950-956 MHz targeting ARIB STD-T96 FSCAL3 [7:4] needs to be set to 0xA

0x24: FSCAL2 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[4:0]	10 (0x0A)	R/W	Frequency synthesizer calibration results register. VCO current calibration result and override value. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting `FSCAL3`, `FSCAL2` and `FSCAL1` register values. Between each frequency hop, calibration can be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values corresponding to the next RF frequency.

0x25: FSCAL1 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration results register. Capacitor array setting for VCO coarse tuning. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting `FSCAL3`, `FSCAL2` and `FSCAL1` register values. Between each frequency hop, calibration can be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values corresponding to the next RF frequency.

0x26: FSCAL0 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF® Studio software [8]. Please note that for operation at 950-956 MHz targeting ARIB STD-T96, FSCAL0 needs to be set to 0x07

0x27: RCCTRL1 – RC Oscillator Configuration

Bit	Field Name	Reset	R/W	Description
7		0	R0	Not used
6:0	RCCTRL1[6:0]	65 (0x41)	R/W	RC oscillator configuration.

0x28: RCCTRL0 – RC Oscillator Configuration

Bit	Field Name	Reset	R/W	Description
7		0	R0	Not used
6:0	RCCTRL0[6:0]	0 (0x00)	R/W	RC oscillator configuration.

29.2 Configuration Register Details – Registers that Loose Programming in SLEEP State

0x29: FSTEST – Frequency Synthesizer Calibration Control

Bit	Field Name	Reset	R/W	Description
7:0	FSTEST[7:0]	89 (0x59)	R/W	For test only. Do not write to this register.

0x2A: PTEST – Production Test

Bit	Field Name	Reset	R/W	Description
7:0	PTEST[7:0]	127 (0x7F)	R/W	Writing 0xBF to this register makes the on-chip temperature sensor available in the IDLE state. The default 0x7F value should then be written back before leaving the IDLE state. Other use of this register is for test only.

0x2B: AGCTEST – AGC Test

Bit	Field Name	Reset	R/W	Description
7:0	AGCTEST[7:0]	63 (0x3F)	R/W	For test only. Do not write to this register.

0x2C: TEST2 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	136 (0x88)	R/W	The value to use in this register is given by the SmartRF® Studio software [8]. This register will be forced to 0x88 or 0x81 when it wakes up from SLEEP mode, depending on the configuration of FIFOTHR. ADC_RETENTION. Note that the value read from this register when waking up from SLEEP always is the reset value (0x88) regardless of the ADC_RETENTION setting. The inversion of some of the bits due to the ADC_RETENTION setting is only seen INTERNALLY in the analog part.

0x2D: TEST1 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	The value to use in this register is given by the SmartRF® Studio software [8]. This register will be forced to 0x31 or 0x35 when it wakes up from SLEEP mode, depending on the configuration of FIFOTHR. ADC_RETENTION. Note that the value read from this register when waking up from SLEEP always is the reset value (0x31) regardless of the ADC_RETENTION setting. The inversion of some of the bits due to the ADC_RETENTION setting is only seen INTERNALLY in the analog part.

0x2E: TEST0 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2 (0x02)	R/W	The value to use in this register is given by the SmartRF® Studio software [8].
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	The value to use in this register is given by the SmartRF® Studio software [8].

29.3 Status Register Details

0x30 (0xF0): PARTNUM – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	0 (0x00)	R	Chip part number

0x31 (0xF1): VERSION – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	5 (0x05)	R	Chip version number.

0x32 (0xF2): FREQEST – Frequency Offset Estimate from Demodulator

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST		R	The estimated frequency offset (2's complement) of the carrier. Resolution is $F_{XTAL}/2^{14}$ (1.59 - 1.65 kHz); range is ±202 kHz to ±210 kHz, depending on XTAL frequency. Frequency offset compensation is only supported for 2-FSK, GFSK, and MSK modulation. This register will read 0 when using ASK or OOK modulation.

0x33 (0xF3): LQI – Demodulator Estimate for Link Quality

Bit	Field Name	Reset	R/W	Description
7	CRC OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0	LQI_EST[6:0]		R	The Link Quality Indicator estimates how easily a received signal can be demodulated. Calculated over the 64 symbols following the sync word

0x34 (0xF4): RSSI – Received Signal Strength Indication

Bit	Field Name	Reset	R/W	Description
7:0	RSSI		R	Received signal strength indicator

0x35 (0xF5): MARCSTATE – Main Radio Control State Machine State

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:5</td><td></td><td></td><td>R0</td><td>Not used</td></tr>
<tr><td>4:0</td><td>MARC_STATE[4:0]</td><td></td><td>R</td><td>Main Radio Control FSM State
<table>
<tr><th>Value</th><th>State name</th><th>State (Figure 20, page 45)</th></tr>
<tr><td>0 (0x00)</td><td>SLEEP</td><td>SLEEP</td></tr>
<tr><td>1 (0x01)</td><td>IDLE</td><td>IDLE</td></tr>
<tr><td>2 (0x02)</td><td>XOFF</td><td>XOFF</td></tr>
<tr><td>3 (0x03)</td><td>VCOON_MC</td><td>MANCAL</td></tr>
<tr><td>4 (0x04)</td><td>REGON_MC</td><td>MANCAL</td></tr>
<tr><td>5 (0x05)</td><td>MANCAL</td><td>MANCAL</td></tr>
<tr><td>6 (0x06)</td><td>VCOON</td><td>FS_WAKEUP</td></tr>
<tr><td>7 (0x07)</td><td>REGON</td><td>FS_WAKEUP</td></tr>
<tr><td>8 (0x08)</td><td>STARTCAL</td><td>CALIBRATE</td></tr>
<tr><td>9 (0x09)</td><td>BWBOOST</td><td>SETTLING</td></tr>
<tr><td>10 (0x0A)</td><td>FS_LOCK</td><td>SETTLING</td></tr>
<tr><td>11 (0x0B)</td><td>IFADCON</td><td>SETTLING</td></tr>
<tr><td>12 (0x0C)</td><td>ENDCAL</td><td>CALIBRATE</td></tr>
<tr><td>13 (0x0D)</td><td>RX</td><td>RX</td></tr>
<tr><td>14 (0x0E)</td><td>RX_END</td><td>RX</td></tr>
<tr><td>15 (0x0F)</td><td>RX_RST</td><td>RX</td></tr>
<tr><td>16 (0x10)</td><td>TXRX_SWITCH</td><td>TXRX_SETTLING</td></tr>
<tr><td>17 (0x11)</td><td>RXFIFO_OVERFLOW</td><td>RXFIFO_OVERFLOW</td></tr>
<tr><td>18 (0x12)</td><td>FSTXON</td><td>FSTXON</td></tr>
<tr><td>19 (0x13)</td><td>TX</td><td>TX</td></tr>
<tr><td>20 (0x14)</td><td>TX_END</td><td>TX</td></tr>
<tr><td>21 (0x15)</td><td>RXTX_SWITCH</td><td>RXTX_SETTLING</td></tr>
<tr><td>22 (0x16)</td><td>TXFIFO_UNDERFLOW</td><td>TXFIFO_UNDERFLOW</td></tr>
</table>
Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.</td></tr>
</table>

0x36 (0xF6): WORTIME1 – High Byte of WOR Time

Bit	Field Name	Reset	R/W	Description
7:0	TIME[15:8]		R	High byte of timer value in WOR module

0x37 (0xF7): WORTIME0 – Low Byte of WOR Time

Bit	Field Name	Reset	R/W	Description
7:0	TIME[7:0]		R	Low byte of timer value in WOR module

0x38 (0xF8): PKTSTATUS – Current GDOx Status and Packet Status

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS		R	Carrier sense
5	PQT_REACHED		R	Preamble Quality reached
4	CCA		R	Channel is clear
3	SFD		R	Sync word found. Asserted when sync word has been sent / received, and de-asserted at the end of the packet. In RX, this bit will de-assert when the optional address check fails or the radio enter RX_OVERFLOW state. In TX this bit will de-assert if the radio enters TX_UNDERFLOW state.
2	`GDO2`		R	Current GDO2 value. Note: the reading gives the non-inverted value irrespective of what `IOCFG2.GDO2_INV` is programmed to. It is not recommended to check for PLL lock by reading `PKTSTATUS [2]` with `GDO2_CFG=0x0A`.
1			R0	Not used
0	`GDO0`		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective of what `IOCFG0.GDO0_INV` is programmed to. It is not recommended to check for PLL lock by reading `PKTSTATUS [0]` with `GDO0_CFG=0x0A`.

0x39 (0xF9): VCO_VC_DAC – Current Setting from PLL Calibration Module

Bit	Field Name	Reset	R/W	Description
7:0	VCO_VC_DAC[7:0]		R	Status register for test only.

0x3A (0xFA): TXBYTES – Underflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO

0x3B (0xFB): RXBYTES – Overflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

0x3C (0xFC): RCCTRL1_STATUS – Last RC Oscillator Calibration Result

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6:0	RCCTRL1_STATUS[6:0]		R	Contains the value from the last run of the RC oscillator calibration routine. For usage description refer to AN047 [7]

0x3D (0xFD): RCCTRL0_STATUS – Last RC Oscillator Calibration Result

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6:0	RCCTRL0_STATUS[6:0]		R	Contains the value from the last run of the RC oscillator calibration routine. For usage description refer to Application Note AN047 [7].

30 Package Description (QFN 20)

30.1 Recommended PCB Layout for Package (QFN 20)

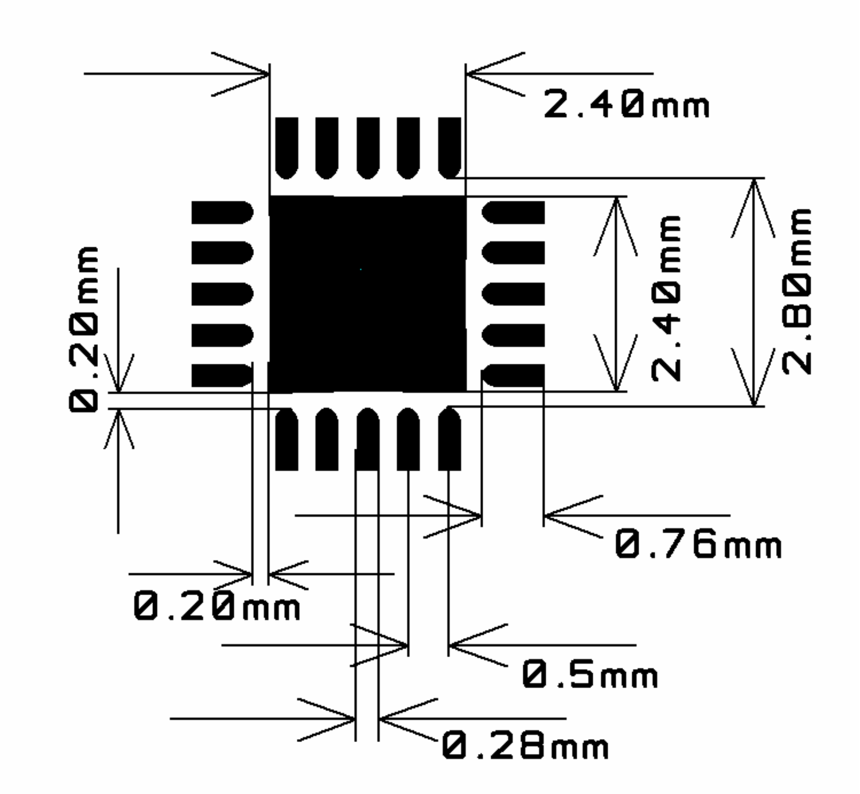


Figure 29: Recommended PCB Layout for QFN 20 Package

Note: Figure 29 is an illustration only and not to scale. There are five 10 mil via holes distributed symmetrically in the ground pad under the package. See also the CC1100EEM reference designs ([3] and [4]).

30.2 Soldering Information

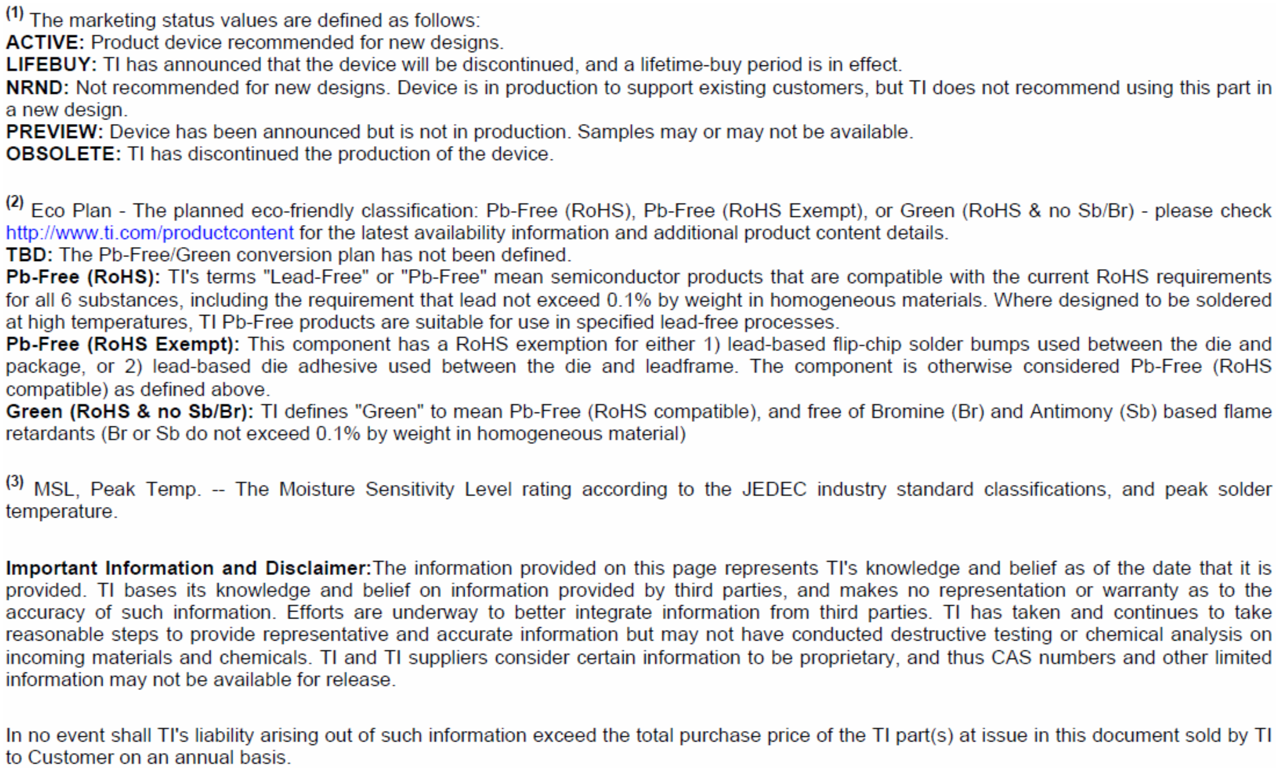
The recommendations for lead-free reflow in IPC/JEDEC J-STD-020 should be followed.

30.3 Ordering Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead Finish	MSL Peak Temp (3)
CC1100ERTKR	Active	QFN	RTK	20	3000	Green (RoHS & no Sb/Br)	Cu NiPdAu	LEVEL3-260C 1 YEAR
CC1100ERTKT	Active	QFN	RTK	20	250	Green (RoHS & no Sb/Br)	Cu NiPdAu	LEVEL3-260C 1 YEAR

Orderable Evaluation Module	Description	Minimum Order Quantity
CC1100E-EMK470	CC1100E Evaluation Module Kit, 470-510 MHz	1
CC1100E-EMK950	CC1100E Evaluation Module Kit, 950-960 MHz	1

Table 42: Ordering Information



(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

References

[1] CC1101 Datasheet

[2] CC1100 Datasheet

[3] CC1100E EM 470 MHz Reference Design

[4] CC1100E EM 950 MHz Reference Design

[5] CC1100E Errata Note

[6] ARIB STD-T96 ver.1.0

[7] AN047 CC1100/CC2500 – Wake-On-Radio (swra126.pdf)

[8] SmartRF® Studio (swrc046.zip)

[9] CC1100 CC1101 CC1100E CC2500 Examples Libraries (swrc021.zip)

[10] CC1100/CC1150DK, CC1101DK, and CC2500/CC2550DK Examples and Libraries User Manual (swru109.pdf)

[11] DN010 Close-in Reception with CC1101 (and CC1100E) (swra147.pdf)

[12] DN015 Permanent Frequency Offset Compensation (swra159.pdf)

[13] DN505 RSSI Interpretation and Timing (swra114.pdf)

[14] AN058 Antenna Selection Guide (swra161.pdf)

[15] DN022 CC11xx OOK/ASK register settings (swra215.pdf)

[16] DN005 CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy (swra122.pdf)

[17] DN501 PATABLE Access

[18] DN504 FEC Implementation

31 General Information

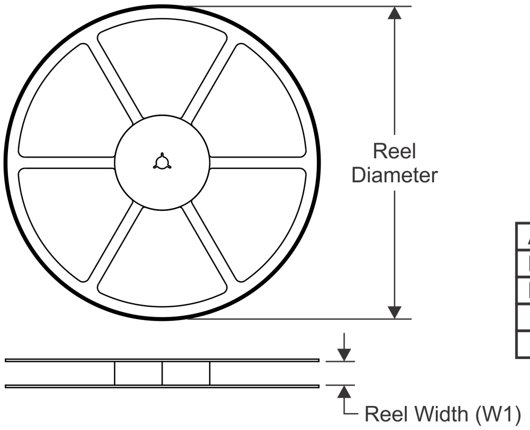
31.1 Document History

Revision	Date	Description/Changes
SWRS082	April 2009	First data sheet release

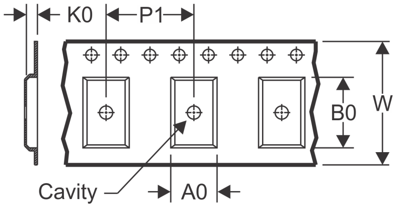
Table 43: Document History

TAPE AND REEL INFORMATION

REEL DIMENSIONS

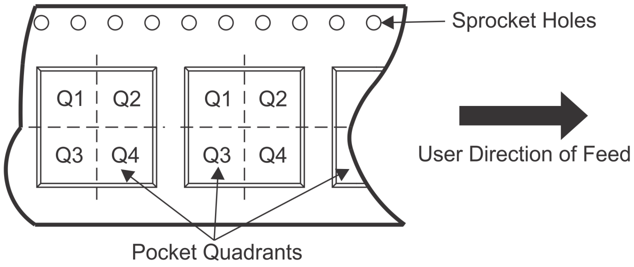


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

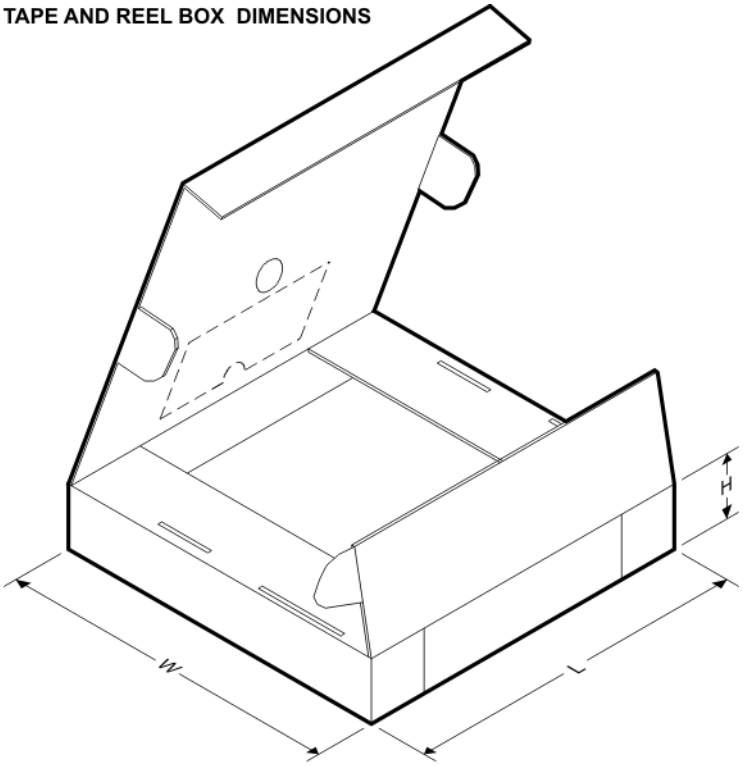
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1100ERGPR	QFN	RGP	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CC1100ERGPT	QFN	RGP	20	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

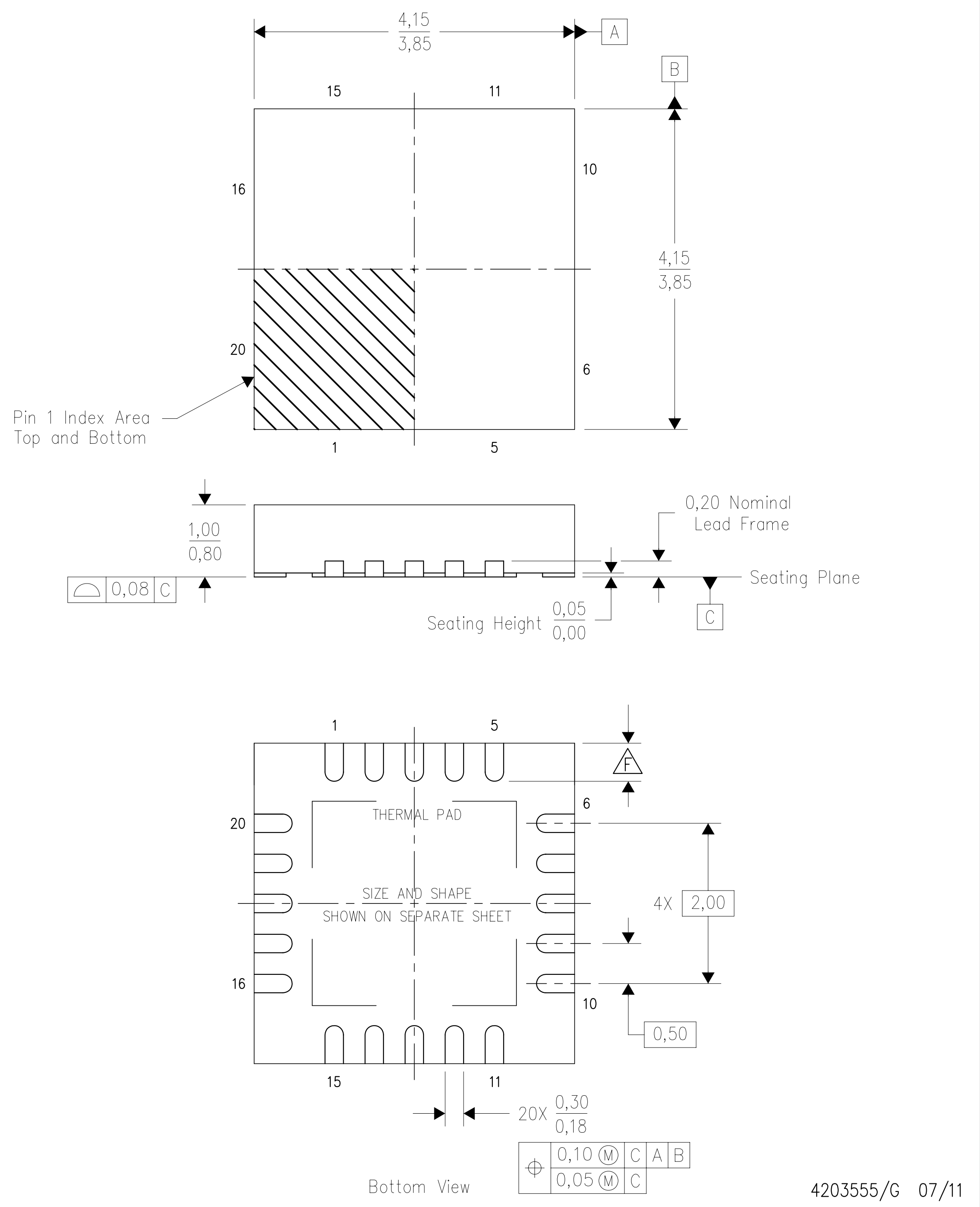
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1100ERGPR	QFN	RGP	20	3000	338.1	338.1	20.6
CC1100ERGPT	QFN	RGP	20	250	338.1	338.1	20.6

RGP (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

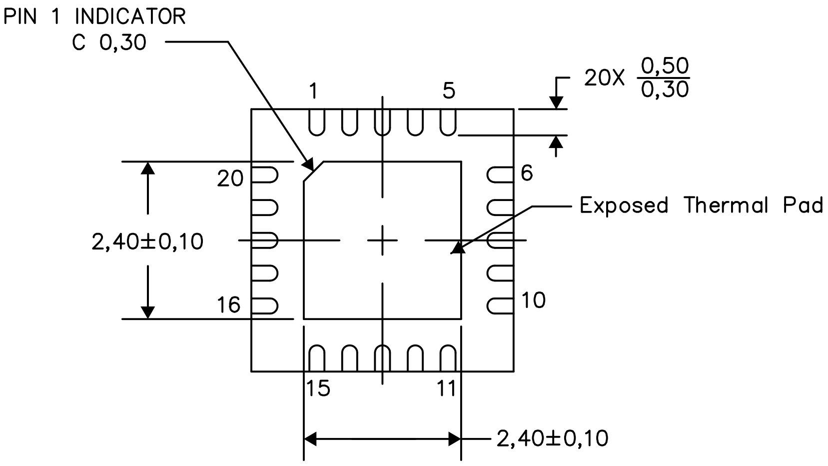
RGP (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206346-7/Y 12/12

NOTES: A. All linear dimensions are in millimeters

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