A Powerful System-On-Chip for 2.4-GHz IEEE 802.15.4, 6LoWPAN and ZigBee Applications

Check for Samples: CC2538

FEATURES

- Microcontroller
  - Powerful ARM Cortex™ M3 With Code Prefetch
  - Up to 32 MHz Clock Speed
  - 512-kB, 256-kB or 128-kB In-System-Programmable Flash
  - Supports On-Chip Over-the-Air Upgrade (OTA)
  - Supports Dual ZigBee Application Profiles
  - Up to 32-kB RAM (16-kB With Retention in All Power Modes)
  - cJTAG and JTAG Debugging
- RF
  - 2.4-GHz IEEE 802.15.4 Compliant RF Transceiver
  - Excellent Receiver Sensitivity of –97 dBm
  - Robustness to Interference With ACR of 44 dB
  - Programmable Output Power Up to 7 dBm
- Security Hardware Acceleration
  - Future Proof AES-128/256, SHA2 Hardware Encryption Engine
  - Optional – ECC-128/256, RSA Hardware Acceration Engine for Secure Key Exchange
  - Radio Command Strobe Processor and Packet Handling Processor for Low-Level MAC Functionality
- Low Power
  - Active-Mode RX (CPU Idle): 20 mA
  - Active-Mode TX at 0 dBm (CPU Idle): 24 mA
  - Power Mode 1 (4-µs Wake-Up, 32 kB RAM retention, full register retention): 0.6 mA
  - Power Mode 2 (Sleep Timer Running, 16-kB RAM Retention, Configuration Register Retention): 1.3 µA
  - Power Mode 3 (External Interrupts, 16-kB RAM Retention, Configuration Register Retention): 0.4 µA
  - Wide Supply-Voltage Range (2 V–3.6 V)
- Peripherals
  - µDMA
  - 4 × General-Purpose Timers (Each 32-Bit or 2 × 16-Bit)
  - 32-Bit 32-kHz Sleep Timer
  - 12-Bit ADC With 8 Channels and Configurable Resolution
  - Battery Monitor and Temperature Sensor
  - USB 2.0 Full-Speed Device (12 Mbps)
  - 2 × SPI
  - 2 × UART
  - I^2C
  - 32 General-Purpose I/O Pins (28 × 4 mA, 4 × 20 mA)
  - Watchdog Timer
- Layout
  - 8-mm × 8-mm QFN56 Package
  - Robust Device for Industrial Operation up to 125°C
  - Few External Components
  - Only a Single Crystal Needed for Asynchronous Networks
- Development Tools
  - CC2538 Development Kit
  - Reference Design Certified Under FCC and ETSI Regulations
  - Full Software Support for ZigBee Smart Energy 1.x, ZigBee Smart Energy 2.0, ZigBee Light Link and ZigBee Home Automation With Sample Applications and Reference Designs Available
  - Code Composer Studio™
  - IAR Embedded Workbench® for ARM
  - SmartRF™ Studio
  - SmartRF™ Flash Programmer

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APPLICATIONS

- **Smart Grid and Home Area Network**
- **Home and Building Automation**
- **Intelligent Lighting Systems**
- **Wireless Sensor Networks**
- **Internet of Things**

DESCRIPTION

The CC2538xFnn is the ideal SoC for high-performance ZigBee applications. It combines a powerful ARM Cortex M3-based MCU system with up to 32K on-chip RAM and up to 512 K on-chip flash with a robust IEEE 802.15.4 radio. This enables it to handle complex network stacks with security, demanding applications, and over-the-air download. Thirty-two GPIOs and serial peripherals enable simple connections to the rest of the board. The powerful security accelerators enable quick and efficient authentication and encryption while leaving the CPU free to handle application tasks. The low-power modes with retention enable quick startup from sleep and minimum energy spent to perform periodic tasks. For a smooth development, the CC2538xFnn includes a powerful debugging system and a comprehensive driver library. To reduce the application flash footprint, CC2538xFnn ROM includes a utility function library and a serial boot loader. Combined with the free to use Z-Stack PRO or ZigBee IP stacks from Texas Instruments, the CC2538 provides the most capable and robust ZigBee solution in the market

Table 1. CC2538 Family of Devices Available

DEVICE	FLASH (kB)	RAM (kB)	SECURITY HW AES/SHA	SECURITY HW ECC/RSA
CC2538SF53	512	32	Yes	Yes
CC2538SF23	256	32	Yes	Yes
CC2538NF53	512	32	Yes	No
CC2538NF23	256	32	Yes	No
CC2538NF11	128	16	Yes	No

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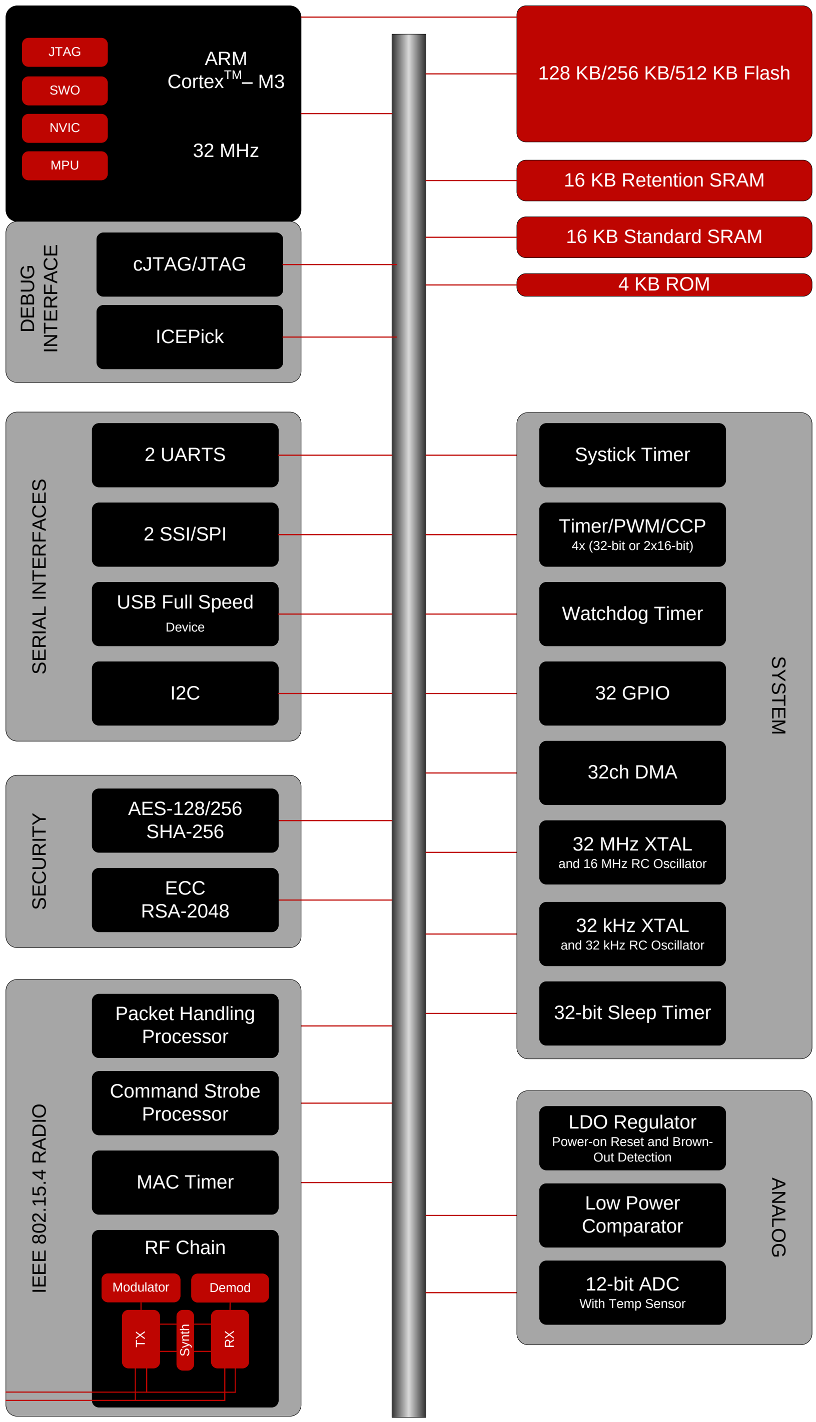
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



For more details about the modules and their usage, see the corresponding chapters in the CC2538 Technical Reference Manual (SWRU319).

ABSOLUTE MAXIMUM RATINGS(1)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.9	V
Voltage on any digital pin		–0.3	V_{DD} + 0.3, ≤ 3.9	V
Input RF level			10	dBm
Storage temperature range		–40	125	°C
ESD(2)	All pads, according to human-body model, JEDEC STD 22, method A114		1	kV
	According to charged-device model, JEDEC STD 22, method C101		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) CAUTION: ESD-sensitive device. Precautions should be used when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Operating ambient temperature range, T_A	–40	125	°C
Operating supply voltage (1)	2	3.6	V

(1) The CC2538 contains a power on reset (POR) module and a brown out detector (BOD) that prevent the device from operating under unsafe supply voltage conditions. In the two lowest power modes, PM2 and PM3, the POR is active but the BOD is powered down, which gives a limited voltage supervision.
If the supply voltage is lowered to below 1.4 V during PM2/PM3, at temperatures of 70°C or higher, and then brought back up to good operating voltage before active mode is re-entered, registers and RAM contents that are saved in PM2, PM3 may become altered. Hence, care should be taken in the design of the system power supply to ensure that this does not occur. The voltage can be periodically supervised accurately by entering active mode, as a BOD reset is triggered if the supply voltage is below approximately 1.7 V.

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ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V, and 8-MHz system clock, unless otherwise noted.
Boldface limits apply over the entire operating range, T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	Digital regulator on. 16-MHz RCOSC running. No radio, crystals, or peripherals active. CPU running at 16-MHz with flash access		7		mA
		32-MHz XOSC running. No radio or peripherals active. CPU running at 32-MHz with flash access,.		13		mA
		32-MHz XOSC running, radio in RX mode, –50-dBm input power, no peripherals active, CPU idle		20		mA
		32-MHz XOSC running, radio in RX mode at –100-dBm input power (waiting for signal), no peripherals active, CPU idle		24	27	mA
		32-MHz XOSC running, radio in TX mode, 0-dBm output power, no peripherals active, CPU idle		24		mA
		32-MHz XOSC running, radio in TX mode, 7-dBm output power, no peripherals active, CPU idle		34		mA
		Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		0.6		mA
		Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		1.3	2	µA
		Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.4	1	µA
I_{peri}	**Peripheral Current Consumption** (Adds to core current I_{core} for each peripheral unit activated)					
	General-purpose timer	Timer running, 32-MHz XOSC used		120		µA
	SPI			300		µA
	I^2C			0.1		mA
	UART			0.7		mA
	Sleep timer	Including 32.753-kHz RCOSC		0.9		µA
	USB	48-MHz clock running, USB enabled		3.8		mA
	ADC	When converting		1.2		mA
	Flash	Erase		12		mA
		Burst-write peak current		8		mA

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC		4		µs
Power mode 2 or 3 → active	Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC		136		µs
Active → TX or RX	Initially running on 16-MHz RCOSC, with 32-MHz XOSC off		0.5		ms
	With 32-MHz XOSC initially on			192	µs
RX/TX and TX/RX turnaround				192	µs
USB PLL start-up time	With 32-MHz XOSC initially on		32		µs
RADIO PART					
RF frequency range	Programmable in 1-MHz steps, 5 MHz between channels for compliance with [1]	2394		2507	MHz
Radio baud rate	As defined by [1]		250		kbps
Radio chip rate	As defined by [1]		2		MChip/s
FLASH MEMORY					
Flash erase cycles				20	k Cycles
Flash page size			2		kB

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RF RECEIVE SECTION

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V, and f_c = 2440 MHz, unless otherwise noted.
Bold limits apply over the entire operating range, T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%, as specified by [1], normal operating conditions (25°C, 3V, 2440 MHz) [1] requires –85 dBm		–97	–92	dBm
	PER = 1%, as specified by [1], entire operating conditions [1] requires –85 dBm			**–88**	dBm
Saturation (maximum input level)	PER = 1%, as specified by [1] [1] requires –20 dBm		10		dBm
Adjacent-channel rejection, 5-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at 5 MHz, PER = 1%, as specified by [1]. [1] requires 0 dB		44		dB
Adjacent-channel rejection, –5-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at –5 MHz, PER = 1%, as specified by [1]. [1] requires 0 dB		44		dB
Alternate-channel rejection, 10-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at 10 MHz, PER = 1%, as specified by [1] [1] requires 30 dB		52		dB
Alternate-channel rejection, –10-MHz channel spacing	Wanted signal –82 dBm, adjacent modulated channel at –10 MHz, PER = 1%, as specified by [1] [1] requires 30 dB		52		dB
Channel rejection ≥ 20 MHz ≤ –20 MHz	Wanted signal at –82 dBm. Undesired signal is an IEEE 802.15.4 modulated channel, stepped through all channels from 2405 to 2480 MHz. Signal level for PER = 1%.		 51 51		dB
Blocking/desensitization 5 MHz from band edge 10 MHz from band edge 20 MHz from band edge 50 MHz from band edge –5 MHz from band edge –10 MHz from band edge –20 MHz from band edge –50 MHz from band edge	Wanted signal 3 dB above the sensitivity level, CW jammer, PER = 1%. Measured according to EN 300 440 class 2.		 –35 –34 –37 –32 –37 –38 –35 –34		dBm
Spurious emission. Only largest spurious emission stated within each band. 30 MHz–1000 MHz 1 GHz–12.75 GHz	Conducted measurement with a 50-Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47 Part 15, and ARIB STD-T-66.		 –80 –80		dBm
Frequency error tolerance (1)	[1] requires minimum 80 ppm		±150		ppm
Symbol rate error tolerance (2)	[1] requires minimum 80 ppm		±1000		ppm

(1) Difference between center frequency of the received RF signal and local oscillator frequency
(2) Difference between incoming symbol rate and the internally generated symbol rate

RF TRANSMIT SECTION

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz, unless otherwise noted.
Boldface limits apply over the entire operating range, T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, and f_c = 2394 MHz to 2507 MHz.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Nominal output power	Delivered to a single-ended 50-Ω load through a balun using maximum-recommended output-power setting [1] requires minimum –3 dBm		7		dBm
Programmable output-power range			30		dB
Spurious emissions Only largest spurious emission stated within each band.	Maximum recommended output power setting(1) Measured according to stated regulations. 25 MHz–1000 MHz (outside restricted bands) 25 MHz–1000 MHz (within FCC restricted bands) 25 MHz–1000 MHz (within ETSI restricted bands) 1800–1900 MHz (ETSI restricted band) 5150–5300 MHz (ETSI restricted band) 1 GHz–12.75 GHz (except restricted bands) At 2483.5 MHz and above (FCC restricted band), f_c= 2480 MHz(2)		 –56 –58 –58 –60 –54 –51 –42		dBm
Error vector magnitude (EVM)	Measured as defined by [1] using maximum-recommended output-power setting [1] requires maximum 35%.		3%		
Optimum load impedance	Differential impedance on the RF pins		66 + j64		Ω

(1) Texas Instruments CC2538 EM reference design is suitable for systems targeting compliance with EN 300 328, EN 300 440, FCC CFR47 Part 15, and ARIB STD-T-66.
(2) To improve margins for passing FCC requirements at 2483.5 MHz and above when transmitting at 2480 MHz, use a lower output-power setting or less than 100% duty cycle.

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32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32		MHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance		6	16	60	Ω
C_0	Crystal shunt capacitance		1	1.9	7	pF
C_L	Crystal load capacitance		10	13	16	pF
	Start-up time			0.3		ms
	Power-down guard time	The crystal oscillator must be in power down for a guard time before using it again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by [1]

32.768-kHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32.768		kHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance			40	130	Ω
C_0	Crystal shunt capacitance			0.9	2	pF
C_L	Crystal load capacitance			12	16	pF
	Start-up time			0.4		s

(1) Including aging and temperature dependency, as specified by [1]

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency(1)			32.753		kHz
Frequency accuracy after calibration			±0.2%		
Temperature coefficient(2)			0.4		%/°C
Supply-voltage coefficient(3)			3		%/V
Calibration time(4)			2		ms

(1) The calibrated 32-kHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 977.
(2) Frequency drift when temperature changes after calibration
(3) Frequency drift when supply voltage changes after calibration
(4) When the 32-kHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC32K_CALDIS is 0.***

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency(1)			16		MHz
Uncalibrated frequency accuracy			±18%		
Calibrated frequency accuracy			±0.6%	±1%	
Start-up time				10	μs
Initial calibration time(2)			50		μs

(1) The calibrated 16-MHz RC oscillator frequency is the 32-MHz XTAL frequency divided by 2.
(2) When the 16-MHz RC oscillator is enabled, it is calibrated when a switch from the 16-MHz RC oscillator to the 32-MHz crystal oscillator is performed while SLEEPCMD.OSC_PD is set to 0.***

RSSI/CCA CHARACTERISTICS

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RSSI range			100		dB
Absolute uncalibrated RSSI/CCA accuracy			±4		dB
RSSI/CCA offset(1)			73		dB
Step size (LSB value)			1		dB

(1) Real RSSI = Register value – offset

FREQEST CHARACTERISTICS

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQEST range			±250		kHz
FREQEST accuracy			±10		kHz
FREQEST offset(1)			15		kHz
Step size (LSB value)			7.8		kHz

(1) Real FREQEST = Register value – offset

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C, V_{DD} = 3 V and f_c = 2440 MHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At ±1-MHz offset from carrier		–111		dBc/Hz
	At ±2-MHz offset from carrier		–119		
	At ±5-MHz offset from carrier		–126		

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2538 EM reference design with T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output at 25°C	Measured using integrated ADC, using internal band-gap voltage reference and maximum resolution		1422		12-bit ADC
Temperature coefficient			4.2		/1°C
Voltage coefficient			1		/0.1 V
Initial accuracy without calibration			±10		°C
Accuracy using 1-point calibration (entire temperature range)			±5		°C
Current consumption when enabled (ADC current not included)			0.3		mA

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ADC CHARACTERISTICS

T_A = 25°C and V_{DD} = 3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	V_{DD} is voltage on AVDD5 pin	0		V_{DD}	V
	External reference voltage	V_{DD} is voltage on AVDD5 pin	0		V_{DD}	V
	External reference voltage differential	V_{DD} is voltage on AVDD5 pin	0		V_{DD}	V
	Input resistance, signal	Using 4-MHz clock speed		197		kΩ
	Full-scale signal (1)	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB (1)	Effective number of bits	Single-ended input, 7-bit setting		5.7		Bits
		Single-ended input, 9-bit setting		7.5		
		Single-ended input, 10-bit setting		9.3		
		Single-ended input, 12-bit setting		10.8		
		Differential input, 7-bit setting		6.5		
		Differential input, 9-bit setting		8.3		
		Differential input, 10-bit setting		10.0		
		Differential input, 12-bit setting		11.5		
	Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD (1)	Total harmonic distortion	Single-ended input, 12-bit setting, –6 dBFS		–75.2		dB
		Differential input, 12-bit setting, –6 dBFS		–86.6		
	Signal to nonharmonic ratio (1)	Single-ended input, 12-bit setting		70.2		dB
		Differential input, 12-bit setting		79.3		
		Single-ended input, 12-bit setting, –6 dBFS		78.8		
		Differential input, 12-bit setting, –6 dBFS		88.9		
CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		>84		dB
	Crosstalk	Single-ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution		< – 84		dB
	Offset	Midscale		–3		mV
	Gain error			0.68%		
DNL (1)	Differential nonlinearity	12-bit setting, mean		0.05		LSB
		12-bit setting, maximum		0.9		
INL (1)	Integral nonlinearity	12-bit setting, mean		4.6		LSB
		12-bit setting, maximum		13.3		
SINAD (1) (–THD+N)	Signal-to-noise-and-distortion	Single-ended input, 7-bit setting		35.4		dB
		Single-ended input, 9-bit setting		46.8		
		Single-ended input, 10-bit setting		57.5		
		Single-ended input, 12-bit setting		66.6		
		Differential input, 7-bit setting		40.7		
		Differential input, 9-bit setting		51.6		
		Differential input, 10-bit setting		61.8		
		Differential input, 12-bit setting		70.8		
	Conversion time	7-bit setting		20		μs
		9-bit setting		36		
		10-bit setting		68		
		12-bit setting		132		
	Current consumption			1.2		mA
	Internal reference voltage			1.19		V
	Internal reference VDD coefficient			2		mV/V
	Internal reference temperature coefficient			0.4		mV/10°C

(1) Measured with 300-Hz sine-wave input and VDD as reference

CONTROL INPUT AC CHARACTERISTICS

T_A = –40°C to 125°C, V_{DD} = 2 V to 3.6 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSCLK} $t_{SYSCLK} = 1/f_{SYSCLK}$	The undivided system clock is 32 MHz when crystal oscillator is used. The undivided system clock is 16 MHz when calibrated 16-MHz RC oscillator is used.	16		32	MHz
RESET_N low duration	See item 1, Figure 1. This is the shortest pulse that is recognized as a complete reset pin request. Note that shorter pulses may be recognized but might not lead to complete reset of all modules within the chip.	1			µs
Interrupt pulse duration	See item 2, Figure 1.This is the shortest pulse that is recognized as an interrupt request.	20			ns

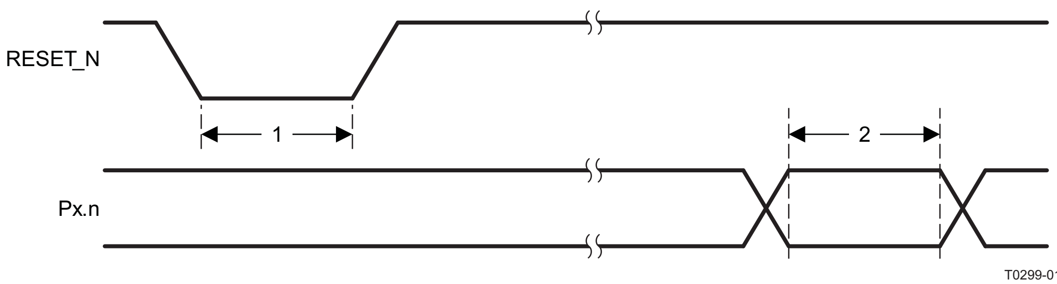

Figure 1. Control Input AC Characteristics

DC CHARACTERISTICS

T_A = 25°C, VDD = 3 V, drive strength set to high with CC_TESTCTRL.SC = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.5			V
Logic-0 input current	Input equals 0 V	–300		300	nA
Logic-1 input current	Input equals V_{DD}	–300		300	nA
I/O-pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage, 4-mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4-mA pins	Output load 4 mA	2.4			V
Logic-0 output voltage, 20-mA pins	Output load 20 mA			0.5	V
Logic-1 output voltage, 20-mA pins	Output load 20 mA	2.4			V

USB INTERFACE DC CHARACTERISTICS

T_A = 25°C, V_{DD} = 3 V to 3.6 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB pad voltage output, high	VDD 3.6 V, 4-mA load		3.4		V
USB pad voltage output, low	VDD 3.6 V, 4-mA load		0.2		V

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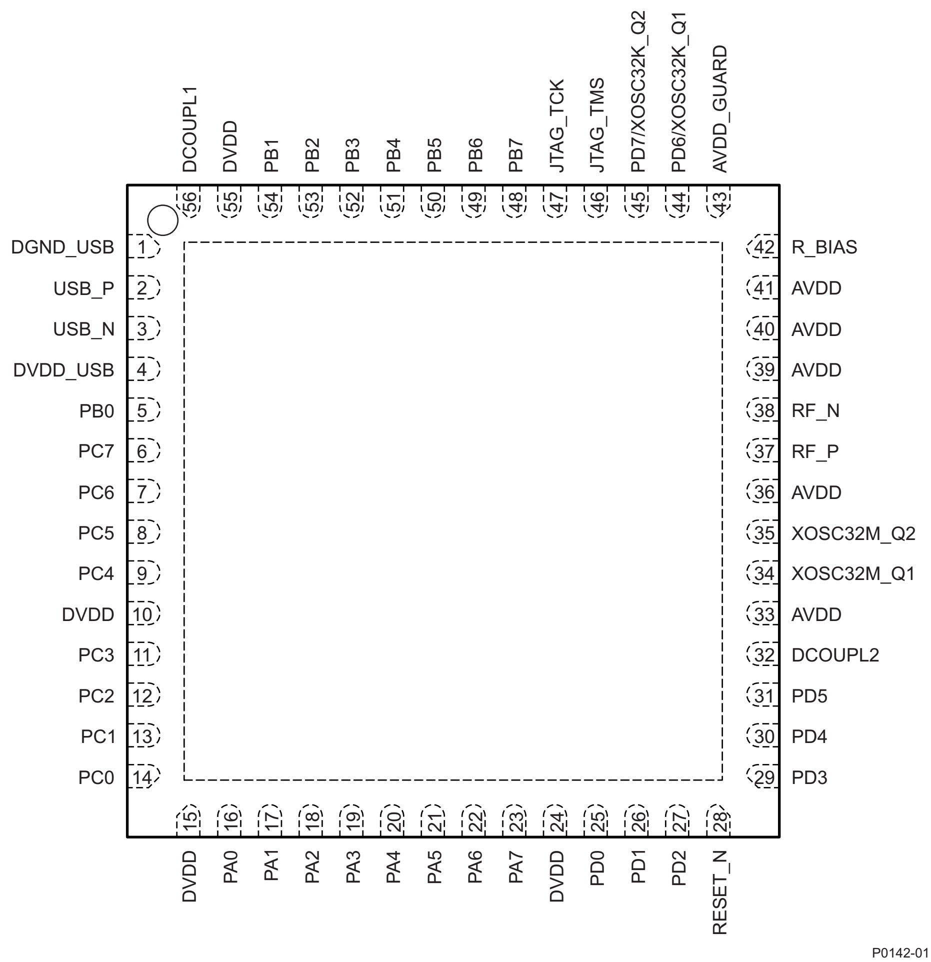
DEVICE INFORMATION



NOTE: Connect the exposed ground pad to a solid ground plane, as this is the ground connection for the chip.

Pin Descriptions

PIN NAME	PIN	PIN TYPE	DESCRIPTION
AVDD	33, 36, 39, 40, 41	Power (analog)	2-V–3.6-V analog power-supply connection
AVDD_GUARD	43	Power (analog)	2-V–3.6-V analog power-supply connection
DCOUPL1	56	Power (digital)	1.8-V regulated digital-supply decoupling capacitor
DCOUPL2	32	Power (digital)	1.8-V regulated digital-supply decoupling capacitor. Short this pin to pin 56.
DGND_USB	1	Ground (USB pads)	USB ground
DVDD	10, 15, 24, 55	Power (digital)	2-V–3.6-V digital power-supply connection
DVDD_USB	4	Power (USB pads)	3.3-V USB power-supply connection
JTAG_TCK	47	Digital I/O	JTAG TCK
JTAG_TMS	46	Digital I/O	JTAG TMS
PA0	16	Digital/analog I/O	GPIO port A pin 0. ROM bootloader UART RXD
PA1	17	Digital/analog I/O	GPIO port A pin 1. ROM bootloader UART TXD
PA2	18	Digital/analog I/O	GPIO port A pin 2. ROM bootloader SSI CLK
PA3	19	Digital/analog I/O	GPIO port A pin 3. ROM bootloader SSI SEL

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Pin Descriptions (continued)

PIN NAME	PIN	PIN TYPE	DESCRIPTION
PA4	20	Digital/analog I/O	GPIO port A pin 4. ROM bootloader SSI RXD
PA5	21	Digital/analog I/O	GPIO port A pin 5. ROM bootloader SSI TXD
PA6	22	Digital/analog I/O	GPIO port A pin 6
PA7	23	Digital/analog I/O	GPIO port A pin 7
PB0	5	Digital I/O	GPIO port B pin 0
PB1	54	Digital I/O	GPIO port B pin 1
PB2	53	Digital I/O	GPIO port B pin 2
PB3	52	Digital I/O	GPIO port B pin 3
PB4	51	Digital I/O	GPIO port B pin 4
PB5	50	Digital I/O	GPIO port B pin 5
PB6	49	Digital I/O	GPIO port B pin 6, TDI (JTAG)
PB7	48	Digital I/O	GPIO port B pin 7, TDO (JTAG)
PC0	14	Digital I/O	GPIO port C pin 0, 20 mA output capability, no pull-up or pull-down
PC1	13	Digital I/O	GPIO port C pin 1, 20 mA output capability, no pull-up or pull-down
PC2	12	Digital I/O	GPIO port C pin 2, 20 mA output capability, no pull-up or pull-down
PC3	11	Digital I/O	GPIO port C pin 3, 20 mA output capability, no pull-up or pull-down
PC4	9	Digital I/O	GPIO port C pin 4
PC5	8	Digital I/O	GPIO port C pin 5
PC6	7	Digital I/O	GPIO port C pin 6
PC7	6	Digital I/O	GPIO port C pin 7
PD0	25	Digital I/O	GPIO port D pin 0
PD1	26	Digital I/O	GPIO port D pin 1
PD2	27	Digital I/O	GPIO port D pin 2
PD3	29	Digital I/O	GPIO port D pin 3
PD4	30	Digital I/O	GPIO port D pin 4
PD5	31	Digital I/O	GPIO port D pin 5
PD6/XOSC32K_Q1	44	Digital/analog I/O	GPIO port D pin 6 / 32-kHz crystal oscillator pin 1
PD7/XOSC32K_Q2	45	Digital/analog I/O	GPIO port D pin 7 / 32-kHz crystal oscillator pin 1
R_BIAS	42	Analog I/O	External precision bias resistor for reference current
RESET_N	28	Digital input	Reset, active-low
RF_N	38	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	37	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
USB_P	2	USB I/O	USB differential data plus (D+)
USB_N	3	USB I/O	USB differential data minus (D–)
XOSC32M_Q1	34	Analog I/O	32-MHz crystal oscillator pin 1 or external-clock input
XOSC32M_Q2	35	Analog I/O	32-MHz crystal oscillator pin 2

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APPLICATION INFORMATION

Few external components are required for the operation of the CC2538xFnn. Figure 2 is a typical application circuit. For a complete USB reference design, see the CC2538xFnn product page on www.ti.com. Table 2 lists typical values and descriptions of external components. The USB_P and USB_N pins require series resistors R21 and R31 for impedance matching, and the D+ line must have a pullup resistor, R32. The series resistors should match the 90-Ω ±15% characteristic impedance of the USB bus. Notice that the pullup resistor and DVDD_USB require connection to a voltage source between 3 V and 3.6 V (typically 3.3 V). To accomplish this, it is recommend to connect the D+ pull-up to a port/pin that does not have an internal pull-up (that is, PC0..3), instead of connecting it directly to a 3.3V supply (that is, software control of D+ pull-up recommended).

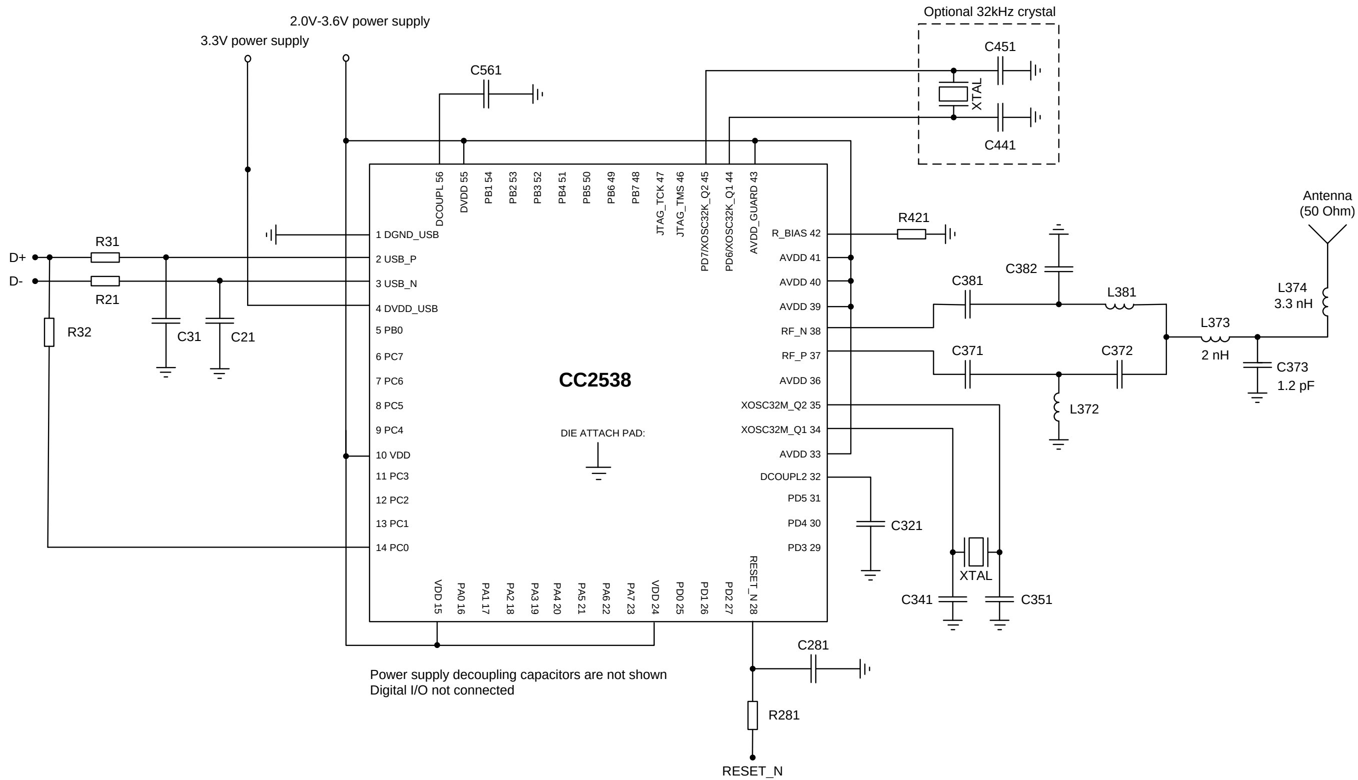

Figure 2. CC2538xFnn Application Circuit

Table 2. Overview of External Components (Excluding Supply Decoupling Capacitors)

Component	Description	Value
C21	USB D– decoupling	47 pF
C31	USB D+ decoupling	47 pF
C341	32-MHz xtal-loading capacitor	12 pF
C351	32-MHz xtal-loading capacitor	12 pF
C371	Part of the RF matching network	18 pF
C381	Part of the RF matching network	18 pF
C382	Part of the RF matching network	1 pF
C372	Part of the RF matching network	1 pF
C441	32-kHz xtal-loading capacitor	22 pF
C451	32-kHz xtal-loading capacitor	22 pF
C561	Decoupling capacitor for the internal digital regulator	1 µF
C321	Decoupling capacitor for the internal digital regulator	1 µF
C281	Filter capacitor for reset line	1 nF
L372	Part of the RF matching network	2 nH
L381	Part of the RF matching network	2 nH
R21	USB D– series resistor	33 Ω
R31	USB D+ series resistor	33 Ω
R32	USB D+ pullup resistor to signal full-speed device presence	1.5 kΩ
R281	Filter resistor for reset line	2.2 Ω
R421	Resistor used for internal biasing	56 kΩ

Input, Output Matching

When using an unbalanced antenna such as a monopole, use a balun to optimize performance. One can implement the balun using low-cost discrete inductors and capacitors. The recommended balun shown consists of L372, C372, C382 and L381.

If a balanced antenna such as a folded dipole is used, omit the balun.

Crystal

The 32-MHz crystal oscillator uses an external 32-MHz crystal, XTAL1, with two loading capacitors (C341 and C351). See the *32-MHz Crystal Oscillator* section for details. Calculate the load capacitance across the 32-MHz crystal by:

$$C_L = \frac{1}{\frac{1}{C_{341}} + \frac{1}{C_{351}}} + C_{parasitic} \tag{1}$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C441 and C451) used for the 32.768-kHz crystal oscillator. Use the 32.768-kHz crystal oscillator in applications where both low sleep-current consumption and accurate wake-up times are needed. Calculate the load capacitance across the 32.768-kHz crystal by:

$$C_L = \frac{1}{\frac{1}{C_{441}} + \frac{1}{C_{451}}} + C_{parasitic} \tag{2}$$

Use a series resistor, if necessary, to comply with the ESR requirement.

On-Chip 1.8-V Voltage-Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires decoupling capacitors (C561, C321) and an external connection between them for stable operation.

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Power-Supply Decoupling and Filtering

Optimum performance requires proper power-supply decoupling. The placement and size of the decoupling capacitors and the power supply filtering are important to achieve the best performance in an application. TI provides a recommended compact reference design for the user to follow.

References

1. IEEE Std. 802.15.4-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

   http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf
2. CC2538xFnn User's Guide
3. Universal Serial Bus Revision 2.0 Specification http://www.usb.org/developers/docs/usb_20_052709.zip

Additional Information

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REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed the Product Preview device	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CC2538SF53RTQR	ACTIVE	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		CC2538SF53	Samples
CC2538SF53RTQT	ACTIVE	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		CC2538SF53	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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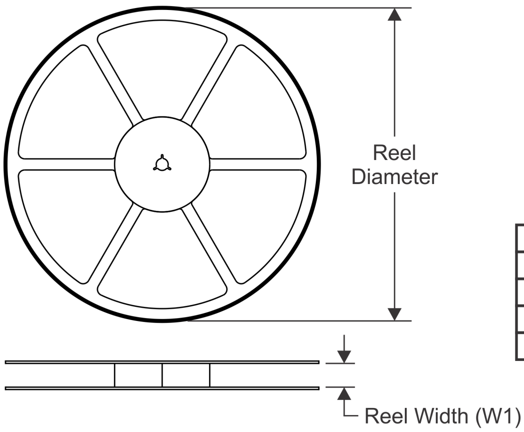
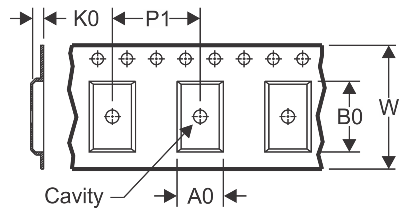
REEL DIMENSIONS

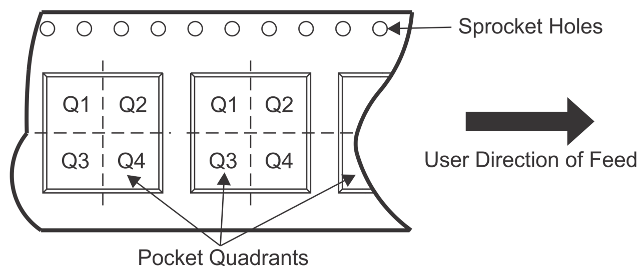


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

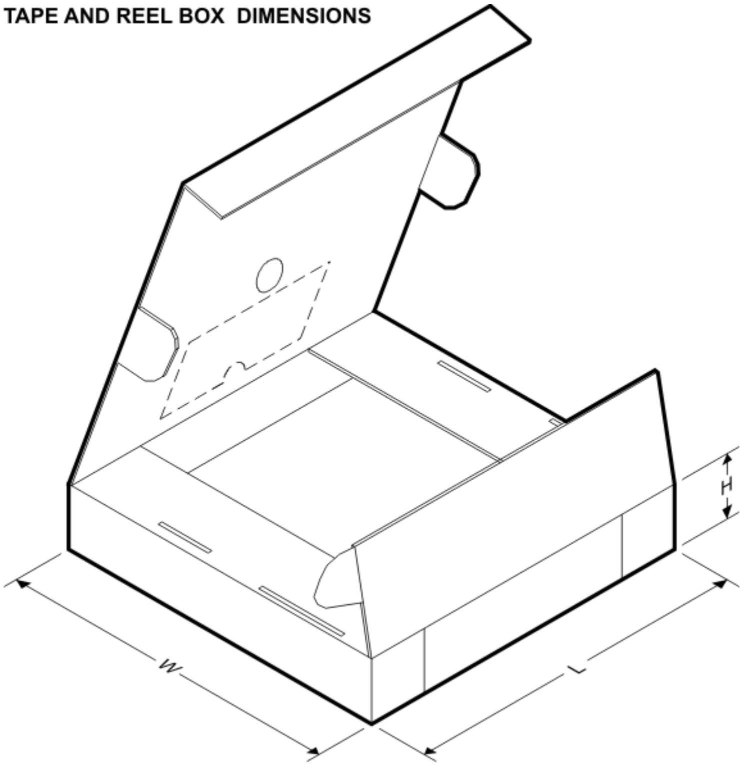
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2538SF53RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
CC2538SF53RTQT	QFN	RTQ	56	250	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

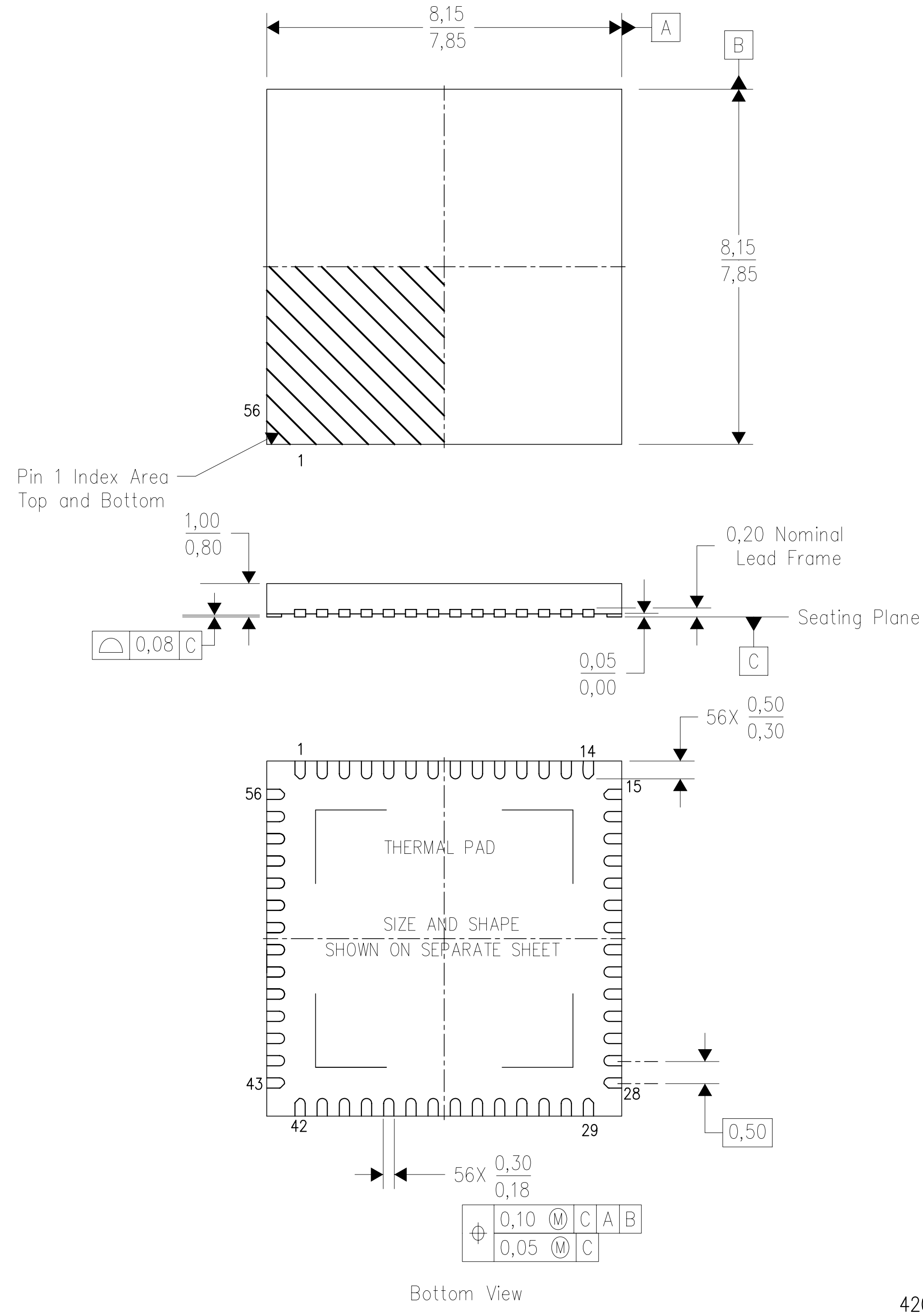
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2538SF53RTQR	QFN	RTQ	56	2000	336.6	336.6	28.6
CC2538SF53RTQT	QFN	RTQ	56	250	336.6	336.6	28.6

RTQ (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD



4206089/D 08/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

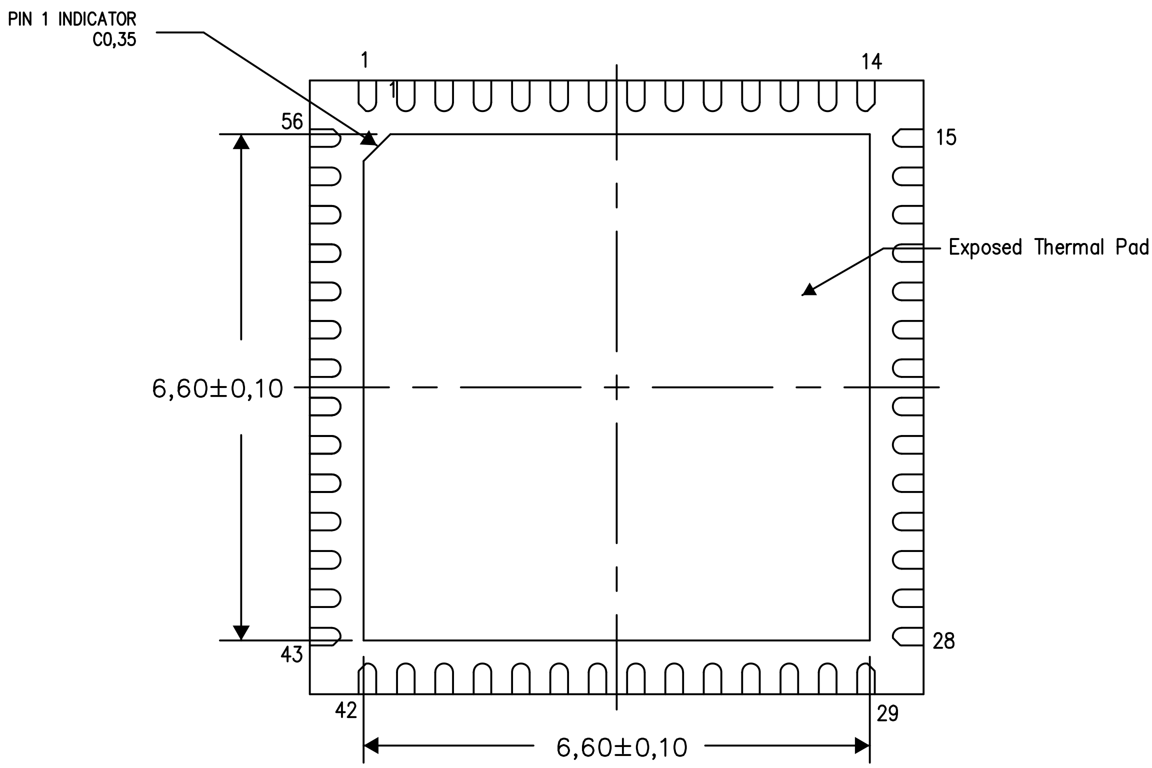
RTQ (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206252-7/M 07/12

NOTE: A. All linear dimensions are in millimeters

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